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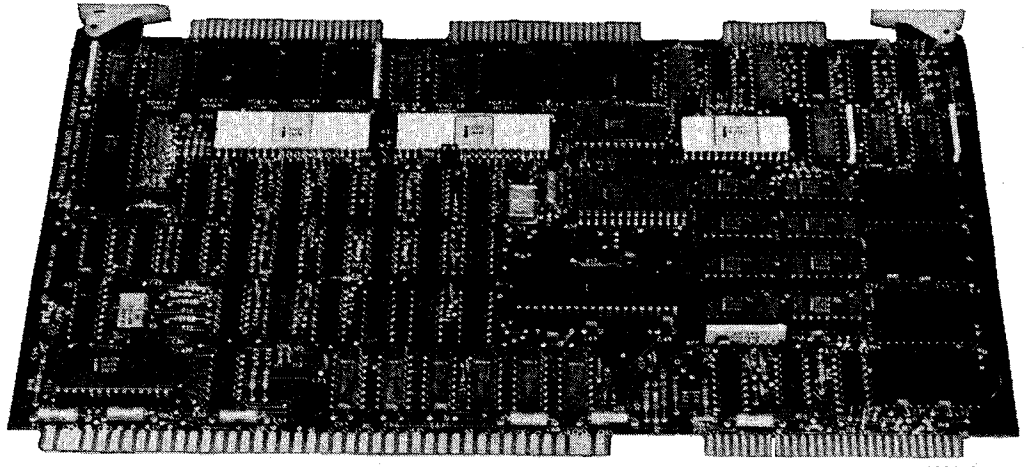
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iSBC® 80/20-4
SINGLE BOARD COMPUTER

- **8080A CPU Used as Central Processor**
- **4K Bytes of Static Read/Write Memory**
- **Sockets for up to 8K Bytes of Erasable Reprogrammable or Masked Read Only Memory**
- **48 Programmable Parallel I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Fully Software Selectable Baud Rate Generation**
- **Full MULTIBUS® Control Logic Allowing up to 16 Masters to Share System Bus**
- **Two Programmable 16-bit BCD and Binary Timers**
- **Eight-Level Programmable Interrupt Control**
- **Compatible with Optional Memory and I/O Expansion Boards**
- **Auxiliary Power Bus, Memory Protect, and Power-Fail Interrupt Control Logic Provided for Battery Backup RAM Requirements**

The iSBC 80/20-4 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. Each iSBC 80/20-4 is a complete computer system on a single 6.75 × 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic, two programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on each board.



280218-1

September 1987
Order Number: 280218-002

FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/20-4. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. Minimum instruction execution time is 1.86 microseconds. A block diagram of iSBC 80/20-4 functional components is shown in Figure 1.

Memory Addressing

The 8080A has a 16-bit program counter which allows direct addressing of up to 65,536 bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/20-4 contains 4K bytes of static read/write memory using Intel low power static RAMs. All on-board RAM read and write operations are performed at maximum processor speed. Power for on-board RAM memory is provided on an auxiliary power bus, and memory protect logic is included for battery backup RAM requirements. Sockets for up to 8K bytes of nonvolatile read only memory are provided on the board. Read only memory may be added in 1K byte increments using Intel 2708 erasable and electrically reprogrammable ROMs (EPROMs), or read only memory may be added in 2K byte increments using Intel 2716 EPROMs. All on-board ROM read operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/20-4 contains 48 programmable parallel I/O lines implemented using two Intel 8255 programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of the unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, woven, or round cable.

Serial I/O Interface

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 80/20-4 board. A software selectable baud

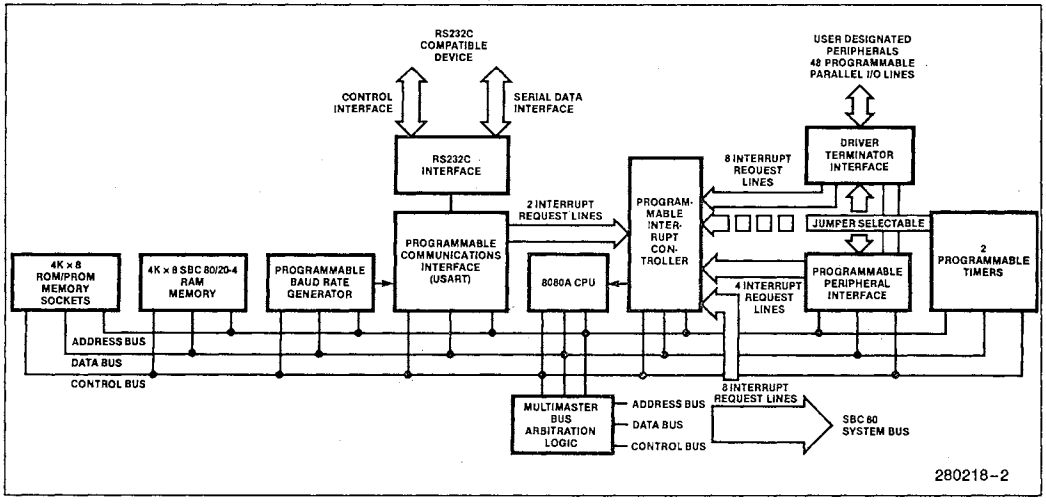


Figure 1. iSBC® 80/20 and iSBC® 80/20-4 Block Diagram Showing Functional Components

rate generator provides the USART with all common communications frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character parity, and baud rate are all under program control. The 8251 provides full duplex, double-buffered transmit and recieve capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable.

Multimaster Capability

The iSBC 80/20-4 is a full computer on a single board with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the system bus), the iSBC 80/20-4 provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/20-4 or high speed controllers to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters may share the system bus with the addition of an external priority network. Once bus control is attained, a bus bandwidth of up to 5M bytes/sec may be achieved.

The bus controller provides its own clock which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data words per second. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct-memory-access (DMA) operations and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/20-4 board provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing of these counters is jumper selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X(1)
	4	X		X			X(1)
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X(2)
	4	X		X			X(2)

NOTES:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

and terminators, or outputs from the 8255 programmable peripheral interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 80/20-4 RS232C USART serial port. In utilizing the iSBC 80/20-4, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly."

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Interrupt Capability

Operation and Priority Assignments—An Intel 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage via software, of a single byte to the interrupt register of the PIC.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until the next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Interrupt Addressing—The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8080 jump instruction at each of these addressed then provides linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation—Interrupt requests may originate from 26 sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt

requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and eight interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Power-Fail Control—Control logic is also included for generation of a power-fail interrupt which works in conjunction with the AC-low signal from iSBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. High speed integer and floating-point arithmetic capabilities may be added by using the iSBC 310A High Speed Mathematics Unit. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as subsystems. Modular expandable backplanes and cardcages are available to support multiboard systems.

SPECIFICATIONS

Word Size

Instruction: 8, 16, or 24 bits
Data: 8 bits

Cycle Time

Basic Instruction Cycle: 1.86 μs

NOTE:
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM—0-0FFF (2708) or 0-1FFF (2716)

On-Board RAM—4K bytes ending on a 16K boundary (e.g., $3FFF_H$, $7FFF_H$, $BFFF_H$, ... $FFFF_H$)

Memory Capacity

On-Board ROM/EPROM—8K bytes (sockets only)

On-Board RAM—4K bytes

Off-Board Expansion—Up to 65,536 bytes in user specified RAM, ROM, and EPROM

NOTE:
ROM/EPROM may be added in 1K or 2K-byte increments.

I/O Addressing

On-Board Programmable I/O (see Table 1)

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel—48 programmable lines (see Table 1)

NOTE:
Expansion to 504 input and 504 output lines can be accomplished using optional I/O boards.

Serial Communications Characteristics

Synchronous—5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous—5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		+ 16	+ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Register Address (hex notation, I/O address space)

DE Baud rate register

NOTE:
Baud rate factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

Interrupts

Register Addresses (hex notation, I/O address space)

DA Interrupt request register
DA In-service register
DB Mask register
DA Command register
DB Block address register
DA Status (polling register)

NOTE:
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Timers

Register Addresses (hex notation, I/O address space)

DF Control register
DC Timer 1
DD Timer 2

NOTE:
Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference	Event Rate
1.0752 MHz ±10% (0.930 μs period, nominal)	1.1 MHz max

NOTE:
Maximum rate for external events in event counter function.

Interfaces

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Interrupt Requests: All TTL compatible
Timer: All signals compatible
Serial I/O: RS232C compatible, data set configuration

System Clock (8080A CPU)

2.1504 MHz ±0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selections of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors*
MULTIBUS System Bus	86	0.156	ELFAB BS1562043PBB Viking 2KH43/9AMK12 Soldered PCB Mount EDAC 337086540201 ELFAB BW1562D43PBB EDAC 337086540202 ELFAB BW1562A43PBB Wire Wrap
Auxiliary Bus	60	0.100	EDAC 345060524802 ELFAB BS1020A30PBB EDAC 345060540201 ELFAB BW1020D30PBB Wire Wrap
Parallel I/O (2)	50	0.100	3M 3415-001 Flat Crimp GTE Sylvania 6AD01251A1DD Soldered
Serial I/O	26	0.100	AMP 15837151 EDAC 345026520202 PCB Soldered 3M 3462-0001 AMP 88373-5 Flat Crimp

NOTE:
*Connectors compatible with those listed may also be used.

Line Drivers and Terminators

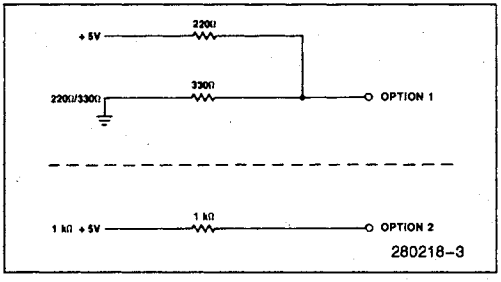
I/O Drivers—The following line drivers are all compatible with the I/O driver sockets on the ISBC 80/20-4.

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 20 mA totem-pole bidirectional drivers and 1 kΩ terminators.

I/O Terminators—220Ω/330Ω divider or 1 kΩ pull-up



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.86 μs	60.948 ms	3.72 μs	1.109 hr
Programmable One-Shot	1.86 μs	60.948 ms	3.72 μs	1.109 hr
Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-Wave Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.31 kHz
Software Triggered Strobe	1.86 μs	60.948 ms	3.72 μs	1.109 hr
Hardware Triggered Strobe	1.86 μs	60.948 ms	3.72 μs	1.109 hr

Physical Characteristics

Width: 12.00 in. (30.48 cm)

Height: 6.75 in. (17.15 cm)

Depth: 0.50 in. (1.26 cm)

Weight: 14 oz. (397.6 gm)

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Reference Manual

9800317D—iSBC 80/20-5 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 80/20-4	Single Board Computer with 4K bytes RAM

Electrical Characteristics

DC POWER REQUIREMENTS

Voltage (±5%)	Without PROM(1) (max)	With 4K PROM(2) (max)	With iSBC 530(3) (max)	RAM Only(4) (max)	With 8K PROM(5) (max)
V_{CC} = +5V	I_{CC} = 4.0A	4.9A	4.9A	1.1A	5.2A
V_{DD} = +12V	I_{DD} = 90 mA	350 mA	450 mA	—	90 mA
V_{BB} = −5V	I_{BB} = 2 mA	180 mA	180 mA	—	2 mA
V_{AA} = −12V	I_{AA} = 20 mA	20 mA	120 mA	—	20 mA

NOTES:
1. Does not include power required for optional PROM, I/O drivers, and I/O terminators.
2. With four 2708 EPROMs and 220Ω/330Ω input terminators installed for 32 I/O lines, all terminator inputs low.
3. With four 2708 EPROMs, 220Ω/330Ω input terminators installed for 32 I/O lines, all terminator inputs low, and iSBC 530 Teletypewriter Adapter drawing power from serial port connector.
4. RAM chips powered via auxiliary power bus.
5. With four 8716 EPROMs and eight 220Ω/330Ω input terminators installed, all terminator inputs low.

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