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Intel® FPGA Download Cable II User Guide

Online Version
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1. Setting Up the Intel® FPGA Download Cable II

Attention: The download cable name has changed to Intel® FPGA Download Cable II. Some file names may still refer to USB-Blaster II.

Attention: Unless otherwise stated, any usage of the terms 'cable' or 'download cable' shall specifically refer to the Intel FPGA Download Cable II.

The Intel FPGA Download Cable II interfaces a USB port on a host computer to an Altera® FPGA mounted on a printed circuit board. The Intel FPGA Download Cable II sends data from the host PC to a standard 10-pin header connected to the FPGA. You can use the Intel FPGA Download Cable II for the following:

- Iteratively download configuration data to a system during prototyping
- Program data into the system during production
- Advanced Encryption Standard (AES) key and fuse programming

1.1. Supported Devices and Systems

You can use the Intel FPGA Download Cable II to download configuration data to the following devices:

- Agilex™ series FPGAs
- Stratix® series FPGAs
- Cyclone® series FPGAs
- MAX® series CPLDs
- Arria® series FPGAs

You can perform in-system programming of the following devices:

- EPC (4/8/16) enhanced configuration devices
- EPCS (1/4/16/64/128), EPCQ (16/32/64/128/256/512,) and EPCQ-L (256/512/1024) and EPCQ-A (4/16/32/64/128) serial configuration devices
- Supported third-party serial configuration devices

The Intel FPGA Download Cable II supports target systems using the following:

- 5.0-V TTL, 3.3-V LVTTL/LVCMOS
- Single-ended I/O standards from 1.5 V to 3.3 V

1.2. Power Source Requirements

- 5.0 V from the Intel FPGA Download Cable II
- Between 1.5 V and 5.0 V from the target circuit board

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1.3. Software Requirements and Support

- Windows 7/8/10/11 (32-bit and 64-bit)
- Windows XP (32-bit and 64-bit)
- Windows Server 2008 R2 (64-bit)
- Linux platforms such as Red Hat Enterprise 5, 6, 7, and above

Use the Quartus® Prime software version 14.0 or later to configure your device.

Note: Quartus Prime version 13.1 supports most of the Intel FPGA Download Cable II's capabilities. If you use this version, install the latest patch for full compatibility.

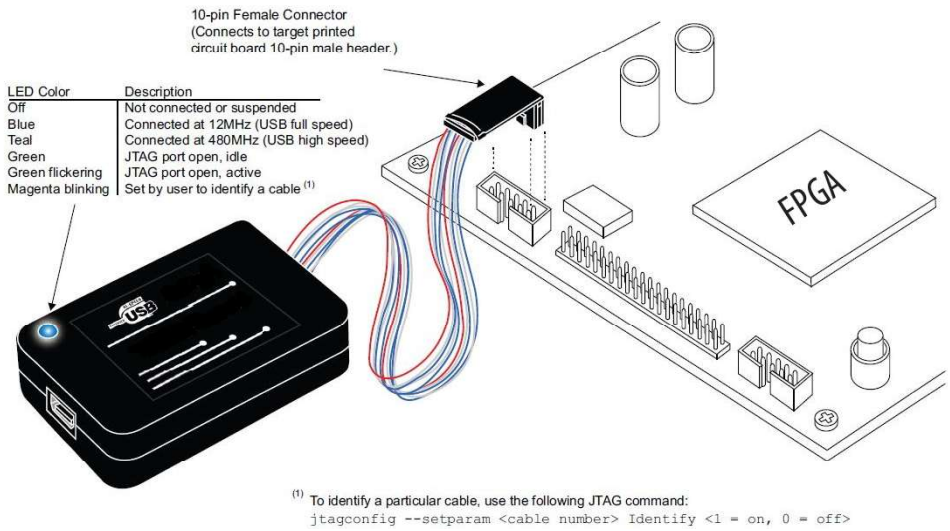
The Intel FPGA Download Cable II also supports the following tools:

- Quartus Prime Programmer (and stand-alone version)
- Quartus Prime Signal Tap Logic Analyzer (and stand-alone version)
- JTAG and debug tools supported by the JTAG Server. For example:
  - System Console
  - Nios® II debugger
  - Arm* DS-5 debugger

1.4. Installing the Intel FPGA Download Cable II for Configuration or Programming

1. Disconnect the power cable from the circuit board.
2. Connect the Intel FPGA Download Cable II to the USB port on your computer and to the download cable port.
3. Connect the Intel FPGA Download Cable II to the 10-pin header on the device board.
4. Reconnect the power cable to reapply power to the circuit board.

Figure 1. The Intel FPGA Download Cable II



Note: For plug and header dimensions, pin names, and operating conditions, refer to the *Intel FPGA Download Cable II Specifications* chapter.

Related Information

Intel FPGA Download Cable II Specifications on page 9

1.5. Installing the Intel FPGA Download Cable II Driver on Windows 7/8/10/11 Systems

You must have system administration (administrator) privileges to install the download cable drivers.

The download cable drivers are included in the Quartus Prime software installation. Before you begin the installation, verify that the download cable driver is located in your directory: `\<Quartus Prime system directory>\drivers\usb-blaster-ii`.

1. Connect the download cable to your computer's USB port.

   When plugged in for the first time, a message appears stating **Device driver software was not successfully installed**.

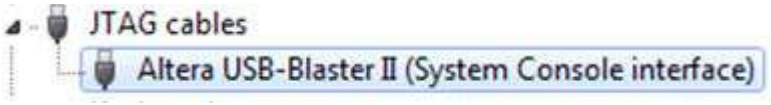
2. From the Windows Device Manager, locate **Other devices** and right-click the top **USB-BlasterII**



You need to install drivers for each interface: one for the JTAG interface and one for the System Console interface.

3. On the right-click menu, click **Update Driver Software**. The **Update Driver Software - USB BlasterII** dialog appears.
4. Click **Browse my computer for driver software** to continue.
5. Click **Browse...** and browse to the location of the driver on your system: `\<Quartus Prime system directory>\drivers\usb-blaster-ii`. Click **OK**.
6. Click **Next** to install the driver.
7. Click **Install** when asked if you want to install.

   You should now have a JTAG cable showing in the Device Manager.



8. Now, install the driver for the other interface. Go back to step 2 and repeat the process for the other download cable devices.

   When you are finished, you will have added **USB-Blaster II (JTAG interface)** under JTAG cables.

1.6. Installing the Intel FPGA Download Cable II Driver on Linux Systems

For Linux, the download cable supports Red Hat Enterprise 5, 6, 7, and above.

To access the cable, the Quartus Prime software uses the built-in Red Hat USB drivers, the USB file system (usbfs). By default, **root** is the only user allowed to use usbfs. You must have system administration (root) privileges to configure the Intel FPGA Download Cable II drivers.

1. Create a file named `/etc/udev/rules.d/51-usbblaster.rules` and add the following lines to it. (The `.rules` file may already exist if you have installed an earlier version.)

   a. Red Hat Enterprise 6 and above, and Ubuntu 18, 20, and 22

```
# USB Blaster II
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6010", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6810", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
```

   Caution: There should be only three lines in this file, one starting with a comment and two starting with BUS. Do not add extra line breaks to the `.rules` file.

2. Create a file named `/etc/udev/rules.d/51-usbblaster.rules`. (The `.rules` file may already exist if you have installed an earlier version.)
3. In the file, add the following lines, depending on the type of download cable.

   Ensure that all the code is in one line.

— Intel FPGA Download Cable:

```
# USB Blaster
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6001", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6002", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6003", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
```

— Intel FPGA Download Cable II:

```
# USB Blaster II
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6010", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
SUBSYSTEM=="usb", ENV{DEVTYPE}=="usb_device", ATTR{idVendor}=="09fb",
ATTR{idProduct}=="6810", MODE="0666", NAME="bus/usb/$env{BUSNUM}/
$env{DEVNUM}", RUN+="/bin/chmod 0666 %c"
```

4. Complete your installation by setting up the programming hardware in the Quartus Prime software. Go to the *Setting Up the Intel FPGA Download Cable II Hardware with the Quartus Prime Software* section.

For more information about download cable driver installation, refer to the *Cable and Adapter Drivers Information* page.

Related Information

- Setting Up the Intel FPGA Download Cable II Hardware with the Quartus Prime Software on page 7
- Cable and Adapter Drivers Information

1.7. Setting Up the Intel FPGA Download Cable II Hardware with the Quartus Prime Software

1. Start the Quartus Prime software.
2. From the Tools menu, click **Programmer**.
3. Click **Hardware Setup**.
4. Click the **Hardware Settings** tab.
5. From the **Currently selected hardware** list, select **Intel FPGA Download Cable II**.
6. Click **Close**.
7. In the **Mode** list, choose an appropriate programming mode. The table below describes each mode.

Table 1. Programming Modes

Mode	Mode Description
Joint Test Action Group (JTAG)	Programs or configures all devices supported by Quartus Prime software via JTAG programming.
In-Socket Programming	Not supported by the Intel FPGA Download Cable II.
Passive Serial Programming	Configures all devices supported by Quartus Prime software excluding enhanced configuration devices (EPC) and serial configuration devices (EPCS/Q).
Active Serial Programming	Programs a single EPCS1, EPCS4, EPCS16, EPCS64, EPCS/Q128, EPCQ256, EPCQ-L, and EPCQ512 device.

For detailed help on using the Quartus Prime Programmer, refer to the *Quartus Prime Pro Edition User Guide: Programmer* or the *Quartus Prime Standard Edition User Guide: Programmer*.

Related Information

- Quartus Prime Pro Edition User Guide: Programmer
- Quartus Prime Standard Edition User Guide: Programmer

2. Intel FPGA Download Cable II Specifications

2.1. Voltage Requirements

The Intel FPGA Download Cable II $V_{CC(TRGT)}$ pin must be connected to a specific voltage for the device being programmed. Connect pull-up resistors to the same power supply as the Intel FPGA Download Cable II $V_{CC(TRGT)}$.

Table 2. Intel FPGA Download Cable II $V_{CC(TRGT)}$ Pin Voltage Requirements

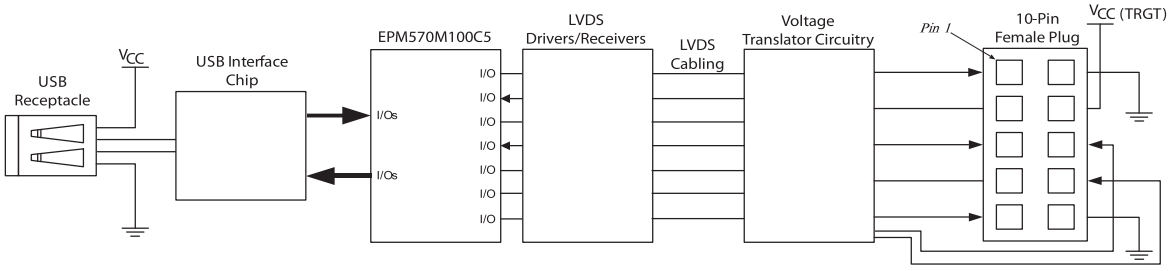
Device Family	Intel FPGA Download Cable II VCC Voltage Required
FPGAs	
Arria GX	As specified by V_{CCSEL}
Arria II GX	As specified by V_{CCPD} or V_{CCIO} of Bank 8C
Arria V	As specified by V_{CCPD} Bank 3A
Arria 10	As specified by V_{CCPGM} or V_{CCIO}
Cyclone III	As specified by V_{CCA} or V_{CCIO}
Cyclone IV	As specified by V_{CCIO}. Bank 9 for Cyclone IV GX and Bank 1 for Cyclone IV E devices.
Cyclone V	As specified by V_{CCPD} Bank 3A
Cyclone 10 GX	As specified by V_{CCPGM} or V_{CCIO}
Cyclone 10 LP	As specified by V_{CCA} or V_{CCIO}
MAX II, MAX V	As specified by V_{CCIO} of Bank 1
MAX 10	As specified by V_{CCIO}
Stratix II, Stratix II GX	As specified by V_{CCSEL}
Stratix III, Stratix IV	As specified by V_{CCPGM} or V_{CCPD}
Stratix V	As specified by V_{CCPD} Bank 3A
Stratix 10	As specified by V_{CCIO_SDM}
Agilex 7	As specified by V_{CCIO_SDM}
Agilex 5	As specified by V_{CCIO_SDM}
Configuration Devices	
EPC (4/8/16)	3.3 V
EPCS (1/4/16/64/128)	3.3 V
EPCQ (16/32/64/128/256/512)	3.3 V
EPCQ-L (256/512/1024)	1.8 V
EPCQ-A (4/16/32/64/128)	3.3 V

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2.2. Cable-to-Board Connection

A standard USB cable connects to the USB port on the device.

Figure 2. Intel FPGA Download Cable II Block Diagram



2.3. Intel FPGA Download Cable II Plug Connection

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device.

Figure 3. Intel FPGA Download Cable II 10-Pin Female Plug Dimensions - Inches & Millimeters

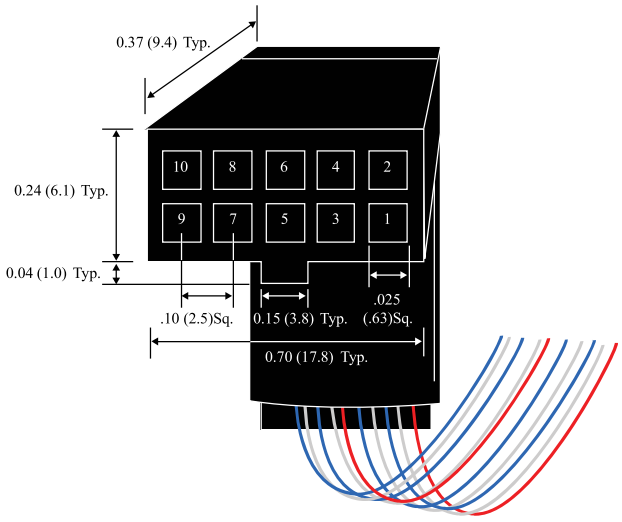
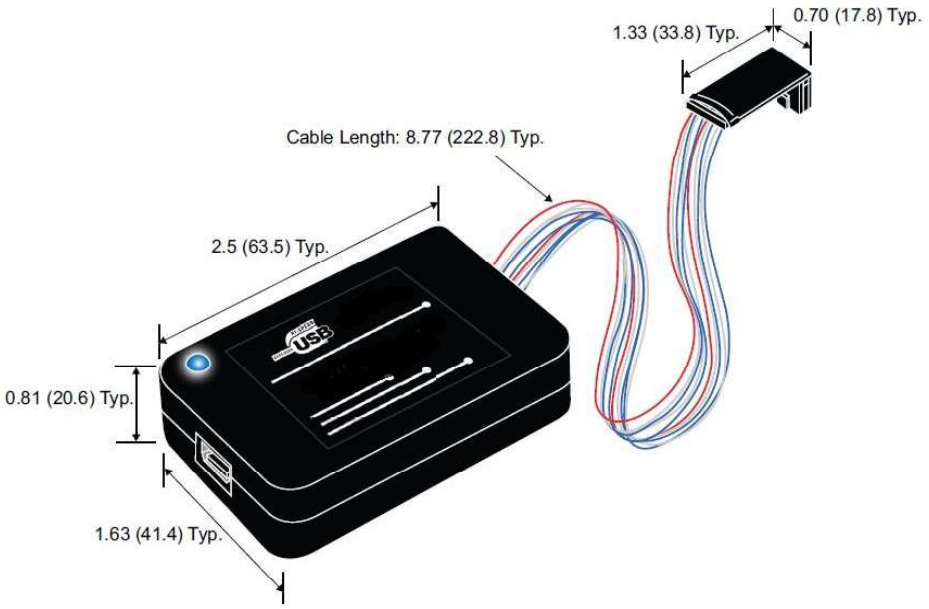


Figure 4. Intel FPGA Download Cable II Dimension - Inches and Millimeters



2.4. 10-Pin Female Plug Signal Names and Programming Modes

Table 3. 10-Pin II Female Plug Signal Names and Programming Modes

Pin	Active Serial (AS) Mode		Passive Serial (PS) Mode		JTAG Mode	
	Signal Name	Description(1)	Signal Name	Description(1)	Signal Name	Description(1)
1	DCLK	Configuration Clock	DCLK	Configuration Clock	TCK	Test Clock
2	GND	Signal ground	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration done	CONF_DONE	Configuration done	TDO	Test Data Output
4	VCC(TRGT)	Target power supply	VCC(TRGT)	Target power supply	VCC(TRGT)	Target power supply
5	nCONFIG	Configuration control	nCONFIG	Configuration control	TMS	Test Mode Select Input
6	nCE	Target chip enable	–	-	PROC_RST	Processor Reset
7	DATAOUT	Active serial data out	nSTATUS	Configuration Status	–	-

continued...

(1) The input or output pin described is referring to the pin of the FPGA device. For more information, refer to the *Configuration User Guide* or *Device Pin Connection Guidelines* of the respective FPGA device.

Pin	Active Serial (AS) Mode		Passive Serial (PS) Mode		JTAG Mode	
	Signal Name	Description(1)	Signal Name	Description(1)	Signal Name	Description(1)
8	nCS	Serial configuration device chip select	nCS	Serial configuration device chip select	–	-
9	ASDI	Active serial data in	DATA0	Passive serial data in	TDI	Test Data Input
10	GND	Signal ground	GND	Signal ground	GND	Signal ground

Note: Use pin 6 for hard processor reset under JTAG mode.

Note: The following note below only applies to Arria 10 and earlier SoC devices. PROC_RST is not used for Stratix 10 and Agilex SoC devices.

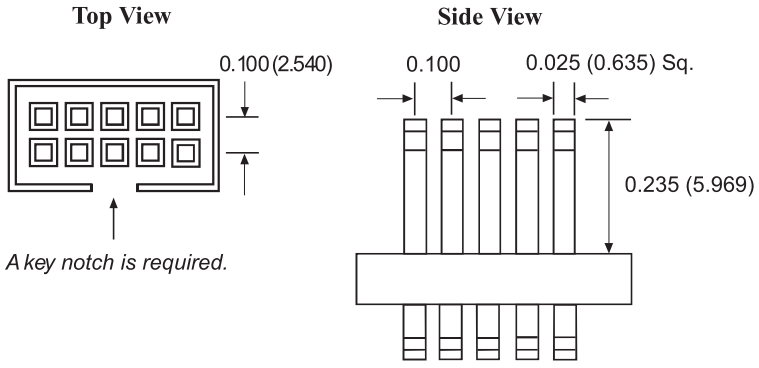
In JTAG mode, the PROC_RST pin can be used to trigger warm reset of the HPS block when prompted via the ARM DS-5 debugger. PROC_RST is an active low signal and not an open collector pin. As such, it is not recommended to connect PROC_RST to HPS_nRST directly. You should instead connect this pin to a secondary device such as the MAX V CPLD, and use the device to manage the reset network for HPS.

2.5. Circuit Board Header Connection

The 10-pin male header, which connects to the Intel FPGA Download Cable II's 10-pin female plug, has two rows of five pins. The pins are connected to the device's programming or configuration pins.

Caution: If the header connection on the circuit board is a male receptacle, it must have a key notch. Without a key notch, the 10-pin female plug will not connect. The following figure shows a typical 10-pin male header with a key notch.

Figure 5. 10-Pin Male Header Dimensions - Inches and Millimeters



(1) The input or output pin described is referring to the pin of the FPGA device. For more information, refer to the *Configuration User Guide* or *Device Pin Connection Guidelines* of the respective FPGA device.

Although a 10-pin surface mount header can be used for the cable, Altera recommends using a through-hole connector. Through-hole connectors hold up better under the repeated insertion and removal.

2.6. Operating Conditions

The following tables summarize the maximum ratings, recommended operating conditions, and DC operating conditions for the Intel FPGA Download Cable II.

Table 4. Intel FPGA Download Cable II Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(TRGT)}$	Target supply voltage	With respect to ground	–0.5	6.5	V
$V_{CC(USB)}$	USB supply voltage	With respect to ground	–0.5	6.0	V
I_I	Target side input current	Pin 7	–100.0	100.0	mA
$I_{I(USB)}$	USB supply current	VBUS	–	200.0	mA
I_o	Target side output current	Pins: 1, 5, 6, 8, 9	–50.0	50.0	mA

Table 5. Intel FPGA Download Cable II Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(TRGT)}$	Target supply voltage, 5.0-V operation	—	4.75	5.25	V
	Target supply voltage, 3.3-V operation	—	3.0	3.6	V
	Target supply voltage, 2.5-V operation	—	2.375	2.625	V
	Target supply voltage, 1.8-V operation	—	1.71	1.89	V
	Target supply voltage, 1.5-V operation	—	1.43	1.57	V

Table 6. Intel FPGA Download Cable II DC Operating Conditions

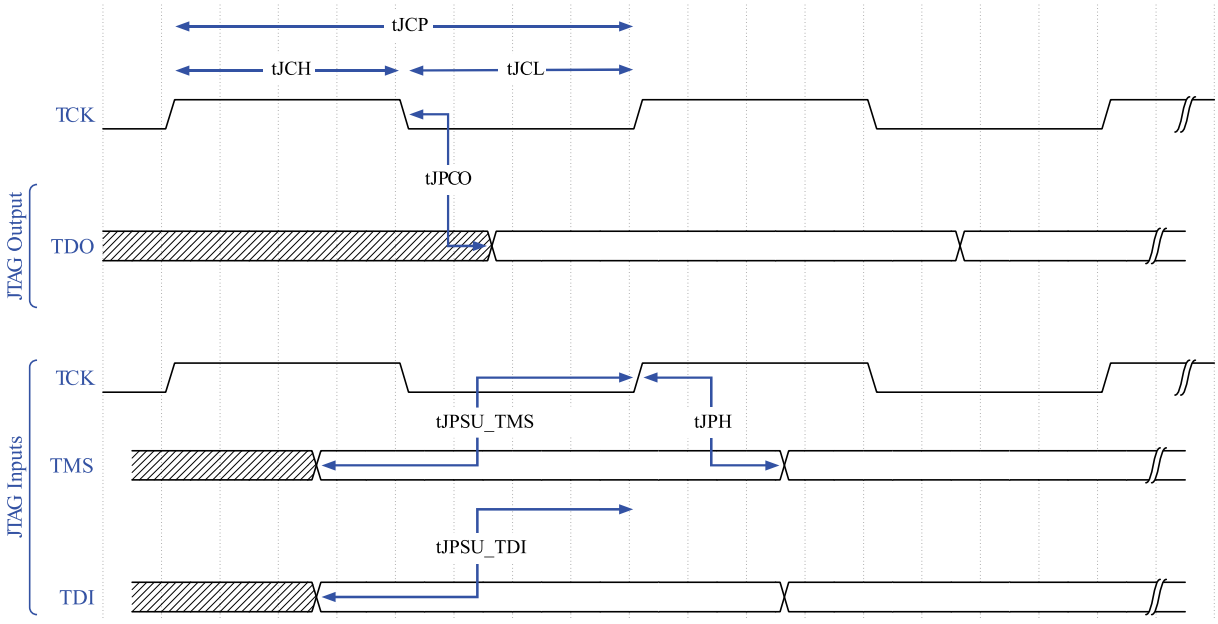
Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	$V_{CC(TRGT)}$ = 3.0 V to 3.6 V	2.0	—	V
		$V_{CC(TRGT)}$ = 2.3 V to 2.7 V	1.7	—	V
		$V_{CC(TRGT)}$ = 1.4 V to 1.95 V	0.65 × $V_{CC(TRGT)}$	—	V
		$V_{CC(TRGT)}$ = 1.2 V	0.8 × $V_{CC(TRGT)}$	—	V
V_{IL}	Low-level input voltage	$V_{CC(TRGT)}$ = 3.0 V to 3.6 V	—	0.8	V
		$V_{CC(TRGT)}$ = 2.3 V to 2.7 V	—	0.7	V
		$V_{CC(TRGT)}$ = 1.4 V to 1.95 V	—	0.35 × $V_{CC(TRGT)}$	V

continued...

Symbol	Parameter	Conditions	Min	Max	Unit
		$V_{CC(TRGT)}$ = 1.2 V	—	0.2 × $V_{CC(TRGT)}$	V
V_{OH}	5.0-V high-level output voltage	$V_{CC(TRGT)}$ = 4.5 V, I_{OH} = -32 mA	3.8	—	V
	3.3-V high-level output voltage	$V_{CC(TRGT)}$ = 3.0 V, I_{OH} = -24 mA	2.4	—	V
	2.5-V high-level output voltage	$V_{CC(TRGT)}$ = 2.3 V, I_{OH} = -12 mA	1.9	—	V
	1.8-V high-level output voltage	$V_{CC(TRGT)}$ = 1.65 V, I_{OH} = -8 mA	1.2	—	V
	1.5-V high-level output voltage	$V_{CC(TRGT)}$ = 1.4 V, I_{OH} = -6 mA	1.0	—	V
V_{OL}	5.0-V low-level output voltage	$V_{CC(TRGT)}$ = 4.5 V, I_{OL} = 32 mA	—	0.55	V
	3.3-V low-level output voltage	$V_{CC(TRGT)}$ = 3.0 V, I_{OL} = 24 mA	—	0.55	V
	2.5-V low-level output voltage	$V_{CC(TRGT)}$ = 2.3 V, I_{OL} = 12mA	—	0.3	V
	1.8-V low-level output voltage	$V_{CC(TRGT)}$ = 1.65 V, I_{OL} = 8mA	—	0.45	V
	1.5-V low-level output voltage	$V_{CC(TRGT)}$ = 1.4 V, I_{OL} = 6mA	—	0.3	V
$I_{CC(TRGT)}$	Operating current (No Load)	$V_{CC(TRGT)}$=5.5 V	—	316	uA

2.7. JTAG Timing Constraints and Waveforms

Figure 6. Timing Waveform for JTAG Signals (From Target Device Perspective)



To use the Intel FPGA Download Cable II at the maximum capability (24 MHz), meet the timing constraints like in the *JTAG Timing Constraints for the Target Device* table below for the target device.

The timing constraints require that you consider device specifications as well as trace propagation delays. If you do not follow the recommended constraints, you might encounter timing issues at 24 MHz. If the target design cannot meet these constraints, reduce the possibility of timing issues by slowing the TCK frequency. Refer to the *Changing the TCK Frequency* section for instructions on running the download cable at a slower speed.

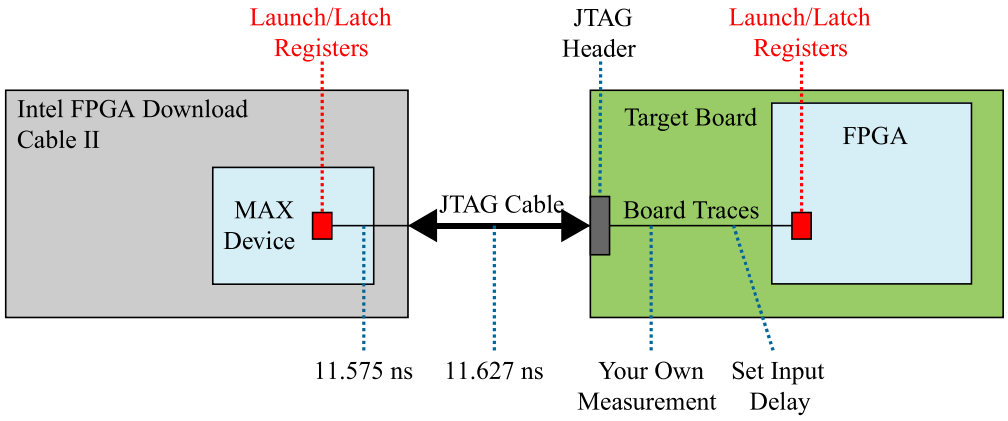
Table 7. JTAG Timing Constraints for the Target Device

Symbol	Parameter	Min	Max	Unit
tJCP	TCK clock period	41.67	—	ns
tJCH	TCK clock high time	20.83	—	ns
tJCL	TCK clock low time	20.83	—	ns
tJPCO	JTAG port clock to JTAG Header output	—	5.46 (2.5 V) 2.66 (1.5 V)	ns
tJPSU_TDI	JTAG port setup time (TDI)	—	24.42	ns
tJPSU_TMS	JTAG port setup time (TMS)	—	26.43	ns
tJPH	JTAG port hold time	—	17.25	ns

The simulated timing is based on a slow timing model, which is a worst-case scenario environment.

For device-specific JTAG timing information, refer to the related device data sheet.

Figure 7. Intel FPGA Download Cable II Timing Constraints



If you cannot meet 24 MHz, you must decrease the frequencies to 16 MHz or 6 MHz. Below is some example code to set the TCK maximum frequency to 6 MHz:

```
jtagconfig --setparam 1 JtagClock 6M
```

To verify the clock frequency of the JTAG cable ID "1", you can use the following example code:

```
jtagconfig --getparam 1 JtagClock
```

Related Information

- Changing the TCK Frequency on page 16
- Documentation: Data Sheets

2.7.1. Timing Closure Guidelines for JTAG Operation

Follow these steps to ensure that you achieve timing closure at 24 MHz:

1. In the Quartus Prime software, click **File ➤ New** and then select the **SDC File (Read by the Timing Analyzer at each fitter stage)** file type. The new file opens in the Text Editor.
2. In the Text Editor, define the JTAG constraints. You can right-click and click **Insert Template ➤ Timing Analyzer ➤ SDC Cookbook ➤ JTAG Signal Constraints**.

   Important: You can adjust the Intel FPGA Download Cable II cable length to match your design. However, you must not modify the following USB blaster parameters, as they are critical for proper operation:

```
set tck_blaster_tco_max 14.603
set tck_blaster_tco_min 14.603
set tms_blaster_tco_max 9.468
set tms_blaster_tco_min 9.468
set tdi_blaster_tco_max 8.551
set tdi_blaster_tco_min 8.551
set tdo_blaster_tsu     5.831
set tdo_blaster_th     -1.651
```

2.8. Changing the TCK Frequency

The Intel FPGA Download Cable II has a default TCK frequency of 24 MHz. Where signal integrity and timing prevents operating at 24 MHz, change the TCK frequency of the download cable:

1. Open the command line interface with the Quartus Prime `bin` directory in your path (for example, `C:\<Quartus Prime installed folder>\<Quartus Prime version>\quartus\bin64`).
2. Type the following command to change the TCK frequency:

```
jtagconfig --setparam <cable number> JtagClock <frequency><unit prefix>
```

Where:

- <*cable number*> is the download cable to be modified.
- <*frequency*> is the desired TCK frequency. Use one the following supported rates:
  - 24 MHz
  - 16 MHz
  - 6 MHz
  - 24/*n* MHz (between 10 KHz and 6 MHz, where *n* represents an integer value number)
- <*unit prefix*> is the unit prefix for the frequency (e.g., M for MHz).

Example for setting TCK maximum frequency to 6 MHz:

```
jtagconfig --setparam 1 JtagClock 6M
```

3. TCK Frequency Auto-Adjust for Intel FPGA Download Cable II

The TCK Frequency Auto-Adjust is a new feature implemented in Quartus Prime software version 19.1 Pro release for the Intel FPGA Download Cable II. This feature provide convenience and prevents incorrect TCK frequency setting that might cause slower device failure during JTAG operation.

The auto-adjust feature is enabled as default. To disable the auto-adjust feature, you can use the command line interface or Programmer GUI. The status of the feature is reset to default (enabled) when the cable is reconnected or JTAG server is restarted.

The auto-adjust feature always applies optimum frequency that can support on the current JTAG chain based on the BYPASS tests. If you specified a TCK frequency, the auto-adjust feature stops at the specified TCK frequency with the condition that the BYPASS tests are passing at the frequency.

Otherwise, the auto-adjust feature continues and will stop at lower frequency which the BYPASS tests are passing.

This new feature is only applicable when both Quartus Prime software and JTAG server are in version 19.1. If you use Quartus Prime software version 19.1 with older JTAG server (before version 19.1), the auto-adjust feature is not available.

Note: The TCK frequency auto-adjust is designed based on the hard JTAG scan chain. For virtual JTAG scan chain, the TCK frequency after auto-adjust may still require further adjustment from the user for successful JTAG operation.

3.1. Turn ON/OFF Auto-Adjust Feature

`JTAG config` command

The `JTAG config` command can be used to query the JTAG frequency auto-adjust status and turning ON/OFF the feature.

To turn off the JTAG frequency auto-adjust feature, use the following command:

```
jtagconfig --setparam <cable number> JtagClockAutoAdjust 0
```

To turn on the JTAG frequency auto-adjust feature, use the following command:

```
jtagconfig --setparam <cable number> JtagClockAutoAdjust 1
```

You may use the following command to check if auto-adjust feature is enabled. The expected output is "0" if auto-adjust is disabled and "1" if the auto-adjust is enabled

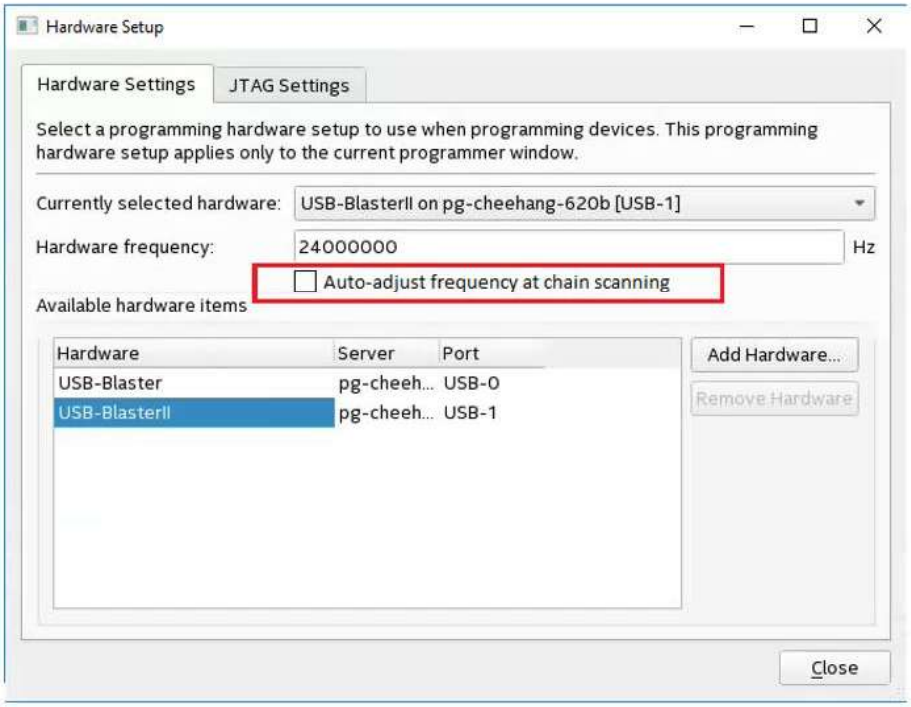
```
Jtagconfig --getparam <cable number> JtagClockAutoAdjust
```

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Programmer GUI

A checkbox is added in the Programmer's "**Hardware Setup**" dialog box to turn On/Off the frequency adjust feature. The checkbox is enabled when the frequency auto-adjust feature is available . Otherwise, it is greyed out. If the frequency auto-adjust-feature is enabled, new adjusted TCK frequency value will be shown under the message box of the programmer GUI.

Figure 8. Programmer GUI (Hardware Settings → Hardware Settings Tab)



4. Document Revision History for the Intel FPGA Download Cable II User Guide

Document Version	Changes
2025.12.05	• Updated the *JTAG Timing Constraints and Waveforms* section for clarity. • Added a new topic under the *JTAG Timing Constraints and Waveforms* section—*Timing Closure Guidelines for JTAG Operation*.
2025.09.26	Updated code in the *Installing the Intel FPGA Download Cable II Driver on Linux Systems* section.
2024.08.22	• Updated the following topics with the latest software requirement and support information: — *Software Requirements and Support* — *Installing the Intel FPGA Download Cable Driver on Linux Systems* • Updated Table: *Intel FPGA Download Cable $V_{CC(TRGT)}$ Pin Voltage Requirements* to include $V_{CC(TRGT)}$ pin voltage requirements for Agilex 5 device family. • Removed *Installing the Intel FPGA Download Cable Driver on Windows XP Systems*. • Retitled topic *Installing the Intel FPGA Download Cable Driver on Windows 7/8/10 Systems* to *Installing the Intel FPGA Download Cable Driver on Windows 7/8/10/11 Systems*. • Made editorial edits throughout the document.
2024.05.13	• Added more information about performing in-system programming in *Supported Devices and Systems*. • Updated the list of configuration devices under Table: *Intel FPGA Download Cable $V_{CC(TRGT)}$ Pin Voltage Requirements*. • Updated the note to clarify that PROC_RST is not used for Stratix 10 and Agilex SoC devices in *10-Pin Female Plug Signal Names and Programming Modes*.
2024.01.16	• Updated *Supported Devices and Systems* to include Agilex series FPGAs support. • Updated Table: *Intel FPGA Download Cable $V_{CC(TRGT)}$ Pin Voltage Requirements* to include $V_{CC(TRGT)}$ pin voltage requirements for Cyclone 10 GX, Cyclone 10 LP, Stratix 10, and Agilex 7 device families.
2023.04.21	Updated the V_{IH} and V_{IL} parameters in Table: *Intel FPGA Download Cable II DC Operating Conditions*.
2022.08.26	Added a footnote to describe the input or output pin in Table: *10-Pin II Female Plug Signal Names and Programming Modes*.
2019.10.23	Added the following sections: • *Windows Troubleshooting Procedure for Intel FPGA Download Cable* • *Troubleshooting Procedure for Error when scanning hardware - No Devices*
2019.04.01	Added new chapter *TCK Frequency Auto-Adjust for Intel FPGA Download Cable II*.
2018.04.19	Updated *10-Pin Female Plug Signal Names and Programming Modes*.

Table 8. Revision History of the Intel FPGA Download Cable II User Guide

Date	Version	Changes
October 2016	2016.10.28	The name USB-Blaster II has changed to Intel FPGA Download Cable II.
December 2015	2015.12.11	Updated Sections:

continued...

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Date	Version	Changes
		• Supported Devices and Systems • Setting Up the USB-Blaster II Hardware with the Quartus II Software • Voltage Requirements • 10-Pin Female Plug Signal Names and Programming Modes
September 2014	1.2	• Added that the USB-II download cable supports Advanced Encryption Standard (AES) key and fuse programming. • Added magenta LED color to Figure 1-1 supporting multiple cable use. • Clarified a cross reference pointing to device-specific JTAG timing information.
June 2014	1.1	• Added LED color table to Figure 1-1. • Added "JTAG Timing Constraints and Waveforms" section. • Added "Changing the TCK Frequency" section.
January 2014	1.0	Initial release.

A. Additional Information

A.1. Windows Troubleshooting Procedure for Intel FPGA Download Cable II

In the Windows version of the Quartus Prime software, you may encounter that the Intel FPGA Download Cable II may occasionally not work well; although you may not observe any problems in the physical connections. In many cases, it is due to:

- Incorrect Windows settings or some unknown problem with the Intel FPGA Download Cable II driver
- The version of JTAG related software like **Jtagconfig** or **Jtagserver** not matching the version of Quartus Prime software
- The version of the Intel FPGA Download Cable II driver is old, not proper, or corrupted

The troubleshooting steps are listed in the following sections.

A.1.1. Jtagconfig Version Setting (Quartus Prime software root directory setting)

1. Open a command prompt of Windows OS.
2. Execute the following command:

   ```
   Jtagconfig -v
   ```

   Example output message:

   ```
   Version 18.1.1 Build 646 04/11/2019 SJ Standard Edition
   ```

3. If the version in the message does not match the Quartus Prime version that you use, you must modify the user system variables for your Windows account or the system variables.

A.1.1.1. Automatic Setting

1. Go to `<Quartus Prime software install folder>\quartus\bin64` for Quartus Prime. Go to `<Quartus Prime Programmer install folder>\qprogrammer\bin64` or `<Quartus Prime Programmer install directory>\qprogrammer\quartus\bin64` for the Quartus Prime Programmer tool.
2. Execute the following command:

   ```
   qreg.exe --force -jtag -setqdir
   ```

3. Altera recommends you verify the environment variables using the manual setting procedure explained in the section below.

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A.1.1.2. Manual Setting

1. Open Environment Variables window of Windows OS.

   `Windows Settings > Type "Environment" into the search area > Choose Edit the system environment variables`

2. Check if Path variable has `%QUARTUS_ROOTDIR%\bin64` in System variables or User variables for your account. If not present, add `%QUARTUS_ROOTDIR%\bin64`.
3. Check if the `QUARTUS_ROOTDIR` variable is in a right path that the **bin64** folder locates.

   Directory for Quartus Prime: `<Quartus Prime software install folder>\quartus`

   Directory for Quartus Prime Programmer tool: `< Quartus Prime Programmer install folder>\qprogrammer` or `< Quartus Prime Programmer install directory>\qprogrammer\quartus`

4. If you notice these variables in both System variables or User variables for your account, Altera recommends that one of them should be deleted.
5. Restart your computer and check the version of **jtagconfig** using step 1 and 2.

A.1.2. Jtagserver Setting

1. Open the Windows OS command prompt.
2. Execute the following command:

   ```
   jtagconfig --serverinfo
   ```

   Example output message:

   ```
   Installed JTAG server is '<Quartus Prime install folder>\quartus
   \bin64\jtagserver.exe'
   Service manager reports server is running
   Server reports path: <Quartus Prime install folder>\quartus
   \bin64\jtagserver.exe
   Server reports version: Version 18.1.1 Build 646 04/11/2019 SJ Standard
   Edition
   Remote clients are disabled (no password)
   ```

   If the installed JTAG server does not match the version of the Quartus Prime software you use, install the same version of JTAG server as the Quartus Prime software.
3. Set the environment variables correctly following the steps described in the **jtagconfig** version setting in the sections above.
4. Execute the following commands:

   ```
   Jtagserver -uninstall
   Jtagserver -install
   ```

5. Restart your computer.

A.1.3. Install/Reinstall the Intel FPGA Download Cable II Driver

1. Connect your Intel FPGA Download Cable or Intel FPGA Download Cable II.
2. Open **Device Manager** window of Windows OS.

   `Windows Settings > Type "Device Manager" into the search area > Choose Device Manager`
3. Find Intel FPGA Download Cable II under JTAG cables or Intel FPGA Download Cable under Universal Serial Bus controllers.
4. Choose Intel FPGA Download Cable or Intel FPGA Download Cable II.
5. Right click and choose **Uninstall device** from context menu.
6. Enable **Delete the driver software for this device** and click **Uninstall**.
7. If you see another Intel FPGA Download Cable or Intel FPGA Download Cable II, uninstall it too.
8. Reinstall the drivers following the steps in the Windows Troubleshooting Procedure for Intel FPGA Download Cable II section.

A.2. Troubleshooting Procedure for Error when scanning hardware - No Devices

You might see this error when connecting multiple download cables to your computer and executing `jtagconfig` command.

```
Error when scanning hardware - No devices
```

It takes a certain finite amount of time for your computer to finish the USB device enumeration after connecting USB devices. The more USB devices are connected, the more time is required for the USB device enumeration.

The above error occurs when `jtagconfig` command is executed before your computer finishes the USB device enumeration to recognize all download cables connected. The error seems to occur only when `jtagconfig` command is executed right after multiple download cables are connected

Troubleshooting Procedure

You need to wait for a while until your computer finishes the USB device enumeration after your Intel FPGA Download Cable II is connected. You can use Device Manager on Windows or `lsusb` command on Linux to check if your Intel FPGA Download Cable II is recognized on your computer.

For Windows: Open **Device Manager** and check if Intel FPGA Download Cable II (JTAG interface) under JTAG cables or Intel FPGA Download Cable under Universal Serial Bus controller is listed.

For Linux: Open a command shell, type `lsusb`, and check if the device with ID of `09fb:6001`, `09fb:6002`, `09fb:6003`, `09fb:6010`, or `09fb:6810` is listed.

A.3. Certification Statements

A.3.1. RoHS Compliance

The table below lists hazardous substances included with the Intel FPGA Download Cable II.

A value of 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold as specified by the SJ/T11363-2006 standard.

Table 9. Hazardous Substances and Concentration

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavelent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Electronic Components	0	0	0	0	0	0
Populated Circuit Board	0	0	0	0	0	0
Manufacturing Process	0	0	0	0	0	0
Packing	0	0	0	0	0	0

A.3.2. USB 2.0 Certification

This product is USB 2.0 certified.

A.3.3. CE EMI Conformity Caution

This product is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user of this product to modify it in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the sole responsibility of the user.

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