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FUNCTIONAL DESCRIPTION

Submit File Execution Control

IF/ELSE/ENDIF—conditional submit file execution based on file existence, program errors, pattern matching, plus several other conditions
GOTO—causes submit execution to resume at a specified label
RETURN—causes execution to return to the "submitter" (calling file)
EXIT—halts submit file execution
LOOP—forces execution to resume at the beginning of the submit file
RESCAN—allows submit execution to begin anywhere in file
NOTE—allows "progress report" notes to be placed in submit files
WAIT—displays a message, and waits for user input to continue or abort
STOPIF—halts submit file execution if specified listing contains errors

Source Management

XLATE2—submit-like tool with intelligent parameter substitution (for version control)
MRKOBJ—"marks" object modules with source version information
CHKLOD—lists source version data put in load modules by MRKOBJ
CLEAN—deletes all old versions off a specified disk
LATEST—displays latest version numbers of specified files

Operating System Functions

CONSOL—reassigns console input and console output as directed
DSORT*—alphabetically sorts floppy disk and hard disk directories
RELAB*—changes disk name to any other specified name

Program Development and Debugging

ERRS—fast display of program errors in PL/M 80, PL/M 86, and ASM 86 listings
MERG80—merges debug data from locate maps into PL/M 80 listings
MERG86—merges debug data from symbol maps into PL/M 86 and Pascal 86 listings
GENPEX—produces include file for PL/M external declarations (source level)
PASSIF—general purpose assertion checking, testing, and reporting tool

Text Processing

COMPAR—performs line-oriented text file comparison (shows source changes)
UPPER—changes all letters in an ASCII text file to uppercase
LOWER—changes all letters in an ASCII text file to lowercase
LAST—displays the last 512 bytes of a file
SORT—sophisticated line-oriented text file sorting tool

Disk Backup and File Processing

DCOPY—fast track-by-track diskette copying
HDBACK*—sophisticated hard disk to floppy disk backup program
PACK—compacts text files by removing strings of blanks
UNPACK—reconstitutes "packed" files

Disk Recovery

GANEF*—interactively reads and writes floppy or hard disk data blocks

Program Identification

WHICH—displays version number of Software Toolbox Programs

*These programs will not operate on the NDS-I remote hard disks.

ORDERING INFORMATION

Product Code	Description
MDS-363†	ISIS-II SOFTWARE TOOLBOX

Requires software license.

SUPPORT CATEGORY: Level C

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8086 SOFTWARE TOOLBOX

- **Collection of Tools That Speed Software Development**
- **MPL, a Standalone Macro Processor, is Ideal for Debugging Macros**
- **SCRIPT and SPELL Assist Text Preparation**
- **OMC286 and E80287 Aid 80286 and 80287 Software Development**
- **Many Other Valuable 16-Bit Software Tools Are Included**
- **Runs on Series III and Series IV Microcomputer Development Systems**
- **Runs under iRMX™ Operating System**

The 8086 Software Toolbox is a collection of 16-bit software tools that can significantly improve programmer productivity. These tools are valuable for text formatting and preparation, software testing and performance analysis, 286/287 software development, and a multitude of other applications.

Text processing tools ease document formatting and preparation. SCRIPT is a text formatting program that uses commands embedded in text to do paging, centering, left and right margins, subscripts, etc. SPELL finds misspelled words in a text file and comes with a user expandable dictionary. COMP compares two text or source files and displays their differences.

Test and performance analysis tools aid software testing and performance evaluation. PERF, a performance analysis tool for 8086 software, is ideal for isolating code "hot spots." PASSIF is a general-purpose assertion checking and reporting tool perfect for running test suites.

Software development for 286/287 components is assisted by two software tools: OMC286, an 8086 to 80286 object module convertor, and E80287, an 80287 emulator that runs on the 80286.

Additional tools are included that aid 16-bit software development efforts. All tools run on Series III and Series IV Microcomputer Development Systems.

TEXT PROCESSING
SCRIPT
MPL
SPELL
WSORT

PERFORMANCE MEASUREMENT & TESTING
PERF
GRAFIT
PASSIF

286/287 DEVELOPMENT
OMC286
E80287

MISCELLANEOUS TOOLS
COMP
FUNC
XREF
DC
HSORT
ESORT

8086 SOFTWARE TOOLBOX TOOLS

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FUNCTIONAL DESCRIPTION

Text Processing

SCRIPT—text formatting program that does paging, centering, left and right margins, justification, page headers and footers, underlines, boldface type, subscripts and superscripts, upper and lower case, and much more. Formatting commands are embedded in text.

MPL—standalone macro processor that processes the macro language used in 8086, 80286, 8089, and 8051 assemblers. Can be used interactively which makes it ideal for debugging macros. MPL can be used to preprocess any text file.

SPELL—finds misspelled words in a text file. Dictionary of correctly spelled words is user expandable.

WSORT—utility for creating the SPELL dictionary.

COMP—performs line-oriented text file comparison (shows source changes). Also understands 8086 object module formats for comparing 8086 object files.

Performance Measurement and Testing

PASSIF—general-purpose assertion checking, testing, and reporting tool. Helps automate the software testing process.

PERF—performance analysis tool for 8086 software. Monitors references in the code segment; segment monitored is user defined. Works with small or compact bound loadable modules. Ideal for isolating code "hot spots." Will only run on the Series III.

GRAFIT—graphing utility for use with PERF.

Miscellaneous Tools

OMC286—object module convetor that converts 8086 object modules into 80286 object modules.

E80287—an 80287 emulator that runs on the 80286.

FUNC—allows user to redefine the keys on a Series III keyboard and define function keys. Requires the iMDX 511 firmware.

XREF—produces cross-reference tables from translator list files. Cross-references all symbols—variables, labels, literallys, and quoted strings.

DC—floating point desk calculator program; allows variable definitions.

HSORT—in memory heap sort utility.

ESORT—very flexible sort program.

SPECIFICATIONS

Operating Environment

ISIS Operating System with RUN or INDX Operating System executing on Series III or Series IV Microcomputer Development Systems.

iRMX™86 Operating System executing in SYS X86/3XX environment.

Required Hardware

Series III or Series IV Microcomputer Development System

Required System Software

ISIS Operating System with RUN or iNDX Operating System

Documentation

"8086 Software Toolbox"
(122203)

Software Support

This product includes a 90-day initial support consisting of new software releases, updates, subscription services (software performance reports and technical reports), and telephone hotline support. Additional software support services are available separately.

ORDERING INFORMATION

Product Code	Description
iMDX-364	8086 Software Toolbox

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AEDIT TEXT EDITOR

- **AEDIT-80 operates on any Intellec® Series II, Model 800 or IPDS™ Development System**
- **Full Screen Editing**
- **Menu-Driven, Easy to Use**
- **Easy Handling of Large Blocks of Text**
- **Dual File Editing**
- **AEDIT-86 Operates on any Intellec® Series III, Series IV, or iRMX™ system.**
- **Powerful Macro Facility**
- **Split-Screen Windowing**
- **Designed for the Programmer and Technical Writer**

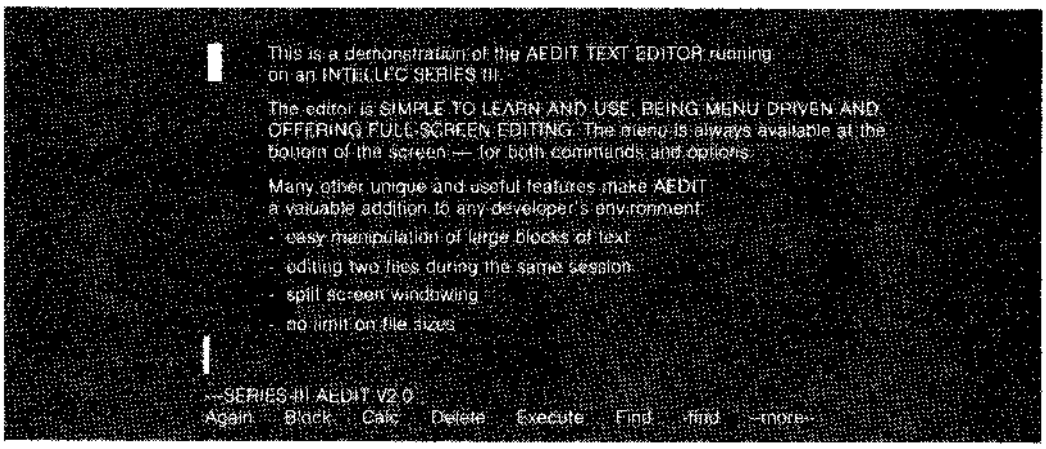
AEDIT is a full screen editor for use on any Intellec® Development or iRMX™ system. It is designed to be easy to learn and easy to use. At all times the user is guided by a menu which is used not only to select commands, but also to select options to commands. There is no need to constantly refer to or memorize detailed manuals.

AEDIT provides full screen editing capabilities and offers features to easily handle (move, copy, delete) large blocks of text. In addition to the basic editing abilities, AEDIT supports tagging positions in the text, string search and replace commands, and the option of automatic text indentation, spilling, and formatting. AEDIT is able to edit files of any length and optionally creates back-up copies of the file being edited

With AEDIT, two files can be edited during one session. The user can easily switch between the files for quick reference, editing, or to transfer text from one file to the other. Using the windowing capabilities available with AEDIT-86, both of these files may be displayed simultaneously in a split-screen format

AEDIT supports a powerful macro facility. AEDIT can create macros by simply keeping track of what a user is executing, "learning" the function the macro is to perform. The editor remembers the user's actions for later execution, and can store them in a file if requested Alternately, a user may enter a macro using AEDIT's macro language, or modify any existing macro interactively.

These and many other features combine to make AEDIT the editor of choice



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SEPTEMBER 1984
ORDER NUMBER:210996-003

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AEDIT TEXT EDITOR

MANUALS

AEDIT is supplied with a user manual documenting all the aspects of the editor, and a pocket reference card. The manual includes an introductory tutorial.

HOST SYSTEM

AEDIT-80 is an 8080/8085-based utility and can be run on any Intellec Development System, Series IIE, Series II, Model 800, or iPDS, as well as on ISIS Cluster workstations.

The higher-performance AEDIT-86 is an 8086-based utility that can be run on any Intellec Series IIIE, Series III, or Series IV Development system. Any Series IIE, Series II or Model 800 system can be upgraded to Series III functionality. AEDIT-86 is also available for the iRMX™ Operating Systems.

AEDIT can be configured to run with non-Intel terminals. Tested configurations are available for the following popular terminals:

ADDS Regent 200, Viewpoint 3A+
Beehive Mini-Bee
DEC VT52, VT100
Hazeltine 1510
Lear-Seigler ADM-3A
Zentec ZMS-35

Regent 200 is a trademark of ADDS
Mini-Bee is a trademark of Beehive
DEC designated Digital Equipment Corporation
ADM-3A is a trademark of Lear-Siegler

ORDERING INFORMATION

iMDX-335	AEDIT-80 Text Editor. Includes 8" single and double density diskettes for Series IIE, Series II, or Model 800, and a 5¼" diskette for iPDS.
iMDX-334	AEDIT-86 Text Editor Includes 8" single and double density diskettes for Series III.

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Communication Software 5

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COMMUNICATION SOFTWARE

Communications software is essential in an environment of multiple host systems. Intel recognizes the need to exchange information between Intel development systems, IBM mainframes, and DEC VAX minicomputers. Intel provides software to make this communication easy.

The asynchronous communication link (ACL) enables an Intel development system to transfer files to and from a VAX minicomputer. Two versions of this program are available, one for VAX/VMS and one for UNIX.

The mainframe link allows any ISIS-II user to transfer files to an IBM mainframe. This package uses the bisynch protocol to communicate with the IBM host by emulating a 2780/3780 batch terminal. Conversion of text files between ASCII and EBCDIC is supported.

iNA955 allows a user to connect an iRMX system to the NDS-II network for file transfer purposes. Network directories can be inspected and created remotely from the iRMX system. File transfer with this program occurs at Ethernet speeds.

iNA960 is an OEM product for use in iRMX systems. It is a general purpose Local Area Network software package that provides the user with guaranteed end to end message delivery. iNA960 conforms to ISO and Ethernet standards. It provides network management functions as well as the 82586 device drivers.

NDS-II Electronic Mail allows human to human communication without wasting time on missed telephone calls. Several types of mailboxes, such as private, group, or bulletin board, are supported. Typical mail uses are to send memos, collect project milestone data, and be a telephone message center.

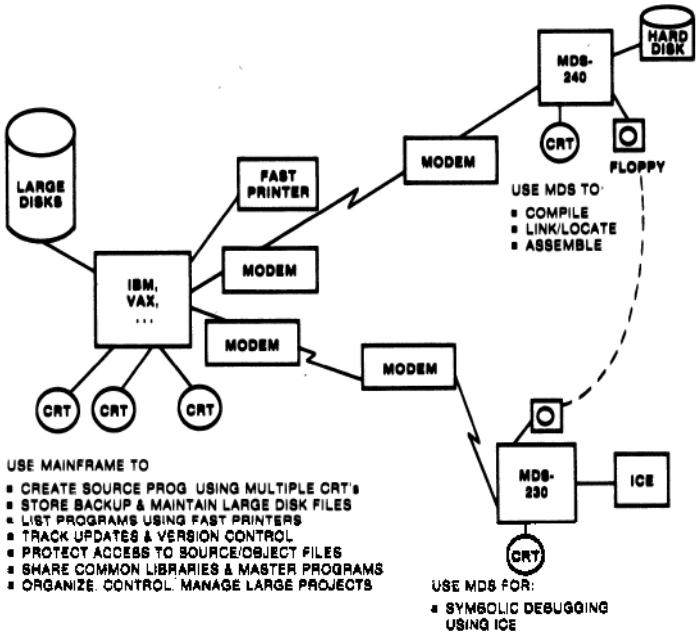
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MAINFRAME LINK FOR DISTRIBUTED DEVELOPMENT

- **Integrates user mainframe resources with Intellec® Development Systems.**
- **Uses IBM 2780/3780 standard BISYNC protocol supported by a majority of mainframes and minicomputers.**
- **Protocol supports full error detection with automatic retry.**
- **Software runs under ISIS-II on any Intellec® Development System.**
- **Communicates with remote systems on dedicated or switched (dial-up) telephone lines.**
- **Package also includes tests and a connector for loop-back self-test capability.**

The Mainframe Link consists of software, modem cable to connect the development system to the modem and a loopback connector for diagnostic testing. The software runs under ISIS-II on Intellec Development Systems. It emulates the operation of an IBM 2780 or 3780 Remote Job Entry (RJE) terminal to (1) transmit ISIS-II files to a remote system or (2) receive files from a remote system using standard BISYNC 2780/3780 protocol. The remote system can be any mainframe or minicomputer which supports the IBM 2780 or 3780 communications interface standard. Files may contain ASCII or binary data so that either program source files (ASCII) or program object files (binary) may be transmitted.

The Mainframe Link allows the user to integrate in-house mainframe resources with Intellec Microcomputer Development resources. The mainframe can be used for storage, maintenance and management of program source and object files. The program source can be downloaded to a development system for compilation, assembly, linkage, and/or location. The linked modules can be transmitted and saved on the mainframe to be shared by all programmers. The linked program can then be downloaded to a development system for debugging using ICE emulation.



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FEATURES

- Runs under ISIS-II on any Intellec® Microcomputer Development System.
- Communicates with a remote system using IBM 2780/3780 standard BISYNC protocol, which is supported by a majority of minicomputers and mainframes, on dedicated or switched (dial-up) telephone lines.
- The modem cable supplied with the package can be used to connect the Intellec® Development System to the modem (or modem eliminator) using the standard RS232C port.
- Supports user selectable data transmission rates of up to 9600 baud.
- Package includes diagnostic tests used to verify the operation of the Intellec® Development System using the loop-back connector supplied and data transmission up to the modem using the analog loop-back feature.
- System can be configured to match the requirements of the installation, i.e., using modem eliminators for connections up to fifty (50) feet, or by using modems and telephone lines.
- Software can be configured from several configuration options such as:

  2780, 3780 or Intel Mode

  Transparent mode for binary data

  Non-transparent mode for ASCII data

  Automatic translation from ASCII to EBCDIC and vice versa

  Receive chaining for receiving multiple files
- Intel mode is used mainly for file transfers between two Intellec® Development Systems. The files are duplicated exactly.
- Console commands support all standard features including:

  SEND data in Transparent or Non-transparent mode, with or without translation to EBCDIC

  RECEIVE in Transparent or Non-transparent mode, with or without translation to EBCDIC.

  Support for an IBM RJE console (such as HASP)
- Special utility programs are provided. STRZ strips extra binary zero's from the end of object files. CONSOL assigns system console input to an ISIS-II disk file.
- Can process commands interactively from the console or sequentially from an ISIS-II file under the SUBMIT facility for semi-automatic batch operation.
- Error detection in line transmission and error recovery by automatic retransmission.
- A special command such as DIAGNOSE, allows logging of all data activity on the line, during transmission and reception.
- When not used for communicating with the mainframe, the Intellec® Development System is available as a complete, stand-alone system.

BENEFITS

- Allows the customer to use an in-house mainframe or minicomputer for program source-preparation, editing, back-up and maintenance using inexpensive CRT's and multi-terminal access. The common files may be shared and others protected.
- Many programmers can use and share the high-performance devices normally available on large computer systems, e.g., fast printers to reduce listing time, the large capacity disks with their fast access time to store large program files.
- The source files can be downloaded using the Mainframe Link to an Intellec Development System (e.g., Model 240 or 245) for compilation, linking and locating.
- The compiled and/or linked object files may be transmitted back to the remote for storage. Updates and version numbers and dates can be tracked to ensure that the latest version is always used and back-up files are available. Binary object files can be later downloaded to an Intellec Development System for debugging using an ICE emulator.
- In short, provides a powerful and flexible tool combining the best of both micro and mainframe worlds, i.e., powerful CPU with large disk capacity, file sharing, multi-terminal access, etc., from a mainframe or minicomputer with Intel's versatile and compatible software support systems (including PL/M, PASCAL, FORTRAN, Assembler, R & L) and sophisticated debugging tools such as ICE emulators.

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SPECIFICATIONS

Operating Environment

Required Hardware:

Intellec® Microcomputer Development System
Model 800
Models 220, 225, 230, 235, 240 or 245

64KB of Memory

One Diskette Drive
Single or Double Density

System Console
Intel CRT or non-Intel CRT

Recommended Hardware for Compilation:

Hard Disk (Models 240, 245, or Model 740 Upgrade)

Additional Hardware Required for Model 800
ISBC-955™, ISBC-534™

Required Software:

ISIS-II Diskette Operating System
Single or Double Density

Documentation Package

Mainframe Link User's Guide (121585-001)

Shipping Media

Flexible Diskettes
Single and Double Density

Remote System Requirements

- IBM 2780/3780 BISYNC protocol as supported by a majority of mainframes and minicomputers including: all IBM-360/370 Systems, PDP-11/70, VAX-11/780, Data General ECLIPSE.
- Users should purchase this standard software package from the remote system vendor and any additional required hardware such as a synchronous communications interface.
- The operating system at the remote must be configured (SYSGEN'ed) with correct options such as line address, 2780 or 3780, . . .

Communication Equipment Requirements

The Intellec Development System may be connected to the remote system using any one of the following methods:

- For short distances (up to 50 feet), use a synchronous modem eliminator (e.g., SPECTRON ME-81FS-2).
- For distances up to four miles, use short haul synchronous modems and telephone lines.
- For distances greater than four miles, use synchronous modems and telephone lines. The following BELL modems or their equivalents are recommended:

BELL 201C	2400 bits/second (half duplex, switched line)
BELL 208A	4800 bits/second (full duplex, leased line)
BELL 208B	4800 bits/second (half duplex, switched line)
BELL 209A	9600 bits/second (full duplex, leased line)

- Modems at either end must be compatible.

ORDERING INFORMATION

Part Number	Description
*MDS-364 Kit	Mainframe Link for Distributed Development

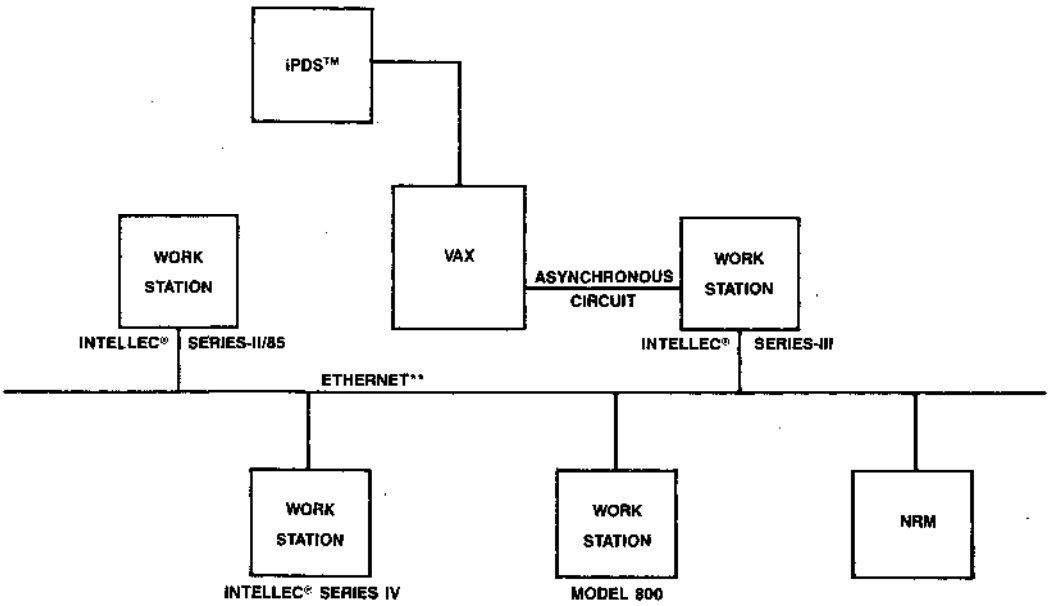
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INTEL ASYNCHRONOUS COMMUNICATIONS LINK

- **Communications software for VAX* host computer and Intel microcomputer development systems**
- **Compatible with VAX/VMS* and UNIX† operating systems**
- **Supports Intel's Model 800, Intellec® Series II, Series III, Series IV and iPDS™ microcomputer development systems**
- **Supports NDS-II workstations**
- **Allows development system console to function as a host terminal**
- **Operates through direct cable connection or over telephone lines**
- **Software selectable transmission rate from 300 to 9600 baud**

Intel's Asynchronous Communications Link (ACL) enables one or more Intel microcomputer development systems to communicate with a Digital Equipment Corporation VAX family computer. The link supports Intel Model 800, Intellec Series II, Series III, Series IV or iPDS™ development systems and NDS-II workstations. Programmers can use the editing and file management tools of the host computer and then download to the Intel microcomputer development system for debugging and execution. Programmers can use their microcomputer development system as a host terminal and control the host directly without changing terminals.



NDS-II Example

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†UNIX is a trademark of Bell Laboratories.
**Ethernet is a trademark of Xerox Corp.

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January, 1984
ORDER NUMBER: 210903-002

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FUNCTIONAL DESCRIPTION

The Asynchronous Communications Link (ACL) consists of cooperating programs: one that runs on the host computer, and others that run on each microcomputer development system. The development system programs execute under the ISIS-II or ISIS-III(N), ISIS-IV, ISIS-II(W) or ISIS-PDS operating system. They invoke the companion program on the VAX-11/7XX, which runs under either the VAX/VMS or UNIX operating system.

The link provides three modes of communication: on-line transmission, single-line transmission, and file transfer. In on-line mode, the development system functions as a host terminal, enabling the programmer to develop programs using the host computer's editing, compilation, and file-management tools directly from the development system's console. Later, switching to file transfer mode, text files and object code can be downloaded from the host to the development system for debugging and execution. Alternatively, files can be sent back to the host for editing or storage. In single line mode, the programmer can send single-line commands to the host computer while remaining in the ISIS environment.

The user can select transmission rates over the link from 300 to 9600 baud. The link transmits in encapsulated blocks. The receiver program validates the transmission by checking record-number and checksum information in each block's header. In the event of a transmission error, the receiving program recognizes a bad block and requests the sender to retransmit the correct block. The result is highly reliable data communications.

SOFTWARE PACKAGE

The Asynchronous Communications Link Package contains either a VAX/VMS or UNIX compatible magnetic tape, a single 8", double 8", Series-IV 5¼", and PDS 5¼" diskette compatible with the Intellec development system, and the *Asynchronous Communications Link User's Guide* containing installation, configuration, and operation information.

HARDWARE CONNECTION

The Link sends data over an RS232C cable. The communication line from the host computer connects directly to a development system port.

TELECOMMUNICATIONS USING THE LINK

The ACL is ideal for cross-host program development using a commercial timesharing service. This configuration requires RS232C compatible modems and a telecommunications line. Depending on the anticipated level of usage, wide-area telephone service (WATS), a leased line, or a data communications network may be chosen to keep operating overhead low.

NDS-II ACCESS USING THE LINK

The ACL is ideal for interconnecting VAX host computers with NDS-II. This configuration requires that an NDS-II workstation be connected to the VAX host computer using the RS232C interface and to NDS-II using the Ethernet interface.

All three modes of communication operate identically on NDS-II. In the on-line mode, the development workstation operates as a host terminal, and concurrently, as an NDS-II workstation. It is an easy transition between the VAX and ISIS operating system environments as LOGON/LOGOFF sequences are not required to re-enter environments.

In file transfer mode, text and object files can be transferred from the VAX directly to the Winchester Disk at the NRM without first copying the files to the workstation local floppy disk. Similarly, files residing on the NDS-II Network File System (the Winchester Disk at the NRM) can be transferred directly to the VAX without using local workstation storage.

Using the EXPORT/IMPORT mechanisms of NDS-II, a network workstation which is not directly connected to the VAX can cause files to be transferred between the VAX and NRM. For example, any NDS-II workstation can "EXPORT" ACL commands to another "IM-

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PORT"ing NDS-II workstation which is physically connected to a VAX. The "IMPORT"ing workstation executes the ACL command file causing the desired action to occur.

VAX ACCESS USING THE LINK

Users who want multiple workstations concurrently operating as VAX terminals (ONLINE mode) must physically connect each workstation to the VAX. However, users who want multiple workstations to be able to upload/download files, for example, must only physically connect one workstation to the VAX. By using the EXPORT/IMPORT mechanism of NDS-II as described above, the user can have multiple workstations accessing the VAX using only one connection.

SPECIFICATIONS

Software

Asynchronous Communications Link development system programs

VAX/VMS or UNIX companion program

Media

Single- or double-density ISIS 8" and Series-IV, PDS 5¼" compatible diskette

600-ft. 1600 bpi magnetic tape, VAX/VMS or UNIX compatible

Data Transfer Speeds

All systems up to 9600 bps

Online Terminal Mode Speeds

Series II, Series III, Series IV — 2400 bps max
PDS — 9600 bps max
Model 800 — equal to or less than the Terminal speed

Manual

Asynchronous Communications Link User's Guide, Order No. 172174-001

Required Host Configuration

VAX-11/7XX running VAX/VMS (Version 3.2) or fourth Berkeley distribution of UNIX 4.1

Required Intel Development System Configuration

Model 800, Series II, Series III, Series IV, or iPDS under ISIS

Required Connection

RS232C compatible — cable 3M-3349/25 or equivalent; 25-pin connector 3M-3482-1000 or equivalent

Recommended Modems for Telecommunications

300 baud — Bell* 103 modem; VADIC† 3455 modem or equivalent

1200 baud — Bell 202 modem; VADIC 3451 modem or equivalent

9600 baud — Bell 209A (full duplex, leased line) or equivalent

Note: Since one of the two Model 800 ports uses a current loop interface, Model 800 users need a terminal or modem that is current loop compatible, or a current loop/RS232C converter.

The Model 800 might require modification by a qualified hardware technician. Intel does not repair or maintain boards with these changes.

ORDERING INFORMATION

Product Name

Asynchronous Communications Link

Ordering Code‡

iMDX 394 for VAX/VMS systems
iMDX 395 for UNIX systems

*Bell is a trademark of American Telephone and Telegraph.
†VADIC is a trademark of Racal-Vadic Inc.
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iNA 960 NETWORK SOFTWARE

- **ISO Transport (8073) Class 4 services**
  - —Guaranteed message integrity
  - —Data rate matching (flow control)
  - —Multiple connection capability
  - —Variable length messages
  - —Expedited delivery
  - —Negotiation of virtual circuit characteristics during opens
- **Additional functionality**
  - —Connectionless transport (Datagram)
  - —External Data Link
- **IEEE 802.3 Data Link protocol (CSMA/CD) supported**
- **Comprehensive Network Management services**
  - —Collection of network usage statistics
  - —Setting and inspecting of transport and data link parameters
  - —Fault isolation and detection
  - —Boot Server
- **Compatible with multiple system environments**
  - —Runs as an iRMX™ 86 job
  - —Supports host operating system independent designs based on 8086, 8088 or 80168 and 82586 components
- **Runs on iSBC® 186/51 COMMputer™ Board**
- **Size configurable to suit specific application requirements**

iNA 960 is a general purpose local area network software package implementing the class 4 services of the ISO transport specification and network management functions in system designs based on the 8086, 8088 and 80186 microprocessors and the 82586 communications co-processor. iNA 960 also supports Intel's board level LAN products, the iSBC® 550 KIT and the iSBC® 186/51. Combined with the iSBC 186/51 COMMputer™ board, iNA 960 offers a high performance, cost effective network solution for MULTIBUS® iRMX™ 86 users. See Figure 1 for iNA 960 functionality and operating environments.

iNA 960 is a ready-to-use software building block for OEM suppliers of networked systems for both technical and commercial applications. Examples for such applications include networked design stations, manufacturing process control, communicating word processors, and financial services workstations. Using the iNA 960 software the OEM can minimize development cost and time while achieving compatibility with a growing number of equipment suppliers adapting the IEEE and ISO standards.

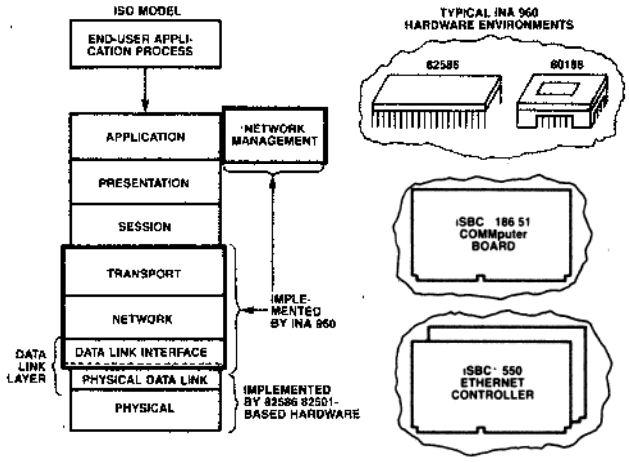


Figure 1.

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FUNCTIONAL OVERVIEW

The iNA 960 design is a standard implementation of the Class 4 transport protocol defined by the ISO OSI model. The Transport Layer provides a reliable full-duplex message delivery service on top of the "best effort" IEEE 802.3 standard packet delivery service implemented by the 82586 (or equivalent) physical and data link functions.

Consisting of linkable modules, the software can be configured to implement a range of capabilities and interface protocols. In addition to reliable process-to-process message delivery, the capabilities include a datagram service, a boot server, a direct user access to the Data Link Layer, and a comprehensive network management facility.

iNA 960 can be configured to run under iRMX 86 along with the user software, or to run on top of a dedicated 8086, 8088 or 80186 processor coupled with an 82586 to provide a communications front end processor.

The software also includes a Network Management service. This facility enables the user to monitor and adjust the network's operation in order to optimize its performance.

The current release of iNA 960 includes a "null" Network Layer supporting the Data Link and Transport Layers without providing internetwork routing service. This capability will be implemented in later releases of iNA 960.

For a conceptual block diagram of iNA 960, refer to Figure 2.

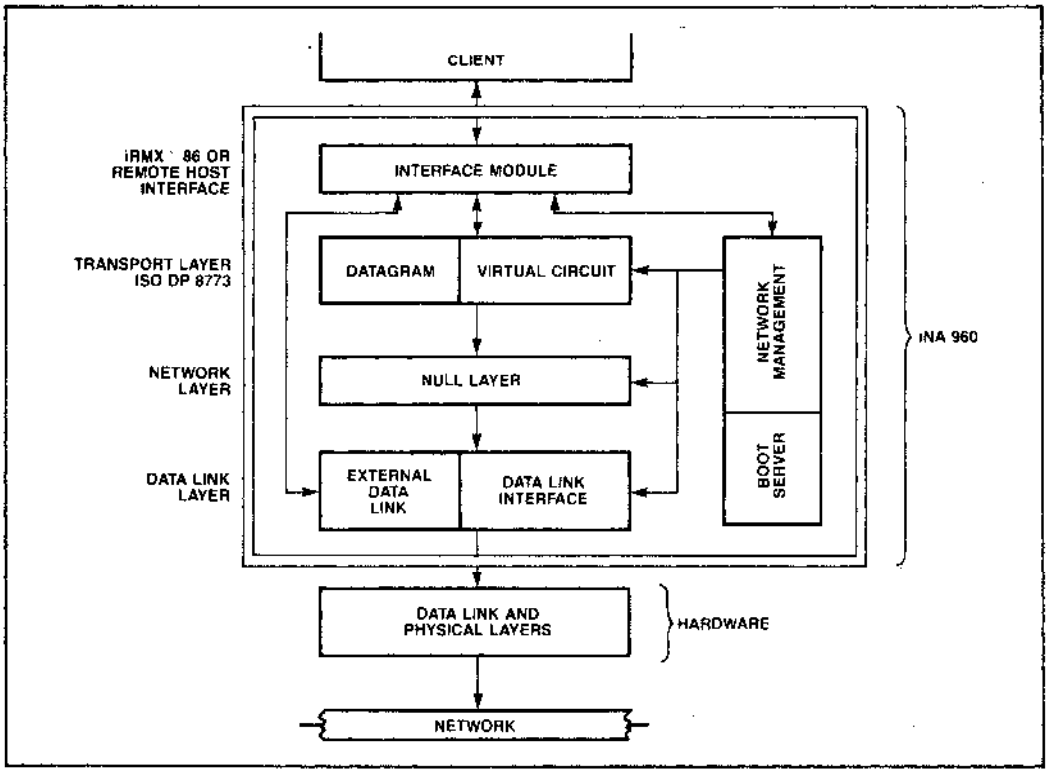


Figure 2. iNA 960 Conceptual Block Diagram

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TRANSPORT LAYER

The Transport Layer provides message delivery services between client processes running on computers (network "hosts" or "nodes") anywhere in the network.

Client processes are identified by a combination of a network address defining the node and a transport service access point defining the interface point through which the client accesses the transport services. The combined parameters, called the transport address, are supplied by the user for both the local and the remote client processes to be connected.

The iNA 960 transport layer implements two kinds of message delivery services: virtual circuit and datagram. The virtual circuit provides a reliable point-to-point message delivery service ensuring maximum data integrity, and it is fully compatible with the ISO 8073 Class 4 protocol. The datagram service provides a best effort message delivery between client processes requiring less overhead and therefore allowing higher throughput than virtual circuits.

Both the datagram and the virtual circuit services are optional and can be included when configuring iNA 960.

Virtual Circuit Services

—Reliable Delivery: Data is delivered to the destination in the exact order it was sent by the source, with no errors, duplications or losses, regardless of the quality of service available from the underlying network service.

—Data Rate Matching (flow control): The Transport Layer attempts to maximize throughput while conserving communication subsystem resources by controlling the rate at which messages are sent. That rate is based on the availablity of receive buffers at the destination and its own resources.

—Multiple Connection Capability (Process Multiplexing): Several processes can be simultaneously using the Transport Layer with no risk that progress or lack of progress by one process will interfere with others.

—Variable Length Messages: The client software can submit arbitrarily short or long messages for transmittal without regard for the minimum or maximum network service data unit (NSDU) lengths supported by the underlying network services.

—Expedited Delivery (optional). With this service the client can transmit up to 16 bytes of urgent data bypassing the normal flow control. The expedited data is guaranteed to arrive before any normal data submitted afterward.

Connectionless Transport (Datagram) Service

The datagram service transfers data between client processes without establishing a virtual circuit. The service is a "best effort" capability and data may be lost or misordered. Data can be transferred at one time to a single destination or to several destinations (multicast).

NETWORK MANAGEMENT FACILITY (NMF)

The network management facility provides the users of the network with planning, operation, maintenance and initialization services described below.

—Planning: This service captures network usage statistics on the various layers to help plan network expansion. Statistics are maintained by the layers themselves and are made available to users via an interface with the NMF.

—Operation: This service allows the user to monitor network functions and to inspect and adjust network parameters. The goal is to provide the tools for performance optimization on the network.

—Maintenance: This service deals with detecting isolating and correcting network faults. It also provides the capability to determine the presence of hosts and the viability of their connection to the network.

—Initialization: NMF provides initialization and remote loading facilities.

Network management provides distributed management of the network; the user can request any of the services to be performed on a remote as well as a local node. The NMF interfaces to every other network layer both to utilize their services and to access their internal data bases.

In support of the above services, the NMF capabilities include layer management, echo testing, limited debugging facilities, and the ability to down line load and dump a remote system.

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Layer management deals with manipulating the internal database of a layer. The elements of these data bases are termed objects. Some examples for objects are the number of collisions, retransmission time-out limit, the number of packets sent, and the list of nodes to boot. NMF can examine and modify objects in a layer's data base.

An echo facility is provided. Using this facility the host can determine if a node is present on the network or not, test the communication path to that node and determine whether the remote node is functional.

NMF enables the user to read or write memory in any host present on the network. This feature is provided as an aid to debugging.

NMF can down line load any system present on the network. A simple Data Link protocol is used to ensure reliability. This facility can be used to load databases, to boot systems without local mass storage or to boot a set of nodes remotely, thus ensuring that they have the same version of software, etc.

Dumping is an operation equivalent to memory read from the user's standpoint; however, dumping uses the Data Link facilities while memory read uses the transport facilities.

EXTERNAL DATA LINK (EDL)

The External Data Link option allows the user to access the functionalities of the Data Link Layer directly instead of having to go through the network and transport layers. This flexibility is useful when the user needs custom higher layer software, or does not need the Network Layer and Transport Layer services (e.g., when sending "best effort" messages, or running customer diagnostics).

Through the EDL the capabilities supporting the lower layers in iNA 960 are made directly available to the user. EDL enables the user to establish and delete data link connections, transmit packets to individual and multiple receivers, and configure the data link software to meet the requirements of the given network environment.

USER ENVIRONMENT

iNA 960 is designed to run on hardware based on the 8086, 8088 or 80186 microprocessors and the 82586 LAN Coprocessor. The software can be configured to run under iRMX 86 or on a dedicated 8086, 8088 or 80186 processor separately from the host. The following section describes these two operating environments.

iRMX Environment

In this configuration, both the user program and iNA 960 are running under iRMX 86. The communications software is implemented as an iRMX 86 job requiring the nucleus only for most operations. The only exception is the boot server option which also needs the Basic I/O System. iNA 960 will run in any iRMX environment including configurations based on the 80130. See Figure 3 for an illustration of iNA 960 running under iRMX 86.

Some of the typical hardware implementations include the iSBC 550 KIT combined with an 8086, 8088 or 80186 based host or the iSBC 186/51 COMMputer™ board integrating the host processor and the communications controller into a single, high performance MULTIBUS board. See Figure 4A and 4B for a conceptual block diagram of these configurations.

Operating System/Processor Independent Implementation

In those systems where iRMX 86 is not the primary operating system, where off-loading the host of the communications tasks is necessary for performance reasons, or where an existing communications front-end processor configuration is being upgraded, the user may wish to dedicate a processor for communications purposes. iNA 960 can be configured to support such implementations by providing network services on an 8086, 8088 or 80186 processor. Figure 5 depicts the conceptual block diagram of this configuration.

This approach provides the component and system designer with an ISO standard communications software building block that can be adapted to his system's needs with a minimum interfacing effort. For added flexibility, iNA 960 provides the user with the alternative of using the included interface module or writing his own module, if necessary.

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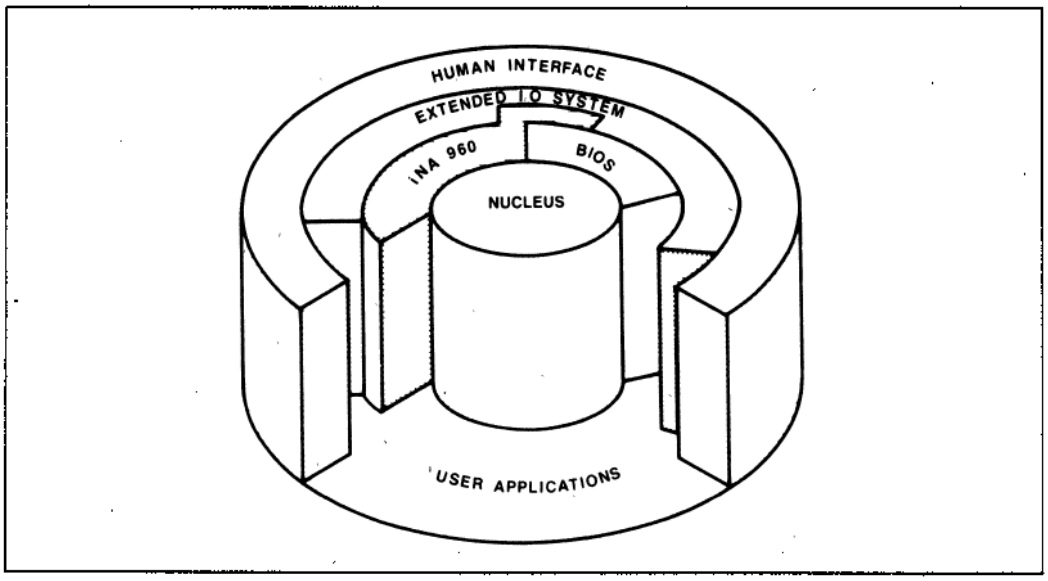


Figure 3. As an iRMX™ job, iNA 960 uses nucleus calls and, when the Boot Server is present, BIOS calls.

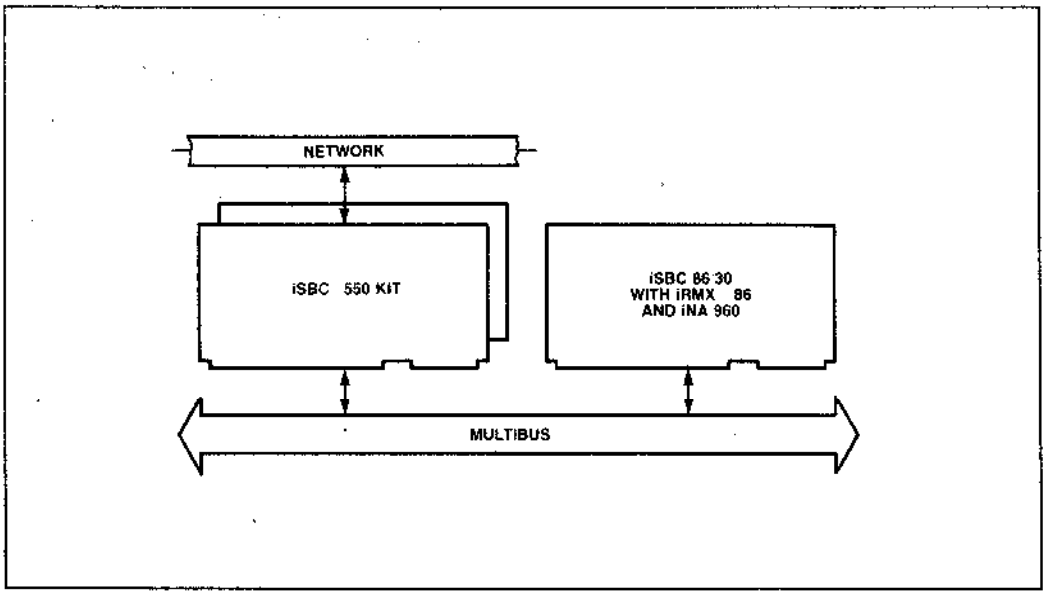


Figure 4A. Typical configuration using iSBC® 550 kit, iSBC® 86/30, iRMX 86™ and iNA 960.

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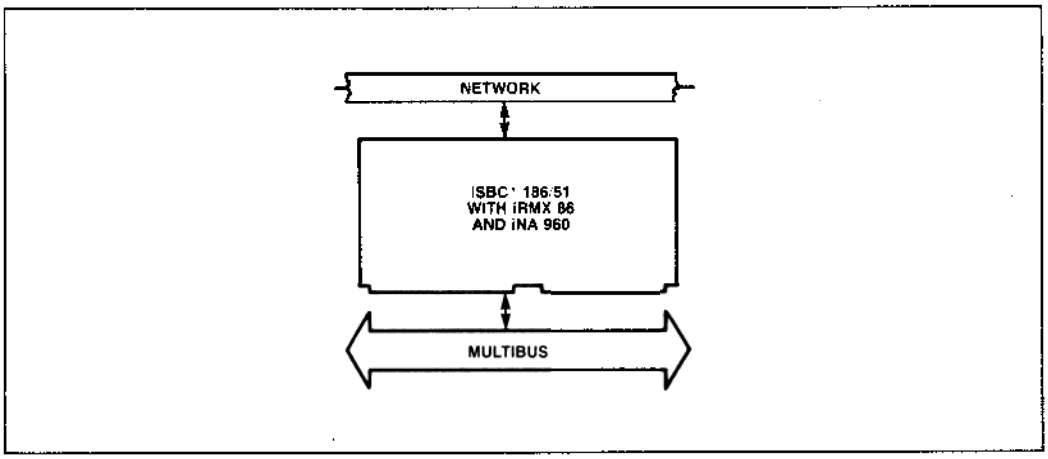


Figure 4B. Configuration using iSBC® 186/51, iRMX 86 and iNA 960.

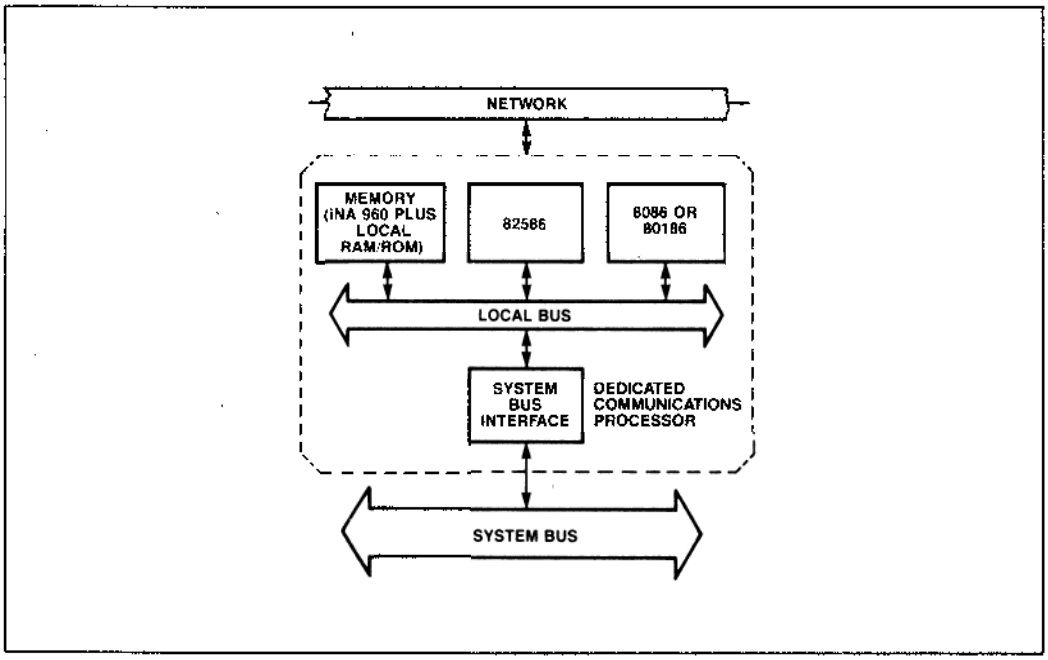


Figure 5. In the operating system/processor independent implementation iNA 960 is running on a dedicated 8086, 8088 or 80186 processor.

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USER INTERFACE

iNA 960 is designed to run both under iRMX 86 and on a dedicated communications front end processor separately from the host. In both environments, the interface is based on exchanging memory segments called request blocks between iNA 960 and the client. The format and contents of the request blocks remain the same in both configurations; only the request block delivery mechanism changes. See Figure 6 for a simplified interface diagram.

Request blocks are memory segments containing the data to be passed from the user to iNA 960 (commands), or from iNA 960 to the user (responses). The iNA 960 request blocks consist of fixed format fields identical across all user commands and argument fields unique to the individual commands. Refer to Figure 7 for the standard request block format.

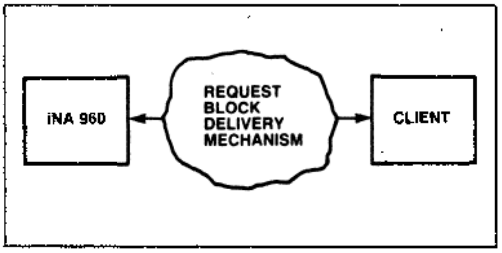


Figure 6.

Issuing an iNA 960 command consists of filling in the request block fields and transferring the block to iNA 960 for execution. After processing the command, iNA 960 returns the request block with one of the pre-defined response codes placed in the response code field of the request block. The response code indicates whether the command was executed successfully or whether an error occurred. By examining the response code, the user can take appropriate action for that command.

For iRMX users, iNA 960 also provides a procedural interface option to simplify writing the application software interface. In this case, the allocation and formatting of request blocks are replaced by a procedure call with parameters that specify the user's command options. The procedure execution will create a request block and fill in the appropriate fields from the user's parameter list.

For component users the request block delivery mechanism is the means by which the host processor and the communications processor running iNA 960 software exchange the request blocks. iNA 960 provides three such mechanisms: the MIP (Multibus Inter-process Protocol), the BCB (Base Control Block) and a user-defined mechanism. The MIP interface is included for use in systems already supporting this protocol; the BCB is a simple interface for single host environments, and the user-defined interface accommodates unique application requirements.

FIELDS	WORD/BYTE	
Reserved (2)	WORD	FIXED FORMAT FIELDS (same for all commands)
Length	BYTE	
User I.D.	WORD	
Response Port	BYTE	
Return Mailbox Token	WORD	
Segment Token	WORD	
Subsystem	BYTE	
Opcode	BYTE	
Response Code	WORD	
Arguments	BYTE	ARGUMENTS (changes by command)
.	.	
.	.	
.	.	

Figure 7. iNA 960 Request Block Format

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Transport Layer User Interface

The following table summarizes the user commands and the corresponding transport layer responses

Command	Function
1. OPEN	Allocates memory for the connection data base of a virtual circuit (or connection) to be established. The connection database contains data concerning the connection
2. SEND CONNECT REQUEST	Requests connection to a fully specified remote transport address using specified ISO connection negotiation options
3. AWAIT CONNECT REQUEST TRAN	Indicates that the transport client is willing to consider incoming connection requests based on pre-established acceptance criteria
4. AWAIT CONNECT REQUEST USER	Indicates that the transport client is willing to consider incoming connection requests. If the request meets the address and negotiation option criteria, it is passed to the client for further consideration.
5. ACCEPT CONNECT REQUEST	Indicates that the connection requested by a remote transport service is accepted by the client
6. SEND DATA or SEND EOM DATA	With this command, the client requests the transmission of the data in the buffers using the normal delivery service of the specified connection. The SEND EOM DATA command signals that the end of the data marks the end of the transport service data unit
7. RECEIVE DATA	Posts normal receive data buffers for a specific connection or for a buffer pool used by a class of connections
8. SEND EXPEDITED DATA	Transmits up to 16 bytes of data using the expedited delivery service. The expedited data is guaranteed to arrive at the destination before any normal data submitted afterward.
9. RECEIVE EXPEDITED DATA	Posts receive data buffers for expedited delivery for a specific connection or for a pool of buffers used by a class of connections
10. CLOSE	Terminates an existing connection or rejects an incoming connection request. Any normal or expedited data queued up to be sent will not be sent
11. AWAIT CLOSE	Requests notification of the client of the termination of a specified connection
12. SEND DATAGRAM	Requests transmission of the data in the buffers using the transport datagram service.
13. RECEIVE DATAGRAM	Posts a receive buffer for a specific receiver or a class of receivers to receive data from a transport datagram.

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Network Management Layer User Interface

Command	Function
1. READ OBJECT	Returns the value of the specified object to the client.
2. SET OBJECT	Sets the value of an object as specified by the client.
3. READ AND CLEAR OBJECT	Returns the value of the specified object to the client then clears the object.
4. ECHO	This function is used to determine the presence of a node, to test the communication path to the node and to ascertain the viability and functionality of the remote host addressed.
5. UP LINE DUMP	Requests a remote node to dump a specified memory area.
6. READ MEMORY	Reads memory of the specified network node.
7. SET MEMORY	Sets memory of the specified network node.
8. FORCE LOAD	Causes a node to attempt a remote load from another node.

External Data Link Interface

Command	Function
1. CONNECT	With this command the client establishes a data link connection.
2. DISCONNECT	Eliminates a previously established connection.
3. TRANSMIT	Transmits data contained in buffers specified by the client.
4. POST RECEIVE PACKET DESCRIPTOR	Allocates memory for maintaining records on receive data buffers. Also may be used to allocate memory for buffering receive data.
5. POST RECEIVE BUFFER	Allocates memory for buffering receive data.
6. ADD MULTICAST ADDRESS	Adds an address to the list of data link multicast addresses.
7. REMOVE MULTICAST ADDRESS	Removes an address from the list of data link multicast addresses.
8. SET DATA LINK I.D.	Sets up a unique data link I.D. for the station.

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CONFIGURING iNA 960

In order to adapt iNA 960 to his specific application, the user must configure the software to define the desired functions, to select the appropriate interface, to set the layer parameters and to set up for the required hardware configuration.

There are a number of capability combinations the user may elect to implement in his application. At the transport layer level the options are: virtual circuit service with or without expedited delivery, or datagram service, or both. At the data link level, the user may include or exclude the External Data Link interface.

The Network Management Facility is also optional. When it is configured in, the user may also include the boot server module. These capabilities can be made available simply by linking in the corresponding software modules. The interface options are also implemented in a modular fashion; the user links in the desired module to set up for the iRMX 86 or the operating system independent configurations.

Layer parameters and configuration options are first edited into layer configuration files, then assembled and linked into iNA 960. Layer parameters adjust the network's operation to match the usage pattern and the available resources. For example, within the Transport Layer, the flow control parameters, the retransmission timer parameters, the transport data base parameters, etc. can be set via this process.

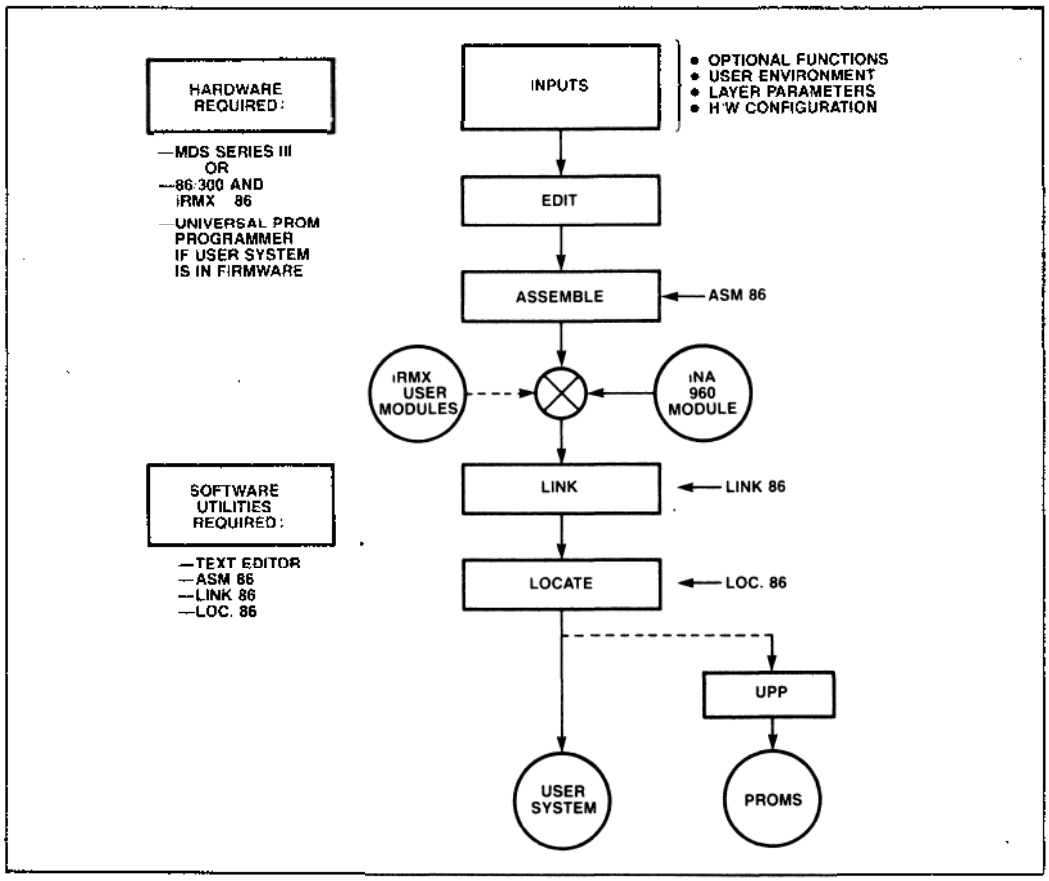


Figure 8. The Configuration Process for iNA 960

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The user also sets up for the required hardware configuration, such as port addresses and interrupt levels, during this process. For the flow diagram of configuring iNA 960, refer to Figure 8.

SPECIFICATIONS

Hardware Supported:

—iSBC 186/51 Communicating Computer.
—iSBC 550 KIT Ethernet controller board(s) configured to run with iSBC 86/30 or iSBC 86/12B Multibus processor boards.
—Custom designs based on 8086, 8088 and 80186 microprocessors and the 82586 Local Communications Controller.

Typical Throughput at transport:

Environments:	
186/51 and iRMX 86	50K to 200K bytes/sec
Dedicated 80186/ 82586 COMMengine	100K to 300K bytes/sec

Memory Requirements: (in bytes)

Base System	12K plus configurable Buffer Memory
Normal Virtual Circuit Option	18K plus configurable Buffer Memory
Expedited Delivery Option	2K
Datagram Option	3K plus Data Base Memory
Net Management Option	1K to 5K
External Data Link Option	5K
Boot Server Option	5K

Available Literature/ Reference Materials:

—iNA 960 Programmer's Reference Manual (11/83)
—iSBC 186/51 Data Sheet (Now)
—iSBC 186/51 Hardware Reference Manual (11/83)

Ordering Information

The following is a list of ordering options for the iNA 960 Network Software. All options include a full year of update service that provides a periodic NEWSLETTER, Software Problem Report Service, and copies of system updates that occur during this period. All of the object code options listed are available on either ISIS or RMX compatible double density diskettes.

As with all Intel software, purchase of any of these options requires the execution of a standard Intel Master Software License. The specific rights granted to users depend on the specific option and the License signed.

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Order Code	Description
iNA 960 YRO	OEM object code license requiring the payment of incorporation fees for each derivative work based on iNA 960; ISIS and RMX formatted diskettes
iNA 960 YST	Object code license to use the product at a second site or facility; ISIS and RMX formatted diskettes
iNA 960 YBY	Object code buy-out license requiring no further payment of incorporation fees; ISIS and RMS formatted diskettes
iNA 960 YSU	Object code single use license only; ISIS and RMS formatted diskettes
iNA 960 ESR	License for machine readable source code of iNA 960. RMX formulated diskettes.
iNA 960 LST	Source listing of iNA 960 provided on microfiche under a special source code license agreement
iNA 960 RF	Order code for the payment of incorporation fees

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NDS-II ELECTRONIC MAIL

- **Improves Project Coordination and Communication**
- **Minimizes "Phone Tag" and Excess Paperwork**
- **Users Can Send and Receive Text or Object Files**
- **MAIL Operates Either Interactively or in Command-Tail Format**
- **User, Group, and "Bulletin Board" Mailboxes Can Be Created**
- **Operates on any Workstation in the NDS-II Development Environment**

Electronic Mail enables users to send and receive messages and files between any nodes on the NDS-II network. In doing so, Electronic Mail improves the communication and coordination between members, reduces "phone tag" and paper generation, aids project configuration management by enabling simplified file transfers, and increases flexibility in workstation location.

The Mail system is governed by an Electronic Mail directory which contains user, group, and bulletin board mailboxes. Each NDS-II user has a mailbox which is only accessible to that user. Group mailboxes are acessible by a defined group of users, and bulletin board mailboxes are accessible by all users. Both group and bulletin board mailboxes can be easily created by any system users.

Users can send a message to any of the mailbox types listed above. Messages can consist of text generated when Mail is invoked, or a text or object file. Options available when sending mail include using a subject string to categorize a message, specifying a message expiration date and time, delaying message delivery until a specific date and time, marking the message URGENT, and maintaining a log of all messages sent.

Users can interactively read their mail and perform the following operations: print messages on their workstation console, delete messages from a mailbox, save messages in a file, forward messages to other users, and reply to message senders. In addition, users can request a mailbox summary which includes, for each message, the sender's name, date sent, subject, urgency, code type (text or object), and message number.

NDS-II Electronic Mail executes on all existing NDS-II workstations using either the iNDX or ISIS-III(N)/ISIS-III(C) operating systems.

TYPICAL MAIL USAGE
• DISTRIBUTE SUPERUSER MESSAGES
• CREATE AND SEND INTERNAL MEMOS
• COLLECT PROJECT MILESTONE DATA
• REPORT PROGRAM BUGS AND RECOMMEND SYSTEM CHANGES
• SEND SOURCE AND OBJECT FILES
• USE AS TELEPHONE MESSAGE CENTER



TYPICAL MAIL BENEFITS
• IMPROVE TEAM COMMUNICATION AND COORDINATION
• REDUCE PHONE TAG
• MINIMIZE PAPER GENERATION
• AID PROJECT CONFIGURATION MANAGEMENT
• INCREASE WORKSTATION LOCATION FLEXIBILITY
• OVERALL, BOOST DEVELOPMENT TEAM PRODUCTIVITY

NDS-II ELECTRONIC MAIL

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OPERATING ENVIRONMENT

Required Hardware
NDS-II Environment with any 8- or 16-bit Microcomputer Development System Workstation

Required Software
iNDX or ISIS-III(N)ISIS-III(C) System Software

DOCUMENTATION
"NDS-II Electronic Mail User's Guide" (122146)

SOFTWARE SUPPORT
This product includes a 90-day initial support consisting of new software releases, updates, subscription services (software performance reports and technical reports), and telephone hotline support. Additional software support services are available separately.

ORDERING INFORMATION

Product Code	Description
iMDX-337	NDS-II Electronic Mail

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iNA955
iRMX™ NDS-II LINK

- Transfers files between iRMX™86-based systems and the NDS-II NRM
- Supports fast and reliable download into iRMX™86 target system
- Supports Intel's 86/310, 86/330A, 86/380 systems
- Configurable at nucleus level with iRMX™86 operating system
- Operates through Ethernet communications controller and cable connected to NDS-II
- Utilizes Ethernet technology with data transmission speeds at 10M bits per second

The iNA955/iRMX™ NDS-II LINK is a software package that allows an iRMX based system 86/310, 86/330A, or 86/380 system to be connected to an Intel Network Development System (NDS-II) network via an Ethernet coaxial cable or Intellink™ module.

iRMX system developers can use the Series II, III, IV and Model 800 for editing, compilation and debugging to develop, store, and manage software programs at the Network Resource manager. Using iNA955 these developers can download programs at Ethernet speeds from the Network Resource Manager into their target iRMX hosts for execution and system integration.

System developers can also use the iNA955 programmatic interface to develop their own application programs which run in the iRMX environment and interface with the NRM. This is a way for OEM developers to customize the operating environment to suit their own application.

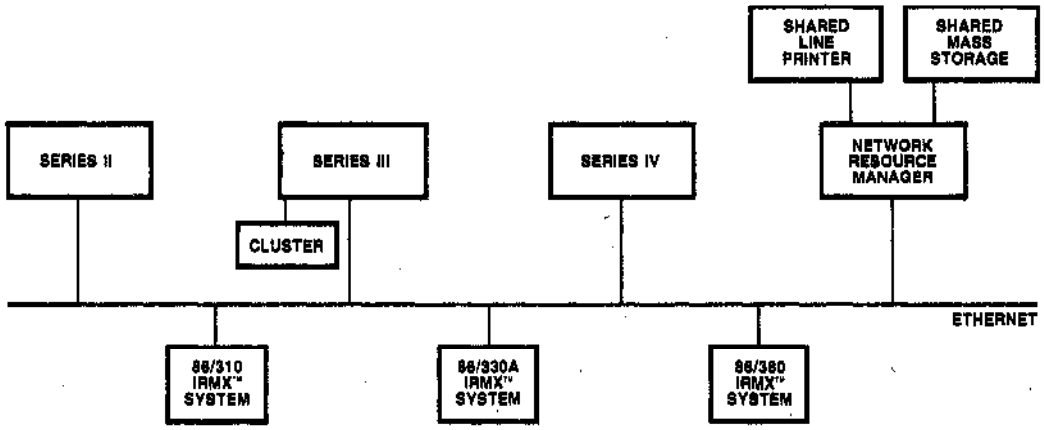


Figure 1. Example of NDS-II Configuration using the iRMX™ NDS-II LINK

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NDS-II OVERVIEW

The NDS-II is a distributed processing local area network optimized for development of microcomputer-based products. It addresses the needs of both software and hardware engineers by providing the base environment for shared development tools plus the capacity for expansion.

An NDS-II network consists of an NRM which serves as the file server for a variety of Intel's development systems. These development systems include Series II, Series III, Series IV, and Model 800. By configuring iNA955 into an iRMX 86 system, an iRMX system can also be served by the NRM.

NDS-II's Network Resource Manager (NRM) manages all workstation requests for network resources. NRM tasks include service of workstation file requests, printer spooling, management of the distributed Hierarchical File System, the Distributed Job Control System and network maintenance functions such as user-name creation, file archival and system generation.

iNA955 provides a basic upload/download file transfer capability between an iRMX 86 system and the NRM. When used with an iSBC® 550 Ethernet controller, iNA955 allows users at iRMX 86 systems to move files between iRMX systems and the NRM, list directories at the NRM, delete or rename files at the NRM and copy files between two directories on the same NRM.

Access to files is accomplished using two interfaces:

A A CUSP interface which operates on the network file system in a manner similar to iRMX CUSPS which operate on local iRMX files under a full iRMX operating system.

B A programmatic interface which allows user programs running with a iRMX nucleus to access files at the NRM. These interfaces are similar to those present in UDI and EIOS.

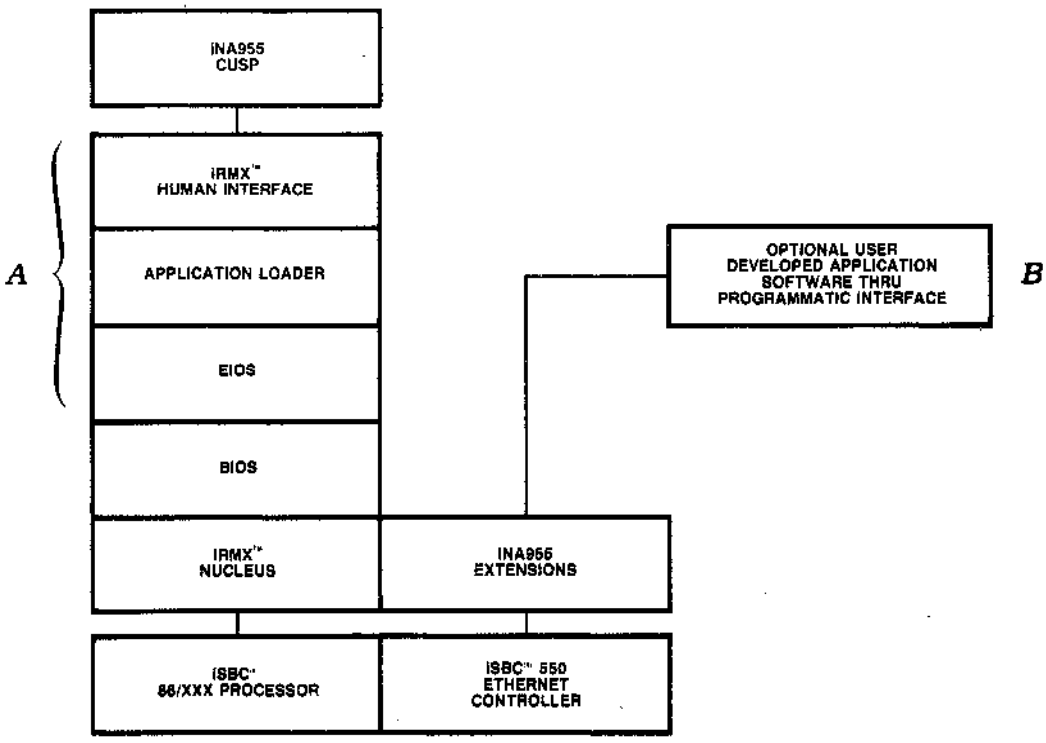


Figure 2. iNA955 Functional Diagram

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FUNCTIONAL DESCRIPTION

iNA955/iRMX NDS-II LINK consists of a program which runs on the system 86/3XX family of host computers. iNA955 executes under the iRMX 86 operating system and uses the local iRMX file system.

The iRMX-based host computers communicate with the NRM via iNA (Intel Network Architecture) which is based upon Ethernet communication protocols. These protocols are supplied by the iSBC550 board set which must be included in the iRMX host system since iNA955 uses the iSBC550 to communicate over Ethernet.

The following tables summarize the user commands and programmatic calls with their descriptions.

User Interface Commands	Function
NACCESS	examines/changes NRM file access rights
NCREATE	creates NRM directory
NDELETE	deletes NRM file
NDIR	examines NRM directory
NLOGOFF	logs off from NRM
NLOGON	logs on to NRM
NRCOPY	copies file from NRM to iRMX station
NNCOPY	copies NRM file to NRM file on the same NRM
RNCOPY	copies files from iRMX station to NRM
NRENAME	renames NRM file or directory

Programmatic Calls	Function
NQ$CHANGE$ACCESS	change access of file on the NRM
NQ$CREATE$DIR	create directory on the NRM
NQ$DELETE	delete file on the NRM
NQ$FILE$INFO	get information of file on the NRM
NQGETVIRTUAL$ROOT	get names of volumes at NRM accessible to user
NQ$LOGOFF	logoff user from the NRM
NQ$LOGON	logon user to the NRM
NQ$OPEN	open file at the NRM
NQ$READ	read contents of file at the NRM
NQ$READ$DIR$ENTRY$EXP	read expanded directory entry at the NRM
NQ$RENAME	rename file at the NRM
NQ$WRITE	write file to the NRM

Configuring iNA955

Like other iRMX systems iNA955 must be configured according to the system environment. To assist you in configuring your system, iNA955 comes with a configuration template. The file containing this template is contained on the release diskette. This template is designed to be self-explanatory.

The user has the option of integrating into his applications the iNA955 CUSPS. iNA955 CUSPS require the iRMX Human Interface to execute.

Physical Connections

The physical Ethernet connections can be made either through an "Intellink"™ module or through transceivers and the Ethernet cable. The Intellink module serves as an Ethernet local station concentrator. It allows workstations to be located up to 50 meters from the Intellink module and has 9 ports for connecting the NRM and workstations, and one port for connecting an Ethernet cable or other Intellink modules.

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SPECIFICATIONS

Operating Environment

HARDWARE SUPPORTED

- System 86/310
- System 86/330A
- System 86/380

HARDWARE REQUIRED

- iSBC® 550 Ethernet Communication Controller Set

SOFTWARE REQUIRED

- iRMX™86 Operating System version 5.0
- NDS-II System software Release 2.5 or greater

Software Supplied

MEDIA

One 8 inch, single sided, double density iRMX™86 format diskette
One 5¼ inch, single sided, double density iRMX™86 format diskette

PROGRAMS

- iRMX/NDS-II LINK software linked into iRMX system library
- Examples of iRMX Integration Configuration utilities
- iSBC550 Diagnostics

DOCUMENTATION

- iNA955/iRMX NDS-II LINK Installation and User's Guide, Order Number 12256-001
- Complete NRM and Network operating manuals are included with the NDS-II systems
- iSBC550 Ethernet communications controller Hardware Reference Manual 121746.

ORDERING INFORMATION

Part Number	Description
iNA 955	iRMX/NDS-II Link
iSBC 550	Ethernet Communication Controller Set
iMDX 457	10 meter transceiver cable
iMDX 458	50 meter transceiver cable
iDCM 911-1	Intellink Module
iMDX 3015	Ethernet transceiver kit
iDMX 3016-1	25 meter Ethernet coaxial assembly
iMDX 3016-2	100 meter Ethernet coaxial assembly

Installation

On-site installation is included with the NDS-II Network Resource Manager. iNA955 is customer installable.

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iRMX™ 510
iDCM SUPPORT PACKAGE

- **Low cost remote communication/ control expansion for MULTIBUS® based systems**
- **Extends functionality of BITBUS™/iDCM systems**
- **Software development support for BITBUS™/IDCM products: iSBX™ 344 and iRCB 44/10 boards**
- **Simple software interface for iRMX™ 86, 286, 88, and iPDS™ ISIS operating system compatibility**

The iRMX™ 510 iDCM Support Package contains the necessary software tools to interface MULTIBUS®, and iPDS™ ISIS systems to BITBUS™ systems in both a development environment and during run-time. With other members of the Distributed Control Modules family, the iRMX 510 iDCM Support Package expands Intel's OEM Microcomputer Systems capabilities to include distributed real-time control.

The iRMX 510 Package software interface handlers and the iSBX™ 344 BITBUS Controller MULTIMODULE™ board extend the capabilities of other microprocessors such as the 8086, 80186, or 80286 in iDCM, MULTIBUS, or iPDS systems. Support of iRMX 51 applications is provided via the iRMX 51 libraries incorporated in the iRMX 510 Support Package. Also, the Support Package completes the development environment for BITBUS/iDCM products : iSBX 344 and iRCB 44/10 boards. When used with an ICE-44 Emulator the iDCM controller is accurately simulated resulting in a highly effective product development effort.



ORDER NUMBER: 230972-001

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MULTIBUS®, iPDS,™ and iDCM SYSTEM EXPANSION

The iRMX 510 Support Package provides the software interface between Intel's MULTIBUS and iPDS environment, and the BITBUS environment. With Intel's Distributed Control Modules hardware interface, the iSBX 344 MULTIMODULE board, this capability enables the user to expand the existing functionality of an iRMX-based SYSTEM 310, for example, to include control and monitoring of a material handling operation. Intel's Personal Development System (iPDS) can be used as a central supervisory station for data acquistion in a laboratory or for program development. The iRMX 510 iDCM Support Package provides a general purpose interface. For custom applications, users may wish to develop a custom interface.

OPERATING ENVIRONMENT

The iRMX 510 Support Package is supplied on diskettes formated for iRMX, Intellec® Series II or III and iPDS ISIS development systems. Application programs or tasks residing on an extension in the iDCM environment may use the iRMX 510 interface. (Application programs or tasks are written in iRMX 88, 86 or ISIS compatible code.) Some examples of extensions in an iDCM system are the iSBC 86/05, 88/25, 186/03 boards and the iPDS system. Figure 2 shows how the iRMX 510 interface is integrated into an iDCM system.

For iRMX 86, 88, or 286R-based systems, configuration of the iRMX 510 interface requires two steps: configuring the interface to the hardware and then the supporting executive. Hardware configuration requires creating a file of configuration parameters, compiling it, and linking the result with the application program. When using the iRMX 510 Package with the iPDS ISIS system, hardware configuration is not required.

ARCHITECTURE

The major functional blocks of the iRMX 510 Support Package are: iRMX 86, 286R, 88 and iPDS ISIS parallel interface handlers, iDCM Controller firmware files, and iRMX 51 include files.

Simple Parallel Interface Handlers

The iRMX 510 Support Package includes parallel interface handlers for systems using the iRMX 86 or 286R Operating System, the iRMX 88 Executive, or Intel's Personal Development System ISIS Operating System. These software handlers pass iRMX 51 messages to and from the iSBX 344 parallel interface (Byte FIFO). In iRMX 86, 286R or 88 — based systems , the interface executes as two tasks: one to transmit, the other to receive the message. In iPDS systems the interface is a procedural call: DCM TRANSMIT, DCM RECIEVE, or DCM STATUS CHECK. In both cases the handlers are straightforward and easy to use. Figure 1 illustrates transmission of a message in an iRMX-based system.

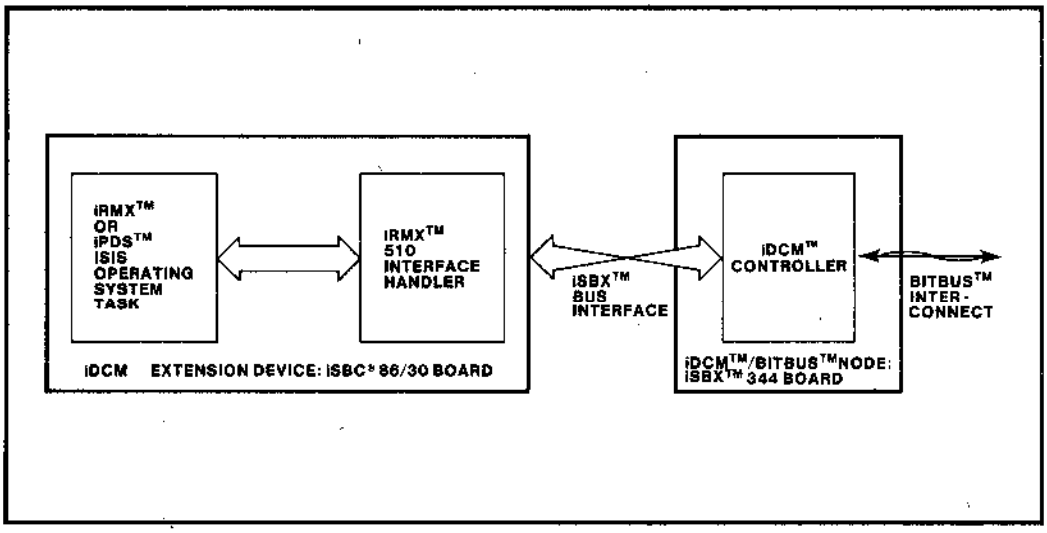


Figure 1. Message Transfer to an iDCM System

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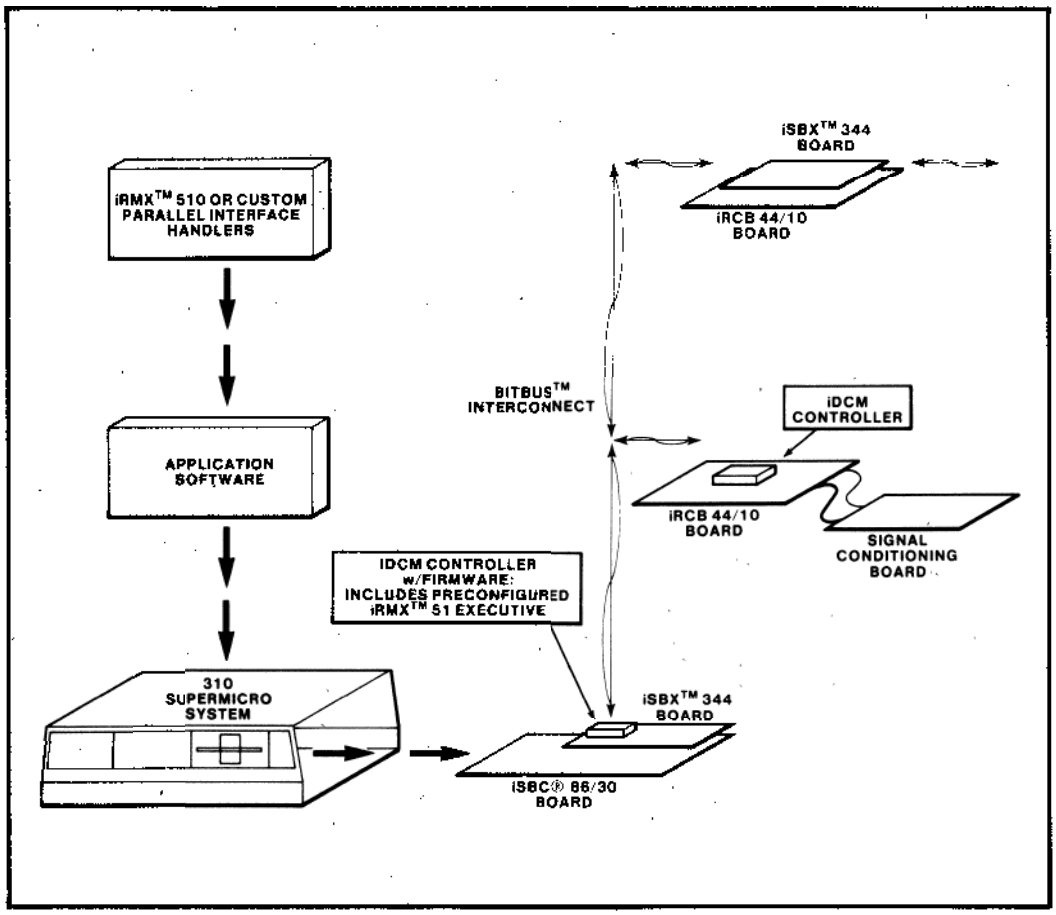


Figure 2. iDCM Operating Environment

The software handlers ease integration of other processors into an iDCM system and provide the tools to quickly expand a MULTIBUS system, or an iPDS ISIS system. Significant reduction in application system software development time results, with more effort concentrated on the overall application.

iDCM Controller Firmware

Also included in the iRMX 510 Support Package is the iDCM Controller firmware in loadable object files, iRMX 51 libraries, and iDCM Controller Include files. An Intellec Development System and ICE-44 Emulator can be used with the loadable object files to accurately simulate the iDCM Controller. This capability significantly decreases development effort by reducing trial and error production of application system software. The iRMX 51 Interface Library and iDCM Controller Include files allow development of user code for iDCM systems.

DEVELOPMENT ENVIRONMENT

The iRMX 510 Support Package completes the development environment for iDCM application system development when used with an Intellec Series II or III Development System and In-Circuit Emulator (ICE-44), or an iPDS system EMV-440 and the 8051 Software Development Package. As part of Intel's complete development environment for the 8051 family of microcontrollers, the iRMX 510 Support Package may also be used with an iPDS system and EMV-51 or an Intellec Series II or III Development System and an ICE-51 Emulator.

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SPECIFICATIONS

Supported Hardware/Software for iDCM Systems

Operating System	Supported Extension*
iRMX 86 Release 5.0	iSBC 86/05, 86/14, 86/30, 186/03, 186/51, 188/48, 88/25, 88/45 boards
iRMX 88 Release 3.0	iSBC 86/05, 86/14, 86/30, 186/03, 186/51, 188/48, 88/25, 88/45 boards
iRMX 286R	iSBC 286/10 board
ISIS Release 1.0 (PDS)	iPDS System

*Each extension device uses an iSBX 344 BIT-BUS Controller MULTIMODULE Board

Supported Hardware — 8051 Microcontroller Family

8051	80C51
8052	8044
8751	8744
8031	80C31
8032	8344

Compatible Software
iRMX 86 Release 5.0
iRMX 286R
iRMX 88 Release 3.0
iPDS ISIS Release 1.0
iRMX 51 Release 1.0

Development Tools
ICE-51 or ICE-44 Emulators
iPDS System with EMV-51
Intellec Series II or III Development System
8051 Software Development Package

Reference Manual

146312-001 — Guide to Using the Distributed Control Modules (Supplied)

Ordering Information

Part Number	Description
iRMX 510BY	iDCM Support Package w/ Reference Manual A,B,E, and F Media Formats Supplied.

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Systems and Applications Software

6

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SYSTEM & APPLICATION SOFTWARE

Thus far in this Handbook you have read about a rich set of software available for Intel's hardware and offered by Intel. Almost all of this software is targetted at the programmer or the engineer, i.e. to highly technical and specialized audiences that are intimately familiar with computers. Intel also has software which can be used by the non-programmer to help him solve problems in his professional arena.

The professional end user (and the Value-Added Reseller who targets his systems at the professional end user) is rapidly evolving as the largest segment of the computer user base. With predicitions that within a decade every professional will have a computer on his (or her) desk or at least readily available, it is easy to see the need for generalized tools to help improve the productivity of these masses.

The advent of the Personal Computer not only made such predicitions plausible but it has already defined many of these tools as necessary for professional productivity: spreadsheets, electronic mail systems, word processors, and graphics displays.

The passage of time and shifting emphasis of our educational systems have also impressed upon these professionals the importance of the data residing in their corporate data processing computers — and their work environment has shown them explicitly what is meant by the data processing application backlog. Database management system (DBMS) is a term now familiar to most professionals.

A demand for combining the benefits of the corporate mainframe with those of the personal computer is now emerging as users see needs for sharing their data and the work performed by other users, for accessing subsets of the mainframe DBMS but not being constrained by the DP backlog, and for doing these things without the constant assistance of a "compute guru". Multi-user small systems with data extract facilities, host communications, PC links, and remote file transfer capabilities are beginning to address this need.

Intel is responding well to this emerging demand. Our multi-user XENIX-based systems are ideally suited for this environment. Our mainframe DBMS SYSTEM 2000 product family, which provides sophisticated data manipulation services, also offers user-friendly non-programmer facilities for today's professional.

In addition, Intel has in place an active and successful program for attracting, qualifyiing, and referencing third-party software to execute on our systems.

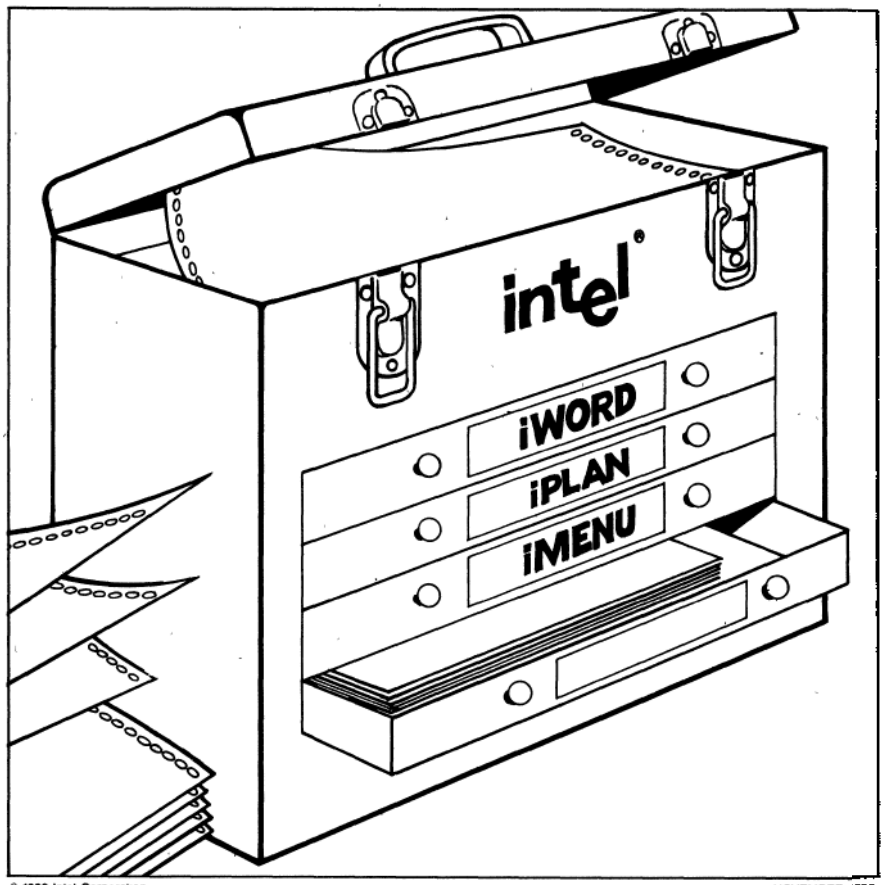
The Intel Database Information System (iDIS 715) is a multiuser XENIX 286-based microcomputer system that includes a complete set of end-user productivity and application development tools. The iDIS system can be purchased as an integrated hardware/software microcomputer system configured for specific departmental computing applications. In addition, the various iDIS productivity tools, application development tools, relational database management system, and communication software options can be purchased separately to run on XENIX-based Intel microcomputers.

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intel®

XENIX* Productivity Software Tools

- iWORD Processing
- iPLAN (Multiplan*) Spreadsheet
- iMENU Development System



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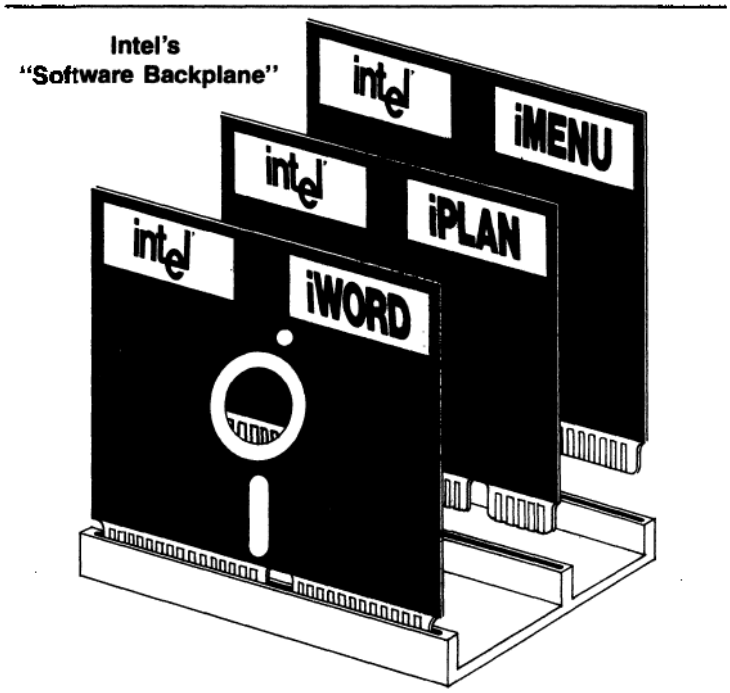
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INTRODUCTION

Software tools for the XENIX environment

Intel's productivity software tools are designed to meet the basic information processing needs of the office environment. Tailored specifically for the XENIX* operating system, the software tools are available as individual packages which can be applied to specific end-user tasks. Intel's application packages are also offered as a Seamless™ set of software tools, integrated with a hardware/software system such as Intel's Database Information System (iDIS™ 86/735). Seamless software tools support the transparent sharing of data files among various application packages with complete data integrity. With Seamless software, results from one application package are readily accessible and compatible as input for another form of processing.



iWORD*

- **Standard text editing/formatting commands**
- **Designed especially for the XENIX operating system**
- **Easy-to-use for beginners, powerful for experts**
- **Full-screen text editor**
- **Access to XENIX typesetter and printer drivers**
- **Embedded commands for global formatting**
- **On-screen display of formatted text**
- **On-line Help facility, spelling/dictionary module, and mail/merge facility**
- **Worldwide service and support**

The powerful, versatile word processing tool

Intel's iWORD package is a sophisticated, yet friendly word processing tool for preparing business documents, such as reports, letters, memoranda, technical papers, and more. Written in the "C" language and tailored to the XENIX operating system, the iWORD package can run in both multi-user and single-user environments. Menu-driven and screen-oriented, the iWORD package supports all standard text editing, storage, and formatting development functions.

An efficient, easy-to-use text processor

Inexperienced users will find the iWORD software concepts intuitively easy. For example, the user accesses a document file by opening a "drawer," and editing commands follow familiar "cut and paste" procedures.

All commands are in plain English. No memorization is necessary, and many operations are executed by a single keystroke. Concise command menus and an on-line Help facility are continuously available so that novice users can quickly advance in their word processing abilities. The iWORD system is sufficiently powerful to meet the needs of more experienced users as well.

Designed around office needs

Intel's iWORD software is based on the simple concept of an office file cabinet, defined by a collection of drawers, each of which contains files (documents).

The user may:

- Open an existing drawer or make a new drawer
- Create a new file or select an existing file
- Rename a drawer or file
- Add to, change, copy, move or delete the selected file.

There is no limit to the number of user-created drawers other than the availability of disk storage space.

*iWORD is a version of Horizon Word Processing, a trademark of Horizon Software Systems, Inc.

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On-screen display of formatted text

The word processor allows users to visually format documents and print them as they are displayed on the terminal, or to format them with the powerful text processing facilities inherent to the XENIX operating system. This on-screen display capability is particularly helpful in preparing documents for typesetting.

The results of text formatting commands appear immediately on the screen. Examples of these commands include:

- Right justification
- Underlining
- Indentation
- Centering
- Alignment.

Advanced word processing features

Inexperienced users may execute commands from a simple menu (and related Help screens), while more proficient users may opt to use up to 64 function keys without accessing the menu.

The iWORD system allows simultaneous support for multiple character and/or line printers at the local or system level; printer selection is an operator option at print time.

The iWORD package includes a spelling checker and correction facility with an extensive on-line dictionary.

A Mail/Merge facility is available to combine mailing lists and document files (e.g., form letters) for printer output. Mail/Merge also provides the capability of incorporating paragraphs from a third file.

The iWORD processing allows on-screen sorting of numeric or alphabetic text.

Special editing commands

- Find commands ("string search") to locate characters or words in text for possible changes or additions
- Deletion commands for removing words, sentences, lines, paragraphs and entire files
- Fill commands to fit as many words as possible in a finite space
- Form command to type over existing text
- Command to mark location of the cursor within text
- Paste-in command to copy a section of text
- Replace command that replaces one text area with another
- Tab setting commands

Embedded "dot" commands

When formatting or printing needs are complex, the user has easy access to more powerful embedded "dot" commands. "Dot" commands are most useful for medium-sized and long documents requiring sophisticated formatting functions like subscripts, superscripts, and footnotes. "Dot" commands are fully compatible with NROFF and TROFF, the XENIX-supplied printing and typesetting utilities. The results of "dot" commands are displayed on-screen before the document is printed.

Embedded commands for global formatting include:

- Page layout
- Justification
- Automatic hyphenation
- Running headers and footers
- Footnotes
- Superscripts and subscripts
- Automatic page numbering
- XENIX typesetting commands (TROFF)
- XENIX printing commands (NROFF).

Editing two files simultaneously

The iWORD package provides a moveable "window" into a file for full-screen text editing. The user may simultaneously display two areas of the same document or two different documents in two screen "windows." Employing this "split screen" capability, the user may review two different files at the same time, as well as move text between files.

Designed for experienced and novice users

The iWORD software provides the experienced word processing user the full strength of XENIX text preparation commands, such as NROFF and TROFF. The iWORD package also offers a comprehensive menu shell which makes the word processing software easy to use for even the most inexperienced computer user. In conclusion, the iWORD system is a powerful, "user friendly," and flexible word processing package intended for all levels of computer proficiency.

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iPLAN*

- **Industry standard advanced electronic spreadsheet functions**
- **Sophisticated formatting options**
- **Easy-to-use English commands**
- **Extensive, on-line Help facilities**
- **Scrolling features and multi-window/multi-table display**
- **Links and updates multiple interrelated spreadsheets**
- **Automatically updates calculations**
- **Worldwide service and support**

The most advanced electronic spreadsheet

The iPLAN Multiplan Spreadsheet software is one of the most powerful, easy-to-use "electronic worksheet" programs available. Developed by Microsoft Corporation, Multiplan has been enhanced for Intel hardware environments operating under XENIX.

The iPLAN package is a multipurpose tool capable of a wide variety of business and scientific applications: financial modeling, planning, forecasting, tabulations, calculation of engineering formulas, and much more. It supports "what-if" decision-modeling with a versatile two-dimensional matrix that can be custom-tailored for specific use.

Unlike other spreadsheets, the iPLAN system is designed to meet the needs of both inexperienced and sophisticated computer users. It also offers versatile presentation and reporting capabilities.

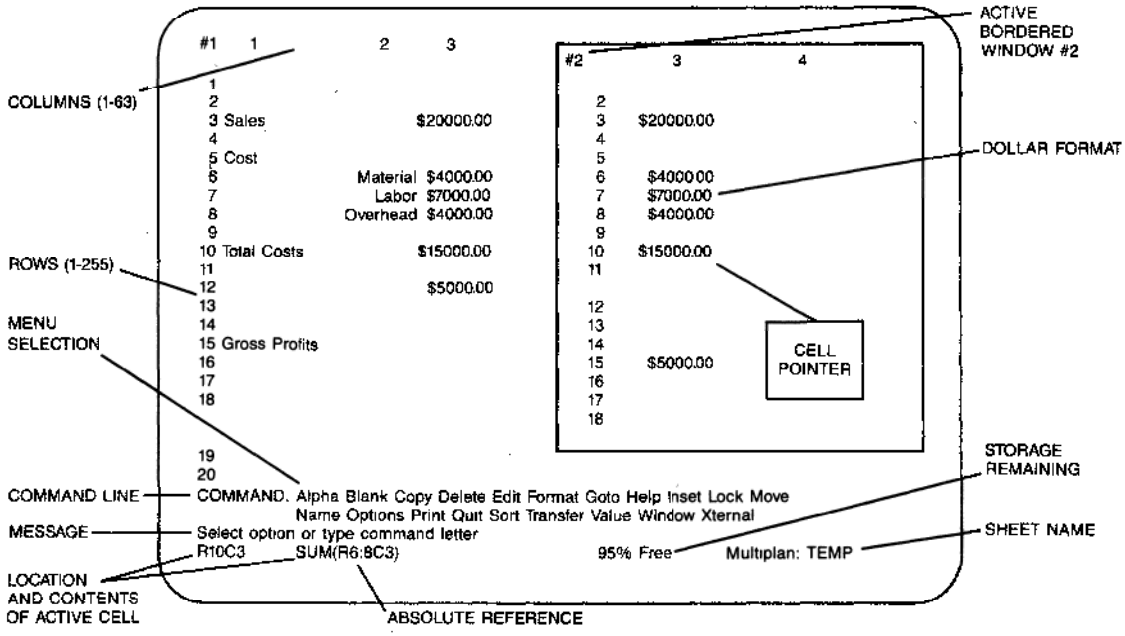
The iPLAN matrix format

The iPLAN software displays numerical data, text, or formulas in matrix (row/column) format. The spreadsheet screen is divided into 'cells' which are referenced by row and column numbers. Cells may contain numeric data, formulas, text, or labels. Commands are listed at the bottom of the screen along with the current addressed cell, the amount of unused spreadsheet storage space, and the name of the file in use.

Designed for ease-of-use

Beginning iPLAN users can start building worksheets after a couple hours of initial use. While simple to operate, the iPLAN system functionality is enhanced by the skill of the user.

* iPLAN is a version of Microsoft Multiplan, a trademark of Microsoft Corporation.



Typical Multiplan Screen Display

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The iPLAN package does not use cryptic, abbreviated commands or reference codes (e.g. "AZ23"). Instead, it uses plain English commands (e.g. COPY) and reference names (e.g. COSTS or SALES). Completely menu-driven, the iPLAN software prompts the user with simple commands that can be executed with a single keystroke. To help in command selection, the user can access a reference guide.

Notable iPLAN features include:

- Ability to build formulas by highlighting cells
- Menu-driven functions and command prompting
- Plain English command words and formulas
- Comprehensive on-line reference guide
- Eight-window display option
- Full-screen display of worksheet formulas.

A dynamic, versatile workspace

The iPLAN package offers an effective workspace that is 63 columns wide by 255 rows long. Worksheets are easily designed to fit project requirements. Moreover, worksheets can be linked to automatically receive or transmit data into other related iPLAN worksheets. Column width can be varied to accept long (or short) words and numerals; lines of text can be typed across several columns.

Up to eight windows are available with vertical and horizontal scrolling, such that different areas of a very large worksheet can be viewed simultaneously. The windows can be aligned, scrolled together, opened, or closed at the user's choice.

Built-in data security

The iPLAN software features cell locking to protect worksheet data. When data and formulas have been entered, the specified information can be "locked" in place so that vital data cannot be accidentally erased or altered.

Flexible presentation features

The iPLAN system enables users to produce printed reports of professional caliber. The program includes special formatting, alignment, and printing functions that support the printing of presentation-quality reports. The iPLAN software can automatically break a spreadsheet into multiple pages, and the user can specify the appropriate margins.

Powerful modeling capabilities

Highlights of iPLAN modeling features include:

- Alphabetical or numerical sorting capabilities
- Links and automatically updates up to eight interrelated worksheets
- Automatically updates subtotals, totals, percentages, growth curves and other calculations
- Performs multiple iterations to solve closed-loop problems
- Automatically revises formulas when reordering rows and columns in displays
- Cells and areas can be named for clarity
- Continuous formatting allows entries across cell boundaries
- Formulas moved to various worksheet locations without retyping
- Includes special editing area for quick additions or deletions
- Sheet display may be redesigned or formatted in various ways without altering the stored data
- Formulas, words, or numerals can be entered into any location so that printed sheets have titles and descriptions
- Offers a rich repertoire of advanced math functions and operators.

iMENU*

- **Hierarchical control of menu screens to organize application program use**
- **On-line application development/maintenance system**
- **A menu screen design and menu development system for non-programmers**
- **On-line Help facility**
- **Written in the "C" language, specifically for XENIX**
- **Supports turnkey application development**
- **Worldwide service and support**

Simplifies use, development and maintenance of XENIX-based applications

The iMENU software package is a hierarchical user interface and application development tool that ties together XENIX-based applications to achieve a high level of software integration. The iMENU package allows applications developers to create integrated, logical, and friendly interfaces to XENIX applications.

In effect, the iMENU system allows the XENIX operating system to appear transparent to the non-technical user, while it offers all the power and functionality inherent to XENIX to the more experienced user. The iMENU package interfaces with virtually all character-oriented terminals.

Aids application development and software packaging

Programmers and experienced users can apply the iMENU system in maintaining or creating menus, forms, or Help screens for existing or new applications.

* iMENU is a version of Schmidt's /menus, a trademark of Schmidt Associates.

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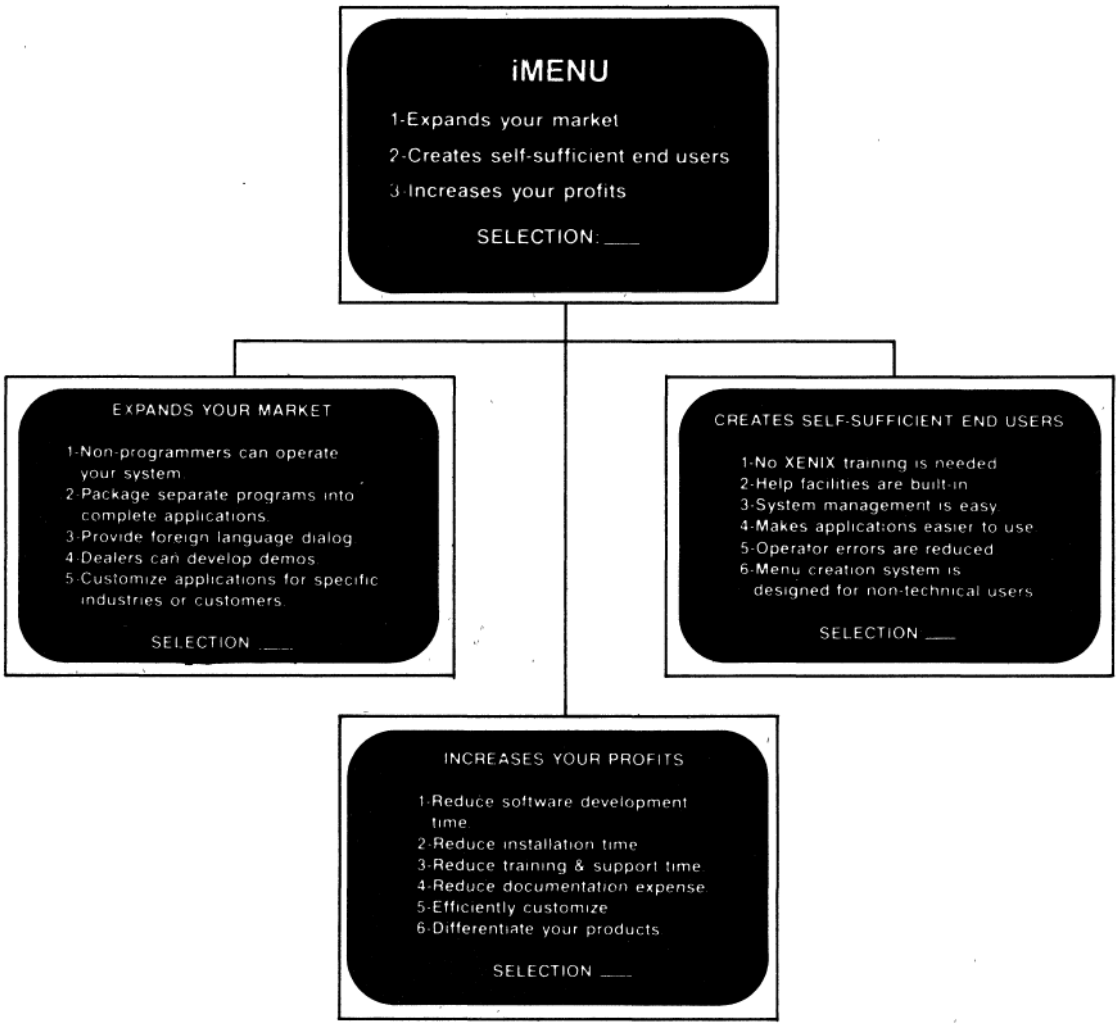
Full XENIX functionality is retained and simplified with the iMENU software. Experienced users have the option of skipping step-by-step menu selection via the fast menu selection mode. Advanced users can also modify the menu system to reflect changes in existing applications or to incorporate new applications.

Standard iMENU package functions include:

- Definition of login IDs
- Add, delete, and list login IDs
- Authorization control
- Define, update, delete and list menu items and attributes
- Screen and forms building
- Interaction with XENIX shell commands
- Powerful macros
- Fast menu selection mode for experienced users
- On-line Help facility.

The iMENU software includes a Menu Development Subsystem, which is a menu-driven set of maintenance functions allowing:

- Menu screen maintenance
- Form screen maintenance
- Help screen maintenance
- Menu selection maintenance
- Macro maintenance
- Shellscript maintenance
- Login ID maintenance
- Deauthorization maintenance
- Backup/restore.



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Comprehensive on-line Help system

The Help system is an interactive user-assistance facility. The Help system is completely integrated with the iMENU package so the user need not rely on bulky reference manuals to operate a particular application. In the event the user encounters problems or has questions, explanatory solutions can be made available at all times. Using the iMENU system itself, programmers and experienced users can extend or modify the Help system to include new applications.

Expands markets and increases profits

Systems integrators will find the iMENU system to be an indispensible tool for packaging XENIX-based applications software and integrated hardware/software systems.

Using the iMENU package, application developers can:

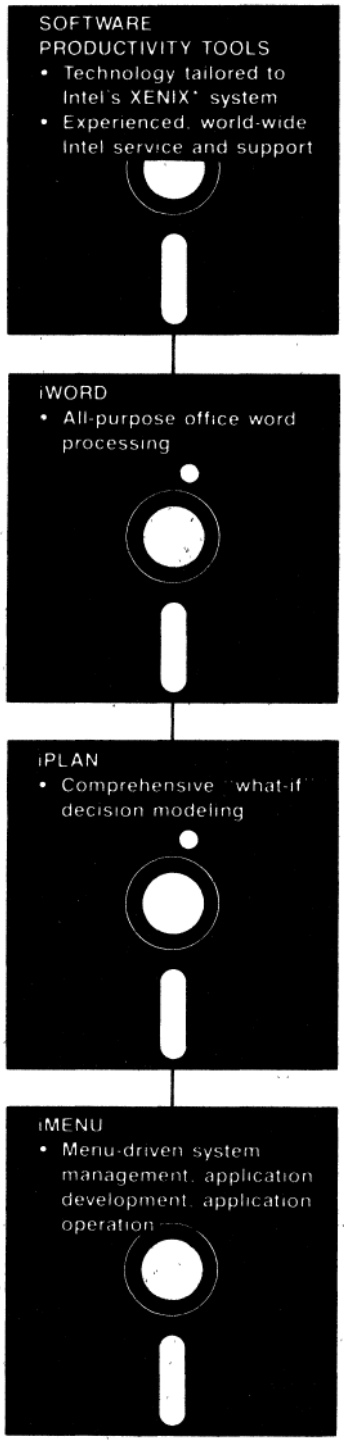
- Extend the user-interface to wrap around new and existing applications software
- Customize existing applications to meet varying customer needs
- Develop application demos
- Create applications that are easily used by non-programmers
- Package separate programs into integrated applications.

The iMENU software enhances the cost-effectiveness of application development by:

- Improving time to market for new software products
- Reducing software development time
- Reducing the need for training and support
- Decreasing software installation time
- Cutting documentation expenses
- Unifying a family of software products for consistent screen appearance and operation.

Integrated software for the iDIS system

Intel's Database Information System (iDIS 86/735) provides end users and systems builders with a vehicle for incorporating a Seamless set of software productivity tools. Seamless software supports the transparent sharing of data files among application packages with complete data integrity. The iDIS system is a multi-user, multi-tasking XENIX-based microcomputer available with the iWORD processor, the iPLAN spreadsheet, the iMENU development system, iXTRACT communication facilities for downloading mainframe databases, the iDB DBMS for local relational database management, and software that supports networking of personal computers. Application development tools and high-level programming languages are also offered with the iDIS system. Data can be transferred among the Seamless software packages, and the iDIS menu system and iHELP facility provide a friendly, common user interface. The iDIS system is an example of how Intel provides hardware/software components at all levels of integration to meet individual system needs.



Worldwide service and support

All Intel software included under an active software maintenance agreement is fully supported by Intel's staff of trained software engineers. Depending on the system configuration, several levels of support are available. Each package is offered with complete documentation, including a comprehensive user manual and installation guide.

SPECIFICATIONS

Required Hardware:

- Any 8086 or 80286-based system including Intel's SYSTEM 86/300, 286/300 family and iDIS systems
- Minimum of 128 KB memory
- At least two floppy disks or one hard disk
- One 8 in. or 5.25 in. double-density floppy disk drive for distribution media

Required Software:

- Intel's XENIX 86/286 Operating System

Warranty:

90 days for:
Software Updates and application support. Continuing support services available with subscription to a Software maintenance agreement.

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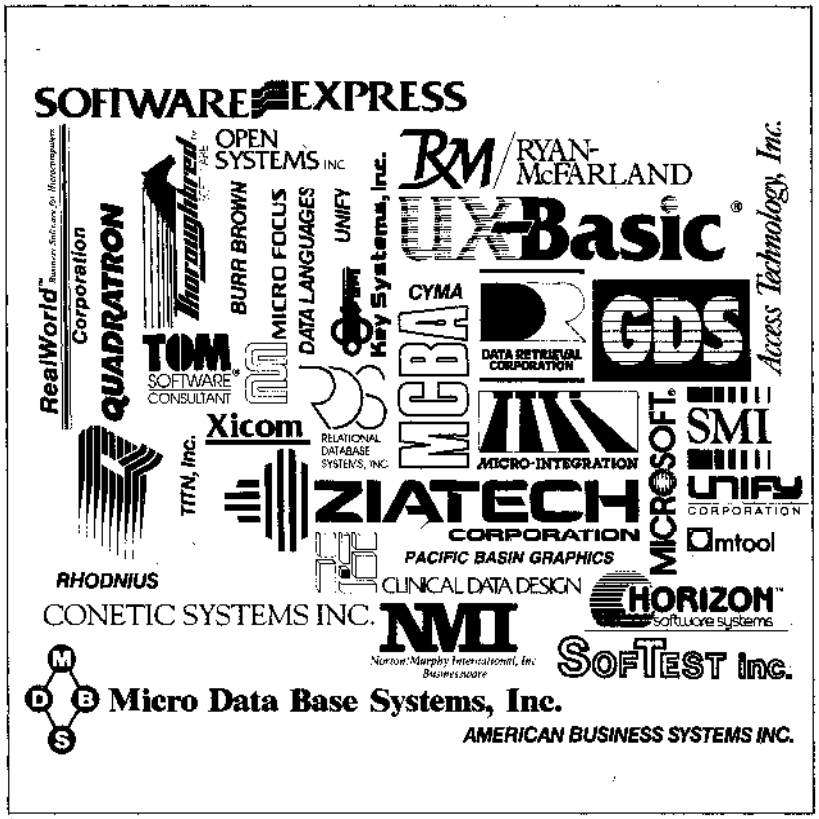
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- Tested by Intel to ensure quality and reliability on Intel Systems



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PRODUCT NAME	VENDOR	SYSTEM				AVAILBILITY
Accounting		**86/310**	**286/310**	**86/380**	**286/380**	
Thoroughbred Accounting	SMC		X			Immediate
Open Systems Accounting	Open Systems		X			Immediate
MCBA Accounting	MCBA		X			Immediate
APPGEN Accounting	Software Express		X			Immediate
BACs	ABS		X			Immediate
Real World Accounting	Real World		X			Q4/84
CYMA Accounting	CYMA		X			Q4/84
Complete Accounting	NMI		X			Q4/84
Manufacturing						
MCBA Manufacturing	MCBA		X			Q4/84
ProfitKey	Key Systems		X			Q1/85
A&M Manufacturing	TOM Software		X			Q4/84
Specialty Manufacturers	NMI		X			Q4/84
Medical						
MDX	Clinical Data		X			Immediate
Vertical						
Contractor Management	TOM Software		X			Q4/84
Distributor Management	TOM Software		X			Q4/84
Not-for-Profit	TOM Software		X			Q4/84
Project Management	TOM Software		X			Q4/84
Property Management	TOM Software		X			Q4/84
Public Accountant	TOM Software		X			Q4/84
Restaurant Management	TOM Software		X			Q4/84
Personnel Searcher	NMI		X			Q4/84
Magazine Circulation	NMI		X			Q4/84
Customer Profile	NMI		X			Q4/84
Trucking Dispatcher	NMI		X			Q4/84
Phototypesetting	NMI		X			Q4/84
Client Accounting	CYMA		X			Q4/84
Construction	CYMA		X			Q4/84
Chiropractic	CYMA		X			Q4/84
Orthodontic	CYMA		X			Q4/84
Dental	CYMA		X			Q4/84
Medical	CYMA		X			Q4/84
THIRD PARTY SOFTWARE FOR INTEL iRMX™ SYSTEMS						
Languages		**86/310**	**286/310**	**86/380**	**286/380**	
Microsoft BASIC	Intel	X	X	X	X	Immediate
Mark Williams C	Intel	X	X	X	X	Immediate
Graphics						
PBG 100	Pacific Basin Graphics	X	X			Immediate
Communications						
3270 SNA	Xicom	X	X	X	X	Immediate
X.25	T.I.T.N.	X	X	X	X	Immediate
3270 Bisync	Data Retrieval	X	X	X	X	Immediate
3780 Bisync	Micro Integration	X	X	X	X	Immediate
Database						
DxSystem	GDS	X	X			Q4/84
Manufacturing						
Ladder 86	Engineering Tools	X	X			Q4/84
Other						
IEEE-488	Ziatech	X	X			Immediate
Driver to Data I/O subsystem	Burr Brown	X	X			Q4/84

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THIRD PARTY SOFTWARE FOR INTEL XENIX* SYSTEMS						
PRODUCT NAME	VENDOR	SYSTEM				AVAILABILITY
		86/310	286/310	86/380	286/380	
Languages						
Microsoft BASIC	Intel	X	X	X	X	Immediate
Micro Focus COBOL	Intel	X	X	X	X	Immediate
Microsoft FORTAN	Intel	X	X	X	X	Immediate
RM COBOL	Ryan McFarland		X			Immediate
SMC BASIC	SMC		X			Immediate
Softbol	Omtool		X	X		Immediate
UX BASIC	UX Software		X			Immediate
S-TRAN	SMI		X			Immediate
TOM BASIC	TOM Software		X			Q4/84
Spreadsheet						
iPlan	Intel	X	X	X	X	Immediate
20/20	Access Technology		X			Q4/84
Office Automation						
iWord	Intel	X	X	X	X	Immediate
iMenu	Intel	X	X	X	X	Immediate
Q-One	Quadratron		X			Immediate
Q-Menu	Quadratron		X			Immediate
Q-Calc	Quadratron		X			Immediate
Q-Mail	Qaudratron		X			Immediate
Q-Date	Quadratron		X			Immediate
Q-Call	Quadratron		X			Immediate
Q-Note	Quadratron		X			Immediate
Q-Form	Quadratron		X			Q4/84
DATA 3500	Tom Software		X			Q4/84
LEX	Softest		X			Immediate
Application Generator						
APPGEN	Software Express		X			Immediate
C/Tools	Conetic Systems		X			Q4/84
Graphics						
iGraph	Intel	X	X	X	X	Q4/84
PBG 200	Pacific Basin Graphics		X			Q4/84
SMC Color Graphics	SMC		X			Q4/84
Communications						
PC Link	Intel	X	X	X	X	Q4/84
3270 Bisync	Intel	X	X	X	X	Q4/84
3270 SNA	Xicom		X		X	Q4/84
X.25	T.I.T.N.		X		X	Q4/84
3780 Bisync	Micro Integration		X		X	Q4/84
HASP	Intel	X	X	X	X	Immediate
Database						
iDB	Intel	X	X	X	X	Q4/84
Informix	RDS		X			Immediate
File-it!	RDS		X			Immediate
C-ISAM	RDS		X			Immediate
Unify	Unify		X			Q4/84
MDBS III	MDBS		X			Q4/84
IDOL	SMC		X			Immediate
Progress	Data Languages		X			Q4/84

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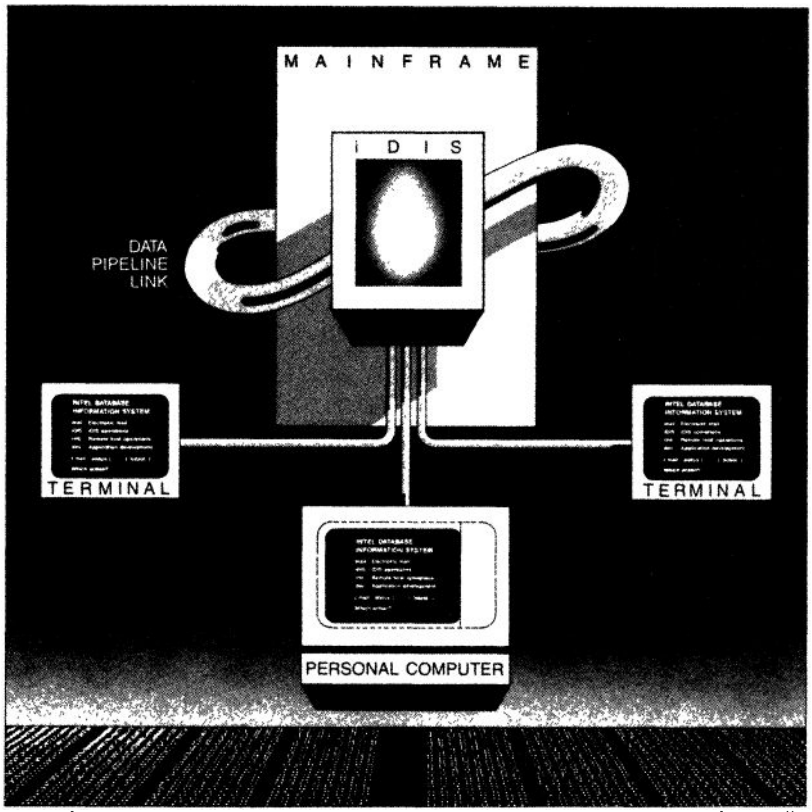
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Database Information System iDIS™ 715

- Building block for departmental-level applications
- Data Pipeline™ system to distribute databases
- Direct mainframe database extract and file transfer facilities
- Gateway for personal computer and terminal access
- Multiuser XENIX* 3.0 operating system
- Local relational database management and report writer
- Integrated software with on-line help facility
- Word processing, spreadsheet, graphics, menu development, and communication options
- C programming language
- Desk-top integrated microsystem
- Worldwide vendor service and support

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Building Vertical Applications with the iDIS™ System

The Intel Database Information System (iDIS™) is a fully-integrated multiuser hardware/software microcomputer system. It serves as a building block for end-user applications and a powerful access tool in the Data Pipeline connection between a mainframe and the end-user. Data can be maintained by central data processing departments and distributed to departmental users through a network of terminals and PCs. The system can be configured as a gateway in the micro-to-mainframe flow of data or as a stand-alone processor with shared local database capabilities. The iDIS system includes an SQL-compatible, multiuser relational DBMS for shared access to disk storage and features a full range of information processing functions for multiple concurrent users at all levels of technical skill.

The iXTRACT remote database extract facilities

The iDIS system offers two interactive, menu-driven modes of database extract. With the Remote File Transfer (RFT) iXTRACT facility, a "flat file" (sequential) data structure can be downloaded from the mainframe and converted into a local relational database. Using host computer utilities to generate the flat file, the RFT facility can download data from virtually any DBMS or file management system. The facility is bidirectional, such that flat files can be transmitted between a mainframe host and an iDIS system with its network of terminals and personal computers.

A second facility, the Direct iXTRACT facility, is a menu-driven data extract facility which directly downloads Intel SYSTEM 2000® databases (from IBM, CDC, and Sperry environments) into an iDIS database. Both RFT and direct modes allow non-technical users to access remote corporate databases and extract information while central data processing controls data security at every terminal.

*UNIX is a trademark of AT&T Bell Laboratories. Multiplan is a registered trademark of Microsoft Corporation.

Microsoft XENIX

The iDIS operating system is provided by XENIX 3.0, an enhanced industry-standard version of UNIX* XENIX is a general-purpose, multiuser, interactive operating system designed to make the computing environment simple, efficient and productive for a wide range of users. While the system developer has access to all XENIX functionality, the operating system appears to be transparent to the user who interacts with the iDIS software through its menu system.

The XENIX system supplies:

- A flexible and logical hierarchical file system, with cross-directory file linking and multiple protection and security modes
- The XENIX shell command language, with conditional, recursive, and iterative constructs (for development of user/application procedures)
- Sequential, asynchronous, and background process execution
- Sophisticated editing and text-processing facilities supporting printers and typesetters
- Device-independent input and output.

The iDB-local relational database management (DBMS)

The iDIS system offers the iDB DBMS, a full-function relational DBMS that supports an interactive query/update language similar to that of IBM's SQL. Included with iDB is a Report Writer package. This allows users to prepare custom reports quickly from information in iDB without programming knowledge. The iDB DBMS offers all the power of a mainframe DBMS at the microsystem level. Multiple iDB users can concurrently access common local databases with confidence in system integrity.

Other features include:

- A user-prompting data entry and update subsystem
- A bulk loading and unloading utility for rapid transfer of data among files and databases
- Extensive on-line help facilities
- Descriptive error and diagnostic messages
- Programmatic interface to the C language and XENIX shell.

Seamless™ software interface

The iDIS software family is integrated into a Seamless set of productivity tools. Data can be easily transferred among the various iDIS application packages, such that the iWORD processor, iPLAN (Multiplan*) spreadsheet, and iDB DBMS can interchange data and reports. All iDIS decision-support tools can be easily brought to bear on a particular data-analysis problem.

Individually, each package is accessible through a common user interface—a hierarchical menu system serving as a superstructure for the complete iDIS system. A common help facility binds all iDIS software.

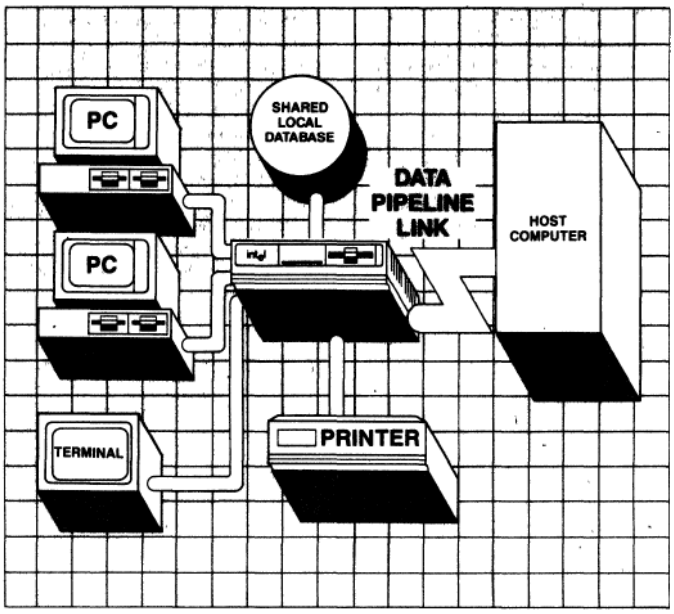
The iWORD processor

The Intel iWORD facility is a sophisticated word processing tool that supports a complete office-wide range of document preparation functions. The iWORD user can develop, edit, store, format and print a variety of presentation-quality business documents, including reports, memoranda, technical documents, specifications and manuals. All iWORD commands are in plain English and many can be executed by a single keystroke. The iWORD processor is also sufficiently powerful for the experienced user, offering access to XENIX text processing capabilities including the printer- and typesetter-drivers nroff and troff. An on-line help facility is continuously available.

Major iWORD editing and formatting features include:

- Full-screen editor with on-line display of formatted text
- Embedded commands for global formatting
- Spelling/dictionary module and mail/merge facility
- Right justification, underlining, indentation, centering, footnotes, superscripts and subscripts.

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The iPLAN (Multiplan) spreadsheet

The iDIS system supports 'what if' decision-modeling with iPLAN (Multiplan) Spreadsheet, a multi-purpose tool capable of a wide variety of business and scientific tabulations. The iPLAN user can custom-tailor a versatile two-dimensional matrix for specific analyses, including financial modeling, planning and forecasting. Like the other functions in the iDIS software environment, the iPLAN spreadsheet accepts data four ways: from the keyboard, from the iDB DBMS, from mainframe databases (via the data extract facility), and from formatted XENIX files.

Important iPLAN features include:

- Easy-to-use English commands
- Vertical and horizontal scrolling, multi-window and multi-table display
- Presentation of extra large tables
- Linking and updating multiple interrelated spreadsheets
- Automatic updating of calculations
- Alphanumeric sorting capabilities
- Extensive, on-line help facility.

*dBASE II is a trademark of Ashton-Tate.
Lotus and 1-2-3 are trademarks of Lotus Development Corporation

The personal computer (IPC) connection

To complete the Data Pipeline connection, the iDIS system offers a menu-driven file conversion and transfer facility that allows single-user PC files to be accessed in the multiuser XENIX environment. The PC user can use the iDIS system to convert database and spreadsheet files from popular PC file formats (such as dBASE II,* Lotus 1-2-3* and Multiplan formats) to iDB file formats. As a result, mainframe files can be downloaded to relational structures within iDB databases and further converted and downloaded to PC-based files for local applications analysis. The PC user can operate in three modes: bidirectional iDIS-to-PC file transfers, iDIS terminal emulation, and local PC-DOS control.

Office automation features

The XENIX operating system provides an electronic mail service in which business messages are shared and relayed with ease. XENIX also includes handy "desk calculator" functions and an electronic calendar that provides an automatic reminder (via electronic mail) of any user appointments.

Application development tools

The iDIS application development subsystem includes such software tools as the iMENU development system, C programming language, the XENIX Shell program, and the full-screen 'vi' editor (visual editor). These tools support efficient development and maintenance of program and text files by technical users.

The iDIS system offers a complete program development and execution environment for C, the versatile general-purpose language in which the operating system and all iDIS application packages are implemented. C maximizes development productivity by its structured programming methodologies and standard flow-control constructions—if, while, for, do, and switch (case). It provides pointers, the ability to perform address arithmetic, and recursive functions. Many existing C-based applications can be efficiently ported to the iDIS system.

The iMENU development facility

The iMENU development facility provides the iDIS system-level user interface, tying together the XENIX operating system, iDIS applications software, and help system. The iMENU facility retains and yet simplifies full XENIX functionality. Programmers and non-programmers alike can use the iMENU facility in creating or modifying menus, forms, and help screens for existing or custom-developed applications.

The on-line help facility

The help facility, a comprehensive on-line documentation feature, is integrated with the menu system so the user need not refer to hard copy reference manuals when using iDIS applications. Experienced users can employ the iMENU facility to extend or modify the help facility to specify help procedures for custom applications.

The iGRAPH facility

The iDIS system offers a presentation graphics package, iGRAPH, that provides high quality output to most

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standard graphics peripherals. Through iDIS integration, data can easily be moved from iPLAN and iDB to iGRAPH, from iGRAPH to iWORD for printed output, and to and from iPC. Graphic peripherals supported are Tektronix 4105, color terminal, Televideo 950 monochrome terminal with Retrographics board, Hewlett-Packard HP7475 plotter, the Epson MX80 printer, and the IBM PC with graphics board. The Intel terminal can be used to generate graphics hard copy.

Communications

The iDIS communications subsystem provides remote job entry (RJE) to mainframe hosts through its emulation of a HASP multileaving workstation or 2780/3780 protocol. TTY passthrough facilities also provide direct access to remote interactive applications, including other iDIS systems and personal computers. Support for 3270 BCS emulation is also available, and SNA support is planned.

BASE SYSTEM HARDWARE

Processor

The iDIS 715 uses the MULTIBUS®-based iSBC® 286/10 board with the 80286 processor. An Intel 80287 coprocessor is standard to provide significant performance boost for numeric operations. Instructions are 8, 16, or 32 bits in length; data are 8 or 16 bits long; numeric processing, with the 80287, is carried out in 80-bit words. Memory management and protection are also included.

One megabyte of high-performance RAM with ECC is standard. To provide faster access, Intel memory boards are connected directly to the 286/10 processor board via iLBX™ (Local Bus Exchange).

Communications support

Asynchronous communication and synchronous mainframe communications support is handled by an iSBC 188/48 Advanced Communications Processor Board. Eight connections can be configured for terminals, PCs and/or mainframe communications.

MASS STORAGE

Winchester disk drive—The iDIS 715 contains a 40 MB 5¼" Winchester technology disk drive for program and data storage. The drive has an average access time about 40 milliseconds and a transfer rate of 6.44 Mbits/sec.

Intelligent controller—The iDIS 715 includes an intelligent, 8089-based iSBC 215 Winchester controller. This high performance interface contains firmware which is executed directly on the iSBC 215 controller to offload a significant portion of disk I/O overhead from the host 80286 processor. In addition, the iSBC 215 board supports an iSBX™ 218 controller to manage the floppy disk.

Floppy disk drive—A 5¼" 320 KB floppy disk drive is included in the base system. This floppy drive has an average access time of 91 milliseconds and a transfer rate of 250 KB/sec.

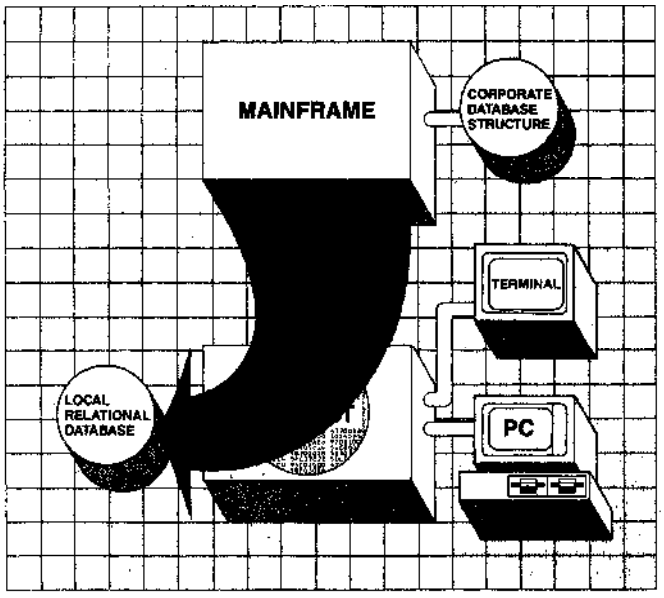
Optional peripherals

Display terminal—The standard iDIS system can connect up to 10 terminals. The terminal connected to the console port can be used for system control and administration, as well as a regular workstation. An iDIS terminal is also available, with 24-80 character lines and a 25th status line. The 96 upper and lower ASCII characters are formed in a 7x9 matrix in an 8x10 cell. The screen is non-reflective and uses green P31 phosphor.

Printer—The iDIS system supports a Centronics-compatible printer. A dot matrix character printer capable of 200 character-per-second bidirectional printing is also available. It includes a Centronics-compatible parallel interface and a 218-character buffer. The printer features a 7×9 dot matrix to form all 96 ASCII characters. Maximum standard print line length is 132 characters or 218 with condensed print. The Intel printer prints 10 characters per inch; spacing of 5, 8.25, and 16.5 characters per inch can also be accommodated.

System support

The iDIS system is fully supported by Intel's worldwide service staff, including a group of information system



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professionals with over 15 years experience in commercial database technologies. Support for iDIS applications software is included with the system price for 90 days and is optional thereafter. All iDIS software with a current software maintenance agreement is supported by the Intel Austin Systems Support Hotline.

In addition to the hotline, system support includes software updates, customer problem reporting, and a product newsletter. Intel provides comprehensive training classes on all iDIS applications, the XENIX operating system, programming languages, and hardware operation.

The iDIS hardware includes a warranty for 90 days mechanical, 45 days labor, and 90 days electrical components. After the warranty period, subscription maintenance is available from the Intel field service organization. Hardware service is also available for users on a per-call basis.

Extensive system documentation

The iDIS 715 is shipped with multiple hardware and software manuals that address all aspects of system operations. Software documentation includes manuals on the XENIX Release 3.0 operating system, iDB and Report Writer software, and each optional application package that is ordered. General overviews and detailed tutorials are an integral part of this documentation. A system installation and maintenance manual, a system overview manual, and a site preparation manual are also provided.

SYSTEM CONFIGURATION

Base Hardware System:

- 1 MB of RAM memory
- 320 KB floppy drive
- 40 MB Winchester disk
- Support for up to 10 terminals and/or PCs
- Printer support for Centronics-compatible printer
- Disk controller board
- Communications processor

Optional Hardware:

- Additional communications processor
- Terminals and dot-matrix printers

Base Software System:

- XENIX 3.0 operating system
- C programming language
- 'vi' editor
- XENIX utilities (including nroff and troff text processors)
- Electronic mail and calendar
- iDB and Report Writer
- iMENU (runtime) system
- Help facility
- Complete systems diagnostics

Optional Software:

- iWORD word processor
- iPLAN (Multiplan) spreadsheet
- iMENU menu development system
- Direct iXTRACT facility
- Remote File Transfer facility
- iPC (personal computer link)
- iGRAPH presentation graphics
- RJE communication support (2780/3780 and/or HASP protocol)
- 3270 BSC emulation

SPECIFICATIONS

Instruction cycle time

250 nanoseconds for fastest executable instructions.

Disk

Standard 40 MB Winchester disk; Second 40 MB disk is planned.

External/PC interface

Serial—8 asynchronous ports, configurable from 110 to 9600 baud. EIA Standard RS232C signal support is provided.

Parallel—one Centronics-compatible parallel I/O port for printer connections.

Regulatory Agency Specifications

Meets UL114-Safety; CSA 22.2-Safety; FCC Docket 20780-RFI/EMI. Designed to meet IEC 435-Safety; VDE 0871-RFI/EMI.

ENVIRONMENTAL OPERATING REQUIREMENTS

Altitude—Sea level to 8000 feet.

Temperature—15 degrees C to 35 degrees C.

Relative humidity—20% to 80% non-condensing over the operating temperature range. The environmental combination of humidity and temperature together cannot exceed 26 degrees C wet bulb.

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Component Software 7

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80130/80130-2
iAPX 86/30, 88/30, 186/30, 188/30
iRMX 86 OPERATING SYSTEM PROCESSORS

- **High-Performance 2-Chip Data Processors Containing Operating System Primitives**
- **Standard iAPX 86/10, 88/10 Instruction Set Plus Task Management, Interrupt Management, Message Passing, Synchronization and Memory Allocation Primitives**
- **Fully Extendable To and Compatible With iRMX® 86**
- **Supports Five Operating System Data Types: Jobs, Tasks, Segments, Mailboxes, Regions**
- **35 Operating System Primitives**
- **Built-In Operating System Timers and Interrupt Control Logic Expandable From 8 to 57 Interrupts**
- **8086/80150/80150-2/8088/80186/80188 Compatible At Up To 8 MHz Without Wait States**
- **MULTIBUS® System Compatible Interface**

The Intel iAPX 86/30 and iAPX 88/30 are two-chip microprocessors offering general-purpose CPU (8086) instructions combined with real-time operating system support. They provide a foundation for multiprogramming and multitasking applications. The iAPX 86/30 consists of an iAPX 86/10 (16-bit 8086 CPU) and an Operating System Firmware (OSF) component (80130). The 88/30 consists of the OSF and an iAPX 88/10 (8-bit 8088 CPU). (80186 or 80188 CPUs may be used in place of the 8086 or 8088.)

Both components of the 86/30 and 88/30 are implemented in N-channel, depletion-load, silicon-gate technology (HMOS), and are housed in 40-pin packages. The 86/30 and 88/30 provide all the functions of the iAPX 86/10, 88/10 processors plus 35 operating system primitives, hardware support for eight interrupts, a system timer, a delay timer and a baud rate generator.

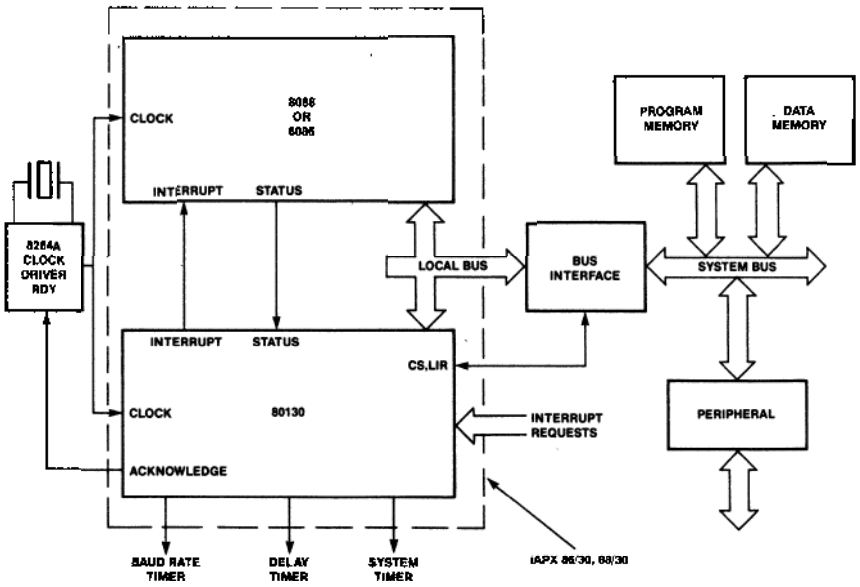


Figure 1. iAPX 86/30, 88/30 Block Diagram

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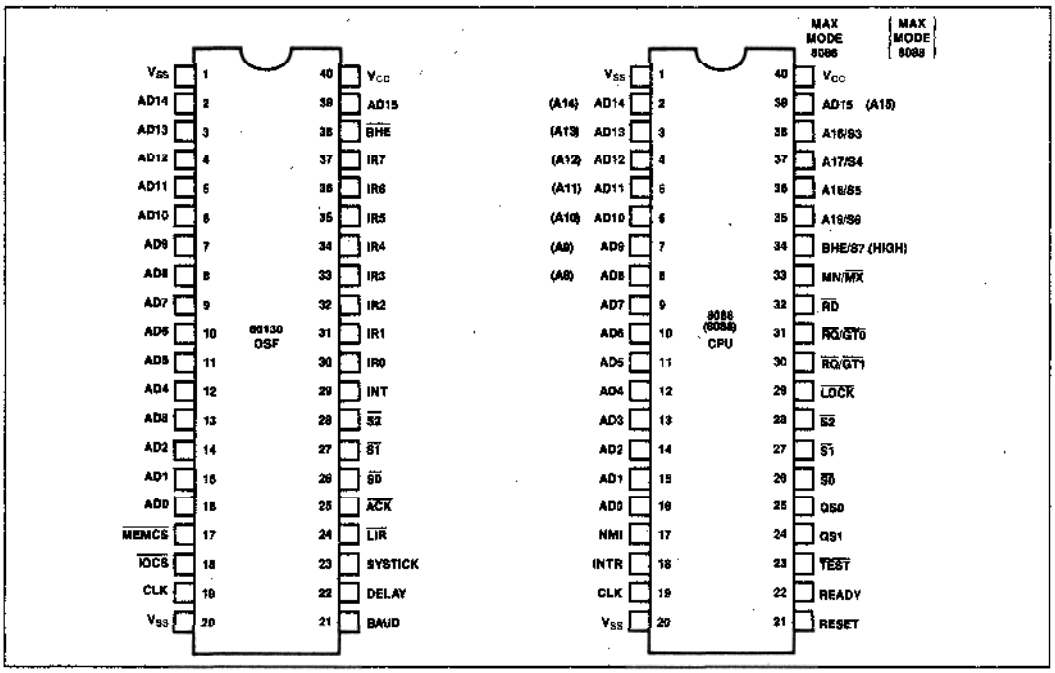


Figure 2. iAPX 86/30, 88/30 Pin Configuration

Table 1. 80130 Pin Description

Symbol	Type	Name and Function
AD_{15}–AD_0	I/O	**Address Data:** These pins constitute the time multiplexed memory address (T_1) and data (T_2, T_3, T_W, T_4) bus. These lines are active HIGH. The address presented during T_1 of a bus cycle will be latched internally and interpreted as an 80130 internal address if MEMCS or IOCS is active for the invoked primitives. The 80130 pins float whenever it is not chip selected, and drive these pins only during T_2–T_4 of a read cycle and T_1 of an INTA cycle.
$\overline{BHE}/S_7$		**Bus High Enable:** The 80130 uses the $\overline{BHE}$ signal from the processor to determine whether to respond with data on the upper or lower data pins, or both. The signal is active LOW. $\overline{BHE}$ is latched by the 80130 on the trailing edge of ALE. It controls the 80130 output data as shown. $\overline{BHE}$ A_0 0 0 Word on AD_{15}–AD_0 0 1 Upper byte on AD_{15}–AD_8 1 0 Lower byte on AD_7–AD_0 1 1 Upper byte on AD_7–AD_0
$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$	I	**Status:** For the 80130, the status pins are used as inputs only. 80130 encoding follows: $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ 0 0 0 INTA 0 0 1 IORD 0 1 0 IOWR 0 1 1 Passive 1 0 0 Instruction fetch 1 0 1 MEMRD 1 1 X Passive

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Table 1. 80130 Pin Description (Continued)

Symbol	Type	Name and Function
CLK	I	**Clock:** The system clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. The 80130 uses the system clock as an input to the SYSTICK and BAUD timers and to synchronize operation with the host CPU.
INT	O	**Interrupt:** INT is HIGH whenever a valid interrupt request is asserted. It is normally used to interrupt the CPU by connecting it to INTR.
IR_7–IR_0	I	**Interrupt Requests:** An interrupt request can be generated by raising an IR input (LOW to HIGH) and holding it HIGH until it is acknowledged (Edge-Triggered Mode), or just by a HIGH level on an IR input (Level-Triggered Mode).
$\overline{ACK}$	O	**Acknowledge:** This line is LOW whenever an 80130 resource is being accessed. It is also LOW during the first INTA cycle and second INTA cycle if the 80130 is supplying the interrupt vector information. This signal can be used as a bus ready acknowledgement and/or bus transceiver control.
$\overline{MEMCS}$	I	**Memory Chip Select:** This input must be driven LOW when a kernel primitive is being fetched by the CPU. AD_{13}–AD_0 are used to select the instruction.
$\overline{IOCS}$	I	**Input/Output Chip Select:** When this input is low, during an IORD or IOWR cycle, the 80130's kernel primitives are accessing the appropriate peripheral function as specified by the following table: $\overline{BHE}$ A_3 A_2 A_1 A_0 0 X X X X Passive X X X X 1 Passive X 0 1 X X Passive 1 0 0 X 0 Interrupt Controller 1 1 0 0 0 Systick Timer 1 1 0 1 0 Delay Counter 1 1 1 0 0 Baud Rate Timer 1 1 1 1 0 Timer Control
$\overline{LIR}$	O	**Local Bus Interrupt Request:** This signal is LOW when the interrupt request is for a non-slave input or slave input programmed as being a local slave.
V_{CC}		**Power:** V_{CC} is the +5V supply pin.
V_{SS}		**Ground:** V_{SS} is the ground pin.
SYSTICK	O	**System Clock Tick:** Timer 0 Output. Operating System Clock Reference. SYSTICK is normally wired to IR2 to implement operating system timing interrupt.
DELAY	O	**DELAY Timer:** Output of timer 1. Reserved by Intel Corporation for future use.
BAUD	O	**Baud Rate Generator:** 8254 Mode 3 compatible output. Output of 80130 Timer 2.

FUNCTIONAL DESCRIPTION

The increased performance and memory space of iAPX 86/10 and 88/10 microprocessors have proven sufficient to handle most of today's single-task or single-device control applications with performance to spare, and have led to the increased use of these microprocessors to control *multiple* tasks or devices in real-time. This trend has created a new challenge to designers—development of real-time, multitasking application systems and software. Examples of such systems include control systems that monitor and react to external events in real-time, multifunction desktop and personal computers, PABX equipment which constantly controls the telephone traffic in a multiphone office, file servers/disk subsystems controlling and coordinating multiple disks and multiple disk users, and transaction processing systems such as electronics funds transfer.

The iAPX 86/30, 88/30 Operating System Processors

The Intel iAPX 86/30, 88/30 Operating System Processors (OSPs) were developed to help solve this

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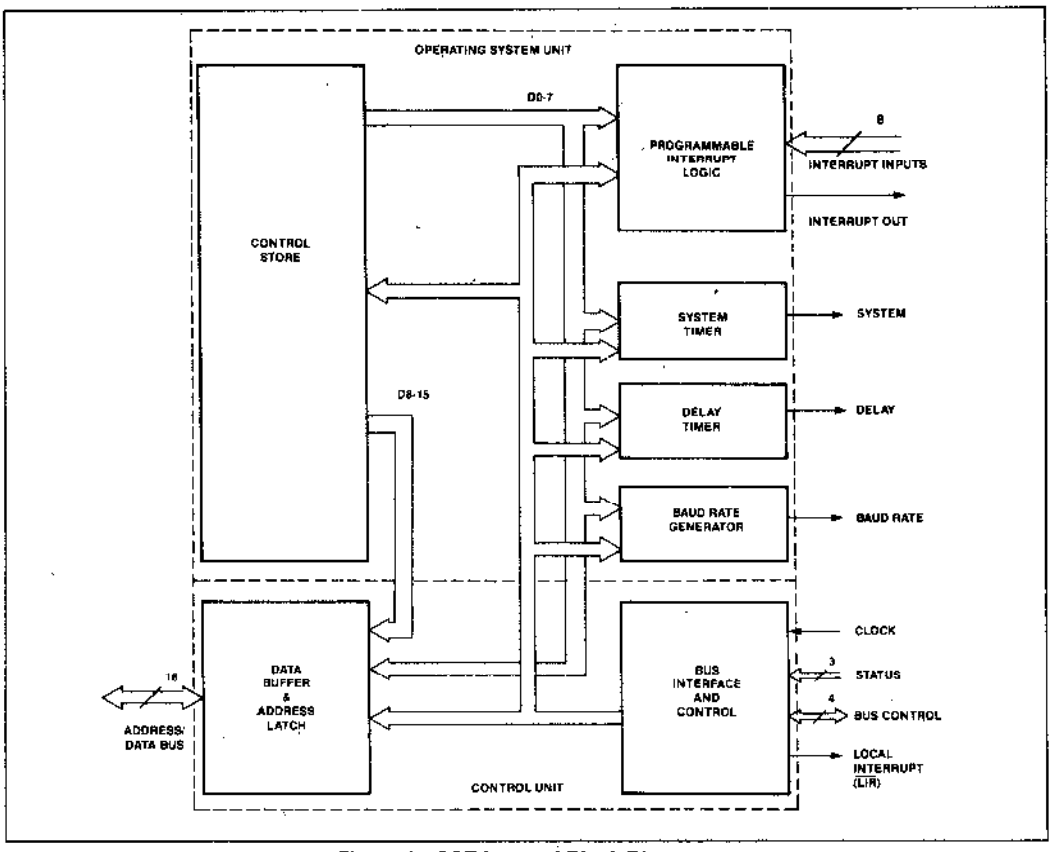


Figure 3. OSF Internal Block Diagram

problem. Their goal is to simplify the design of multitasking application systems by providing a well-defined, fully debugged set of operating system primitives implemented directly in the hardware, thereby removing the burden of designing multitasking operating system primitives from the application programmer.

Both the 86/30 and the 88/30 OSPs are two-chip sets consisting of a main processor, an 8086 or 8088 CPU, and the Intel 80130, Operating System Firmware component (OSF) (see Figure 1). The 80130 provides a set of multitasking kernel primitives, kernel control storage, and the additional support hardware, including system timers and interrupt control, required by these primitives. From the application programmer's viewpoint, the OSF extends the base iAPX 86, 88 architecture by providing 35 operating system primitive instructions, and supporting five new system data types, making the OSF a logical and easy-to-use architectural extension to iAPX 86, 88 system designs.

The OSP Approach

The OSP system data types (SDTs) and primitive instructions allocate, manage and share low-level processor resources in an efficient manner. For example, the OSP implements task context management (managing a task state image consisting of both hardware register set and software control information) for either the basic 86/10 context or the extended 86/20 (8086+8087) numerics context. The OSP manages the entire task state image both while the task is actively executing and while it is inactive. Tasks can be created, put to sleep for specified periods, suspended, executed to perform their functions, and dynamically deleted when their functions are complete.

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The Operating System Processors support event-oriented systems designs. Each event may be processed by an individual responding task or along with other closely related events in a common task. External events and interrupts are processed by the OSP interrupt handler primitives using its built-in interrupt controller subsystem as they occur in real-time. The multiple tasks and the multiple events are coordinated by the OSP integral scheduler whose preemptive, priority-based scheduling algorithm and system timers organize and monitor the processing of every task to guarantee that events are processed as they occur in order of relative importance. The 86/30 also provides primitives for intertask communication (by mailboxes) and for mutual exclusion (by regions), essential functions for multitasking applications.

Programming Language Support

Programs for the OSP can be written in ASM 86/88 or PL/M 86/88, Intel's standard system languages for iAPX 86,88 systems.

The Operating System Processor Support Package (iOSP 86) provides an interface library for application programs written in any model of PL/M-86. This library also provides 80130 configuration and initialization support as well as complete user documentation.

OSF PROGRAMMING INTERFACE

The OSF provides 35 operating system kernel primitives which implement multitasking, interrupt management, free memory management, intertask communication and synchronization. Table 4 shows each primitive, and Table 5 gives the execution performance of typical primitives.

OSP primitives are executed by a combination of CPU and OSF (80130) activity. When an OSP primitive is called by an application program task, the iAPX CPU registers and stacks are used to perform the appropriate functions and relay the results to the application programs.

OSP Primitive Calling Sequences

A standard, stack-based, calling sequence is used to invoke the OSF primitives. Before a primitive is called, its operand parameters must be pushed on the task stack. The SI register is loaded with the offset of the last parameter on the stack. The entry code for the primitive is loaded into AX. The primitive invocation call is made with a CPU software interrupt (Table 4). A representative ASM86 sequence for calling a primitive is shown in Figure 4. In PL/M the OSP programmer uses a call to invoke the primitive.

```
                SAMPLE ASSEMBLY LANGUAGE PRIMITIVE CALL

PUSH P1                         ;PUSH PARAMETER 1
PUSH P2                         ;PUSH PARAMETER 2
 .                               .  .  .
 .                               .  .  .
 .                               .  .  .
PUSH PN                         ;PUSH PARAMETER N
PUSH BP                         ;STACK CALLING CONVENTION
MOV BP,SP
LEA SI,SS:NUM_BYTES_PARAM - 2[BP]
                                ;SS:SI POINTS TO FIRST
                                ;PARAMETER ON STACK
MOV AX, ENTRY CODE              ;AX SETS PRIMITIVE ENTRY CODE
INT 194                         ;OSF INTERRUPT

                    OSP PRIMITIVE INVOKED

POP BP
RET NUM_BYTES_PARAM_            ;POP PARAMETERS
                                ;CX CONTAINS EXCEPTION CODES
                                ;DL CONTAINS PARAMETER NUMBER
                                ;   THAT CAUSED EXCEPTION (IF
                                ;   CX IS NON ZERO)
                                ;AX CONTAINS WORD RETURN VALUE
                                ;ES:BX CONTAINS POINTER
                                ;   RETURN VALUE
```

Figure 4. ASM/86 OSP Calling Convention

OSP Functional Description

Each major function of the OSP is described below. These are:

Job and Task Management
Interrupt Management
Free Memory Management
Intertask Communication
Intertask Synchronization
Environmental Control

The system data types (or SDTs) supported by the OSP are capitalized in the description. A short description of each SDT appears in Table 2.

JOB and TASK Management

Each OSP JOB is a controlled environment in which the applications program executes and the OSF system data types reside. Each individual application program is normally a separate OSP JOB, whether it has one initial task (the minimum) or multiple tasks. JOBs partition the system memory into pools. Each memory pool provides the storage areas in which the OSP will allocate TASK state images and other system data types created by the executing TASKs, and free memory for TASK working space. The OSP supports multiple executing TASKs within a JOB by managing the resources used by each, including the CPU registers, NPX registers, stacks, the system data types, and the available free memory space pool.

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When a TASK is created, the OSP allocates memory (from the free memory of its JOB environment) for the TASK's stack and data area and initializes the additional TASK attributes such as the TASK priority level and its error handler location. (As an option, the caller of CREATE TASK may assign previously defined stack and data areas to the TASK.) Task priorities are integers between 0 and 255 (the lower the priority number the higher the scheduling priority of the TASK). Generally, priorities up to 128 will be assigned to TASKs which are to process interrupts. Priorities above 128 do not cause interrupts to be disabled, these priorities (129 to 255) are appropriate for non-interrupt TASKs. If an 8087 Numerics Processor Extension is used, the error recovery interrupt level assigned to it will have a higher priority than a TASK executing on it, so that error handling is performed correctly.

EXECUTION STATUS

A TASK has an execution status or execution state. The OSP provides five execution states: RUNNING, READY, ASLEEP, SUSPENDED, and ASLEEP-SUSPENDED.

- A TASK is RUNNING if it has control of the processor.
- A TASK is READY if it is not asleep, suspended, or asleep-suspended. For a TASK to become the running (executing) TASK, it must be the highest priority TASK in the ready state.
- A TASK is ASLEEP if it is waiting for a request to be granted or a timer event to occur. A TASK may put itself into the ASLEEP state.
- A TASK is SUSPENDED if it is placed there by another TASK or if it suspends itself. A TASK may have multiple suspensions, the count of suspensions is managed by the OSP as the TASK suspension depth.
- A TASK is ASLEEP-SUSPENDED if it is both waiting and suspended.

TASK attributes, the CPU register values, and the 8087 register values (if the 8087 is configured into the application) are maintained by the OSP in the TASK state image. Each TASK will have a unique TASK state image.

SCHEDULING

The OSP schedules the processor time among the various TASKs on the basis of priority. A TASK has an execution priority relative to all other TASKs in the system, which the OSP maintains for each TASK in its TASK state image. When a TASK of higher priority than the executing TASK becomes ready to execute, the OSP switches the control of the processor to the higher priority TASK. First, the OSP saves the outgoing (lower priority) TASK's state including CPU register values in its TASK state image. Then, it restores the CPU registers from the TASK state image of the incoming (higher priority) TASK. Finally, it causes the CPU to start or resume executing the higher priority TASK.

TASK scheduling is performed by the OSP. The OSP's priority-oriented preemptive scheduler determines which TASK executes by comparing their relative priorities. The scheduler insures that the highest priority TASK with a status of READY will execute. A TASK will continue to execute until an interrupt with a higher priority occurs, or until it requests unavailable resources, for which it is willing to wait, or until it makes specific resources available to a higher priority TASK waiting for those resources.

TASKs can become READY by receiving a message, receiving control, receiving an interrupt, or by timing out. The OSP always monitors the status of all the TASKs (and interrupts) in the system. Preemptive scheduling allows the system to be responsive to the external environment while only devoting CPU resources to TASKs with work to be performed.

TIMED WAIT

The OSP timer hardware facilities support timed waits and timeouts. Thus, in many primitives, a TASK can specify the length of time it is prepared to wait for an event to occur, for the desired resources to become available or for a message to be received at a MAILBOX. The timing interval (or System Tick) can be adjusted, with a lower limit of 1 millisecond.

APPLICATION CONTROL OF TASK EXECUTION

Programs may alter TASK execution status and priority dynamically. One TASK may suspend its own execution or the execution of another TASK for a period of time, then resume its execution later. Multiple suspensions are provided. A suspended TASK may be suspended again.

The eight OSP Job and TASK management primitives are:

CREATE JOB	Partitions system resources and creates a TASK execution environment.
CREATE TASK	Creates a TASK state image. Specifies the location of the TASK code instruction stream, its execution priority, and the other TASK attributes.

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DELETE TASK	Deletes the TASK state image, removes the instruction stream from execution and deallocates stack resources. Does not delete INTERRUPT TASKS.
SUSPEND TASK	Suspends the specified TASK or, if already suspended, increments its suspension depth by one. Execute state is SUSPEND.
RESUME TASK	Decrements the TASK suspension depth by one. If the suspension depth is then zero, the primitive changes the task execution status to READY, or ASLEEP (if ASLEEP/SUSPENDED).
SLEEP	Places the requesting TASK in the ASLEEP state for a specified number of System Ticks. (The TICK interval can be configured down to 1 millisecond.)
SET PRIORITY	Alters the priority of a TASK.

Interrupt Management

The OSP supports up to 256 interrupt levels organized in an interrupt vector, and up to 57 external interrupt sources of which one is the NMI (Non-Maskable Interrupt). The OSP manages each interrupt level independently. The OSF INTERRUPT SUBSYSTEM provides two mechanisms for interrupt management: INTERRUPT HANDLERs and INTERRUPT TASKs. INTERRUPT HANDLERs disable all maskable interrupts and should be used only for servicing interrupts that require little processing time. Within an INTERRUPT HANDLER only certain OSF Interrupt Management primitives (DISABLE, ENTER INTERRUPT, EXIT INTERRUPT, GET LEVEL, SIGNAL INTERRUPT) and basic CPU instructions can be used, other OSP primitives cannot be. The INTERRUPT TASK approach permits all OSP primitives to be issued and masks only lower priority interrupts.

Work flow between an INTERRUPT HANDLER and an INTERRUPT TASK assigned to the same level is regulated with the SIGNAL INTERRUPT and WAIT INTERRUPT primitives. The flow is asynchronous. When an INTERRUPT HANDLER signals an INTERRUPT TASK, the INTERRUPT HANDLER becomes immediately available to process another interrupt. The number of interrupts (specified for the level) the INTERRUPT HANDLER can queue for the INTERRUPT TASK can be limited to the value specified in the SET INTERRUPT primitive. When the INTERRUPT TASK is finished processing, it issues a WAIT INTERRUPT primitive, and is immediately ready to process the queue of interrupts that the INTERRUPT HANDLER has built with repeated SIGNAL INTERRUPT primitives while the INTERRUPT TASK was processing. If there were no interrupts at the level, the queue is empty and the INTERRUPT TASK is SUSPENDED. See the Example (Figure 5) and Figures 6 and 7.

OSP external INTERRUPT LEVELs are directly related to internal TASK scheduling priorities. The OSP maintains a single list of priorities including both tasks and INTERRUPT LEVELs. The priority of the executing TASK automatically determines which interrupts are masked. Interrupts are managed by INTERRUPT LEVEL number. The OSP supports eight levels directly and may be extended by means of slave 8259As to a total of 57.

The nine Interrupt Management OSP primitives are:

DISABLE	Disables an external INTERRUPT LEVEL.
ENABLE	Enables an external INTERRUPT LEVEL.
ENTER INTERRUPT	Gives an Interrupt Handler its own data segment, separate from the data segment of the interrupted task.
EXIT INTERRUPT	Performs an "END of INTERRUPT" operation. Used by an INTERRUPT HANDLER which does not invoke an INTERRUPT TASK. Reenables interrupts, when the INTERRUPT HANDLER gives up control.
GET LEVEL	Returns the interrupt level number of the executing INTERRUPT HANDLER.
RESET INTERRUPT	Cancels the previous assignment made to an interrupt level by SET INTERRUPT primitive request. If an INTERRUPT TASK has been assigned, it is also deleted. The interrupt level is disabled.
SET INTERRUPT	Assigns an INTERRUPT HANDLER to an interrupt level and, optionally, an INTERRUPT TASK.

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```
/*  CODE EXAMPLE A   INTERRUPT TASK TO KEEP TRACK OF TIME-OF-DAY
DECLARE SECOND$COUNT BYTE,
    MINUTE$COUNT BYTE,
    HOURS$COUNT BYTE;
TIME$TASK:  PROCEDURE;
    DECLARE TIME$EXCEPT$CODE WORD;
    AC$CYCLE$COUNT=0;
    CALL RQ$SET$INTERRUPT(AC$INTERRUPT$LEVEL, 01H),
        @AC$HANDLER,0,@TIME$EXCEPT$CODE);
    CALL RQ$RESUME$TASK(INIT$TASK$TOKEN,@TIME$EXCEPT$CODE);
    DO HOURS$COUNT=0 TO 23;
        DO MINUTE$COUNT=0 TO 59;
            DO SECOND$COUNT=0 TO 59;
                CALL RQ$WAIT$INTERRUPT(AC$INTERRUPT$LEVEL,
                    @TIME$EXCEPT$CODE);
                IF SECOND$COUNT MOD 5=0
                    THEN CALL PROTECTED$CRT$OUT(BEL);
                END;    /*  SECOND LOOP  */
            END;    /*  MINUTE LOOP  */
        END;    /*  HOUR LOOP  */
    CALL RQ$RESET$INTERRUPT(AC$INTERRUPT$LEVEL, @TIME$EXCEPT$CODE);
    END TIME$TASK;
/*  CODE EXAMPLE B     INTERRUPT HANDLER TO SUBDIVIDE A.C. SIGNAL BY 60.  */
DECLARE AC$CYCLE$COUNT BYTE;
AC$HANDLER:  PROCEDURE INTERRUPT 59;
    DECLARE AC$EXCEPT$CODE WORD;
    AC$CYCLE$COUNT=AC$CYCLE$COUNT +1;
    IF AC$CYCLE$COUNT>=60 THEN DO;
        AC$CYCLE$COUNT=0;
        CALL RQ$SIGNAL$INTERRUPT(AC$INTERRUPT$LEVEL,@AC$EXCEPT$CODE);
        END;
    END  AC$HANDLER;
```

Figure 5. OSP Examples

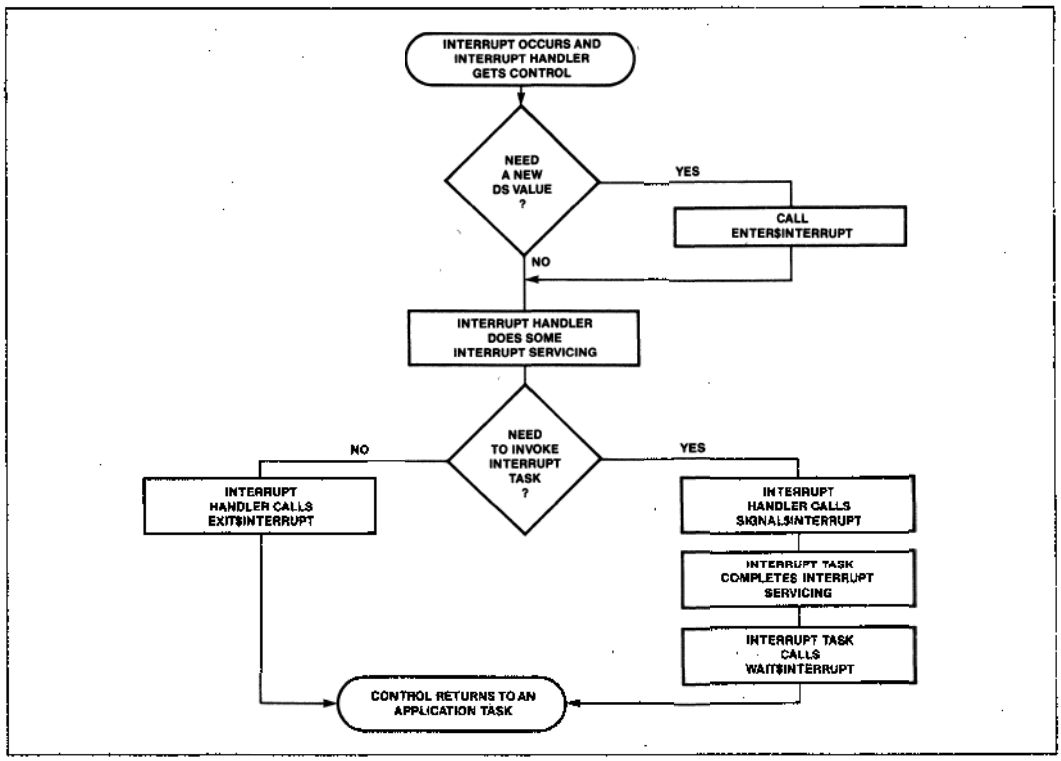


Figure 6. Interrupt Handling Flowchart

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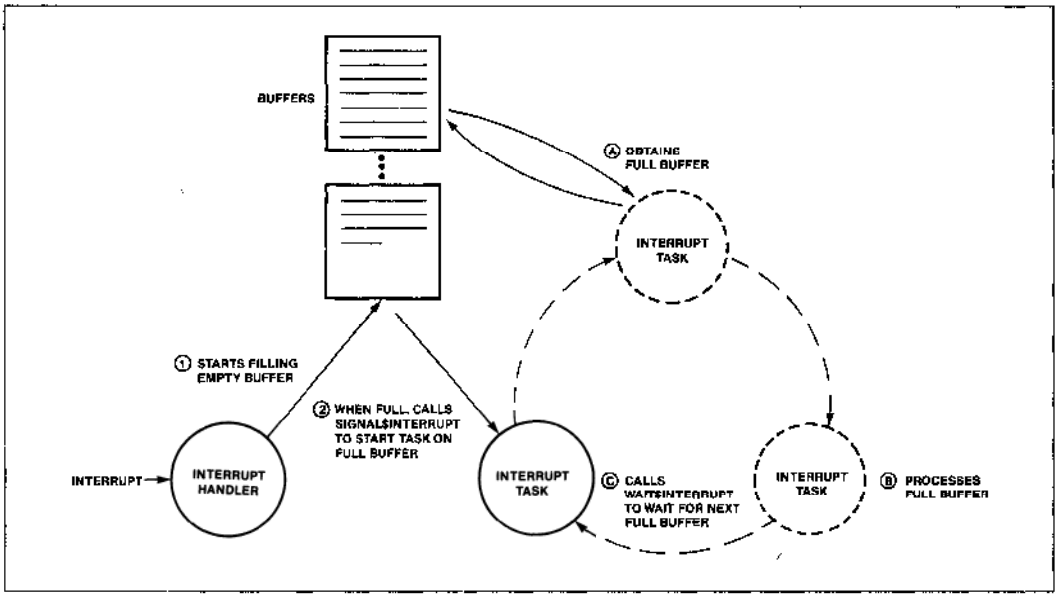


Figure 7. Multiple Buffer Example

SIGNAL INTERRUPT	Used by an INTERRUPT HANDLER to activate an Interrupt Task.
WAIT INTERRUPT	Suspends the calling Interrupt Task until the INTERRUPT HANDLER performs a SIGNAL INTERRUPT to invoke it. If a SIGNAL INTERRUPT for the task has occurred, it is processed.

FREE MEMORY MANAGEMENT

The OSP Free Memory Manager manages the memory pool which is allocated to each JOB for its execution needs. (The CREATE JOB primitive allocates the new JOB's memory pool from the memory pool of the parent JOB.) The memory pool is part of the JOB resources but is not yet allocated between the tasks of the JOB. When a TASK, MAILBOX, or REGION system data type structure is created within that JOB, the OSP implicitly allocates memory for it from the JOB's memory pool, so that a separate call to allocate memory is not required. OSP primitives that use free memory management implicitly include CREATE JOB, CREATE TASK, DELETE TASK, CREATE MAILBOX, DELETE MAILBOX, CREATE REGION, and DELETE REGION. The CREATE SEGMENT primitive explicitly allocates a memory area when one is needed by the TASK. For example, a TASK may explicitly allocate a SEGMENT for use as a memory buffer. The SEGMENT length can be any multiple of 16 bytes between 16 bytes and 64K bytes in length. The programmer may specify any number of bytes from 1 byte to 64 KB, the OSP will transparently round the value up to the appropriate segment size.

The two explicit memory allocation/deallocation primitives are:

CREATE SEGMENT	Allocates a SEGMENT of specified length (in 16-byte-long paragraphs) from the JOB Memory Pool.
DELETE SEGMENT	Deallocates the SEGMENT's memory area, and returns it to the JOB memory pool.

Intertask Communication

The OSP has built-in intertask synchronization and communication, permitting TASKs to pass and share information with each other. OSP MAILBOXes contain controlled handshaking facilities which guarantee that a *complete* message will always be sent from a sending TASK to a receiving TASK. Each MAILBOX consists of two interlocked queues, one of TASKs

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and the other of Messages. Four OSP primitives for intertask synchronization and communication are provided:

CREATE MAILBOX	Creates intertask message exchange.
DELETE MAILBOX	Deletes an intertask message exchange.
RECEIVE MESSAGE	Calling TASK receives a message from the MAILBOX.
SEND MESSAGE	Calling TASK sends a message to the MAILBOX.

The CREATE MAILBOX primitive allocates a MAILBOX for use as an information exchange between TASKs. The OSP will post information at the MAILBOX in a FIFO (First-In First-Out) manner when a SEND MESSAGE instruction is issued. Similarly, a message is retrieved by the OSP if a TASK issues a RECEIVE MESSAGE primitive. The TASK which creates the MAILBOX may make it available to other TASKs to use.

If no message is available, the TASK attempting to receive a message may choose to wait for one or continue executing.

The queue management method for the task queue (FIFO or PRIORITY) determines which TASK in the MAILBOX TASK queue will receive a message from the MAILBOX. The method is specified in the CREATE MAILBOX primitive.

Intertask Synchronization and Mutual Exclusion

Mutual exclusion is essential to multiprogramming and multiprocessing systems. The REGION system data type implements mutual exclusion. A REGION is represented by a queue of TASKS waiting to use a resource which must be accessed by only one TASK at a time. The OSP provides primitives to use REGIONs to manage mutually exclusive data and resources. Both critical code sections and shared data structures can be protected by these primitives from simultaneous use by more than one task. REGIONs support both FIFO (First-In First-Out) or Priority queueing disciplines for the TASKS seeking to enter the REGION. The REGION SDT can also be used to implement software locks.

Multiple REGIONs are allowed, and are automatically exited in the reverse order of entry. While in a REGION, a TASK cannot be suspended by itself or any other TASK, and thereby avoids deadlock.

There are five OSP primitives for mutual exclusion:

CREATE REGION	Create a REGION (lock).
SEND CONTROL	Give up the REGION.
ACCEPT CONTROL	Request the REGION, but do not wait if it is not available.
RECEIVE CONTROL	Request a REGION, wait if not immediately available.
DELETE REGION	Delete a REGION.

The OSP also provides dynamic priority adjustment for TASKs within priority REGIONs: If a higher-priority TASK issues a RECEIVE CONTROL primitive, while a (lower-priority) TASK has the use of the same REGION, the lower-priority TASK will be transparently, and temporarily, elevated to the waiting TASK's priority until it relinquishes the REGION via SEND CONTROL. At that point, since it is no longer using the critical resource, the TASK will have its normal priority restored.

OSP Control Facilities

The OSP also includes system primitives that provide both control and customization capabilities to a multitasking system. These primitives are used to control the deletion of SDTs and the recovery of free memory in a system, to allow interrogation of operating system status, and to provide uniform means of adding user SDTs and type managers.

DELETION CONTROL

Deletion of each OSP system data type is explicitly controlled by the applications programmer by setting a deletion attribute for that structure. For example, if a SEGMENT is to be kept in memory until DMA activity is completed, its deletion attribute should be disabled. Each TASK, MAILBOX, REGION, and SEGMENT SDT is created with its deletion attribute enabled (i.e., they may be deleted). Two OSP primitives control the deletion attribute: ENABLE DELETION and DISABLE DELETION.

ENVIRONMENTAL CONTROL

The OSP provides inquiry and control operations which help the user interrogate the application environment and implement flexible exception handling. These features aid in run-time decision making and in application error processing and recovery. There are five OSP environmental control primitives.

OS EXTENSIONS

The OSP architecture is defined to allow new user-defined System Data Types and the primitives to manipulate them to be added to OSP capabilities

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provided by the built-in System Data Types. The type managers created for the user-defined SDTs are called user OS extensions and are installed in the system by the SET OS EXTENSION primitive. Once installed, the functions of the type manager may be invoked with user primitives conforming to the OSP interface. For well-structured extended architectures, each OS extension should support a separate user-defined system data type, and every OS extension should provide the same calling sequence and program interface for the user as is provided for a built-in SDT. The type manager for the extension would be written to suit the needs of the application. OSP interrupt vector entries (224–255) are reserved for user OS extensions and are not used by the OSP. After assigning an interrupt number to the extension, the extension user may then call it with the standard OSP call sequence (Figure 4), and the unique software interrupt number assigned to the extension.

ENABLE DELETION	Allows a specific SEGMENT, TASK, MAILBOX, or REGION SDT to be deleted.
DISABLE DELETION	Prevents a specific SEGMENT, TASK, MAILBOX, or REGION SDT from being deleted.
GET TYPE	Given a token for an instance of a system data type, returns the type code.
GET TASK TOKENS	Returns to the caller information about the current task environment.
GET EXCEPTION HANDLER	Returns information about the calling TASK's current information handler: its address, and when it is used.
SET EXCEPTION HANDLER	Provides the address and usage of an exception handler for a TASK.
SET OS EXTENSION	Modifies one of the interrupt vector entries reserved for OS extensions (224–255) to point to a user OS extension procedure.
SIGNAL EXCEPTION	For use in OS extension error processing.

EXCEPTION HANDLING

The OSP supports exception handlers. These are similar to CPU exception handlers such as OVERFLOW and ILLEGAL OPERATION. Their purpose is to allow the OSP primitives to report parameter errors in primitive calls, and errors in primitive usage. Exception handling procedures are flexible and can be individually programmed by the application. In general, an exception handler if called will perform one or more of the following functions:

—Log the Error.
—Delete/Suspend the Task that caused the exception.
—Ignore the error, presumably because it is not serious.

An EXCEPTION HANDLER is written as a procedure. If PLM/86 is used, the "compact," "medium" or "large" model of computation should be specified for the compilation of the program. The mode in which the EXCEPTION HANDLER operates may be specified in the SET EXCEPTION HANDLER primitive. The return information from a primitive call is shown in Figure 4. CX is used to return standard system error conditions. Table 7 shows a list of these conditions, using the *default* EXCEPTION HANDLER of the OSP.

HARDWARE DESCRIPTION

The 80130 operates in a closely coupled mode with the iAPX 86/10 or 88/10 CPU. The 80130 resides on the CPU local multiplexed bus (Figure 8). The main processor is always configured for maximum mode operation. The 80130 automatically selects between its 88/30 and 86/30 operating modes.

The 80130 used in the 86/30 configuration, as shown in Figure 8 (or a similar 88/30 configuration), operates at both 5 and 8 MHz without requiring processor wait states. Wait state memories are fully supported, however. The 80130 may be configured with both an 8087 NPX and an 8089 IOP, and provides full context control over the 8087.

The 80130 (shown in Figure 3) is internally divided into a control unit (CU) and operating system unit (OSU). The OSU contains facilities for OSP kernel support including the system timers for scheduling and timing waits, and the interrupt controller for interrupt management support.

iAPX 86/30, iAPX 88/30 System Configuration

The 80130 is both I/O and memory mapped to the local CPU bus. The CPU's status S0/-S2/ is decoded along with IOCS/ (with BHE and AD_3–AD_0) or MEMCS/ (with AD_{13}–AD_0). The pins are internally latched. See Table 1 for the decoding of these lines.

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Memory Mapping

Address lines A_{19}–A_{14} can be used to form MEMCS/ since the 80130's memory-mapped portion is aligned along a 16K-byte boundry. The 80130 can reside on any 16K-byte boundry excluding the highest (FC000H-FFFFFH) and lowest (00000H-003FFH). The 80130 control store code is position-independent except as limited above, in order to make it compatible with many decoding logic designs. AD_{13}–AD_0 are decoded by the 80130's kernel control store.

I/O Mapping

The I/O-mapped portion of the 80130 must be aligned along a 16-byte boundry. Address lines A_{15}–A_4 should be used to form IOCS/.

System Performance

The approximate performance of representitive OSP primitives is given in Table 5. These times are shown for a typical iAPX 86/30 implementation with an 8 MHz clock. These execution times are very comparable to the execution times of similar functions in minicomputers (where available) and are an order of magnitude faster than previous generation microprocessors.

Initialization

Both application system initialization and OSP-specific initialization/configuration are required to use the OSP. Configuration is based on a "database" provided by the user to the iOSP 86 support package. The OSP-specific initialization and configuration information area is assigned to a user memory address adjacent to the 80130's memory-mapped location. (See Application Note 130 for further details.) The configuration data defines whether 8087 support is configured in the system, specifies if slave 8259A interrupt controllers are used in addition to the 80130, and sets the operating system time base (Tick Interval). Also located in the configuration area are the exception handler control parameters, the address location of the (separate) application system configuration area and the OSP extensions in use. The OSP application system configuration area may be located anywhere in the user memory and must include the starting address of the application instruction code to be executed, plus the locations of the RAM memory blocks to be managed by the OSP free memory manager. Complete application system support and the required 80130 configuration support are provided by the iAPX 86/30 and iAPX 88/30 OPERATING SYSTEM PROCESSOR SUPPORT PACKAGE (iOSP 86).

RAM Requirements

The OSP manages its own interrupt vector, which is assigned to low RAM memory. Working RAM storage is required as stack space and data area. The memory space must be allocated in user RAM.

OSP interrupt vector memory locations 0H–3FFH must be RAM based. The OSP requires 2 bytes of allocated RAM. The processor working storage is dynamically allocated from free memory. Approximately 300 bytes of stack should be allocated for each OSP task.

TYPICAL SYSTEM CONFIGURATION

Figure 8 shows the processing cluster of a "typical" iAPX 86/30 or iAPX 88/30 OSP system. Not shown are subsystems likely to vary with the application. The configuration includes an 8086 (or 8088) operating in maximum mode, an 8284A clock generator and an 8288 system controller. Note that the 80130 is located on the CPU side of any latches or transceivers. See Intel Application Note 130 for further details on configuration.

OSP Timers

The OSP Timers are connected to the lower half of the data bus and are addressed at even addresses. The timers are read as two successive bytes, always LSB followed by MSB. The MSB is always latched on a read operation and remains latched until read. Timers are not gatable.

Baud Rate Generator

The baud rate generator is 8254 compatible (square wave mode 3). Its output, BAUD, is initially high and remains high until the Count Register is loaded. The first falling edge of the clock after the Count Register is loaded causes the transfer of the internal counter to the Count Register. The output stays high for N/2 [(N+1)/2 if N is odd] and then goes low for N/2 [(N−1)/2 if N is odd]. On the falling edge of the clock which signifies the final count for the output in low state, the output returns to high state and the Count Register is transferred to the internal counter. The whole process is then repeated. Baud Rates are shown in Table 6.

The baud rate generator is located at 0CH (12), relative to the 16-byte boundary in the I/O space in which the 80130 component is located ("OSF" in the following example), the timer control word is located at

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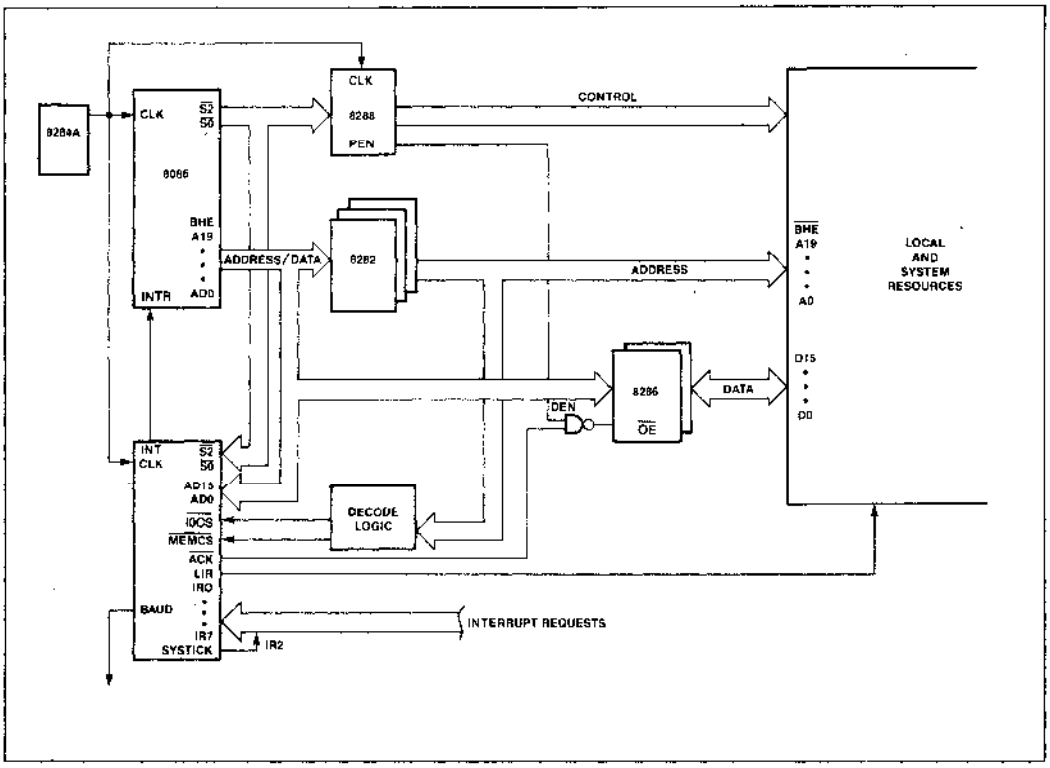


Figure 8. Typical OSP Configuration

relative address, 0EH(14). Timers are addressed with IOCS=0. Timers 0 and 1 are assigned to the use by the OSP, and should not be altered by the user.

For most baud-rate generator applications, the command byte

0B6H Read/Write Baud-Rate Delay Value

will be used. A typical sequence to set a baud rate of 9600 using a count value of 52 follows (see Table 6):

```
MOV  AX,0B6H     ;Prepare to Write Delay to
                  Timer 3.
OUT  OSF+14,AX   ;Control Word.
MOV  AX, 52
OUT  OSF+12,AL   ;LSB written first
XCHG AL,AH
OUT  OSF+12,AL   ;MSB written after.
```

The 80130 timers are subset compatible with 8254 timers.

Interrupt Controller

The Programmable Interrupt Controller (PIC), is also an integral unit of the 80130. Its eight input pins handle eight vectored priority interrupts. One of these pins must be used for the SYSTICK time function in timing waits, using an external connection as shown. During the 80130 initialization and configuration sequence, each 80130 interrupt pin is individually programmed as either level or edge sensitive. External slave 8259A interrupt controllers can be used to expand the total number of OSP external interrupts to 57.

In addition to standard PIC funtions, 80130 PIC unit has an $\overline{LIR}$ output signal, which when low indicates an interrupt acknowledge cycle. $\overline{LIR}$=0 is provided to control the 8289 Bus Arbiter SYSB/$\overline{RESB}$ pin. This will avoid the need of requesting the system bus to acknowledge local bus non-slave interrupts. The user defines the interrupt system as part of the configuration.

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INTERRUPT SEQUENCE

The OSP interrupt sequence is as follows:

1. One or more of the interrupts is set by a low-to-high transition on edge-sensitive IR inputs or by a high input on level-sensitive IR inputs.
2. The 80130 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an interrupt acknowledge cycle which is encoded in $\overline{S_2}$-$\overline{S_0}$.
4. Upon receiving the first interrupt acknowledge from the CPU, the highest-priority interrupt is set by the 80130 and the corresponding edge detect latch is reset. The 80130 does not drive the address/data bus during this bus cycle but does acknowledge the cycle by making $\overline{ACK}$=0 and sending the $\overline{LIR}$ value for the IR input being acknowledged.
5. The CPU will then initiate a second interrupt acknowledge cycle. During this cycle, the 80130 will supply the cascade address of the interrupting input at T_1 on the bus and also release an 8-bit pointer onto the bus if appropriate, where it is read by the CPU. If the 80130 does supply the pointer, then $\overline{ACK}$ will be low for the cycle. This cycle also has the value $\overline{LIR}$ for the IR input being acknowledged.
6. This completes the interrupt cycle. The ISR bit remains set until an appropriate EXIT INTERRUPT primitive (EOI command) is called at the end of the Interrupt Handler.

OSP APPLICATION EXAMPLE

Figure 5 shows an application of the OSP primitives to keep track of time of day in a simplified example. The system design uses a 60 Hz A.C. signal as a time base. The power supply provides a TTL-compatible signal which drives one of 80130 edge-triggered interrupt request pins once each A.C. cycle. The Interrupt Handler responds to the interrupts, keeping track of one second's A.C. cycles. The Interrupt Task counts the seconds and after a day deletes itself. In typical systems it might perform a data logging operation once each day. The Interrupt Handler and Interrupt Task are written as separate modular programs.

The Interrupt Handler will actually service interrupt 59 when it occurs. It simply counts each interrupt, and at a count of 60 performs a SIGNAL INTERRUPT to notify the Interrupt Task that a second has elapsed. The Interrupt Handler (ACS HANDLER) was assigned to this level by the SET INTERRUPT primitive. After doing this, the Interrupt Task performed the Primitive RESUME TASK to resume the application task (INITS TASKS TOKEN).

The main body of the task is the counting loop. The Interrupt Task is signaled by the SIGNAL INTERRUPT primitive in the Interrupt Handler (at interrupt level ACS INTERRUPTS LEVEL). When the task is signalled by the Interrupt Handler it will execute the loop exactly one time, increasing the time count variables. Then it will execute the WAIT INTERRUPT primitive, and wait until awakened by the Interrupt Handler. Normally, the task will now wait some period of time for the next signal. However, since the interface between the Handler and the Task is asynchronous, the handler may have already queued the interrupt for servicing, the writer of the task does not have to worry about this possibility.

At the end of the day, the task will exit the loop and execute RESET INTERRUPT, which disables the interrupt level, and deletes the Interrupt task. The OSP now reclaims the memory used by the Task and schedules another task. If an exception occurs, the coded value for the exception is available in TIMES EXCEPTS CODE after the execution of the primitive.

A typical PL/M-86 calling sequence is illustrated by the call to RESET INTERRUPT shown in Figure 5.

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Table 2. OSP System Data Type Summary

Job	Jobs are the means of organizing the program environment and resources. An application consists of one or more jobs. Each iAPX 86/30 system data type is contained in some job. Jobs are independent of each other, but they may share access to resources. Each job has one or more tasks, one of which is an initial task. Jobs are given pools of memory, and they may create subordinate offspring jobs, which may borrow memory from their parents.
Task	Tasks are the means by which computations are accomplished. A task is an instruction stream with its own execution stack and private data. Each task is part of a job and is restricted to the resources provided by its job. Tasks may perform general interrupt handling as well as other computational functions. Each task has a set of attributes, which is maintained for it by the iAPX 86/30, which characterize its status. These attributes are: its containing job its register context its priority (0–255) its execution state (asleep, suspended, ready, running, asleep/suspended). its suspension depth its user-selected exception handler its optional 8087 extended task state
Segment	Segments are the units of memory allocation. A segment is a physically contiguous sequence of 16-byte, 8086 paragraph-length, units. Segments are created dynamically from the free memory space of a Job as one of its Tasks requests memory for its use. A segment is deleted when it is no longer needed. The iAPX 86/30 maintains and manages free memory in an orderly fashion, it obtains memory space from the pool assigned to the containing job of the requesting task and returns the space to the job memory pool (or the parent job pool) when it is no longer needed. It does not allocate memory to create a segment if sufficient free memory is not available to it, in that case it returns an error exception code.
Mailbox	Mailboxes are the means of intertask communication. Mailboxes are used by tasks to send and receive message segments. The iAPX 86/30 creates and manages two queues for each mailbox. One of these queues contains message segments sent to the mailbox but not yet received by any task. The other mailbox queue consists of tasks that are waiting to receive messages. The iAPX 86/30 operation assures that waiting tasks receive messages as soon as messages are available. Thus at any moment one or possibly both of two mailbox queues will be empty.
Region	Regions are the means of serialization and mutual exclusion. Regions are familiar as "critical code regions." The iAPX 86/30 region data type consists of a queue of tasks. Each task waits to execute in mutually exclusive code or to access a shared data region, for example to update a file record.
Tokens	The OSP interface makes use of a 16-bit TOKEN data type to identify individual OSF data structures. Each of these (each instance) has its own unique TOKEN. When a primitive is called, it is passed the TOKENs of the data structures on which it will operate.

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Table 3. System Data Type Codes and Attributes

S.D.T.	Code	Attributes
Jobs	1	Tasks Memory Pool S.D.T. Directory
Tasks	2	Priority Stack Code State Exception Handler
Mailboxes	3	Queue of S.D.T.s (generally segments) Queue of Tasks waiting for S.D.T.s
Region	5	Queue of Tasks waiting for mutually exclusive code or data
Segments	6	Buffer Length

Table 4. OSP Primitives

Class	OSP Primitive	Interrupt Number	Entry Code in AX	Parameters On Caller's Stack
JOB	CREATE JOB	184	0100H	*See 80130 User Manual
TASK	CREATE TASK	184	0200H	Priority, IP Ptr, Data Segment, Stack Seg, Stack Size Task Information, ExceptPtr
	DELETE TASK	184	0201H	TASK, ExceptPtr
	SUSPEND TASK	184	0202H	TASK, ExceptPtr
	RESUME TASK	184	0203H	TASK, ExceptPtr
	SET PRIORITY	184	0209H	TASK, Priority, ExceptPtr
	SLEEP	184	0204H	Time Limit,ExceptPtr
INTERRUPT	DISABLE	190	0705H	Level, ExceptPtr
	ENABLE	184	0704H	Level #, ExceptPtr
	ENTER INTERRUPT	184	0703H	Level #, ExceptPtr
	EXIT INTERRUPT	186	NONE	Level #,ExceptPtr
	GET LEVEL	188	0702H	Level #, ExceptPtr
	RESET INTERRUPT	184	0706H	Level #, ExceptPtr
	SET INTERRUPT	184	0701H	Level, Interrupt Task Flag Interrupt Handler Ptr, Interrupt Handler DataSeg ExceptPtr
	SIGNAL INTERRUPT	185	NONE	Level, ExceptPtr
	WAIT INTERRUPT	187	NONE	Level, ExceptPtr
SEGMENT	CREATE SEGMENT	184	0600H	Size, ExceptPtr
	DELETE SEGMENT	184	0603H	SEGMENT, ExceptPtr

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Table 4. OSP Primitives (Continued)

Class	OSP Primitive	Interrupt Number	Entry Code in AX	Parameters On Caller's Stack
MAILBOX	CREATE MAILBOX	184	0300H	Mailbox flags, ExcptPtr
	DELETE MAILBOX	184	0301H	MAILBOX, ExcptPtr
	RECEIVE MESSAGE	184	0303H	MAILBOX, Time Limit ResponsePtr, ExcptPtr
	SEND MESSAGE	184	0302H	MAILBOX,Message Response, ExcptPtr
REGION	ACCEPT CONTROL	184	0504H	REGION, ExcptPtr
	CREATE REGION	184	0500H	Region Flags, ExcptPtr
	DELETE REGION	184	0501H	REGION, ExcptPtr
	RECEIVE CONTROL	184	0503H	REGION, ExcptPtr
	SEND CONTROL	184	0502H	ExcptPtr
ENVIRONMENTAL	DISABLE DELETION	184	0001H	TOKEN,ExcptPtr
	ENABLE DELETION	184	0002H	TOKEN,ExcptPtr
	GET EXCEPTION HANDLER	184	0800H	Ptr,ExcptPtr
	GET TYPE	184	0000H	TOKEN,ExcptPtr
	GET TASK TOKENS	184	0206H	Request, ExcptPtr
	SET EXCEPTION HANDLER	184	0801H	Ptr, ExcptPtr
	SET OS EXTENSION	184	0700H	Code,InstPtr, ExcptPtr
	SIGNAL EXCEPTION	184	0802H	Exception Code, Parameter Number, StackPtr,0,0,ExcptPtr

NOTES:
All parameters are pushed onto the OSP stack. Each parameter is one word. See Figure 3 for Call Sequence.

Explanation of the Symbols

JOB	OSP JOB SDT Token
TASK	OSP TASK SDT Token
REGION	OSP REGION SDT Token
MAILBOX	OSP MAILBOX SDT Token
SEGMENT	OSP SEGMENT SDT Token
TOKEN	Any SDT Token
Level	Interrupt Level Number
ExcptPtr	Pointer to Exception Code
Message	Message Token
Ptr	Pointer to Code,Stack etc. Address
Seg	Value Loaded into appropriate Segment Register
—	Value Parameter.

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Table 5. OSP Primitive Performance Examples

Datatype Class	Primitive Execution Speed* (microseconds)	
JOB	CREATE JOB	2950
TASK	CREATE TASK (no preemption)	1360
SEGMENT	CREATE SEGMENT	700
MAILBOX	SEND MESSAGE (with task switch)	475
	SEND MESSAGE (no task switch)	265
	RECEIVE MESSAGE (task waiting)	540
	RECEIVE MESSAGE (message waiting)	260
REGION	SEND CONTROL	170
	RECEIVE CONTROL	205

*8 MHz iAPX 86/30 OSP Configuation.

Table 6. Baud Rate Count Values (16X)

Baud Rate	8 MHz Count Value	5 MHz Count Value
300	1667	1042
600	833	521
1200	417	260
2400	208	130
4800	104	65
9600	52	33

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Table 7a. Mnemonic Codes for Unavoidable Exceptions

E$OK	Exception Code Value = 0 the operation was successful
E$TIME	Exception Code Value = 1 the specified time limit expired before completion of the operations was possible
E$MEM	Exception Code Value = 2 insufficient nucleus memory is available to satisfy the request
E$BUSY	Exception Code Value = 3 specified region is currently busy
E$LIMIT	Exception Code Value = 4 attempted violation of a job, semaphore, or system limit
E$CONTEXT	Exception Code Value = 5 the primitive was called in an illegal context (e.g., call to enable for an already enabled interrupt)
E$EXIST	Exception Code Value = 6 a token argument does not currently refer to any object; note that the object could have been deleted at any time by its owner
E$STATE	Exception Code Value = 7 attempted illegal state transition by a task
ENOTCONFIGURED	Exception Code Value = 8 the primitive called is not configured in this system
E$INTERRUPT$SATURATION	Exception Code Value = 9 The interrupt task on the requested level has reached its user specified saturation point for interrupt service requests. No further interrupts will be allowed on the level until the interrupt task executes a WAIT$INTERRUPT. (This error is only returned, in line, to interrupt handlers.)
E$INTERRUPT$OVERFLOW	Exception Code Value = 10 The interrupt task on the requested level previously reached its saturation point and caused an E$INTERRUPT$SATURATION condition. It subsequently executed an ENABLE allowing further interrupts to come in and has received another SIGNAL$INTERRUPT call, bringing it over its specified saturation point for interrupt service requests. (This error is only returned, in line, to interrupt handlers).

Table 7b. Mnemonic Codes for Avoidable Exceptions

E$ZERO$DIVIDE	Exception Code Value = 8000H divide by zero interrupt occurred
E$OVERFLOW	Exception Code Value = 8001H overflow interrupt occurred
E$TYPE	Exception Code Value = 8002H a token argument referred to an object tha was not of required type
E$BOUNDS	Exception Code Value = 8003H an offset argument is out of segment bounds
E$PARAM	Exception Code Value = 8004H a (non-token,non-offset) argument has an illegal value
EBADCALL	Exception Code Value = 8005H an entry code for which there is no corresponding primitive was passed
E$ARRAY$BOUNDS = 8006H	Hardware or Language has detected an array overflow
ENDPERROR	Exception Code Value = 8007H an 8087 (Numeric data Processor) error has been detected; (the 8087 status information is contained in a parameter to the exception handler)

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bins ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin With
Respect to Ground ..... −1.0V to +7V
Power Dissipation ..... 1.0 Watts

**NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.*

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + .5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400μA
I_{CC}	Power Supply Current		200	mA	T_A = 25 C
I_{LI}	Input Leakage Current		10	μA	$0 < V_{IN} < V_{CC}$
I_{LR}	IR Input Load Current		10 −300	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0$
I_{LO}	Output Leakage Current		10	μA	$.45 < V_{IN} < V_{CC}$
V_{CLI}	Clock Input Low		0.6	V	
V_{CHI}	Clock Input High	3.9		V	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		15	pF	
I_{CLI}	Clock Input Leakage Current		10 150 10	μA μA μA	$V_{IN} = V_{CC}$ V_{IN} = 2.5V V_{IN} = 0V

A.C. CHARACTERISTICS (T_A = 0-70°C, V_{CC} = 4.5-5.5 Volt, V_{SS} = Ground)

		80130		80130-2			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Test Conditions
T_{CLCL}	CLK Cycle Period	200	–	125	–	ns	
T_{CLCH}	CLK Low Time	90	–	55	–	ns	
T_{CHCL}	CLK High Time	69	2000	44	2000	ns	
T_{SVCH}	Status Active Setup Time	80	–	65	–	ns	
T_{CHSV}	Status Inactive Hold Time	10	–	10	–	ns	
T_{SHCL}	Status Inactive Setup Time	55	–	55	–	ns	
T_{CLSH}	Status Active Hold Time	10	–	10	–	ns	
T_{ASCH}	Address Valid Setup Time	8	–	8	–	ns	
T_{CLAH}	Address Hold Time	10	–	10	–	ns	
T_{CSCL}	Chip Select Setup Time	20	–	20	–	ns	
T_{CHCS}	Chip Select Hold Time	0	–	0	–	ns	
T_{DSCL}	Write Data Setup Time	80	–	60	–	ns	
T_{CHDH}	Write Data Hold Time	10	–	10	–	ns	
T_{JLJH}	IR Low Time	100	–	100	–	ns	
T_{CLDV}	Read Data Valid Delay	–	140	–	105	ns	C_L = 200 pF
T_{CLDH}	Read Data Hold Time	10	–	10	–	ns	
T_{CLDX}	Read Data to Floating	10	100	10	100	ns	
T_{CLCA}	Cascade Address Delay Time	–	85	–	65	ns	

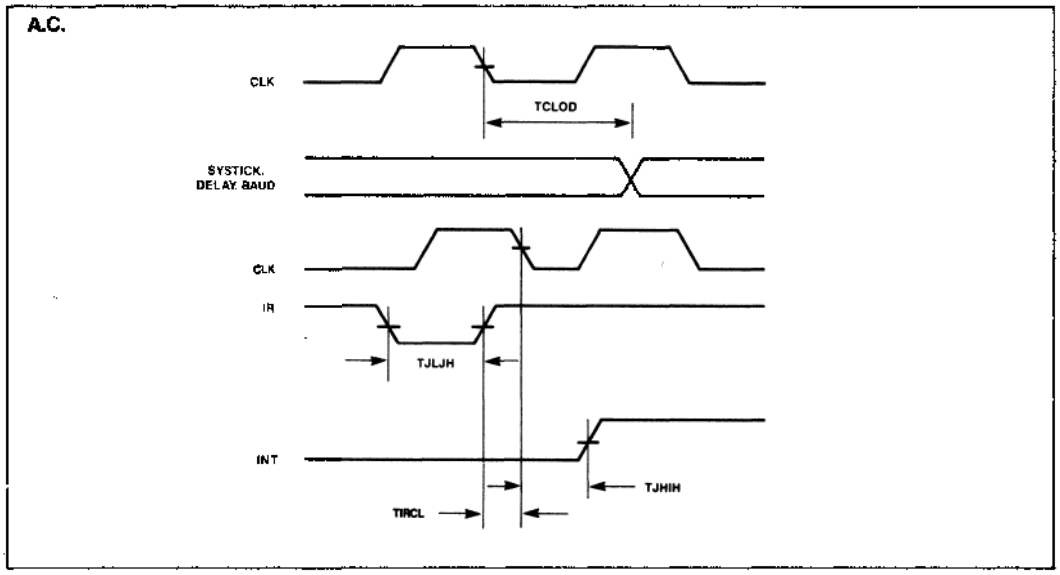
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A.C. CHARACTERISTICS (Continued)

		80130		80130-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Notes**
T_{CLCF}	Cascade Addresse Hold Time	10	–	10	–	ns	
T_{IAVE}	INTA Status t Acknowledge	–	80	–	80	ns	
T_{CHEH}	Acknowledge Hold Time	0	–	0	–	ns	
T_{CSAK}	Chip Select to ACK	–	110	–	110	ns	
T_{SACK}	Status to ACK	–	140	–	140	ns	
T_{AACK}	Address to ACK	–	90	–	90	ns	
T_{CLOD}	Timer Output Delay Time	–	200	–	200	ns	C_L = 100 pF
T_{CLOD1}	Timer1 Output Delay Time	–	200	–	200	ns	C_L = 100 pF
T_{JHIH}	INT Output Delay	–	200	–	200	ns	
T_{IRCL}	IR Input Set Up	20		20		ns	

WAVEFORMS

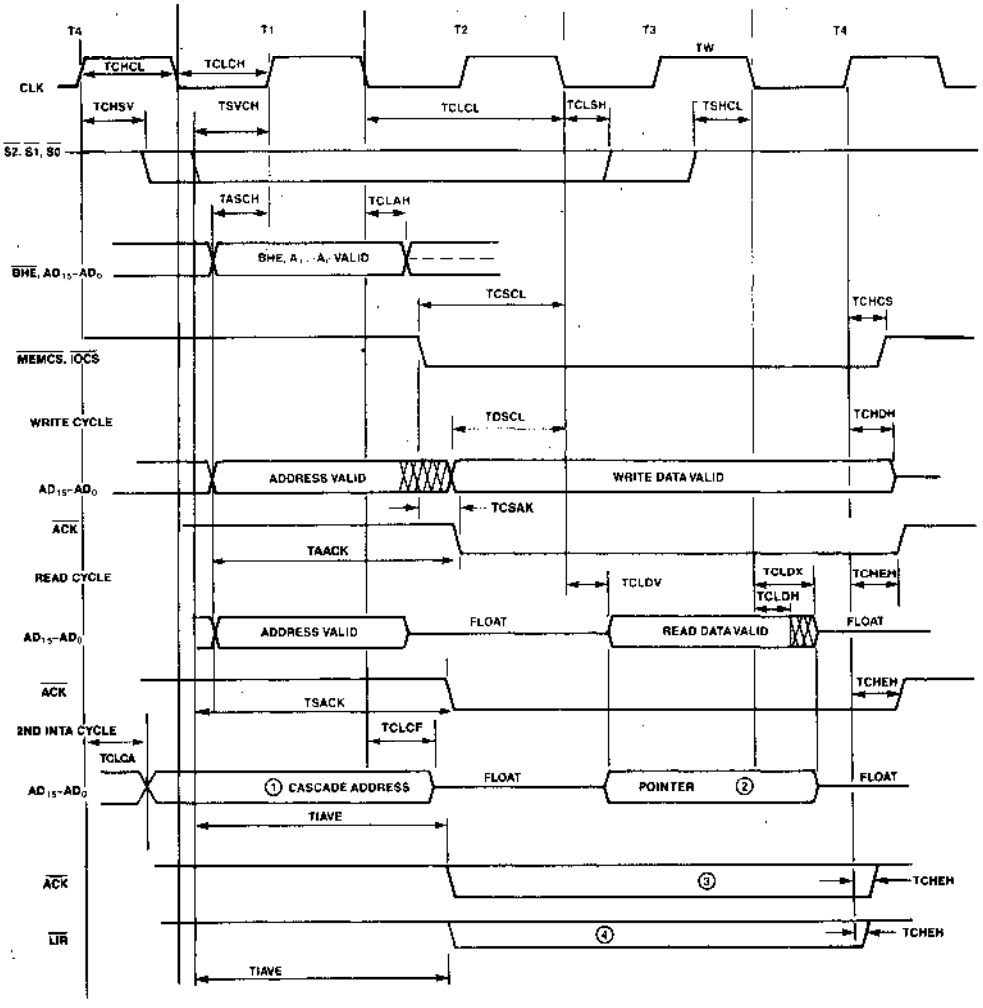
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WAVEFORMS

A.C.



NOTES
1. CASCADE ADDRESS PRESENTED ON AD8, AD9 AND AD10 CORRESPONDING TO CAS0, CAS1 AND CAS2 RESPECTIVELY. AD11–AD15 LINES ARE ACTIVE AND HAVE UNKNOWN VALUES. AD0–AD7 ARE TRISTATE.
2. POINTER VALUE IS ACTIVE ONLY IF POINTER IS GENERATED FROM THE 80150 AND NOT FROM EXTERNAL SLAVE UNIT.
3. ACTIVE LOW ONLY WHEN POINTER DATA IS BEING SUPPLIED BY THE 80150.
4. LOW ONLY FOR LOCAL INTERRUPT.

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ADVANCE INFORMATION

80150/80150-2
iAPX 86/50, 88/50, 186/50, 188/50
CP/M-86 OPERATING SYSTEM PROCESSORS

- **High-Performance Two-Chip Data Processors Containing the Complete CP/M-86 Operating System**
- **Standard On-Chip BIOS (Basic Input/Output System) Contains Drivers for 8272A, 8274, 8255A, 8251A, 7220 Bubble Memory Controller**
- **BIOS Extensible with User-Supplied Peripheral Drivers**
- **User Intervention Points Allow Addition of New System Commands**
- **Memory Disk Makes Possible Diskless CP/M-86 Systems**
- **No License or Serialization Required**
- **Built-in Operating System Timers and Interrupt Controller**
- **8086/80150/80150-2/8088/80186/80188 Compatible At Up To 8 MHz Without Wait States**

The Intel iAPX 86/50, 88/50, 186/50, and 188/50 are two-chip microprocessors offering general-purpose CPU instructions combined with the CP/M-86 operating system. Respectively, they consist of the 8- and 16-bit software compatible 8086, 8088, 80186, and 80188 CPU plus the 80150 CP/M-86 operating system extension.

CP/M-86 is a single-user operating system designed for computers based on the Intel iAPX 86, 88, 186, and 188 microprocessors. The system allows full utilization of the one megabyte of memory available for application programs. The 80150 stores CP/M-86 in its 16K bytes of on-chip memory. The 80150 will run third-party applications software written to run under standard Digital Research CP/M-86.

The 80150 is implemented in N-Channel, depletion-load, silicon-gate technology (HMOS), and is housed in a 40-pin package. Included on the 80150 are the CP/M-86 operating system, Version 1.1, plus hardware support for eight interrupts, a system timer, a delay timer, and a baud rate generator.

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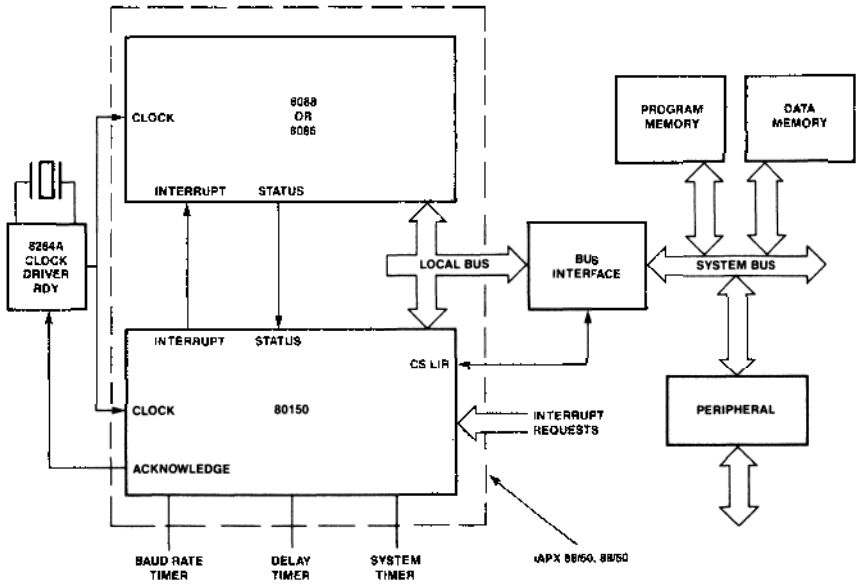


Figure 1. iAPX 86/50, 88/50 Block Diagram

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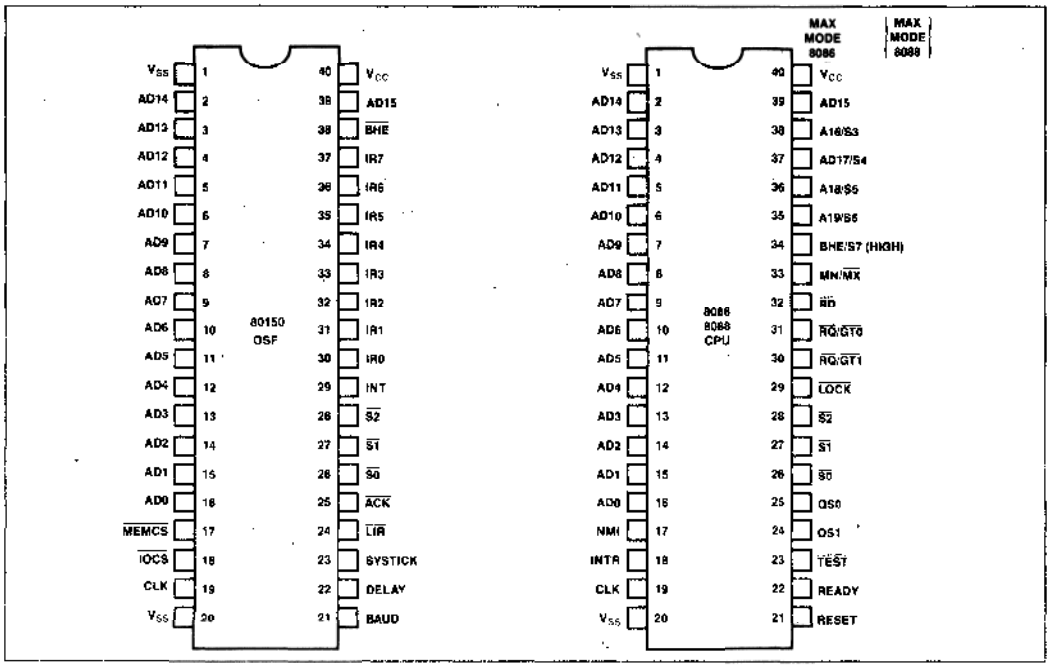


Figure 2. iAPX 86/50, 88/50 Pin Configuration

Table 1. 80150 Pin Description

Symbol	Type	Name and Function
AD_{15}-AD_0	I/O	**Address Data:** These pins constitute the time multiplexed memory address (T_1) and data (T_2, T_3, T_W, T_4) bus. These lines are active HIGH. The address presented during T_1 of a bus cycle will be latched internally and interpreted as an 80150 internal address if MEMCS or IOCS is active for the invoked primitives. The 80150 pins float whenever it is not chip selected, and drive these pins only during $T_2 - T_4$ of a read cycle and T_1 of an INTA cycle.
$\overline{BHE}/S_7$	I	**Bus High Enable:** The 80150 uses the BHE signal from the processor to determine whether to respond with data on the upper or lower data pins, or both. The signal is active LOW. BHE is latched by the 80150 on the trailing edge of ALE. It controls the 80150 output data as shown. $\overline{BHE}$ A_0 0 0 Word on AD_{15}-AD_0 0 1 Upper byte on $AD_{15} - AD_8$ 1 0 Lower byte on AD_7-AD_0 1 1 Upper byte on AD_7-AD_0
$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$	I	**Status:** For the 80150, the status pins are used as inputs only. 80150 encoding follows: $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ 0 0 0 INTA 0 0 1 IORD 0 1 0 IOWR 0 1 1 Passive 1 0 0 Instruction fetch 1 0 1 MEMRD 1 1 X Passive

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Table 1. 80150 Pin Description (Continued)

Symbol	Type	Name and Function
CLK	I	**Clock:** The system clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. The 80150 uses the system clock as an input to the SYSTICK and BAUD timers and to synchronize operation with the host CPU
INT	O	**Interrupt:** INT is HIGH whenever a valid interrupt request is asserted. It is normally used to interrupt the CPU by connecting it to INTR
IR_7-IR_0	I	**Interrupt Requests:** An interrupt request can be generated by raising an IR input (LOW to HIGH) and holding it HIGH until it is acknowledged (Edge-Triggered Mode), or just by a HIGH level on an IR input (Level-Triggered Mode).
$\overline{ACK}$	O	**Acknowledge:** This line is LOW whenever an 80150 resource is being accessed. It is also LOW during the first INTA cycle and second INTA cycle if the 80150 is supplying the interrupt vector information. This signal can be used as a bus ready acknowledgement and/or bus transceiver control.
$\overline{MEMCS}$	I	**Memory Chip Select:** This input must be driven LOW when a kernel primitive is being fetched by the CPU. AD_{13}-AD_0 are used to select the instruction
$\overline{IOCS}$	I	**Input/Output Chip Select:** When this input is low, during an IORD or IOWR cycle, the 80150's kernel primitives are accessing the appropriate peripheral function as specified by the following table: $\overline{BHE}$ A_3 A_2 A_1 A_0 0 X X X X Passive X X X X 1 Passive X 0 1 X X Passive 1 0 0 X 0 Interrupt Controller 1 1 0 0 0 Systick Timer 1 1 0 1 0 Delay Counter 1 1 1 0 0 Baud Rate Timer 1 1 1 1 0 Timer Control
$\overline{LIR}$	O	**Local Bus Interrupt Request:** This signal is LOW when the interrupt request is for a non-slave input or slave input programmed as being a local slave
V_{CC}		**Power:** V_{CC} is the +5V supply pin
V_{SS}		**Ground:** V_{SS} is the ground pin
SYSTICK	O	**System Clock Tick:** Timer 0 Output
DELAY	O	**DELAY Timer:** Output of timer 1
BAUD	O	**Baud Rate Generator:** 8254 Mode 3 compatible output. Output of 80150 Timer 2.

The 80150 breaks new ground in operating system software-on-silicon components. It is unique because it is the first time that an industry-standard personal/small business computer operating system is being put in silicon. The 80150 contains Digital Research's CP/M-86 operating system, which is designed for Intel's line of software- and interface-compatible iAPX 86, 88, 186, and 188 microprocessors. Since the entire CP/M-86 operating system is contained on the chip, it is now possible to design a diskless computer that runs proven and commonly available applications software. The 80150 is a true operating system extension to the host microprocessor, since it also integrates key operating system-related peripheral functions onto the chip.

MODULAR DESIGN

Based on a proven, modular design, the system includes the:

- CCP: Console Command Processor

  The CCP is the human interface to the operating system and performs decoding and

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execution of user commands.

- BDOS: Basic Disk Operating System

  The BDOS is the logical, invariant portion of the operating system; it supports a named file system with a maximum of 16 logical drives, containing up to 8 megabytes each for a potential of 128 megabytes of on-line storage.

- BIOS: Basic Input/Output System

  The physical, variant portion of the operating system, the BIOS contains the system-dependent input/output device handlers.

CP/M* COMPATIBILITY

CP/M-86 files are completely compatible with CP/M for 8080- and 8085-based microcomputer systems. This simplifies the conversion of software developed under CP/M to take full advantage of iAPX 86, 88, 186, 188-based systems.

The user will notice no significant difference between CP/M and CP/M-86. Commands such as DIR, TYPE, REN, and ERA respond the same way in both systems.

CP/M-86 uses the iAPX 86, 88, 186, 188 registers corresponding to 8080 registers for system call and return parameters to further simplify software transport. The 80150 allows application code and data segments to overlap, making the mixture of code and data that often appears in CP/M applications acceptable to the iAPX 86, 88, 186, 188.

Unique Capabilities of CP/M-86 in Silicon

1. CP/M-86 on-a-chip reduces software development required by the system designer. It can change the implementation of the operating system into the simple inclusion of the 80150 on the CPU board.

   As described later, the designer can either simply incorporate the Intel chip without the need for writing even a single line of additional code, or he can add additional device drivers by writing only the small amount of additional code required.

2. The 80150 is the most cost-effective way to implement CP/M-86 in a microcomputer. The integration of CP/M-86 with the 16K bytes of system memory it requires, the two boot ROMS required in a diskette-based CP/M-86, and the on-chip peripherals (interrupt controller and timers) lead to savings in software, parts cost, board space, and interconnect wiring.

3. The reliability of the microcomputer is increased significantly. Since CP/M-86 is now always in the system as a standard hardware operating system, a properly functioning system diskette is not required. CP/M-86 in hardware can no longer be overwritten accidentally by a runaway program. System reliability is enhanced by the decreased dependence on floppy disks and fewer chips and interconnections required by the highly integrated 80150.

4. The microcomputer system boots up CP/M-86 on power-on, rather than requiring the user to go through a complicated boot sequence, thus lowering the user expertise required.

5. Diskless CP/M-based systems are now easy to design. Since CP/M is already in the microcomputer hardware, there is no need for a disk drive in the system if it is not desired. Without a disk drive, a system is more portable, simpler to use, less costly, and more reliable.

6. The administrative costs associated with distributing CP/M-86 are eliminated. Since CP/M-86 is now resident on the 80150 in the microcomputer system, there is no end-user licensing required nor is there any serialization requirement for the 80150 (because no CP/M diskette is used).

7. End-users will value having their CP/M operating system resident in their computer rather than on a diskette. They will no longer have to back up the operating system or have a diskette working properly to bring the system up in CP/M, increasing their confidence in the integrity, reliability, and usability of the system.

80150 FUNCTIONAL DESCRIPTION

The 80150 is a processor extension that is fully compatible with the 8086, 8088, 80186, and 80188 microprocessors. When the 80150 is combined with the microprocessor, the two-chip set is called an Operating System Processor and is denoted as the iAPX 86/50, 88/50, 186/50, or 188/50. The basic system configuration is shown in Figure 1. The 80150 connects directly to the multiplexed address/data bus and runs up to 8 MHz without wait states.

A. Hardware. Figure 3 is a functional diagram of the 80150 itself. CP/M-86 is stored in the 16K-bytes of control store. The timers are compatible with the standard 8254 timer. The interrupt controller, with its eight programmable interrupt inputs and one interrupt output, is compatible with the 8259A Programmable Interrupt Controller. External slave 8259A inter-

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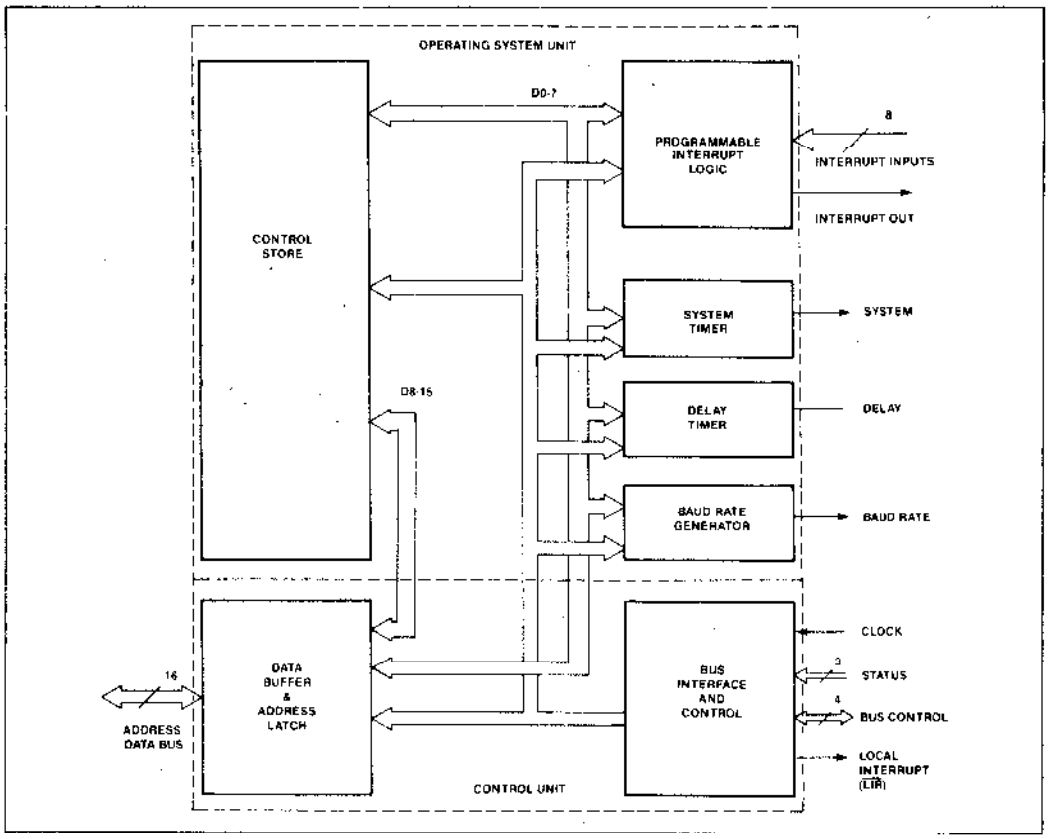


Figure 3. 80150 Internal Block Diagram

rupt controllers can be cascaded with the 80150 to expand the total number of interrupts to 57.

B. Software. Digital Research's version 1.1 of CP/M-86 forms the basis of the 80150. CP/M consists of three major parts: the Console Command Processor (CCP), the Basic Disk Operating System (BDOS), and the Basic Input/Output System (BIOS). Details on CP/M-86 are provided in Digital Research's *CP/M-86 Operating System User's Guide* and *CP/M-86 Operating System System Guide*.

CCP - Console Command Processor

The CCP provides all of the capabilities provided by Digital Research's CCP. Built-in commands have been expanded to include capabilities normally included as transient utilities on the Digital Research CP/M-86 diskette. Commands are provided to format diskettes, transfer files between devices (based on Digital Research's Peripheral Interchange Program PIP), and alter and display I/O device and file status (based on Digital Research's STAT).

Through User Intervention Points, the standard CP/M-86 CCP is enhanced to allow the user to add new built-in commands to further customize a CP/M-86 system.

BDOS - Basic Disk Operating System

Once the CCP has parsed a command, it sends it to the BDOS, which performs system services such as managing disk directories and files. Some of the standard BDOS functions provide:

Console Status
Console Input and Output
List Output
Select Drive
Set Track and Sector

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Read/Write Sector
Load Program

The BDOS in the 80150 provides the same functions as the standard Digital Research CP/M-86 BDOS.

BIOS - Basic Input/Output System

The BIOS contains the system-dependent I/O drivers. The 80150 BIOS offers two fundamental configuration options:

1. **A predefined configuration** which supports minimum cost CP/M-86 microcomputer systems and which requires no operating system development by the system designer.
2. **An OEM-configurable mode**, where the designer can choose among several drivers offered on the 80150 or substitute or add any additional device drivers of his choice.

These two options negate the potential software-on-silicon pitfall of inflexibility in system design. The OEM can customize the end system as desired.

The **predefined configuration** offers a choice among several peripheral chip drivers included on the 80150. Drivers for the following chips are included in the 80150 BIOS:

8251A	Universal Synchronous/ Asynchronous Receiver/Transmitter (USART)
8274	Multi-Protocol Serial Controller (MPSC)
8255A	Programmable Parallel Interface (PPI)
8272A	Floppy Disk Controller
7220	Bubble Memory Controller

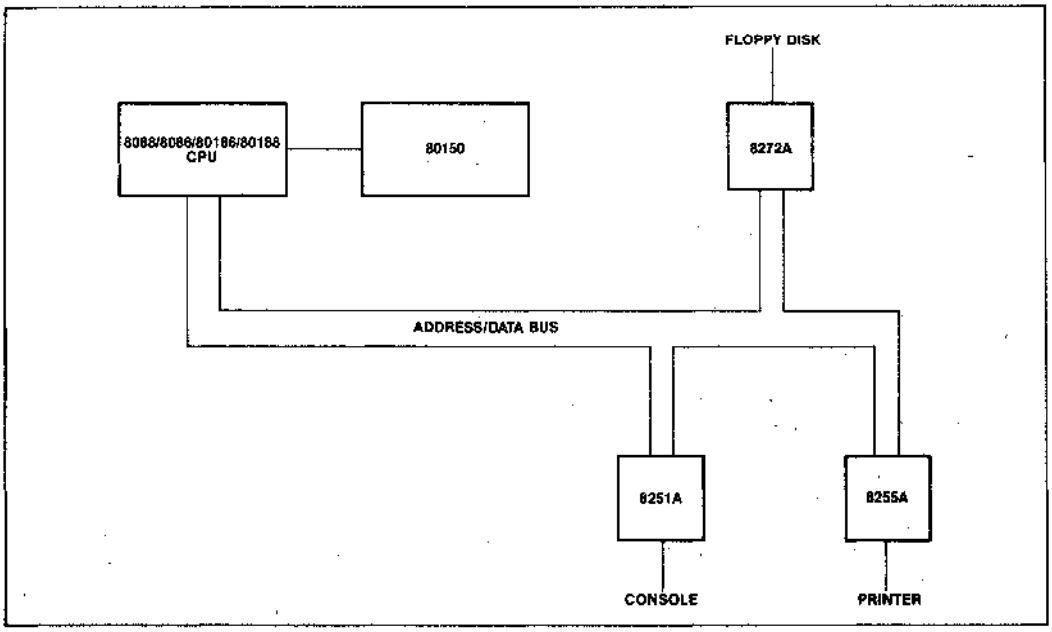


Figure 4. Predefined Configuration

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Even in the predefined configuration, the system designer (or end user, if the system designer desires) may select parameters such as the baud rates for the console and printer, and the floppy disk size (standard 8" or 5¼" mini-floppy) and format (FM single density or MFM double density, single-sided or double-sided).

Drivers for the 80150 on-chip timers and interrupt controller are also included in the BIOS.

The 80150 takes advantage of the 80186 and 80188 on-chip peripherals in an iAPX 186/50 or 188/50 system. For example, the integrated DMA controller is used. Also fully utilized are the integrated memory chip selects and I/O chip selects.

Since all microcomputer configurations cannot be anticipated, the **OEM-configurable mode** allows the system designer to use any set of peripheral chips desired. This configuration is shown in Figure 5.

By simply changing the jump addresses in a configuration table, the designer can also gain the flexibility of adding custom BIOS drivers for other peripheral chips, such as bubble memories or more complex CRT controllers. These drivers would be stored in memory external to the 80150 itself. By providing the configurability option, the 80150 is applicable to a far broader range of designs that it would be with an inflexible BIOS.

MEMORY ORGANIZATION

When using the **predefined configuration** of the 80150 BIOS, the 80150 must be placed in the top 16K of the address space of the microprocessor (starting at location FC000H) so that the 80150 gains control when the microprocessor is reset. Upon receipt of control, the 80150 writes a **configuration block** into the bottom of the microprocessor's address space, which must be in RAM. The 80150 uses the area after the interrupt vectors for system configuration information and scratch-pad storage.

When using the **OEM-configurable** mode of the 80150 BIOS, the 80150 is placed on any 16K boun-

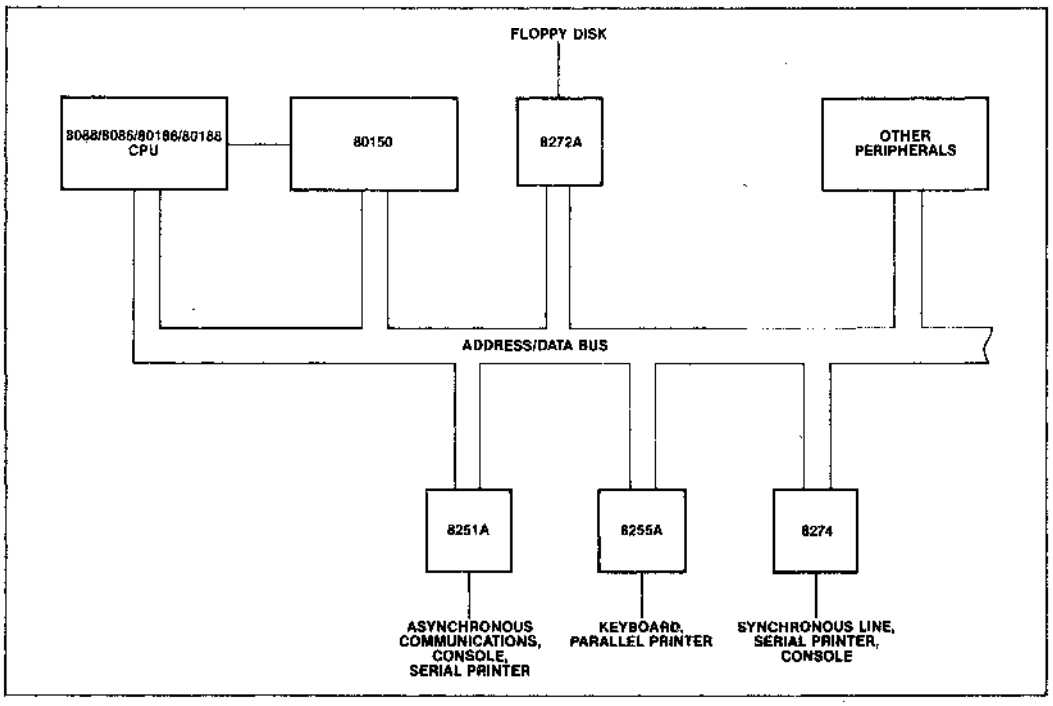


Figure 5. OEM Configurable System

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dary of memory **except** the highest (FC000H) or lowest (00000H). The user writes interface code (in the form of a simple boot ROM) to incorporate and link additional features and changes into the standard 80150 environment. The configuration block may be located as desired in the address space, and its size may vary widely depending on the application.

Memory Disk and Bubble Memories

A unique capability offered by the 80150 is the Memory Disk. The Memory Disk consists of a block of RAM whose size can be selected by the designer. The Memory Disk is treated by the BDOS as any standard floppy disk, and is one of the 16 disks that CP/M can address. Thus files can be opened and closed, programs stored, and statistics gathered on the amount of Memory Disk space left.

The 80150 also contains software drivers for 7220 bubble memory controller. Use of a bubble memory board as a substitute for one floppy disk drive is directly supported.

The Memory Disk opens the possibility of a portable low-cost diskless microcomputer or network station. Applications software can be provided in a number of ways:

a. telephone lines via a modem.
b. ROM-based software.
c. a network.
d. bubble memory based software.
e. low-cost cassettes.

TYPICAL SYSTEM CONFIGURATION

Figure 6 shows the processing cluster of a "typical" iAPX 86/50 or iAPX 88/50 OSP system. Not shown are subsystems likely to vary with the application. The configuration includes an 8086 (or 8088) operating in maximum mode, an 8284A clock generator and an 8288 system controller. Note that the 80150 is located on the CPU side of any latches or transceivers.

Timers

The Timers are connected to the lower half of the data bus and are addressed at even addresses. The timers are read as two successive bytes,

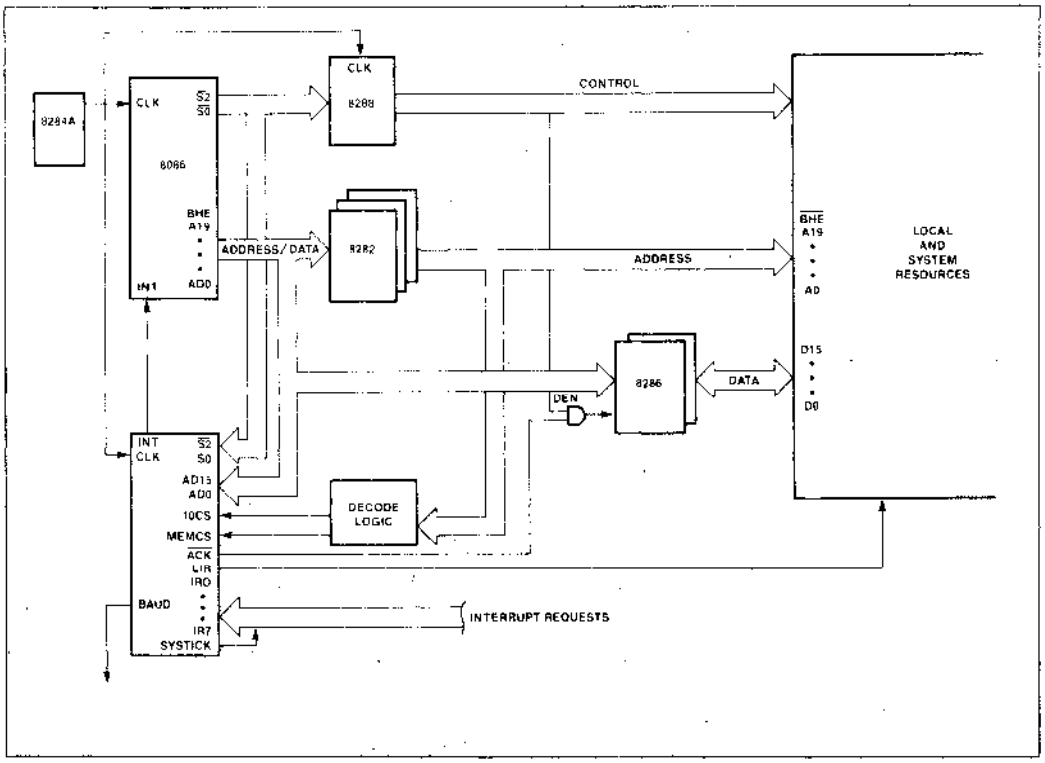


Figure 6. Typical OSP Configuration

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always LSB followed by MSB. The MSB is always latched on a read operation and remains latched until read. Timers are not gatable. An external 8254 Programmable Interval Timer may be added to the system.

Baud Rate Generator

The baud rate generator operates like an 8254 (square wave mode 3). Its output, BAUD, is initially high and remains high until the Count Register is loaded. The first falling edge of the clock after the Count Register is loaded causes the transfer of the internal counter to the Count Register. The output stays high for N/2 [(N + 1)/2 if N is odd] and then goes low for N/2 [(N – 1)/2 if N is odd]. On the falling edge of the clock which signifies the final count for the output in low state, the output returns to high state and the Count Register is transferred to the internal counter. The baud rates can vary from 300 to 9600 baud.

The baud rate generator is located at 0CH (12), relative to the 16-byte boundary in the I/O space in which the 80150 component is located. The timer control word is located at relative address, 0EH(14). Timers are addressed with IOCS = 0. Timers 0 and 1 are assigned to use by the OSP, and should not be altered by the user.

The 80150 timers are subset compatible with 8254 timers.

Interrupt Controller

The Programmable Interrupt Controller (PIC), is also an integral unit of the 80150. Its eight input pins handle eight vectored priority interrupts. One of these pins must be used for the SYSTICK time function in timing waits, using an external connection as shown. During the 80150 initialization and configuration sequence, each 80150 interrupt pin is individually programmed as either level or edge sensitive. External slave 8259A interrupt controllers can be used to expand the total number of interrupts to 57.

In addition to standard PIC functions, the 80150 PIC unit has an $\overline{LIR}$ output signal, which when low indicates an interrupt acknowledge cycle. $\overline{LIR} = 0$ is provided to control the 8289 Bus Arbiter SYSB/$\overline{RESB}$ pin. This will avoid the need of requesting the system bus to acknowledge local bus non-slave interrupts. The user defines the interrupt system as part of the configuration.

INTERRUPT SEQUENCE

The interrupt sequence is as follows:

1. One or more of the interrupts is set by a low-to-high transition on edge-sensitive IR inputs or by a high input on level-sensitive IR inputs.
2. The 80150 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an interrupt acknowledge cycle which is encoded in $\overline{S_2} - \overline{S_0}$.
4. Upon receiving the first interrupt acknowledge from the CPU, the highest-priority interrupt is set by the 80150 and the corresponding edge detect latch is reset. The 80150 does not drive the address/data bus during this bus cycle but does acknowledge the cycle by making $\overline{ACK} = 0$ and sending the $\overline{LIR}$ value for the IR input being acknowledged.
5. The CPU will then initiate a second interrupt acknowledge cycle. During this cycle, the 80150 will supply the cascade address of the interrupting input at T_1 on the bus and also release an 8-bit pointer onto the bus if appropriate, where it is read by the CPU. If the 80150 does supply the pointer, then $\overline{ACK}$ will be low for the cycle. This cycle also has the value $\overline{LIR}$ for the IR input being acknowledged.
6. This completes the interrupt cycle. The ISR bit remains set until an appropriate EXIT INTERRUPT primitive (EOI command) is called at the end of the Interrupt Handler.

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ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin With
Respect to Ground ..... −1.0V to +7V
Power Dissipation ..... 1.0 Watts

NOTICE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 4.5 to 5.5V)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + .5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400μA
I_{CC}	Power Supply Current		200	mA	T_A = 25°C
I_{LI}	Input Leakage Current		10	μA	0 ≤ V_{IN} ≤ V_{CC}
I_{LR}	IR Input Load Current		10 −300	μA μA	V_{IN} = V_{CC} V_{IN} = 0
I_{LO}	Output Leakage Current		10	μA	.45 ≤ V_{IN} ≤ V_{CC}
V_{CLI}	Clock Input Low		0.6	V	
V_{CHI}	Clock Input High	3.9		V	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		15	pF	
I_{CLI}	Clock Input Leakage Current		10 150 10	μA μA μA	V_{IN} = V_{CC} V_{IN} = 2.5V V_{IN} = 0V

A.C. CHARACTERISTICS (T_A = 0-70°C, V_{CC} = 4.5-5.5 Volt, V_{SS} = Ground)

		80150		80150-2			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Test Conditions
T_{CLCL}	CLK Cycle Period	200	–	125	–	ns	
T_{CLCH}	CLK Low Time	90	–	55	–	ns	
T_{CHCL}	CLK High Time	69	2000	44	2000	ns	
T_{SVCH}	Status Active Setup Time	80	–	65	–	ns	
T_{CHSV}	Status Inactive Hold Time	10	–	10	–	ns	
T_{SHCL}	Status Inactive Setup Time	55	–	55	–	ns	
T_{CLSH}	Status Active Hold Time	10	–	10	–	ns	
T_{ASCH}	Address Valid Setup Time	8	–	8	–	ns	
T_{CLAH}	Address Hold Time	10	–	10	–	ns	
T_{CSCL}	Chip Select Setup Time	20	–	20	–	ns	
T_{CHCS}	Chip Select Hold Time	0	–	0	–	ns	
T_{DSCL}	Write Data Setup Time	80	–	60	–	ns	
T_{CHDH}	Write Data Hold Time	10	–	10	–	ns	
T_{JLJH}	IR Low Time	100	–	100	–	ns	
T_{CLDV}	Read Data Valid Delay	–	140	–	105	ns	C_L = 200 pF
T_{CLDH}	Read Data Hold Time	10	–	10	–	ns	
T_{CLDX}	Read Data to Floating	10	100	10	100	ns	
T_{CLCA}	Cascade Address Delay Time	–	85	–	65	ns	

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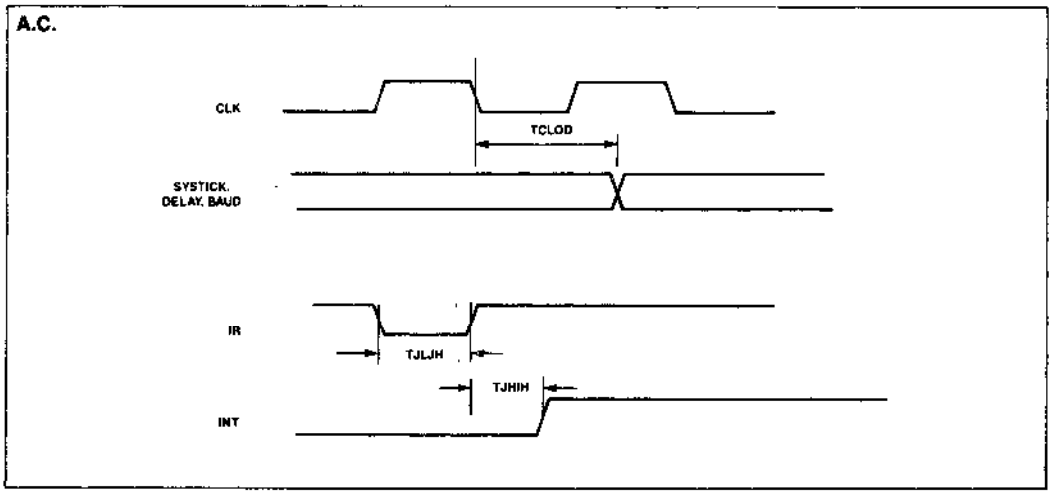
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A.C. CHARACTERISTIC (Continued)

		80150		80150-2			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Notes**
T_{CLCF}	Cascade Addresse Hold Time	10	–	10	–	ns	
T_{IAVE}	INTA Status t Acknowledge	–	80	–	80	ns	
T_{CHEH}	Acknowledge Hold Time	0	–	0	–	ns	
T_{CSAK}	Chip Select to ACK	–	110	–	110	ns	
T_{SACK}	Status to ACK	–	140	–	140	ns	
T_{AACK}	Address to ACK	–	90	–	90	ns	
T_{CLOD}	Timer Output Delay Time	–	200	–	200	ns	C_L = 100 pF
T_{CLOD1}	Timer1 Output Delay Time	–	200	–	200	ns	C_L = 100 pF
T_{JHIH}	INT Output Delay	–	200	–	200	ns	
T_{IRCL}	IR Input Set Up	20		20		ns	

WAVEFORMS

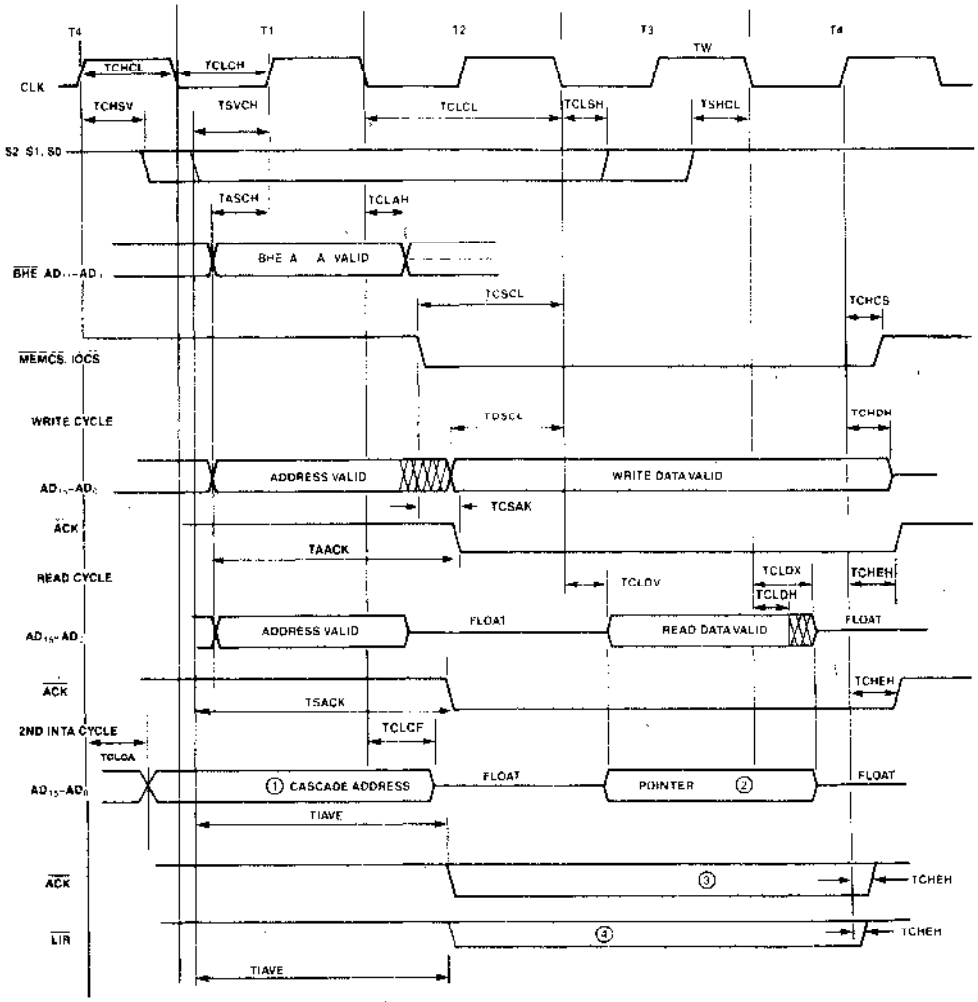
A.C.



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WAVEFORMS

A.C.



NOTES
1. CASCADE ADDRESS PRESENTED ON AD8, AD9 AND AD10 CORRESPONDING TO CAS0, CAS1 AND CAS2 RESPECTIVELY. AD11-AD15 LINES ARE ACTIVE AND HAVE UNKNOWN VALUES. AD0-AD7 ARE TRISTATE.
2. POINTER VALUE IS ACTIVE ONLY IF POINTER IS GENERATED FROM THE 80150 AND NOT FROM EXTERNAL SLAVE 8INT.
3. ACTIVE LOW ONLY WHEN POINTER DATA IS BEING SUPPLIED BY THE 80150.
4. LOW ONLY FOR LOCAL INTERRUPT.

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User Library 8

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The Insite User's Program Library is an Intel-sponsored software library supporting Intel microcomputer products. There are currently over 325 programs in the Library collection.

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As the Library collection is built on programs submitted by Intel employees as well as customers, we encourage and welcome all program contributions. These contributions are essential to the growth and success of Insite.

In the following pages you will be introduced to more in-depth information about Insite. Membership and program submittal forms, including a complete program index listing, are also included for your convenience.

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- **Updates of New Programs Sent During Subscription Period**

Insite, Intel's Software Index and Technology Exchange Library, is a varied collection of programs and routines that have been written by users of Intel microcomputers, single-board computers, and development systems. This expanding library of programs covers a broad range of software tools that includes monitors, conversion routines, peripheral drivers, translators, math packages, and even games. As a library member, you can acquire a copy of any program within the library on any of its available types of media. By taking advantage of the availability of existing library programs, numerous hours of coding and debugging time can be saved and routine or redundant programming operations can be eliminated. The Insite Program Library also serves as a learning tool for individuals unfamiliar with assembly or high-level languages associated with Intel's family of microcomputers.

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Insite™ Program Library Catalog. Each member will be sent the Program Library Catalog consisting of an abstract for each program indicating the function of the routine, required hardware and software, and memory requirements.

Insite members will be updated with abstracts of new programs submitted to the Library during the subscription period. For catalog and yearly subscription fee please refer to the Intel OEM Price List or contact the nearest Insite or Intel Sales Office.

INSITE OFFICES ARE WORLDWIDE, WITH FIVE LOCATIONS TO SERVE YOU:

NORTH AMERICA
Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051
ATTN: Insite User's Program Library
Telephone: 408-987-8080

THE ORIENT
Intel Japan K.K.
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Tsukuba-gun, Ibaraki, 300-26, Japan
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Telephone: 029747-8511

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Telephone: 089-5389-1

Intel Corporation (U.K.) Ltd.
Pipers Way
Swindon SN3 LRJ
Wiltshire, England
ATTN: Insite User's Program Library
Telephone: 0793-488-388

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SUBMITTAL REQUIREMENTS

Programs submitted for Insite review must follow the guidelines listed below:

Programs must be written in a language capable of compilation and assembly by the currently-supported version of an Intel standard compiler/assembler. Accepted languages are documented in the following manuals available through Intel's Literature Department.

- BASIC-80 Reference Manual, Order No. 980758
- FORTRAN-80 Programming Manual, Order No. 980481
- FORTRAN-86 User's Guide, Order No. 121570
- Pascal-80 User's Guide, Order No. 981015
- Pascal-86 User's Guide, Order No. 121539
- PL/M-80 Programming Manual, Order No. 980268
- PL/M-86 Programming Manual, Order No. 980466
- MCS-48 and UPI-41A Assembly Language Manual, Order No. 980255
- MCS-86 Macro Assembly Language Reference Manual, Order No. 121703
- 8080/8085 Assembly Language Programming Manual, Order No. 980940
- 8086/8087/8088 Macro Assembly Language Reference Manual for 8085 Based Development System, Order No. 121623
- 8086/8087/8088 Macro Assembly Language Reference Manual for 8086 Based Development System, Order No. 121703
- 8089 Assembler User's Guide, Order No. 980938
- Microsoft BASIC Compiler Reference Manual, Order No. 121805
- Microsoft BASIC-80 Reference Manual, Order No. 121806
- Microsoft BASIC Reference Book, Order No. 121857
- Microsoft Cobol User's Guide, Order No. 121802
- Microsoft FORTRAN-80 Reference Manual, Order No. 121798
- Microsoft FORTRAN-80 User's Manual, Order No. 121799
- Microsoft M/Sort Reference Manual, Order No. 121809
- Microsoft Utility Software Manual, Order No. 121797
- C-86 Compiler Language User's Guide, Order No. 122085

A well-documented source code furnished on an ISIS-formatted 8" diskette, CP/M-formatted 8" diskette, RMX-formatted 8" diskette, or PDS 5¼" ISIS CP/M diskette.

A source listing of the program must be included. This must be the output listing of a compilation or an assembly. No consideration will be given to incomplete programs or duplications of programs already in the Library.

A link and locate listing (whenever applicable).

A demonstration program which assures the validity of the contributed program must be included. This must show the accurate operation of the program.

A complete submittal form.

Licensed software or copyrighted material must be accompanied by a written release from the appropriate, authorized person.

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INSITE™ USER'S PROGRAM LIBRARY SUBMITTAL FORM

Processor

☐ 8048 ☐ 8051 ☐ 8080/8085 ☐ 8086/8087/8088 ☐ Other _____

Indicate the MDS series model the program was created on by checking the appropriate box, and identify other MDS series models the program may be compatible with.

Program Title

Function

Required Hardware

Required Software

Input Parameters

Output Results

Registers Modified:	**Programmer:**
RAM Required:	**Company:**
ROM Required:	**Address:**
Maximum Subroutine Nesting Level:	**City:**
Assembler/Compiler Used:	**State:**
Programming Language:	**Telephone:**

ACKNOWLEDGEMENT AND AGREEMENT

To the best of my knowledge, I have the right to contribute this program material without breaching any obligation concerning nondisclosure of proprietary or confidential information of other persons or organizations. I am contributing this program material on a nonconfidential nonobligatory basis to the Insite User's Library for inclusion in its program library, and I agree that the Library may use, duplicate, modify, publish, and sell the program material without obligation or liability of any kind. The Insite User's Library may publish my name and address, as the contributor, to facilitate user inquiries pertaining to this program material.

Signature _____ Date _____

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LIST OF PROGRAMS
ALPHABETICAL, BY APPLICATION

Program Title	Order No.
ADD AND SUBTRACT: BCD Numbers	CB11
AEDIT: Tutorial	E7
ASSEMBLER: 8080 MACRO, V4.1	BF4
ASSEMBLER, CROSS: 8008 Code	BC5
ASSEMBLER, CROSS: 8048 On DG Nova	BC6
ASSEMBLER, CROSS: DEC PDP-8 or PDP-11	BC2
ASSEMBLER, CROSS: DEC PDP-11	PC3
ASSEMBLER, CROSS: DEC PDP-11	BC4
ASSEMBLER, CROSS: MCS-48	BC1
ASSEMBLER: MCS-48	BF11
ASSEMBLER, ON-LINE	BF5
BAUD RATE: Detection and Setting Routine for MCS-51	BG50
BAUD RATE: Modify	BG25
BAUD RATE: Modify Under CP/M	BG26
BIT HANDLING: 8048	BG35
BRANCH: MCS-48 Branch Table Routine	BG37
BREAKPOINT: 8089	BD15
CALCULATE: CHECKSUM	BD16
CALCULATE: Sine or Cosine Routine	CB13
CALCULATE: Square Root	CB5
CALCULATION: Least Squares Quadratic Fitting	CB3
CALCULATION: Natural Logarithm	CB4
CAPITALIZE: PL/M-86 Keywords	BG55
CHANGE: Load Addresses, iAPX-86/88 Object File	BG42
CHECKBOOK	BA6
CLOCK: 8748 Clock and LCD Tachometer	BG30
CLOCK: MICRO/SYS MC1460 Real Time Clock Board Utilities	BG31
CLOCK: Real Time	BG29
COMMANDS: Meta-Programs	BG38
COMMUNICATION: DEC PDP-11 to Intellec Development System	BB16
COMMUNICATION: HP Calculator with Intellec Development System-800	AD1
COMMUNICATION: Intellec Development System 220/230 with SDK-85, V1.0	AD4
COMMUNICATION: Intellec Model 220/230 to Timesharing Computer	AD6
COMMUNICATION: Intellec Model 800 to/from DEC PDP-10	AD8
COMMUNICATION: Intellec Development System to/from DEC	AD10
COMMUNICATION: Intellec Development System to/from Tektronix 8001	AD11
COMMUNICATION: Intellec Development System Series-II with Minicomputer	AD9
COMMUNICATION: Intellec Development System Series-II with PROMPT-48	AD2
COMMUNICATION: Intellec Development System PROMPT-48 or -80	AD3
COMMUNICATION: Intellec System to Serial Output Device	AD14
COMMUNICATION: Intel Development System to/from Hewlett-Packard Computer	AD15
COMMUNICATION: Intel Development System to/from VAX 11	AD13
COMMUNICATION: Intel MDS-Data I/O Programmer Interface	BE8
COMMUNICATION: iPDS to/from MDS-800 under CP/M-80	AD19
COMMUNICATION: NDS-II to/from iPDS Running CP/M-80	AD17
COMMUNICATION: Series-III to/from IBM PC or PC-Compatible	AD23
COMMUNICATION: Tektronix DAS 9100 Digital Analysis System to Intel Development System	AD12
COMMUNICATION: Two Intellec Series-II Development Systems	AD7
COMMUNICATION: Xerox File Transfer Facility	AD16

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Program Title	Order No.
COMPARE: 8048 or 8049 ROMS	AE11
COMPARE: Files	BD11
COMPILER: Pascal	BF1
CONSOLE ACCESS: Input and Output for Series III	BD36
CONTROLLER: 8278 Keyboard/Display	AC3
CONTROLLER: 8292 on 8741A	AC4
CONTROLLER: Dual Floppy Disk Drive	AB11
CONTROLLER: Firmware for iSBC-589	AC7
CONTROLLER: PID Control Loops	AB20
CONTROLLER: PROMPT-48 Interactive	AB2
CONTROLLER: UP1-41 8-Digit LED Display	AC1
CONTROLLER: UP1-41A/42 Digital Cassette, V2.5	AC5
CONVERSION: ASCII-Decimal to/from FPAL Number	BB13
CONVERSION: ASCII Floating Point Numbers to AM9711 and Intel 8231 4 Byte FP Format	BB5
CONVERSION: ASCII to Floating Point	BB14
CONVERSION: ASCII to/from EBCDIC	BB1
CONVERSION: ASCII to/from Floating Point	BB11
CONVERSION: ASCII Code to/from Intel Floating Point	BB12
CONVERSION: Binary to BCD	BB6
CONVERSION: Binary to BCD	BB7
CONVERSION: Convert/Format/Print	BB8
CONVERSION: Decimal to/from Floatingh Point	BB9
CONVERSION: FORTRAN or FPAL Floating Point to/from Decimal	BB10
CONVERSION: Hex to ASCII	BB2
CONVERSION: ISIS-II to/from CP/M	BB18
CONVERSION: MCON-6800 Source Code to 8086/88 Source Code	BB3
CONVERSION: ZCON-Z80 to 8086/88 Source Converter	BB4
CONVERT: 8051 Binary to/from BCD	BB24
CONVERT: 8086 HEX File to 8080 HEX File	BB26
CONVERT: ASCII Octal/Decimal/Hexadecimal to ASCII Octal/Decimal/Hexadecimal/Internal Binary	BB27
CONVERT: Double word to ASCII String	BB22
CONVERT: Fixed Point to Floating Point	BB21
CONVERT: FPAL Numbers to/from IBM 32-Bit Floating Point	BB28
CONVERT: Intel HEX Code to BASIC DATA Statements	BB25
CONVERT: ISIS Object Module to CP/M Object Module	BB23
COPY: Disk	BG28
COPY: Diskette	BG27
COPY: Diskette	BG43
COPY: iPDS CP/M-80 Diskette	BG45
COPY: PDP—11 Disk File to Intel ISIS-II Disk File	BB15
COUNT: ICE-80 Machine Cycles	BD10
COUNT: Program Usage	BG40
CREDIT: Tutorial	E6
CREDIT: Used on Modified Hazeltine 1500	BG33
DEBUG: CAT.88 (iRMX88 Task Debugger)	BD34
DEMO: 208	AE7
DEMO: iAPX-88	AE13
DEMO: iRMX 86 Multitasking Spectrum Analysis	AE8
DEMO SOFTWARE: 8275	AE6
DEVICE, I/O: UPI-41A Combination	AC2
DIAGNOSTIC: 8080 I/O	AE2
DIAGNOSTIC: Microcomputer Development System 230	AE9
DISASM	BD6
DISASSEMBLER: 8048 Object Code	BD8

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Program Title	Order No.
DISASSEMBLER: 8080 Code	BD1
DISASSEMBLER: 8080 Code	BD4
DISASSEMBLER: 8080 Object Code	BD2
DISASSEMBLER: ICE-80 Ver 2.1	BD3
DISASSEMBLER: ISIS-II Object Files	BD5
DISPLAY: ISIS Directory under CP/M	BG46
DIVISION: 32-Bit by 16-Bit	CB12
DOWNLOAD: iPDS to Serial Port	AD18
DRIVER: 8048 Seven-Segment Display	AB5
DRIVER: 8085 Serial I/O	AB1
DRIVER: Audio Cassette Recorder	AB6
DRIVER: Bios and Boot Program for CP/M-80	AB22
DRIVER: Cassette Operating System	AB7
DRIVER: Dumb Terminal Simulator	AB10
DRIVER: Intellec Development System Series-II as Dumb Terminal	AB9
DRIVER: iPDS Dumb Terminal	AB23
DRIVER: iSBC 86/12 Real Time Clock Driver	AB19
DRIVER: Okidata Microline 84 Line Printer	AB25
DRIVER: PROM Programmer	BE7
DRIVER: RMX-80, for the iSBC 254 Bubble Memory with 80/10 Board	AB14
DRIVER: RMX-80, for the iSBC 254 Bubble Memory with 80/20/30 Board	AB15
DRIVER: RMX-86, for the iSBC 254 Bubble Memory Board	AB16
DRIVER: RMX-80 for iSBC 534	AB12
DRIVER: RMX-80 for SBC 215 Controller Board	AB13
DRIVER: RMX-86, for the iPAB-128, iPAB-256, iSBX-251 Bubble Memory Products	AB17
DRIVER: RMX-86, High Performance Drver for iSBC-550 Ethernet Communications Controller	AB18
DRIVER: SYCOR 135 Cassette Operating System	AB8
DRIVER: Tektronix 4010 Graphic Screen	AB3
DRIVER: T.I. Omni 810 Lineprinter	AB4
DRIVER: USART for iSBC-86/XX	AB21
DUMP: Diskette	BD27
DUMP: Diskette File	BD28
DUMP: Diskette File	BD26
DUMP: iAPX-86/88 Absolute Object File	BD30
DUMP: iSBC 86/12 Memory	BD29
DUMP: Screen	BG54
DUMP: Symbol Table	BD21
EDIT: Disk	BD33
EDIT: Hex File	BD31
EDIT: Inspect and Change File	BD32
EDIT: Text	BA4
EDITOR: Text, Intel X111	BA3
EXECUTIVE: Real Time	AA8
EXERCISE: Data Translation MULTIBUS Analog I/O Boards	BE6
FIFO	BG13
FIFO	BG12
GAME: Bandit	D3
GAME: Black Box	D15
GAME: Breakout	D13
GAME: Craps	D5
GAME: Darts	D6

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Program Title	Order No.
GAME: Fruit Machine	D4
GAME: Hangman	D7
GAME: Mastermind	D9
GAME: Maze	D2
GAME: Maze	D1
GAME: Othello	D10
GAME: Poker	D14
GAME: Slalom, V1.4	D8
GAME: Tiny Chess 86	D12
GENERATE: 16-Bit Random Number	CB2
GENERATE: Calendar	BA8
GENERATE: CCITT Cyclic Redundancy Check	BD37
GENERATE: Disk Directory Library	BA15
GENERATE: Fast Generation of IBM Bi-Sync CRC16	BD20
GENERATE: Graph	CB7
GENERATE: High and Low Bytes from 8086 Hex File	BD35
GENERATE: Histogram	CB8
GENERATE: IBM Bi-Sync CRC16	BD19
GENERATE: Music for SDK-85	D11
GENERATE: Output Signal	BG5
GENERATE: PL/M Cross Reference	BD25
GENERATE: PROM Checksum Calculation	BD18
GENERATE: Public Symbol Cross Reference	BD38
GENERATE: Public Symbol Cross Reference (Update)	BD24
GENERATE: Random Number	CB6
GENERATE: Software Documentation	BA14
GENERATE: Stochastic Variates and Histograms	CA23
GENERATE: Symbol List	BD24
GENERATE: Symbol Table for BASIC-80	BD23
GENERATE: Tabs	BA16
GENERATE: X-Y Graphs	CB9
HANDLER: Enhanced RMX-80 Terminal Handler	BE10
HANDLER: RMX/80 Minimal Terminal	BE2
INCREMENT: Program Counter	BG39
INFO: NDS-II File Information Utility	BG56
INITIALIZE: Baud Rate	BG24
INITIALIZE: Baud Rate	BG23
INTERPRETER: 8086 Tiny BASIC	BF9
INTERPRETER: Interactive 8087 Instruction Interpreter	AA12
INTERPRETER: LISP	BF3
INTERPRETER: LLL BASIC-II	BF7
INTERPRETER: LLL/Chernack BASIC	BF8
INTERPRETER: MCS-51 Tiny BASIC, V2.2	BF10
INTERPRETER: PILOT-80	BF2
INTERPRETER: RMX/80 Command Line	BG4
INTERPRETER: Single-Step	BD7
LINKAGE: Series III i8087 Linkage Modules	BG36
LIST: 8086 Public and External Symbols	BD41
LIST: Directory, ISIS Diskette/NDS Disk	BG18
LIST: Diskette Directory	BG17
LIST: File	BG15
LIST: File	BG16
LIST: File Errors	BD12
LIST: PL/M Compiler Errors	BD13

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Program Title	Order No.
LIST/PRINT/TYPE	BG14
LIST: Save Error	BD14
LOAD/SAVE: RAM	BG1
MACROS: Block Structures	BG10
MACROS: Block Structures	BG11
MACROS: Enhancements for Credit Text Editor	BA22
MAIL LIST	BA9
MAIL LIST	BA11
MAIL LISTS FOR BASIC 80	BA12
MATH PACKAGE: 8231	CA17
MATH PACKAGE: 8051	CA18
MATH PACKAGE: 8080/8085 Fundamental Support Package	CA20
MATH PACKAGE: 8231 Arithmetic Processing Unit	CA16
MATH PACKAGE: Arithmetic Functions	CA11
MATH PACKAGE: Arithmetic Functions for MCS-48	CA22
MATH PACKAGE: Double Precision Floating Point	CA12
MATH PACKAGE: Double Precision Integer	CA4
MATH PACKAGE: Fixed and Floating Point	CA5
MATH PACKAGE: Floating Point	CA2
MATH PACKAGE: Floating Point	CA1
MATH PACKAGE: Floating Point	CA7
MATH PACKAGE: Floating Point	CA6
MATH PACKAGE: Floating Point Library/8086	CA13
MATH PACKAGE: Floating Point Utilities for FPAL.LIB	CA8
MATH PACKAGE: High Speed Binary Math Package for 8031/8051	CA21
MATH PACKAGE: Multiple Precision Arithmetic/8086	CA14
MATH PACKAGE: Multiplication, Division, and BCD-Binary Binary-BCD Conversion for 8051	CA24
MATH PACKAGE: Multiply/Divide	CA15
MATH PACKAGE: Optimized Floating Point	CA9
MATH PACKAGE: Optimized Floating Point	CA10
MATH PACKAGE: PL/M Multiple Precision	CA3
MATH PACKAGE: Recursive Computation of Mean and Standard Deviation	CA19
MERGE: Mailing List	BA10
MONITOR: Intellec 8/MOD80	AA1
MONITOR: Bubble Memory Development Software for Intel BPK-72	AA10
MONITOR: HSE-49 Expansion Monitor	AA13
MONITOR: Intellec Development System, V2.0	AA6
MONITOR: iSBC 250 1-Megabit Bubble Memory	AA9
MONITOR: iSBC 254 Bubble Memory Board Monitor	AA11
MONITOR: iSBC 544	AA7
MONITOR: iSBC 80/05 or 80/04	AA14
MONITOR: iSBC 80/10	AA15
MONITOR: iSBC 80/10 or 80/10A	AA16
MONITOR: iSBC 80/20 or 80/20-4	AA17
MONITOR: iSBC 80/24	AA18
MONITOR: iSBC 80/30	AA19
MONITOR: iSBC 86/12 Numeric Processor Extension (NPX) Monitor	AA2
MONITOR: SDK-85, V2.0	AA3
MONITOR: SDK-86 Keypad	AA5
MONITOR: SDK-86 Serial, V1.1	AA4
MONITOR: Super Monitor 80	AA20
MONITOR: Super Monitor 86	AA21
MONITOR: Super Monitor 86 for the iSBC 88/45	AA22
MORSE CODE TUTOR V2.0	E3

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Program Title	Order No.
MULTIPLICATION: 8748 BCD	CB10
MULTIPLICATION: 40-Bit	CB14
PRINT .86	BG58
PRINT: Cover Page	BA1
PRINT: Discounted Cash Flow	BA7
PRINT: File	BA17
PRINT: Files	BA18
PRINT: Files	BA19
PRINT: High Speed Utility	BG32
PROCEDURE: Pascal 86 Screen/Cursor Control	BG34
PROCEDURE: PL/M DOCASE	BG9
PROCEDURES: PL/M-86 General Purpose Library	BG49
PROCEDURES: PL/M Output	BG8
PROCEDURES: PL/M Utilities	BG7
PROCESSOR: Macro	BF6
PROCESSOR: Text	BA5
PROGRAM: 8741A as iSBC 941	AC6
PROGRAMMER: EPROM-8755A	BE5
PROGRAMMER: EPROMS 2708/16/32	BE4
PURGE: Symbol Tables	BD42
READ/PUNCH: Paper Tape to/from SDK-85 RAM	BE3
RECEIVE	AD5
RECOVER: Diskette	BG2
RECOVER: Lost AEDIT Files	BG51
RECOVERY: Diskette File	BA2
RELOCATE	BG41
REMOTE: NDS-II Communication with IBM PC running MS/DOS	AD22
REMOTE: NDS-II Communication with iPDS/Series-II/III/IV (UPDATE)	AD20/ AD21
REMOTE: Terminal Control on Series-II under CP/M-80	AB24
REMOTE: IRMX-86 Communication Program	AD24
REPORT: Status of Exported Job	BG44
RUNOFF: ASCII Text File to Epson Printer	BG48
SEND: CP/M-80 PDS Files to Printer Via Modems	BG53
SEND: Intel HEX Code to PROM Programmer	BE9
SEND: ISIS-PDS Files to Printer Via Modems	BG52
SIMULATE: iACX-96	BD40
SIMULATE: Light Box	E8
SIMULATOR: 8048/49 Code, V1.3	BB19
SIMULATOR: 8048/49 Simulator	BB20
SORT: Bubble Sort and Binary Search Routines	BG22
SORT: Disk Directory	BG19
SORT: Disk Directory	BG20
SORT: Diskette File	BG21
SORT: General	BA13
SORT: Public Symbols	BD39
SORT: Symbol Table from an Absolute File	BD22
SOURCE FILES: iAPX-86/88 System Workshop Summary and Review	E1
SOURCE FILES: iAPX-80/85 System Workshop Summary and Review	E2
SPELL	BA21
SUBMIT: ISIS Command String	BG6
SWEEP: ISIS-II General Disk File Utility	BG47

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Program Title	Order No.
TEST: 8080 CPU	AE1
TEST: iSBC 80/10 I/O Ports	AE3
TEST: Error Correcting Code	AE12
TEST: MCS-48 Family CPU	AE10
TEST: Memory	AE5
TEST: Memory	AE4
TEST: PROM/ROM Checksum Self-Test	BD17
TEST: RAM	AE14
THERMOMETER: Thermistor Controlled	BE1
TRACE: ICE-80	BD9
TRANSFORM: DISCRETE Fourier	CB1
TREE: Utilities for Series-IV or NRM	BG57
UTILITIES: Circular Lists	BG3
UTILITIES: Menu	E5
UTILITIES: RT11 Diskette Utility for Intellec 800	BB17
UTILITIES: Talk	E4
WORD PROCESSOR	BA20

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Appendix A

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INTEL SOFTWARE STANDARDS

Intel's software is built on standards which facilitate software portability and provide an open system for software.

Intel's software utilizes the emerging standards in graphics, networking, database and portable operating system interfaces. This base system software provides a mapping from architectural and operating system dependencies to a standard interface. High-level applications are built from the standard interfaces and remain portable across multiple configurations and operating systems. Figure 1 illustrates the open software model relationship.

OPEN SOFTWARE MODEL

Applications	Languages R & L	Word Processing	Spread Sheet	Mail & Document Filling	Business Graphics	Project Management
Base System Software	UDI	Language Run-Time	LAN	Graphics	Database	
Operating Systems	RMX, Xenix CP/M, MS-DOS					
Micro-processors	86, 186, 286, 386					

Figure 1

Intel has supported its fundamental software across multiple operating systems through the UDI operating system interface. By writing software to use the UDI interface which provides memory management, I/O routines, and exception handling—Intel is able to port high level languages, language run-time, and fundamental software to a new release or new operating system in minimal time. Thus Intel's software is operating system independent.

Intel's local area networking products use the IEEE 802.3 CSMA/CD Access Method and physical layer. The work for this standard was done jointly by Intel, DEC, and Xerox and is commonly known as the Ethernet protocol. The transport layer uses the proposed ISO transport protocol specification.

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Intel supports the ANSI graphics standardization effort and will offer products which utilize these standards. The Virtual Device Interface (VDI) standard developed by the ANSI X3H3 committee is intended to provide a single standard which supports mulitple graphics devices with the same set of graphics functions. A companion standard Virtual Device Metafile (VDM) will give a means of storing or transmitting pictures as streams of VDI functions. A third graphics standard being supported by Intel is the North American Presentation Level Protocol Syntax (NAPLPS). NAPLPS is suited for raster-scan display (both CRT and hardcopy) and is currently in final approval stage by ANSI.

Intel's Pascal and FORTRAN adhere to the ANSI standard and support optional extensions. All Intel languages (ASM-86, PL/M, FORTRAN, and Pascal) use common data types and parameter passing conventions to allow inter-language calls. The real number data types in these languages utilize the IEEE real math standard and use the numerics coprocessor or an emulator to support the real math operations and functions. The object module formats (OMF) are commonly used by all of the 86 language products as well as many language products supplied by independent software vendors.

INTEL SOFTWARE STANDARDS DOCUMENTS

Standard	Document
UDI	Run-Time Support Manual For iAPX 86, 88 Applications, Appendix A (Intel 121776-002)
NAPLPS	Intel's Guide To Understanding The ANSI Videotex Presentation Level Protocol (Intel 145412-001)
VDM, VDI	Draft of proposed American Standard for the Virtual Device Metafile, ANSI X3H33 Virtual Device Interface Task Group
Local Area Network	
— Data link and physical layer (Ethernet)	Draft IEEE Standard 802.3 CSMA/CD Access Method and Physical Layer Specifications, IEEE Computer Society
— Transport layer	ISO draft proposal 8073 Information Processing Systems, Open Systems Interconnection-Connection Oriented Transport Protocol Specification
FORTRAN 77	Intel's extension to ANSI FORTRAN 77 specified in FORTRAN-86 User's Guide (Intel 121570-002)
Pascal	Intel's extension to ANSI Pascal specified in Pascal-86 User's Guide (Intel 121539-001)
Real Math	Draft 10.0 of IEEE Task P754, December 1982.
	8087 Support Library Reference Manual (Intel 121725-001).
Language Data Types, and Parameter Passing	
— Pascal	Pascal-86 User's Guide, Appendix J (Intel 121539-003)
— FORTRAN	FORTRAN-86 User's Guide, Appendix H (Intel 121570-002)
Object Module Formats	
— 86	8086 Relocatable Object Module Formats (Intel 121748-001)
— 286	The Concrete Representation of 80286 Object Modules, Intel internal document
	iAPX 286 Compilers Writer's Guide, (Intel-in preparation)

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Intel's Software Support Services is a comprehensive range of post-sales support programs for software and systems purchased from Intel. Its objectives are to maximize the system's performance and minimize unnecessary downtime for greater productivity. These services are provided for all Intel developed and most Intel marketed third-party software.

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   Software Problem Reporting Service (SPR)
   Intel will respond to written questions (submitted on a standard SPR form) on product-specific software, system, or documentation issues. Intel will verify receipt of the SPR promptly and normally will respond within approximately 3 weeks. Intel does not guarantee a resolution will always be available to specific problems.

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   — operational understanding.
   Obtain product specific information.
   — problem identification.
   — work-around, patch, or other solution when available.
   — information on existing SPRs.
   If the reported condition is not an already documented SPR, obtain assistance in problem isolation techniques.

   As part of the TIPS, Software Support Services maintains a list of reported problems and problem resolutions. TIPS does not include user application assistance or engineering time to derive a resolution to a problem if none is currently available. (See Phone Consulting under Consulting Services.) However, the Software Support Engineer will submit a problem report into the SPR system under the Customer name when appropriate.

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We have structured very specific support packages to assist our customers with the installation and reconfiguration of such systems as NDS-II, 86/330, RMX and XENIX. See Intel's current price book for a listing of support packages available today.

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Intel's Software Index and Technology Library is a library of programs that have been submitted by users of Intel microcomputers, single-board computers, and development systems. Membership in INSITE enables the Customer to order programs at a nominal charge. Members are provided a program catalog and catalog updates.

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B. Software support services do not include hardware maintenance.

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A. Software Support Services is Intel's commitment to providing the customer with consistent, high-quality, post-sales software support. It is our way of delivering guaranteed support which the customer can rely on. To tailor a full service software support program that addresses specific needs, contact the local Intel sales or service office for more information.

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C. Charges: There are three kinds of billings utilized with the service offerings: front-end billing, monthly billing (not less than $100 per month), and post-service billing. The customer will be billed on one of the referenced types of billings, depending on the type of service. Prices will be those specified in the current Intel price list.

D. In order to obtain maximum service from Software Support Services, it is advised that the customer maintain the system to the latest revision level, and assign a System Manager who will be the key contact for Software Support Services.

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   2. The License Fee or List Price for covered software products includes a period of Initial Support as defined in individual product descriptions. Additional support services may be obtained as listed in the price list.

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iRUG DESCRIPTION

iRUG is the Intel iRMX™ 86 User's Group. It is a non-profit group chartered to establish a forum for users of the iRMX 86 Operating System and to promote and encourage development of iRMX 86 based software.

iRUG membership is free to licensed iRMX 86 Operating System users and to their employees. Benefits of membership include: access to the user's library of iRMX software tools and utilities; membership in local and national chapters; access to the group bulletin board; receipt of quarterly national newsletters; synopsis of software problem reports (SPRs) submitted by members; opportunity to present papers and conduct workshops; invitations to seminars devoted to the use of Intel products.

The user's library, maintained by iRUG, contains software programs written and submitted by members and Intel employees. Programs available range from file or directory manipulation commands and terminal attribute selection utilities to dynamic logon, background job facilities and basic communication utilities.

Programs in the library are available through a telephone dial-up service.

Local and national iRUG chapters provide a forum for members to meet other iRMX Operating System users in an informal setting. At local meetings and the annual international seminar, members can discuss their ideas, share their experiences and techniques, and give feedback to Intel for future improvements and features of the iRMX 86 Operating System. The meetings also showcase new products offered by Intel and other developments in iRMX based software supplied by other companies.

iRUG sponsors a Special Interest Group (SIG) on the CompuServe Information Service. The SIG offers two features, message facilities and an online conference facility. The message facility (buttetin board) allows members to leave and receive messages from other members. These might include problems and solutions regarding the iRMX 86 Operating System or new techniques to be shared. The online conference facility allows users to hold scheduled meetings on any topic. Whatever information a member types at his/her terminal will be displayed at all terminals logged into the conference facility.

"Human Interface" in iRUG's quarterly national newsletter in the United States. It serves as a supplement to chapter meetings by providing: library listings, informtion on the latest releases of products running on the iRMX 86 Operating System; officer messages; member SPRs; release and update plans for the iRMX Operating System; and member articles.

If you are interested in becoming a member of iRUG or desire further information contact the Intel iRUG liason.

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