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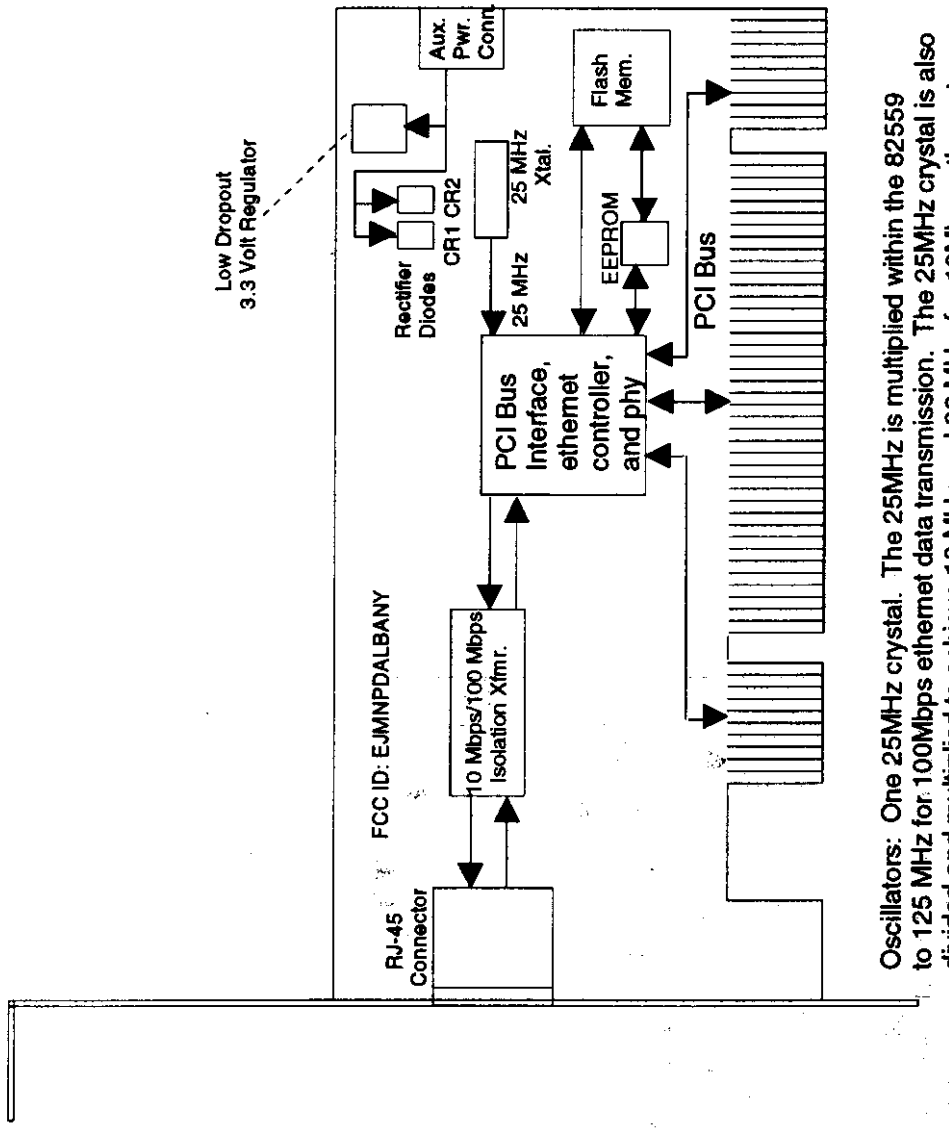
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4.0 Block Diagram of EUT



Oscillators: One 25MHz crystal. The 25MHz is multiplied within the 82559 to 125 MHz for 100Mbps ethernet data transmission. The 25MHz crystal is also divided and multiplied to achieve 10 MHz and 20 MHz for 10Mbps ethernet data transmission.

PB 721503-004 10/100 Mbps ethernet, PCI Bus, LAN adapter with management functions.

Figure 1.

4.1 Block Diagram Description

Refer to figure 4.0 for the block diagram.

82559 Ethernet Controller, PCI Bus Interface Controller, and 10/100 Mbps Ethernet Physical Layer

- Interfaces to the host PC (Personal Computer) through the PCI bus. The PCI bus address, data, and control lines connect the PC to the 82559's internal Ethernet Controller/PCI Bus Interface Controller (also referred to as the MAC-Media Access Controller). Data is transferred between the 82559 and the PC under software direction.
- The 82559 provides specific functions required to assemble/interpret data to/from the network.
- Internal registers in the 82559 are configured, controlled, and accessed by the host PC, under software direction. These registers are used in both 10Mb/s and 100Mb/s modes.
- The 82559 implements the local host DMA (Direct Memory Addressing) functions, the local or host memory structure logic, and the specific I/O bus interface logic.
- The 82559 has internal RAM that is used to implement the FIFO required to buffer incoming and outgoing data.
- The 82559 also communicates with the serial EEPROM and the parallel flash module for configuration and stored software.
- The 82559's internal Physical Layer (or PHY) provides the physical layer interface and analog signaling to communicate on 100BASE-TX and 10BASE-T ethernet interfaces.
- The 82559's internal PHY interfaces with the Isolation Transformer using analog differential pairs (one pair for transmit, one pair for receive).

10/100 Isolation Transformer

- The Isolation Transformer provides electrical isolation between the 82559 and the RJ45 connection to the ethernet.
- The Isolation Transformer provides common mode rejection of high frequency noise for 10Mb/s and 100 Mb/s operation.

Low-Dropout 3.3 Volt Regulator

- This is the device that regulates the voltage conversion from 5 volts to 3.3 volts. (The 82559 is powered by 3.3 volts.

25 MHz Crystal

- The 25 MHz Crystal provides a 25 MHz clock signal to the 82559 which is multiplied up to 125 MHz for 100Mb/s operation, and divided down to 20 MHz and 10 MHz for 10Mb/s operation.

Serial EEPROM

- The Serial EEPROM is a non-volatile IC which contains configuration data that is read by the 82559 when the board is powered up. The data may be changed by the 82559, under software control.

Flash Memory

- The Flash Memory is an optionally installed device that provides software code that can be loaded through the 82559 to the host PC. The contents of the Flash Memory can be modified by host software through the 82559.

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