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Intel® NetStructure™ ZT 5504

System Master Processor Board

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Revision History

Revision Date	Revision History
03/19/02	Added information on use in 3.3V systems. Removed Optional CompactFlash Carrier appendix.
06/06/02	Added references to the ZT 96080 and to the ZT 96080 user documentation.

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Manual Organization

This manual describes the operation and use of the Intel® NetStructure™ ZT 5504 System Master Processor Board with a Mobile Intel® Pentium® III Processor - M. The following topics are covered in this manual.

**Chapter 1, "Introduction," ** introduces the key features of the ZT 5504. This chapter includes a product definition, a list of product features, and a functional block diagram with a brief description of each block. This chapter can be used to compare the features of the ZT 5504 against the needs of a specific application.

**Chapter 2, "Getting Started," ** provides unpacking instructions and initial setup information for the ZT 5504. This chapter summarizes configuration information and should be read before using the board.

**Chapter 3, "Configuration," ** describes the switches and cuttable traces on the ZT 5504. This chapter details factory default settings and provides information about tailoring the board to the needs of specific applications.

**Chapter 4, "Reset," ** discusses the reset types and reset sources available on the ZT 5504.

**Chapter 5, "System Monitoring and Control," ** lists various system monitoring and control features available on the ZT 5504.

**Chapter 6, "IDE Controller," ** provides an introduction to the ZT 5504's IDE Controller. This chapter covers drive configuration, IDE I/O mapping, device drivers, and the ZT 5504's support for internal and external disk drives.

**Chapter 7, "Watchdog Timer," ** explains the operation of the ZT 5504's watchdog timer. Sample code is provided to illustrate how the watchdog's functions are used in an application.

**Chapter 8, "BIOS Recovery," ** discusses recovery from and correction of a corrupted BIOS.

**Appendix A, "Specifications," ** contains the electrical, environmental, and mechanical specifications for the ZT 5504. This chapter also provides a connector location illustration and connector pinout tables.

**Appendix B, "Thermal Considerations," ** describes the thermal requirements for reliable operation of the ZT 5504.

**Appendix C, "System Registers," ** provides a detailed description of the system registers available for monitoring and controlling various board operations.

**Appendix D, "Datasheet Reference," ** provides links to Websites with information about many of the devices and technologies used in the ZT 5504.

**Appendix E, "Agency Approvals," ** presents UL, CE, and FCC agency approval and certification information for the ZT 5504.

**Appendix F, "Customer Support," ** provides technical and sales assistance information.

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1. Introduction

This chapter provides an introduction to the ZT 5504 including a product definition, a list of product features, and a functional block diagram with descriptions of each block.

The "ZT 5504 Faceplate" illustration identifies the connectors, indicators, and switches available on the ZT 5504's faceplate. Optional rear-panel transition boards are available to extend various faceplate features to a system's rear-panel. For more information about compatible rear-panel transition boards, see the *Intel NetStructure ZT 4807 Packet Switched Rear-Panel Transition Board Hardware Manual*.

Product Definition

The Intel NetStructure ZT 5504 System Master Processor Board is a single board computer designed to work as a modular component in a high-performance CompactPCI* system. It utilizes the Mobile Intel Pentium III Processor - M, in a BGA2 package, to provide extremely high PCI performance and the latest in memory and I/O technology combined with low power requirements. The ZT 5504 includes CompactPCI Packet Switching Backplane (CompactPCI/PSB) compliance and Intelligent Platform Management Bus (IPMB) system management features. The ZT 5504 CPU board is an ideal solution for telecommunications, Internet, and industrial control applications with demanding performance and system reliability requirements.

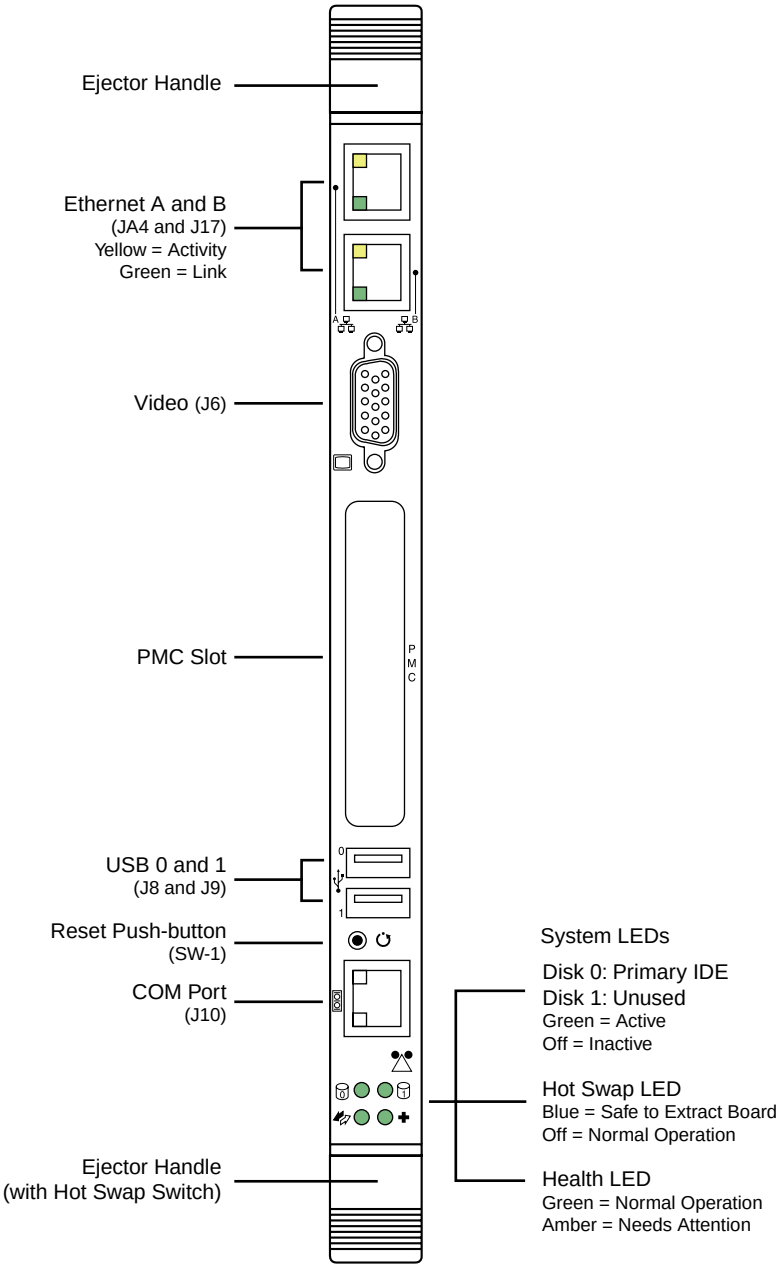
The ZT 5504 occupies a single 6U high Eurocard slot. The board can be used as a System Master or it can operate in "Drone Mode" when installed in a peripheral slot. When in Drone Mode the ZT 5504 operates on its own without communicating over the CompactPCI bus.

Though the ZT 5504 is highly integrated, its capabilities can be extended with optional boards available from Intel. Expansion boards are available to add IDE devices such as a CD-ROM drive or CompactFlash and transition boards are available to extend I/O access to the rear of a system. For more information about options and accessories, including the ZT 96080 CompactFlash Carrier, see the Intel NetStructure building blocks page at:

http://developer.intel.com/design/network/products/cbp/linecard.htm

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ZT 5504 Faceplate



Features

- *CompactPCI Specification, PICMG 2.0, Version 2.1* and *CompactPCI Specification, PICMG 2.16, Version 1.0* compliant
- 6U single-slot CompactPCI form factor
- Mobile Intel Pentium III Processor - M, BGA2 package
- Intel® 440 GX chipset

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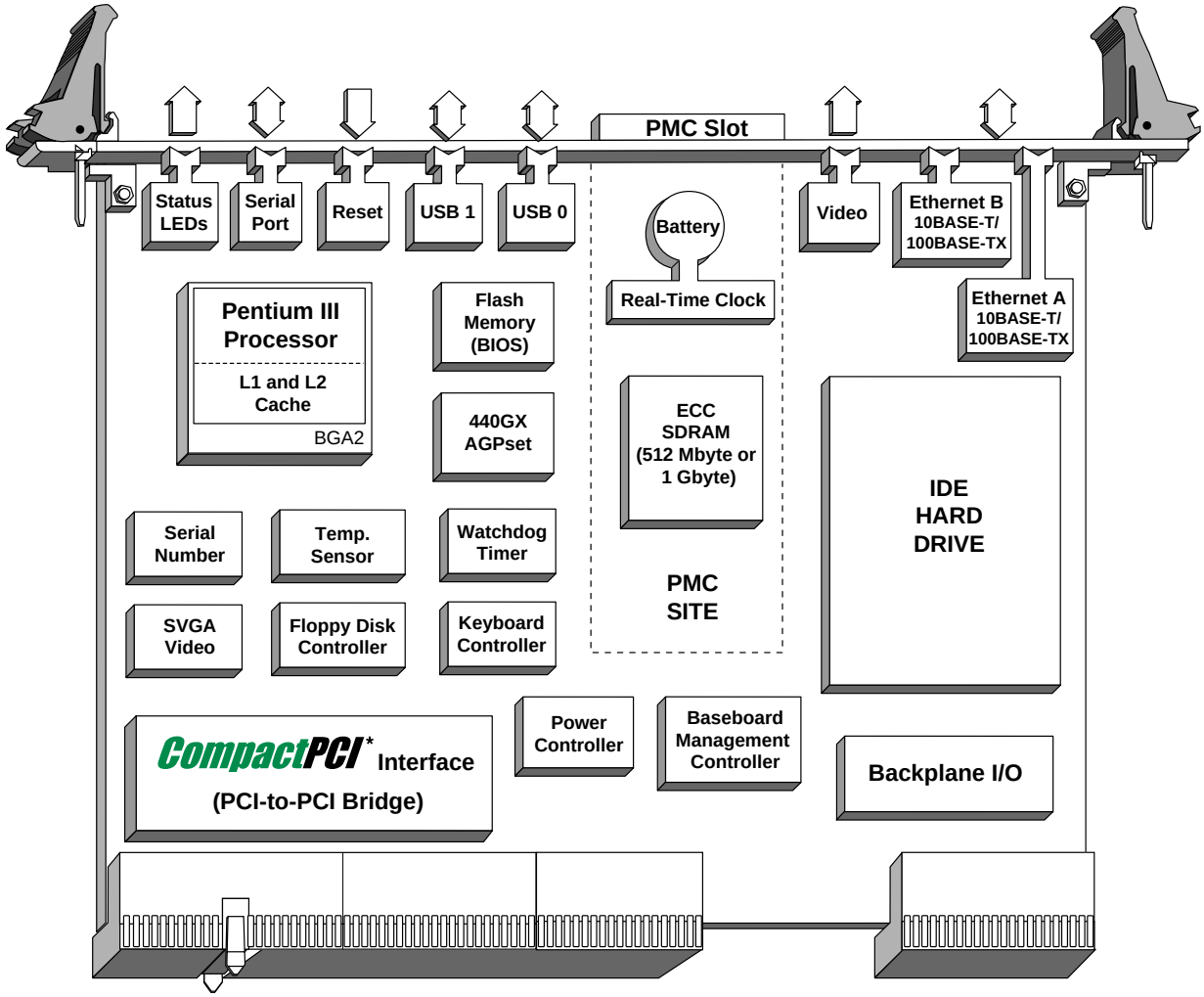
- Built-in numeric coprocessor support
- 16 KB of CPU instruction cache
- 16 KB of CPU data cache
- 256 KB of Level 2 cache
- 512 MB or 1 GB of ECC SDRAM
- BIOS stored in flash memory
- Standard AT* Systems include:
  - Two enhanced interrupt controllers (8259)
  - Three counter/timers (one 8254)
  - Real-time clock/CMOS RAM (146818)
  - Two enhanced DMA controllers (8237)
  - 8042 compatible keyboard controller
  - Speaker interface
  - PS/2 mouse and keyboard
- Dual stage watchdog timer
- Intel® 69000 series AGP graphics chip
- IPMI through an Intel® Baseboard Management Controller chip
- Dual 10/100 Mbit/s Ethernet* (available at the faceplate or the J3 backplane connector)
- Primary IDE channel supports the on-board 2.5 inch hard disk and an IDE device (CD-ROM) on a media expansion board
- Single on-board PCI Mezzanine Card (PMC) slot, 32-bit @ 33 MHz using 3.3V signaling
- Two 16C550 RS-232 serial ports (COM1 available at the faceplate, COM1 and COM2 available through the J5 backplane connector)
- Push Button Reset on the front panel
- Rear-Panel I/O Availability (at J5) includes the following
  - Secondary IDE channel
  - Rear panel eject
  - Push-button reset input
- DC power monitors (+3.3V, +5V, +12V, -12V, and CPU core voltage)
- Support for Windows* 2000 Professional, Windows 2000 Server, Linux*, and VxWorks*

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Functional Blocks

The following topics provide overviews of the ZT 5504's main features, some of which are shown in the functional block diagram below.

Functional Block Diagram



CompactPCI/PSB Architecture

The ZT 5504 is designed to operate in a CompactPCI Packet Switching Backplane (CompactPCI/PSB) system. The CompactPCI/PSB specification is an extension to the PICMG 2.x family of specifications that overlays a packet-based switching architecture on top of CompactPCI to create an Embedded System Area Network (ESAN). CompactPCI/PSB supplements the robust, reliable and hot-swap capable CompactPCI architecture with the easily integrated, low-cost, high-performance, and extensible Ethernet.

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When used in accordance with the *CompactPCI Packet Switching Backplane Specification, PICMG 2.16, Version 1.0*, the ZT 5504 functions as a "Dual Link Port Node" board. The ZT 5504 can be connected to a system's fabric-switched Link Ports A and B, and can be inserted into system or peripheral slots. The ZT 5504 is keyed for insertion into compatible slots.

The "CompactPCI" topic in Appendix E contains a link to the PCI Industrial Computer Manufacturers Group.

Processor

The ZT 5504 uses the Mobile Pentium III Processor - M in a BGA2 package. The 0.18 micron BGA2 package is a highly integrated assembly containing a mobile version of the Pentium III processor and its immediate system-level support. This mobile processor runs at a lower voltage than the desktop version.

The 256 KB on-die transfer L2 cache is integrated with the CPU, eliminating the need for separate components and improving performance. The BGA2 package Pentium III processor also operates with a 100 MHz Processor Side Bus for faster access to memory and data.

The "Mobile Pentium III Processor - M in BGA2 Package" topic in Appendix E contains a link to the datasheet for the processor.

Chipset

The Intel 440GX AGPset consists of the 82443GX Host Bridge and the 82371EB (PIIX4E) I/O subsystem chip. The Host Bridge includes an optimized SDRAM controller. The I/O subsystem is a highly integrated PCI ISA IDE Xcelerator Bridge.

The "Intel 440GX AGPset" topic in Appendix E contains a link to information about the chipset.

PCI-to-PCI Bridge (P2P)

The ZT 5504 features one Intel® 21154 PCI-to-PCI bridge to support the J1/J2 CompactPCI buses. The bridge provides the isolation, arbitration, and clocks for seven PCI peripheral cards without the need for an external bridge board.

Special features of the 21154 include:

- 33 MHz or 66 MHz PCI bus operation
- Support for independent primary and secondary PCI clocks
- 64-bit PCI operation

The "PCI-to-PCI Bridge" topic in Appendix E contains a link to information about the chipset.

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Memory and I/O Addressing

The ZT 5504 supports 512 MB or 1 GB of local memory. This memory is installed at the factory and is not field upgradeable. The local memory is implemented as Error-Correcting Code (ECC) SDRAM. ECC will correct single bit errors (97% of all DRAM errors are single bit errors) and can report multiple bit errors to the operating system. How ECC errors are reported is a BIOS setup option.

In addition to SDRAM, the ZT 5504 uses an on-board flash memory device to store the system BIOS.

See the "Memory Configuration" and "I/O Configuration" topics in Chapter 2 for more information.

Drone Mode

Typically, the ZT 5504 operates as the System Master from the system slot. The ZT 5504 can also operate in Drone Mode from a peripheral slot. In Drone Mode, the CPU board receives power from the system but it cannot communicate on the CompactPCI bus. Onboard logic uses SYSEN# to qualify the ZT 5504's location when inserted in a peripheral slot, thereby isolating the board from the CompactPCI bus.

The ZT 5504 can be hot swapped when operating in Drone Mode (in peripheral slots, the board is operating in isolation from the backplane).



CAUTION: The ZT 5504 is not intended to be hot swapped in the system slot. Hot swapping the CPU board in the system slot may damage other boards in the system.

Power Ramp Circuitry

The ZT 5504 features a power controller with power ramp circuitry that allows the board's voltages to be ramped in a controlled fashion. The power ramp circuitry eliminates large voltage or current spikes caused by hot swapping boards. This controlled ramping is a requirement of the *CompactPCI Hot Swap Specification, PICMG 2.1, Version 1.0*.

The ZT 5504's power controller unconditionally resets the board when it detects that the 3.3V, 5V, and 12V supplies are below an acceptable operating limit. Minimum voltage thresholds for the ZT 5504 are: 4.75V (5V supply), 3.0V (3.3V supply), and 10.0V (+12V supply).

Fault current sensing is also provided. If a board fault (short circuit) or over-current condition is detected, the power controller removes power from the ZT 5504's components and the Health LED on the faceplate turns amber. Fault protection activates if the current exceeds the threshold for greater than 50µs. The ZT 5504's fault current limits are shown in the following table.

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Fault Current Limits

Power Source	Minimum	Maximum
+5.0V	10.0A	15.0A
+3.3V	9.4A	14.1A
+12V	1.0A	1.5A
-12V	0.6A	0.9A

Notes:

- The fault trip currents listed above are design values. Noisy power sources can lower the fault trip current limits to less than the minimum design values.
- Over-current on the -12V supply does not activate the fault trip circuit breaker and the LED will not turn amber. -12V is over-current protected by a resettable (PTC) 0.75A fuse.

Rear-Panel I/O

The following I/O signals are available from the J5 connector at the back of the ZT 5504. These signals are available for use by a rear panel transition board such as the ZT 4807.

- Serial ports (COM1 and COM2)
- USB Ports 0 and 1 (through cuttable trace configuration)
- Floppy Interface
- Keyboard
- PS/2 mouse
- Push button reset input
- IDE secondary channel
- SMBus
- Ejector
- Video
- Speaker Output (AT compatible)

PCI Video

The ZT 5504 provides on-board video using the Chips and Technologies 69000 HiQVideo Accelerator with Integrated Memory. This device is configured for PCI bus transactions at speeds up to 33 MHz.

The 69000 incorporates 2 MB of integrated SDRAM for the graphics/video frame buffer. The integrated SDRAM memory can support up to 83 MHz operation, thus increasing the available

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memory bandwidth for the graphics subsystem. Video signals are available at the ZT 5504's J6 faceplate connector or at the J5 Rear Panel I/O connector. See "SW2-3 (VGA Routing Control)" in Chapter 3 for information on directing video signals to the front or rear of the board.

The "Video" topic in Appendix E contains a link to the datasheet for this device.

PCI Mezzanine Card (PMC) Interface

The ZT 5504 provides a location for one on-board PMC device with front panel access. The PMC interface is on PCI Bus 0 and uses a 32-bit 3.3V PCI bus.

The "PMC Specification" topic in Appendix E contains a link to the sponsoring organization for the PMC specification.

Dual Ethernet Interfaces

The ZT 5504 provides two 10/100BaseTx Ethernet channels (A and B) through the Intel® 82550 Fast Ethernet Multifunction PCI Controller with integrated Alert On LAN (AOL). The 82550 consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution. Two RJ-45 connectors with integrated LEDs are available at the faceplate. Both Ethernet channels can be directed to the J3 backplane connector. See "Geographic Addressing (E4h)" in Appendix C for more information.

The "Ethernet" topic in Appendix E contains links to the datasheets for the Ethernet devices used on the ZT 5504.

IDE Hard Drive

The ZT 5504 includes an on-board 2.5-inch Enhanced IDE hard drive. The hard drive is on the ZT 5504's primary IDE channel and is assigned "device 0" (master) identity.

See Chapter 6, "IDE Controller", for more information.

Serial I/O

The ZT 5504 provides support for two RS-232 compatible serial ports. COM1 is accessible at the faceplate through an RJ-45 connector or through the J5 Rear Panel I/O connector. This port is typically used for test access. COM2 is accessible only through the J5 Rear Panel I/O connector. No strapping option or software control is required to use either port.

The front panel RJ-45 connector is configured as DTE. SRI (Serial Ring Indicator) and SCD (Serial Carrier Detect) signals are not included in the front panel RJ-45 connector. Refer to the "J10 (COM1 Serial Port)" topic in Appendix A for a connector pinout.



Note: COM1 signals are available to the front- and rear-panel simultaneously. Utilizing the COM1 signal at the front and rear at the same time will cause a signaling conflict.

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The ZT 5504's serial controller resides in the National Semiconductor* PC87309 SuperI/O* device. The "SuperI/O" topic in Appendix E provides a link to the datasheet for this device.

Interrupts

Two enhanced, 8259-style interrupt controllers provide the ZT 5504 with a total of 15 interrupt inputs. Interrupt controller features include support for:

- Level-triggered and edge-triggered inputs
- Individual input masking
- Fixed and rotating priorities

Interrupt sources include:

- Counter/Timers
- Serial I/O
- Keyboard
- Printer Port
- Floppy disk
- IDE interface
- Real-Time Clock
- CompactPCI backplane (21154)
- On-board PCI devices

Enhanced capabilities include the ability to configure each interrupt level for active high-going edge or active low-level inputs.

The ZT 5504's interrupt controllers reside in the Intel® 82371EB (PIIX4E) device. The "Intel 440GX AGPset" topic in Appendix E provides a link to the datasheet for this device.

Counter/Timers

Three 8254-style counter/timers, as defined for the PC/AT, are included on the ZT 5504. Operating modes supported by the counter/timers include:

- Interrupt on count
- Frequency divider
- Square wave generator
- Software triggered
- Hardware triggered
- One shot

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The ZT 5504's Counter/Timers reside in the Intel 82371EB (PIIX4E) device. The "Intel 440GX AGPset" topic in Appendix E provides a link to the datasheet for this device.

DMA

Two enhanced, 8237-style DMA controllers are provided on the ZT 5504 for use by the on-board peripherals.

The ZT 5504's DMA controllers reside in the Intel 82371EB (PIIX4E) device. The "Intel 440GX AGPset" topic in Appendix E provides a link to the datasheet for this device.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 256 bytes of general-purpose, battery-backed, CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. The system BIOS uses a portion of this RAM for BIOS setup information.

The ZT 5504's Real-Time Clock resides in the Intel 82371EB (PIIX4E) device. The "Intel 440GX AGPset" topic in Appendix E provides a link to the datasheet for this device.

Reset

The push-button reset on the ZT 5504's faceplate functions as a "Hard Reset". See Chapter 4, "Reset," for more information about reset sources for the ZT 5504.

Two-Stage Watchdog Timer

The watchdog timer optionally monitors system operation and is programmable for one of eight different timeout periods (from 0.25 seconds to 256 seconds). It is a two-stage watchdog, meaning that it can be enabled to produce a non-maskable interrupt (NMI) or a "CPU init" before it generates a Reset. Failure to strobe the watchdog timer within the programmed time period may result in an NMI, a reset request, or both. A register bit can be enabled to indicate if the watchdog timer caused the reset event. This watchdog timer register is cleared on power-up, enabling system software to take appropriate action if the watchdog generated the reboot.

See Chapter 7, "Watchdog Timer," for more information, including sample code.

Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a common interface to slower-speed peripherals. Functions such as keyboard, serial ports, printer port, and mouse ports can be consolidated into USB, simplifying cabling requirements. The ZT 5504 provides two USB ports at its faceplate (connector J8 is Port 0, J9 is Port 1). USB Port 0 can be routed to the ZT 5504's J5 Rear Panel I/O connector by reconfiguring CT57 and CT58. USB Port 1 can be routed to the ZT 5504's J5 Rear Panel I/O connector by reconfiguring CT31 and CT32.

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The ZT 5504's USB channels are controlled by the Intel 82371EB (PIIX4E) device. The "Intel 440GX AGPset" topic in Appendix E provides a link to the datasheet for this device.

Baseboard Management Controller

The ZT 5504 includes an Intel Baseboard Management Controller (BMC) chip. The BMC provides SMBus (System Management Bus) interfaces and is IPMI (Intelligent Platform Management Interface) compliant. The BMC subsystem monitors, controls, and performs remote diagnostics for on- and off-board functions.

IDE Controller

The ZT 5504 features an ATA-33 IDE controller that supports onboard external IDE drives. ATA-33, also called Ultra-DMA and DMA-33, is an enhancement to earlier IDE standards that increases throughput to 33 MBps.

Primary channel IDE signals are available through the J14 IDE connector. Secondary channel IDE signals are available through the J5 Rear Panel I/O connector. See Chapter 6, "IDE Controller," for more information on the ZT 5504's IDE controller.

The ZT 5504's IDE controller resides in the Intel 82371EB (PIIX4E) device. The "Intel 440GX AGPset" topic in Appendix E provides a link to the datasheet for this device.

Floppy Disk Controller

The ZT 5504 includes a 2.88 MB Super I/O Floppy Disk Controller that supports an optional external floppy drive. Floppy signals are available through the J5 Rear Panel I/O connector.

The "SuperI/O" topic in Appendix E provides a link to the datasheet for ZT 5504's I/O controller.

Keyboard and Mouse Controller

The ZT 5504 includes an on-board PC/AT keyboard controller. The ZT 5504 also includes an on-board PS/2-style mouse controller. Keyboard and mouse signals are available through the J5 Rear Panel I/O connector.

The "SuperI/O" topic in Appendix E provides a link to the datasheet for ZT 5504's I/O controller.

LED Indicators

The LEDs located at the ZT 5504's faceplate are defined below.

- Ethernet (in the ENETA and ENETB RJ 45 connectors):

  Green = network connection

  Yellow = network activity

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- IDE Activity (Disk 0)

  Green = disk activity

- Hot Swap

  Blue = safe to extract board

  Off = not safe to extract board

- Health

  Green = normal operation

  Amber = needs attention

Software

The ZT 5504 includes the Intel® NetStructure™ Embedded BIOS v5.x loaded in on-board flash. The BIOS is user-configurable to boot an operating system from local flash memory, a hard drive, CD-ROM drive, or over a network. BIOS and firmware updates can be downloaded from the Intel Website.

The ZT 5504 is compatible with all major PC operating systems, including Microsoft Windows 2000, Linux, and VxWorks. Intel may provide additional drivers for Intel peripherals, flash drives, and for supported operating systems. Software device drivers for the ZT 5504 may be found on the Intel Website.

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2. Getting Started

This chapter summarizes the information needed to make the ZT 5504 operational. This chapter should be read before using the board.

Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Intel for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Intel. Refer to the "Customer Support" section for assistance information.



CAUTION: This board must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a wrist strap grounded through one of the system's ESD Ground jacks when servicing system components.

System Requirements

The following topics briefly describe the basic system requirements and configurable features of the ZT 5504. Links are provided to other chapters and appendices containing more detailed information.

BIOS Version

For proper operation, the ZT 5504 must run Intel NetStructure Embedded BIOS v5.x, revision C01 or P01 and later (P01-Pxx). The revision level is shown in the BIOS Identification string displayed during the Power On Self Test (POST). The revision level is the fourth field in the BIOS ID string. The Intel NetStructure Embedded BIOS Manual is available from Intel's Web site.

Connectivity

The ZT 5504 can be installed as a System Master in the System Slot or as a stand-alone computer in a peripheral slot. Refer to the "Drone Mode" topic for more information on using the ZT 5504 as a stand-alone computer.

The ZT 5504 features an ejector handle that is keyed for compatible slots. The board can only be inserted into slots fitted with a compatible mating key.

The ZT 5504 is designed to operate in a backplane providing CompactPCI form factor interfaces at J1, J2, J3, and J5. The J1 and J2 connectors interface with the system's CompactPCI bus. J3 signaling must comply with the PICMG* 2.16 Packet Switching Backplane specification. The J5 interface must have through-pins for the ZT 5504 to interface with a rear panel transition card such as the ZT 4807. See the "Connectors" topic in Appendix A for connector descriptions.

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Electrical and Environmental

The ZT 5504 requires:

- +5VDC +5%, -3% @ 4A typical
- +3.3VDC +5%, -3% @ 6A typical
- +12VDC ±10% @ 20mA typical
- -12VDC may be required by a PMC peripheral installed on the ZT 5504.

Configuration	5V (avg)	5V (peak)	3.3V (avg)	3.3V (peak)	12V (avg)	12V (peak)	-12V (avg)	-12V (peak)
850MHz 512MB	4A	TBD	6A	TBD	20mA	50mA	0.0A	0.0A
Hard disk (add) (typical)	540mA	1.00A	N/A	N/A	N/A	N/A	N/A	N/A
PMC card typical[1] (add)	1.00A	1.70A	0.75A	1.30A	100mA	200mA	20mA	40mA
PMC card max.[2] (add)	1.50A	3.00A	2.25A	4.50A	500mA	500mA	500mA	500mA

Notes:
1. Consult manufacturer of installed PMC card for actual values.
2. In no case shall the total power dissipated by the PMC card exceed 10.0 W.

The ZT 5504 requires 5V V(I/O) to operate as a system master. It supports either 3.3V or 5V V(I/O) in drone mode. It will not correctly terminate the PCI bus if used in a system slot configured for 3.3V V(I/O). For this reason, Intel ships the ZT 5504 with a blue key in CompactPCI connector J1, which prevents the ZT 5504 from being installed in any slot configured for 3.3V V(I/O).

For the ZT 5504 to be used in drone mode in a peripheral or non-bused slot configured for 3.3V V(I/O), the key must be removed from J1. The ZT 5504 with the key removed can be used without damage in a system slot configured for 3.3V V(I/O), but the PCI bus will not operate correctly. The following table shows ZT 5504 V(I/O) functionality:

Mode	V(I/O)	Blue Key
System Slot – PCI bus in use	5V	Installed
System Slot – PCI bus not in use	3.3V	Removed
	5V	Installed
Peripheral Slot – Drone mode	3.3V	Removed
	5V	Installed
Non-Bused Node Slot – Drone mode	3.3V	Removed
	5V	Installed

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The ZT 5504 is supplied with a heatsink allowing the processor to operate between 0° and approximately 50°C ambient with a minimum of 200 LFM (1 meter per second) of external airflow. It is the users' responsibility to ensure that the ZT 5504 is installed in a chassis capable of supplying adequate airflow. The maximum power dissipation of the processor (BGA2 package) is 21W. External airflow **must** be provided at all times. See Appendix A, "Specifications," and Appendix B, "Thermal Considerations," for more details.

It is strongly recommended that the airflow be measured while the ZT 5504 is installed in its intended location. Insert a thermistor type air velocity meter (Kane-May KM4007 or similar) through the PMC access on the faceplate and make the air velocity measurement near the processor heat sink. Power should not be applied to the ZT 5504 during airflow measurements (slightly disengage the ZT 5504 from the backplane connectors if necessary).



CAUTION: The processor "core" temperature must **never** exceed 100°C under any condition of ambient temperature or usage. This may result in permanent damage to the processor.

The ZT 5504 may contain materials that require regulation upon disposal. Please dispose of this product in accordance with local rules and regulations. For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance at http://www.eiae.org/.

Memory Configuration

The ZT 5504 addresses up to 4 GB of memory. The address space is divided between memory local to the board and memory located on the Local PCI (or CompactPCI) bus. Any memory not reserved or occupied by a local memory device (DRAM/flash) is available to PCI memory devices.

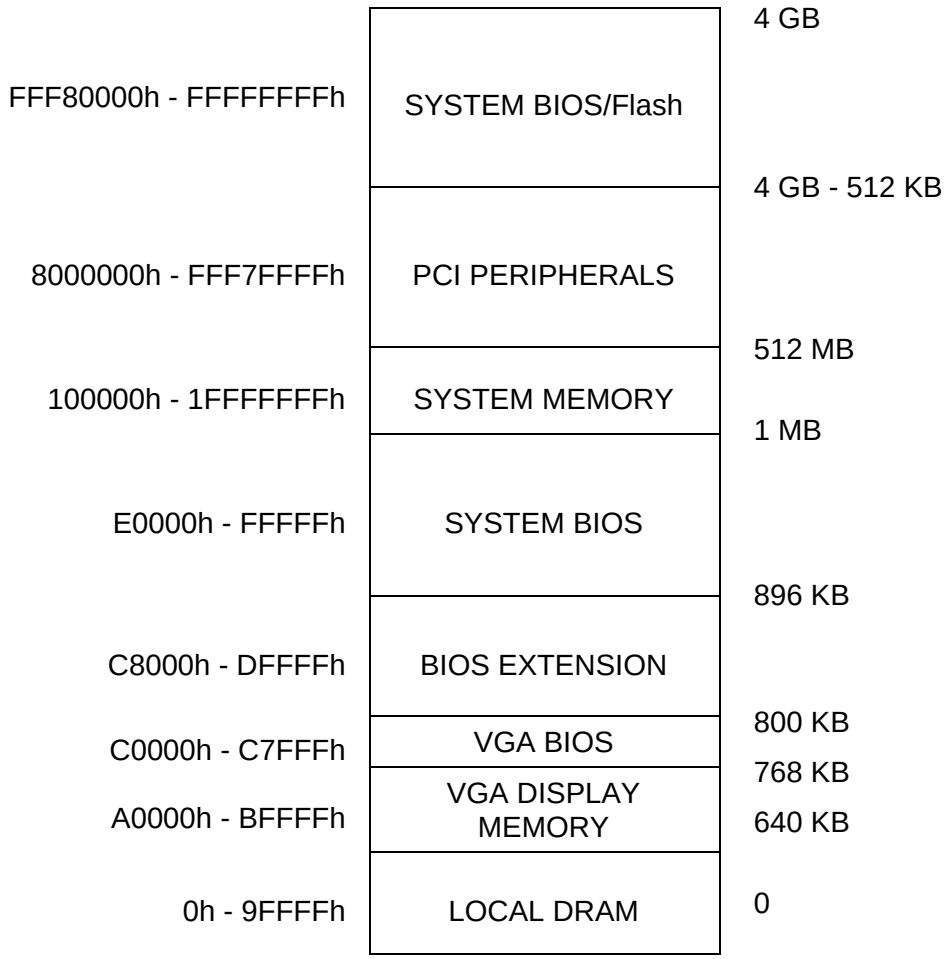
The ZT 5504 includes 512 MB or 1 GB of ECC SDRAM soldered directly onto the board. 256 KB of L2 cache is integrated with the Mobile Pentium III Processor - M.

Local flash memory is soldered directly to the board. The ZT 5504 supports 4 MB of flash memory divided into 512 KB pages.

The "Memory Address Map Example" illustration shows example memory addressing for the ZT 5504.

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Memory Address Map Example



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I/O Address Map

*Onboard ISA peripherals addressed between 100h - 7FFh decode 11 bits of address (A0h - A10h). Therefore, these peripherals will alias throughout the 16-bit I/O space at the following ranges:

- x100-x3FFh
- x500-x7FFh
- x900-xBFFh
- xD00-xFFFh

PCI devices can fully utilize the address space from D00 - FFFFh, since subtractive decoding is used for the onboard ISA devices.

D00 - FFFFh	PCI*
CF8 - CFFh	PCI Config/RST Control
780 - CF7h	PCI Reserved
778 - 77Fh	LPT ECP Registers
400 - 777h	Reserved
3F8 - 3FFh	COM1
3F0 - 3F7h	Floppy / IDE Registers
3E0 - 3EFh	Reserved
3B0 - 3DFh	VGA Registers
380 - 3AFh	Reserved
378 - 37Fh	LPT
300 - 377h	Reserved
2F8 - 2FFh	COM2
200 - 2F7h	Reserved
1F8 - 1FFh	Reserved
1F0 - 1F7h	Primary IDE Registers
178 - 1DFh	Reserved
170 - 177h	Secondary IDE Registers
100 - 16Fh	Reserved
F0 - FFh	Coprocessor
E6 - EFh	Reserved
E1 - E5h	ZT 5504 System Registers 1-5
E0Fh	Reserved
C0 - DFh	On-board Slave DMA Controller
B4 - BFh	Reserved
B2 - B3h	APM Registers
B0 - B1h	Reserved
A0 - AFh	On-board Slave Interrupt Controller
93 - 9Fh	Reserved
92h	Fast RESET and Gate A20
90 - 91h	Reserved
81 - 8Fh	On-board DMA Page Registers
80h	Diagnostic Port
79h	Board's Watchdog Timer Register
78h	Board's System Register 0
70 - 77h	On-board Real-Time Clock
60 - 6Fh	Keyboard and System Ports
50 - 5Fh	Reserved
40 - 4Fh	On-board Timer/Counters
30 - 3Fh	Reserved
2E - 2Fh	87309 Super I/O Configuration
22 - 2Dh	Reserved
20 - 21h	On-board master Interrupt Controller
0 - 1Fh	On-board Master DMA Controller

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I/O Configuration

The ZT 5504 addresses up to 64 KB of I/O using a 16-bit I/O address. The ZT 5504 is populated with many commonly used I/O peripheral devices. The I/O address location for each peripheral is shown in the "I/O Address Map" illustration.

Connectors

The ZT 5504 includes several connectors to interface to application-specific devices. Refer to the "Connectors" topic in Appendix A for complete connector descriptions and pinouts.

Switches and Cuttable Traces

The ZT 5504 provides several switch and cuttable trace configuration options for features that cannot be provided through the BIOS Setup Utility. Location figures and descriptions are provided in Chapter 3, "Configuration."

BIOS Configuration Overview

This topic presents an introduction to the ZT 5504's BIOS. For more detailed information about the BIOS and other utilities, see the *Intel NetStructure Embedded BIOS Manual* available on the Intel Website.

The BIOS has many separately configurable features. These features are selected by running the built-in Setup utility. System configuration settings are saved in a portion of battery-backed RAM in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

To access the Setup utility, press **F2** during the system RAM check at boot-up. When Setup runs, an interactive configuration screen displays. Refer to the following "Setup Screen" illustration for an example.

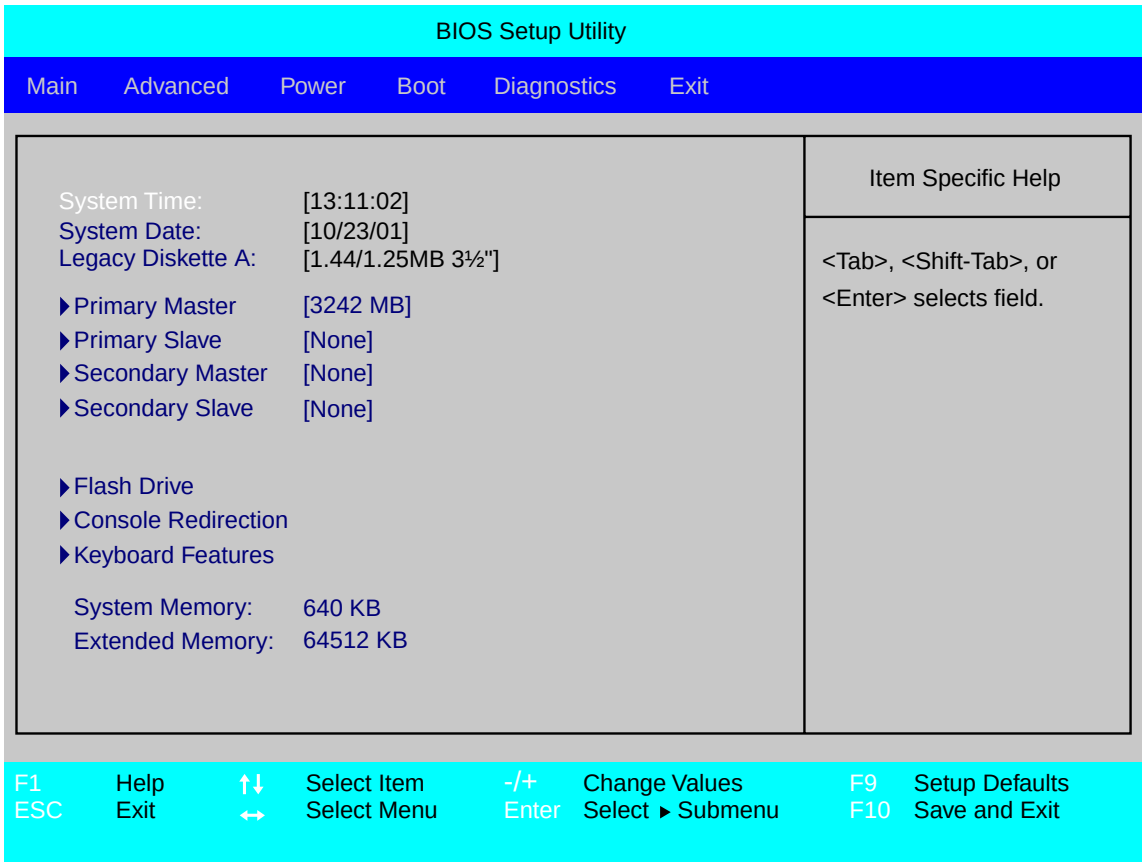
Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the Setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the Setup screen. Context sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the Setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the **+** or **–** keys to change the value of a parameter.

Solid arrows next to menu items in the main screen indicate submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press **Enter**.

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Setup Screen



Operating System Installation

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor.

1. Install peripheral devices. CompactPCI devices are automatically configured by the BIOS during the boot sequence.

2. Most operating systems require initial installation on a hard drive from a floppy or CD-ROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.

3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.

4. Select the appropriate boot device order in the SETUP boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation floppy, select **Removable Media** as the first boot device and reboot the system with the installation floppy installed in the floppy drive. (Note that if the installation requires a non-bootable CD-ROM, it is necessary to boot an OS with the proper CD-ROM drivers in order to access the CD-ROM drive).

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5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of Intel products.

6. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu appropriately.

7. The Flash Write Protect/Write Enable switch, SW3-2, must be open when installing an operating system image into flash. See "SW3-2 (Flash Write Protect)" in Chapter 3 for more information.

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3. Configuration

The ZT 5504 has been designed for maximum flexibility. Many features can be configured by the user for specific applications. Most configuration options are selected through the BIOS Setup utility (discussed in the "BIOS Configuration Overview" topic in Chapter 2). Some options cannot be software controlled and are configured with switches or cuttable traces. Switch options are made by closing or opening the appropriate switch. Cuttable trace options are made by installing or removing surface mount zero Ω resistors.

Switch Options and Locations

The ZT 5504 contains a push-button switch on the faceplate and three banks of DIP switches on the component side of the board. The switches are listed and briefly described in the "Switch Cross-Reference" table below.

Factory default switch settings are shown in the "Default Switch Settings" figure.

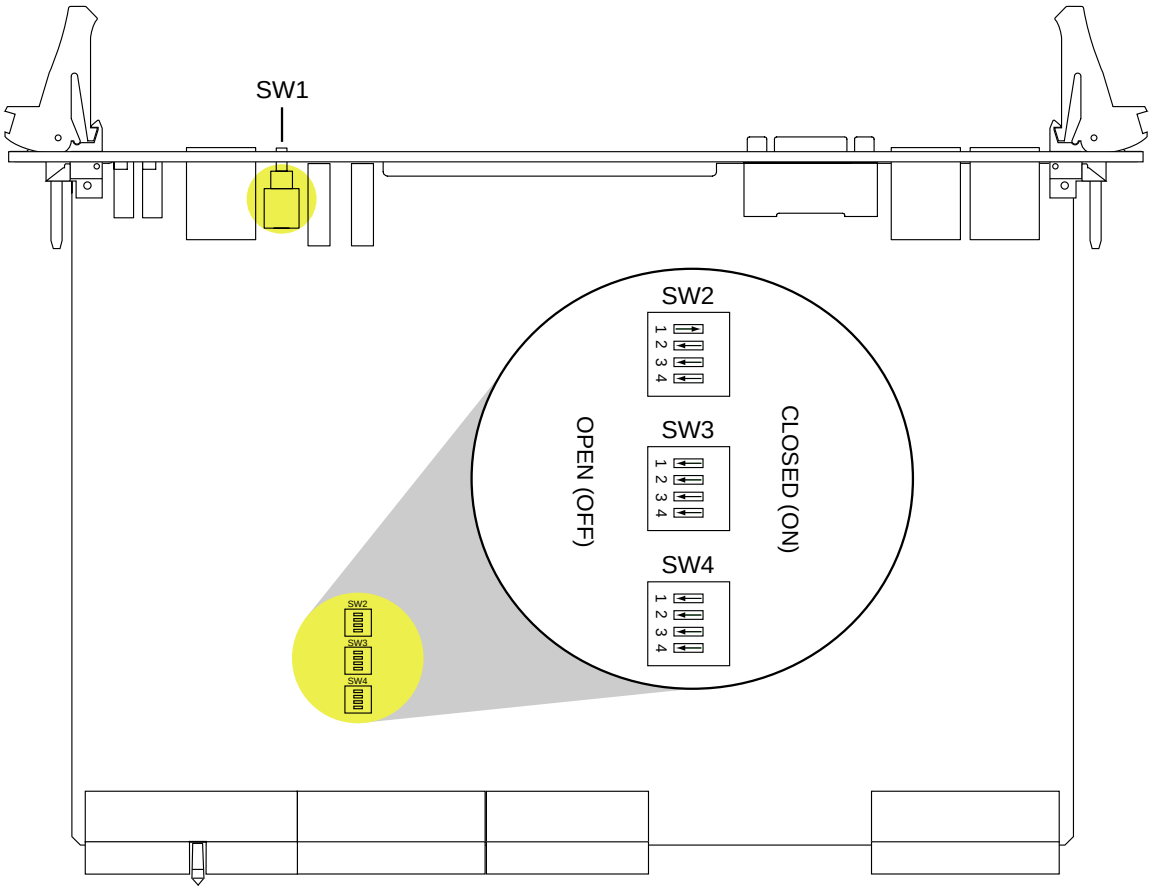
Note: Where switches are referenced in this chapter, "SWx" refers to the switch number and "-N" refers to the switch segment (SW4-2 means "switch number 4, segment 2").

Switch Cross-Reference Table

Switch	Function
SW1	Reset (push-button on faceplate)
SW2-1	Battery-back Real-Time Clock
SW2-2	Clear Real-Time Clock
SW2-3	Enable VGA Routing to Rear Panel
SW2-4	Reserved
SW3-1	BIOS Recovery Module/Flash Select
SW3-2	Flash Write-Protect
SW3-3	IPMI Flash Write Protect
SW3-4	Drone Mode Reset
SW4-1	User Software Configuration 0
SW4-2	User Software Configuration 1
SW4-3	User Software Configuration 2
SW4-4	Console Redirection

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Default Switch Configuration



Switch Descriptions

The following topics list the switches in numerical order and provide a detailed description of each switch.

SW1 (Reset)

SW1 is a push-button on the front of the ZT 5504. Pressing SW1 issues a hard reset. Reset is discussed in more detail in Chapter 4.

SW2-1, SW2-2 (Real-Time Clock Battery Backup)

Use these switch segments to battery back and clear the Real-Time Clock. When closed, SW2-1 connects the Real-Time Clock to the on-board battery. Keep this switch in the closed position for normal operation.

If the Real-Time Clock and CMOS contents need to be cleared, open SW2-1 and close SW2-2. After two seconds, return SW2-2 to the open position and SW2-1 to the closed position. Factory default is SW2-1 closed and SW2-2 open.

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CAUTION: Do not close SW2-1 and SW2-2 at the same time. Doing so will significantly shorten battery life.

SW2-1	SW2-2		CMOS Configuration RAM
Closed	Open	Default	Normal operation - battery backed.
Open	Closed		Clear CMOS (return to default after clearing).

SW2-3 (VGA Routing Control)

This switch controls the routing of VGA signals to either the front or rear of the board. The default switch configuration routes VGA signals to the faceplate video connector.

SW2-3		Function
Open	Default	VGA routed to the J6 video connector on the faceplate.
Closed		VGA routed to the J5 Rear Panel I/O connector.

SW3-1 (BIOS Recovery Module/Flash Select)

Use this switch to boot from the BIOS Recovery Socket (U38). When SW3-1 is open, the BIOS boots from the on-board flash memory. When SW3-1 is closed, the BIOS boots from the BIOS Recovery Socket. Factory default is open. See the "BIOS Recovery Module" topic in Chapter 8 for details on how to flash the BIOS.

SW3-1		Function
Open	Default	Boots from on-board flash memory.
Closed		Boots from the BIOS recovery socket.

SW3-2 (Flash Write-Protect)

Closing this switch write-protects flash memory. Open SW3-2 when installing an operating system image (such as VxWorks) into flash or when using the FLASH.EXE utility to recover from a corrupted BIOS. The status of this switch can be read back at the Switch Monitor register (Port E3h, bit 7). Factory default is open.

SW3-2		Function
Open	Default	Flash disk/BIOS read/write.
Closed		Flash disk/BIOS read only.

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SW3-3 (IPMI Flash Write Protect)

Closing this switch write-protects the IPMI firmware flash memory. Opening the switch allows IPMI firmware updates. This switch must be open when using an update utility.

SW3-3		Function
Open	Default	Flash firmware read/write.
Closed		Flash firmware read only.

SW3-4 (Drone Mode Reset)

Use this switch to configure the ZT 5504 to accept backplane PCI resets when in drone mode. When SW3-4 is closed, the ZT 5504 is reset when the system master CPU issues a PCI reset. When open, the ZT 5504 does not respond to system master PCI resets.

SW3-4		Function
Open	Default	ZT 5504 in Drone Mode does not respond to backplane PCI resets.
Closed		ZT 5504 in Drone Mode responds to backplane PCI resets.

SW4-1, SW4-2, SW4-3 (Software Configuration)

These switch segments provide configuration information to the user's software. The Switch Monitor register (Port E3h Bits 0-3) monitors the status of SW4 segments as listed below. An open switch reads back a 0; a closed switch reads back a 1. The factory default is open. The switch segments correspond to register bits as follows:

SW4-1 = Bit 0; **SW4-2** = Bit 1; **SW4-3** = Bit 2

SW4-4 (Console Redirection)

Console Redirection provides a serial communication link (through COM1 or COM2) between a terminal or terminal emulation program and the ZT 5504. This feature requires specific parameters to be set in the BIOS Setup utility before configuring SW4-4.

SW4-4		Function
Open	Default	Normal Operation.
Closed		Console redirection enabled.

Refer to the "Console Redirection" chapter in the *Intel NetStructure Embedded BIOS Manual* before attempting to use this feature.

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Cuttable Trace Options and Locations

The ZT 5504 contains several cuttable traces (zero Ω shorting resistors) that allow the user to configure certain options not configurable through the BIOS Setup Utility. The "Cuttable Trace Locations" figure shows the placement of the ZT 5504's cuttable traces. The "Cuttable Trace Locations" table provides a quick cross-reference for the cuttable trace descriptions that follow.

There are two types of cuttable traces on the ZT 5504: single-option and double-option. **Single option cuttable traces** are implemented using 0603 surface mount pads. A zero Ω shorting resistor is then soldered between these pads to make the connection. **Double option cuttable traces** (CTx, CTy, CTz) are implemented using three 0603 size surface mount pads. The zero Ω shorting resistor is then soldered between one set of pads, depending on the chosen option.



CAUTION: The ZT 5504 has additional cuttable traces not documented in this manual. These should not be modified by the user. Modifications to documented cuttable traces should only be performed by a qualified technician familiar with surface mount soldering techniques. The product warranty is voided if the board is damaged by customer modifications.

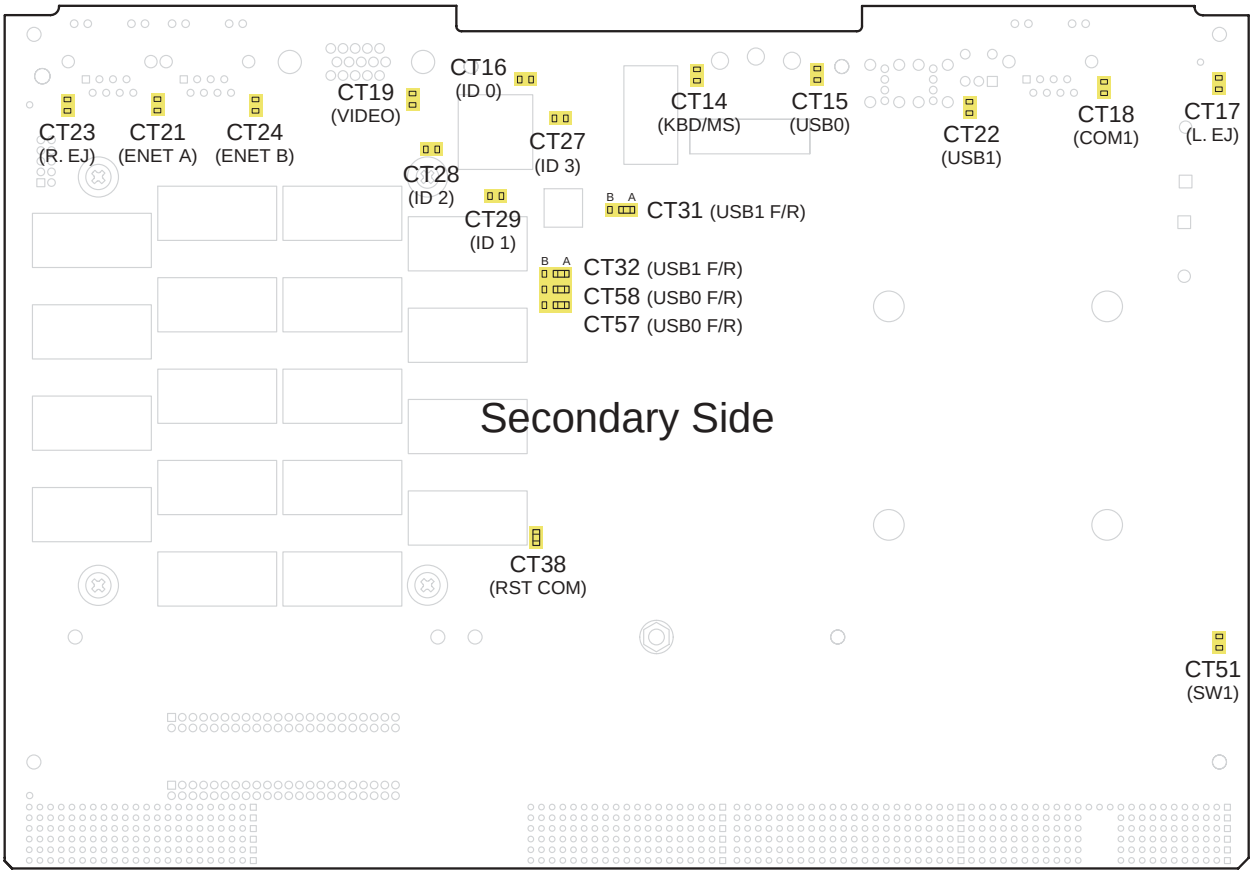
Cuttable Trace Definitions

CT#	Description
CT15	USB0 (J8) chassis GND to logic GND
CT16	Revision ID bit 0
CT17	Left ejector chassis GND to logic GND
CT18	COM1 (J10) chassis GND to logic GND
CT19	VGA (J6) chassis GND to logic GND
CT21	Ethernet A (JA4) chassis GND to logic GND
CT22	USB1 (J9) chassis GND to logic GND
CT23	Right ejector chassis GND to logic GND
CT24	Ethernet B (J17) chassis GND to logic GND
CT27	Revision ID bit 3
CT28	Revision ID bit 2
CT29	Revision ID bit 1
CT31	USB1- front or rear routing
CT32	USB1+ front or rear routing

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CT#	Description
CT38	D_RSTDRV- to COM port driver
CT51	Push-button reset (SW1) chassis GND to logic GND
CT57	USB0- front or rear routing
CT58	USB0+ front or rear routing

Cuttable Trace Locations



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CT14, CT15, CT17-19, CT21-24, and CT51 (Connect Chassis GND to Logic GND)

The ZT 5504's faceplate connectors, push-button reset, and ejectors are on an isolated chassis ground. These components can be connected to the ZT 5504 logic ground by installing the ten cuttable traces listed above. All ten cuttable traces should be installed or all ten should be removed. The factory default is removed.

Position		Function
All Out	Default	Front-panel connectors on an isolated chassis ground.
All In		Front-panel connectors connected to logic ground.

CT16 and CT27-29 (Board Revision)

These cuttable traces are set at the factory to identify the current board revision. The user should not modify them.

CT31 and CT32 (USB1 Front/Rear Routing)

CT31 and CT32 determine the routing for USB channel 1. The A position (default) routes USB1 to J9 at the front panel. The B position routes USB1 to Rear Panel I/O connector J5. The same position (A or B) must be used for both cuttable traces.

Position		Function
CT31A, CT32A	Default	USB1 routed to the front panel connector J9.
CT31B, CT32B		USB1 routed to the Rear Panel I/O connector J5.

CT57 and CT58 (USB0 Front/Rear Routing)

CT57 and CT58 determine the routing for USB channel 0. The A position (default) routes USB0 to J8 at the front panel. The B position routes USB0 to Rear Panel I/O connector J5. The same position (A or B) must be used for both cuttable traces.

Position		Function
CT57A, CT58A	Default	USB0 routed to the front panel connector J8.
CT57B, CT58B		USB0 routed to the Rear Panel I/O connector J5.

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CT38 (D_RSTDRV- to COM Port Driver)

Installing CT38 disables the COM port driver during board reset to prevent glitching of the RS-232 interface as the ZT 5504 comes out of reset. The factory default installs CT36.

CT38		Function
In	Default	Disable RS-232 driver during board reset.
Out		Enable RS-232 driver during board reset.

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4. Reset

This chapter discusses the reset types and reset sources on the ZT 5504. If necessary, the ZT 5504's board reset characteristics can be tailored to the requirements of a specific system.

Reset Types and Sources

The ZT 5504's reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Hard Reset:** All devices are held in reset.
- **Soft Reset:** CPU initialization only. Other devices are not reset.
- **Backend Power Down:** The backend logic is powered off. The board is powered on and is held in reset.
- **NMI:** Non-maskable interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

Hard Reset Sources

Faceplate Reset Push-button (SW-1)

Press push-button SW-1 on the ZT 5504's faceplate to issue a system reset.

System Register CF9h (PIIX4E Reset Control Register)

Bits 1 and 2 in this register are used by the PIIX4E to generate a hard reset or a soft reset. During a hard reset, the PIIX4E asserts CPURST, PCIRST#, and RSTDRV, and resets its core and suspend well logic.

Soft Reset Sources

System Register CF9h (PIIX4E Reset Control Register)

Bits 1 and 2 in this register are used by the PIIX4E to generate a hard reset or a soft reset. During a soft reset, the PIIX4E asserts INIT to the CPU. This causes the processor to enter "real mode", initialize its internal registers, and begin instruction execution from FFFFFFF0h (the boot vector).

Keyboard Controller Reset

The keyboard controller generates a keyboard controller reset when FEh is written to port 64h. This causes the PIIX4E to assert INIT to the CPU.

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Keyboard CTRL-ALT-DEL

Simultaneously pressing these keys calls a BIOS function that reboots the system. This method does not work under operating systems that trap calls to this BIOS function.

Watchdog Timer (System Register Address 79h)

The watchdog timer may be programmed to generate a "CPU Init" if it is not strobed within a given time-out period. This function is discussed in Chapter 7, "Watchdog Timer."

Backend Power Down Sources

Board Extraction

When a board is extracted from an enclosure (specifically, when the "board-select" pin is disengaged), the hot swap controller unconditionally removes backend power from the board and holds the board in reset.

Low Voltage

When any of the 3.3V, 5V, or 12V supply voltages are detected to be below an acceptable operating limit, the hot swap controller unconditionally removes backend power and holds the board in reset.

Overcurrent Fault

If a power fault condition (overcurrent) is detected, the hot swap controller removes backend power and turns the Health LED amber. The board is held in reset.

NMI Sources

Watchdog Timer (System Register Address 79h)

The watchdog timer may be programmed to generate a non-maskable interrupt if it is not strobed within a given time-out period. This function is discussed in Chapter 7, "Watchdog Timer."

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5. System Monitoring and Control

The ZT 5504 performs system control and monitoring functions using an Intel Baseboard Management Controller (BMC) ASIC. The BMC has the following features.

- IPMB_PWR delivers 5VDC (1A/pin) to the BMC; other required voltages are derived from this.
- Power ramping controls inrush current and avoids glitching the IPMB power rail.
- On power-up, the BMC is held in reset until power is stable.
- A 1024K x 8 flash device and a 32K x 8 SRAM device are used for code and data storage.
- Six IPMI-compliant Interfaces are available.

Monitoring and Control Functions

The BMC tracks the heartbeat of the Host CPU by monitoring several parameters on the ZT 5504. Most of these parameters are measured by the Analog Devices, ADM1026, System Monitoring Device. Monitoring and control functions are listed below.

Monitoring Functions

- Onboard Power Supplies, +3.3, +5, +12, and –12V supplies.
- VTT Supply
- CPU Core Supply
- Onboard and CPU Temperatures
- CPU VID Lines
- Eject signals from front- and rear-panel
- Global Addressing Bits GA[0:4]
- SIO Low Frequency Clock (Real Time Clock Monitoring Frequency from SIO)
- Power Ok
- Hot swap controller fault condition
- Back end Power Fail and Power Degrade signals
- SMBUS Alert signals
- PCI_PRESENT#, SYSSLOT#, BDSEL# for dual domain mode support

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Control Functions

- CPU board Reset Control
- CPU board power on/power off control
- CPU NMI Assertion to processor
- Dual Domain Mode (TBD)

BMC LED Control

The BMC controls the following status LED pins:

LED0	FP_BMC_BLUE_LED-
LED1	RP_BLUE_LED-
LED2	Health LED (normal - green)
LED3	Health LED (needs attention - amber)
LED4	Not used
LED5	Not used

Field Replaceable Unit Information

The BMC controller monitors Field Replaceable Unit (FRU) information for the ZT 5504 and a rear panel I/O board (if present). Each device has its own address.

System Event Log Information

The BMC controller stores system event information in an 8K x 8 serial EEPROM device. Both the in-band KCS interface and the out-of-band IPMB interface provide access to the System Event Log (SEL). This allows SEL information to be accessed through the IPMB interface even if the system is down.

SMBus Address Map

The table below lists the location, function, and address of each SMBus device used on the ZT 5504.

Device	ZT 5504 Function	Address
ADM1026	CPU voltage and temperature monitoring	0101 110
Ethernet A	Ethernet controller A	0101 100

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Device	ZT 5504 Function	Address
Ethernet B	Ethernet controller B	0101 101
FRU	Field Replaceable Unit SEEPROM	1010 010
SEL	System Event Log SEEPROM	1010 011
SDRAM Banks (1 and 2)	Signal Presence Detect (SPD) PROM in Bank #1	1010 000
	Signal Presence Detect (SPD) PROM in Bank #2	1010 001
CY2310NZ	Clock generator	1101 001

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6. IDE Controller

The ZT 5504's IDE controller provides two IDE channels for interfacing with up to four IDE devices. The IDE controller is incorporated into the Intel PIIX4E (82371EB) device, which uses the Peripheral Component Interconnect (PCI) bus to provide exceptional IDE performance. The IDE controller can sustain a maximum transfer rate of 33 Mbps between the IDE drive buffer and the PCI bus.

The "Intel 440GX AGPset" topic in Appendix E provides a link to the PIIX4E datasheet.

Features of the IDE Controller

- Primary and Secondary channels for interfacing up to four devices
- IBM-AT compatible
- Supports PIO and Bus Master IDE
- "Ultra DMA/33" Synchronous DMA Operation
- Bus Master IDE transfers up to 33 MB/sec.
- Individual software control for each IDE channel
- 32-bit, 33 MHz, high performance PCI bus interface

Disk Drive Support

The ZT 5504 supports internal and external IDE devices. These configurations are described below.

Primary IDE Channel

The ZT 5504's primary IDE channel is directed to the J14 IDE connector. J14 is used to interface with the locally mounted hard drive and with an optional IDE device, such as a CD-ROM drive, installed elsewhere in the system.

Secondary IDE Channel

The ZT 5504's Secondary IDE channel is directed via the J5 rear-panel I/O connector to a compatible rear panel I/O board. Rear Panel I/O boards, such as the ZT 4807, can be installed in-line behind the ZT 5504 to provide expanded I/O capability. Refer to the *Intel NetStructure ZT 4807 Packet Switched Rear-Panel Transition Board Hardware Manual* for product information.

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I/O Mapping

The I/O map for the IDE interface varies depending on the mode of operation. The default mode is "compatibility mode," meaning that the interface uses the PC-AT legacy addresses of 1F0h-1F7h, with 3F6h and interrupt IRQ14 for the primary channel. The secondary channel uses I/O addresses 170h-177h, 376h and interrupt IRQ15. No memory addresses are used.

CompactFlash Carrier

Intel provides an optional IDE CompactFlash Carrier (ZT 96080) that can be mounted in the hard drive location on the ZT 5504. This carrier accommodates multiple types of CompactFlash cards, which appear to the system as a hard drive, and are automatically supported by most operating systems. For more information about the ZT 96080 CompactFlash Carrier, see the Intel NetStructure building blocks page at:

http://developer.intel.com/design/network/products/cbp/linecard.htm

Device Drivers

The IDE interface works with all applications by default. To fully utilize the IDE interface, additional software drivers may be installed. Contact the vendor of your intended operating system to receive the latest drivers for the Intel PIIX4E (82371EB) EIDE interface.

Note: If problems are encountered installing the QNX operating system, ver. 4.24, on a CompactFlash card, restart the install program and specify regular IDE drivers (Fsys.ide) instead of the default EIDE drivers (Fsys.eide).

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7. Watchdog Timer

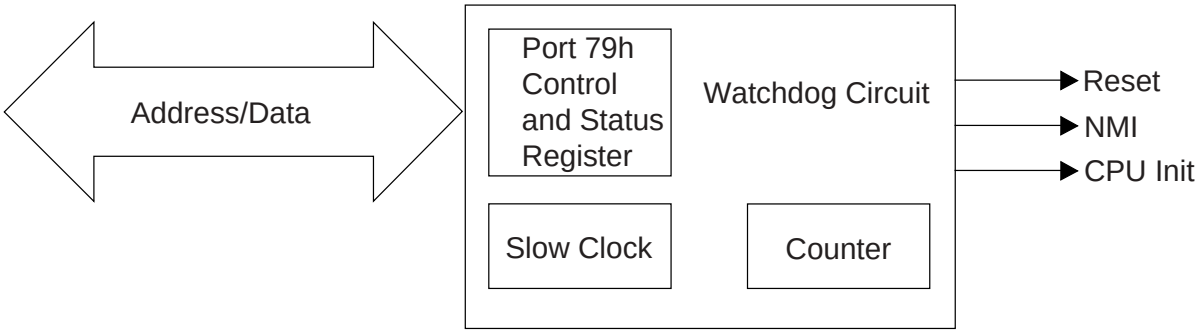
This chapter explains the operation of the ZT 5504's watchdog timer. It provides an overview of watchdog operation and features, as well as sample code to help you learn how the watchdog timer works with applications.

Watchdog Timer Overview

The primary function of the watchdog timer is to monitor the ZT 5504's operation and take corrective action if the software fails to function as programmed. The major features of the watchdog timer are:

- Two-stage operation
- Enabled and disabled through software control
- Armed and strobed through software control

Watchdog Timer Architecture



The ZT 5504's custom watchdog timer circuit is implemented in a programmable logic device. The watchdog timer contains a "Control and Status Register" which is documented in Appendix C as Watchdog (79h). The register allows applications to determine if a watchdog timeout caused a particular reset.

The watchdog timer drives the First and Second Stages as follows:

1. The watchdog times out (First Stage) after a selected timeout interval.
2. NMI or INIT (software selectable) is driven high.
3. A hard reset occurs (Second Stage) 250 ms later.

Eight timeout intervals are selectable through bits 0-2 of the register. The intervals range from a minimum of 250 ms to a maximum of 256 seconds.

The watchdog is normally strobed by reading the Watchdog Register (79h), which clears the counter. Writes to this register also clear the counter.

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Power Up Initialization

The watchdog timer's logic is initialized at power up. This ensures that the STAGE1 MONITOR, STAGE2 MONITOR, STAGE1 ENABLE, and STAGE2 ENABLE status and control bits power up to unasserted states (0). This allows an application to determine if the reset was caused by a watchdog timeout or a power up.

Timeout Values

The watchdog timer has a separate slow clock source that runs at a maximum frequency of 32 Hz (25 Hz nominal). Because the clock is based on an RC oscillator, the nominal timeout period is approximately 30% longer than the minimum value. The watchdog is guaranteed to timeout in no less than the programmed minimum value.

Using the Watchdog in an Application

The following topics are provided to aid you in learning to use watchdog in an application. The watchdog's Reset and NMI functions are described and sample code is provided.

Watchdog Reset and NMI are controlled through the watchdog's "Control and Status Register", documented in Appendix C as Watchdog (79h).

Watchdog Reset

An application using the reset feature enables the watchdog reset, sets the terminal count period, and then periodically strobes the watchdog to keep it from resetting the system. If a strobe is missed, the watchdog times out and resets the system hardware.

Enabling the Watchdog Reset

C code for enabling the watchdog reset might look like the following:

```
#define WD_RESET_EN_BIT_SET      0x20


void EnableWatchdogReset(void){
   unsigned char WdValue;              // Holds watchdog register values.
                                       //
   WdValue = inb(WD_CSR_IO_ADDRESS);   // Read the current contents of the
                                       // watchdog register.
   WdValue |= WD_RESET_EN_BIT_SET;     // Assert the enable bit in the
                                       // local copy.
   outb(WD_CSR_IO_ADDRESS,WdValue);    // Assert the enable in the
                                       // watchdog register.
}
```


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Setting the Terminal Count

The terminal count determines how long the watchdog waits for a strobe before resetting the hardware. C code for setting the terminal count might look like the following:

```
#define WD_CSR_IO_ADDRESS  0x79  // IO address of the watchdog
#define WD_T_COUNT_MASK    0x07  // Bit mask for terminal count bits.
#define WD_500MS_T_COUNT   0x01  // Terminal count values . . . .
#define WD_1S_T_COUNT      0x00  //
#define WD_250MS_T_COUNT   0x00  //
.
.
.
void SetTerminalCount(void){
      unsigned char WdValue;              // Holds watchdog register values.
                                          //
      WdValue = inb(WD_CSR_IO_ADDRESS);   // Get the current contents of the
                                          // watchdog register.
      WdValue &= ~ WD_T_COUNT_MASK;       // Mask out the terminal count bits.
      WdValue |= WD_500MS_T_COUNT;        // Set the desired terminal count.
      outb(WD_CSR_IO_ADDRESS,WdValue);    // Furnish the watchdog register
                                          // with the new count value.
}
```

Strobing the Watchdog

Once the watchdog is enabled, it must be periodically strobed within the terminal count period to avoid resetting the system hardware. C code to strobe the watchdog might look like the following:

```
void StrobeWatchdog(void){
      inb(WD_CSR_IO_ADDRESS);             // A single read is all it takes.
}
```

Watchdog NMI

When enabled, an NMI precedes a watchdog reset by 250 ms. The NMI generation feature gives the application 250 ms to perform essential tasks before the hardware is reset. Before using watchdog NMI, ensure the following:

- The essential task code is included in an interrupt service routine (ISR).
- The ISR is chained to the existing NMI ISR.
- The watchdog NMI is enabled.

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Chaining the ISRs

Save the original NMI ISR vector so that it can be invoked from the new watchdog NMI ISR. Alter the interrupt vector table so that the NMI ISR vector is overwritten with a vector to the watchdog ISR. C code to do this in DOS might look like the following:

```
#define NMI_INTERRUPT_VECTOR_NUMBER 2


void interrupt far (*OldNmiIsr)();


void HookWatchdogIsr(void){


      //
      // To be absolutely certain the interrupt table is not accessed by an
      // NMI (this is quite unlikely), the application could disable NMI in
      // the chip set before installing the new vector.
      //
                  .
                  .
                  .
      //
      // Install the new ISR.
      //
      oldNmiIsr = getvect(IsrVector);  // Save the old vector.
      setvect(NMI_INTERRUPT_VECTOR_NUMBER, WatchdogIsr); // Install the new.
}
```

Enabling the Watchdog NMI

To activate the NMI feature, enable it in the watchdog register (Port 79h). The code to do this might look like the following:

```
#define WD_NMI_EN_BIT_SET  0x10
void EnableWatchdogNmi(void){
      unsigned char WdValue;              // Holds watchdog register values.
                                          //
      WdValue = inb(WD_CSR_IO_ADDRESS);   // Read the current contents of the
                                          // watchdog register.
      WdValue |= WD_NMI_EN_BIT_SET;       // Assert the enable bit in the
                                          // local copy.
      outb(WD_CSR_IO_ADDRESS,WdValue);    // Assert the enable in the watchdog
                                          // register.
}
```


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NMI Handler

Because an NMI may originate from a source such as a RAM Error Correction Code (ECC) error, the NMI handler cannot assume that an NMI occurred due to a watchdog timeout. Therefore, the NMI handler must check the watchdog status register before taking watchdog-related emergency action. When the NMI handler completes handling the emergency, it invokes the original NMI Handler (discussed above). The code to do this might look like the following:

```
#define WD_NMI_DETECT_BIT_SET       0x40    // Bit indicates an NMI occurred, set.
                                            //
void WatchdogIsr(void){                     //
                                            //
                                            //
                                            // Did the watchdog cause the NMI?
                                            //
    if(inb(WD_CSR_IO_ADDRESS) & WD_NMI_DETECT_BIT_SET){
                                            //
            TripAlarm();                    // Take care of essential tasks.
                                            //
            TurnOffTheGas();                //
    }                                       //
    _chain_intr(OldNmiIsr);                 // Invoke the originally installed ISR.
}
```


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8. BIOS Recovery

The ZT 5504 implements two non-volatile memory devices. These devices are listed below and described in the following topics.

- **Flash:** 4 MB Flash Memory device
- **BIOS Recovery Module:** 512 KB EPROM Memory device

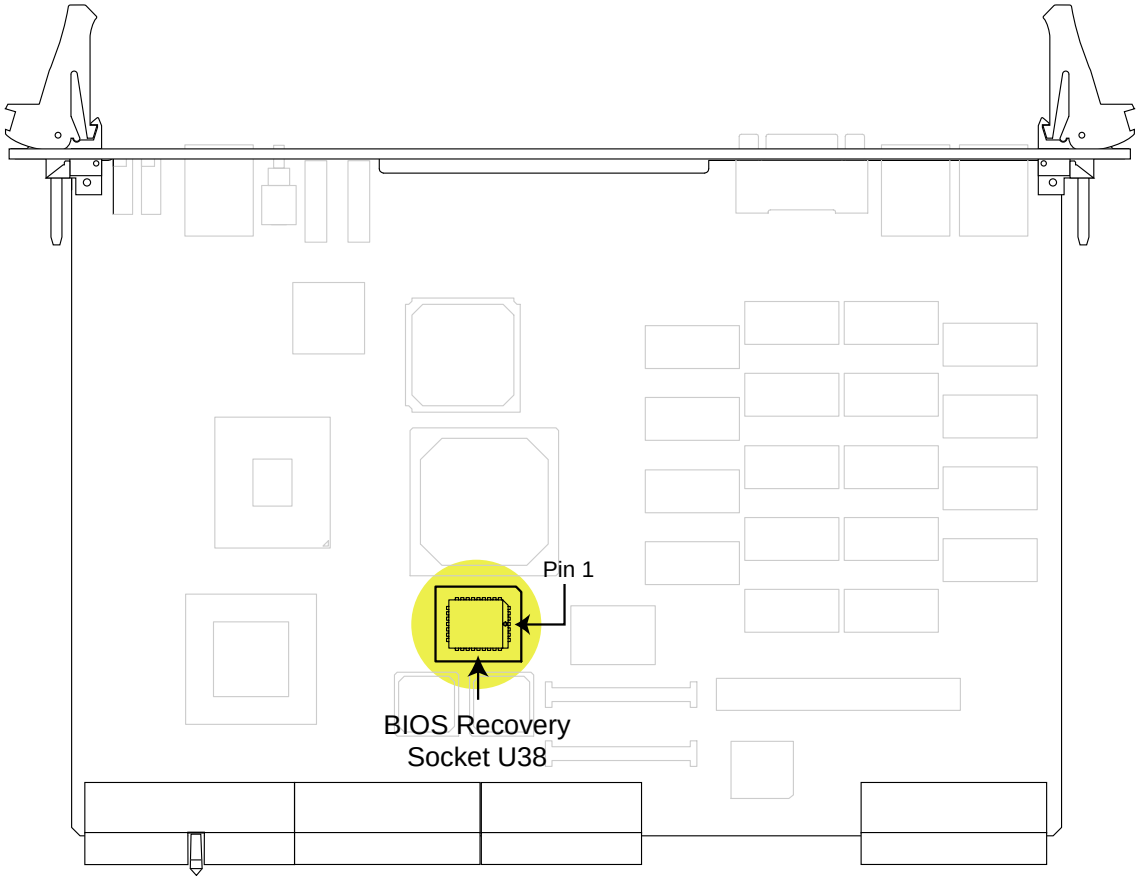
Flash

The ZT 5504 provides 4 MB of on-board flash memory containing the system BIOS.

The flash device is divided into 8 pages mapped into a window in extended memory (FFF80000h – FFFFFFFFh). The BIOS occupies 512 KB in flash page 0. To reprogram the BIOS or update it if it becomes corrupted, use the BIOS Recovery Module and FLASH.EXE utility available from Intel and discussed later in this chapter.

The flash memory is write-protected through switch SW3-2.

BIOS Recovery Socket Location



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BIOS Recovery Module

The ZT 5504 provides a 512 KB EPROM programmed with the BIOS for use if the ZT 5504's BIOS becomes corrupted. The board is shipped with the device pre-installed in a 32-pin socket (U38). If the EPROM is removed for any reason, ensure that it is correctly oriented when reinstalled, as shown in the "BIOS Recovery Socket Location" figure above. The BIOS recovery EPROM must be installed for the ZT 5504 to boot (if SW3-1 is closed).

Should the BIOS image in flash memory become corrupted the ZT 5504 may fail to boot. If this happens, follow the steps below to force a boot from the BIOS Recovery Module. Note that the BIOS contained in the recovery module is the default configuration whereas the BIOS in flash memory may have been modified.

To force a boot from the BIOS Recovery Module:

1. Remove the board from the enclosure.
2. Close switch SW3-1.
3. Make sure flash write protection is disabled (SW3-2 = open).
4. Re-insert the board in the enclosure and power on the board. The system should boot.
5. See the "Flash Utility Program" topic below for detailed instructions on reprogramming the on-board flash with the BIOS.
6. After flashing the BIOS, turn off power, remove the board from the enclosure, and open switch SW3-1.
7. If desired, enable flash write protection by closing switch SW3-2.
8. Re-insert the board in the enclosure.

Flash Utility Program

FLASH.EXE is a utility program that comes with the Intel Development Toolkit. Run FLASH.EXE to modify the BIOS in the on-board flash memory. FLASH.EXE eliminates the need for a PROM programmer and for removing boards and chips from the system.

Before attempting to program the flash, make sure that switch SW3-2 (Flash Write Protect) is open.

To reprogram the BIOS on the ZT 5504, use the following syntax at a DOS prompt:

FLASH /b BIOS.XXX

where BIOS.XXX is the BIOS image for the ZT 5504. See the *Intel NetStructure Embedded BIOS Manual* for more information on the flash utility.

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A. Specifications

This appendix describes the electrical, environmental, and mechanical specifications of the ZT 5504. It includes connector descriptions and pinouts, as well as illustrations of the board dimensions and connector locations.

Electrical and Environmental

The topics listed below provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the ZT 5504 at these maximums. See the "DC Operating Characteristics" section in this appendix for operating conditions.

Supply Voltage, Vcc:	6.5V
Supply Voltage, Vcc3:	4.5V
Supply Voltage, AUX +:	15V
Supply Voltage, AUX -:	-15V
Storage Temperature (no hard disk):	-40° to +85° Celsius
Storage Temperature (with hard disk):	-40° to +65° Celsius
Non-Condensing Relative Humidity:	<95% at 40° Celsius

DC Operating Characteristics

Supply Voltage, Vcc:	4.85 minimum to 5.25V maximum
Supply Voltage, Vcc3:	3.20 minimum to 3.47V maximum
Supply Voltage, AUX +:	10.8 minimum to 13.2V maximum
Supply Voltage, AUX -:	-13.2 minimum to -10.8V maximum

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Supply Current, Icc:	4A average (typical with 850 MHz processor and 512 MB SDRAM. Peak (short duration) power supply current may be significantly higher (up to 50%) and will vary depending upon the application.
Supply Current, Icc3:	6A average (typical with 850 MHz processor and 512 MB SDRAM. Peak (short duration) power supply current may be significantly higher (up to 50%) and will vary depending upon the application.
Supply Current, AUX + (12V):	50mA maximum

Battery Backup Characteristics

Battery Voltage:	3V
Battery Capacity:	250mAh
Real-Time Clock Requirements:	8µA maximum (Vbat = 3V, Vcc=0V)
Real-Time Clock Data Retention:	31,250 hours / 3.7 years minimum (not powered); 5.2 years minimum (with Vcc power applied 8 hours per day)
Electrochemical Construction:	Long life lithium with solid-state polycarbon monofluoride cathode.



CAUTION: The ZT 5504 contains a lithium battery. This battery is not field-replaceable. There is a danger of explosion if the battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the board to Intel for battery service.

Operating Temperature

The ZT 5504's heatsink allows a maximum ambient air temperature of 50°C with 200 LFM (linear feet per minute) of airflow. External airflow **must** be provided to the ZT 5504 at all times. Refer to the "Electrical and Environmental" topic in Chapter 2 for additional information. Also refer to the topic "Temperature Monitoring" in Appendix B, "Thermal Considerations", for details on monitoring the processor temperature.

Reliability

MTBF: 14.6 years (excluding on-board hard disk drive)

MTTR: 3 minutes (based on board replacement), plus system startup

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Mechanical

This section includes the following mechanical specifications:

- Dimensions and weight
- Connector locations, descriptions, and pinouts

Board Dimensions and Weight

The ZT 5504 meets the *CompactPCI Specification, PICMG 2.0, Version 2.1* for all mechanical parameters. In a CompactPCI enclosure with 0.8 inch spacing.

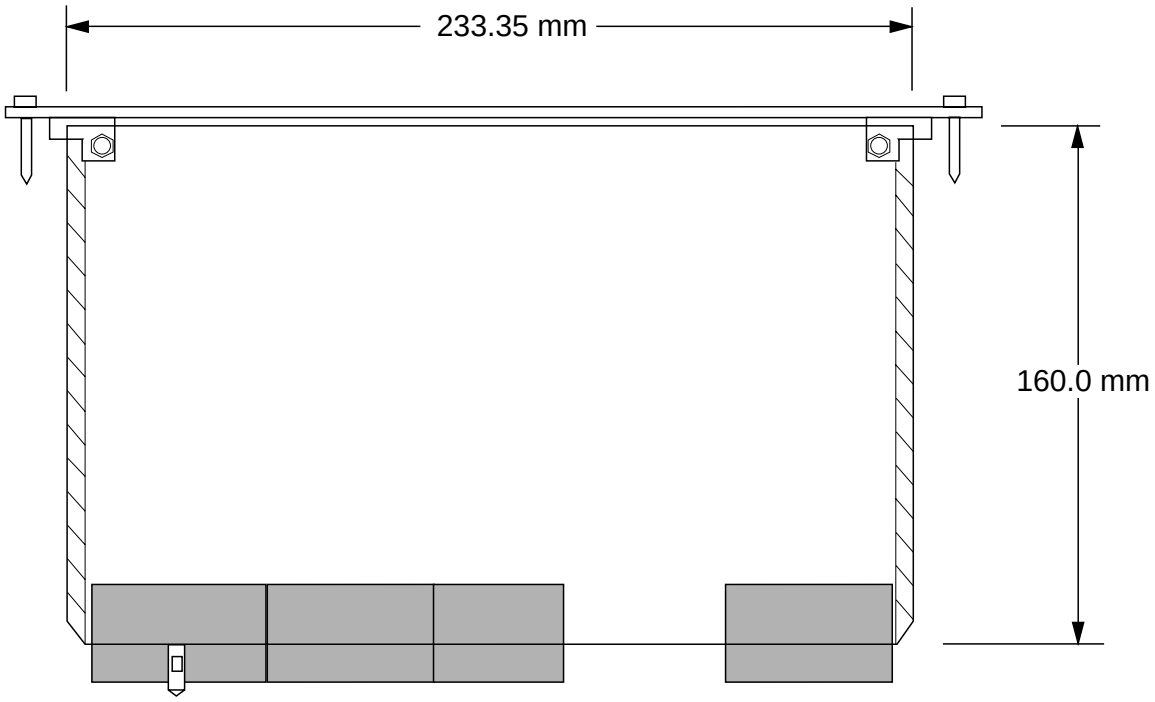
Mechanical dimensions are shown in the "PCB Dimensions" illustration and are outlined below.

PCB Dimensions: 233.35 mm x 160 mm x 1.6 mm

Board Dimensions: 6U x 4HP (one slot)

Weight: 595 grams (21 ounces)

PCB Dimensions



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Connectors

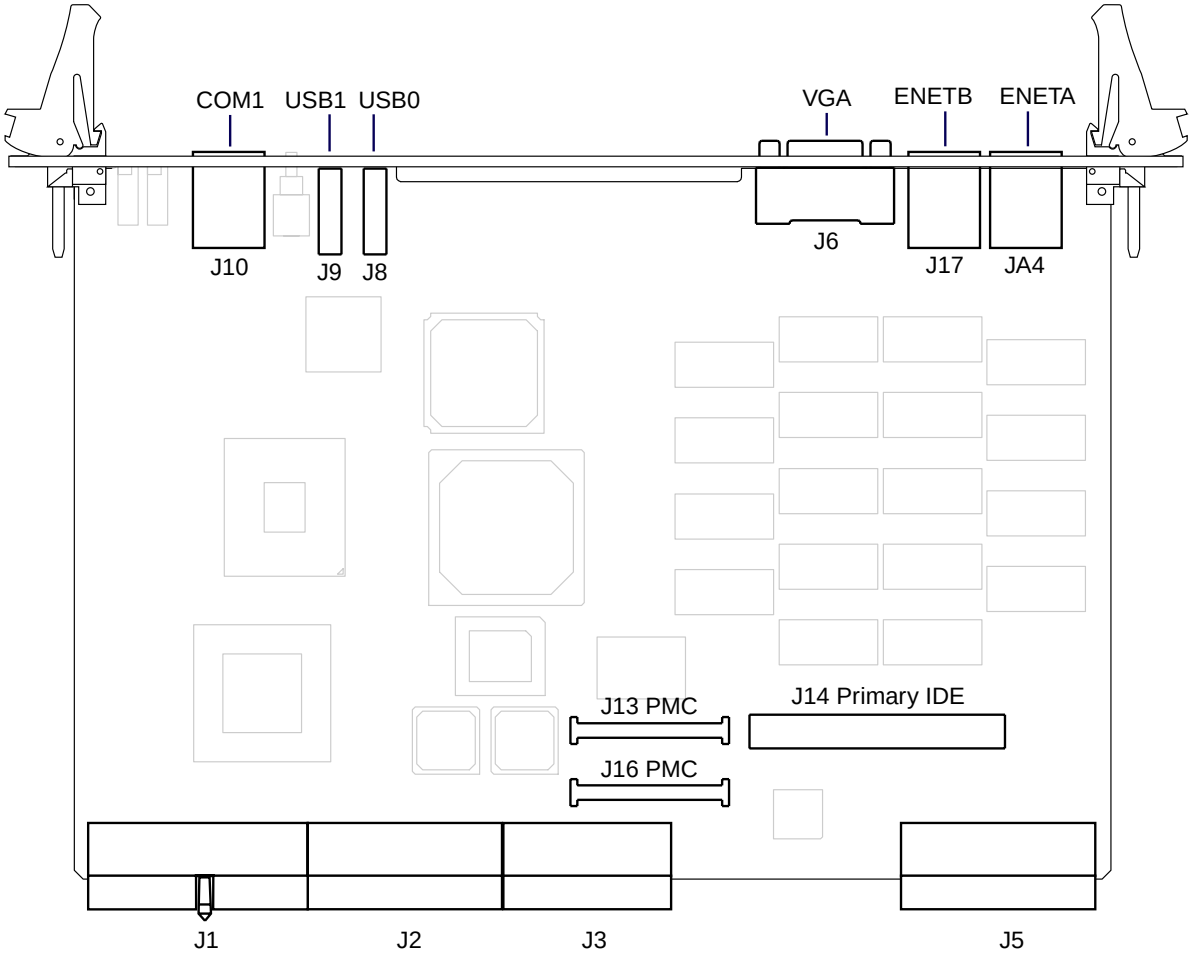
As shown in the "Connector Locations" figure, the ZT 5504 includes several connectors to interface to application-specific devices. A brief description of each connector is given in the "Connector Assignments" table below. A detailed description and pinout for each connector is given in the following topics.

Connector Assignments

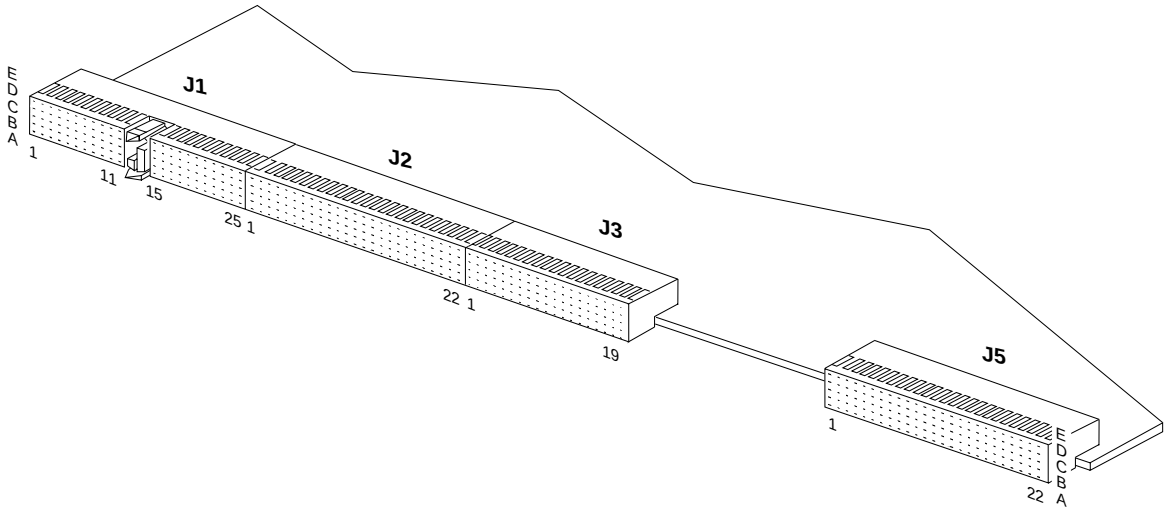
Connector	Function
J1	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
J2	CompactPCI Bus Connector (110-pin, 2 mm x 2 mm, female)
J3	CompactPCI Connector (95-pin, 2 mm x 2 mm, female)
J5	Rear-panel I/O Connector (110-pin 2 mm x 2 mm, female)
JA4	Ethernet A Connector (8-pin)
J17	Ethernet B Connector (8-pin)
J6	VGA Connector (15-pin, D-Shell)
J8	Universal Serial Bus Connector (4-pin, USB, Port 0)
J9	Universal Serial Bus Connector (4-pin, USB, Port 1)
J10	COM1 Serial Port (8-pin, RJ-45)
J13	PCI Mezzanine Connector (64-pin, 1 mm)
J14	IDE Connector (primary channel – local hard drive)
J16	PCI Mezzanine Connector (64-pin, 1 mm)

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Connector Locations



Backplane Connectors - Pin Locations



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J1 (CompactPCI Bus Connector)

J1 is a 110-pin, 2 mm x 2 mm, female 32-bit CompactPCI connector (AMP 352068-1). Rows 12-14 are used for connector keying. See the "J1 CompactPCI Bus Connector Pinout" table below for pin definitions. Refer to the "Backplane Connectors – Pin Locations" illustration for pin placement.

J1 CompactPCI Bus Connector Pinout

Pin#	A	B	C	D	E	F
25	5V	REQ64#	ENUM#	3.3V	5V	GROUND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	
23	3.3V	AD[4]	AD[3]	5V	AD[2]	
22	AD[7]	GND	3.3V	AD[6]	AD[5]	
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	
19	3.3V	AD[15]	AD[14]	GND	AD[13]	
18	SERR#	GND	3.3V	PAR	C/BE[1]#	
17	3.3V	IPMB_CLK	IPMB_DATA	GND	PERR#	
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK	
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	
KEY						
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	SHIELD
10	AD[21]	GND	3.3V	AD[20]	AD[19]	
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	
6	REQ#	PCI_PRESENT#	3.3V	CLK	AD[31]	
5	BRSVP1A5	BRSVP1B5	PCI_RST#	GND	GNT#	
4	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	
3	INTA#	INTB#	INTC#	5V	INTD#	
2	TCK	5V	TMS	TDO	TDI	
1	5V	-12V	TRST	+12V	5V	

Notes:

= Interfaces to long connector pins on the backplane.

= Interfaces to short connector pins on the backplane.

Row F interfaces to long connector pins on the backplane.

All other signals interface to medium length connector pins on the backplane.

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J2 (CompactPCI Bus Connector)

J2 is a 110-pin 2 mm x 2 mm female 64-bit CompactPCI connector (AMP 352152-1). See the "J2 CompactPCI Bus Connector Pinout" table for pin definitions and the "Backplane Connectors - Pin Locations" illustration for pin placement.

J2 CompactPCI Bus Connector Pinout

Pin#	A	B	C	D	E	F
22	GA4	GA3	GA2	GA1	GA0	GROUND SHIELD
21	SS_CLK6	SS_GND2	RSVC21	RSVD21	PRTACH	
20	SS_CLK5	SS_GND3	RSVC20	GND	HEART	
19	SS_GND4	SS_GND1	SMBDATA	SMBCLK	SMBALERT-	
18	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	
17	BRSVP2A17	GND	SS_PRST	SS_REQ6	SS_GNT6	
16	BRSVP2A16	BRSVP2B16	SS_DEG-	GND	BRSVP2E16	
15	J2STAGEEN#	GND	SS_FAL-	SS_REQ5	SS_GNT5	
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	
5	C/BE[5]#	64EN-	V(I/O)	C/BE[4]#	PAR64	
4	V(I/O)	J2_BPID#	C/BE[7]#	GND	C/BE[6]#	
3	SS_CLK4	GND	SS_GNT3	SS_REQ4	SS_GNT4	
2	SS_CLK2	SS_CLK3	SYSEN-	SS_GNT2	SS_REQ3	
1	SS_CLK1	GND	SS_REQ1	SS_GNT1	SS_REQ2	
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

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J3 (CompactPCI Connector)

J3 is a 95-pin 2 mm x 2 mm female connector (AMP 352171-1). See the "J3 Connector Pinout" table below for pin definitions and the "Backplane Connectors - Pin Locations" illustration for pin placement.

J3 Connector Pinout

Pin#	A	B	C	D	E	F
19	NC	NC	NC	NC	NC	GROUND SHIELD
18	RP_TXA+	RP_TXA-	GND	NC	NC	
17	RP_RXA+	RP_RXA-	GND	NC	NC	
16	RP_TXB+	RP_TXB-	GND	NC	NC	
15	RP_RXB+	RP_RXB-	GND	NC	NC	
14	NC	NC	NC	NC	NC	
13	NC	NC	NC	NC	NC	
12	NC	NC	NC	NC	NC	
11	NC	NC	NC	NC	NC	
10	NC	NC	NC	NC	NC	
9	NC	NC	NC	NC	NC	
8	NC	NC	NC	NC	NC	
7	NC	NC	NC	NC	NC	
6	NC	NC	NC	NC	NC	
5	NC	NC	NC	NC	NC	
4	NC	NC	NC	NC	NC	
3	NC	NC	NC	NC	NC	
2	NC	NC	NC	NC	NC	
1	NC	NC	NC	NC	NC	
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

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J5 (Rear Panel I/O CompactPCI Connector)

J5 is a 110-pin 2 mm x 2 mm female connector (AMP 352152-1) providing rear-panel user I/O. See the "J5 Rear Panel I/O Connector Pinout" table below for pin definitions and the "Backplane Connectors - Pin Locations" illustration for pin placement.

J5 Rear Panel I/O Connector Pinout

Pin#	A	B	C	D	E	F
22	USB0+	USB0-	SW-5V	USB1+	USB1-	GROUND SHIELD
21	SW-3.3V	GND	GND	GND	GND	
20	RED	GND	H-SYNC	GND	SMBD	
19	GND	SW-5V	GND	SW-5V	SMBC	
18	GREEN	GND	V-SYNC	GND	SMBA-	
17	GND	RSVD	RPIO_PRESENT#	RSVD	IPMB_PWR	
16	BLUE	GND	DDCCLK	KBDAT	KBCLK	
15	GND	SW-5V	DDCDAT	MSDAT	MSCLK	
14	S1RTS	S1CTS	S1R1N	S1DTR	ENETA-LINK	
13	S1DCD	S1TXD	S1RXD	S1DSR	ENETA-ACT	
12	S2RTS	S2CTS	S2RIN	S2DTR	ENETB-LINK	
11	S2DCD	S2TXD	S2RXD	S2DSR	ENETB-ACT	
10	TRK0-	WP-	RDATA-	HDSEL-	DSKCHG-	
9	MTR1-	DIR-	STEP-	WDATA-	WGATE-	
8	DENSL	INDEX-	MTR0-	DR1-	DR0-	
7	CS1S-	CS3S-	DA1	RPELED	RPEJECT-	
6	PWRGD	SPKR	NMI-	DA0	DA2	
5	DDRQ	IORDY	DIOW-	DDACK	DIOR-	
4	DD14	DD0	IDE_ACT	DD15	DRV-IRQ	
3	DD3	DD12	DD2	DD13	DD1	
2	DD9	DD5	DD10	DD4	DD11	
1	PBRST-	DRST-	DD7	DD8	DD6	
Pin#	**A**	**B**	**C**	**D**	**E**	**F**

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JA4 and J17 (Ethernet A and B Connectors)

JA4 (Ethernet A) and J17 (Ethernet B) are 8-pin RJ-45 connectors providing both 10 Mbit (10BASE-T) and 100 Mbit (100BASE-TX) protocols. Two LEDs are located inside each RJ-45 connector:

- Yellow indicates activity
- Green indicates a link

See the "JA4 and J17 Ethernet A and B Connector Pinout" table below for pin definitions.

Ethernet signals can be directed out J3 to the backplane. See system register E4h.

JA4 and J17 Ethernet A and B Connector Pinout

Pin#	Function
1	TX+
2	TX-
3	RX+
4	Unused
5	Terminated on ZT 5504
6	RX-
7	Unused
8	Terminated on ZT 5504

J6 (VGA Connector)

J6 is a 15-pin, female, D-shell connector (AMP 748390-6) providing a front panel interface for VGA signals. See the "J6 VGA Connector Pinout" table for pin definitions.

Video signals can be directed out J5 to an RPIO board. See switch SW2-3.

J6 VGA Connector Pinout

Pin#	Signal
1	RED
2	GREEN
3	BLUE
4	NC
5	DGND

Pin#	Signal
6	RGND
7	GGND
8	BGND
9	+5V (fused)
10	SGND

Pin#	Signal
11	NC
12	DDC DAT
13	HSYNC
14	VSYNC
15	DDC CLK

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J8 and J9 (Universal Serial Bus 0 and 1 Connectors)

J8 (Port0) and J9 (Port1) are Universal Serial Bus (USB) Interface connectors (AMP 440260-1). See the "J8 and J9 Universal Serial Bus 0 and 1 Connector Pinout" table below for pin definitions.

USB Port 0 can be directed out J5 to an RPIO board. See cuttable trace option CT57 and CT58. USB Port 1 can be directed out J5 to an RPIO board. See cuttable trace option CT31 and CT32.

J8 and J9 Universal Serial Bus 0 and 1 Connector Pinout

Pin#	Function
1	Vcc (Fused)
2	DATA-
3	DATA+
4	GND

J10 (COM1 Serial Port)

J10 is an RJ-45 connector providing a front-panel COM1 interface. COM1 signals are also directed out J5 to the backplane. See the "J10 COM1 Serial Port Pinout" table below for pin definitions. SRI (Serial Ring Indicator) and SCD (Serial Carrier Detect) signals are not included in the front panel RJ-45 connector.

Note: COM1 signals are available to the front- and rear-panel (at J5) simultaneously. Utilizing COM1 at the front and rear at the same time will cause a signaling conflict.

J10 COM1 Serial Port Pinout

Pin#	Function
1	RTS
2	DRT
3	TXD
4	GND
5	GND

Pin#	Function
6	RXD
7	DSR
8	CTS
-	SRI
-	SCD

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J13 and J16 (PCI Mezzanine Connectors)

J13 and J16 are 64-pin, 1.00mm, dual row, vertical stacking receptacles providing a PCI local bus interface to optional PMC cards. These connectors provide a complete 32-bit PCI interface. See the following "J13 PCI Mezzanine Connector Pinout" and "J16 PCI Mezzanine Connector Pinout" tables for pin definitions.

J13 PCI Mezzanine Connector Pinout

Pin	Signal
1	NC
3	GND
5	B0_INTD-
7	NC
9	B0_INTB-
11	GND
13	PMCB_PCICLK
15	GND
17	PMC2_REQ-
19	VIO (VCC3)
21	B0_PAD28
23	B0_PAD25
25	GND
27	B0_PAD22
29	B0_PAD19
31	VIO (VCC3)
33	B0_FRAME-
35	GND
37	B0_DEVSEL-
39	GND
41	NC
43	B0_PAR
45	VIO (VCC3)
47	B0_PAD12
49	B0_PAD9
51	GND
53	B0_PAD6
55	B0_PAD4
57	VIO (VCC3)
59	B0_PAD2
61	B0_PAD0
63	GND

Pin	Signal
2	-12V
4	B0_INTC-
6	B0_INTA-
8	VCC
10	NC
12	NC
14	GND
16	PMC2_GNT-
18	VCC
20	B0_PAD31
22	B0_PAD27
24	GND
26	B0_CBE-3
28	B0_PAD21
30	VCC
32	B0_PAD17
34	GND
36	B0_IRDY-
38	VCC
40	B0_LOCK-
42	NC
44	GND
46	B0_PAD15
48	B0_PAD11
50	VCC
52	B0_CBE-0
54	B0_PAD5
56	GND
58	B0_PAD3
60	B0_PAD1
62	VCC
64	REQ64B

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J16 PCI Mezzanine Connector Pinout

Pin	Signal
1	+12V
3	NC
5	NC
7	GND
9	NC
11	PMC2-BUSMODE2[1]
13	B0_PCIRST-
15	VCC3
17	NC
19	B0_PAD30
21	GND
23	B0_PAD24
25	PMC2_IDSEL[4]
27	VCC3
29	B0_PAD18
31	BO PAD16
33	GND
35	B0_TRDY-
37	GND
39	B0_PERR-
41	VCC3
43	B0_CBE-1
45	B0_PAD14
47	GND
49	B0_PAD8
51	B0_PAD7
53	VCC3
55	NC
57	NC
59	GND
61	ACK64B
63	GND

Pin	Signal
2	NC
4	NC
6	GND
8	NC
10	NC
12	VCC3
14	PMC2-BUSMODE3[2]
16	PMC2-BUSMODE4[3]
18	GND
20	B0_PAD29
22	B0_PAD26
24	VCC3
26	B0_PAD23
28	B0_PAD20
30	GND
32	B0_CBE-2
34	NC
36	VCC3
38	B0_STOP-
40	GND
42	B0_SERR-
44	GND
46	B0_PAD13
48	B0_PAD10
50	VCC3
52	NC
54	NC
56	GND
58	NC
60	NC
62	VCC3
64	NC

---

1 PMC2-BUSMODE2 has a 10k pullup to VCC3.

2 PMC2-BUSMODE3 has a 10k pulldown to GND.

3 PMC2-BUSMODE4 has a 10k pulldown to GND.

4 PMC2_IDSEL is connected to B0_PAD31 (PCI device 14h).

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J14 (IDE Connector)

J14 is a 44-pin, male, 2mm (.079") header (Samtec EHT-122-01-S-D), providing a primary channel IDE interface. See the "J14 IDE Connector Pinout" table below for pin definitions.

J14 IDE Connector Pinout

Pin#	Signal	Pin#	Signal
1	RST-	2	GND
3	DDP7	4	DDP8
5	DDP6	6	DDP9
7	DDP5	8	DDP10
9	DDP4	10	DDP11
11	DDP3	12	DDP12
13	DDP2	14	DDP13
15	DDP1	16	DDP14
17	DDP0	18	DDP15
19	GND	20	NC
21	PDREQ-	22	GND
23	PDIOW-	24	GND
25	PDIOR-	26	GND
27	PDIORDY	28	CSEL1[1]
29	PDACK-	30	GND
31	IRQ14	32	IOCS16-[2]
33	DAP1	34	PDIAG
35	DAP0	36	DAP2
37	CS1P-	38	CS3P-
39	PDASP	40	CS3P-
41	VCC	42	VCC
43	GND	44	NC

1 CSEL1 has 475Ω pulldown to GND.

2 IOCS16- has 10k pullup to VCC3 (+3.3V).

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B. Thermal Considerations

This appendix describes the thermal requirements for reliable operation of a ZT 5504 using the Mobile Pentium III Processor - M. It covers basic thermal requirements and provides specifics about monitoring the board and processor temperature.

Thermal Requirements

The ZT 5504 is equipped with an integrated heatsink for cooling the processor module. The maximum processor core temperature ***must not exceed 100°C***. The heatsink allows a maximum ambient air temperature of 50°C with 200 linear feet per minute (LFM) of airflow. The maximum power dissipation of the CPU is 21 W at 850 MHz and 1.60V.



CAUTION: External airflow must be provided at all times during operation to avoid damaging the CPU. Intel strongly recommends the use of a fan tray below the card rack to supply the external airflow.

The "Thermal Requirements" table below shows the relationship between ambient air temperature, board temperature, and processor core temperature.

Thermal Requirements

External Ambient Air Temperature (°C)	Temperature Around the Board (°C)	Pentium III Processor Core Temperature (°C)
0	13	44
5	18	49
10	22	54
15	27	60
20	33	65
25	37	69
30	42	74
35	47	79
40	52	84
45	57	89
50	63	95
55	68	100 = maximum

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Temperature Monitoring

Because reliable long-term operation of the ZT 5504 depends on maintaining proper temperature, Intel strongly recommends verifying the operating temperature of the processor module and processor core in the final system configuration.

The Pentium III processor incorporates an on-die thermal diode that can be used to monitor the processor's die temperature. The ZT 5504 includes an AMD 1026 Hardware Monitor to monitor the die temperature of the processor for thermal management purposes.

When checking airflow conditions, let the Processor Core Temperature Test dwell for at least 30 minutes and verify that the core temperature does not exceed 65°C. The processor "core" temperature must **never** exceed 100°C under any condition of ambient temperature or usage.



WARNING: Temperatures over 100°C may result in permanent damage to the processor.

Refer to the "Thermal Requirements" table for more information.

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C. System Registers

The ZT 5504 provides several system registers to control and monitor a variety of functions. Normally, only the system BIOS uses these registers, but they are documented here for application use as needed. Take care when modifying the contents of these registers, as the system BIOS may be relying on the state of the bits under their control.

System Register Definitions

The System Registers are accessible as follows:

	I/O Address	Register Name	Default Value	Access	Size
PAL	78h	Flash Control	0x00	R/W	8 bits
	79h	Watchdog	0x00	R/W	8 bits
	7Bh	J1 IPMB Control	0x00	R/W	8 bits
	80h	Port 80	0x00	WO	8 bits
	E1h	Event Monitors	0x00	RO	8 bits
	E3h	Switch Monitors	0x00	RO	8 bits
	E4h	Geographic Address	0x00	RO	8 bits
	E5h	Control Bits	0x00	WO	8 bits
	E6h	J5 SMBus Enable	0x00	WO	8 bits

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Flash Control (78h)

I/O Address: 78h

Default Value: 0x00

Size: 8 bits

Attribute: R/W

Note: This register is reset to 00h on init or reset. The BIOS resides in page 000.

Bit	Description	Default
7	**Flash Write Protection** Controls Write Enable to flash: 0 = Write protects flash. 1 = Allows writes to flash. Flash memory is discussed in Chapter 8 BIOS Recovery.	0
6	**BIOS Recovery Module Access Override** Controls flash access to the BIOS Recovery Module. The BIOS Recovery Module is discussed in Chapter 8. 0 = Allows access to the BIOS Recovery Module. 1 = Disallows access to the BIOS Recovery Module, reset/cpuinit to 0.	0
5:3	**RESERVED**	0
2	**Page 2** Flash A21 (512 KB page)	0
1	**Page 1** Flash A20 (512 KB page)	0
0	**Page 0** Flash A19 (512 KB page)	0

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Watchdog (79h)

I/O Address: 79h

Default Value: 0x00

Attribute: R/W

Bit	Description
7	**Stage 2 Monitor (Reset Monitor)** Monitors the second stage (Reset) timer status. Read Value: 0 = Watchdog has not timed out since power up or since this bit was last set to 0. 1 = Watchdog reset timeout occurred since power up or since bit was last set to 0. Write Value: 0 = Sets this bit to 0. 1 = No effect. Power Up Value = 0. A hard reset not caused by a watchdog timeout will set this bit to 0.
6	**Stage 1 Monitor (NMI or INIT Monitor)** Monitors the first stage (NMI or INIT) timer status. Read Value: 0 = Watchdog has not timed out since power up or since this bit was last set to 0; 1 = Watchdog timed out and either: • NMI output was asserted if bit 3 = 0; or • INIT output was asserted if bit 3 = 1. Write Value: 0 = Sets this bit to 0. 1 = No effect. Power Up Value = 0. A hard reset will set this bit to 0.

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Watchdog (79h), continued

Bit	Description
5	**Stage 2 Enable** Enables second stage (Reset) activation on timeout. Read Value: 0 = Reset activation on timeout disabled. 1 = Reset activation on timeout enabled. Write Value: 0 = Reset operation of the watchdog is not enabled. When the watchdog times out, the Stage 2 Monitor bit is not set to 1 and the Reset output is not asserted. 1 = Reset operation of the watchdog is enabled. When and if the watchdog times out: • The Reset output asserts. • The Stage 2 Monitor bit is set to 1 and stays high until set to 0 by software. • Reset action occurs approximately 250 ms after the NMI or INIT action. Power Up Value = 0. Value After Timeout = 0 (doesn't re-arm). A hard reset will set this bit to 0.
4	**Stage 1 Enable** Enables NMI or INIT activation on timeout. Read Value: 0 = Disabled. 1 = Enable NMI activation on timeout if bit 3 = 0. Enable INIT activation on timeout if bit 3 = 1. Write Value: 0 = Disable NMI operation of the watchdog. When the watchdog times out, the Stage 1 Monitor bit is not set to 1 and the NMI or INIT output is not asserted. 1 = Enable NMI operation of the watchdog. When and if the watchdog times out: • The Stage 1 output (NMI if bit 3 = 0 or INIT if bit 3 = 1) occurs after the period of time specified by the Terminal Count bits. • The Stage 1 Monitor bit is set to 1 and stays high until set to 0 by software. • The Stage 2 Reset occurs approximately 250 ms after Stage 1 output, allowing the system software to take action before the reset occurs. Power Up Value = 0. Post Timeout Value = 0. A hard reset will set this bit to 0.

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Watchdog (79h), continued

Bit	Description
3	**NMI or INIT** Selects between generating an NMI or a CPU INIT. Read Value: 0 = NMI 1 = INIT This bit is set to 0 at reset. Write Value: 0 = NMI is generated when the watchdog times out. 1 = INIT is generated when the watchdog times out. Power Up Value = 0. A hard reset will set this bit to 0.
2:0	**Terminal Count (TermCnt2…TermCnt0)** Read Value: Reflects the value written to bits 2 through 0. Write Value: These bits determine the terminal count of the watchdog. Below is the minimum timeout period. The watchdog times out in no less than the minimum value. The nominal timeout period is 30% longer than the minimum. 000 = 250 ms 100 = 32 s 001 = 500 ms 101 = 64 s 010 = 1 s 110 = 128 s 011 = 8 s 111 = 256 s Power Up Value = 000. A hard reset will set these bits to 000.

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J1 IPMB Control (7Bh)

I/O Address: 7Bh

Default Value: 0x00

Attribute: R/W

Bit	Description
7:5	**RESERVED**
4	**J1 IPMB Enable** Connect/disconnect IPMB signals to the ZT 5504's J1 connector. Read Value: 0 = Disconnect. 1 = BMC IPMB is connected to J1. Write Value: 0 = Disconnect. 1 = BMC IPMB is connected to J1.
3:0	**RESERVED**

Port 80 BIOS POST Codes (80h)

I/O Address: 80h

Default Value: 0x00

Size: 8 bits

Attribute: WO

Bit	Description
7:0	**D7-D0** These bits correspond to eight LEDs (labeled D0 through D7) on the solder side of the PCB. The Port 80 bits report the BIOS POST (diagnostic) codes. These LEDS may not be visible if a hot swap shield is installed on the board. D7 corresponds to the most significant bit.

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Event Monitors (E1h)

I/O Address: E1h

Default Value: 0x00

Size: 8 bits

Attribute: RO

Bit	Description
7	**RESERVED**
6	**ENUM-** This bit displays the value of ENUM- from backplane J1-C25. A logical 0 means that ENUM- is not asserted on the backplane. A logical 1 means that ENUM- is asserted on the backplane.
5:0	**RESERVED**

Switch Monitors (E3h)

Address Offset: E3h

Default Value: 0x80

Size: 8 bits

Attribute: RO

Bit	Description
7	**Flash Write-Protect Status** This bit corresponds to the status of switch SW3-2. A logical 0 means that the flash is write-protected by SW3-2; a logical 1 means the flash is **not** write-protected by SW3-2.
6	**System Enable** This bit corresponds to the status of SYSEN. A logical 1 indicates that the ZT 5504 is plugged into a system slot. A logical 0 indicates that the ZT 5504 is plugged into a peripheral slot.
5	**RESERVED**
4	**Manufacturing Mode** This bit is used during production testing to load a default CMOS image. A logical 1 indicates manufacturing mode. A logical 0 indicates non-manufacturing mode.

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Switch Monitors (E3h), continued

3	**Console Redirection Enable** This bit reads the status of switch SW4-4. A logical 0 means that SW4-4 is open and console redirection is not enabled. A logical 1 means SW4-4 is closed and console redirection is enabled. Refer to the "Console Redirection" chapter in the *Intel NetStructure Embedded BIOS Manual* before attempting to use this feature.
2:0	**Software Configuration** These bits are used to provide configuration information to the user's software by monitoring the status of the Software Configuration SW4 segments listed below. An open switch reads back a 0; a closed switch reads back a 1. The bits correspond to switch segments as follows: **Bit 0** = SW4-1; **Bit 1** = SW4-2; **Bit 2** = SW4-3

Geographic Addressing (E4h)

Address Offset: E4h

Default Value: 0x00

Size: 8 bits

Attribute: RO

Bit	Description
7	**Ethernet Channel B Front/Rear panel Switching** This bit controls the MUX used to switch Ethernet channel B between the front and rear panel. A logical 0 selects the front panel. A logical 1 selects the rear panel. The power up default is 0. This is also a BIOS selectable option.
6	**RESERVED**
5	**Ethernet Channel A Front/Rear panel Switching** This bit controls the MUX used to switch Ethernet channel A between the front and rear panel. A logical 0 selects the front panel. A logical 1 selects the rear panel. The power up default is 0. This is also a BIOS selectable option.

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Geographic Addressing (E4h), continued

4:0	**Geographic Addressing** CompactPCI defines several signal additions to the PCI specification. One of these is GA[4..0], used for geographic addressing on the backplane. Geographic addressing uniquely differentiates each board based upon the physical slot into which it was inserted. Each backplane connector in a CompactPCI system has a unique code for GA[4..0]. See the *CompactPCI Specification, PICMG 2.0, Version 2.1* for more information on geographic addressing. The bits correspond to signals as follows: **Bit 0** = GA0; **Bit 1** = GA1; **Bit 2** = GA2; **Bit 3** = GA3; **Bit 4** = GA4. A logical 0 indicates that the corresponding GA pin is open. A logical 1 indicates that the corresponding GA pin is low (GND).

Control Bits (E5h)

Address Offset: E5h

Default Value: 0x00

Size: 8 bits

Attribute: W

Bit	Description
7:0	**RESERVED**

J5 SMBus Enable (E6h)

Address Offset: E6h

Default Value: 0x00

Size: 8 bits

Attribute: W

Bit	Description
7	**J5 SMBus Enable** This bit enables SMBus function through the rear panel J5 connector. A logical 1 enables this function.
6:0	**RESERVED**

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D. Datasheet Reference

This appendix provides links to datasheets, standards, and specifications for the technology designed into the ZT 5504.

Board Serial Number

Refer to the Dallas Semiconductor *DS2401 Silicon Serial Number* datasheet for information about the DS2401. The datasheet is available on the Web at:

http://dbserv.maxim-ic.com/quick_view2.cfm?qv_pk=2903

CompactPCI

CompactPCI specifications can be purchased from the PCI Industrial Computer Manufacturers Group (PICMG) for a nominal fee. A short form CompactPCI specification is also available on PICMG's Website at:

http://www.picmg.org

Ethernet

Refer to the Intel *82550 Fast Ethernet Multifunction PCI/Cardbus Controller* datasheet for more information on the Ethernet LAN Controller. The datasheet is available from Intel's Website at:

http://developer.intel.com/design/network/index.htm

Intel 440GX AGPset

For more information on the following ZT 5504 functions, refer to the Intel *440GX AGPset: 82443GX Host Bridge/Controller* datasheet.

- USB
- Counter/Timers
- DMA controllers
- Real-Time Clock
- Interrupt controllers
- Reset Control register
- IDE Interface Controller

This datasheet and other information is available online at:

http://developer.intel.com/design/chipsets/datashts/index.htm

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Mobile Pentium III Processor - M in BGA2 Package

For more information about the Intel Mobile Pentium III Processor - M in BGA2 Package, see the *Mobile Intel Pentium III Processor - M in BGA2 and Micro-PGA2 Packages* datasheet. This document is available online at:

http://developer.intel.com/design/mobile/datashts/245302.htm

PCI-To-PCI Bridge

For more information about the Intel 21154 PCI-to-PCI bridge, refer to the 21154 PCI-to-PCI Bridge datasheet available from the Intel Website at:

http://developer.intel.com/design/bridge/datashts/

PMC Specification

For more information about PMC modules and the PMC Specification, refer to the sponsoring organization's Website at:

http://www.vita.com/

SuperI/O

Refer to the National Semiconductor *PC87309 SuperI/O Plug and Play Compatible Chip in Compact 100-Pin VLJ Packaging* datasheet for more information on the following ZT 5504 functions:

- Floppy Disk controller
- Serial Port controller
- Mouse and Keyboard controller
- Parallel Port

The datasheet is available online from the National Semiconductor Website at:

http://www.national.com/pf/PC/PC87309.html

Video

For more information about the Chips and Technologies 69000 HiQVideo* Accelerator with Integrated Memory, refer to the *69000 HiQVideo Accelerator with Integrated Memory* datasheet. This and related documents are available online at:

http://www.asiliant.com/69000.htm

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E. Agency Approvals

CE Certification

The ZT 5504 meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility and Low-Voltage Directive 73/23/EEC for Product Safety. The ZT 5504 has been designed for NEBS/ETSI compliance.

Safety

UL/cUL 60950	Safety for Information Technology Equipment (UL File # E179737)
EN/IEC 60950	Safety for Information Technology Equipment
CB Report Scheme	CB certificate and Report

Emissions Test Regulations

FCC Part 15, Subpart B

EN 55022

CISPR 22

Bellcore GR-1089

EN 50081-1 Emissions

GR-1089-CORE	Sections 2 and 3
EN 55022	Class A Radiated
EN 55022	Power Line Conducted Emissions
EN 61000-3-2	Power Line Harmonic Emissions
EN 61000-3-3	Power Line Fluctuation and Flicker

EN 55024 Immunity

GR-1089-CORE	Sections 2 and 3
EN 61000 4-2	Electro-Static Discharge (ESD)
EN 61000 4-3	Radiated Susceptibility
EN 61000 4-4	Electrical Fast Transient Burst
EN 61000 4-5	Power Line Surge
EN 61000 4-6	Frequency Magnetic Fields
EN 61000 4-11	Voltage Dips, Variations, and Short Interruptions

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Regulatory Information

FCC (USA)

This product has been tested and found to comply with the limits for a Class A digital device pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This product generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Note: This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.

2. This device must accept any interference received, including interference that may cause undesired operation.



CAUTION: If you make any modification to the equipment not expressly approved by Intel, you could void your authority to operate the equipment.

Industry Canada (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadien des Communications.

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

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F. Customer Support

This appendix offers technical and sales assistance information for this product, and information on returning an Intel NetStructure product for service.

Technical Support and Return for Service Assistance

For all product returns and support issues, please contact your Intel product distributor or Intel Sales Representative for specific information

Sales Assistance

If you have a sales question, please contact your local Intel NetStructure Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information is available at Intel's website, located at http://www.intel.com/network/csp/sales.

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