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Introduction

The TriVideo board with the TriMedia chip is a complex multiprocessor module. The functionality of the TriVideo module is determined by the Trimedia chip and the firmware that is running. It is important that TriVideo users understand the features of the Trimedia chip and the basic functionality of the firmware is implemented and what it can do and what it can not do.

Pipelines and processing

The TriVideo board is called TriVideo because it supports three simultaneous pipelines.

- Video input for grayscale image processing

- Video input for color live video display and possible capture
- Video output for display

It can also process this video information on the fly in different ways

- Control brightness and contrast and hue
- Select image format between full, half or CIF format ($\frac{1}{4}$ frame)
- Impose a window of interest on the image at the moment of capture
- Threshold the pixel grayscale data to binary information
- Delay the video stream to the output port
- Invert the image
- Convert from YUV to RGB
- Scale horizontally
- Scale vertically
- Overlay locally or host generated information on the live video pipeline
- Overlay locally or host generated information on the video output pipeline

Some of these options are mutually exclusive.

An application scenario

A normal application scenario for the simultaneous use of these pipelines is described below.

The high-speed grayscale image processing pipeline is used to fill a user application buffer every 25 or 50 milliseconds depending on the frame and field rate. This takes about 3 - 6 milliseconds depending on PCI bus bandwidth which leaves a large about of time per frame/field over for processing by the host. This may well be a DSP board.

A horizontally and vertically scaled window of live video can be opened for display on the VGA screen. This can be turned on and off at will in order to see what the camera is doing. Scaling is step-less but introduces a delay. Use is also made of the conversion to RGB in order to display information on the VGA screen. An overlay can be included in this live video display.

After the image has been processed and some calculations made it is often the case that this information has to be merged with the original video signal for display on the output pipeline. The host can write information to the output overlay buffer or invoke local line drawing functions on the TriMedia CPU. In this way moving objects can be highlighted and tracked on the output display.

Functional description

System description

This block diagram explains the active parts of the TriVideo firmware and the relationship between hardware and software. At the same time it attempts to give insight into the buffering mechanisms and the delays that can occur.

There are 4 important hardware engines that can be used to make the three video processing pipelines:

- *Input port*
- *Output port*
- *Image Co Processor (ICP)*
- *The DMA engine*

These have to be correctly initialised in order to work together. The CPU performs this initialisation with configuration settings that the user will have written into the shared memory API registers.

Once these hardware engines are running the CPU is basically only doing minor things

- *Handling interrupts*
- *Housekeeping*
- *Collecting statistics*
- *Executing user commands*

Unless the user has configured thresholding, which is done by CPU, there is a lot of CPU power left over for custom image processing

Basic Buffering

There are actually multiple YUV input ring buffers that are filled in sequence by the input port. Due to the interlaced nature of video one buffer is not enough and two is only just enough. The TriMedia output and input ports are not synchronised and therefore if the output port just runs slightly faster or slower than the input port, eventually the output port will end up displaying the same buffer that the video input port is still capturing. Therefore it is necessary to have multiple raw input buffers. The input port end of field interrupt is used to calculate which buffer the output port will use. If there is a wrap around problem in this small circular queue then the output port will very infrequently display the same buffer twice. The output port will never show the same buffer as the input port is capturing.

The input port fills the basic circular YUV frame-buffer set sequentially. There are three static frame buffers which are filled by the CPU according to the requested mode. These are the greyscale, binary and inverted binary buffers. The CPU performs the optional image processing actions of thresholding and inversion on the fly in the input port ISR in-between frames.

The various hardware engines can then use either the ring buffers or the static buffers for the generation of the three video pipelines. All pipelines can be used in continuous or single frame mode.

Image processing pipeline

The simplest pipeline is the movement of greyscale images to a user supplied image-processing buffer over the PCI bus. After a frame interrupt the CPU programs a DMA request and the Y part of the YUV buffer is sent in one burst over the PCI bus to the host.

The image processing pipeline can be configured to use the static buffers which have already been processed to binary data by thresholding and/or inversion. All aspects of the image processing pipeline work in 50 field per second mode or 25 frame per second mode.

Output pipeline

The output pipeline uses one of the YUV ring buffers to create a live video out stream. It can also use its overlay buffer to merge user programmed information into the output stream. There is also a static output buffer which can be used by the output port to display host generated information. This could be another external video channel if the DMA engine is used to transport the video over the PCI bus and refresh this buffer.

The overlay buffers and the output buffers have different formats. The merging is controlled by an alpha blending bit which is available to the user.

ICP and live video buffering

The ICP pipeline is the most complex and can introduce delays due to the large amount of processing that has to be done. Basically the ICP can read information from any of the input buffers in YUV format and write it out to another temporary buffer in different format. Each time it does this a new buffer is required and a complete frame delay is introduced into the pipeline. Finally it can output this stream to the DMA engine. In the simplest case the ICP can take the raw YUV buffer and write it (using DMA) to the host memory. This will take about 40 milliseconds because it does not program the DMA engine in a single burst but spreads this out over the complete frame period. A YUV to RGB conversion can also be carried out on the fly so that this data can be copied directly to the VGA frame buffer of the host. This does not normally require extra buffering. However, in order to scale an image extra passes through the ICP are required and extra temporary buffers and therefore delays are added to the pipeline. Normally vertical and horizontal scaling will be required in order to present a small window of live video. This requires two passes and one buffer. First vertical scaling is applied and the complete frame is written to a buffer. Then RGB conversion and horizontal scaling can be performed together. A buffer is only needed if the local CPU is going to start a single DMA burst transfer, otherwise the ICP will write in multiple bursts on the fly to the PCI bus.

Memory areas

It can be seen that the TriVideo firmware requires a lot of memory for buffering of video data in addition to the normal memory requirements for program and data. In the end it is the availability of this memory which decides the functionality that can be configured in the firmware. Not all options are mutually inclusive.

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