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Find the *Interface Concept IC-FEP-VPX6a* at our website: *Click HERE*

IC-FEP-VPX6a

Virtex®-6 & QorIQ™ 6U VPX processing unit

The **IC-FEP-VPX6a** is a VPX hybrid processing engine coupling the latest generations of FPGAs and processor, both of them delivering a very high level of performance per watt.

With its QorIQ™ processor for system management and a PCIe advanced switch for a versatile coupling between the processing nodes, the **IC-FEP-VPX6a** board expands the flexibility of the two Virtex-6 FPGAs and the VPX high bandwidth serial interfaces.

Two FMC mezzanine sites enlarge the adaptability of the board to connect ADC, DAC, general IOs, video, sFPDP or additionnal FPGA FMC modules.

With this combination of high performance CPU, dual FPGAs and FMC sites, the **IC-FEP-VPX6a** provides the ideal platform for radar, sonar, electronic warfare and other very high demanding digital signal processing applications.



RoHS✓

Description

The **IC-FEP-VPX6a** is controlled by a P2020 processor integrating an e500 v2 Power Architecture core, a DP-FPU, an integrated Sec security engine and peripherals, as well as being fully software compatible with the existing PowerPC processors. (note : new QorIQ processor with Altivec under consideration)
The QorIQ provides the usual external interfaces (3*Ethernet, 2*Serial and 3*USB ports). Moreover, one eUSB slot allows to plug an optional SSD module.

The PCIe advanced switch allows versatile coupling between the processor, fabric links of the VPX backplane and the FPGAs. (Non transparent configuration possible for VPC fabric link).
Other Fabric Links of the VPX backplane are directly connected to the FPGAs GTX transveivers. Moreover, the two FPGAs are directly interconnected via GTX ports - allowing data rate up to 6,5 Gbps (*), LVDS and single-ended signals.

Each Virtex®-6 FPGAs of the **IC-FEP-VPX6a** is associated with two DDR3 memory banks, supporting a 800 MT/s transfer data rate (per bank), and a bank of SRAM DDRII running at 600 MT/s.

Each Virtex®-6 FPGA is interfaced with its own SPI flash (user parameters storage) and through a Spartan®-6 to the Mirror flash (local bitstreams storage - up to four bitstreams). Thanks to its PCIe link, this Spartan®-6 FPGA (control node) can also manage the downloading “on the fly” of the Virtex®-6 bitstreams, offering thus a dynamic reconfiguration of the FPGAs. This control node FPGA is also connected to the backplane via two GTP links.

The FMC sites of the **IC-FEP-VPX6a** are fully compliant with the FPGA Mezzanine Card standard (VITA 57.1), allowing to install FMC modules provided by IC, third-party or developped by the customers. Each FMC can be equipped with an optionnal IOs connector to route sixteen differential pairs (100 Ohms) from the FMC module directly to the VPX backplane.

(*) : FPGA -2 speed grade : 6.Gbps, -1 speed grade : 5Gbps

Main features

Processing Units

- One QorIQ processor P2020, 1GHz, e500 v2 core with :
  - 1 GB of DDR3 with ECC
  - 256 or 512 MBytes of NOR Flash
  - optional Nand Solid-state Disk (eUSB module)
- two Xilinx Virtex-6 : SX315T (-1 or -2),*SX475T (-1 only), LX240T or LX550T*, both offering
  - two banks of DDR3 : 40-bit wide, 1.25 GBytes each
  - one SRAM DDRII+ : 18-bit wide / 9 MB
  - one SPI flash (16 MBytes)
- one Spartan®-6 LX-45T (control Node)
  - one NOR flash (128 MBytes, for bistreams)

VPX Interfaces

- 4 * PCIe x4 port (from PCIe switch)
- GTX ports (1 or 2 * GTX x8 from each FPGAs)
- 2 * GTP (from Ctrl node FPGA)
- General purpose IOs
  - 2*16LVDS (16 from each FPGAs)
  - 2*16 differential pairs (16 from each FMC IOs connector)
  - GPIOs (from ctrl node FPGA)
- 2 * Ethernet ports (1000BT or 1000BX - from P2020)
- 1 * RS485/RS232 port
- 2 * USB 2.0 ports
- PIC µ-controller for System Management (per VITA 46.11)

FMC interfaces (for each site, from FPGAs)

- 80 LVDS
- 4 reference clocks
- 1 * GTX x4 link

Front panel interfaces

- 1 * USB 2.0, 1 * Ethernet 1000BT and 1 * console port

Accessories

- Engineering kit for debug : JTAG/COP and RS232 console.
- Rear transition module

The **IC-FEP-VPX6a** is a VPX 6U / 5HP board compliant with 6U module definitions of the VITA 46.0 standard. It is available in air cooled (**EFC1** & **EFC3**) and conduction cooled (**ECC3** & **ECC4**) VITA 47 classes.

IC-FEP-VPX6a

Virtex®-6 & QorIQ™ 6U VPX processing unit with two FMC sites

On-board firmware

Our basic firmware takes in charge Freescale's new QorIQ and its internal chipset initialization. This on-board firmware, based on the open-source UBOOT, is an efficient set of software stored in a secured flash.

UBoot

It is called by the reset vector when the board is powered up. It initializes the processor, performs a comprehensive Power-on self-tests (PBIT), before jumping into different applications according to the values stored in memory.

IC-BSP basic

These BSPs products are based on the standard distribution of the OS editor. They take in charge hardware initialization, interrupt handling and generation, hardware clock and timer services, memory management, PCIe management, mapping of memory spaces, serial ports, MAC driver for Gigabit ports... Interface Concept provides BSP for VxWorks® and Linux® operating systems. Other RTOS can be ported on request.

The **IC-FEP-VPX6a** hardware platform is compatible with the Xilinx development tools (ISE Design Suite, Platform cable...). Interface Concept provides :

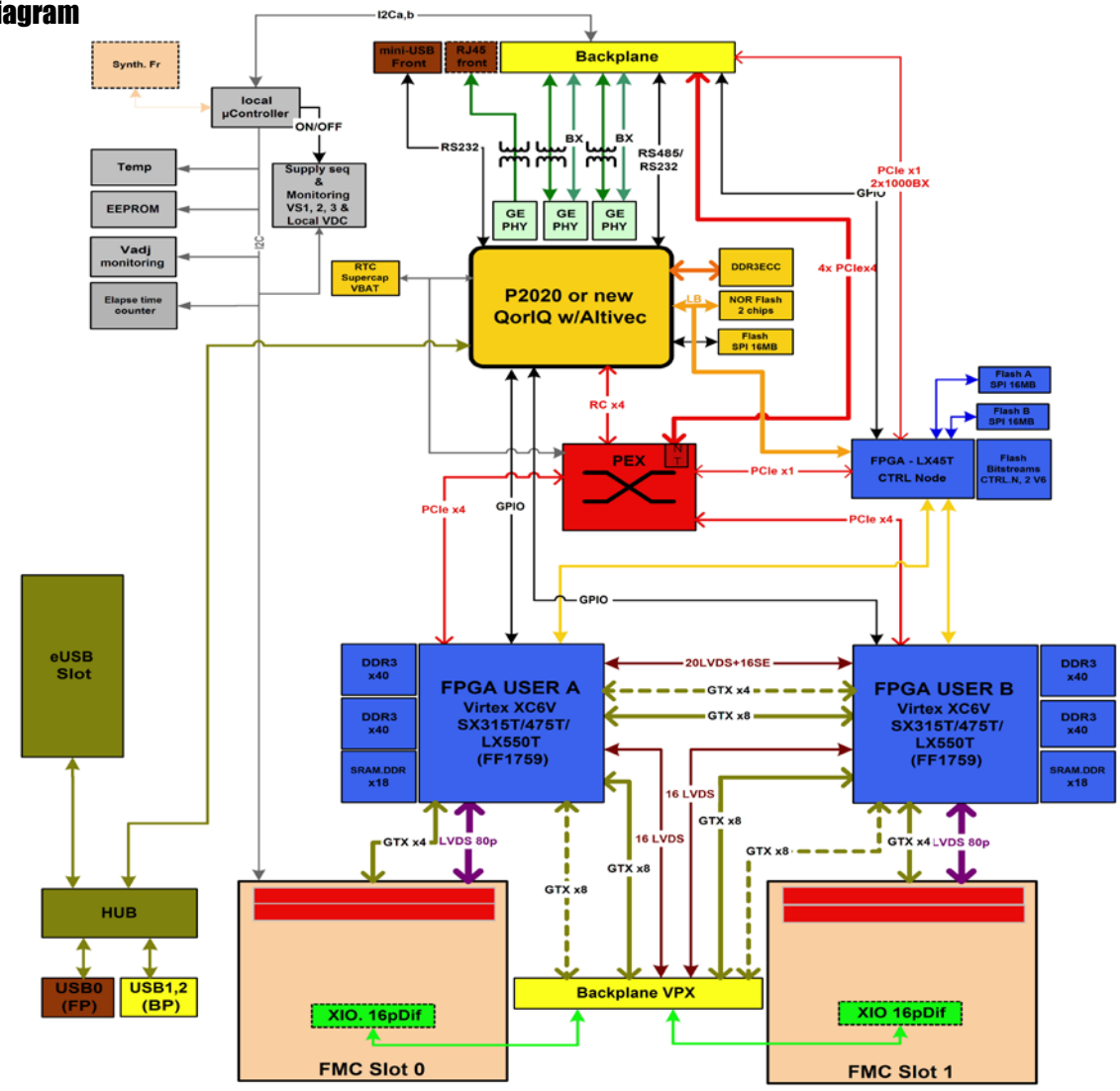
►VHDL code for system services (DDR3, SRAM DDRII, PCIe, Aurora, IC FMC interfaces...). Their implementation requires the Xilinx ISE Design Tools. Integration from Xilinx System Generator will be availble soon.

►host drivers for the CPU (Linux, VxWorks)

►Reference Designs (such as

The customers implement their own realtime applications with the capability to integrate the existing openSource code or third-party IP cores.

Block Diagram



Environnement Specifications:

Please consult the **IC-FEP-VPX6a** page at **www.interfaceconcept.com**.

Ordering Information:

Please contact our sales department : tel. **+33 (0)2 98 573 030** - email : **info@interfaceconcept.com**

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