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Find the *Interface Concept IC-FEP-VPX6e* at our website: ***Click HERE***

IC-FEP-VPX6e

UltraScale™ FPGA 6U VPX board with FMC+ sites

- *6U VPX*
- *2*Kintex® UltraScale™ KU115*
- *QorIQ LS1046A*
- *Gen2/3 PCIe switch*
- *Giga Ethernet L2 switch*
- *2 FMC+ sites*



Based on the latest Xilinx 20nm FPGA family, the **IC-FEP-VPX6e** enhances the Front-End Processing (FEP) Interface Concept product line.

By offering a higher performance/power consumption ratio compared to previous FPGAs, the UltraScale™ FPGAs make the **IC-FEP-VPX6e** the perfect solution to applications requiring DSP intensive processing in a 6U VPX form factor.

The **IC-FEP-VPX6e** together with other IC building blocks (Intel® and PowerPC SBCs, Ethernet Switches & Routers, FMC) running our Signal Processing Reference Design, are the ideal platforms for customers who want to streamline development by concentrating their efforts on their most strategical tasks.

Description

The high-end **IC-FEP-VPX6e** is controlled by a QorIQ® LS1046A processor integrating quad 64-bit Arm® Cortex A72 cores with high-performance Data Path Acceleration Architecture (DPAA) and network peripheral interfaces required by demanding processing applications.

The QorIQ® LS1046A provides the usual external interfaces: Ethernet, PCI Express, Serial and USB ports. In addition, an eUSB connector offers the capability to integrate a SSD module.

The PCIe advanced switch allows versatile coupling between the processor, the FPGAs and the fabric links of P1 VPX connector (Non-transparent configuration possible).

Thanks to the IC MultiWare software package and its simplified API, it is easy to integrate the **IC-FEP-VPX6e** in heterogeneous multi-domains PCIe architectures.

Other Fabric Links of the VPX backplane are directly connected to the two FPGAs GTH transceivers, the latter being directly interconnected via 12 GTY lanes and 24 differentials pairs.

Interface Concept has based the **IC-FEP-VPX6e** design on the Xilinx FPGA package B1204, providing the board with a high scalability level. While the standard configuration comes with the Kintex® UltraScale™ KU115, upgraded configurations with Virtex® UltraScale™or Virtex® UltraScale+™ can be supplied.

Each FPGA is coupled with two DDR4 SDRAM memory banks (supporting up to 2400 MT/s transfers), one optional QDRII+ SRAM memory bank and one SPI Mirror flash memory for local bitstreams storage and for user parameters.

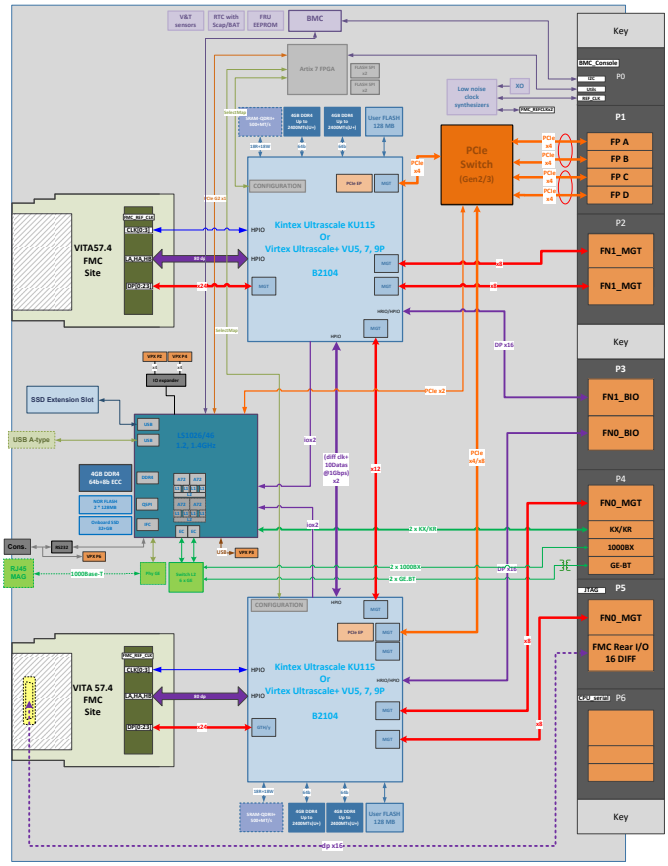
Both FMC+ sites are compliant with the FPGA Mezzanine Card standard (VITA 57.4), allowing to add FMC and FMC+ modules provided by IC, third-parties or developed by customers.

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IC-FEP-VPX6e

UltraScale™ FPGA 6U VPX board with FMC+ sites

Block Diagram



Main features

Processing Units

- QorIQ® LS1046A - quad 64-bit Arm Cortex®-A72 cores @1,8 GHz:
  - 4 GB DDR4 ECC
  - 2* 1Gbit QSPI Flash
  - on board SSD (32GB), eMMC
  - optional Nand Solid-state Disk (eUSB module)
- Two Kintex® UltraScale™ KU115, Virtex® UltraScale™ (or Virtex® UltraScale+™), both offering :
  - Two banks of DDR4 : 64-bit wide, up to 4GB each
  - QDRII SRAM
- The two FPGAs are interconnected:
  - directly via 12 GTY lanes and 24 differential pairs
  - via the Gen2/3 PCIe switch
- **One Gen2/3 PCIe switch**
- **One Giga Ethernet L2 switch**

VPX Interfaces

- 4 * PCIe x4 ports or 2* PCIe x8 ports (from the PCIe switch)
- GTH ports (2 * GTH x8 from each FPGA)
- General purpose IOs
  - 16 differential pairs each FPGA
  - 16 differential pairs from one FMC IOs connector (option)
  - GPIOs (from ctrl node FPGA)
- 2 * 10GigaBase-KR (or 1000BaseKX) from the processor
- 2 * 1000BaseKX and 2 * 1000BaseBT ports from the switch
- 1 * RS232 port
- 1 * USB 2.0 port
- PIC µ-controller for System Management (per VITA 46.11)

FMC+ interfaces (HSPC for each FPGA site)

- 80 * differentials pairs
- 4 * reference clocks
- 24 * GTH/Y lanes

Front panel interfaces

- 1 * USB 2.0, 1 * Ethernet 1000BaseT and 1*console port

The **IC-FEP-VPX6e** is a VPX 6U / 5HP board compliant with 6U module definitions of the VITA 46.0 standard. It is available in air-cooled and conduction-cooled grades.

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On-board firmware

UBoot

Our basic firmware supports NXP's new QorIQ initialization. This on-board firmware is an efficient set of software stored in a secured flash.

OS support

Interface Concept provides LSP Linux® distribution (IC-SDK development tool chain) and VxWorks® 7.0.

Firmware

The **IC-FEP-VPX6e** hardware platform is compatible with Xilinx Vivado development tools.

Multiware

In order to empower customers to concentrate their efforts on their most critical tasks, Interface Concept has developed a Fabric Management Software implemeting optimized services between PCIe domains over non-transparent bridges NTB such as: DMA transfers, Ethernet emulation over PCIe, management of shared memory, messages and semaphores, etc. (consult us for details).

Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 75°C or 85° C (*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : Temperature grades are subject to availability according to IC products. Please consult us.

All information contained herein is subject to change without notice.

For more information, please contact:

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