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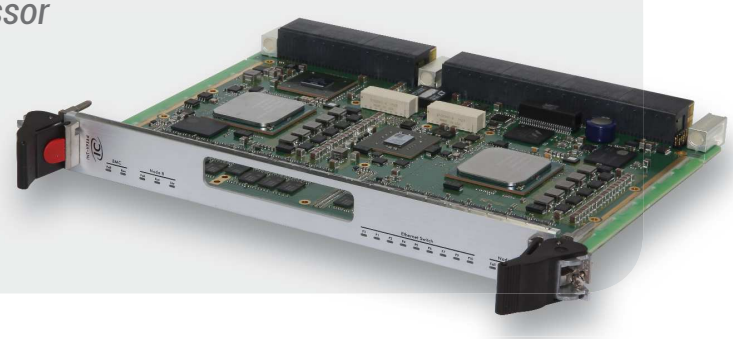
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Find the *Interface Concept IC-INT-VPX6d* at our website: *Click HERE*

IC-INT-VPX6d

Dual Intel® XEON SBC (Broadwell-DE SoC)

- *Dual Intel® Xeon® D-1500 processor*
- *up to 128 GB DDR4 with ECC*
- *Xilinx Kintex®-7 FPGA*
- *PCIe Switch*
- *XMC slot*



The new VPX 6U Digital Signal Processor (DSP) board **IC-INT-VPX6d** is the result of the experience and expertise gained by Interface Concept in the High Performance Embedded Computing (HPEC) field.

Taking advantages of the latest Intel's 14nm Xeon enhancements and the intercommunication capabilities provided by the OpenVPX standard, the **IC-INT-VPX6d** is the current most comprehensive dual Intel® processor design for applications requiring the highest processing capabilities together with "controlled" power consumption.

In the same spirit, IC offers the users with its own boot loader the security of always being able to support them as expected.

Description

The two computing nodes (A&B) are populated with XEON-D processors implementing up to twelve cores, and operate with up to 64GB DDR4/nodes offering the board an overall capability of 128GB.

For Data Plane and Expansion Plane, the **IC-INT-VPX6d** implements one PCIe Gen2/Gen3 switch attached to both CPUs via x8 links and to the backplane trough 16 lanes (4 x4 or 2 x8) on P1 and, optionnaly, 12 lanes (4 x4 or 2 x8) on P2. Optimized features of this PCIe switch (such as virtualization) allow versatile PCIe backplane configurations. Moreover, the two processors are linked together via a PCIe x4 link.

For Control Plane, the **IC-INT-VPX6d** implements an ultra low latency GE switch attached to each CPU and offering seven GigE ports (two of them capable of handling 2.5 Gbps). Moreover, one rear 10GigaE port is connected directly to each processor (10G KR).

An XMC site is attached to Node A (PCIe X4 / optional attachment to Node B PCIe X1 for custom application) and provides 20 differential I/O pairs routed from Pn6 to P6 in accordance with X12d+X8d pattern of VITA 46.9 and 9 single ended IO to P5/P6.

The IC-INT-VPX6d also takes advantage of the capabilities of this SoC solution to provide GPIOs, two USB and one SATA ports per processor. For storage, the board also features soldered SATA NAND SSD.

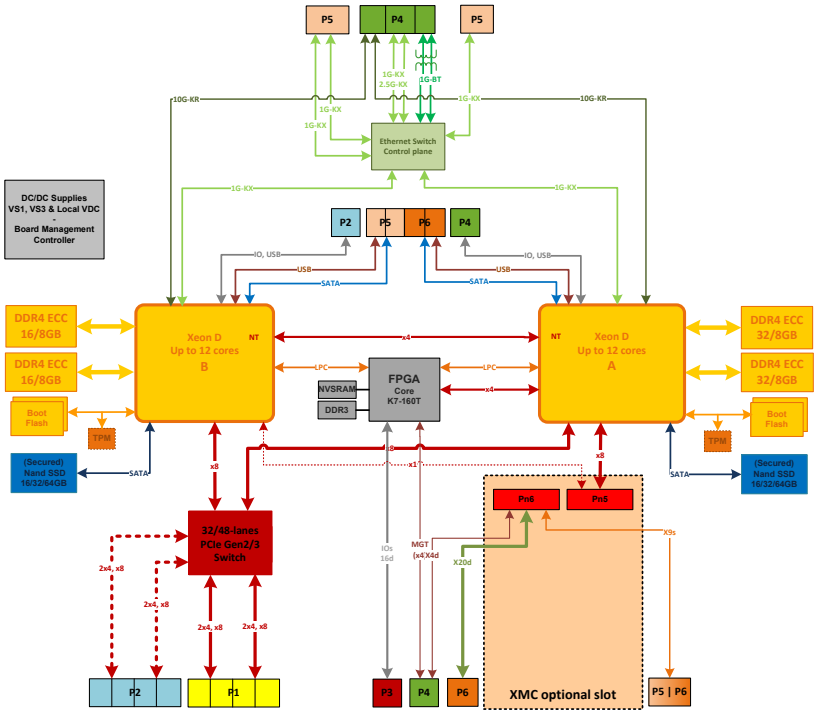
The **IC-INT-VPX6d** implements one FPGA interfaced with Node A (PCIe x4) to add Core Functions, for which IC provides a variety of IPs. This FPGA is connected directly to the P3/P4 connectors (SERDES/GPIOs).

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IC-INT-VPX6d

Dual Intel® XEON SBC (Broadwell-DE SoC)

Block Diagram



Main features

Processing Unit (per processor)

- Xeon D-15xx
- DDR4 with ECC (up to 64GB)
- Boot flash memory
- On board SATA SSD (up to 64GB)
- TPM 2.0

Communication subsystem (per processor)

- 1 * PCIe x8 to PCIe switch
- 1 * PCIe x4 to second processor
- 2 * USB ports (2 rear)
- 1 * Console port
- 2 * rear SATA interfaces
- GPIOs (Rear)
- 1 * GigE port (attached to the switch)
- 1 * 10G-KR (rear)

Ethernet Switch

- 7 * GigE ports (rear.2*1000Base-T and 5*1000Base-BX)

Extension (Node A)

- 1 * XMC slot (PCIe x8)
- 20 differential pairs (from Pn6 to P6 - X12d+X8d)

FPGA (Node A)

- 1 * FPGA Kintex-7
- MGT x4 (to P4)
- 16 differential pairs (to P3)

Miscellaneous

- BMC for System Management (per VITA 46.11)
- Power supply monitoring / Temperature sensor...
- Status LEDs
- Engineering kit for debug: JTAG
- 6U Rear Transition Module

The **IC-INT-VPX6d** is a 6U x 5HP (1") VPX board compliant with 6U module definitions of the VITA 46.0 standard (0.80 or 0.85" : please consult us), available in air-cooled and conduction cooled (without any front I/O) versions.

Note: this board is compatible with our previous versions of Intel® Core™ i7 (Gen 2 & 3) SBC to allow customers to upgrade existing systems and/or maintain existing design for long term support.

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On-board firmware

Interface Concept Single Board Computers based on Intel CPUs, use the new UEFI firrmware technology.

This Boot Loader, **developed and tested by our R&D team**, implements all the initializations and optimized PBITs while

ensuring the shortest boot time before launching the UEFI shell or loading the Operating System from storage devices

(CD, DVD, HDD, USB...) or network.

When the final application is running, Runtime services remain in memory thus allowing the user to access UEFI variables

for monitoring (e.g. PBIT results) or setup operations.

On request, we can customize the Boot Loader to keep only what is strictly necessary for customer's applications.

OS Support

Interface Concept provides LSP Linux® distributions (IC SDK, others...) and VxWorks® 7.0.

Multiware

In order to empower customers to concentrate their efforts on their most critical tasks, Interface Concept has developed a Fabric Management Software implementing optimized services between PCIe domains over non transparent bridges NTB) such as: DMA transfers, Ethernet emulation over PCIe, management of shared memory, messages and semaphores, etc. (Please consult us for details)

Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 75°C or 85° C (*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : Temperature grades are subject to availability according to IC products. Please consult us.

All information contained herein is subject to change without notice.

For more information, please contact:

INTERFACE CONCEPT
ADVANCED ELECTRONIC SOLUTIONS

3, rue Félix Le Dantec
29000 QUIMPER
Tel. +33 (0)2 98 57 30 30
Fax. +33 (0)2 98 57 30 00
info@interfaceconcept.com

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