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INTERFACE CONCEPT
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IC-PMC-CPCIa – 3U

Air or Conduction-cooled

CompactPCI Carrier

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TABLE OF CONTENTS

1. OVERVIEW 5

1.1 Introduction 5

1.2 References 5

1.3 Trademarks 5

1.4 Definitions 6

1.5 Board photograph 7
1.5.1 IC-PMC-CPCIa, standard version 7
1.5.2 IC-PMC-CPCIa, conduction-cooled version 8

2. DESCRIPTION 10

2.1 Configuration 10
2.1.1 Host configuration 10
2.1.2 Agent configuration 11

2.2 External interfaces 12
2.2.1 CPCI interface 12
2.2.2 PMC interface 12

2.3 Internal board functions 13
2.3.1 Board block diagram 13
2.3.2 Clock 13
2.3.3 Reset 13
2.3.4 Interrupts 14
2.3.5 PCI arbiter 15

2.4 Power consumption 16
2.4.1 PMC_cPCI board 16
2.4.2 PMC additional board 16
2.4.3 Hot-Swap functions 16

3. CONNECTORS 17

3.1 PMC Connectors 17
3.1.1 Pn1 & Pn2 PMC Connectors 17
3.1.2 Jn4 PMC-I/O Connector 18

3.2 CPCI Connectors 19
3.2.1 J1 CPCI Connector (32-bit PCI) 19
3.2.2 J2 CPCI Connector 20

4. LAYOUT 25

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5. CHARACTERISTICS 26
5.1 Physical dimension 26
5.2 Environment 26
5.3 Electromagnetic parameters 26
6. ACRONYMS 27

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1. Overview

1.1 Introduction

IC-PMC-CPCIa is a 3U compact PCI carrier for PCI Mezzanine Cards. The carrier integrates a 32-bit PCI bus capable of 33 or 66MHz frequencies.

It is compatible with 3V3-only signaling environment on the PCI interface, but requires 3V3 and 5V power supplies.

The carrier offers the ability to operate :

- as **host** on the PCI bus when it is plugged in a system slot
- as **agent** on the PCI bus when it is plugged in a peripheral slot

IC-PMC-CPCIa is available in **standard**, **rugged** or **conduction-cooled** version (See §5.2 for more details)

1.2 References

The following documents would be helpful to the understanding of the board :

- PCI Local Bus Specification, revision 2.2
- Compact PCI Specification, PICMG 2.0
- PMC on Compact PCI, PICMG 2.3
- Mechanical specification for conduction-cooled eurocards, IEEE 1101.2
- 2mm connector on conduction-cooled eurocards, VITA 30.1
- Processor PMC Standard, VITA 32
- Conduction-cooled PMC, VITA 20

1.3 Trademarks

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1.4 Definitions

Agent : an entity (component, board, IO pmc,...) on a PCI bus (non host of the system)

Arbiter : an entity that arbitrates transactions on a PCI bus

Carrier : the board on which is plugged a mezzanine card

Host : an entity that performs enumeration, processes interrupts, provides PCI clock and reset to all the agents

Master (or initiator): an entity (host or agent) that initiates a PCI bus transaction

Monarch : a processor PMC, configured (by the carrier) as host on a PCI bus

Non Monarch : a processor PMC, configured (by the carrier) as agent on a PCI bus

Peripheral : an agent on a Compact PCI bus

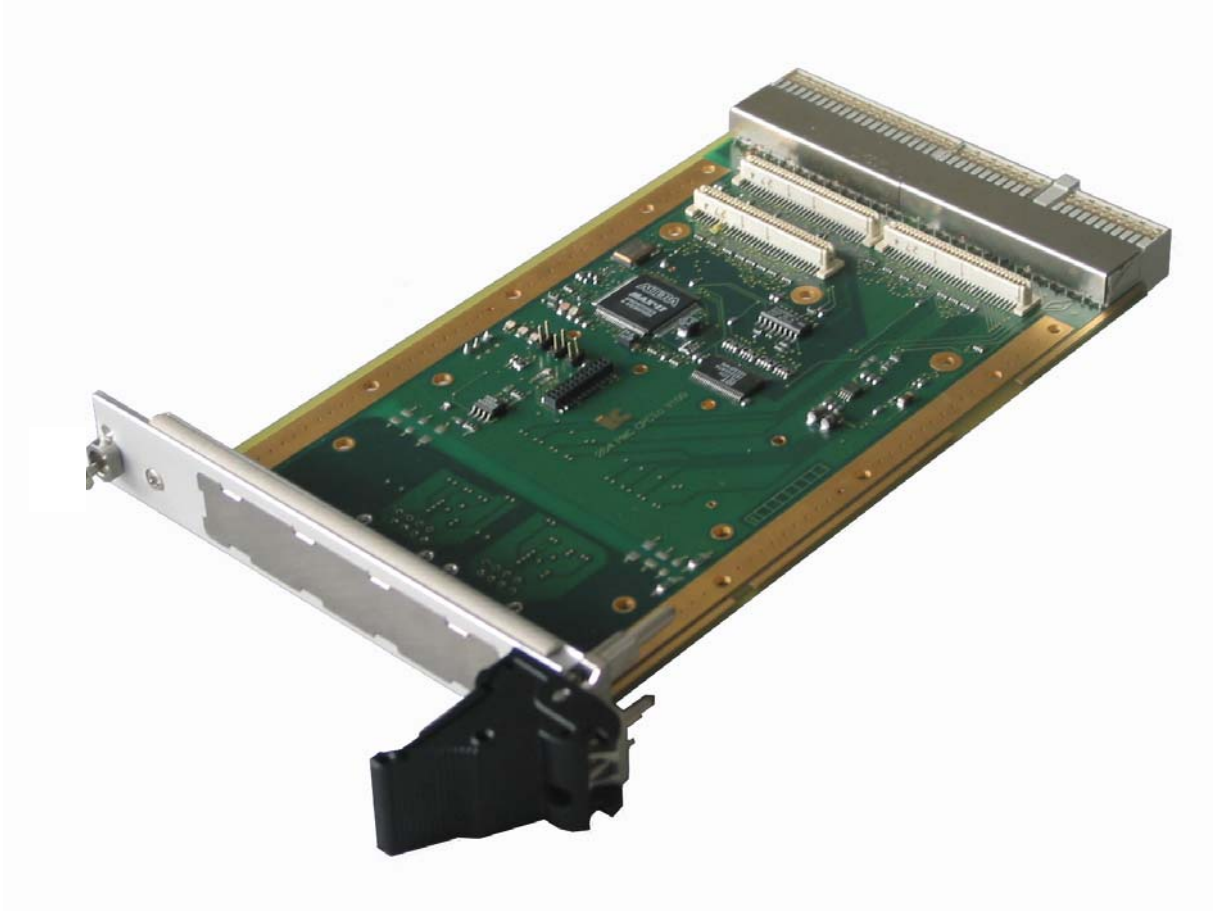
Slave (or target) : an entity (host or agent) that responds to a bus transaction initiated by a master

System : Compact PCI bus's host

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1.5 Board photograph

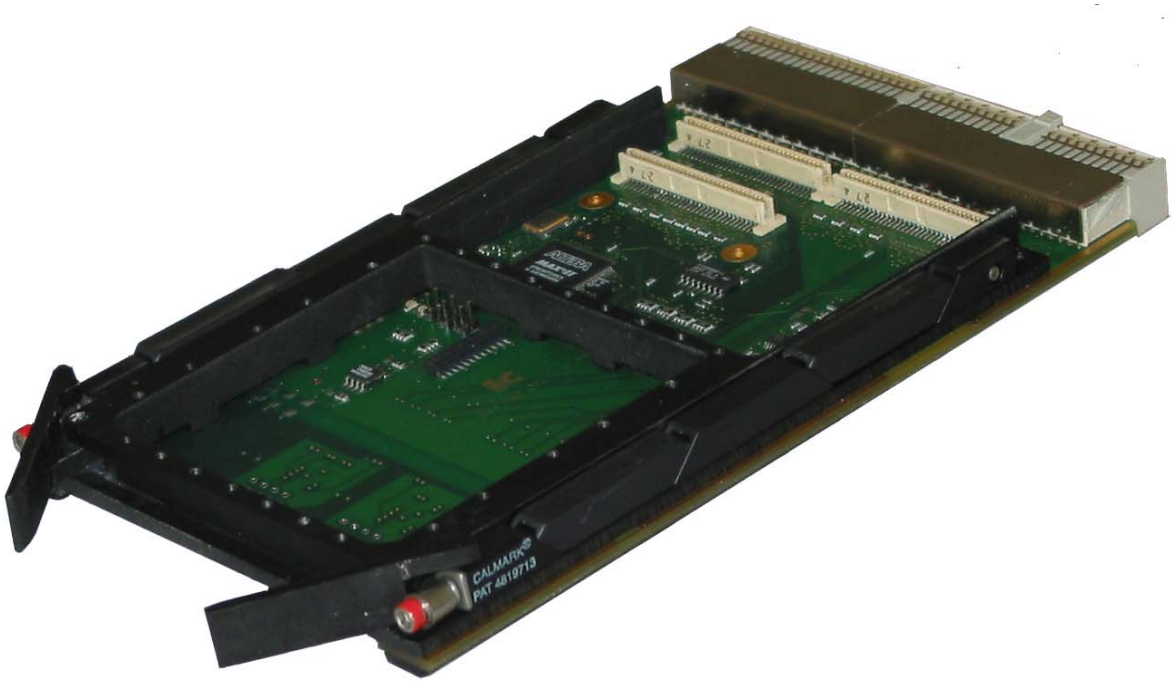
1.5.1 IC-PMC-CPCIa, standard version



IC-PMC-CPCIa standard version's photograph.

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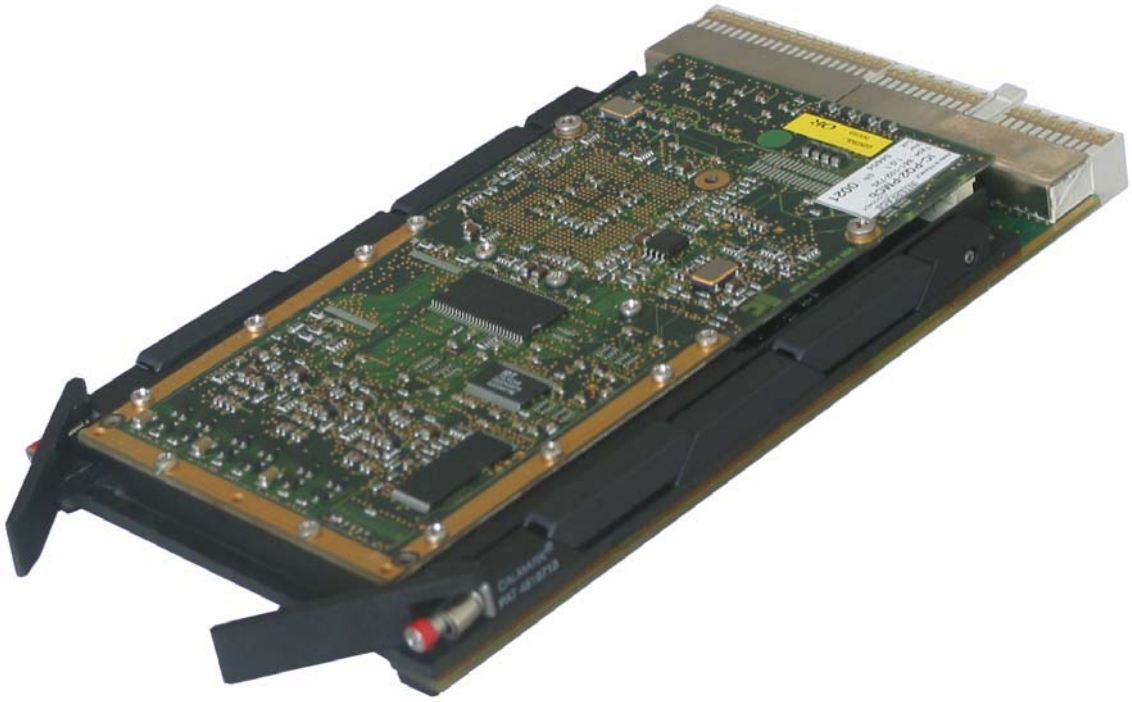
1.5.2 IC-PMC-CPCIa, conduction-cooled version



IC-PMC-CPCIa conduction-cooled version's photograph.

IC-PMC-CPCIa conduction-cooled is equipped with a thermal frame, integrating a conduction-cooled PMC interfacing area.

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IC-PMC-CPCIa with IC-PQ2-PMCb.

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2. Description

2.1 Configuration

The carrier offers the ability to operate as host or agent on the PCI bus. Depending on the slot in which it is plugged, it puts the PMC in monarch or non-monarch state.

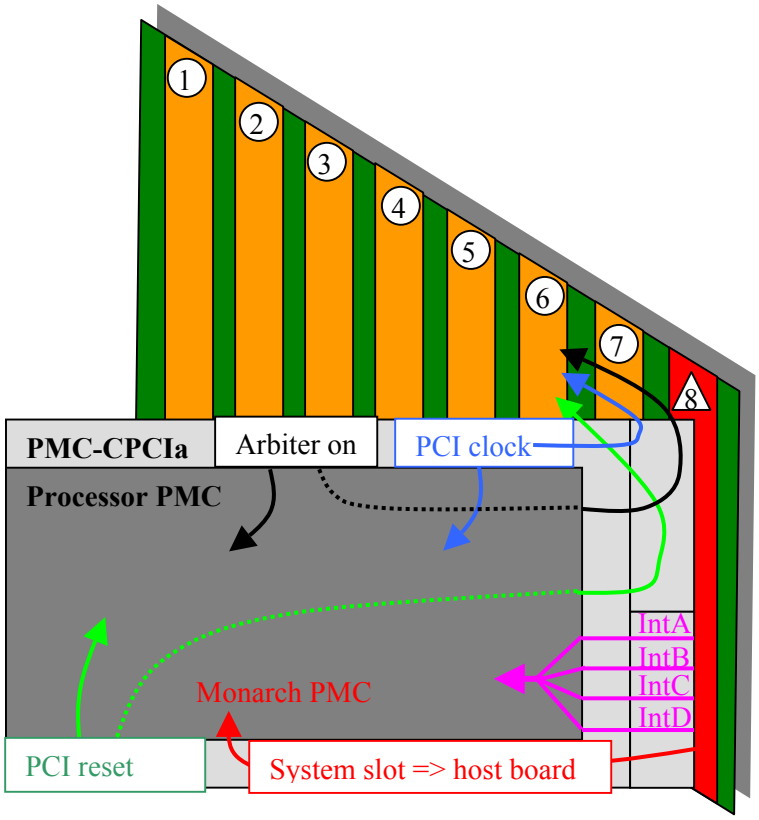
This configuration governs the routing of PCI reset and clocks, controlled by the CPLD.

2.1.1 Host configuration

If SYSEN signal is grounded (system slot) the carrier is host and puts the PMC in monarch state via the CPLD.

The PMC board cannot generate a PCI reset on the backplane, but there is a reset circuit on the carrier that controls the PCI reset of PMC and agent boards.
PCI interrupts (IntA, B, C, D) are transmitted by the carrier to the monarch PMC to be processed.
The carrier provides PCI clock to its monarch PMC and all the agents.

The carrier's PCI arbiter is asserted and controls the system.



△ : System slot (1 or 8)

○ : Peripheral slot

2.1.2 Agent configuration

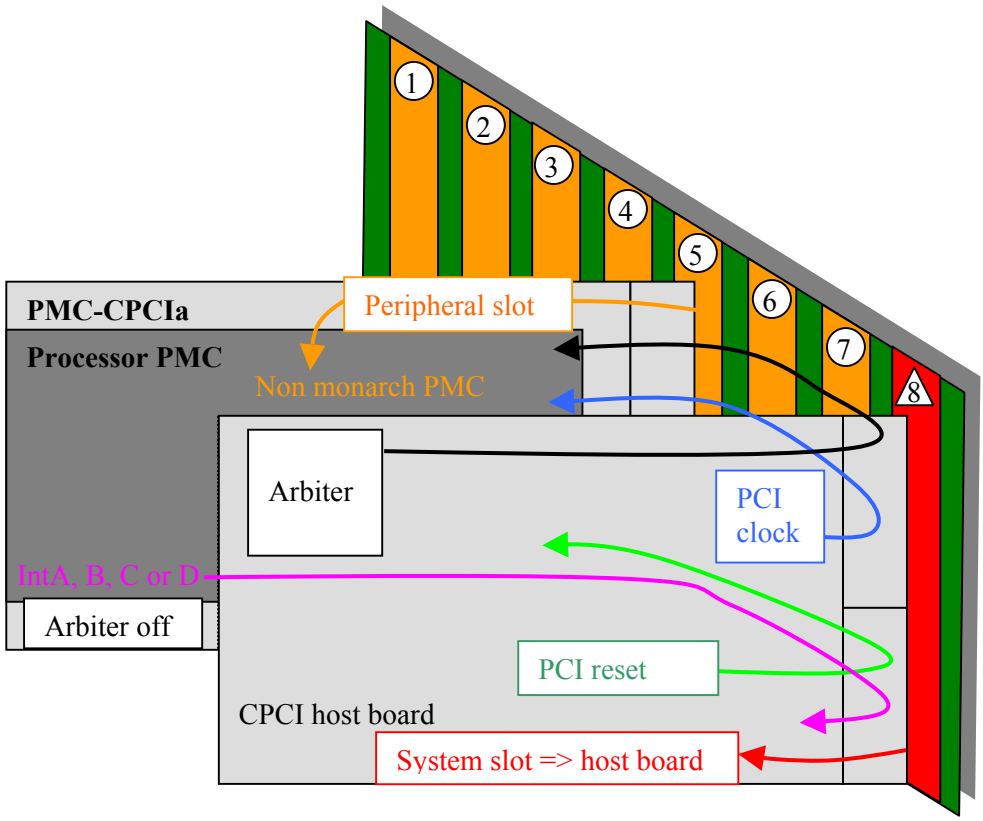
If SYSEN signal is high (agent slot) the carrier is agent and puts the PMC in non-monarch state via the CPLD.

The carrier asserts the PMC PCI reset if at least one of both following events occurs :

- a PCI reset coming from cPCI backplane
- a reset from the reset circuit (on the carrier)

The host board provides PCI clock to the carrier, that propagates it to its non-monarch PMC.
The non-monarch PMC can generate a PCI interrupt towards the cPCI backplane through the carrier.

The carrier's PCI arbiter is deactivated ; the host board's arbiter controls the system.



△ : System slot (1 or 8)

○ : Peripheral slot

2.2 External interfaces

2.2.1 CPCI interface

IC-PMC-CPCIa is compatible with PICMG 2.0 Compact PCI standard.

J1 CPCI connector is connected to 32-bit PCI bus. The board can operate at 33 or 66MHz, depending on the other boards of the system.

Except arbiter, clock signals and geographic addresses, J2 is connected to the Pn4 PMC connector as defined in PICMG 2.3 standard (refer to §3.2.2).

2.2.2 PMC interface

IC-PMC-CPCIa conduction-cooled version is designed to receive conduction-cooled PMC boards. A thermal frame fixed on the carrier dissipates the heat of the PMC through the chassis of the system, thanks to the thermal interfaces on the top and bottom of the carrier.

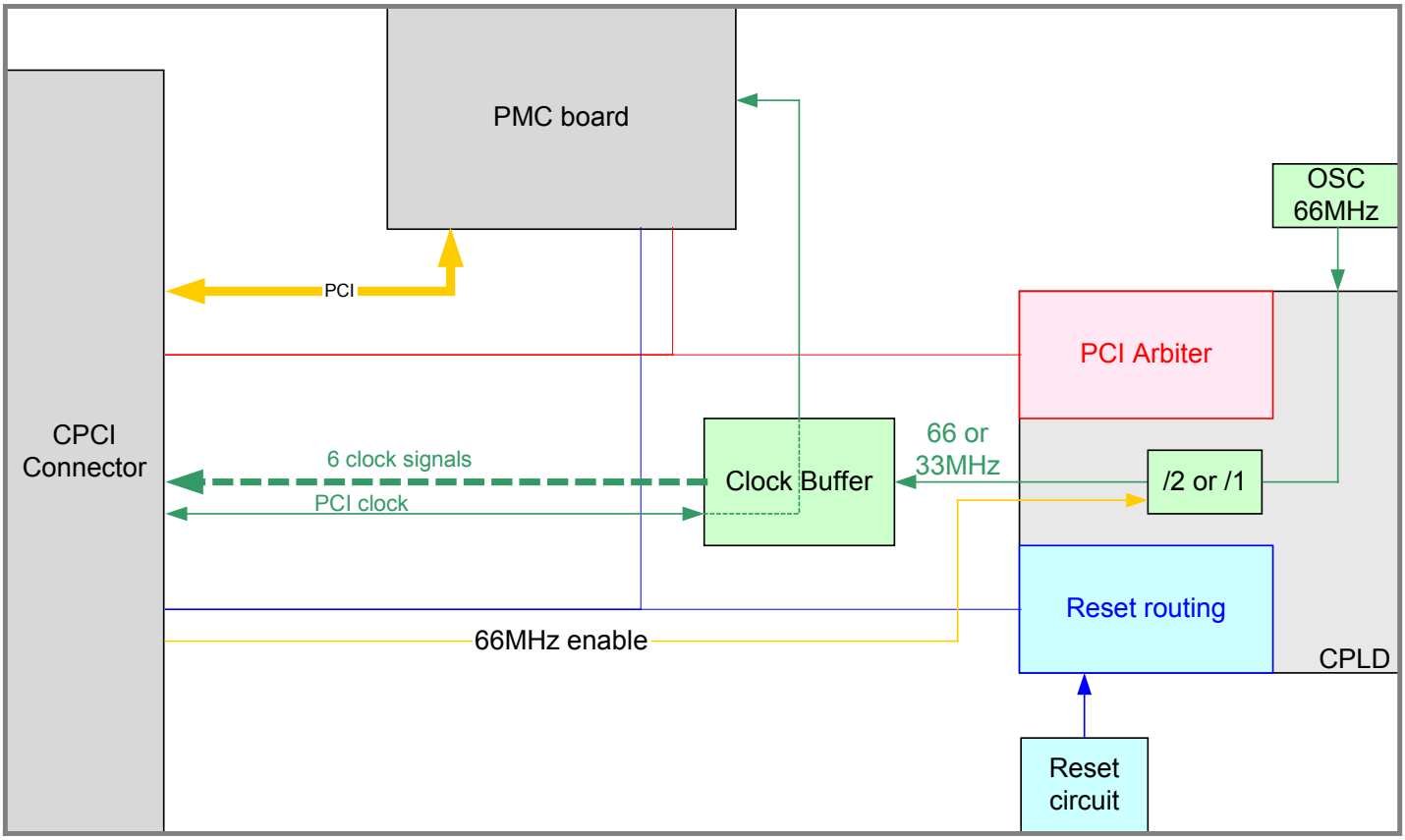
The carrier can also receive a standard PMC and be plugged in a standard Compact PCI backplane.

EREADY signal is usually used between PMC to indicate to the monarch board that the agent is ready to be enumerated.
In the case of IC-PMC-CPCIa, this signal is not used. The monarch board is waiting for 500µs at 66MHz (resp. 1s at 33MHz) before the beginning of the enumeration.

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2.3 Internal board functions

2.3.1 Board block diagram



2.3.2 Clock

A 66MHz 50ppm oscillator provides both clocks needed for the PCI interface (66MHz or 33MHz according to M66EN pin state) and for the CPLD.
PCI clocks are routed to each agent slot only when the carrier is plugged in a cPCI system slot. (See configurations §2.1)

2.3.3 Reset

The reset circuit provides a local power-on reset, a PCI reset for the PMC board, and a cPCI reset when using the board in a system slot.
The power-on reset is still active during 350ms after power supplies high level reach (90% of 3.3V and 5V).

The PMC board can also generate a PMC_RESET_OUT. This reset is spread through the carrier, over the cPCI interface in host configuration.

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2.3.4 Interrupts

The cPCI interrupt management depends on whether the board is placed on a system or a peripheral cPCI slot. The shift between the two modes is managed by the PLD by reading the SYSEN# line. When the carrier, in the system slot, puts the PMC in monarch state, the PMC is interrupt handler. Otherwise, the PMC can only generate PCI interrupt.

2.3.4.1 Agent mode

In this mode, the cPCI board may be an interrupt generator and so, generates interrupts on the PCI bus INTA# line.

PCI INT[A..D] are seen as outputs in agent mode. Only PCI INTA# line is used to generate interrupts. PCI INT[B..D] lines are tri-stated.

In Agent mode, the CPLD asserts PCI INTA# signal when the PMC, configured in non monarch mode, asserts its PCI INTA# output pin.

2.3.4.2 Host mode

The IC-PMC-cPCIa board in host mode is an interrupt receiver and handles interrupts on the PCI bus INT[A..D]# lines.

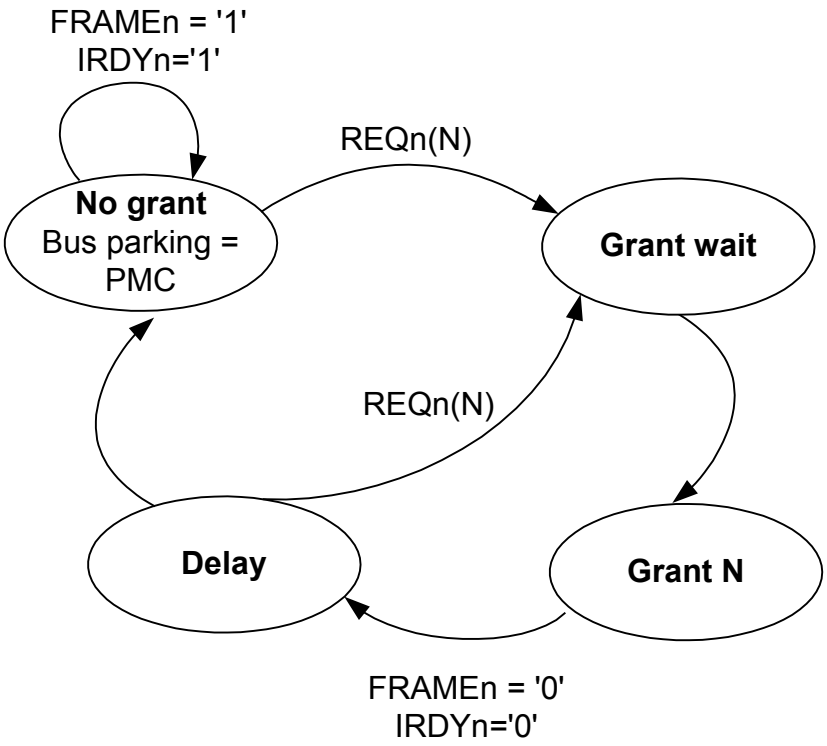
PCI INT[A..D] signals are seen as input to the IC- PMC -CPCIa board. They are directly connected to the cPLD.

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2.3.5 PCI arbiter

PCI uses a central arbitration scheme, where each master agent has a unique request (REQ#) and grant (GNT#) signal.

To do this arbitration, a PCI arbiter is integrated in the carrier's CPLD. It is a one-level arbiter, with bus parking to the PMC, as defined in the following resumed scheme :



Remarks :

- the arbiter is asserted only when the board is host.
- The bus parking is implemented to have a default bus owner in order that the PCI bus lines are always driven (See PCI specifications for more details about this function)

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2.4 Power consumption

2.4.1 PMC_cPCI board

Table below shows the maximum expected power consumption of IC-PMC-cPCIa :

Voltage	Consumption
+12V	0 W (not used for cPCI board)
-12V	0 W (not used for cPCI board)
5V	0 W (not used for cPCI board)
3.3V	Less than 2W

2.4.2 PMC additional board

the additional PMC board must not exceed the following limits:

- I/O PMC (IEEE 1386 CMC board specifications)

	Maw power Consumption
Side 1	6W
Side 1+ Side 2	7,5W

- PrPMC (ANSI VITA 32 specifications)

	Maw power Consumption
Standard modules	12W

The maximum rated current requirements of a Processor PMC must also not exceed the connector's maximum rated current limit.

2.4.3 Hot-Swap functions

No hot-Swap functions are provided by the IC-PMC-cPCIa board

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3. Connectors

3.1 PMC Connectors

3.1.1 Pn1 & Pn2 PMC Connectors

Jn1 (32-bit PCI)

Pin	Signal name	Signal name	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	PRESENT#	+5V	8
9	INTD#	PMC RSVD (●)	10
11	GND	+3.3V_Aux	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	S_V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	S_V(I/O)	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	PMC RSVD (●)	PMC RSVD (●)	42
43	PAR	GND	44
45	S_V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	S_V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	REQ64#	64

Jn2 (32-bit PCI)

Pin	Signal name	Signal name	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PMC RSVD (●)	8
9	PCI RSVD	PMC RSVD (●)	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE 3#	14
15	+3.3V	BUSMODE 4#	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE[2]#	32
33	GND	IDSELB	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE[1]#	GND	44
45	AD[14]	AD[13]	46
47	M66_EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	REQB#	52
53	+3.3V	GNTB#	54
55	PMC RSVD (●)	GND	56
57	PMC RSVD (●)	EREADY#	58
59	GND	RESET_OUT#	60
61	ACK64#	3.3V	62
63	GND	MONARCH#	64

(●) : these signals are left unconnected.

The grey signals are not used.

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3.1.2 Jn4 PMC-I/O Connector

IC-PMC-CPCIa J2	Pn4
A5	45
A6	40
A7	35
A8	30
A9	25
A10	20
A11	15
A12	10
A13	5
B4	49
B5	44
B6	39
B7	34
B8	29
B9	24
B10	19
B11	14
B12	9
B13	4
C4	48
C5	43
C6	38
C7	33
C8	28
C9	23
C10	18
C11	13
C12	8
C13	3
D4	47
D5	42
D6	37
D7	32
D8	27
D9	22
D10	17
D11	12
D12	7
D13	2
E4	46
E5	41
E6	36
E7	31
E8	26
E9	21
E10	16
E11	11
E12	6
E13	1

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3.2 CPCI Connectors

3.2.1 J1 CPCI Connector (32-bit PCI)

Table 1 –J1 Pin Assignment

25	5V	REQ64#	ENUM#	3.3V	5V	P1 / J1 CONNECTOR
24	AD1	5V	VI/O(1)	AD0	ACK64#	
23	3.3V	AD4	AD3	5V	AD2	
22	AD7	GND	3.3V	AD6	AD5	
21	3.3V	AD9	AD8	M66EN	C/BE0#	
20	AD12	GND	VI/O(1)	AD11	AD10	
19	3.3V	AD15	AD14	GND	AD13	
18	SERR#	GND	3.3V	PAR	C/EB1#	
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	
16	DEVSEL#	GND	VI/O(1)	STOP#	LOCK#	
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	
12 -14	KEY AREA					
11	AD18	AD17	AD16	GND	C/EB2#	
10	AD21	GND	3.3V	AD20	AD19	
9	C/BE3#	IDSEL	AD23	GND	AD22	
8	AD26	GND	VI/O(1)	AD25	AD24	
7	AD30	AD29	AD28	GND	AD27	
6	REQ0#	**PCI_PRESENT#**	3.3V	PCI_CLK	AD31	
5	BRSVP1A5	BRSVP1B5	PCI_RST#	GND	GNT0#	
4	IPMB PWR	HEALTHY#	VI/O(1)	INTP	INTS	
3	INTA#	INTB#	INTC#	5V	INTD#	
2	TCK	5V	TMS	TDO	TDI	
1	5V	-12V(2)	TRST#	+12V(2)	5V	
Pin	A	B	C	D	E	

(1) VI/O is equal to 3.3V
(2) Not connected

The grey signals are not used.

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3.2.2 J2 CPCI Connector

J2 Pin Assignment, host version

22	**GA4**	**GA3**	**GA2**	**GA1**	**GA0**	P2 / J2 CONNECTOR
21	**CLK6**	GND	GND	GND	GND	
20	**CLK5**	GND	GND	*RSV PLD*	GND	
19	GND	GND	GND	GND	GND	
18	*RSV PLD*	*RSV PLD*	*RSV PLD*	*UNC*(3)	*UNC*(3)	
17	*RSV PLD*	*RSV PLD*	**PRST#**	**REQ6#**	**GNT6#**	
16	*RSV PLD*	*RSV PLD*	**DEG#**	*UNC*(3)	*UNC*(3)	
15	*UNC*(3)	*UNC*(3)	**FAL#**	**REQ5#**	**GNT5#**	
14	*UNC*(3)	*UNC*(3)	*UNC*(3)	*UNC*(3)	*UNC*(3)	
13	Pn4 Pin 5	Pn4 Pin 4	Pn4 Pin 3	Pn4 Pin 2	Pn4 Pin1	
12	Pn4 Pin 10	Pn4 Pin 9	Pn4 Pin 8	Pn4 Pin 7	Pn4 Pin 6	
11	Pn4 Pin 15	Pn4 Pin 14	Pn4 Pin 13	Pn4 Pin 12	Pn4 Pin 11	
10	Pn4 Pin 20	Pn4 Pin 19	Pn4 Pin 18	Pn4 Pin 17	Pn4 Pin 16	
9	Pn4 Pin 25	Pn4 Pin 24	Pn4 Pin 23	Pn4 Pin 22	Pn4 Pin 21	
8	Pn4 Pin 30	Pn4 Pin 29	Pn4 Pin 28	Pn4 Pin 27	Pn4 Pin 26	
7	Pn4 Pin 35	Pn4 Pin 34	Pn4 Pin 33	Pn4 Pin 32	Pn4 Pin 31	
6	Pn4 Pin 40	Pn4 Pin 39	Pn4 Pin 38	Pn4 Pin 37	Pn4 Pin 36	
5	Pn4 Pin 45	Pn4 Pin 44	Pn4 Pin 43	Pn4 Pin 42	Pn4 Pin 41	
4	V(I/O)(1)	Pn4 Pin 49	Pn4 Pin 48	Pn4 Pin 47	Pn4 Pin 46	
3	**CLK4**	GND	**GNT3#**	**REQ4#**	**GNT4#**	
2	**CLK2**	**CLK3**	**SYSEN#**	**GNT2#**	**REQ3#**	
1	**CLK1**	GND	**REQ1#**	**GNT1#**	**REQ2#**	
Pin	A	B	C	D	E	

(1) VI/O is equal to 3.3V
(3)This pin shall be left unconnected

The grey signals are reserved.

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J2 Pin Assignment, agent version

22	**GA4**	**GA3**	**GA2**	**GA1**	**GA0**	**P2 / J2 CONNECTOR**
21	*RSV*	GND	GND	GND	GND	
20	*RSV*	GND	GND	*RSV PLD*	GND	
19	GND	GND	GND	GND	GND	
18	*RSV PLD*	*RSV PLD*	*RSV PLD*	*UNC*(3)	*UNC*(3)	
17	*RSV PLD*	*RSV PLD*	**PRST#**	*RSV*	*RSV*	
16	*RSV PLD*	*RSV PLD*	**DEG#**	*UNC*(3)	*UNC*(3)	
15	*UNC*(3)	*UNC*(3)	**FAL#**	*RSV*	*RSV*	
14	*UNC*(3)	*UNC*(3)	*UNC*(3)	*UNC*(3)	*UNC*(3)	
13	Pn4 Pin 5	Pn4 Pin 4	Pn4 Pin 3	Pn4 Pin 2	Pn4 Pin1	
12	Pn4 Pin 10	Pn4 Pin 9	Pn4 Pin 8	Pn4 Pin 7	Pn4 Pin 6	
11	Pn4 Pin 15	Pn4 Pin 14	Pn4 Pin 13	Pn4 Pin 12	Pn4 Pin 11	
10	Pn4 Pin 20	Pn4 Pin 19	Pn4 Pin 18	Pn4 Pin 17	Pn4 Pin 16	
9	Pn4 Pin 25	Pn4 Pin 24	Pn4 Pin 23	Pn4 Pin 22	Pn4 Pin 21	
8	Pn4 Pin 30	Pn4 Pin 29	Pn4 Pin 28	Pn4 Pin 27	Pn4 Pin 26	
7	Pn4 Pin 35	Pn4 Pin 34	Pn4 Pin 33	Pn4 Pin 32	Pn4 Pin 31	
6	Pn4 Pin 40	Pn4 Pin 39	Pn4 Pin 38	Pn4 Pin 37	Pn4 Pin 36	
5	Pn4 Pin 45	Pn4 Pin 44	Pn4 Pin 43	Pn4 Pin 42	Pn4 Pin 41	
4	V(I/O)(1)	Pn4 Pin 49	Pn4 Pin 48	Pn4 Pin 47	Pn4 Pin 46	
3	*RSV*	GND	*RSV*	*RSV*	*RSV*	
2	*RSV*	*RSV*	*UNC*(3)	*RSV*	*RSV*	
1	*RSV*	GND	*RSV*	*RSV*	*RSV*	
Pin	A	B	C	D	E	

(1) VI/O is equal to 3.3V
(3)This pin shall be left unconnected

The grey signals are reserved.

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3.2.2.1 Using an Interface Concept PrPMC with IC-PMC-CPCIa

The following table lists the PMC signals available on the IC-PQ2-PMCa/b 's Pn4 connector :

Pn4 (User I/O)			
Pin	Signal name	Signal name	Pin
1	FCC1 TX+ (►)	FCC1 RX+ (◄)	2
3	FCC1 TX- (►)	FCC1 RX- (◄)	4
5	GND	GND	6
7	FCC2 TX+ (►)	FCC2 RX+ (◄)	8
9	FCC2 TX- (►)	FCC2 RX- (◄)	10
11	GND	GND	12
13	FCC3 TX+ (►)	FCC3 RX+ (◄)	14
15	FCC3 TX- (►)	FCC3 RX- (◄)	16
17	GND	GND	18
19	SCC1 RxD (◄)	SCC1 TxD (►)	20
21	SCC1 RxClk (◄)	SCC1 TxClko (►)	22
23	SCC1 TxClki (◄)	SCC1 RTS (►)	24
25	SCC1 CTS (◄)	SCC1 DTR (►)	26
27	SCC1 DSR (◄)	SCC1 DCD (◄►)	28
29	SCC2 RxD (◄)	SCC2 TxD (►)	30
31	SCC2 RxClk (◄)	SCC2 TxClk (◄►)	32
33	SCC2 CTS (◄)	SCC2 RTS (►)	34
35	SCC2 DSR (◄)	SCC2 DTR (►)	36
37	SCC2 DCD (◄►)	SCC3 TxD (►)	38
39	SCC3 RxD (◄)	SCC3 TxClk (◄►)	40
41	SCC3 RxClk (◄)	SCC3 RTS (►)	42
43	SCC3 CTS (◄)	SCC3 DTR (►)	44
45	SCC3 DSR (◄)	SCC3 DCD (◄►)	46
47	SCC4 RxD (◄)	SCC4 TxD (►)	48
49	SCC4 RxClk (◄)	SCC4 TxClk (◄►)	50
51	SCC4 CTS (◄)	SCC4 RTS (►)	52
53	SCC4 DSR (◄)	SCC4 DTR (►)	54
55	SCC4 DCD (◄►)	GND	56
57	SPI Sel0 (◄►)	SMC2 RxD (◄)	58
59	SPI CLK (►)	SMC2 TxD (►)	60
61	SPI Mosi (►)	I2C SCL (►)	62
63	SPI Miso (◄)	I2C SDA (◄►)	64

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The following table lists the PMC signals available on the IC-PQ3-PMCb 's Pn4 connector :

Pn4 (User I/O) with MPC 8555

Pin	I/O	Alternate function	Alternate function	I/O	Pin
1		FCC1 TX+ (►)	FCC1 RX+ (◄)		2
3		FCC1 TX- (►)	FCC1 RX- (◄)		4
5	GND		GND		6
7		TSEC1 0+ (◄►)	TSEC1 1+ (◄►)		8
9		TSEC1 0- (◄►)	TSEC1 1- (◄►)		10
11	GND		GND		12
13		TSEC1 2+ (◄►) *TSEC2 0+ (◄►)*	TSEC1 3+ (◄►) *TSEC2 1+ (◄►)*		14
15		TSEC1 2- (◄►) *TSEC2 0- (◄►)*	TSEC1 3- (◄►) *TSEC2 1- (◄►)*		16
17	GND		GND		18
19	PD[31] (◄►)	SCC1 RxD (◄)	SCC1 TxD (►)	PD[30] (◄►)	20
21	PC[28] (◄►)	SCC1 RxClk (◄)	SCC1 TxClko (►)	PC[29] (◄►)	22
23	PC[21] (◄►)	SCC1 TxClki (◄)	SCC1 RTS (►)	PD[29] (◄►)	24
25	PC[15] (◄►)	SCC1 CTS (◄)	SCC1 DTR (►)	PA[10] (◄►)	26
27	PC[4] (◄►)	SCC1 DSR (◄)	SCC1 DCD (◄►)	PC[14] (◄►)	28
29		UART1_SIN (◄)	UART1_SOUT (►)		30
31	*PC[20] (◄►)*				32
33		UART1_CTS (◄)	UART1_RTS (►)		34
35	PC[5]			PA[11] (◄►)	36
37	PC[12] (◄►)			*PD[24] (◄►)*	38
39	*PD[25] (◄►)*	USB_DATAP		*PC[27] (◄►)*	40
41	*PC[26] (◄►)*	USB_DATAN		*PD[23] (◄►)*	42
43	*PC[11] (◄►)*	USB_V+	VBAT (►)	*PA[12] (◄►)*	44
45	*PC[6] (◄►)*	USB_GND		*PC[10] (◄►)*	46
47	PD[22] (◄►)	SCC4 RxD (◄)	SCC4 TxD (►)	PD[21] (◄►)	48
49	PC[24] (◄►)	SCC4 RxClk (◄)	SCC4 TxClk (◄►)	PC[25] (◄►)	50
51	PC[9] (◄►)	SCC4 CTS (◄)	SCC4 RTS (►)	PD[20] (◄►)	52
53	PC[7] (◄►)	SCC4 DSR (◄)	SCC4 DTR (►)	PA[13] (◄►)	54
55	PC[8] (◄►)	SCC4 DCD (◄►)	GND		56
57	PD[19] (◄►)	SPI Sel (◄►)	SMC2 RxD (◄) *UART0_SIN (◄)*	PA[8] (◄►)	58
59	PD[18] (◄►)	SPI CLK (►)	SMC2 TxD (►) *UART0_SOUT (►)*	PA[9] (◄►)	60
61	PD[17] (◄►)	SPI Mosi (►)	I2C SCL (►)(from CPM)	PD[14] (◄►)	62
63	PD[16] (◄►)	SPI Miso (◄)	I2C SDA (◄►)(from CPM)	PD[15] (◄►)	64

(◄) : input signals.
(►) : output signals.
(◄►) : bi-directional signals.

VBAT = 2V to 3.3V for SRAM and RTC data retention

XXXXXXX : Alternate function (Factory specific configuration)

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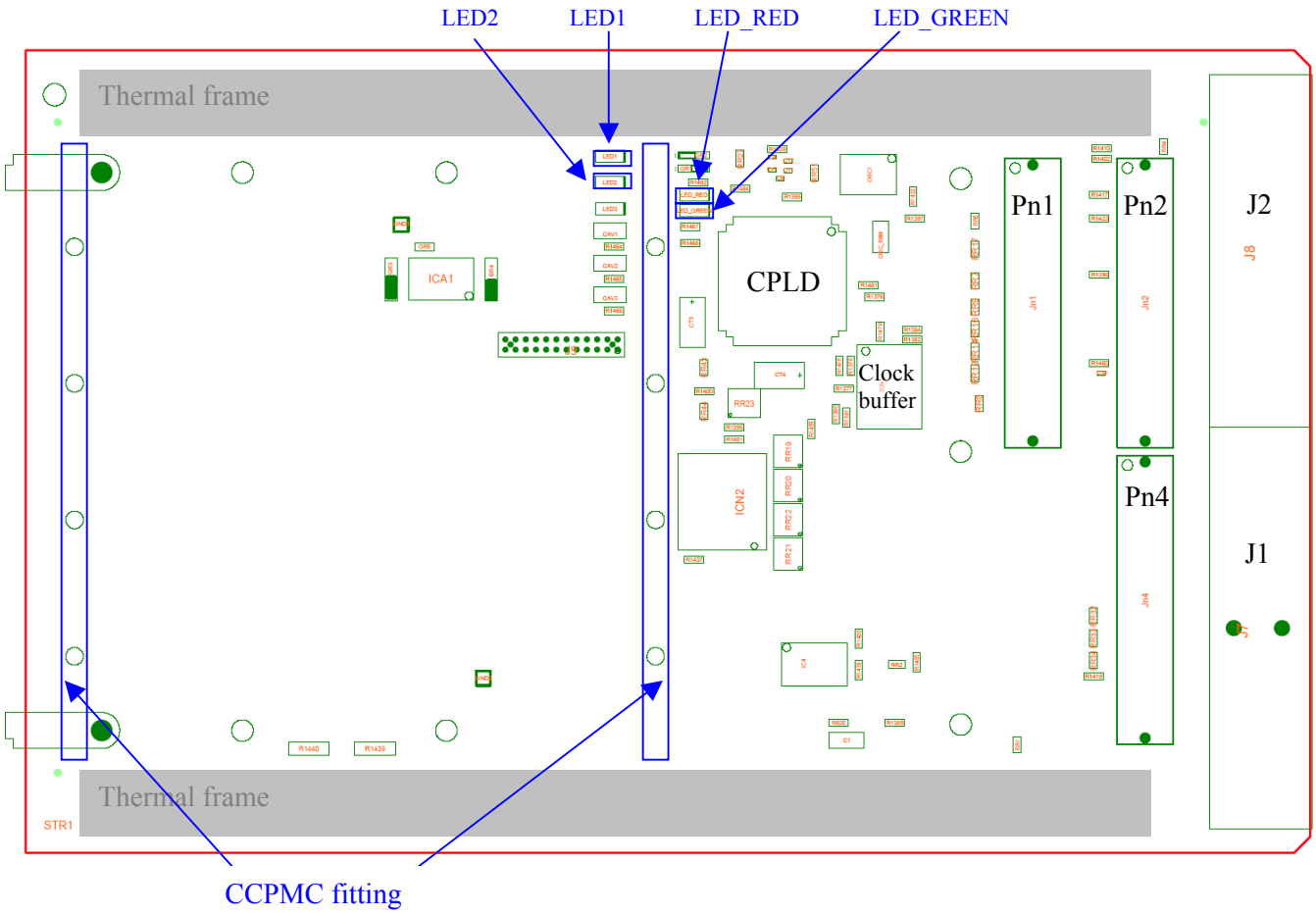
The following table lists the PMC signals available on the IC-e6-PMCa 's Pn4 connector :

Pn4 (User I/O)			
Pin	Signal name	Signal name	Pin
1	GB1_MDI+[0] (◄►)	GB1_MDI+[2] (◄►)	2
3	GB1_MDI-[0] (◄►)	GB1_MDI-[2] (◄►)	4
5	GND	GND	6
7	GB1_MDI+[1] (◄►)	GB1_MDI+[3] (◄►)	8
9	GB1_MDI-[1] (◄►)	GB1_MDI-[3] (◄►)	10
11	GND	GND	12
13	GB2_MDI+[0] (◄►)	GB2_MDI+[2] (◄►)	14
15	GB2_MDI-[0] (◄►)	GB2_MDI-[2] (◄►)	16
17	GND	GND	18
19	GB2_MDI+[1] (◄►)	GB2_MDI+[3] (◄►)	20
21	GB2_MDI-[1] (◄►)	GB2_MDI-[3] (◄►)	22
23	GND	GND	24
25	VDD_GB1	MPP[0] (◄►)	26
27	VDD_GB2	MPP[6] (◄►)	28
29	MPP[1] (◄►)	MPP[2] (◄►)	30
31	MPP[5] (◄►)	MPP[14] (◄►)	32
33	MPP[6] (◄►)	MPP[4] (◄►)	34
35	MPP[3] (◄►)	MPP[12] (◄►)	36
37	MPP[15] (◄►)	MPP[10] (◄►)	38
39	MPP[11] (◄►)	MPP[13] (◄►)	40
41	MPP[9] (◄►)	MPP[16] (◄►)	42
43	MPP[7] (◄►)	MPP[18] (◄►)	44
45	MPP[17] (◄►)	MPP[19] (◄►)	46
47	MPP[8] (◄►)	MPP[20] (◄►)	48
49	MPP[28] (◄►)	MPP[21] (◄►)	50
51	MPP[29] (◄►)	MPP[22] (◄►)	52
53	MPP[30] (◄►)	MPP[23] (◄►)	54
55	MPP[31] (◄►)	GND	56
57	SPI Sel (◄►)	MPP[11] (◄►)	58
59	SPI CLK (►)	MPP[12] (◄►)	60
61	SPI Mosi (►)	I2C SCL (►)	62
63	SPI Miso (◄)	I2C SDA (◄►)	64

(◄) : input signals.
(►) : output signals.
(◄►) : bi-directional signals.

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4. Layout



LED	Colour	Description
LED_RED	Red	On : PCI reset asserted
		Off : PCI reset deasserted
LED_GREEN	Green	On : Power supply present
		Off : No power supply
LED1	Yellow	On : IC-PMC-CPCIa in host configuration
		Off : IC-PMC-CPCIa in agent configuration
LED2	Yellow	On : 66MHz PCI clock
		Off : 33MHz PCI clock

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5. Characteristics

5.1 Physical dimension

This board is a 3U Compact PCI board (single width), PICMG 2.0 compliant.

5.2 Environment

The table below outlines the expected operating environment.

Parameter	Standard version	Rugged version	Conduction cooled
Operating temperature	0 to +55°C	-40 to +75°C	-40 to +75°C at the thermal interface
Recommended air flow	1m/s	2m/s	
Storage temperature	-45°C to +85	-45°C to +100	-45°C to +100
Humidity (non-condensing)	5-90%	5-95%	5-95%
Sinusoidal vibration	2G [20..2000]Hz	5G [20..2000]Hz	5G [20..2000]Hz
Random vibration	0.002g²/Hz [10..2000]Hz	0.05g²/Hz [10..2000]Hz	0.1g²/Hz [10..2000]Hz
Shock 1/2Sin. 11ms	20G	40G	40G

All these grades are for the PMC carrier alone. With a PMC or PrPMC, you must consider the limitation brought by this additional board.

5.3 Electromagnetic parameters

The table below outlines expected operating conditions for this product.

Nature of perturbations	Norms	Severity	Comments
ESD discharge	EN61000-4-2	TT/TR	+/-6kV (contact), +/-8kV (air)
HF radiation	EN61000-4-3	10V/m	80 to 1000Mhz
Fast transient burst	EN61000-4-4	+/-2kV +/-4kV	on Ethernet bus on Ethernet bus with surge protections
Shock waves	EN61000-4-5	+/-2kV +/-4kV	on Ethernet bus on Ethernet bus with surge protections
Common HF tests	EN61000-4-6	CT/CR	
Electromagnetic emission	EN55022	B	Conduction
Electromagnetic emission	EN55022	B	Radiation

To obtain these values, use a properly grounded shielded cable.

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6. Acronyms

CCPMC : Conduction-cooled PMC

CMC : Common Mezzanine Card

CPCI : Compact PCI

CPLD : Complex Programmable Logic Device

PCI : Peripheral Component Interconnect

PMC : PCI Mezzanine Card

PrPMC : Processor PCI Mezzanine Card

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