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# DDG200/400

## Table Driven Digital Delay Generator



- Table Driven with up to 500,000 User Programmed Pulse Delay/ Width Entries per Channel
- 2 or 4 Independent Channels
- 1 nsec Pulse Width / Delay Resolution
- ± 2 nsec of Trigger to Output Jitter
- Wide Delay Range From 270 nsec To 4 msec
- Wide Pulse Range From 50 nsec To 1 msec
- Programmable Pulse Amplitude Up To 5.0 V In 10 mV Steps
- Pulse Trigger Range of 100 Hz to 1 MHz
- Ovenized 10 MHz Crystal Oscillator With 0.25 ppm Accuracy
- Adjustable Trigger Threshold Input Levels
- Source signals to the VXI TTLTRG bus to Synchronize Multiple Instruments
- Register-based, C-1 VXI Module with IVI Compliant Drivers and GUI control
- IRIG-B Time Stamp (option)

The DDG200/400 Digital Delay Generator is a C-size, register-based VXI instrument with programmable delay and width parameter memory behind each channel. The instrument provides two (DDG200) or four channel (DDG400) output pulses with variable delay and width, and programmable pulse amplitude. Pulses can be used to gate an RF synthesizer to control the delay and width of RF pulses, or it can be used for precise sequence timing of experiments, tests, and similar applications. Pulse and delay parameters are programmable with 1 ns resolution over a wide range of values. Both internal and external pulse-triggering modes are provided. The four individual pulse outputs are controlled by a user programmable "***scenario table***", containing individual delay and width parameters for each output channel. The scenario table is capable of containing up to 500,000 individual delay/ width settings per channel. All internal timing is derived from a highly stable, ovenized 10MHz crystal oscillator reference.

The DDG200/400 can be triggered either internally by a 100 Hz to 1 MHz programmable clock, from an external trigging source, or from the VXI TTLTRG bus. It can also source signals to the TTLTRG bus to synchronize instruments across the VXI backplane. The delay from trigger to pulse output is programmable from 270 ns to 4 ms while pulse width is programmable from 50 nsec to 1 msec. Pulse amplitude is programmable from -2 to +5 Vdc into 50 ohms. The DDG200/400 is a new class of instrument specifically designed to provide test engineers with a flexible timing tool to aid in the generation of complex radar pulse simulations. When combined with an IF or RF source, the DDG200/400 can be used to control the timing of pulses to a radar receiver, simulating target movement or terrain variations. Multiple timing channels allow the DDG200/400 to control the simulation of multiple signals, useful for simulating multiple targets or in Electronic Counter-Measure (ECM) simulation.

Other features of the DDG200/400 include independent asynchronous triggering and timing parameters for each channel plus an optional IRIG-B time code input for correlating activity with other instruments and across multiple channels. The DDG200/400 comes standard with IVI compliant drivers and a Graphical User Interface to aid in the development and debug of timing scenarios.

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# *DDG200/400 Specifications**

## Clock, Internal:

| | |
|---|---|
| PLL Oscillator Frequency | 1 GHz, fixed |
| PLL Reference, Internal | 10 MHz, temperature stabilized |
| Reference Accuracy | 0.25 ppm |
| Jitter | <10 psec |

## Clock, External:

| | |
|---|---|
| PLL Reference, External | 10 MHz |
| Input Level | 1 Vp:p to 5 Vp:p |
| Coupling | Capacitive |
| Input Termination | Unterminated |
| Connector | SMB |

## Channels (Electrically/ Functionally Independent Outputs):

| | |
|---|---|
| Pulse Outputs | 2 standard, 4 maximum |
| IRIG-B Time Code (option) | 0 to 1, in/out |

## Pulse Output Characteristics:

| | |
|---|---|
| Output Levels: | |
| $V_{OL}$ | -2 V to 0.99 V into 50 ohms |
| $V_{OH}$ | -2 V to 5 V into 50 ohms |
| Resolution | 10 mV |
| Rise/Fall Time | 5 nsec at 5.0 Vp:p |
| Programmable | Yes |
| Level Accuracy | ±2% |

## Delay Characteristics:

| | |
|---|---|
| Insertion Delay | 270 nsec |
| Programmable Range | |
| Minimum | 0 nsec (+ insertion delay) |
| Maximum | 4 msec (+ insertion delay) |
| Resolution | 1 nsec |
| Accuracy | ±2 nsec |
| Max Jitter, trigger to output | ±2 nsec |

## Pulse Characteristics:

| | |
|---|---|
| Width | 50 nsec to 1msec |
| Width Control Resolution | 1 nsec |
| Width Control Accuracy | ±2 nsec |

## Pulse Trigger (per channel):

| | |
|---|---|
| Internal Trigger Generator (one per system) | Programmable |
| Range | 100 Hz to 1 MHz |
| VXI TTL | (0:7) |
| External: | |
| Max. Input Range | -2 V to +6 V |
| Threshold Range | -2 V to +5 V |
| Threshold Resolution | 10 mV |
| Input Impedance | 50 ohms or 10k ohms, selectable |
| Min. Trigger Width | 20 nsec |
| Polarity | Rising/falling, selectable |

## Table Memory (per channel):

| | |
|---|---|
| Size | 500,000 entries |
| Scan Rate | 100 Hz to 1 MHz |
| Table Trigger | |
| Internal Trigger Gen: | Programmable (one per channel) |
| Range | 100 Hz to 1 MHz |
| VXI TTL | (0:7) |
| External: | |
| Max. Input Range | -2 V to +6 V |
| Threshold Range | -2 V to +5 V |
| Threshold Resolution | 10 mV |
| Input Impedance | 50 ohms or 10K ohms, selectable |
| Min. Trigger Width | 20 nsec |
| Polarity | Rising/falling, selectable |

## IRIG-B Time Stamp (Option):

| | |
|---|---|
| Continuous | Yes |
| Time Stamp Storage | 64K event FIFO |
| Time Stamp Accuracy | 1 µsec |
| FIFO Status | Interrupt driven, register polling |
| Spooling | DDG FIFO, host RAM, host hard drive |

## Front Panel:

Inputs:
10 MHz Ref In, Pulse Trigger (Ch1-4), Table Trigger (Ch1-4), IRIG-B Time Code

Outputs:
10 MHz Ref Out, Pulse (Ch 1-4), IRIG-B Phase Clock

LED Indicators:
Power, Access,
Ch1-4: Armed, Pulse Active

Connectors: SMB

# VXI Specifications

## Interface Compatibility:

| | |
|---|---|
| Size | C-size, single slot |
| Type | Register-based, servant |
| Logical Address | Static or dynamic |
| Interrupt Level | Programmable 1-7 |
| Triggers | TTLTRG 0-7 |

## Power Requirements:

| | DDG400 | | DDG200 | |
|---|---|---|---|---|
| +5.0 Volts | 6.5 A | 32.5 W | 6.4 A | 32.0 W |
| -5.2 Volts | 2.5 A | 13.0 W | - n/a - | - n/a - |
| +12.0 Volts | 1.2 A | 14.4 W | 1.0 A | 12.0 W |
| -12.0 Volts | 0.8 A | 9.6 W | 0.7 A | 8.4 W |
| -2.0 Volts | 0.9 A | 1.8 W | - n/a - | - n/a - |
| +24.0 Volts | 0.22 A | 5.3 W | - n/a - | - n/a - |
| | | -------- | | -------- |
| Total Power | | 76.6 W | | 52.4 W |

## Cooling Requirements:

| | |
|---|---|
| Per Slot Average | 77 W (DDG400)<br>52 W (DDG200) |
| Airflow (DDG400) | 6L/sec @ 0.38mm water pressure for 10° C temperature rise (typ) |
| Airflow (DDG200) | 4L/sec @ 0.38mm water pressure for 10° C temperature rise (typ) |

## Environmental Specifications:

| | |
|---|---|
| Temperature | Storage = -40° C to +75° C<br>Operating = 0° C to 45° C |
| Humidity | 5% to 95% relative, noncondensing |

## Software Drivers:

VXI Plug & Play, IVI Compliant

* Specifications subject to change without notice.

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