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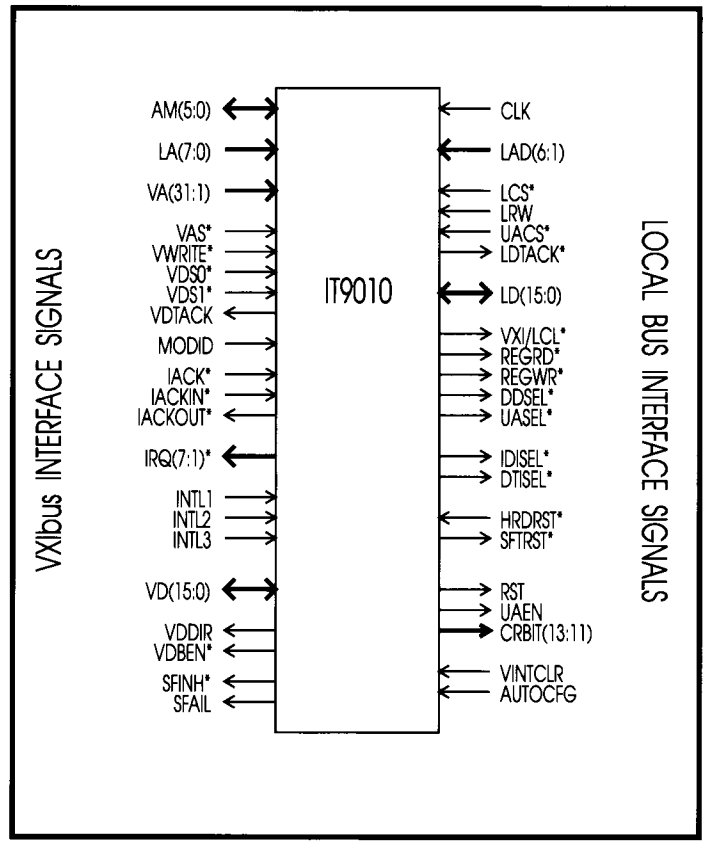
interface TECHNOLOGY

IT9010 VXIntegrator
Register-Based Interface Chip

FEATURES

- Interrupter Capability
- Dynamic or Static Configuration
- A24/A32 Register Support
- Device Dependant Register Support
- Integration of the following VXI registers:
  - Programmable Logical Address
  - ID
  - Device Type
  - Offset
  - Status/Control
  - Status/ID (used for Interrupts)
- Power dissipation < 400mW @ 5V
- Surface-mount or PGA package

SUPPORTS D32

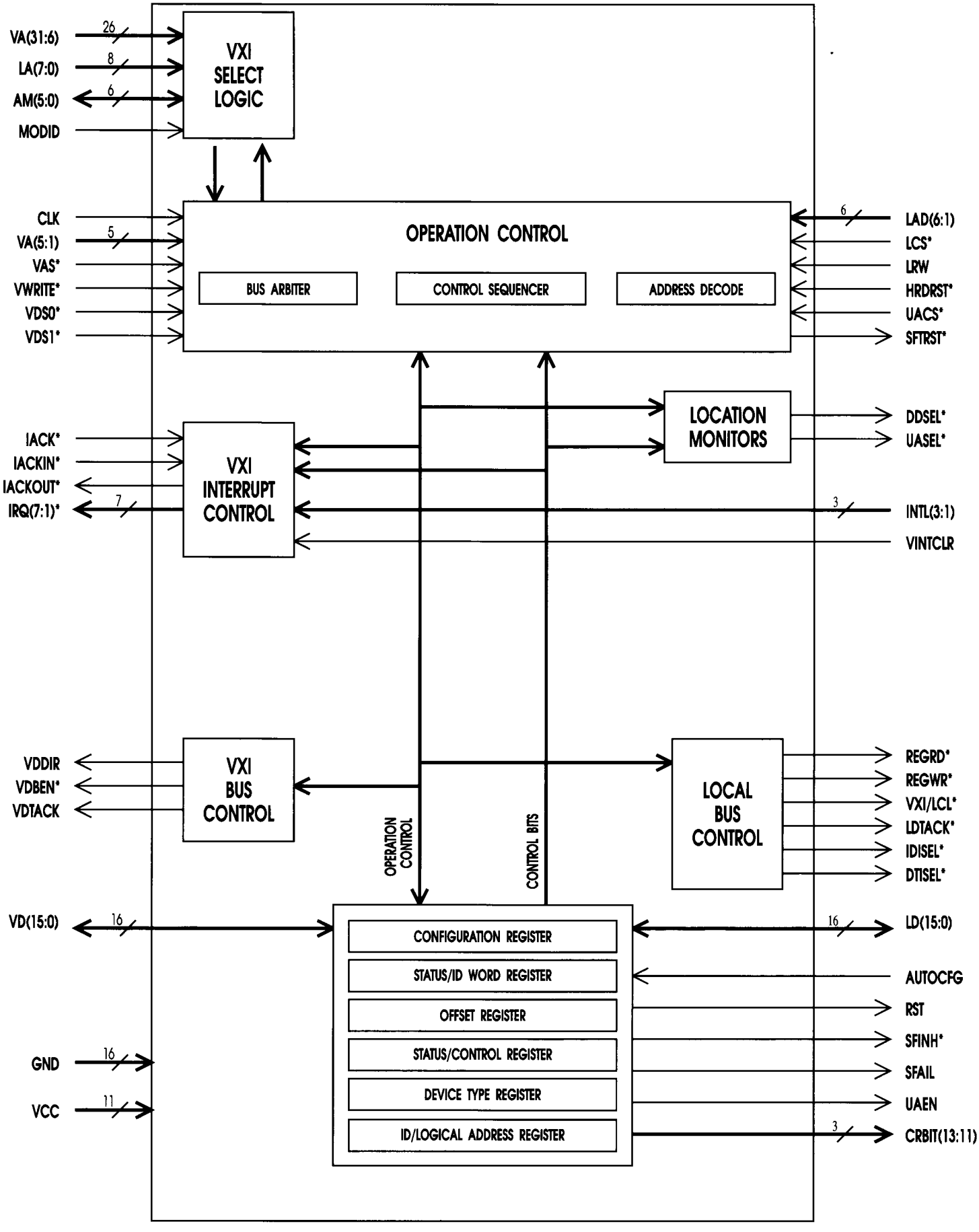


DESCRIPTION

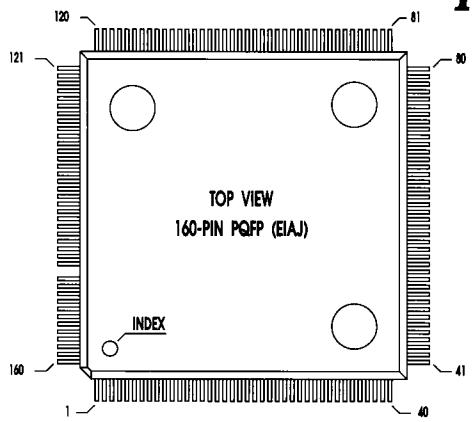
The IT9010 register-based Interface chip integrates the required VXIbus registers, VXIbus address decoding, and VXI/Local bus arbitration into a single chip. This allows the designer to implement a VXIbus register-based interface with a minimum of support hardware, complexity, and board space. MODID support allows the chip to implement either Static or Dynamic logical address configuration. The IT9010 has the capability of decoding all 31 VXI bus address lines (A1-A31), allowing the user to configure the chip as either an A24 device or an A32 device. An on-board offset register will automatically map to, and decode, the correct VXI bus address lines as determined by the configured device type (A24 or A32) and the amount of A24/A32 memory requested. Other features of the IT9010 include interrupter capability, A16 Device Dependent register decoding, and automatic configuration of the ID and Device Type registers from external switches, allowing the IT9010 to be programmed with or without a microprocessor.



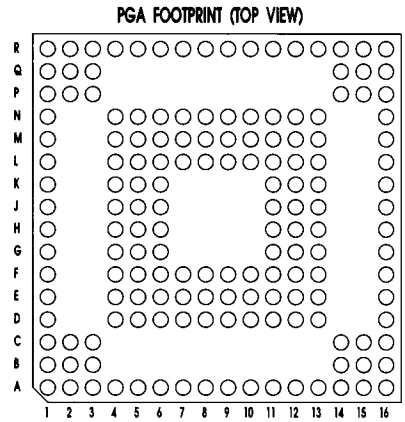
IT9010 FUNCTIONAL BLOCK DIAGRAM



PINOUT



PQFP



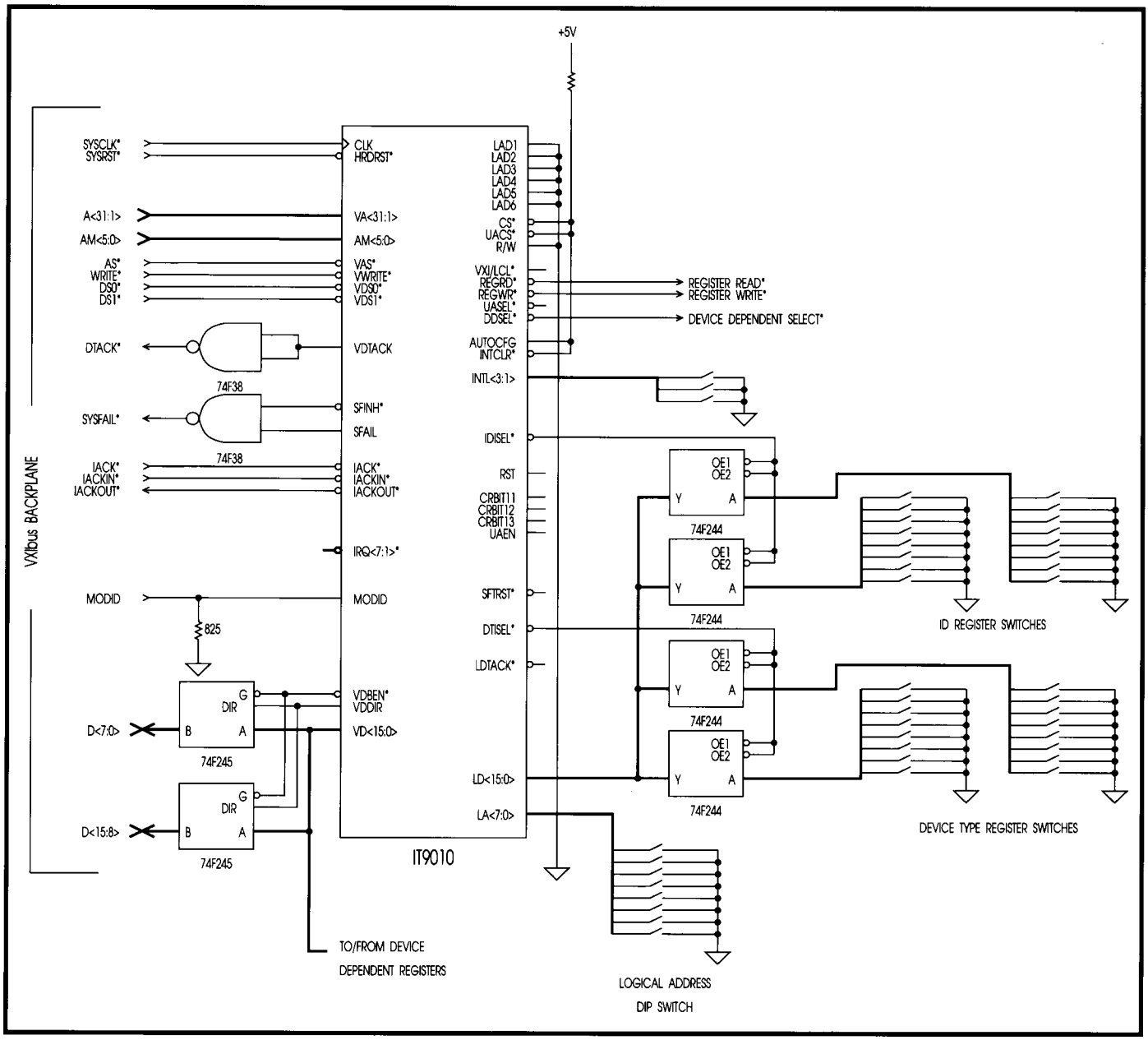
PGA

PIN	NAME	TYPE	PIN	NAME	TYPE	PIN	NAME	TYPE	PIN	NAME	TYPE
1(B3)	GND	—	41(C15)	GND	—	81(Q.14)	GND	—	121(P2)	GND	—
2(A1)	LD8	I/O	42(A16)	IRQ7*	O	82(R16)	VDS1*	I	122(R1)	VD7	I/O
3(A2)	LD9	I/O	43(B16)	IRQ6*	O	83(R15)	VDS0*	I	123(Q1)	VD6	I/O
4(A3)	LD10	I/O	44(C16)	IRQ5*	O	84(R14)	VAS*	I	124(P1)	VD5	I//O
5(F6)	LD11	I/O	45(F11)	IRQ4*	O	85(L11)	VA1	I	125(L6)	VD4	I/O
6(E5)	LD12	I/O	46(E12)	IRQ3*	O	86(M12)	VA2	I	126(M5)	VD3	I/O
7(A4)	LD13	I/O	47(D16)	IRQ2*	O	87(R13)	VA3	I	127(N1)	VD2	I/O
8(D5)	LD14	I/O	48(E13)	IRQ1*	O	88(N12)	VA4	I	128(M4)	VD1	I/O
9(A5)	LD15	I/O	49(E16)	CRBIT13	O	89(R12)	VA5	I	129(M1)	VD0	I/O
10(E6)	GND	—	50(F12)	GND	—	90(M11)	GND	—	130(L5)	GND	—
11(A6)	LA0	I(PU)	51(F16)	CRBIT12	O	91(R11)	VA6	I	131(L1)	VDBEN*	O
12(D6)	LA1	I(PU)	52(F13)	CRBIT11	O	92(N11)	VA7	I	132(L4)	VDDIR	O
13(F7)	LA2	I(PU)	53(G11)	-NC-	—	93(L10)	VA8	I	133(K6)	AM5	I
14(A7)	LA3	I(PU)	54(G16)	VINTCLR	I	94(R10)	VA9	I	134(K1)	AM4	I
15(D7)	LA4	I(PU)	55(G13)	UAEN	O	95(N10)	VA10	I	135(K4)	AM3	I
16(E7)	LA5	I(PU)	56(G12)	SFAIL	O	96(M10)	VA11	I	136(K5)	AM2	I
17(F8)	LA6	I(PU)	57(H11)	SFINH*	O	97(L9)	VA12	I	137(J6)	AM1	I
18(A8)	LA7	I(PU)	58(H16)	VDTACK	O	98(R9)	VA13	I	138(J1)	AM0	I
19(D8)	UASEL*	O	59(H13)	GND	—	99(N9)	VA14	I	139(J4)	GND	—
20(E8)	VCC	—	60(H12)	VCC	—	100(M9)	VCC	—	140(J5)	VCC	—
21(F9)	RST	O	61(J11)	GND	—	101(L8)	VA15	I	141(H6)	AUTOCFG	I
22(A9)	DDSEL*	O	62(J16)	MODID	I	102(R8)	VA16	I	142(H1)	INTL3	I
23(D9)	IDISEL*	O	63(J13)	-NC-	—	103(N8)	VA17	I	143(H4)	INTL2	I
24(E9)	DTISEL*	O	64(J12)	-NC-	—	104(M8)	VA18	I	144(H5)	INTL1	I
25(F10)	UACS*	I	65(K11)	VCC	—	105(L7)	VA19	I	145(G6)	HRDRST*	I
26(A10)	VXI/LCL*	O	66(K16)	-NC-	—	106(R7)	VA20	I	146(G1)	VCC	—
27(D10)	REGWR*	O	67(K13)	VA31	I	107(N7)	VA21	I	147(G4)	SFTRST*	O(H)
28(E10)	REGRD*	O	68(K12)	VA30	I	108(M7)	VA22	I	148(G5)	-NC-	—
29(D11)	LDTACK*	O	69(L13)	VA29	I	109(N6)	VA23	I	149(F4)	CLK	I
30(A11)	GND	—	70(L16)	GND	—	110(R6)	GND	—	150(F1)	GND	—
31(E11)	LCS*	I	71(L12)	VA28	I	111(M6)	GND	—	151(F5)	VCC	—
32(A12)	LRW	I	72(M16)	VA27	I	112(R5)	VD15	I/O	152(E1)	LD0	I/O
33(D12)	LAD6	I	73(M13)	VA26	I	113(N5)	VD14	I/O	153(E4)	LD1	I/O
34(A13)	LAD5	I	74(N16)	VA25	I	114(R4)	VD13	I/O	154(D1)	LD2	I/O
35(D13)	LAD4	I	75(N13)	VA24	I	115(N4)	VD12	I/O	155(D4)	LD3	I/O
36(A14)	LAD3	I	76(P16)	IACKIN*	I	116(R3)	VD11	I/O	156(C1)	LD4	I/O
37(C14)	LAD2	I	77(P14)	IACK*	I	117(P3)	VD10	I/O	157(C3)	LD5	I/O
38(A15)	LAD1	I	78(Q16)	IACKOUT*	O(M)	118(R2)	VD9	I/O	158(B1)	LD6	I/O
39(B15)	-NC-	—	79(Q15)	VWRITE*	I	119(Q2)	VD8	I/O	159(B2)	LD7	I/O
40(B14)	VCC	—	80(P15)	VCC	—	120(Q3)	VCC	—	160(C2)	VCC	—

PIN: PQFP (PGA)

I = Standard Input
I(PU) = Input with Pullup

O = Standard Output (I_{OL} = 3.2 mA, I_{OH} = -2 mA)
O(M) = Medium Drive Output (I_{OL} = 8 mA, I_{OH} = -2 mA)
O(H) = High Drive Output (I_{OL} = 24 mA, I_{OH} = -8 mA)
I/O = Bidirectional (I_{OL} = 3.2 mA, I_{OH} = -2 mA)



REGISTER–BASED INTERFACE SCHEMATIC EXAMPLE

ORDERING INFORMATION

IT9010–PQFP	VXIntegrator 159–Pin Plastic Quad Flatpack.
IT9010–PGA	VXIntegrator PQFP Mounted on a 160–Pin Pin Grid Array Adaptor.

interface TECHNOLOGY

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