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RS-4004

20 MHz PATTERN GENERATOR/ANALYZER

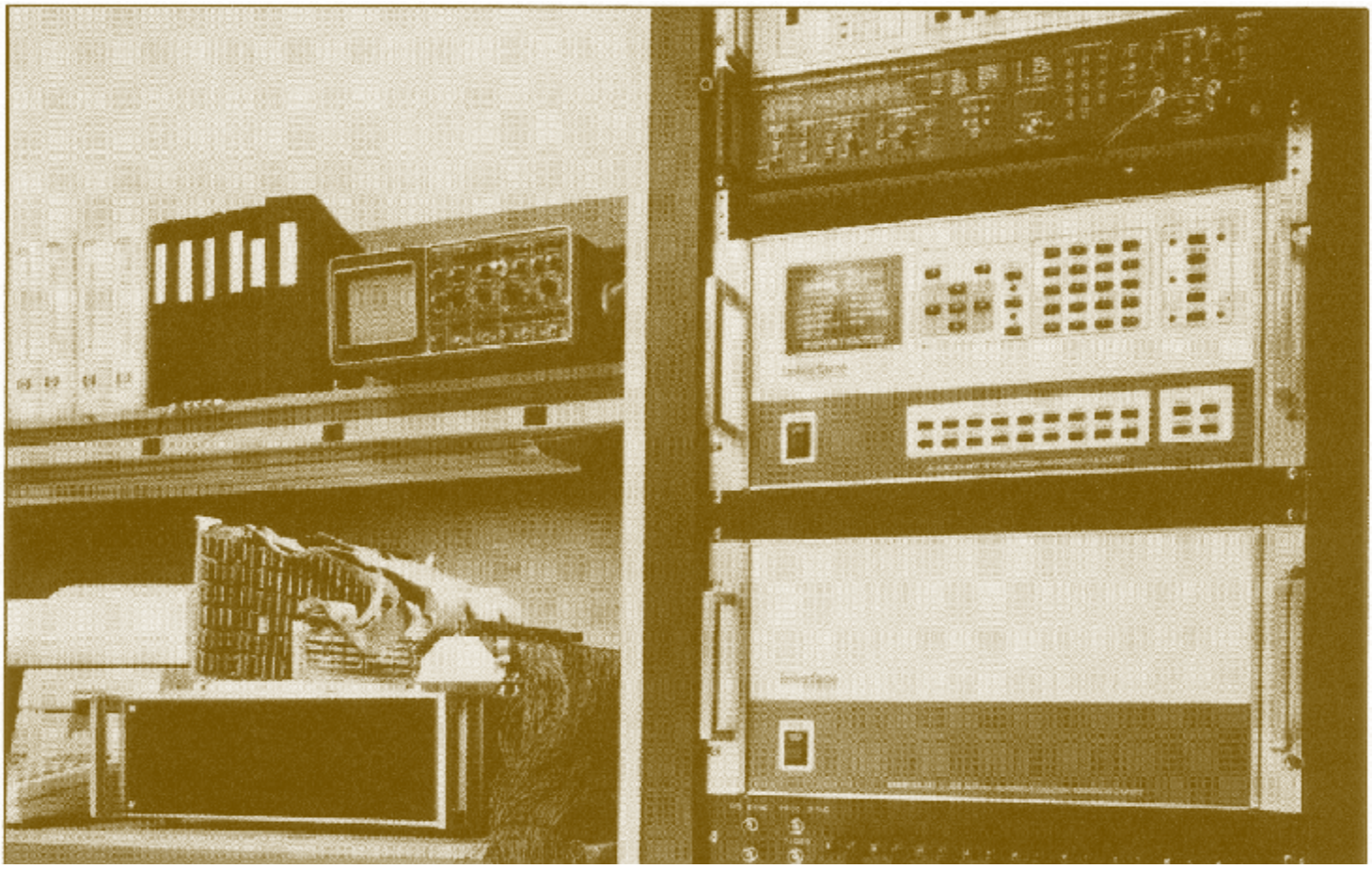
A TECHNICAL GUIDE TO DIGITAL STIMULUS/RESPONSE TESTING



interface
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INSTRUMENTS FOR DIGITAL STIMULUS/RESPONSE TESTING



Until now, if you wanted to perform functional digital testing you had to use a variety of devices which probably didn't meet your needs: an expensive PC card tester, a system "hot mock-up," or even a special purpose tester designed and built in-house.

Now there is a genuine alternative: The RS-4004 20 MHz Pattern Generator/Analyzer from Interface Technology. The RS-4004 combines the best of an Automated Test Equipment (ATE) system with the smaller size and cost of an instrument.

Now you have the capability to develop the test you need for your application. You can test complex digital circuits and assemblies at their operating speed, providing functional verification. You can design test setups using a wide range of I/O signals, such as discrete control lines, bidirectional data lines, sync lines, clocks, and triggers. Data I/O lines can be configured modularly using plug-in I/O cards, allowing up to 512 data channels. A memory depth of 4 Kbits per channel is standard.

A wide variety of discrete signal lines help you set up and control your Unit Under Test (UUT). For example, input flag lines from the UUT can be checked and used to branch on and change output conditions.

For functional testing, stimulus patterns may be generated and the UUT response accepted and compared against expected results. This can take place at a 10 MHz data rate, while either output pattern generation or data pattern recording can take place at 20 MHz.

Stimulus/response testing isn't all these instruments do. They can also be used as multiple table logic recorders, as multiple channel timing simulators, or as intelligent pattern generators. They can even verify logic designs of gate arrays, PALs or VLSI devices.

The RS-4004 effectively and economically solves your high speed digital testing problems.

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GENERAL DESCRIPTION

The RS-4004 employs a dual microprocessor architecture and modular, plug-in I/O cards to provide high speed pattern generation and test capabilities. The System CPU (SCPU) is a Motorola 68000 microprocessor and the Bit Slice Microprocessor (BSM) is an AMD 2901. The I/O cards provide flexible pattern generation, recording and testing capabilities with pattern memory up to 4K bits per channel. Several standard remote control interfaces are also provided. Figure 1 is a simplified block diagram of the instrument architecture.

SYSTEM ARCHITECTURE

The System CPU handles all interaction between the operator, the instrument's front panel and the remote interfaces. It also communicates with the BSM and the I/O cards to handle programming, data entry, data recall, status, and run control.

The System CPU manages all menu entry and MACRO language programming, thus simplifying front panel operation.

The Bit Slice Microprocessor (BSM) contains RAM, which is programmed for each specific test operation. To facilitate this programming requirement, the BSM has four levels of nested subroutines, four general purpose internal counters, a 16-bit arithmetic logic accumulator with eight working registers, 16 general purpose program flags, and 40 discrete flag and pulse lines. These discrete signal lines can be interfaced to the unit under test to provide handshake, control, and device status. During operation, the BSM executes a MACRO language instruction every 200 nanoseconds. The BSM is also responsible for controlling the word generator/timing simulator section. Here it provides the selection of the clock rate, the pattern memory locations to output, the number of pattern loops to output, and the start/stop conditions. The word generator section provides addressing logic required by the data I/O cards, which contain the actual data memories for testing, generating, or recording data patterns.

Standard features of the RS-4004 include multiple clock signals, synchronizing signals, and a composite video output. Synchronizing signals include external trigger, program address sync output and word pattern sync output. Pulse control lines allow you to force the output data high or low enabling you to emulate RZ data. Force tristate lines allow you to enable the high impedance state on groups of output channels. This can also be accomplished on a line-by-line basis using the programmable tristate memory. IEEE 488, RS-232C, and a high speed 16-bit parallel interface are standard remote control interfaces.

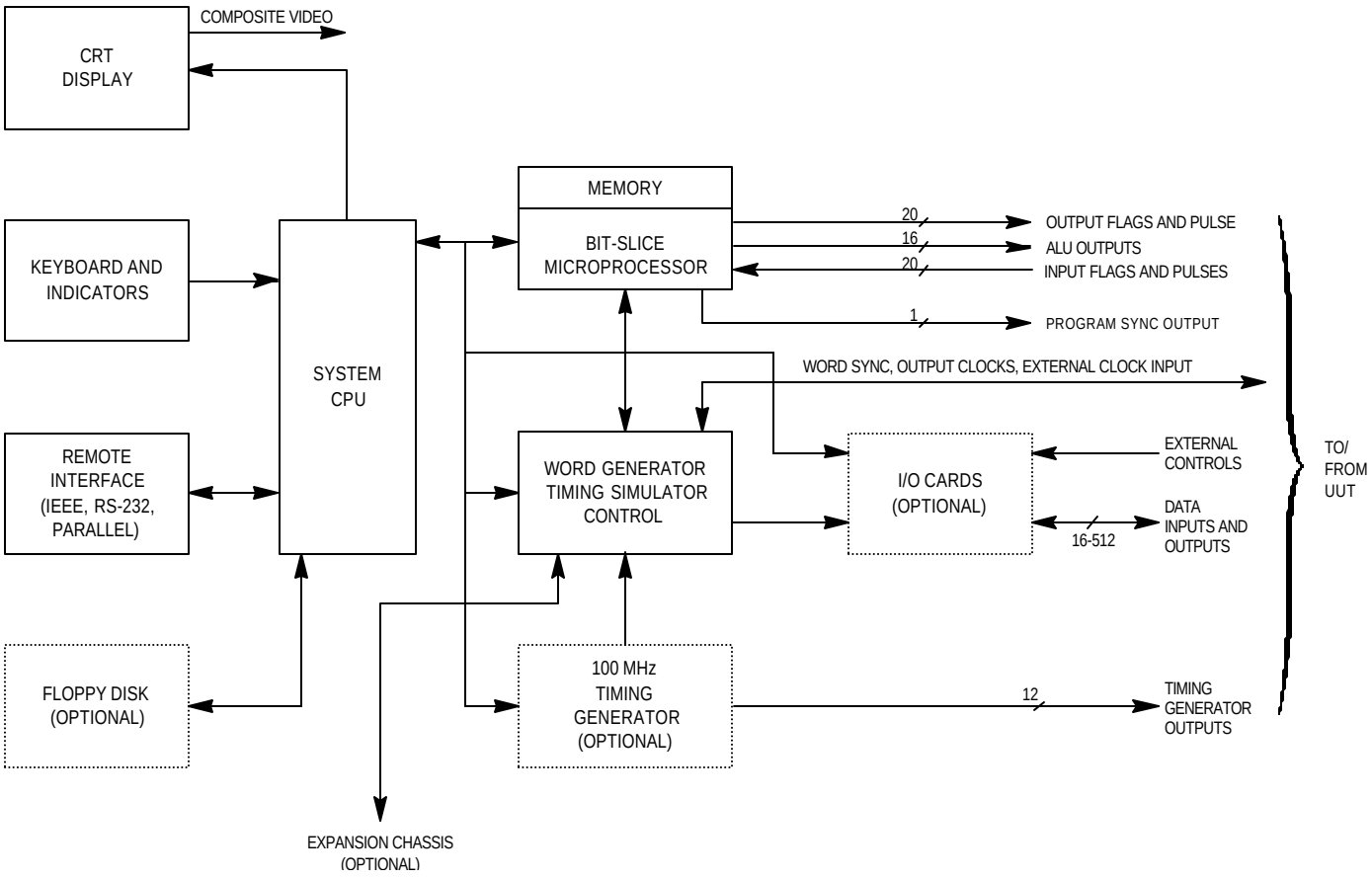


Figure 1. Instrument Block Diagram.

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I/O OPTIONS INCREASE SYSTEM FLEXIBILITY

A wide variety of I/O card options are available. These cards determine the channel width, memory depth, and memory type. There are four types of I/O cards: 16-channel I/O, 32-channel I/O, 64 channel input, and 64-channel output. Memory depth of 4K bits per channel is provided, see Fig 2.

All card types provide complete measurement capability at 10 MHz. Additionally, some operating modes may allow stimulus or response data rates up to 20 MHz.

I/O CARD OPTIONS

	16 Channel I/O		32 Channel I/O		64 Channel Input		64 Channel Output	
Mainframe	Depth	Capability	Depth	Capability	Depth	Capability	Depth	Capability
RS-4004	4K	output tristate expected mask record	4K	output tristate record	4K	 record	4K	output tristate

Figure 2: I/O Options -- Memory Depth and Capability

64-CHANNEL OUTPUT TRISTATE CARD

The 64-Channel Output Tristate Card (see Fig 3) contains 64 parallel channels of output arranged in four groups of 16 channels. Each channel has a memory depth of 4K bits. Individual tristate control memories can place outputs in a tristate, or high impedance state, on a channel-by-channel and clock-by-clock basis. The RS-4004 provides only the ability to externally force tristate outputs on groups of 16 channels. Used in a serial mode, four serial bit streams may be generated, each having 64K bits per channel.

64-CHANNEL INPUT CARD

The 64-Channel Input Card (see Fig 4) provides 64 input record channels organized in four groups of 16 channels. Each channel has a memory depth of 4K bits. In serial mode, four channels of record data are provided, each 64K bits deep. Additionally, the RS-4004 allows you to selectively write-enable each channel bank, which would allow 16 channels of record data, each 16K bits deep.

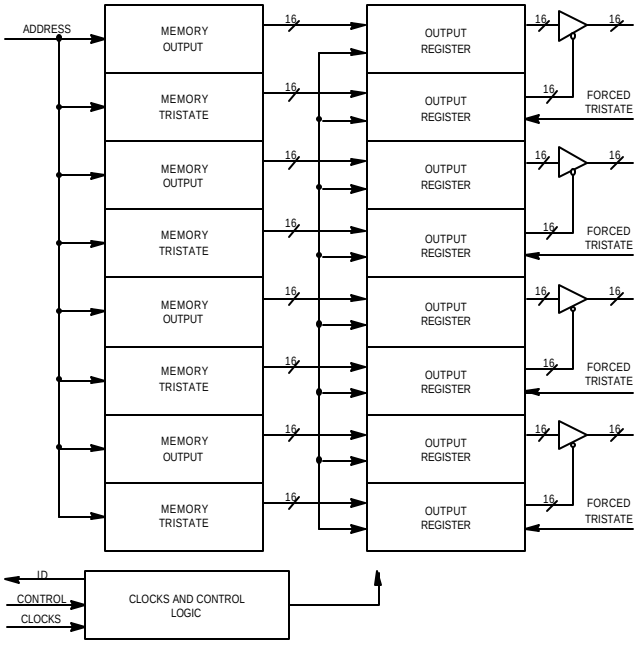


Figure 3: 64-Channel Tristate Output Card

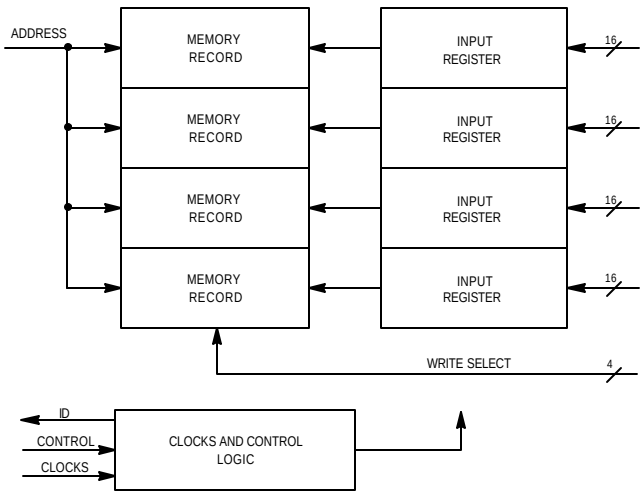


Figure 4: 64-Channel Input Card

32-CHANNEL TRISTATE I/O CARD

The 32-Channel Tristate I/O Card (see Fig 5) combines both input and output with 4K bits of memory per channel. Thirty-two channels are dedicated to output with individual tristate control memories. This additional set of memories permits chanel-to-channel and state-to-state control over tristate output. This means that you can now define when a channel is to output data and when it is to be in the high impedance (tristate) mode, see Fig 6 for an example). Thirty-two input channels permit recording of UUT response data.

Bidirectional capability is achieved by connecting the output channels to the input channels. This allows the UUT to be driven by the RS-4004 on one cycle and on the next cycle to receive data on the same channel.

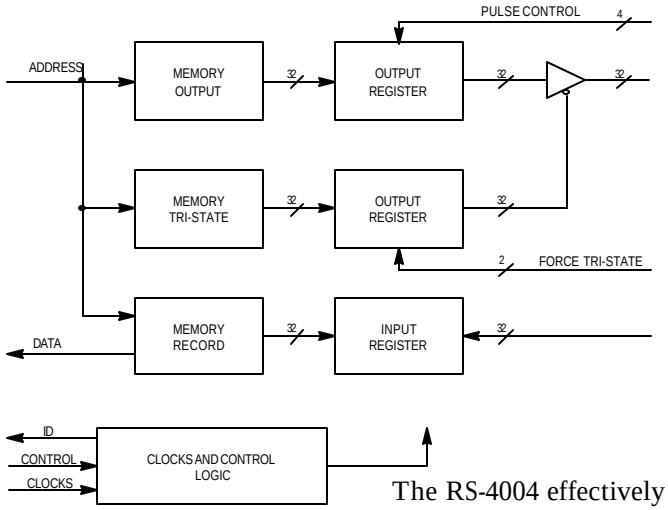


Figure 5: 32-Channel Tristate I/O Card

16-CHANNEL UNIVERSAL I/O CARD

The 16-Channel Universal I/O Card (see Fig 7) is also a combination input/output card with 4K bits of memory per channel. This card provides a real-time digital comparison capability through the use of expected value memories. The expected value memory contains data that the user expects from the UUT in response to the stimulus provided by the RS-4004. A mask memory allows bits to be excluded from the compare function. You now have the capability to stimulate the unit under test, receive response data, compare it against expected data, mask off data to be ignored, and declare a pass or fail. Tristate memory also allows this card to be used for bidirectional applications.

The 16-Channel I/O Card provides other functions. It can compare and store errors or simply sample and store raw UUT response data. It also may be programmed for edge sample, edge compare or window compare modes. In the edge sample mode, the edge of the sample clock (either internal or external) determines when the input data is sampled. In the edge compare mode, the edge of the sample clock determines when the comparison is performed. In window compare mode, input data must remain stable for the entire window width (sample clock duration). Any change in state during the window will cause an error indication. The error data will be recorded in the record memory. The 16-Channel I/O Card can also be used as a single serial channel with 64K bits of memory.

The RS-4004 effectively and economically solves your high speed digital testing problems.

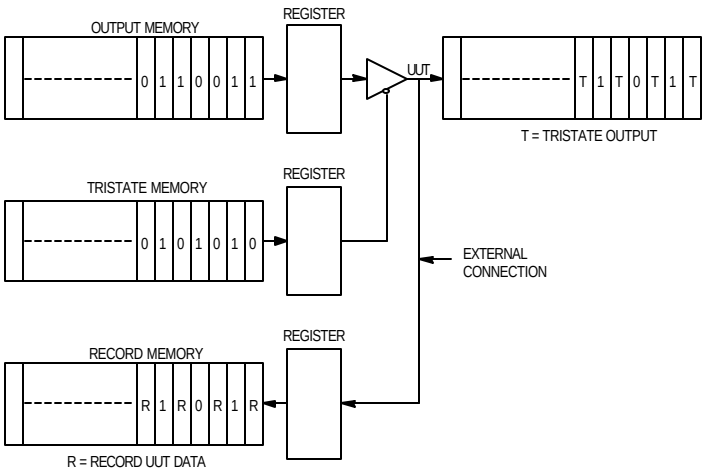


Figure 6: Tristate Output for Bidirectionality

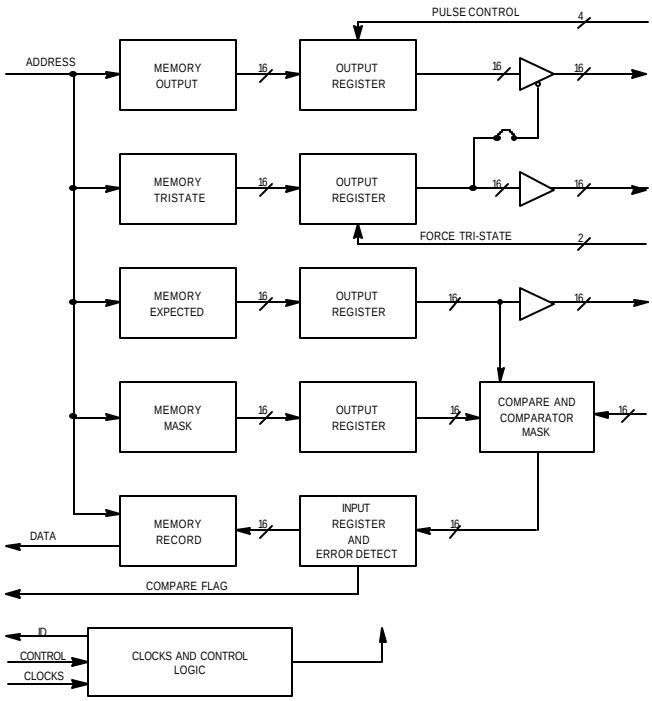


Figure 7: 16-Channel Universal I/O Card

OPERATIONAL OVERVIEW

100 MHz TIMING GENERATOR ALLOWS HIGH RESOLUTION SAMPLING

The optional 100 MHz TIMING GENERATOR module serves two function. It may be used as a 12-channel, 256-state, timing simulator or as a high resolution, 10 nanosecond sample clock for test purposes. See figure 8, all 12 channels are available for external use. The user may choose, via program control, to use channels 0, 1, 2 and 3 (which are connected internally) for output clocking and input sampling. Channels utilized externally may represent clocks, strobes, enables, or timing signals to the UUT. They are particularly useful for strobing patterns into the unit under test.

The Timing Generator may be run independently of the word generator. In addition, multiple first and last addresses can be used to segment the data memory. Timing generator operation in the RS-4004, however, is coupled with the word generator.

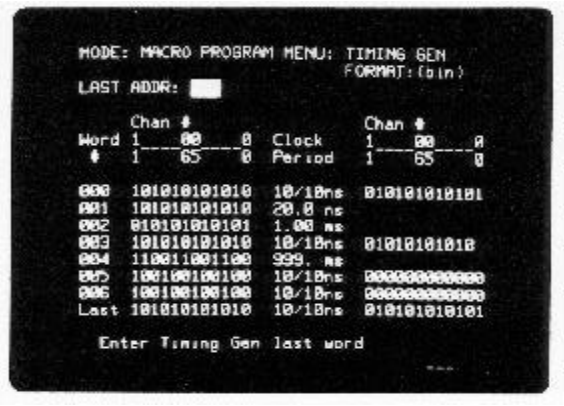


Figure 8: 10 ns Resolution Timing Generator.

THE SYSTEM

Modular design of the RS-4004 permits you to configure a system to meet your particular needs. The basic mainframe has five option card slots. One slot is dedicated to the 100 MHz Timing Generation option. If more than four I/O cards are desired, then up to two expansion chassis may be added, providing a maximum of 12 additional I/O card slots as shown in figure 9. Various I/O card options may be intermixed and field installation of cards makes expansion easy.

An example of memory organization in an RS-4004 system configured with one of each of the available I/O cards is shown in Figure 10. System configuration may extend up to 512 parallel channels. In addition to the option I/O cards, there are many other I/O signals that are standard, such as discrete control, flag, Arithmetic Logic Unit (ALU), and clock lines.

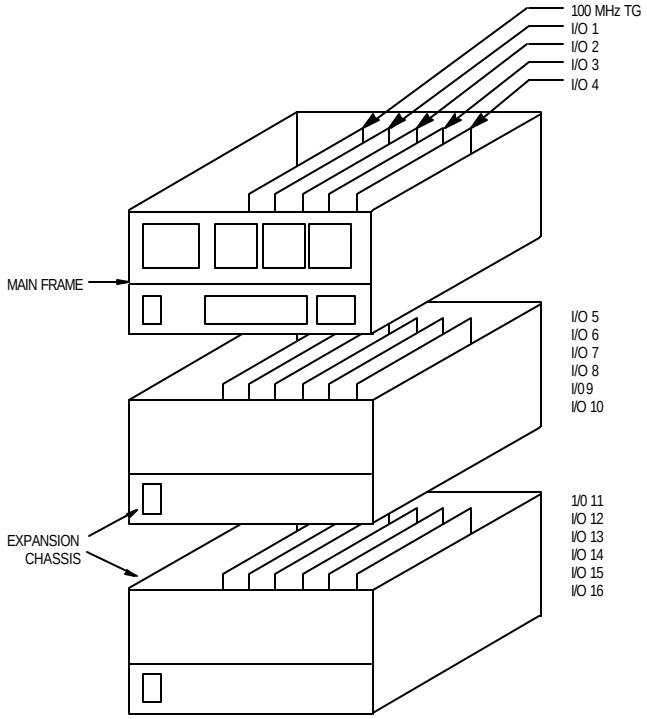


Figure 9: Expansion Chassis Configuration.

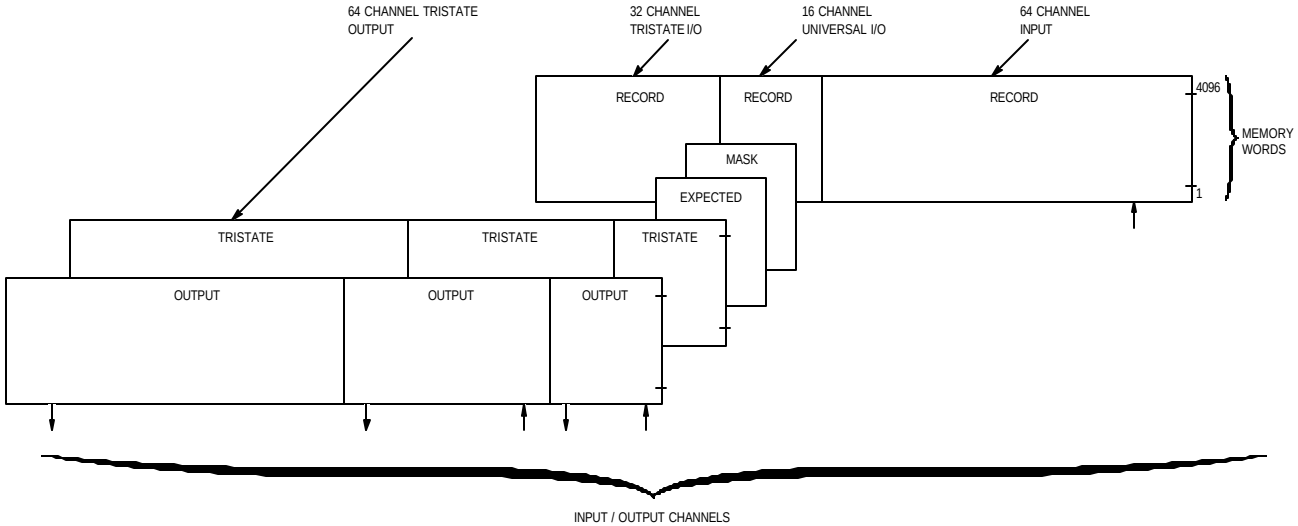


Figure 10: Memory Organization for I/O Cards.

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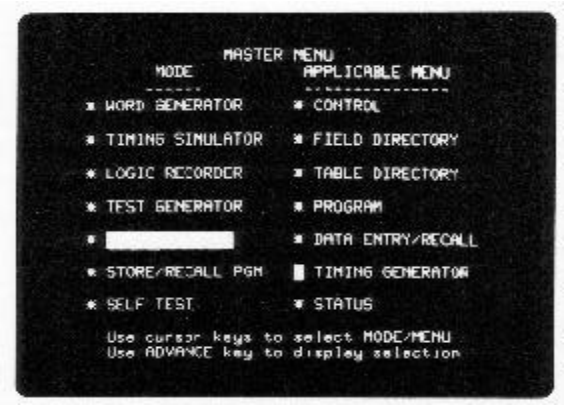


Figure 11: RS-4004 -- Operating Modes.



Figure 12: Word Generator Mode -- Typical Setup Menu.

MODES OF OPERATION

Setup, data entry and data recall tasks are simplified through the use of self-prompting menus. The instrument is divided into several operating modes, each with its associated menus, which present parameter questions and choices. The available modes and a typical setup menu for the word generator mode are shown in Figures 11 and 12.

For the WORD GENERATOR, TIMING SIMULATOR, LOGIC RECORDER and TEST GENERATOR modes of operation, you need only enter setup parameters and data patterns. Detailed MACRO instructions need not be entered as they are assembled for you by the System CPU using the parameters entered via the menus.

The SELF TEST mode allows you to perform confidence testing and fault isolation of the instrument hardware.

FIELD AND TABLE CONCEPTS

Field assignments allow you to define from 1-32 channels with an assigned name which can represent a logical function in the unit under test such as an address bus, a data bus or a control bus. You may assign the channels in the specified field to any pin on the rear panel. This eliminates the complex external wiring usually associated with testing a large number of parallel digital signals. The pin assignment feature can also eliminate the need for a switching matrix since the switching can now be done in the System CPU software.

Table assignments let you divide the available memory into smaller segments or tables. Tables may be output in any sequence desired and each table may be repeated as many as 4096 times. For example, a table may represent a memory write cycle which needs to be repeated 4096 times, or a simple clocking waveform for a shift register, or a header pattern for a communications link that is sent once each data frame. All such tables may be though of as data pattern subroutines which can be called and repeated. Figures 13 and 14 show an example of table assignments and output sequencing.

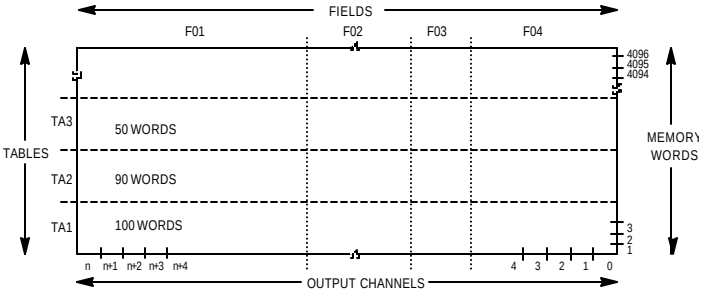


Figure 13: Field and Table Concepts

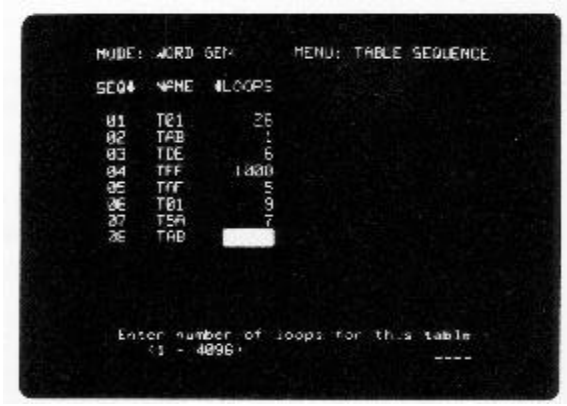


Figure 14: Word Generator Mode -- Table Sequencing

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MACRO PROGRAMMING ADDS ADDITIONAL POWER

The MACRO mode allows you to create an application-specific test sequence program. Even at this detailed level of operation, the System CPU assists you in the creation of the final MACRO instruction program. The MACRO instructions as shown are programmed into the instrument via special function keys on the front panel. Operator entry is simplified because English syntax is presented rather than assembly level code.

SAMPLE MACRO PROGRAM

Prog. Macro-Instruction syntax

00 FLAG STR OUTBITS 0000000000000000
01 DEF FST ADDR AT 0000
02 DEF LST ADDR AT 0100 01 SHIFTS
03 DEF CLK SRCE PERIOD OF 1 uS
04 FETCH ADDR 0000
05 IF INFLAG 5 TRUE GOTO 05
06 IF INFLAG 5 FALSE GOTO 06
07 START WORDGEN IMMED 0128 LOOPS
08 FLAG SET OUTBITS XXXXXXXXXXXX1XXX
09 IF INFLAG 6 TRUE GOTO 01
10 FLAG STR OUTBITS 0000000000010000
11 GOTO 12
12 FLAG CLR OUTBITS XXXXXXXXXXX1XXXX
13 HALT PGM-ONLY

MACRO PROGRAM EXPLANATION

00 Sets output flags to initial conditions
01 Sets the first memory address register of the word generator sequence to zero (0)
02 Sets the last memory address register of the word generator sequence to 100
03 Defines the word generator clock source to be the internal period clock with a period of 1 microsecond
04 Causes the contents of the word generator address 0 to be placed on the output lines available at the rear panel
05 Tests the state of input flag line 5, will stay at this programm address until flag 5 is false
06 Tests the state of input flag line 5, will stay at this program address until flag 5 is true
07 The word generator is started without needing to wait for a trigger, the word generator will loop from address 0 to address 100 a total of 128 times
08 The set function will set to a logic high only outflag 3
09 Tests the state of input flag line 6, if true jumps back to program address 01 and repeats the pattern
10 Sets output flag 3 to a logic low and output flag 4 to a logic high
11 Delays program execution for 200 ns
12 Sets output flag 4 to a logic low
13 Stops program execution

RS-4004 SERIES CONDENSED MACRO INSTRUCTION SET

1. **IF** Branch (jump) to the specified address if the condition being tested is true. Conditions being tested could be sense bits, input flags, input pulses, word generator status, comparison error, loop counter status, etc.

2. **GOTO** Branch (jump) to the specified address, unconditionally.

3. **GOSUB** Branch (jump) to the specified subroutine address.

4. **RTN SUB** Return from subroutine to program address plus one.

5. **LOOP** Define loop counter values from1 through 64K, for any of the available four loop counters.

6. **END LOOP** Defines the last instruction in the program loop, and also decrements specified loop counter.

7. **DELAY** Define a pause or delay in program execution with 200-nanosecond increments.

8. **FLAG** Define the status (high or low) of the sixteen output flag lines or define internal program flag states.

9. **ALU** Executed to create arithmetic or logical functions such as addition, subtraction, AND, OR, etc. User also has available 8 general purpose working registers in addition to the accumulator.

10. **HALT** Stops the execution of either the program, word generator, or timing generator. This can be dome in any combination or all at once.

11. **DEFINE** Define word generator and bit slice parameters, e.g., define last memory address, first memory adress, select clock source, sample mode, pulse polarity, etc.

12. **CLOCK** Bit Slice control of word generator clocking and/or comparators. Also controls output pulse line clocking.

13. **FETCH** Bit Slice control of word generator to fetch a specific word from memory to the output register and drivers.

14. **START** Bit Slice control instruction to start the word generator or timing generator.

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EDITING AND REMOTE CONTROL

The editing functions provide assistance in several ways. The FORMAT function permits data entry and pattern viewing in hex, octal or binary formats. The INSERT and DELETE keys are used to change fields, tables, pin assignments, program instructions, or to insert varous entries. The FILL function allows you to specify the filing of any of the data pattern memories with functions such as incrementing, decrementing, complementing or alternating patterns. It also allows the filling of memories with random data from a Pseudo Random Number Generator. You can specify the seed value and the number of words to fill. You can also copy from one memory type to another. For example, data from the recorded data memory can be copied to an expected data memory so that it becomes the new reference against which future recordings can be compared.

There are many applications in which users will employ the RS-4004 as the heart of a digital test system. To permit this type of use, IEEE 488, RS-232C, and a high speed 16-bit parallel interface are standard features.

All three interfaces use similar formats for control and parameter transfer. The system controller may load data and set up parameter information and determine RUN/STOP conditions. Instrument status as well as data and parameter information may be read back via the remote interfaces. The IEEE interface also provides functions such as local lockout, CRT blanking, and service requests.

FLEXIBILITY DENOTES A BROAD RANGE OF APPLICATIONS

The RS-4004 is a general purpose, programmable digital test tool. It provides unsurpassed versatility and flexibility to meet a variety of application needs. Here are some examples of its many uses:

DEVELOPMENT

- As a pattern generator for stimulating LSI and VLSI integrated circuits in characterization environments.
- As a digital timing signal and pattern generator for communication circuit breadboarding.
- As a logic state recorder with a wide number of channels for system troubleshooting and data capture.
- As a general purpose benchtop tool for testing digital circuits.

RESEARCH

- As a general purpose signal generator for experimentation in pulsed nuclear magnetic resonance, fiber optics, image processing, laser, and memory devices.
- As a timing generator for synchronization of laboratory experiments.
- As a pattern generator/tester for new integrated circuit development and materials research.
- As a phase signal generator for magnetic media research.

PRODUCTION

- As a functional tester for printed circuit cards.
- As a functional tester for black box system modules.
- As a simulator for certification and quality assurance testing.
- As a pattern generator/exerciser for burn-in applications.

FIELD/DEPOT TESTING & REPAIR

- As a functional printed circuit board or black box tester.
- As a stimulus/response unit for repair of digital equipment.

A series of applications notes and examples have been generated for the RS-4004. Simply contact the factory or your local Interface Technology representative for more information.

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SPECIFICATIONS

1. CLOCKS:

Internal oscillator: 40 MHz, frequency stability/accuracy = ±0.1%

Internal period generator (50% duty cycle, true and complement output available)	**Range**	**Resolution**
	50 ns -- 102.35 µs	50 ns
	102 µs -- 1023 µs	1 µs
	1.02 ms -- 10.23 ms	10 µs
	10.2 ms -- 102.3 ms	100 µs
	102 ms -- 1023 ms	1 ms
With 100 MHz Timing Generator:	50 ns -- 1 sec	6 digits
100 MHz Timing Generator Oscillator:	100 MHz, frequency stability/ accuracy = ± 0.005%	
External Input Clock:	20 MHz max for Word Generator Mode, 10 MHz max for Test Generator Mode; 20 ns min pulse width.	
External Window/ Sample:	10 MHz max for Test Generator Mode, synchronized to fall within period of external input clock.	
Trigger Input:	20 ns min pulse width; high to low transition triggers.	

2. CLOCK/DATA/SYNC RELATIONSHIPS:

Gated Output Clock to any data channel output: 35 ns typ.
Data channel to any other data channel, same card: 5 ns typ.
Data channel to any other data channel, same chassis: 10 ns typ.
Data channel to any other data channel, any chassis: 20 ns typ.
Gated Output clock to Table/Loop/Word Output sync: 15 ns typ.
External clock input to any data channel output: 65 ns typ.
External clock input to gated output clock: 30 ns typ.
External clock input to Table/Loop/Word Output sync: 45 ns typ.
External trigger to data channel output (Gated Output clock): 25 ns + clock period, typ.
External window/sample to gated output window: 27 ns typ.
External clock qualifier to external clock setup and hold time: 10 ns setup, 5 ns hold, typ.
Timing Generator Clock to any data channel: 70 ns typ.
Timing Generator sample clock to gated output window: 32 ns typ.
Timing Generator sample clock to gated output window: 32 ns typ.
Timing Generator skew between channels: < 5 ns.
Force tristate input to data out: 30 ns typ.
Pulse control input to data out: 35 ns typ.

3. DRIVER/RECEIVER CHARACTERISTICS

Data Output signals, Option 4003X, 4004X: user removable 100 ohm series terminated, capable of driving 2 TTL loads; with termination removed sink current = 256 mA, source current = 60 mA.
Output Clocks, Data Output Signals, Option 4006X, and Auxiliary Output Signals Option 4003X: user removable 100 ohm series terminated, capable of driving 2 TTL loads; with termination removed sink current = 128 mA, source current = 30 mA.
Output Flags, Pulses: user removable 100 ohm series terminated, capable of driving 2 TTL loads; with termination removed sink current = 64 mA, source current = 15 mA.
Output Sync: user removable 50 ohm series terminated, capable of driving 2 TTL loads; with termination removed sink current = 128 mA, source current = 30 mA.
Input Data:
Input Flag ad Pulse:
External Clocks:
External Force Tristate:
External Pulse Control:
External Trigger:
External Window:
External Clock Qualifiers:
1 STTL load with 10k ohm pull up resistor or user configurable for 100 ohm termination with resistive pad consisting of 180 ohm to +5 390 ohm to ground.

4. CRT VIDEO:

75 ohm, composite TV, vertical sync = 17 ms, horizontal sync = 60 µs.

5. MECHANICAL:

Main Chassis: 17" W x 8.75" H x 22" D, 75 lbs max.
Expansion Chassis: 17" W x 8.75" H x 22" D, 65 lbs max.

6. POWER:

Standard	110 Vac, Option 4030 for 220 Vac operation.
Main Chassis:	110 Vac ± 20%, 7A max, 50/60 Hz
	220 Vac ± 20%, 3.5A max, 50/60 Hz
Expansion Chassis:	110 Vac ± 20%, 5A max, 50/60 Hz
	220 Vac ± 20%, 2.5A max, 50/60 Hz

7. ENVIRONMENTAL:

Temperature:	0° to 40° C, all specifications valid at 25° C
Humidity:	80% relative humidity, noncondensing

8. REMOTE INTERFACES:

IEEE: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, CO, E2
RS-232C: half duplex, 110, 150, 300, 600, 1200, 2400, 4800, 9600 baud, switch selectable

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ORDERING INFORMATION

RS-4004 Mainframe. Includes interactive CRT and keyboard, 1K macro program memory, 56 discrete control and status lines, clocking and trigger lines, IEEE-488, RS-232C, and 16-bit parallel mode interfaces. Provides capability for four I/O cards plus 100 MHz timing generator card.

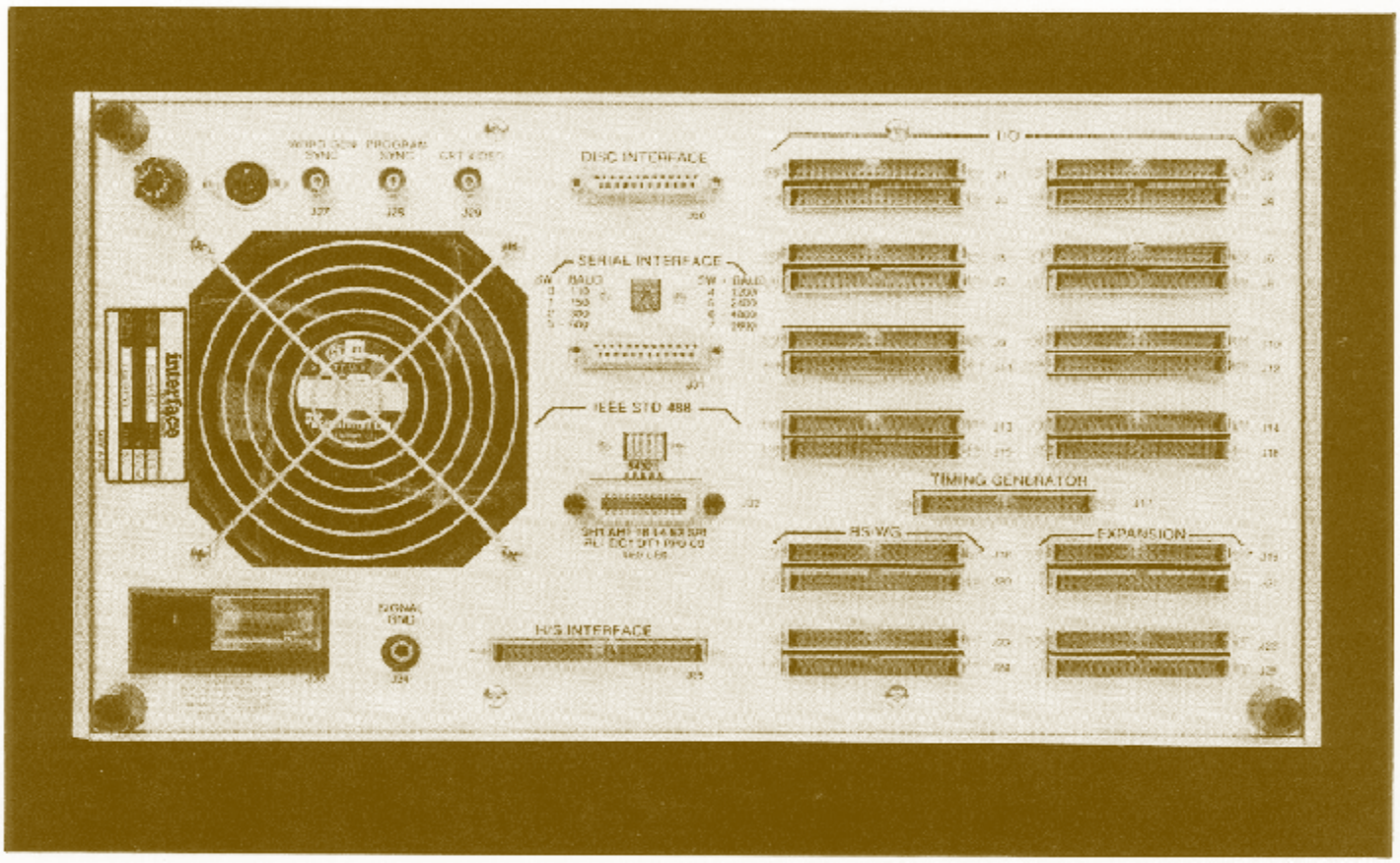
RS-4002 Expansion Chassis. Provides capability for six additional I/O cards.

Options:

40034	16 channel universal I/O card (4K)
40044	32 channel tristate I/O card (4K)
40054	64 channel input card (4K)
40064	64 channel tristate output card (4K)
40074	100 MHz timing generator card
4008	2048 word macro program memory

LOGIC CONVERSION PRODUCTS:

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