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User's Manual

SR5030 Variable Voltage I/O Module



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Record of Changes

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Rev 1.1	Mar 03, 1998	Chapter 4, pgs 4-6. Added coverage for output termination. Changed number of Fig 4-6 to Fig 4-7; added new Fig 4-6. Changed contents pages i and ii.	Factory
Rev 2.0	Mar 01, 1999	Updated and reformatted for consistency with other ITI manuals.	Factory
Chg 1.0	Sep 17, 2001	pg 1-4. Reformat specifications page.	Factory

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CHAPTER 1

General Description

Purpose of Manual

This manual provides installation and operation information for the Interface Technology SR5030 Variable Voltage I/O Module. Information contained herein is intended for use by technical personnel involved in the actual installation and operation of the subject instrument.

About This Manual

Arrangement of Contents

Information contained in this manual is arranged in four chapters, as follows:

- Chapter 1 General Information
- Chapter 2 Theory of Operation
- Chapter 3 Programming
- Chapter 4 Installation

Applicability

The information contained in this manual covers a single equipment configuration designated ***SR5030 Variable Voltage I/O Module***. Differences, if any, between this equipment and the actual equipment supplied are covered by Difference Data included at the front of this manual.

Supersedure Notice

This manual supersedes completely revision 1.1 of the SR2530 User's Manual for the subject equipment.

Equipment Description.

See Fig.1-1. The SR5030 Variable Voltage I/O Module provides 16 programmable stimulus drivers and 16 programmable response receivers for exercising various logic families. This makes it possible to test both industry standard logic circuitry (TTL, ECL, CMOS, etc.) and custom logic circuitry. The SR5030 is contained within a single C-size VXI module. Up to 20 I/O modules may be controlled by the SR5010 Timing/Control Module for a total of 320 I/O channels. Input and output pins are grouped on separate connectors, providing the most effective method of interfacing to the UUT. Bidirectional capability is accomplished by externally connecting the input pins to the output pins. Module control and status reporting are provided by the SR5010 Timing/Control module through a single CONTROL connector on the SR5030 front panel. All

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Features

- **16 Input and 16 Output Pins Per Module.**
- **64K Vectors per Channel.**
- **RAM-Backed & Algorithmic Pattern Generation.**
- **NRZ, RZ, RONE, RTC and RI Output Data Formats Supported.**
- **8 Stimulus Timing Generators & 2 Response Timing Generators Per Module.**
- **100 ps Edge Placement Resolution.**

module operating voltages are obtained from the host VXI chassis. The SR5030 can be operated in any slot within the VXI chassis, except slot-0 or slot-1, but must be located at a higher logical address than the SR5010 Control/Timing Module.

Seven I/O Memory Types

The SR5030 I/O Module contains seven separate memory banks, each 64K vectors in depth, for generating stimulus patterns, expected response patterns and recording UUT response data. All memory banks operate at full 50 MHz data rates.

The *Stimulus Memories* consist of the Output, Tristate, and Algorithmic Output Memories. The *Output Memory* contains the actual data patterns to be generated to the UUT. *Tristate Memory* provides tristate control that supports bidirectional I/O. The *Algorithmic Output Memory* determines which algorithmic pattern will be output.

The *Response Memories* consist of the Expect, Mask and Algorithmic Expect memories. The *Expect Memory* contains the expected response for the UUT and is the basis for input compare operations. The *Mask Memory* determines which patterns are to be ignored for input response comparison. *Algorithmic Expect Memory* determines which algorithmic expect pattern will be compared against the UUT input response.

Record Memory is used to store either the UUT response data or the result of the comparison between the UUT response data and the expected response pattern.

Data Formatting with Precise Edge Placement

Stimulus pins may be independently programmed for any of the following data formats: Non Return to Zero (NRZ), Return to Zero (RZ), Return to One (R1), Return to Complement (RC) and Return to Inhibit/Tristate (RI).

Each SR5030 I/O Module contains 8 timing generators for stimulus edge placement and pulse width timing. Output pins can select from 2 pairs of timing generators to define the leading and trailing edges of each signal pin. Groups of 8 output pins share an independent set of 2 timing generator pairs for a total of 2 stimulus timing generator sets pr module. 100 ps edge placement resolution provides precise UUT timing for bus emulation testing, memory testing, and functional testing.

Controls and Indicators

See Fig. 1-1. All the connectors and LEDs for the SR5030 I/O module are located on the front panel.

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LEDs

There are four LEDs located at the top of the SR5030 I/O Module:

- **SYSFAIL** (red) - Off during normal operation. During the power-up sequence, this indicator is lit until the internal self-test is complete. The indicator remains lit if the self-test fails. The error code information stored in the Data Low Register indicates the origin of the self-test failure.
- **ACCESS** (yellow) - Illuminates briefly each time the SR5010 Timing/Control Module communicates with the I/O modules as Bus Master.
- **CURRENT** (red) - Off during normal operation. If the drive current of any output driver exceeds 50 mA, the CURRENT LED will light.
- **TEMP** (red) - Off during normal operation. If the internal temperature of the SR5030 exceeds 75 degrees Celsius, the TEMP LED will light.

Connectors

The group of two 34-pin connectors located directly below the LEDs comprise the input/output connectors. The stimulus (output) pins are located on the left side of the module; the response (input) pins on the right.

The 34-pin CONTROL connector receives clock and control commands from the SR5010 Timing/Control Module and supplied real-time status signals back to the SR5010.

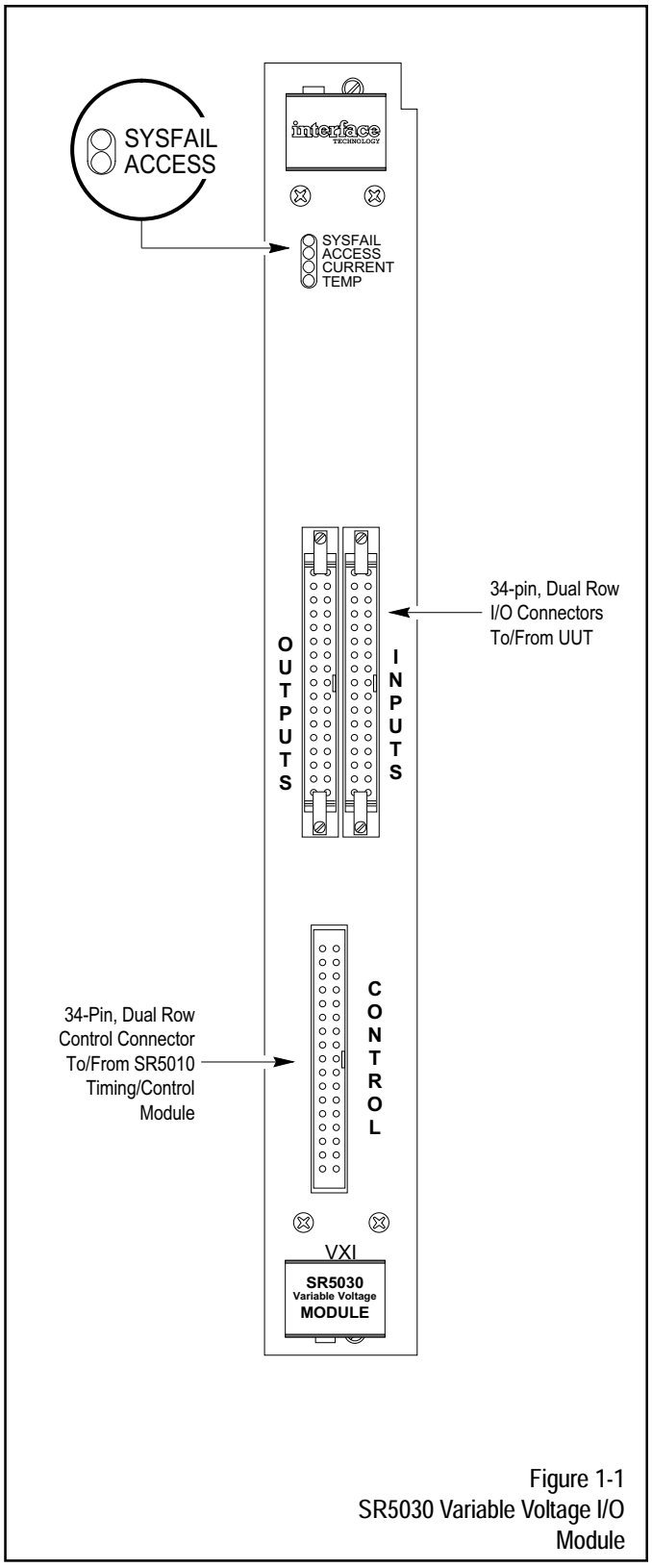


Figure 1-1
SR5030 Variable Voltage I/O Module

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*SR5030 SPECIFICATIONS**

Channels per Module:

Inputs	16
Outputs	16

Memory Types:

Stimulus	Output, Tristate, Algorithmic
Response	Expect, Mask, Algorithmic
Record	

Memory Depth:

65,500 vectors

Output Drivers:

Type	Variable Voltage
Voh	-5.5 V to +15 V, unterminated
Vol	-6.0 V to +14.5 V, unterminated
Output Swing	0.5 V to 21 V p-p, unterminated
Output Current	± 50 mA, maximum
Output Protection	Current and temperature
Abs Max Volt	-7.0 V to +16 V (high Z)
Output Impedance	50 ohms, ± 10%
Voltage Resolution	0.01 volt
Absolute Accuracy	0.1 volt
Slew Rate	1 volt/ns, nominal: internally controlled according to output level

Data Formats:

RZ	Return to Zero
NRZ	Non-Return to Zero
RONE	Return to One
RC	Return to Complement
RI	Return to Inhibit/Tristate

Output Timing:

Clock Pairs	4 total per card (assert/deny) 2 per eight channels
Delay Range	One clock period
Pulse Width	10 ns, min. (high or low)
Resolution	100 ps, non-monotonic 2.0 ns, monotonic
Delay Accuracy	2.0 ns, typ; 3.0 ns, max. (single channel)
Pulse Width	3.0 ns, typ; 5.0 ns, max. Accuracy

Skew:

Same Module	±2 ns typical, ±4 ns maximum
SR5030-SR5030	±3 ns typical, ±5 ns maximum

Input Receivers:

Type	Variable Threshold
Input Thresh. Range	-6 V to +12 V
Vth Resolution	0.01 V
Vth Absolute Accuracy	0.1 V
Input Hysteresis	60 mV p-p, typical
Input Resistance	30k ohms, typical to Vth
Input Termination	Jumper selectable: none, 50 ohms to ground, or 50 ohms to -2.0 V

Input Sample / Compare Modes:

Formats	Edge / window
Range	One period clock cycle
Resolution	100 psec
Accuracy	±1 ns typical; ±2 ns maximum

Input Timing:

Number of Timing Clocks	Two per card (edge mode); one per card (window mode)
Input Delay Range	One clock period
Clock Separation	10.0 ns, minimum
Resolution	100 ps, non-monotonic; 2.0 ns, monotonic

VXI Specifications

Interface Compatibility:

Type	Register-based, servant only (controlled by SR5010)
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Memory	2 MB VME A32/D32

Power Requirements:

+5.0 volts	5.0 A	25.0 W
-5.2 volts	2.5 A	13.0 W
+12.0 volts	0.1 A	1.20 W
+24.0 volts	1.6 A	38.4 W
-24.0 volts	0.75 A	18.0 W
-12.0 volts	0.1 A	1.20 W
-2.0 volts	2.0 A	4.00 W

Total Power		100.8 W (max.)

Cooling Requirements:

Per-slot Average	101 W (max.)
Airflow	8 L/sec @ 0.38 mm water pressure for 10°C temperature rise

Environmental Specifications:

Temperature	Storage = -40°C to +75°C Operating = 0°C to +45°C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

National Instruments	LabView
National Instruments	LabWindows/CVI

* Specifications subject to change without notice.

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CHAPTER 2

Theory of Operation

Block Diagram

See Fig. 2-1. The SR5030 Variable Voltage I/O Module contains Stimulus, Response, and Record logic for 16 channels of output and 16 input channels. Figure 2-1 shows the main components and data paths for this module.

VXI Register-Based Interface

The SR5030 I/O module uses an Interface Technology IT9010 interface chip to implement a VXI register-based interface. All I/O board memory in the SR5010 module is mapped to the system processor, while all I/O board memory in the SR5030 is mapped to VME A32 memory on the VXI bus. The slot-0 controller should not directly access the SR5030 module or its memory, except to test for its existence during resource management functions and ID. Any other direct access to the SR5030 memory, other than by the SR5010 in Bus Master mode, may cause unpredictable results when executing a test.

Stimulus and Response Memory

The stimulus and response memory block contains data needed to generate the stimulus and expect response data patterns. The VXI bus may read and write this memory when the control processor is not running. When the control processor is running, access to the VXI bus is blocked and the stimulus and Response Gate Arrays have exclusive read-only access to the memory. The address counters regenerate the control processor address on each stimulus gate array and are used to drive the memory for the pair of stimulus and Response Gate Arrays. Each I/O board contains four of these address buses. However, the buses are effectively locked together with the control processor's address counter.

Record Memory

The Record Memory stores the data returned by the UUT, or the results of the data returned by the UUT and compared to the data provided by the expected response pattern generator. This is a read only memory for the user and can be read only when the control processor is not running. When the control processor is running, access to the memory by the user is blocked and the Response Gate Arrays have exclusive write-only access to the memory. The record address counters are generated on each Response Gate Array and are effectively locked together. The record address counter is independent of the control processor’s address counter, which controls stimulus and response vector sequencing.

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Formatting Clocks

Each I/O card contains 10 clock delay generators used to adjust the edge timing of the output and sample inputs. Four separate delayed clocks are applied to each of the four Stimulus Gate Arrays. A total of eight delay generators are used by the stimulus section. In each Stimulus Gate Array, logic is provided for the eight output pins to select one of the two delay clocks to assert the output (NRZ mode) or select one of two delay clock pairs to define the assert and deny times for the output (return-to-modes).

The remaining two delayed clocks are applied in parallel to the two Response Gate Arrays. Each response input pin can be clocked using the Edge mode with either of these clocks or using both clocks in the Window mode.

Basic Delay

The system VCO operates between 200 MHz and 100 MHz, counted down by four and distributed to the system as a 50 MHz to 25 MHz, four-phase, ECL clock (period clock). Each generator has a range switch used to select one of the four phases, displaced from each other by 90 degrees. For example, when operating at 25 MHz (40 ns period), the delay allows for the selection of an additional delay of 0 ns, 10 ns, 20 ns and 30 ns from the beginning of the period clock. When combined with the fine delay, the delay provides a total range of 40 ns, or one period of the slowest VCO clock rate.

Fine Delay

An 8-bit digital-to-analog converter (DAC) drives a voltage controlled analog delay line that provides an additional programmable delay of up to 10 ns, in 100 ps steps. The actual range of this delay line is 14 ns. During factory calibration, a table is generated, and saved in EEPROM, of the phase delay generated for each control voltage produced by the DAC. This information, along with the extra 4 ns of analog delay, is used by the System Processor to compensate for system skew and the nonlinearity of the analog delays.

Extended Delay

When the system is operating below 25 MHz, a clock divider circuit is employed inside the gate arrays to allow additional delays from 1 to 65,535 clocks. When combined with the basic and fine delays, a range of 65,536 clock periods is possible, with a 100 ps resolution. In the stimulus section, the selected assert delay clock must be located within one period of the system clock. The selected deny delay clock must be located at least 10 ns after the selected assert clock and no more than one clock period minus 10 ns after the assert time. The minimum pulse width of any channel is 10 ns.

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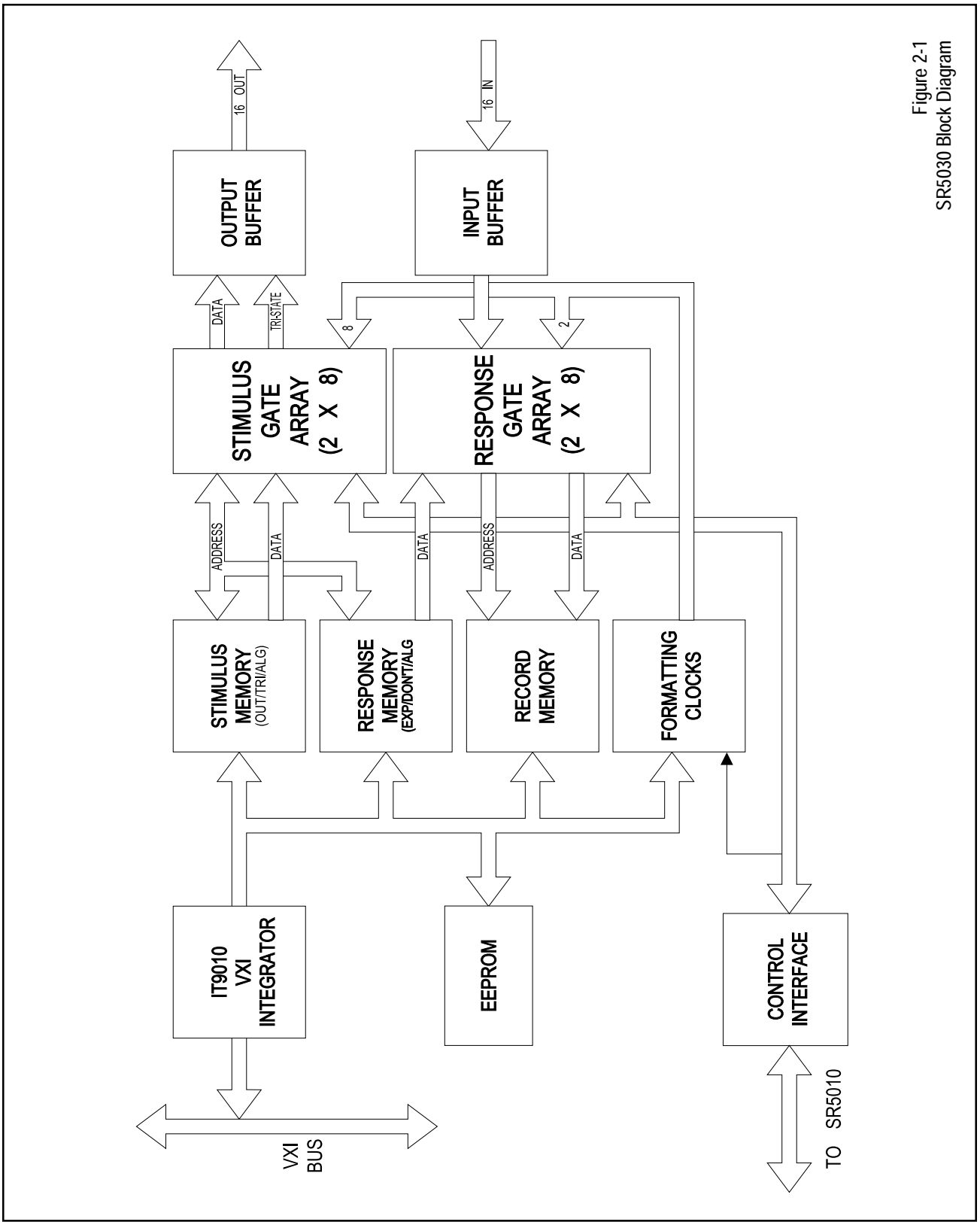


Figure 2-1
SR5030 Block Diagram

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EEPROM

The EEPROM in each SR5030 stores timing and calibration information that is unique to that module, refer to Fine Delay in previous paragraph. The calibration information is used to deskew output channels and to compensate for nonlinearity and metastability in the analog delay circuit. The EEPROM is programmed at the factory and is not accessible to the user. If any component in the path of an output channel is replaced, or in the delay circuitry, the I/O module must be returned to the factory for recalibration.

Control Board Interface

The Control Board Interface receives and buffers the stimulus, response and record signals from the SR5010 Timing/Control Module and returns the response status information back to the SR5010. These signals are passed via the Control Bus Cable, which interconnects the SR5010 and each of the I/O modules. (Refer to SR5010 manual for discussion of the Control Bus.)

Stimulus Gate Arrays

(Fig 2-2). The Stimulus Gate Arrays, in conjunction with the stimulus memories (Output, Tristate and Algorithmic Command) form the heart of the SR5030 stimulus pattern generator. Each gate array is an 8-bit wide, high-speed pattern generator and data formatter. Pattern generation is accomplished by outputting the contents of the stimulus RAM directly or by algorithmically generating the data within the gate array using a high-speed ALU state machine. Some gate arrays may be programmed for RAM-backed pattern generation, while other gate arrays on the same card may be programmed for algorithmic pattern generation. While any gate array supports only one type of pattern generation during any test run, one of the algorithmic commands instructs the ALU state machine to pass data directly from RAM to the outputs. This allows mixing of algorithmic and RAM-backed pattern generation on the same pins.

Each stimulus channel contains its own output formatter, but all channels in a gate array share the four timing clocks. These timing generator clocks define the assert and deny times for channels that use the return-to-data formatting capabilities of the gate array. Each I/O card contains two stimulus gate arrays, providing 16 stimulus channels per SR5030 I/O module.

Stimulus Pattern Generator

The pattern generator within the Stimulus Gate Array is a high-speed programmable state machine. Instructions for this state machine are stored in the stimulus algorithmic command memory and instruct the gate array on a clock-by-clock basis to either load the ALU output register from RAM or to algorithmically modify the contents of the ALU register. The output memory holds the clock-by-clock state of the output pins. The

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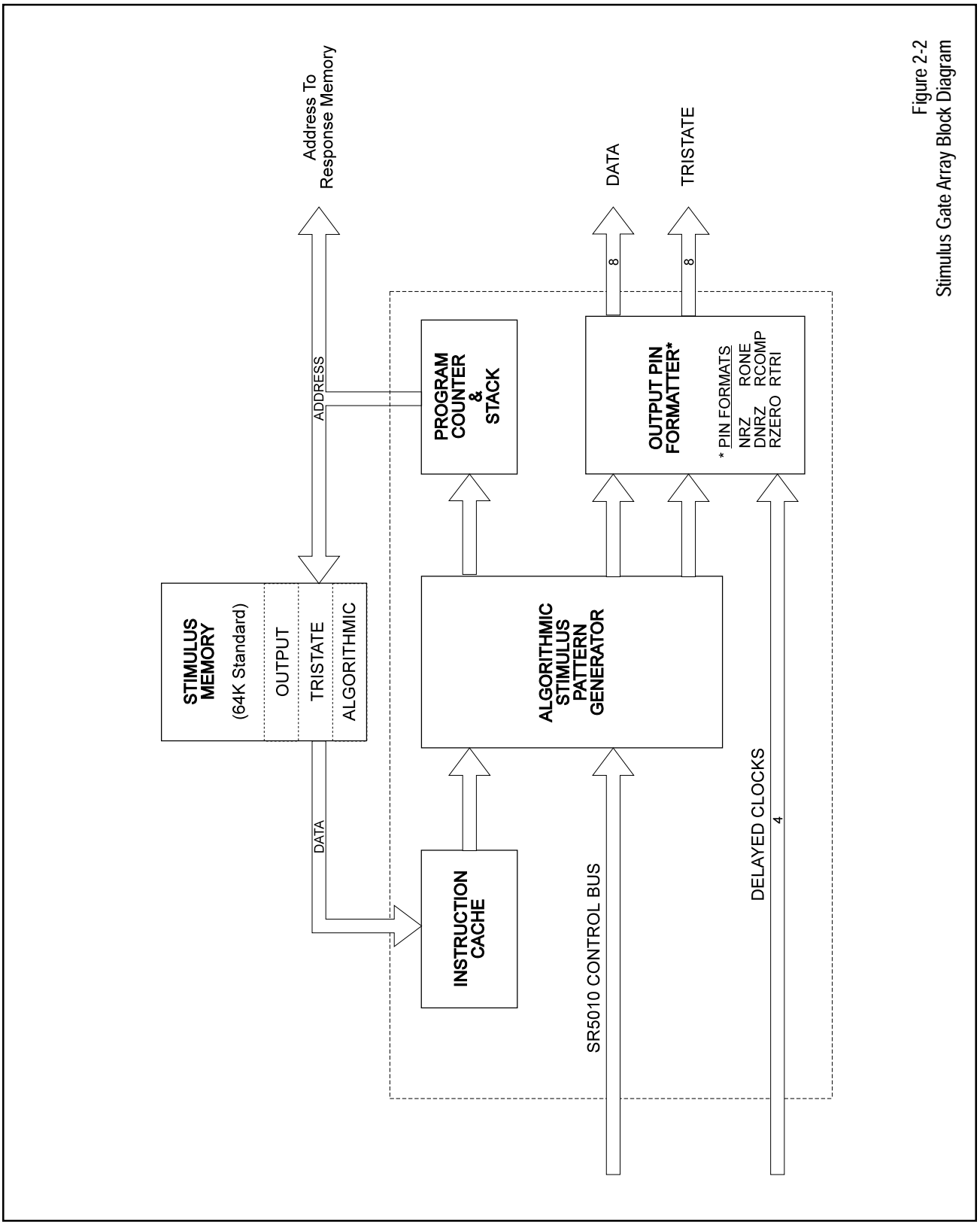


Figure 2-2
Stimulus Gate Array Block Diagram

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Tristate Memory holds the clock-by-clock state of the output enable, which allows a pin to be driven by the output memory on one clock cycle and tristated on the next clock cycle, thus achieving a bidirectional pin. In algorithmic mode, data patterns are defined by applying an algorithmic function to the internal ALU register. Multiple stimulus gate arrays may be cascaded together to create 16-bit wide algorithmic patterns.

Stimulus Output Formatter

Each output channel contains a pin formatter that provides the following data formats: Non Return-to-Zero (NRZ), Return-to-Zero (RZ), Return to One (R1), Return-to-Compliment (RC), and Return-to-Inhibit (RI). The pin formatter section of each gate array can access the four precision timing generator clocks, which are used to define the assert and deny times for the output channels.

Response Gate Arrays

(Fig 2-3). The Response Gate Arrays, in conjunction with the response memories (Expect, Don't Care and Algorithmic Command) form the heart of the SR5030 expected response pattern generator, used in real-time compare operations. Each gate array is an 8-bit wide, high-speed pattern generator. Pattern generation is accomplished by outputting the contents of the RAM directly or by algorithmically generating the data within the gate array using a high-speed ALU state machine. Some gate arrays may be programmed for RAM-backed pattern generation, while other gate arrays on the same card may be programmed for algorithmic pattern generation. While any gate array supports only one type of pattern generation during any test run, one of the algorithmic commands instructs the ALU state machine to pass data directly from RAM to the outputs. This effectively allows mixing of algorithmic and RAM-backed pattern generation on the same pins.

All input channels share the two sample timing generator clocks. These clocks define the sample timing when in the edge sample/compare mode of the gate array, or the window open and window close times for channels that use the window compare capabilities. Each I/O module contains two Response Gate Arrays, providing the 16 response/record channels per SR5030 I/O module.

Expected Response Pattern Generator

The expected pattern generator within the Response Gate Array is a high-speed, programmable state machine. Instructions for this state machine are stored in the Response Algorithmic Command Memory and instruct the gate array on a clock-by-clock basis to either load the ALU output register from RAM or to algorithmically modify the contents of the ALU register. The Expect Memory holds the clock-by-clock state of the expected response pattern. The Don't Care Memory holds the clock-by-clock state of the compare enable, which allows a pin to be disabled for compare on one clock cycle and enabled for compare on the next clock

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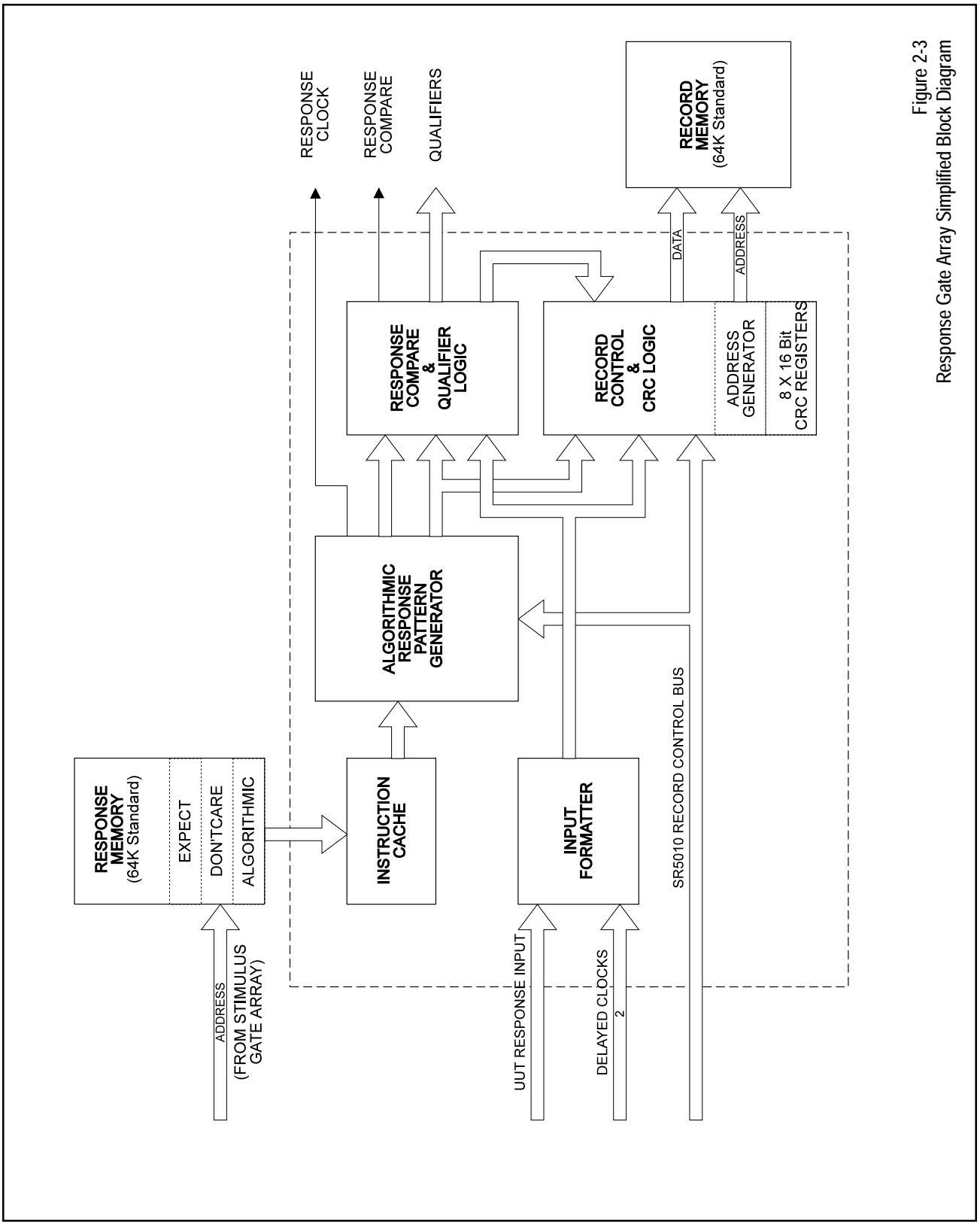


Figure 2-3
Response Gate Array Simplified Block Diagram

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cycle. In algorithmic mode, data patterns are defined by applying an algorithmic function to the internal ALU register. Multiple gate arrays may be cascaded together to create 16-bit wide algorithmic patterns.

Response Input Formatter

The response input formatter latches the response data from the UUT and passes it on to the Response Compare Logic and the Record Control Logic, where it is used for other processes.

The pin formatter section of each gate array can access the two precision timing generator clocks, which are used to define the edge and window sample times. For convenience, these two sample clocks may be thought of as a leading clock and a trailing clock. The two sample clocks must be positioned at least 10 ns from each other and must reside in the same vector cycle. The trailing edge sample clock must be defined first, and the leading sample clock, if used, defined second. In the Window mode, both clocks are defined in the same command.

Response Comparator

The Response Comparator logic compares the data latched by the input formatter to the pattern generated by the Response Pattern Generator, and passes the result to the Record Control Logic. A response compare signal is generated for each test cycle, regardless of whether the real-time compare mode is being used. These signals, one from each I/O module, are summed on the SR5010 and used for generation of the Error Latch, and may also be used for test sequence control decisions based on real-time compare results.

Input Qualifier

The Response Gate Arrays also contain eight Qualifier Trigger Registers and the Qualifier Compare Logic. All eight qualifier triggers (qualifiers) are compared to the latched input data that is passed from the input formatter on each test cycle. The results of the qualifier compare are passed back to the SR5010 module. The qualifier compare signals from each I/O board are summed on the SR5010 and used by the Record State Machine to start and stop data recording, provide filtered data recording, to start and stop CRC sampling. These signals may also be used for test sequence control decisions based on qualifier compare results. Qualifiers may be enabled in Qualifier Combinations (QCOMBINATIONS) providing logical ANDing and ORing of triggers.

Record Control

The Record Control Logic in the Response Gate Array provides two main functions: to generate Record Memory addresses and to pass data to the Record Memory for storing. This logic receives instructions from the

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SR5010 Record State Machine, over the Control Bus, which determines when to record data and what data to record. After each record operation the Record Memory address is incremented by one, therefore, all data is recorded in a continuous, linear sequence. Since the Record Memory is addressed separately from the stimulus and response memories, there is no assurance that the number of record vectors is the same as the number of stimulus and response vectors. Also, if record data wrapping is enabled, and the number of vectors recorded exceeds the size of the test, the oldest data in the Record Memory is overwritten. This will continue until the test stops or is aborted. Record Memory is then rearranged to provide a linear sequence of recorded data from oldest to most recent, accessed from the first vector to the last vector, respectively.

Two types of data may be passed to the Record Control Logic for recording; the UUT response data latched by the input formatter, or the results of the real-time comparison performed in the Response Comparator. The latter is known as Error Data, or errors, and is represented as a "0" stored for each bit where the compare matched, and a "1" stored for each bit where the compare did not match. Selecting which data to record may be changed from within the SR5000 test using control structures called Trace Sequences. As there are 16 levels of Trace Sequences, this start and stop process of recording data may occur multiple times in a single test, allowing invalid or inappropriate responses to be ignored. For additional information about Trace Sequences, refer to the *Record State Machine* section earlier in this chapter.

CRC Logic

Each input pin on the SR5030 I/O board has a 16-bit register and logic used for calculating CRC signatures, all located within the Response Gate Arrays. CRC calculations are controlled from the same Trace Sequences as are used to control data recording. Based on matching of a trigger condition, CRC calculations may either be enabled or disabled. As there are 16 levels of Trace Sequences, this start and stop process of calculating CRC signatures may occur multiple times in a single test, allowing invalid or inappropriate samples to be ignored. For additional information about Trace Sequences, refer to the *Record State Machine* section earlier in this chapter.

For the purpose of signature analysis, each input pin may be thought of as a separate serial channel. So, each SR5030 I/O module has 16 independent signature analysis channels. Enabling or disabling the CRC calculation is performed globally within the SR5000 system using the trace sequences. The Don't Care Memory, which is used to enable individual bits for real-time compare, is also used to dynamically enable or disable individual CRC calculations. If CRC calculations are globally enabled, and the individual CRC calculation is enabled (Don't Care bit set to "0"), a

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CRC calculation is performed. If the individual CRC calculation is disabled (Don't Care Memory set to "1"), the CRC calculation is disabled for that channel on that test cycle. When the CRC calculation is enabled, the data passed from the input formatter is used to update the value in the CRC registers based on the CCITT standard communication polynomial used to perform CRC calculations. When disabled, the data passed from the input formatter is ignored by the calculation logic, i.e., no calculation takes place. Data is passed to the CRC logic from the input formatter using the same sample clocks used to record data, so timing for CRC samples is identical to timing for record samples.

Algorithmic Commands

The Stimulus and Response Gate Arrays each contain algorithmic pattern generators that generate stimulus and response patterns, respectively. The following list of algorithmic commands are common to both stimulus and response pattern generation.

NONAlgorithmic

The Nonalgorithmic command allows the gate arrays to act as a pass through for data from RAM to the output pins. The data that is passed from RAM to output is also used to initialize the algorithmic register. This register can be acted on by other algorithmic commands to modify the data content programmatically after initialization.

INCrement

Increment the contents of the algorithmic register and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. If an increment instruction causes an overflow, the overflow is used as a carry input to the next most significant gate array thus extending the count up to a maximum of 2^{16} before roll over.

DECrement

Decrement the contents of the algorithmic register and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. If a decrement instruction causes an underflow, the underflow is used as a borrow input from the next most significant gate array thus extending the count up to a maximum of 2^{16} before roll over.

XOR

The XOR instruction will perform a bit-wise exclusive "ORing" of the algorithmic register with the contents of RAM. In this case the RAM acts as a modifier to the register and does not directly load it. In this way, selective bits of the algorithmic register may be complemented before passed to the output pins.

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SLEFTZero

Shift the contents of the algorithmic register left (LSB to MSB) one bit, fill the LSB with "0" and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the MSB output of a less significant gate array is used as a LSB input to the next most significant gate array, thus extending the shift to a maximum 16-bits.

SLEFTOne

Shift the contents of the algorithmic register left (LSB to MSB) one bit, fill the LSB with "1" and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the MSB output of a less significant gate array is used as a LSB input to the next most significant gate array, thus extending the shift to a maximum 16-bits.

SLEFTComplement

Shift the contents of the algorithmic register left (LSB to MSB) one bit, complement the LSB and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the MSB output of a less significant gate array is used as a LSB input to the next most significant gate array, thus extending the shift to a maximum 16-bits.

RLEFT

Rotate the contents of the algorithmic register left (LSB to MSB) one bit, wrap the MSB to the LSB and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the MSB output of a less significant gate array is used as a LSB input to the next most significant gate array and the MSB of the most significant gate array is wrapped to the LSB of the least significant gate array, thus extending the rotate to a maximum 16-bits.

SRIGHTZero

Shift the contents of the algorithmic register right (MSB to LSB) one bit, fill the MSB with "0" and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the LSB output of a more significant gate array is used as a MSB input to the next least significant gate array and the LSB of the least significant gate array is wrapped to the MSB of the most significant gate array, thus extending the rotate to a maximum 16-bits.

SRIGHTOne

Shift the contents of the algorithmic register right (MSB to LSB) one bit, fill the MSB with "1" and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked.

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In this case, the LSB output of a more significant gate array is used as a MSB input to the next least significant gate array and the LSB output of a more significant gate array is used as an MSB input to the next least significant gate array, thus extending the shift to a maximum of 16-bits.

SRIGHTComplement

Shift the contents of the algorithmic register right (MSB to LSB) one bit, complement the MSB and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the LSB output of a more significant gate array is used as an MSB input to the next least significant gate array, thus extending the shift to a maximum of 16-bits.

RRIGHT

Rotate the contents of the algorithmic register right (MSB to LSB) one bit, wrap the LSB to the MSB and pass the results to the output pins. If algorithmic fields greater than 8-bits are used, multiple gate arrays are interlinked. In this case, the LSB output of a more significant gate array is used as an MSB input to the next most significant gate array and the LSB of the most significant gate array is wrapped to the MSB of the least significant gate array, thus extending the rotate to a maximum 16-bits.

Programmable Output Drivers

See Fig 2-4. Each group of four driver pins has independent control of the output high (Voh) and output low (Vol) voltage levels. To facilitate programming of output logic levels, "field" definitions are used to define a logical grouping of output pins, (refer to main manual for further discussion on fields; refer to Chapter 3 of this manual for further discussion of programming output levels.)

Programmable Input Receivers

See Fig 2-5. Each group of four receiver pins has independent control of the input threshold voltage level. Again, as in the case of the programmable output drivers, "fields" are used to assign the input threshold voltage setting to a logical grouping of pins, (refer to main manual for further discussion on fields; refer to Chapter 3 of this manual for further discussion of programming output levels.)

Over-Current and Over-Temperature Protection

The SR5030 provides both current and temperature sensing to protect the SR5030 and the UUT from damage. The maximum stimulus driver current is 50 mA per output driver circuit. It a UUT load causes any stimulus driver to exceed 50 mA, then all the output drivers will be disabled (disconnected) to protect the UUT and the SR5030. The CURRENT indicator on the front panel lights to indicate the over-current condition. Likewise, if the internal temperature of the SR5030 exceeds 75 degrees Celsius, then all the output drivers will be disconnected. The TEMP indicator on the front panel lights to indicate the over-temperature condition.

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When an over-current or over-temperature shutdown occurs, the SR5030 will wait ten seconds, then check again for the presence of the fault condition. If the current or temperature fault has cleared, then the output drivers will be reconnected, otherwise the output drivers will remain disconnected and the LED indicator(s) will remain lit. The SR5030 will then wait five seconds before checking once again for the presence of a fault condition. After six successive fault events have occurred, the SR5000 will assume that the fault is catastrophic and will shutdown the entire system completely. In that case, the power must be cycled to the SR5000 system in order to regain access to the SR5000 system.

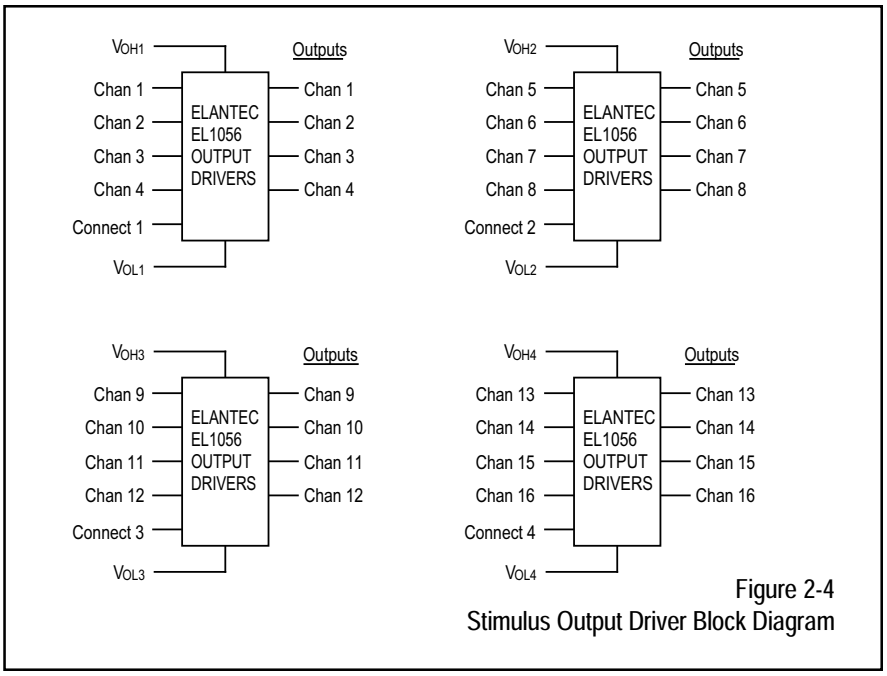


Figure 2-4
Stimulus Output Driver Block Diagram

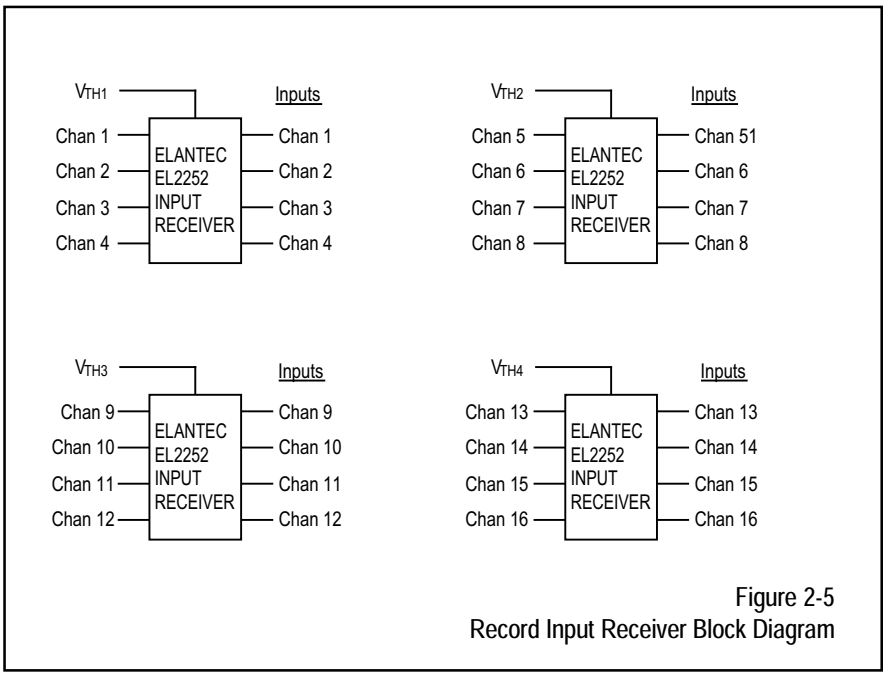


Figure 2-5
Record Input Receiver Block Diagram

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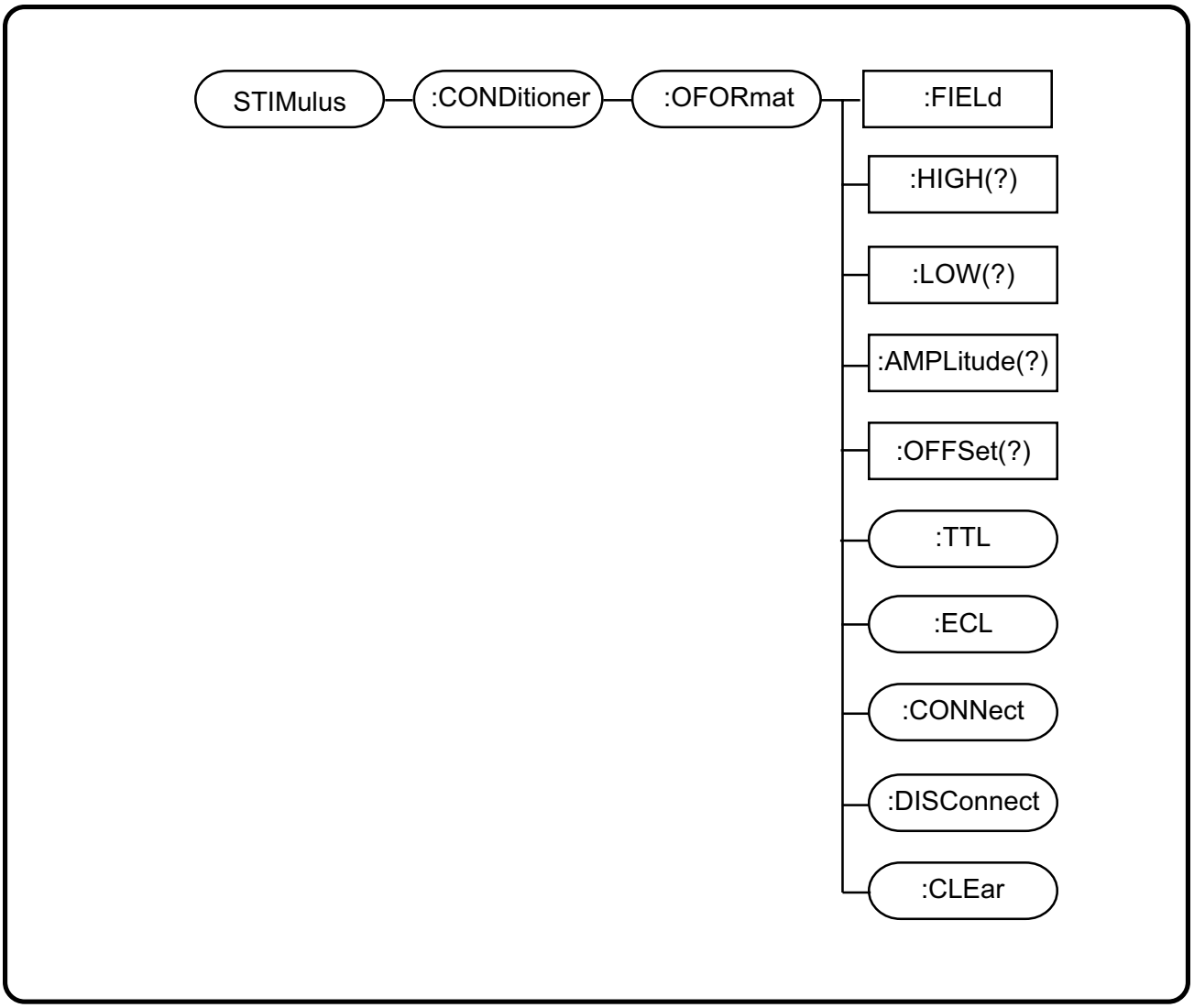
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CHAPTER 3

Programming

Scope of Chapter

This chapter contains the programming command routines that are unique to the SR5030 Variable Voltage I/O Module. The routines in this chapter should be used in conjunction with the general programming commands and command routines contained in the SR5000 main manual.



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Setting the Stimulus Output High Voltage Level (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::HIGH** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus:::HIGH command sets the output high voltage level for the specific stimulus field. The high level can be entered as a floating point numeric or in scientific notation. The HIGH command is used in conjunction with the LOW command to set the output high/low voltage levels. If multiple fields overlap, meaning they were defined as sharing common pins, then the high voltage level for all overlapping pins will be set to the last parameters defined for any one of the fields. The STIMulus::::HIGH? query command returns the stimulus output high level for the specified field.

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELD <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameter will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO) and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and HIGH parameters must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be set to the same output high voltage setting.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:HIGH<volts>

Parameter Definition **volts** = (-5.50 V to +15.00 V) Values can be specified as a floating point numeric or in scientific notation using exponential values. Optional V, MV, and UV suffixes can be used for engineering unit multipliers. The default engineering unit is volts (V).

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Setting the Stimulus Output High Voltage Level (cont) (NON-SCPI)

Examples
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA:HIGH 5e+0V
STIM:COND:OFOR:HIGH 5

:HIGH?

Returns the output high voltage level for the specified test.

Response
name volts | UNDEFINED {;name volts | UNDEFINED}

Parameter Definition
name = any alphanumeric string and '_' (max 8 characters).

volts = The output high voltage setting specified in volts using scientific notation values from -5.500000e+00 to 1.500000e+01.

UNDEFINED = The output voltage level has not been defined for the specified field, or the output amplitude has been cleared.

Examples
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;HIGH?
DATA 5.000000E+00

STIM:COND:OFOR:FIELD ALL;HIGH?
Data 5.000000e+00;ADDR UNDEFINED

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Setting the Stimulus Output Low Voltage Level (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::LOW** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::LOW command sets the output low voltage level for the specified stimulus field. The low level can be entered as a floating point numeric or in scientific notation. The LOW command is used in conjunction with the HIGH command to set the output high/low voltage levels. If multiple fields overlap, then the low voltage level for all overlapping pins will be set to the last parameters defined for any one of the fields. The STIMulus::::LOW? query command returns the stimulus output high level for the specified field.

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and LOW parameters must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be set to the same output low voltage setting.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:LOW<volts>

Parameter Definition **volts** = (-6000 V to +14.50 V) Values can be specified as a floating point numeric or in scientific notation using exponential values. Optional V, MV, and UV suffixes can be used for engineering unit multipliers. The default engineering unit is volts (V).

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Setting the Stimulus Output Low Voltage Level (cont) (NON-SCPI)

Examples

STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;LOW 1e+0V
STIM:COND:OFOR:LOW 1

:LOW?

Returns the output low voltage level for the specified field.

Response

name volts | UNDEFINED {;name volts | UNDEFINED}

Parameter Definition

name = any alphanumeric string and '_' (max 8 characters).

volts = the output low voltage setting specified in volts using scientific notation values from -6.000000e+00 to +1.450000e+01.

UNDEFINED = the output low level has not been defined for the specified field, or the output low level has been cleared.

Examples

STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;LOW?
DATA 1.000000e+00

STIM:COND:OFOR:FIELD ALL;LOW?
DATA 1.000000e+00;ADDR UNDEFINED

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Setting the Stimulus Output Amplitude (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::AMPLitude** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::AMPLitude command sets the amplitude peak-to-peak level for the specified stimulus field. The amplitude level can be entered as a floating point numeric or in scientific notation. The AMPLitude command is used in conjunction with the OFFSet command to set the output high/low amplitude levels. For example, to set the output high level to +5.0 volts and the output low level to 0.0 volts, the amplitude must be set to 5.0 volts peak-to-peak and offset must be set to 2.5 volts. If multiple fields overlap, meaning they were defined as sharing common pins, then the amplitude for all overlapping pins will be set to the last parameters defined for any one of the fields. The STIMulus::::AMPLitude? query command returns the stimulus output amplitude for the specified field.

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition

None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and AMPLitude parameters must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition

name = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be set to the same output amplitude setting.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

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Setting the Stimulus Output Amplitude (cont) (NON-SCPI)

:AMPLitude<volts>

Parameter Definition **volts** = (0.50 V to 21.00 V) Values can be specified as a floating point numeric or in scientific notation using exponential values. Optional V, MV, and UV suffixes can be used for engineering unit multipliers. The default engineering unit is volts (V).

Examples
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;AMPLITUDE 5E+0V
STIM:COND:OFOR:AMPL 5

:AMPLitude?

Returns the output amplitude for the specified field.

Response name volts | UNDEFINED {;name volts | UNDEFINED}

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

volts = the output low voltage setting specified in volts using scientific notation values from 5.000000e-01 to 2.100000e+01.

UNDEFINED = the output amplitude has not been defined for the specified field, or the output amplitude has been cleared.

Examples
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;AMPLITUDE?
DATA 5.000000e+00

STIM:COND:OFOR:FIELD ALL;AMPL?
DATA 5.000000e+00;ADDR UNDEFINED

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Setting the Stimulus Output Offset (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::OFFSet** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::OFFSet command sets output offset level for the specified stimulus field. The offset level can be entered as a floating point numeric or in scientific notation. The OFFSet command is used in conjunction with the AMPLitude command to set the output high/low amplitude levels. If multiple fields overlap, meaning they were defined as sharing common pins, then the offset level for all overlapping pins will be set to the last parameters defined for any one of the fields. The STIMulus::::OFFSet? query command returns the stimulus output amplitude for the specified field.

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and OFFset parameters must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be set to the same offset voltage setting.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:OFFSet<volts>

Parameter Definition **volts** = (-5.75 V to +14.75 V) Values can be specified as a floating point numeric or in scientific notation using exponential values. Optional V, MV, and UV suffixes can be used for engineering unit multipliers. The default engineering unit is volts (V).

Examples

```
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;OFFSET 2.5E+0V
STIM:COND:OFOR:OFFS 2.5
```


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Setting the Stimulus Output Offset (cont) (NON-SCPI)

:OFFSet? Returns the output amplitude for the specified field.

Response name volts | UNDEFINED {;name volts | UNDEFINED}

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

volts = the output low voltage setting specified in volts using scientific notation values from -5.750000e+00 to 1.475000e+01.

UNDEFINED = the output amplitude has not been defined for the specified field, or the output amplitude has been cleared.

Examples STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;OFFSET?
DATA 2.5000000e+00

STIM:COND:OFOR:FIELD ALL;OFFS?
DATA 2.5000000e+00;ADDR UNDEFINED

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Setting the Stimulus Output to TTL Levels (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::TTL** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::TTL command sets the output amplitude to TTL voltage levels for the specified stimulus field. If multiple fields overlap, then all overlapping pins will be set to TTL voltage levels. The TTL voltage levels are +5.00 volts for TTL logic high and 0.00 volts for TTL logic low.

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and TTL strings must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be set to TTL voltage levels.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:TTL

Parameter Definition None

Examples
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;TTL
STIM:COND:OFOR:TTL

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Setting the Stimulus Output to ECL Levels (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::ECL** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::ECL command sets the output amplitude to ECL voltage levels for the specified stimulus field. If multiple fields overlap, then all overlapping pins will be set to ECL voltage levels. The ECL voltage levels are -0.80 volts for ECL logic high and -1.80 volts for ECL logic low.

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and ECL strings must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition

name = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be set to ECL voltage levels.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:ECL

Parameter Definition None

Examples

STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;ECL
STIM:COND:OFOR:ECL

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Connecting the Output Drivers (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIMulus::::CONNect** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::CONNect command "turns on" the output drivers for the specified stimulus field. Upon power up or system reset (*RST), the state of the output drivers if off (disconnected), which places the output drivers in a high impedance state. If multiple fields overlap, then all overlapping pin groups will be turned on (connected).

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and CONNect strings must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

ALL = All output drivers of all stimulus fields will be connected.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:CONNect

Parameter Definition None

Examples
```
STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;CONNECT
STIM:COND:OFOR:CONN
```


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Disconnecting the Output Drivers (NON-SCPI)



] CAUTION [

Like many Test Setup commands, the **STIM ulus::::DISConnect** command is executed only when the INITiate command is executed. Caution should be taken so as not to inadvertently damage the UUT when changing logic levels.

The STIMulus::::DISConnect command "turns off" the output drivers for the specified stimulus field. The power up/system reset state of the output drivers is off (disconnected), which places the output drivers in a high impedance state. If multiple fields overlap, then all overlapping pin groups will be turned off (disconnected).

:OFORmat

Selects the Output Format path of the STIMULUS:CONDITIONER subsystem.

Parameter Definition None

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field that the OFORmat parameters will act on. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and DISConnect parameters must be separated by a semicolon, as shown. If the FIELd parameter is omitted, then the default stimulus field is used. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition

name = any alphanumeric string and '_' (max 8 characters).

ALL = The output drivers of all stimulus fields will be disconnected.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:DISConnect

Parameter Definition None

Examples

STIMULUS:CONDITIONER:OFORMAT:FIELD DATA;DISCONNECT
STIM:COND:OFOR:DISC

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Clearing Stimulus Output Voltage Settings (NON-SCPI)



The STIMulus:CONDitioner:OFORmat:CLEar command clears the output logic voltage settings for the specified stimulus field. The stimulus output voltage will be set to UNDEFINED. If multiple fields overlap, then the voltage setting for all overlapping pins will be cleared. This same command is also used to clear the stimulus output format and timing values.

:FIELd <name | ALL>

The optional FIELd parameter specifies the stimulus type field from which the output format and timing edge placement values will be cleared. Stimulus field types are Output (OUT), Output/Tristate (OT), Algorithmic Output (ALGO), and Hardware Output (HOUT). If the optional FIELd parameter is used, then the FIELd and CLEar strings must be separated by a semicolon. If the FIELd parameter is omitted, then the default stimulus field is assumed. The default stimulus field is defined by the STIMulus:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all stimulus type fields.

Parameter Definition

name = any alphanumeric string and '_' (max 8 characters).

ALL = All stimulus fields will be cleared.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:CLEar

Terminates the command and executes the clear function.

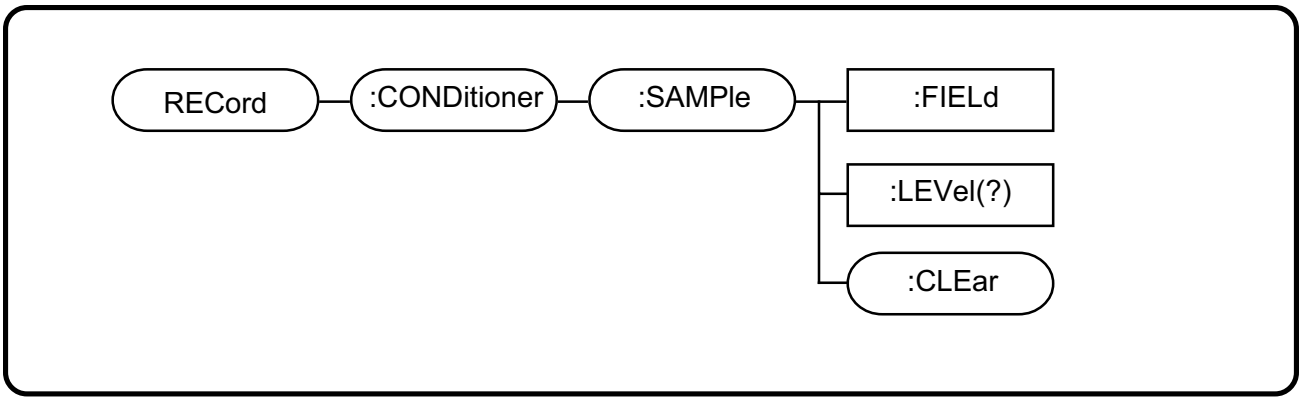
Parameter Definition

None

Examples

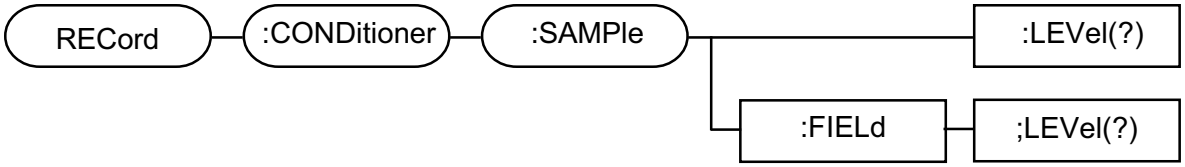
STIMULUS:COND:OFORMAT:FIELD ADDR;CLEAR
STIM:COND:OFOR:CLE

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Setting the Input Sample Threshold Voltage (NON-SCPI)



The RECord::::LEVel command sets the input sample threshold voltage for the specified record field. The threshold level can be entered as a floating point numeric or in scientific notation. Input voltages above the threshold level are detected as a logic "1," input voltages below the threshold level are detected as a logic "0." If multiple fields overlap, then the threshold settings for all overlapping pins will be set to the last parameters defined for any one of the fields. The RECord::::LEVel? query command returns the input sample threshold voltage for the specified record field.

:SAMPle Selects the Sample path of the RECORD:CONDITIONER subsystem.

Parameter Definition None

:FIELd<name | ALL> The optional FIELd parameter specifies the record type field that the LEVel parameters will act on. Record field types include Expected (EXP), Expected/Dontcare (ED), Algorithmic Expected (ALGE), and Hardware Expected (HEXP). If the optional FIELd parameter is used, then the FIELd and LEVel parameters must be separated by a semicolon. If the FIELd parameter is omitted, then the default record field is assumed. The default record field is defined by the RECord:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all record type fields.

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

ALL = All record fields will be set to the same input threshold setting.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

:LEVel<volts>

Parameter Definition **volts** = (-6.00 V to +12.00 V) Values can be specified as a floating point numeric or in scientific notation using exponential values. Optional V, MV, and UV suffixes can be used for engineering unit multipliers. The default engineering unit is volts (V).

Examples
```
RECORD:CONDITIONER:SAMPLE:FIELD DATA;LEVEL 2.5e+0v
REC:COND:SAMP:LEV 2.5V
```


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Setting the Input Sample Threshold Voltage (cont) (NON-SCPI)

:LEVel? Returns the input sample threshold voltage for the specified record field.

Response name volts | UNDEFINED {;name volts | UNDEFINED}

Parameter Definition **name** = any alphanumeric string and '_' (max 8 characters).

volts = the threshold setting specified in volts using scientific notation values from 6.000000e+00 to 1.200000e+01.

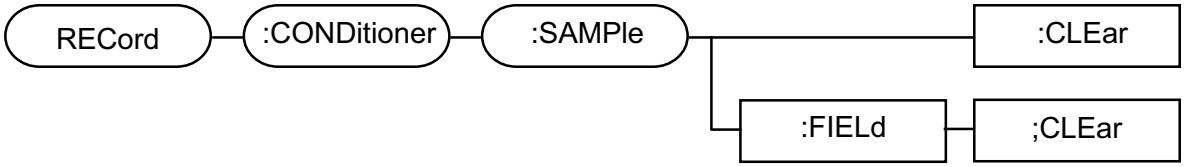
UNDEFINED = the threshold setting has not been defined for the specified field, or the threshold setting has been cleared.

Examples RECORD:CONDITIONER:SAMPLE:FIELD DATA;LEVEL?
DATA 2.5000000e+00

REC:COND:SAMP:LEV?
DATA 2.5000000e+00;INPUT UNDEFINED

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Clearing the Input Sample Threshold Settings (NON-SCPI)



The RECord:CONDitioner:SAMPle:CLEar command clears the input sample threshold voltage settings for the specified record field. The input sample voltage will be set to UNDEFINED. If multiple fields overlap, meaning they share common pins, then the voltage setting for all overlapping pin groups will be cleared.

:FIELd <name | ALL> The optional FIELd parameter specifies the record type field on which the sample mode and timing values will be cleared. Record field types include Expected (EXP), Expected/Dontcare (ED), Algorithmic Expected (ALGE), and Hardware Expected (HEXP). If the optional FIELd parameter is used, then the FIELd and CLEar strings must be separated by a semicolon. If the FIELd parameter is omitted, then the default record field is assumed. The default record field is defined by the RECord:FIELd command. The field name can also be specified by the literal string "ALL," where "ALL" refers to all record type fields.

Parameter Definition

name = any alphanumeric string and '_' (max 8 characters).

ALL = All record fields will be cleared.

Note

The FIELd parameter changes the destination field only for the same command but does not change the default field.

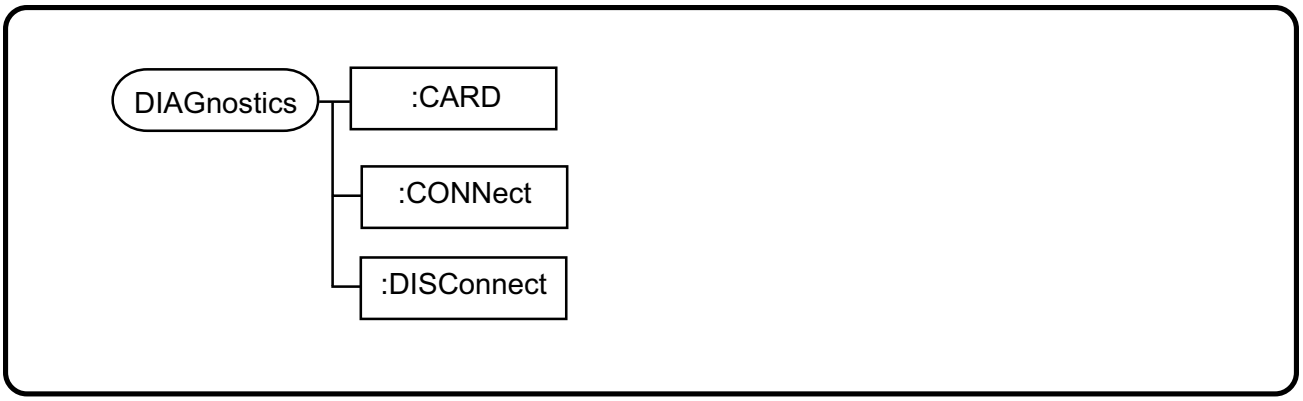
:CLEar Executes the clear function.

Parameter Definition None

Examples

```
RECORD:CONDITIONER:SAMPLE:FIELD:ADDR;CLEAR
REC:COND:SAMP:CLE
```


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Connecting Output Drivers for Diagnostic Testing (NON-SCPI)



Note

The DIAGnostics::::CONNect command executes immediately. The variable voltage commands; High, Low, Amplitude, and Offset will execute when the INITiate command is received.

The DIAGnostics::CONNect command "turns on" the output drivers for the specified SR5030 card slot and pin group. This command is used for troubleshooting the UUT or the SR5030 output drivers by applying an output voltage on the stimulus pins and measuring the actual voltage level. The SR5030 output drivers must be connected prior to executing the diagnostic self-test. Upon completion of the DIAGnostics:EXECute command, the output drivers will automatically be disconnected. Refer to Section 3.4.1 for additional information on diagnostic testing.

:CARD<card_num | ALL>

The CARD parameter specifies which SR5030 card number will be selected for connection, where "1" through "20" is the card number of the SR50XX I/O Modules. The card number can also be specified by the literal string "ALL," where all SR5030 system modules will be selected. If the CARD parameter string is not specified, then all SR5030 cards will be selected.

Parameter Definition

card_num = (1 - 20)

ALL = All SR5030 modules will be selected.

;CONNect<pin_group | ALL>

The CONNect command connects the specified SR5030 card pin group.

Parameter Definition

pin_group = (0 - 3); where pin group 0 selects pins 1-4, pin group 1 selects pins 5-8, pin group 2 selects pins 9-12, and pin group 3 selects pins 13-16.

ALL = all pin groups will be connected.

Examples

```
DIAGNOSTICS:CARD 2;CONNECT 2
DIAG:CARD ALL;CONN ALL
DIAG:CONN ALL
```


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Disconnecting Output Drivers for Diagnostic Testing (NON-SCPI)



Note

The DIAGnostics::::DISConnect command executes immediately. The variable voltage commands; High, Low, Amplitude, and Offset will execute when the INITiate command is received.

The DIAGnostics:;DISConnect command "turns off" the output drivers for the specified SR5030 card slot and pin group. This command is used in conjunction with the CONNect command for troubleshooting the UUT or the SR5030 output drivers. Upon completion of the DIAGnostics :EXECute command, the output drivers will automatically be disconnected. Refer to main manual for additional information on diagnostic testing.

:CARD<card_num | ALL>

The CARD parameter specifies which SR5030 card number will be selected for connection, where "1" through "20" is the card number of the SR50XX I/O Modules. The card number can also be specified by the literal string "ALL," where all SR5030 system modules will be selected. If the CARD parameter string is not specified, then all SR5030 cards will be selected.

Parameter Definition

card_num = (1 - 20)

ALL = All SR5030 modules will be selected.

;DISConnect<pin_group | ALL>

The DISConnect command disconnects the specified SR5030 card pin group.

Parameter Definition

pin_group = (0 - 3); where pin group 0 selects pins 1-4, pin group 1 selects pins 5-8, pin group 2 selects pins 9-12, and pin group 3 selects pins 13-16.

ALL = all pin groups will be connected.

Examples

```
DIAGNOSTICS:CARD 2;DISCONNECT 2
DIAG:CARD ALL;DISC ALL
DIAG:DISC ALL
```


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CHAPTER 4

Installation

Scope of Chapter

This chapter contains instructions for unpacking, inspecting, installing, and checking out the SR5030 CMOS I/O Module.

Unpacking and Inspection

Your SR5030 was thoroughly inspected and tested before shipment from the factory and is ready for immediate operation once all installation procedures have been completed. Carefully remove the instrument from its shipping carton and check for any obvious damage that may have occurred during shipment. If damage is found, report it to the freight carrier immediately. Interface Technology is not liable for damage that may have occurred during transit. Save the shipping carton and all packing material for possible future use.

Installation

Logical Addressing

Before installation, the logical address for the SR5030 must be set according to the requirements of the Slot-0 Controller. The address switches are numbered from one to eight. Switch 1 corresponds to the least significant bit (LSB) of the logical address. The address is entered in binary, where an ON switch sets the corresponding bit to "0", see Fig. 4-1.

Note

The logical address of the SR5030 CMOS I/O Module must be set to a higher value than the logical address of the SR5010 Timing/Control Module. If there is more than one SR5010 in a single VXI chassis, the address of an SR5030 located between any two SR5010s will be part of the lower addressed SR5010's system. The SR5030 with the lowest numbered logical address is I/O card #1. The next highest SR5030 logical address is I/O card #2. The highest SR5030 logical address is the most significant I/O card number. To verify all I/O modules have been recognized by the system, send a "SYSTEM:IDN?" query command.

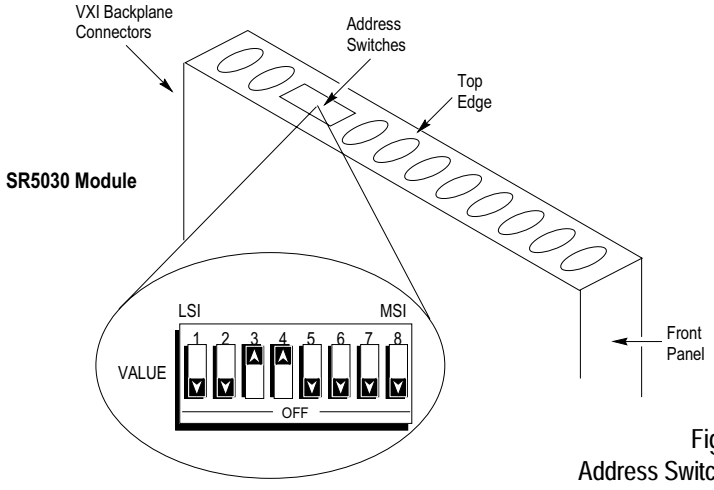


Figure 4-1
Address Switches Set to Logical Address 12.

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Slot Dependency

The SR5030 CMOS I/O Module may be installed in any available VXI chassis card slot except Slot-0 (occupied by the Slot-0 controller), and in any slot relative to the SR5010 Timing/Control Module. The SR5000 subsystem uses Bus Master functions to identify the I/O cards installed. This makes it possible to place the SR5030 in any slot within the VXI chassis, or even in another chassis connected by means of bus extenders such as the MXI bus.

Using Multiple Chassis.

If multiple chassis are used, the SR5010 and SR5030 interconnect cables must be lengthened and the SR5000 system must be recalibrated using the longer cable sets. If an existing (single chassis) SR5000 system needs to be expanded into a multi-chassis configuration, it must first be returned to the factory for recalibration. Contact the Interface Technology Customer Service Department to arrange for retrofit and recalibration.

Backplane Jumpers

The SR5030 does not use any of the IACK or BG3 signals. Instead, these signals are simply passed through. You may either remove or install jumpers for these VXI slots, as required.

Interconnections With Timing/Control Module

To connect the SR5030 CMOS I/O Module with the SR5010 Timing/Control Module, do this (see Fig. 4-2 and 4-3).

1. Remove the side cover from the SR5010 Timing/Control Module.
2. Thread the required number of SR5030 I/O Module interconnect cables through the access slot located on the front panel of the SR5010 Timing/Control Module (once cable per I/O module).
3. Plug the I/O module interconnect cables into their corresponding connectors located inside the SR5010 (Fig. 4-2).
4. Reinstall the side cover on the SR5010 module; insert the module into the VXI chassis.
5. Install the first SR5030 into the VXI slot immediately to the right of the SR5010 Timing/Control module (Fig. 4-3).
6. Connect the free end of the shortest I/O interconnect cable from the SR5010 to the CONTROL connector on the SR5030 I/O module installed immediately to the right of the SR5010 module (Fig. 4-3).
7. Install the next I/O module into the VXI slot immediately to the right of the previously installed I/O module (step 5); plug the next shortest SR5010 I/O interconnect cable into the CONTROL connector of that I/O module.

Note

You can control more than 10 I/O modules with a single SR5010 Timing/Control Module by using Bridge Cards to control two I/O modules with a single control cable, refer to the *Bridge Cards* supplement of this manual.

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8. Repeat step 7 for all remaining I/O modules.

9. Tighten the retaining screws at the top and bottom of all SR5030 I/O modules, and also those of the SR5010 Timing/Control Module.

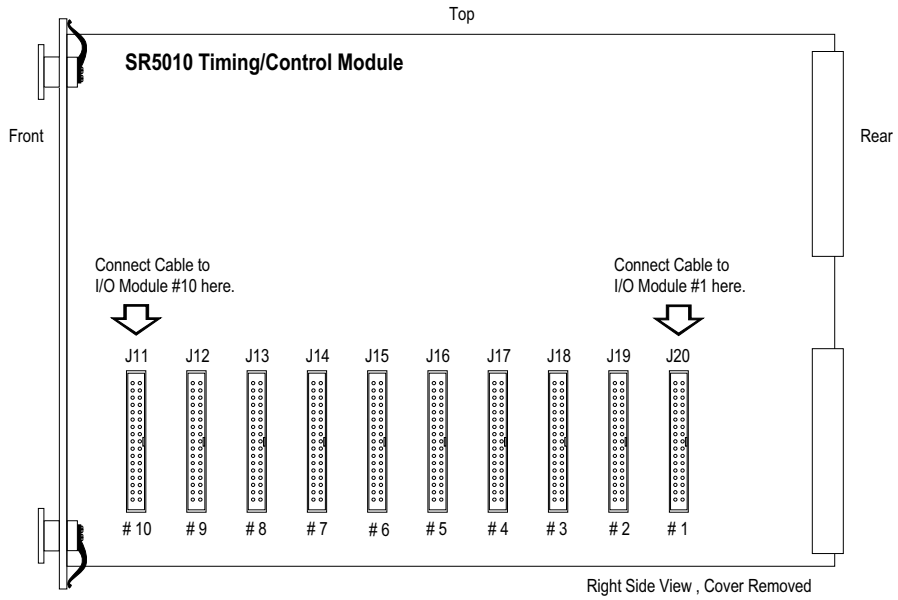
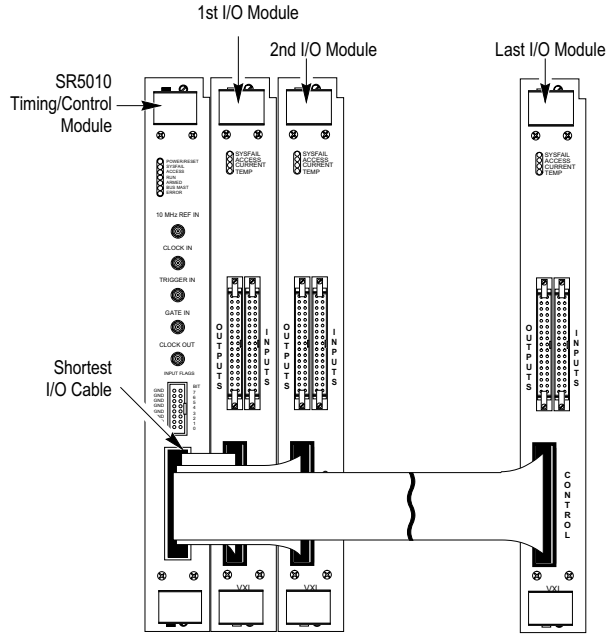


Figure 4-2
SR5010 I/O Control Connectors



] CAUTION [

Make these connections only with the cables that are supplied with the I/O modules (p/n 5030-002). This cable has a special wiring arrangement that differs from standard flat cable. Failure to observe this precaution may cause erratic behavior and/or damage to the SR5000 subsystem.

Turn power off before installing timing and control cables.

Figure 4-3
SR5010-to-SR5030
Interconnect Cables

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Input Termination

See Fig 4-4 and 4-5. The input receiver is the Elantec EL2252 device with programmable input threshold. The 100 Ω series resistor is used as a dampening resistor for the input receivers. The input termination is jumper selectable and can be configured for 100 Ω pull-down to ground, 100 Ω pull-up to -2.0 V, or no termination. The factory default termination setting is with the jumpers selecting the 100 Ω pull-down to ground. The pull-up/pull-down resistors are socketed and can easily be changed to other termination values. It is recommended that 50 Ω to -2.0 V termination be selected for ECL input levels and 100 Ω to ground be selected for TTL levels. To select the termination scheme, remove the top cover of the SR5030 and find the J2 header located near the I/O connectors. Configure the jumpers according to the desired termination scheme. Each jumper selects the termination scheme for a group of four channels.

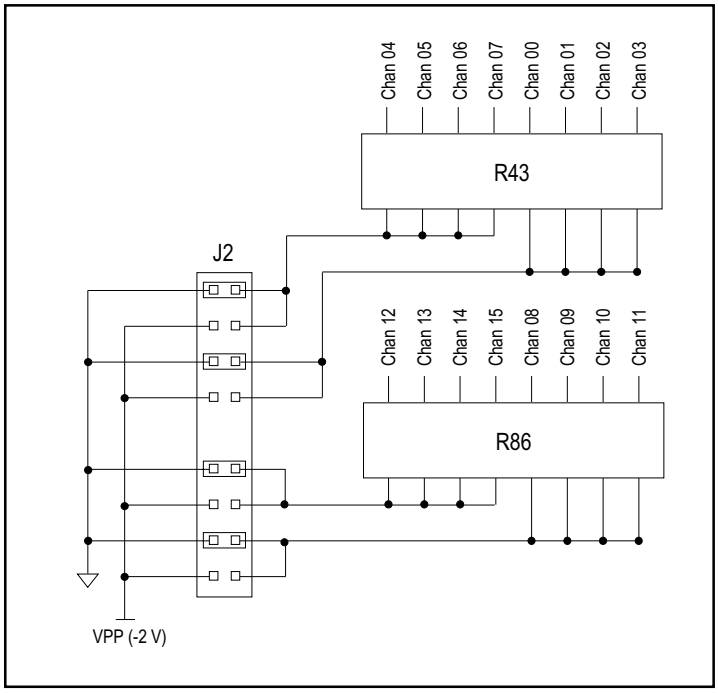


Figure 4-4
SR5030 Input Termination Jumpers

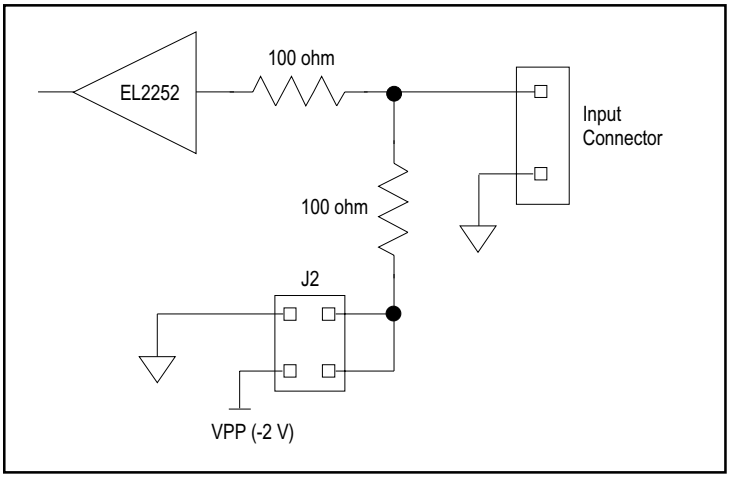


Figure 4-5
SR5030 Input Termination, Simplified Schematic

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Output Termination

See Fig 4-6. The output driver is the Elantec EL1056 programmable voltage driver. The output drivers have a 50Ω termination with short-circuit protection. The 51Ω resistor and 15 pF capacitor minimize overshoot, undershoot, and ringing on the output edge transitions.

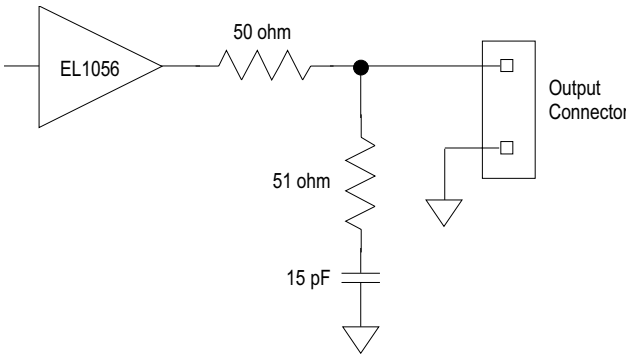
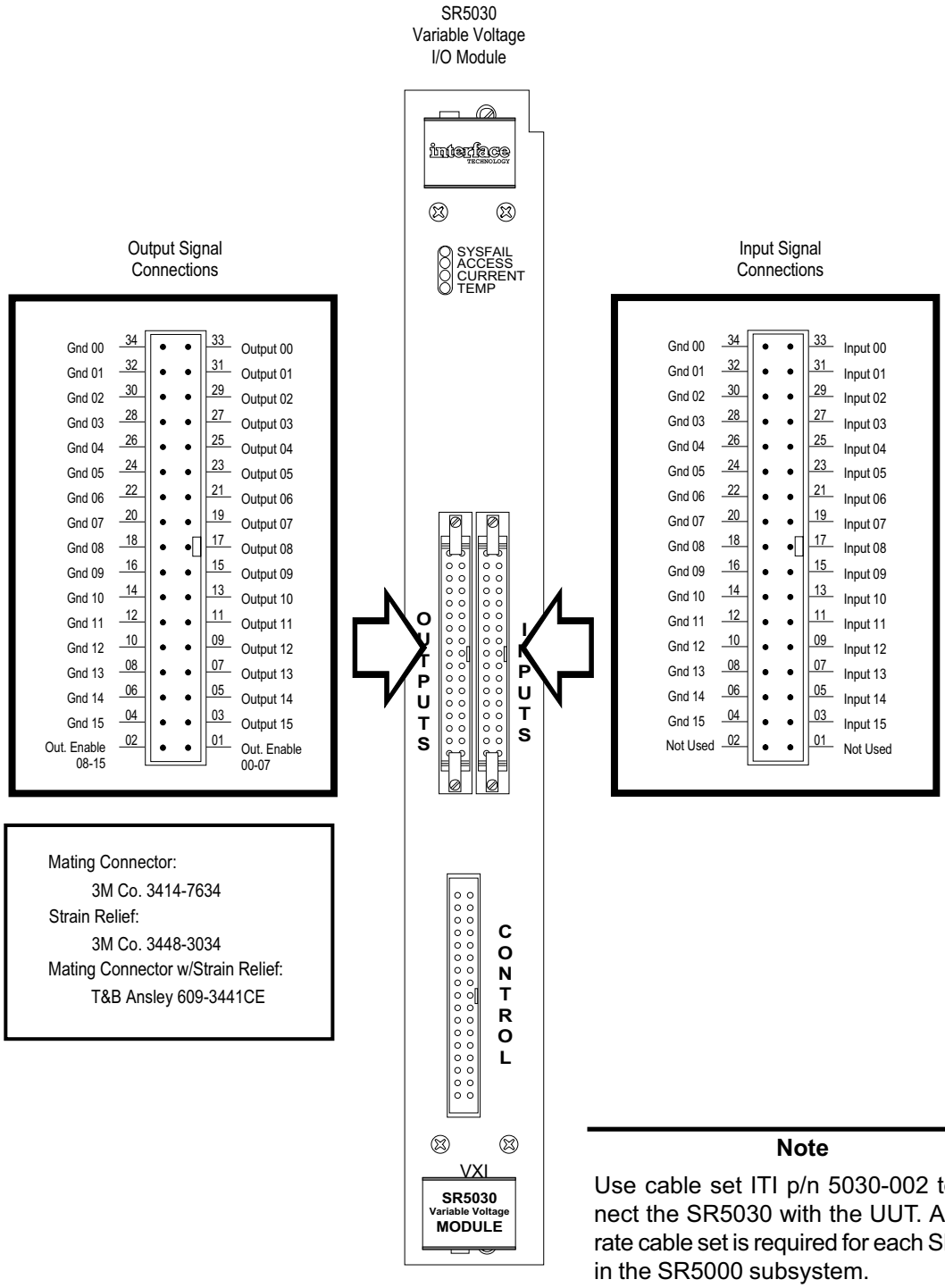


Figure 4-6
SR5030 Output Termination, Simplified Schematic

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Note

Use cable set ITI p/n 5030-002 to connect the SR5030 with the UUT. A separate cable set is required for each SR5030 in the SR5000 subsystem.

Figure 4-7
SR5030 I/O Pinouts

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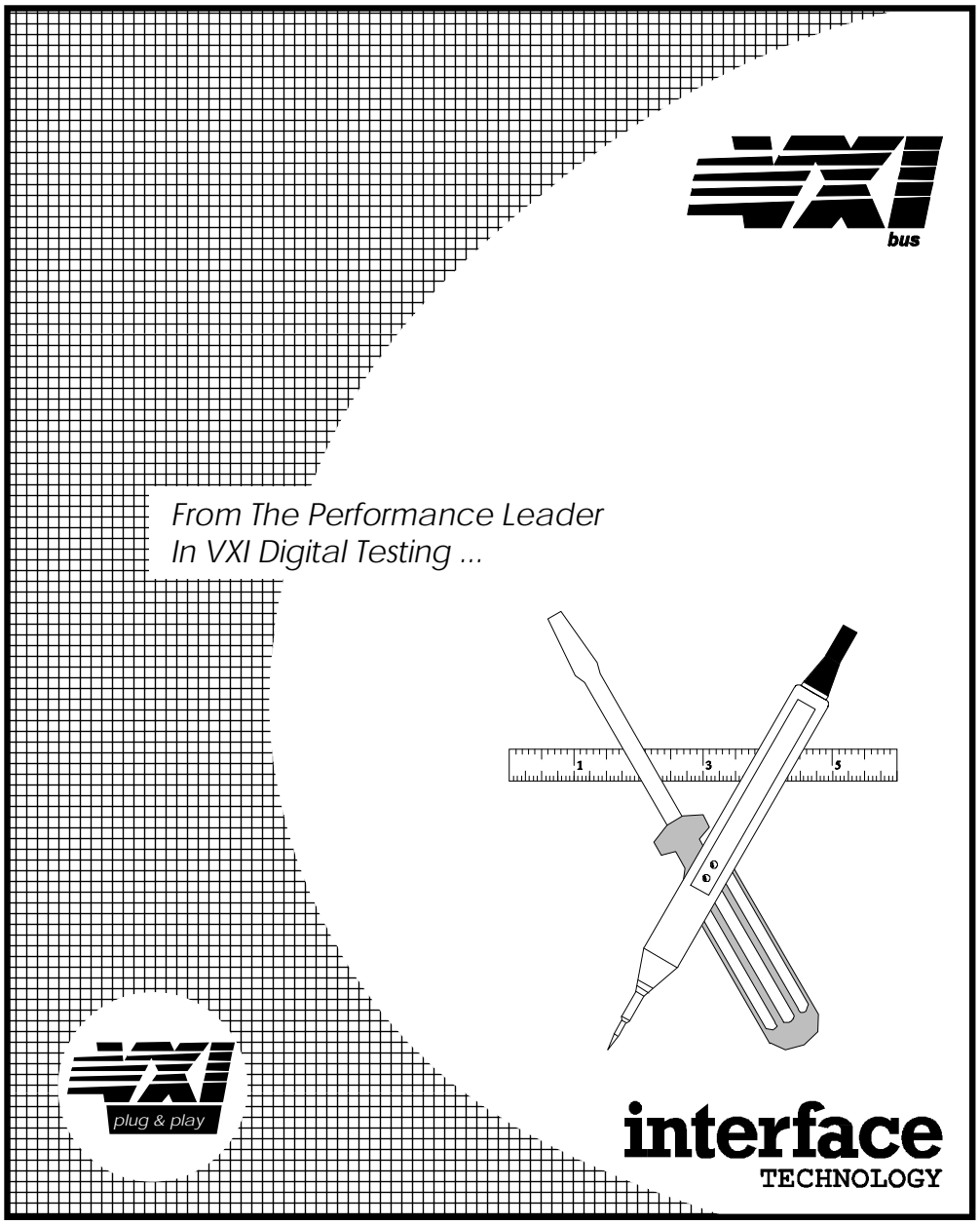
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TecNote **SR5030-01**

SR5010 / SR5030
Calibration Verification



Rev. 2.0
April, 1995

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TECNOTE

Calibration Verification, SR5010 - SR5030

Introduction

This TecNote describes a method of verifying the calibration of the Interface Technology SR5010 and SR5030 VXI modules by using standard test equipment with NIST traceable calibration. It does not describe the calibration itself, which requires special software using specific test instruments and fixtures.

This TecNote assumes that the SR50x0 modules are working and have passed self test. The operations verified are:

- ❑ system clock stability
- ❑ system clock accuracy
- ❑ output levels and timing
- ❑ input thresholds and timing.

No verification procedure is provided for programmable thresholds on the External Clock, External Trigger Input, nor External Gate Inputs.

Required Equipment

1. **VXI Cardrack** and power supply (providing all VXI specified voltages). A slot-0 controller is required to control the SR50x0 modules. The slot-0 controller may be an embedded computer, or an interface to some other host computer. The computer controlling the test operation will also require a GPIB interface for controlling other test instruments.

2. **Dual Input Counter/Timer - HP5335A, HP5370B** (or equivalent) for measuring frequency accuracy, frequency stability, pulse width, and time interval accuracy. Time interval accuracy better than 500 ps, with or w/o averaging.

3. **Digital Voltmeter - HP3458A** (or equivalent) with DC and AC RMS measurement capability. DC measurement better than .005% accuracy in 10 Vdc range (0.5 mV error) with at least 2.5 mV resolution. Better than 60 dB normal mode (ripple) rejection at 1 kHz. AC RMS measurement - true RMS measurement, 1% accuracy at 1 kHz in 10 Vrms range. Input impedance greater than 1M ohm in DC and RMS functions.

4. **Waveform Generator - Wavetek 1375, HP3325B** (or equivalent). AC + DC output amplitude ±5 Vdc into 50 ohms, +10 Vdc into high impedance preferable ... i.e., the sum of the peak AC voltage and the DC offset voltage should not "clip" below ±10 V peak into a high

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impedance. DC offset setting resolution 10 mV or better into 5 Vdc output range. The DC meter can be used if this resolution is not available (refer to Input Threshold test). AC setting resolution 50 mV or better in 5 V peak output range.

5. **SR5030 Calibration Verification Test Cable Set.** The output/input connector is a two-pin, dual row, connector terminating in a BNC connector. Two of these are required, both of equal length. Another BNC to SMB coax lead is required for interconnecting to the counter/timer. A wraparound cable terminating 16 signal/ground lead pairs is used to connect the SR5030 outputs to the inputs for input timing verification.

6. Various adapters to convert from SMB to BNC or banana plug, depending on instrument connector requirements, BNC "T" adapter, and BNC-to-BNC cables.

Verification Procedure

Overview.

The basic sequence of operations will be to verify output driver level accuracy using DC voltage readings. The output waveform timing is then verified using a counter/timer. The input threshold levels are then verified using a sine wave with a known DC offset voltage. Finally, the SR5030 outputs are used to verify input timing.

The verification philosophy is to test a particular voltage parameter at 10%, 50%, and 90% of full scale. This will verify that the calibration for any gain and offset errors is effective. If ranging or gain switching is used, additional readings will be taken after changing the ranging values.

Output Driver Level Verification.

The SR5030 outputs are connected to the DC meter using a single test cable, which must be moved for testing each of the 16 outputs per SR5030 module. The output drivers are set in volts, calibrated for no load conditions. The test sequence allows measurement of the low data reference level at 10%, 50%, and 90% voltage levels. The data pattern is changed to high and the same settings are verified at the high level. After testing the static output levels, the dynamical output levels are tested using an AC RMS meter.

The static test DC meter reading must be within ±150 mV DC for the low data reference output levels and within ±100 mV DC for the high data reference output levels.

The dynamic output pattern appears at a 1 kHz square wave with a 10 volt p-p output, which the RMS voltmeter must measure as 5.0 Vac RMS within ±75 mV.

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Note

For all code samples that follow: Comment lines begin with "##". Lines where a pause is required to verify a meter reading, or wait for operator input begin with "#@."

Execute Static Output Test

```
*rst
## ;define a general purpose test name and output field
test:def out_test:size 2
field:def all_outs:type out:pin clp16-1
## ;turn all output drivers on
stimulus:conditioner:oformat:connect
```

For n = 0 to 15 DO

```
## ;force output pin data value to low (0)
stimulus:armdata:mode on;pattern #h0
## ;set low to 10%
stimulus:conditioner:oformat:high 15.0v;low -4.0v
initiate
#@ ;measure here for output = -4.0v ±.0.15v
abort
## ;set low to 50%
stimulus:conditioner:oformat:low 4.0v
initiate
#@ ;measure here for output = 4.0v ± 0.15v
## ;set low to 90%
stimulus:conditioner:oformat:low 12.5v
initiate
#@ ;measure here for output = 12.5v ± 0.15v
abort
## ;force output pin data value to high (1)
stimulus:armdata:mode on;pattern #hffff
## ;set high to 10%
stimulus:conditioner:oformat:high -3.50v;low -6.0v
initiate
#@ ;measure here for output = 3.50v ± 0.10v
abort
```


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```
## ;set high to 50%
stimulus:conditioner:oformat:high 4.5v
initiate
#@ ;measure here for output = 4.5v ± 0.10v
abort
## ;set low to 90%
stimulus:conditioner:oformat:high 13.0v
initiate
#@ ;measure here for output = 13.0v ± 0.10v
#@ ;operator now moves test cable to next output
## ;sequence repeats 15 more times.
```

Next n

```
## ;turn all output drivers off
stimulus:conditioner:oformat:disconnect
################################################
## ;begin dynamic output RMS test here
*RST
test:def out_test:size 2
field:def all_outs:type ot:pin clp16-1
syst:freq 2.0 KHZ
field:name all_outs:radix hex
stimulus:vector 1;count 2;data:pattern 0,ffff
stimulus:conditioner:oformat:mode nrz,0.0 ns
## ;all 16 pins should output alternating 0-1 pattern
## ;with .5 ms per bit for a 1 kHz square wave effect
## ;set high to +5.0v and low to -5.0v
stimulus:conditioner:oformat:high 5.0v
stimulus:conditioner:oformat:low -5.0v
## ;run test and verify each output for 5.0 VRMS ± 75 mV
## ;using meter RMS AC function moving test cable down
## ;all 16 outputs while test runs
stimulus:conditioner:oformat:connect
system:programloop continuous
\initiate;*trg
#@ ;pause here for reading, move cable to all 16 in turn
```


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```
## ;stop test when complete
abort
*rst
```

Output Driver Timing Verification

Internal Timing Reference Verification.

The Clock Out connector of the SR5010 is connected to the timer counter input to measure the internal frequency reference. No programming is required to measure the clock output frequency.

The Clock Out signal is a TTL level suitable for driving a 50 ohm input. The input threshold level on the timer/counter should be set to an appropriate level ... e.g., 1.5 volts.

Measure the frequency of the system clock on channel A with a resolution of 1 Hz (25 ms gate on the HP-5335A counter). Passing criteria is from 25,012,812 Hz to 24,987,188 Hz). This criteria includes the error of the internal clock source and the counter.

Period Clock/Pulse Width Timing Verification.

The SR5030 output test cable from channel 00 is initially connected to the timer/counter start channel (A on HP counters), and then the other 15 outputs will be connected in turn for time interval measurement.

Note that to measure a high or low pulse width using some counters it may be necessary to use the Common switch to combine the A and B input channels, then set the start channel trigger edge opposite to the stop channel trigger edge (i.e., start-rising/stop-falling for high pulse width and vice-versa for low pulse width).

The timer/counter input channels are set for 0.0 volt input threshold level with 50 ohm termination. The test program will output a 25 MHz square wave on each output with a +2.0 Vdc high level and a -2.0 Vdc low level. At the 0 Vdc threshold level, the high and low pulse widths should be symmetrical 20 ns nominal bit times. The general procedure is ...

1. Measure Output 00 pin signal pulse width using counter time interval function. Using averaging if necessary, the timer resolution should be 0.1 ns. The pulse width passing criteria is from 16.8 to 23.2 ns for both rising and falling edge pulse widths.

2. Change the data rate to 400 Hz. Measure the pulse width as before with 1 ns resolution. Passing criteria is from 2,498,752 ns to 2,501,256 ns.

3. Repeat for all 15 remaining channels.

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Pulse Width Timing Test

```
*RST
test:def out_test:size 2
field:def all_outs:type ot:pin clp16-1

## ;set bit rate at 50 MHz - 20 ns bit width
syst:freq 50 MHZ
field:name all_outs:radix hex
stimulus:vector 1;count 2;data:pattern 0,ffff
stimulus:conditioner:oformat:mode nrz,0.0 ns
## ;all 16 pins should output alternating 0-1 pattern
## ;with 20 ns per bit or a 25 MHZ square wave
## ;set high to +2.0v and low to -2.0v so counter
## ;trigger input can be at 0v
stimuilus:conditioner:oformat:high 2.00v
stimulus:conditioner:oformat:low -2.00v
stimulus:conditioner:oformat:connect
system:programloop continuous
initiate;*TRG
## ;verify high pulse width and low pulse width within spec
#@ ;pause here for reading, move cable to all 16 in turn
## ;stop test when complete
abort
syst:freq 400 Hz
init;*trg
## ;verify high pulse width and low pulse width within spec
#@ ;pause here for reading, move cable to all 16 in turn
*rst
```


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Output Skew.

All the output channel edges are measured with respect to a reference (Output 00) and verified to have their output channel delays within the timing skew tolerance of each other on a given SR5030 module. The test cable pair for the outputs being compared must be matched in length to within .25 inch.

The SR5030 outputs will be set to +2.0 volts and -2.0 volts as in the previous test.

The general test sequence will be ...

1. The timer/counter *start channel* input is connected to the *Output 00* connector of the SR5030 module. The timer/counter *stop channel* input is then connected, in turn, to each of the other SR5030 outputs starting with *Output 01*. The *timer input thresholds* are set up to 0.0 volt. The *timer* is set for 0.1 ns resolution using averaging, if necessary.

2. *Data output pattern* is set for all ones with Return-to-Zero (RZ) formatting. The *system test rate* is set for 10 MHz. The *output assert time* for *Output 00* will be at 10 ns, the *output width* will be 80 ns. The 10 ns delay from the reference to the timed channel is to avoid negative time measurements for channel skew.

3. The test pattern is output continuously with the timer/counter measuring the *average time interval* from *start input* to *stop input* using at least a 1000 sample count. This time interval from the *Output 00* pin will be used as the reference for other pins. This reading can be stored as the counter reference (or *offset*, if this feature is available).

4. Move the test connector from *Output 01* to the next output pin (*Output 02)* and measure the time interval as before. The time interval shall be within ±4.2 ns of the reference interval from the first pin.

5. Repeat for remaining outputs 03-15.

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Output Skew Timing Test

```
*rst
test:def out_test:size 2
## ;channel one will be clock at 10 ns, all others at 20 ns
field:def clk:type ot:pin clpl
field:fef all_outs:type ot:pin clp16-2
field:name all_outs:radix hex
field:name clk:radix bin
stimulus:vector 1;count 2;data:field clk;pattern 0,1
stimulus:vector 1;count 2;data:field all_outs;pattern 0,7fff
stimulus:conditioner:oformat:field clk;mode rz,10.0ns,70ns
stimulus:conditioner:oformat:field all_outs;mode rz,20.0ns,80ns
## ;all 16 pins should output alternating 0-1 pattern
## ;with 100 ns per bit and varying duty cycle
## ;set high to +2.0v and low to -2.0v
## ;trigger input can be at 0 v
stimulus:conditioner:oformat:field clk;high 2.00v;low -2.0v
stimulus:conditioner:oformat:field all_outs;high 2.0v;low -2.00v
stimulus:conditioner:oformat:field clk;connect
stimulus:conditioner:oformat:field all_outs;connect
system:programloop continuous
initiate;*trg
## ;verify channel 1-15 variance from reference within spec
#@ ;pause here for reading, move cable to all 16 in turn
## ;stop test when complete
abort
*rst
```


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Output Edge Placement Timing Verification.

The *output edge delay calibration* is verified by timing the pulse widths as they are varied across their programmable range. The timer/counter time interval function is used to measure the pulse width of each channel in turn. Counter/timer input thresholds are then reset for 0.0 volts, SR5030 outputs for ±2.0 volts.

The general test sequence is as follows:

1. Output data vectors are set for all one with Return-to-Zero (RZ) formatting. The test data rate is set for 10 MHz. Assert time for the signal is set at 0.0 ns, width is 80 ns.

2. The counter/timer *start channel* is connected to the output under test with an input threshold of 0 Vdc with 50 ohm termination. The timer is set for 0.1 ns resolution, using averaging if necessary.

3. The test is run continuously and the average high pulse width (from rising to falling edge) is measured using at least 1000 samples. Passing criteria is initially 80 ns ±5.2 ns (nominal ± width error ± 2 LSD timer).

4. Repeat the above test while decreasing the pulse width from 80 ns to 70 ns in 1.0 ns steps. This checks the fine delay calibration.

5. Set the pulse width to 60 ns. Increase the assert time from 0 to 10 ns in 1 ns steps verifying each pulse width for 60 ns ± 5.2 ns.

6. Repeat the timing test while reducing the pulse width from 60 ns to 10 ns in steps of 10 ns. Each pulse width must be nominal ±5.2 ns.

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Output Edge Timing Test

```
*rst
test:def out_test:size 2
field:def all_outs:type ot:pin clp16-1
syst:freq 10 MHZ
field:name all_outs:radix hex
stimulus:vector 1;count 2;data:field all_outs;pattern 0,ffff
stimulus:conditioiner:oformat:field all_outs;mode rz,0.0ns,80ns
## ;all 16 pins should output alternating 0-1 pattern
## ;with 100 ns per bit time, varying duty cycle
## ;set high to +2.0v and low to -2.0v
## ;trigger input can be at 0v
stimulus:conditioner:oformat:field all_outs;high 2.0v;low -2.00v
stimulus:conditioner:oformat:field all_outs;connect
system:programloop continuous
initiate;*TRG
## ;nominal  80 ns, tolerance ±5.2 ns
## ;verify pulse width is within specified tolerance.
#@ ;pause here for reading, move cable to all 16 in turn
## ;stop test when complete
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,79ns
init;*trg
## ;nominal 79 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,78ns
init;*trg
## ;nominal 78 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,77ns
init;*trg
## ;nominal 77 ns, tolerance ±5.2 ns
```


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```
## ;verify pulse width within specified variance of nominal
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,76ns
init;*trg
## ;nominal 76 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,75ns
init;*trg
## ;nominal 75 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,74ns
init;*trg
## ;nominal 74 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,73ns
init;*trg
## ;nominal 73 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,72ns
init;*trg
## ;nominal 72 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,71ns
init;*trg
## ;nominal 71 ns, tolerance ±5.2 ns
```


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```
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,70ns
init;*trg
## ;nominal 70 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,1.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,2.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,3.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,4.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
```


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```
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,5.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,6.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,7.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,8.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,9.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,60ns
init;*trg
## ;nominal 60 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
```


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```
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,50ns
init;*trg
## ;nominal 50 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,40ns
init;*trg
## ;nominal 40 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,30ns
init;*trg
## ;nominal 30 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,20ns
init;*trg
## ;nominal 20 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
stimulus:conditioner:oformat:field all_outs;mode rz,0.0ns,10ns
init;*trg
## ;nominal 10 ns, tolerance ±5.2 ns
## ;verify pulse width within specifications
#@
abort
*rst
```


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Input Threshold Verification

The input thresholds are verified using a sine wave input with a DC offset to achieve a data input pattern with equal numbers of ones and zeros. The function generator is connected to the input channel under test and set to generate a 1 kHz sine wave. In order to test the input receivers across their full range (-6 Vdc to +12 Vdc), DC offsets within 10% of these values are desirable. Since many function generators are limited to ±5 V into 50 ohms, compromise is required.

The SR5030 input receivers are factory shipped without any input termination (high impedance input), and many function generator outputs will double to ±10 V AC+DC under such conditions. The lower threshold limit can be tested at about -4.0 Vdc (2 Vdc setting value) with a 1.0 Vp-p sine wave. The upper threshold limit can be tested at about 8.0 Vdc (4.0 Vdc setting) with a 1.0 Vp-p sine wave.

The input threshold is set for -4 volts, initially, and will sample input data at X100 the input frequency (100 kHz) for a time equal to exactly one period of the input frequency (100 samples). The number of resulting one and zero readings should be the same, 50 ±3 readings. The SR5000 compare memory is used to achieve a count of the number of vectors read that matched the expected input on a given pin. Since the expected input is constant, half the 100 vectors in the test should cause errors if the SR5030 input threshold matches the sine wave DC offset. An error of 50 mV will cause a count error of 7-8 vectors. If the number of vectors is too high, increasing the DC offset of the sine wave will reduce it, and vice versa.

Note that the sine wave frequency must be set to 1000 Hz ±1 Hz, so if the setting accuracy of the function generator is in doubt, as frequency counter should be used to set the frequency. In addition, most function generators are designed to output into a 50 ohm load, so to their output setting value will be half the desired value to achieve the test voltages required.

The DC offset setting resolution on many function generators will not meet the required accuracy for this test, making it desirable to connect a DC meter to the sine wave signal to measure offset directly. Virtually any DC meter will have the required AC rejection at 1 kHz signal frequency.

Passing criteria for the threshold settings is ±100 mV + any setting error for function generator DC offset or meter reading error.

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The General Procedure is:

1. Connect SR5030 input under test to function generator output and DC meter using a BNC "T" adapter. The function generator is set for a 0.5 Vp-p amplitude with -2.0 Vdc offset. This should give an output of 1.0 Vp-p with -4.0 Vdc offset into a high impedance.
2. Set test system frequency at 100 kHz.
3. Record 100 values for the pin under test at 100 kHz. Read the number of error vectors recorded for comparison.
4. Add or subtract the DC offset, as required, and repeat the test to obtain equal ones and zeros ±4 responses.
5. Read DC content of signal using DC meter. Pass/fail criteria is ±100 mV of threshold setting.
6. Repeat for 0 and 8 Vdc offsets on same pin.
7. Repeat for remaining 15 pins by moving test cable.

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Input Threshold Verification

```
##############################
## ;Input threshold level test starts here
*RST
test:def in_test:size 100
field:def all_outs:type ot:pin clp16-1
## ;set input frequency sine wave for 1 kHz for X100 sampling
syst:freq 100 khz
field:name all_outs:radix hex
field:def all_ins:type rec:pin clp16-1
record:field all_ins
## ;set input threshold to 10%
record:conditioner:sample:field all_ins;level -4.0v
record:conditioner:sample:field all_ins;mode edge,0ns
record:trace:sequence 1:define:filter error:record com
field:define in_chk:type ed:pin clp16-1
record:vector 1;count all;data:field in_chk;fill:type rep;pattern
#h0;exec
system:programloop 1
initiate
*TRG
abort
test:name in_test:stat?
## ;nominal offset -4.0 Vdc
## ;set sine wave generator DC offset to nominal threshold
## ;verify that count of vectors recorded is within tolerance
#@ ;pause to check vector count before next test
record:conditioner:sample:field all_ins;level 0.0v
initiate
*TRG
abort
test:name in_test:stat?
## ;nominal offset 0 VDC
## ;set sine wave generator DC offset to nominal threshold
## ;verify that count of vectors recorded is within tolerance
#@ ;pause to check vector count before next test
```


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```
record:conditioner:sample:field all_ins;level 8.0v
initiate
*TRG
abort
test:name in_test:stat?
## ;nominal offset 8.0 Vdc
## ;set sine wave generator DC offset to nominal threshold
## ;verify that count of vectors recorded is within tolerance
#@ ;pause to check vector count before next test
## ;now move test cable and change compare pattern to match
## ;and start back at threshold 10% (-4 V)
record:vector 1;count all;data:field in_chk;fill:type rep;pattern
#h1;exec
record:conditioner:sample:field all_ins;level -4.0v
initiate
*trg
abort
test:name in_test:stat?
## ;nominal offset -4.0 VDC
## ;set sine wave generator DC offset to nominal threshold
## ;verify that count of vectors recorded is within tolerance
#@ ;pause to check vector count before next test
record:conditioner:sample:field all_ins;level 0.0v
initiate
*trg
abort
test:name in_test:stat?
## ;nominal offset 0.0 VDC
## ;set sine wave generator DC offset to nominal threshold
## ;verify that count of vectors recorded is within tolerance
#@ ;pause to check vector count before next test
record:conditioner:sample:field all_ins;level 8.0v
initiate
*trg
abort
```


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```
test:name in_test:stat?
## ;nominal offset 8.0 VDC
## ;set sine wave generator DC offset to nominal threshold
## ;verify that count of vectors recorded is within tolerance
#@ ;pause to check vector count before next test
## ;now move test cable and change compare pattern to match
record:vector 1;count all;data:field in_chk;fill:type rep;pattern
#h2,exec
## ;NOTE - repeat above pattern changing compare pattern each time
## ;cable is moved with the following patterns

record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h4;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h8;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h10;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h20;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h40;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h80;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h100;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h200;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h400;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h800;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h1000;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h2000;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h4000;exec
record:vector 1;count all;data:field in_chk;fill:type rep;pattern #h8000;exec

## ;stop test when complete
abort
```


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Input Timing Verification

With confidence in the output levels, output timing, and input thresholds established, the outputs can now be used to verify operation of the input timing. The 16 output pins are each connected to the corresponding input pin using a wrap around cable as short as possible. Output patterns with varying edge placements are used to verify input setup and hold times.

All inputs are set to capture on the same clock edge, and that clock edge is set for 40 ns after the cycle clock. The output memory is set to output an alternating one-zero pattern, starting with one. The capture clock edge starts at less than the setup time + error, so that the initial pattern captured will be zero-one-zero. The capture edge is then moved to be within the setup time + error range so that the data pattern captured will be one-zero-one. Input setup for the SR5030 variable inputs is 18 ns minimum, and hold time is zero. The error in edge placement is 3.0 ns. The test will be run at a test system frequency of 10 MHz.

The SR5000 expected data memory is used to record errors resulting from the real time comparison. At the end of the 100 vector test, the memory is searched for errors and the result should be a null count.

The recommended procedure is as follows:

1. Set output data pattern for all channels to alternating one-zero with a depth of 100 output vectors. All data output edges placed at 40 ns into cycle. Normal data formatting, NRZ. Output high level set to +2 Vdc, output low set to -2 Vdc.
2. The test frequency is set for 10 MHz, all input thresholds set for 0.0 volts. Edge capture mode is selected with the clock edge set to 37 ns into cycle (40 ns - 3 error).
3. The test is started and 100 cycles output and captured. The results are verified to be alternating zero-one-zero patterns.
4. The capture edge is moved to 61 ns (40 + 18 setup + 3 error). The test is run again with 100 cycles, and the results verified to be a one-zero-one pattern.
5. The test is repeated using the other edge capture clock.
6. The test is repeated with the capture edge held at 40 ns and the data output edge varied from 37 ns to 61 ns.

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Input Timing Verification Test

```
*rst
test:def in_test:size 100
field:def all_outs:type ot:pin clp16-1
## ;input edge timing test starts here
syst:freq 10 mhz
field:name all_outs:radix hex
## ;data output pattern 1,0,1
stim:vec 1;count all;data:field all_outs;fill:type alt;patt
#hffff;exec
stimulus:conditioner:oformat:mode nrz,40.0 ns
stimulus:armdata:mode on;pattern #h0
stimulus:conditioner:oformat:high 4.00v
stimulus:conditioner:oformat:low 0v
stimulus:conditioner:oformat:connect
field:def all_ins:type rec:pin clp16-1
rec:field all_ins
record:conditioner:sample:field all_ins;level +2.0
record:conditioner:sample:field all_ins;mode edge,37ns
record:trace:sequence 1:define:filter error:record always
## ;all 16 pins should output alternating 1,0,1 pattern
## ;with 100 ns per bit
field:define in_chk:type ed:pin clp16-1
rec:vector 1;count all;data:field in_chk;fill:type alt;pattern
#h0;exec
system:programloop 1;initiate
*trg
abort
test:name in_test:stat?
rec:vec 1;count all;data:field all_ins;search:patt #h0;mode ne;occ
all;vector?
#@ ;verify result is null count on error search
record:conditioner:sample:field all_ins;mode edge,53ns
## ;now fill expected with 1,0,1 pattern
rec:vec 1;count all;data:field in_chk;fill:type alt;patt #hffff;exec
initiate
*trg
```


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```
abort
test:name in_test:stat?
rec:vec 1;count all;data:field all_ins;search:patt #h0;mode ne;occ
all;vector?
#@ ;verify result is null count on error search
## ;now fix capture edge at 40, move data
record:conditioner:sample:field all_ins;mode edge,40 ns
stimulus:conditioner:oformat:mode nrz,43.0 ns
## ;fill expected with 0,1,0 pattern
rec:vector 1;count all;data:field in_chk;fill:type alt;pattern
#h0;exec
initiate
*trg
abort
test:name in_test:stat?
rec:vec 1;count all;data:field all_ins;search:patt #h0;mode ne;occ
all;vector?
#@ ;verify result is null count on error search
stimulus:conditioner:oformat:mode nrz,27.0 ns
## ;fill expected with 1,0,1 pattern
rec:vector 1;count all;data:field in_chk;fill:type alt;pattern
#hffff;exec
initiate
*trg
abort
test:name in_test:stat?
rec:vec 1;count all;data:filed all_ins;search:patt #h0;mode ne;occ
all;vector?
#@ ;verify result is null count on error search

   ;END of TEST
```


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