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SR5060

LVDS I/O Module

For SR5000 Digital Test Subsystem

- 32 Input/Output Pins per Module and 32 Tristate Output Pins
- 64K Vectors per Channel at 50 MHz Data Rates
- RAM-Backed and Algorithmic Pattern Generation
- NRZ, RZ, RONE, RTC, and RI Output Data Formats Supported
- 8 Stimulus Timing Generators per Module (Four Assert/Deny Pairs)
- Four Response Generators per Module
- <100 ps Edge Placement Resolution

High Channel Density

The SR5060 LVDS I/O Module provides 32 stimulus pins, 32 tristate output pins, and 32 response pins, operating at 50 MHz, in a single C-size slot. Up to 20 I/O modules may be controlled by the SR5010A Timing/Control Module for a total of 640 I/O pins. Input and output pins are grouped on separate connectors, providing the most efficient method of interfacing to the UUT. Bidirectional capability is accomplished by externally connecting the input pins to the output pins.

Seven Distinct I/O Memory Types

The SR5060 I/O Module contains seven separate memory banks, each 64K vectors in depth, for generating stimulus patterns, expected response patterns, and recording UUT response data. The Stimulus Memories consist of the Output, Tristate and Algorithmic Output memories. The Output Memory contains the actual data patterns to be generated to the UUT. Tristate Memory provides tristate control which supports bidirectional I/O. The Algorithmic Output Memory determines which algorithmic pattern will be output.

The Response Memories consist of the Expect, Mask, and Algorithmic Expect memories. The Expect Memory contains the expected response data for the UUT and is the basis for input compare operations. The Mask Memory determines which patterns are to be ignored for input response comparison. Algorithmic Expect Memory determines which algorithmic expect pattern will be compared against the UUT input response.

Record Memory is used to store either the UUT response data or the result of the comparison between the UUT response data and the expected response pattern.

12 Timing Generators per Module

Each I/O module contains 12 separate timing generators, eight for stimulus edge placement and four for response edge placement. The output pins use four of the stimulus timing generators to define the leading (assert) and trailing (deny) edges of the stimulus signal. Used with data formatting, the output pins acquire the ability to produce clocks and strobes within one test cycle. The response pins use the four response timing generators to define the sample and compare edges to determine when to compare and record UUT response data.

Multiple Data Formats

The stimulus pins may be independently programmed for any of the following formats: Non-Return-to-Zero (NRZ), Return-to-Zero (RZ), Return-to-One (RONE), Return-to-Complement (RC), and Return-to-Inhibit (RI). The formats are applied to the selected stimulus pins to force the outputs to the defined state when the pin is not actively driving the programmed state. This allows clocks and strobes of either polarity to be generated in a single test cycle, or allows bi-directional control of data busses.

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*SR5060 SPECIFICATIONS***

Channels per Module:

Inputs	32
Outputs	32

Memory Types:

Stimulus	Output, Tristate, Algorithmic
Response	Expect, Mask, Algorithmic
Record	

Memory Depth:

Memory Depth	65,500 vectors

Output Timing:

Clock Pairs (assert/deny)	4 per I/O module
Delay Range	One clock period
Resolution	<100 ps (1/256 of data rate), monotonic
Delay Accuracy	2.0 ns typ., 3.0 ns maximum
Output Pulse Width	2.0 ns (high or low inputs)
Pulse Width Accuracy	3.0 ns typ., 5.0 ns maximum

Skew:

Same Module	±2 ns typical, ±4 ns maximum
SR5060-SR5060	±3 ns typical, ±5 ns maximum

Data Formats:

RZ	Return to Zero
NRZ	Non-Return to Zero
RONE	Return to One
RC	Return to Complement
RI	Return to Inhibit/Tristate

Output Drivers:

Type	LVDS 2.5/3.3 V	LVDS EXT 2.5/3.3 V	BLVDS 2.5 V
Voh	1.575 max.	1.785 max.	n/a
Vol	0.925 min.	0.705 min.	n/a
Vod*	n/a	n/a	2.5 to 0.450 V
Tout*	n/a	n/a	n/a

** Vod = output differential voltage*
Tout = output termination

Input Receivers:

Type	LVDS 2.5/3.3 V	LVDS EXT 2.5/3.3 V	BLVDS 2.5 V
Vid*	0.100 min.	0.100 min.	0.100 min.
Vicm*	0.200 to 2.80	0.200 to 2.80	0.200 to 2.80
Tin*	100 ohm diff.	100 ohm diff.	100 ohm diff.

* *Vid = input differential voltage*
Vicm = input common mode voltage
Tin = input termination

Input Sample / Compare Modes:

Formats	Edge
Range	One period clock cycle
Resolution	<100 ps (1/256 of data rate), monotonic
Accuracy	±1 ns typical; ±2 ns maximum

Input Timing:

Sample/Compare Clocks	Two per card (edge mode)
Input Delay Range	One clock period
Resolution	<100 ps (1/256 of data rate), monotonic

VXI Specifications

Interface Compatibility:

Type	Register-based, servant only (controlled by SR5010)
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Memory	2 MB VME A32/D32

Power Requirements:

+5.0 volts	9.5 A	47.5 W
-5.2 volts	4.3 A	21.8 W
+12.0 volts	0.1 A	1.2 W
-12.0 volts	0.1 A	1.2 W
-2.0 volts	2.8 A	5.6 W

Total Power		77.3 W

Cooling Requirements:

Per-slot Average	77 W maximum
Airflow	6 L/sec @ 0.38 mm water pressure for 10°C temperature rise

Environmental Specifications:

Temperature	Storage = -40°C to +75°C Operating = 0°C to +45°C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

VXI Plug & Play

** Specifications subject to change without notice.

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