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SR5170

100 MHz PECL I/O Module For SR5000 Digital Test Subsystem

- 16 Input/Output Pins per Module and 16 Tristate Output Pins
- 128K Vectors per Channel at 100 MHz Data Rates
- RAM-Backed Pattern Generation
- 8 Stimulus Timing Generators per Module (Four Assert/Deny Pairs)
- NRZ, RZ, RONE, RTC, and RI Output Data Formats Supported
- Four Response Generators per Module
- <100 ps Edge Placement Resolution

High Channel Density

The SR5170 PECL I/O Module provides 16 stimulus pins, 16 tristate output pins, and 16 response pins, operating at 100 MHz, in a single C-size slot. Up to 20 I/ O modules may be controlled by the SR5010A Timing/Control Module for a total of 320 I/O pins at data rates to 100 MHz.

Five Distinct I/O Memory Types

The SR5170 I/O Module contains five separate memory banks, each 128K vectors in depth, for generating stimulus patterns, expected response patterns, and recording UUT response data. All memory banks operate at full 100 MHz data rates when configured for 16 channel operation. The Stimulus Memories contain the Output and Tristate Control patterns, which are used to define the stimulus output to the UUT. The tristate memory drives separate output pins that are used to control external pin drivers, as the SR5170's outputs are not directly tristated.

The Response Memories contain the Expect, Mask and Record memories. The Expect and Mask patterns are used to define the expected response from the UUT, and to ignore response data bits on a vector-by-vector basis. The Record Memory is used to store either the response data or the result of the comparison between the response data and the Expect Memory. It is operated independently in a manner much like a logic analyzer. A sixteen level state machine and nine system-wide comparators are used to control what data is saved in the memory. In addition to the record memory, each input channel is provided with a 16-bit CCITT CRC register for signature analysis applications.

12 Timing Generators per Module

Each I/O module contains 12 separate timing generators, eight for stimulus edge placement and four for response edge placement. The output pins use four of the stimulus timing generators to define the leading (assert) and trailing (deny) edges of the stimulus signal. Used with data formatting, the output pins acquire the ability to produce clocks and strobes within one test cycle. The response pins use the four response timing generators to define the sample and compare edges to determine when to compare and record UUT response data.

Multiple Data Formats

The stimulus pins may be independently programmed for any of the following formats: Non-Return-to-Zero (NRZ), Return-to-Zero (RZ), Return-to-One (RONE), Return-to-Complement (RC), and Return-to-Inhibit (RI). The formats are applied to the selected stimulus pins to force the outputs to the defined state when the pin is not actively driving the programmed state. This allows clocks and strobes of either polarity to be generated in a single test cycle, or allows bi-directional control of data busses.

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*SR5170 SPECIFICATIONS***

Channels per Module:

Inputs	16
Outputs	16

Memory Types:

Stimulus	Output, Tristate Control
Response	Expect, Mask
Record	

Memory Depth:

Memory Depth:	128K vectors

Output Timing:

Clock Pairs (assert/deny)	4 per I/O module
Delay Range	One clock period
Resolution	<100 ps (1/256 of data rate), monotonic
Delay Accuracy	2.0 ns (typical), 3.0 ns (maximum)
Output Pulse Width	2 ns (high or low inputs)
Pulse Width Accuracy	3.0 ns (typical), 5.0 ns (maximum)

Skew:

Same Module	±2 ns (typical), ±4 ns (maximum)
SR5170-SR5170	±3 ns (typical), ±5 ns (maximum)

Data Formats:

RZ	Return to Zero
NRZ	Non-Return to Zero
RONE	Return to One
RC	Return to Complement
RI	Return to Inhibit

Output Drivers:

Type	LVPECL 3.3 V
Voh	1.920 V to 2.280 V
Vol	1.060 V to 1.430 V
Output Termination	50 ohms

Input Receivers:

Type	LVPECL 3.3 V
Vih	1.4920 V to 2.720 V
Vil	0.860 V to 2.125 V
Vid*	0.300 min.
Input Termination	100 ohm differential

* *Vid = input differential voltage*

Input Sample / Compare Modes:

Formats	Edge
Range	One period clock cycle
Resolution	<100 psec (1/256 of data rate), monotonic
Accuracy	±1 ns (typical), ±2 ns (maximum)

Input Timing:

Sample/Compare Clocks	Two per card (edge mode)
Input Delay Range	One clock period
Resolution	<100 ps, (1/256 of data rate), monotonic

VXI Specifications

Interface Compatibility:

Type	Register-based, servant only (controlled by SR5010A)
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Memory	2 MB VME A32/D32

Power Requirements:

+5.0 volts	9.5 A	47.50 W
-5.2 volts	4.2 A	21.84 W
+12.0 volts	0.1 A	1.2 W
-12.0 volts	0.1 A	1.2 W
-2.0 volts	2.8 A	5.6 W

Total Power		77.34 W

Cooling Requirements:

Per-slot Average	77 W maximum
Airflow	6L/sec @ 0.38 mm water pressure for 10°C temperature rise

Environmental Specifications:

Temperature	Storage = -40°C to +75°C Operating = 0°C to +45°C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

VXI Plug & Play

** Specifications subject to change without notice.

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