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Find the *Interface Technology SR5500* at our website: ***Click HERE***



SR5500

VXI Digital Pin Electronics Controller

- DC to 50 MHz Data Rates
- Stimulus / Response / Real-Time Compare / Record
- 32 Differential ECL Input, Output and Tristate Channels per Module
- 256K or 1M Vectors per Channel
- Algorithmic and RAM-Backed Pattern Generation
- Data Formatting with 100 ps Programmable Edge Placement
- NRZ, RZ, RONE, RTC, and RINH Data Formats
- 18 Timing Generators per Module
- 100 ps Edge Placement Resolution
- Ideally Suited for Both Unit and Component Testing

1 Meg

Vector Depth



WaveEdit Graphical Waveform Editor. (optional)

General

The SR5500 VXI Digital PIN Electronics Controller consists of a single SR5510 Timing / Control Module and up to 20 SR5540 Differential ECL I/O Modules. All units are housed in two VXI mainframes (not included).

The SR5540 contains 32 stimulus output pins, 32 tristate control output pins and 32 response input pins in a single VXI C-size card. Up to 20 I/O modules can be controlled by a single SR5510 Timing / Control Module. Intermodule communication occurs through a VXI register-based interface and VXI direct memory access.

All outputs and inputs are differential ECL compatible. Input pins are grouped together on one connector, stimulus outputs are grouped on another connector, and tristate control outputs are grouped on a separate connector. This configuration provides the most efficient method of interfacing to the test head.

Simple Test Program Development

The SR5500 includes fully compliant VXI Plug & Play software drivers that includes a stand-alone, executable soft panel program to interactively control the instrument. The soft panel provides complete control of the instrument without requiring a particular programming environment. A standard installation program allows for quick setup and ability to get up and running in minutes. This control software also includes standardized instrument drivers to control the instrument from within the user's own application program. National Instruments Lab Windows/CVI graphical programming language is supported to provide interactive screens for micro-management of virtually any digital test application.

Test program development is further aided in that the SR5500 uses an ASCII message-based command set based on the SCPI-syntax (Standard Commands for Programmable Instruments) test language. The use of SCPI-syntax simplifies test program development by providing an "English-like" programming environment that is widely accepted by the test and measurement industry.

In addition, test program development is further simplified by data entry commands such as Pin Assignments. Pin Assignments allow you to

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SR5500 Digital PIN Electronics Controller

group I/O pins by their logical function (address bus, data bus, etc.) and assign a field name to that pin group. Pin Assignments streamline programming by allowing you to enter patterns by referring to the UUT signal names.

To make test development even easier, an optional graphical waveform editor (WaveEdit) can be added as an add-on extension to the existing SR5500 WIN VXI Plug & Play Soft Panel. WaveEdit allows you to define stimulus and response tests patterns using waveform graphics in order to represent data in the same format that you use every day. Recorded data can also be viewed in context with stimulus data, permitting you to be more productive in developing and debugging test programs.

Fast Test Pattern Download From Slot-0

SR5500 test programs and stimulus / response test patterns may also be downloaded from the Slot-0 Controller using high-speed binary block transfers, therefore, providing the best of both worlds; ASCII based test language for simple test program development and binary block transfers for high-speed download of test programs.

To further maximize test download time, the SR5500 provides internal program storage capable of storing up to 32 different test programs. Any test program can be "activated" by selecting its test name with a simple command string.

RAM Backed and Algorithmic Pattern Generation

The SR5500 offers traditional RAM-backed pattern generation and compare, while also providing algorithmic pattern generation and compare capabilities. Test patterns that ordinarily consume large amounts of I/O memory, such as for RAM memory testing, can be reduced to just a few algorithmic commands. Algorithmic capability reduces the need for large pattern memory, increases test throughput by minimizing test download time, and reduces test programming and debug time.

Seven Distinct I/O Memory Types

Each SR5540 contains seven separate memory banks, each either 256K or 1 mega-vectors in depth. All memory banks operate at full 50 MHz data rates.

The stimulus memory contains the output, tristate, and algorithmic patterns, which are used to define the stimulus to the DUT / UUT. The tristate memory is normally used to control external pin drivers in bidirectional applications. For certain applications, the tristate memory may be used to provide additional non-algorithmic stimulus outputs. The response memory contains the expect, algorithmic, and mask patterns, which are used to define the expected response from the DUT / UUT. The mask memory provides a means to ignore individual response data bits on a vector by vector basis. Algorithmic memory is used to define the arithmetic operations needed to generate stimulus and response data with the algorithmic hardware.

Record memory can be used to store either the response data or the result of the comparison between the response data and the Expect memory. It is operated independently in a manner much like a logic analyzer. A 16-level state machine and nine system-wide comparators are used to control what data is saved in the memory. In addition to the record memory, each input channel is provided with a 16-bit CCITT CRC register for signature analysis applications.

18 Timing Generators per Module

Each I/O module contains 18 separate timing generators for stimulus and response edge placement. Each output pin can select from 4 timing generators to define the leading and trailing edges of each stimulus pin. Each group of eight output pins share an independent set of 4 timing generators for a total of 16 stimulus timing generators per card. Each response pin can select from 2 response timing generators to define the sample and compare edges, or the 2 response timing generators can be combined together for window compare with glitch detection.

Multiple Data Formats

Each stimulus pin may be independently programmed for any of the following formats: Non Return to Zero (NRZ), Return to Zero (RZ), Return to One (RONE), Return to Complement (RTC), and Return to Inhibit (RINH).

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