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Find the *Interface Technology SR5510A* at our website: *Click HERE*

SR5510

Timing/Control Module for SR5500



- Up to 50 MHz Data Rates
- Stimulus / Response / Real-Time Compare
- Powerful Dual-Processor Architecture
- Store Up to 32 Different Test Programs
- 256K or 1M Vector Depth
- Expandable to 640 Inputs and 640 Outputs
- RAM-Backed and Algorithmic Pattern Generation
- Multilevel Triggering and Advanced Logic Analysis
- Data Formatting with Programmable Edge Placement
- Message-Based Commands for Easy Test Program Development
- A32 / D32 Binary Transfer for High-Speed Test Program Download
- Conditional Pattern Looping and Branching for Real Time Test Sequence Control

Description

The SR5510 module has a dual processor architecture that is optimized for digital testing. The System Processor, the powerful 68030 running at 25 MHz, provides the VXI Bus message-based interface to the Slot-0 Controller. The Control Processor is the real-time digital test engine controlling the conditional test branching, looping, sequencing, logic analysis and control.

VXI Bus Interface

Based on the IT9010M industry standard VXI bus interface chip, the SR5510 meets the requirements of VXI Bus Specification Versions 1.3 and 1.4. The SR5510 VXI bus interface receives message-based commands from the Slot-0 Controller, then becomes the VXI Bus Master to pass test parameters and data to the SR5540 I/O module. The System Processor provides the command power for the SCPI-syntax word serial command structure.

Real Time Digital Testing

The 50 MHz Control Processor provides real time control of the test pattern sequence by controlling nested looping and conditional branching. This capability allows the SR5500 to generate stimulus patterns to the UUT, analyze the UUT response patterns, and determine the next test pattern based on test conditions such as expected response pass/fail, loop count, external input flags, response trigger qualifiers, etc.

Powerful Macro Commands Control Test Execution and Data Analysis

Stimulus pattern and response compare sequencing is controlled through a Test Program Macro Command language. The test program language contains over 100 macro command combinations to control the test sequence. All this digital testing capability is performed at full test speed and in real time, therefore, off-loading your Slot-0 Controller from extensive response data analysis.

High Performance Response Logic Analysis

The Record capability of the SR5500 is similar to that of an advanced logic analyzer. For simple logic analysis and recording, Trace Macro Commands allow you to quickly and easily program pre-trigger, center-trigger, and post-trigger conditions.

The Advanced Trace Macro Commands provide more sophisticated logic analysis functions. In this mode, the user may define instructions for a 16-level state machine operating at up to 50 MHz. At each state level, the user may define the conditions which cause the state machine to advance to the next state, return to a previous state, store UUT response data or UUT compare error data, and calculate CRS (signature analysis).

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*SR5510 SPECIFICATIONS**

CPU:

System Processor	Motorola 68EC030 @ 25 MHz
Control Processor	50 MHz Custom Gate Array

Internal Clock:

Range	2.2 ms to 20 ns, 400 Hz to 50 MHz
Resolution	≤ 0.005%
Data Output Jitter	10 MHz reference jitter + 100 ps (short term RMS)

External Clock:

Range	DC to 50 MHz
Pulse Width	10 ns, minimum
Active Edge	Rising or falling
Input Voltage	-5.0 to +10.0 volts
Input Threshold	-5.0 to + 4.99 volts in 20 mV steps
Input Impedance	1M ohm

External 10 MHz Ref Input:

Input Coupling	Capacitor coupled
Input Signal Waveform	Square to sine wave
Input Voltage Level	1-5 V p-p
Input Impedance	High impedance

External Trigger Input:

Active Level	High or low
Input Voltage	-5.0 to +10.0 V
Input Threshold	-5.0 to + 4.99 V, in 20 mV steps
Input Impedance	1M ohm

External Gate Input:

Active Edge	Rising or falling
Input Voltage	-5.0 to +10.0 V
Input Threshold	-5.0 to + 4.99 V, in 20 mV steps
Input Impedance	1M ohm

External Input Flags:

Receiver Type	74ACT244
Number	Eight
Active Level	High or low
Input Voltage	Vil = ≤ 0.8 V Vih = ≥ 2.0 V
Input Impedance	10k ohms

Clock Output:

Driver Type	74F244
Output Level	TTL
Duty Cycle	50%
Output Termination	50 ohm, series

VXI Specifications

Interface Compatibility:

Type	Message-based, bus master / servant
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Interrupt Level	Programmable 1-7
Triggers	TTLTRG 0-7
Memory	1 MB VME A32 / D32 / D16 / D8

Power Requirements:

+5.0 volts	5.5 A	27.5 W
-5.2 volts	0.8 A	4.16 W
+12 volts	0.2 A	2.4 W
-12 volts	0.2 A	2.4 W
-2.0 volts	0.2 A	0.4 W

Total Power		36.86 W (max.)

Cooling Requirements:

Per-slot Average	37 W (max.)
Airflow	3L / sec @ 0.20 mm water pressure for 10° C temperature rise

Environmental Specifications:

Temperature	Storage = -40° C to +75° C Operating = 0° C to +45° C
Humidity	5% to 95% relative, non-condensing

Weight:

Approx 3.0 lb

Software Drivers:

National Instruments	LabView
National Instruments	LabWindows/CVI

* Specifications subject to change without notice.

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