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SR5540A

Differential ECL I/O Module for SR5500 Digital Pin Electronics Controller

- 32 Input / Output Pins per Module and 32 Tristate Output Pins
- 256K or 1M Vectors per Channel
- RAM-Backed and Algorithmic Pattern Generation
- NRZ, RZ, RONE, RTC , and RI Output Data Formats Supported
- 16 Stimulus Timing Generators per Module
- Two Response Generators per Module
- 100 ps Edge Placement Resolution

High Channel Density

The SR5540A ECL I/O Module provides 32 stimulus pins, 32 tristate control output pins, and 32 response pins in a single C-size slot. Up to 20 I/O modules may be controlled by the SR5510A Timing/Control Module. Intermodule communication occurs through a VXI register-based interface and VXI direct memory access.

Seven I/O Memory Types

The SR5540A I/O Module contains seven separate memory banks, each either 256K or 1M vectors in depth, for generating stimulus patterns, expected response patterns, and recording DUT / UUT response data. All memory banks operate at full 50 MHz data rates.

The Stimulus Memories contain the Output, Tristate, and Algorithmic patterns, which are used to define the stimulus output to the DUT / UUT. The tristate memory is normally used to control external pin drivers in bidirectional applications. For certain applications, the tristate memory may be used to provide additional non-algorithmic stimulus outputs. The Response Memory contains the Expect, Algorithmic, and Mask patterns, which are used to define the expected response from the DUT / UUT. The Mask memory provides a means to ignore individual response data bits on a vector by vector basis. Algorithmic memory is used to define the arithmetic operations needed to generate stimulus and response data with the algorithmic hardware.

Record Memory can be used to store either the response data or the result of the comparison between the response data and the Expect memory. It is operated independently in a manner much like a logic analyzer. A sixteen level state machine and nine system-wide comparators are used to control what data is saved in the memory. In addition to the record memory, each input channel is provided with a 16-bit CCITT CRC register for signature analysis applications.

18 Timing Generators per Module

Each I/O module contains 18 separate timing generators for stimulus and response edge placement. Each output pin can select from 4 timing generators to define the leading and trailing edges of each stimulus pin. Each group of eight output pins share an independent set of 4 timing generators for a total of 16 stimulus timing generators per card. Each response pin can select from 2 response timing generators to define the sample and compare edges, or the 2 response timing generators can be combined together for window compare with glitch detection.

Multiple Data Formats

Each stimulus pin may be independently programmed for any of the following formats: Non-Return to Zero (NRZ), Return to Zero (RZ), Return to One (RONE), and Return to Complement (RC), and Return-to-Inhibit (RI).

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*SR5540A SPECIFICATIONS**

Channels per Module:

Inputs	32
Outputs	32

Memory Types:

Stimulus	Output, Tristate, Algorithmic
Response	Expect, Mask, Algorithmic
Record	Record

Memory Depth:

1, 048, 540 vectors

Output Timing:

Clock Pairs (assert/deny)	8 total per card; 2 per 8 channels
Delay Range	One clock period
Resolution	100 ps, nonmontonic 2.0 ns, monotonic
Delay Accuracy	2.0 ns typ., 3.0 ns maximum
Output Pulse Width	Min: 10 ns Max: period clock - 10 ns
Pulse Width Accuracy	3.0 ns typ., 5.0 ns maximum

Skew:

Same Module	±2 ns typical, ±4 ns maximum
SR5540-SR5540	±3 ns typical, ±5 ns maximum

Data Formats:

RZ	Return to Zero
NRZ	Non-Return to Zero
RONE	Return to One
RC	Return to Complement
RI	Return to Inhibit/Tristate

Output Drivers:

Type	Differential ECL, 100324
Voh (50 ohms to -2.0 V)	-1.025 V, min., -0.870 V, max.
Vol (50 ohms to -2.0 V)	-1.830 V, min., -1.620 V, max.
Output Termination	50 ohms to -2.0 volt

Input Receivers:

Type	Differential ECL, 100325
Vih (single-ended)	-1.165 V, min., -0.870 V, max.
Vil (single-ended)	-1.830 V, min., -1.475 V, max.
Vdiff (differential)	150 mV, min.
Input Termination	50 ohms to -2.0 V

Input Sample/Compare Formats:

Formats	Edge / Window
Range	One period clock cycle
Resolution	100 psec
Accuracy	±1 ns typical, ±2 ns maximum

Input Timing:

Sample/Compare Clocks	Two per card (edge mode); One per card (window mode)
Input Delay Range	One clock period
Clock Separation	10 ns, min.
Resolution	100 ps, nonmonotonic 2.0 ns, monotonic

VXI Specifications

Interface Compatibility:

Type	Register-based, servant only (controlled by SR5510A)
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Memory	2 MB VME A32/D32

Power Requirements:

+5.0 volts	9.5 A	47.50 W
-5.2 volts	4.2 A	21.84 W
+12.0 volts	0.1 A	1.2 W
-12.0 volts	0.1 A	1.2 W
-2.0 volts	2.8 A	5.6 W

Total Power		77.34 W

Cooling Requirements:

Per-slot Average	78 W maximum
Airflow	6 L/sec @ 0.38 mm water pressure for 10°C temperature rise

Environmental Specifications:

Temperature	Storage = -40°C to +75°C Operating = 0°C to +45°C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

National Instruments	LabView
National Instruments	LabWindows/CVI

* Specifications subject to change without notice.

Interface Technology, Inc. • 300 S. Lemon Creek Dr., • Walnut CA • 91789
Phone: (909)595-6030 • FAX: (909)595-7177 • e-mail: info@interfacetech.com • www.interfacetech.com

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