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INTERPHASE

iSPAN

iSPAN 1635 T1/E1/J1 Communications Controller

The Industry's Most Advanced CompactPCI PSB Controller for Telecommunications



2.16 CPSB Compliant

Signaling Gateways/Softswitches • Radio Network Controllers Node Bs • Base Station Controllers • Base Transceiver Stations LMDS Gateways

FEATURES

- Motorola MPC8260 (PowerQUICC II™) 200 MHz on-board processor
- ATM to IP interworking
- SS7 to IP interworking
- Narrowband to broadband interworking
- Optional Inverse Multiplexing for ATM (IMA)
- 64-bit, 33 MHz (upgradeable to 66 MHz) PCI bridge, supporting multiple transfer modes
- PICMG® 2.16 10/100 Ethernet CPSB Compliant
- Hostless functionality allows use without a host processor or a PCI bus on the backplane
- 16 MB of downloadable Flash EEPROM
- 8 MB of CPM connection memory
- Both front and rear access (via passive Rear Transition Module) options available
- 8 software selectable front or rear T1/E1/J1 interfaces
- Three 10/100 Ethernet interfaces with autonegotiation (two on the backplane and one on the front panel)
- Integrated CSU on T1 lines with support for Facility Data Link
- Full hot swap capability
- H.110 bus, 512 time slot local-to-H.110 bus,1024 local-to-local time slots
- Support for ATM AAL0, AAL2, and AAL5 Adaptation Layers
- Multiprotocol support for SS7, ATM, Frame Relay, X.25, ISDN, HDLC, and PPP
- On-board support for multiple types of voice and data traffic:
  - Frame Relay and voice traffic over TDM
  - Frame Relay conversion to IP over Ethernet
  - Packetized voice
  - SS7 (MTP1 and MTP2), ISDN

The new world packet technologies, IP and ATM, have drastically increased the speed of connectivity and flexibility of services at greatly reduced costs, and enabled a new generation of applications. In response, the PCI Industrial Computers Manufacturers Group (PICMG) has developed the new CompactPCI Packet Switching Backplane (CPSB) 2.16 standard to combine the benefits of CompactPCI® and Ethernet. Designed to *enhance* and *combine* the steadfast, robust capabilities of CompactPCI with the ubiquity of Ethernet, CPSB designs allow engineers to migrate current infrastructures to support these enhancements, rather than replacing previous R&D investments with an entirely new architecture. The CPSB standards provide for improved communication among boards in the system by transmitting data via a switched, high-speed, Ethernet star topology. Giving boards a "system-on-a-card" functionality and providing a "virtual backplane" to interconnect multiple chassis, 2.16 compliance indicates performance, scalability, flexibility, and reliability improvements along with shortened integration time. Interphase takes it further by also differing ATM to IP interworking capability.

The Interphase *i*SPAN 1635 T1/E1/J1 Communications Controller sets the standard for high-performance and reliability as the industry's most advanced PICMG 2.16-compliant CompactPCI T1/E1/J1 communications controller for telecommunication applications. The 1635 outshines its competition with the industry's best performance, a comprehensive array of protocol and operating system support, and robust development tools to simplify the integration process in either standard CompactPCI systems or new packet switched backplane architectures.

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Powerful Features for Next-Generation Telecommunications

1635 Architecture

The *i*SPAN 1635 CompactPCI T1/E1/J1 Communications Controller is the flagship product in the Interphase line of MPC8260-based communications controllers for carrier-class telecommunication environments. The software selectable interfaces for 8 T1/E1/J1 ports enable maximum flexibility to support multiple national variants with just one board.

The T1/E1/J1 framers feed DS0 traffic to an on-board H.110 TDM switch module, which then feeds multiple DS0s to the 8260 for internal processing or to the H.110 TDM bus for I/O to/from other slots. The T1/E1/J1 framers can also simultaneously feed any number of DS0s to the Inverse Multiplexer over ATM (IMA) chip on the 1635, which then aggregates the DS0s in full or fractional T1 streams into a single ATM pipe to be processed by the 8260's CPM.

With this powerful functionality, the 8260 Communications Processor Module (CPM) can simultaneously support multiple protocols including ATM, SS7, Frame Relay and others via the internal time slot assigner and the internal UTOPIA bus interface. The 8260 CPM has access to its own 32-bit local bus, where the 32 K entry look-up Content Addressable Memory (CAM) and 128 MB SDRAM are available for unimpeded read/write access to connection and routing tables.

The 8260 features a 64-bit, 66 MHz local data bus connecting 128 MB of SDRAM, 16 MB of boot code FLASH EEPROM, and a 64-bit wide PowerSpan® PCI bridge. The PowerSpan bridge operates at 33 MHz (upgradeable to 66 MHz) on the backplane, supporting several DMA transfer modes for enhanced interprocess communications.

The 1635 is also equipped with three fast Ethernet ports; two RMII interfaces on the backplane and one on the faceplate. The 10/100 Base-T ports support full duplex 100 Mbps traffic, and can be used for a variety of bridging/routing purposes, protocol interworking purposes, or simply to download/communicate with the 8260 CPU. Port selection is controlled by software and can be changed dynamically at any time. Mini-DIN TTY ports are also provided on the front panel.

Processor/Memory

- PowerQUICC II (MPC8260) 64-bit RISC processor allows full support of various communications protocols, reducing host CPU processing
  - Dual bus architecture: 64-bit 60x bus and 32-bit local CPM bus
    - 200 MHz core, 133 MHz CPM, 280 MIPS CPU
    - 128 MB 64-bit SDRAM memory
    - 16 MB downloadable 8-bit Flash EEPROM
  - 8 MB 32-bit Connection Memory
  - 280 MIPS
- 64-bit, 66 MHz local data bus
- Up to 700 Mbps CPM protocol engine



Line Interfaces

- No component changes between T1, E1 or J1 terminations
- Each RJ-48C line is software configurable in Line Termination or Network Termination mode
- Integrated Channel Service Unit (CSU) in T1 mode
- Rear Transition Module includes line protections to comply with ETS300 046-3, UL1459, FCC68 and Bellcore TR-NWT-001089
- QuadFALC™ framer supports long haul or short haul interface, AMI, HDB3, or B8ZS line coding and various Superframe Formats
- One Mini-DIN TTY console port on front panel

CPSB 2.16-Compliant Architecture Benefits

- Improved communication among boards in a system because they are interconnected by a switched, high-speed Ethernet backplane, which greatly improves system throughput.
- Combined benefits of all of the best attributes of three widely accepted standards: Ethernet, CompactPCI, and ATM in order to deliver an advanced solution requiring greatly reduced development time.
- A "system-on-a-card" hostless functionality resulting from slot interconnection via a network stack over Ethernet.
- Significantly improved development time since protocol integration takes place at the Transport/Network layer instead of the backplane/driver data-link layer.
- Adherence to the reliability, applicability, and serviceability attributes of the widely-accepted CompactPCI installed base. For example, a point of failure on one interface card can render the entire system inoperable in typical CompactPCI configurations with only one bus interface. Packet switching backplanes have dual fabric topologies, providing redundancy, to eliminate this threat of failure.
- Support for interconnection of multiple systems, creating one big "virtual backplane" among separate enclosures. This virtual backplane supports QoS/CoS, redundant connections to each board, modifiable bit rate assignments to each card (10/100/1000/2000 Mb), modifiable bandwidths to each enclosure (200 Mb to 40 Gb), flow control to the link layer, a standard pin interface to each card slot, and much more
- Migratation of current infrastructures to support the above-mentioned enhancements, rather than replacing previous R&D investments with an entirely new architecture. Thus, the life-cycle of installed components are extended and past infrastructure investments are preserved.

Inverse Multiplexing for ATM (IMA)

- Supports up to 8 T1, E1, or J1 lines into a single ATM pipe
- Allows a mix of IMA and non-multiplexed DS0 channels to co-exist on the same facilities (ex. IMA or fractional T1/E1/J1)
- Up to 4 IMA groups
- Provides cost-effective bandwidth aggregation

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Reduce Time-to-Market with Robust Software Development Tools

Interphase offers a robust suite of software development tools to help shorten the learning curve and design cycle for integration projects based on the 1635 communications controller. Because integrators and equipment providers have diverse development environments, Interphase provides two types of development tools, each tailored to the needs of different integration types. The Board Development Kit (BDK) facilitates development of device drivers, embedded protocol firmware and applications for the 1635 hardware module. The *i*WARE™ Software Development Suite offers developers a set of Interphase-developed firmware protocol stacks, accessible via APIs provided by Interphase.

Board Development Kit

The 1635 BDK is specific to the 1635 hardware, but it is not tied to a particular operating system environment.

The kit contains the following main components:

- **Board Development Guide** - provides valuable information and software implementation directives, as well as source examples
- **Setup Utility** - allows the user to modify the content of the various programmable elements of the board, and especially the FLASH EEPROM memory
- **Interactive Built-In Test Utility** - allows the management of the card such as reset/run action, memory and registers dump, memory and DMA tests, line parameters manipulation, and more

*i*WARE Software Development Suite

The 1635 *i*WARE Software Development Suite reduces software development time and facilitates faster time to market by supplying embedded protocol support for ATM and SS7, base drivers for a selected operating system, configuration and diagnostic utilities, and sample programs.

The 1635 is initially offered with an *i*WARE Software Development Suite for Solaris 2.6, 2.7 and 2.8. The *i*WARE Software Development Suites enable easy integration, and tools and diagnostics to enable faster time to market. The *i*WARE Software Development Suites also provide Interphase's own ATM, SS7 and Ethernet protocol support for SS7 MTP2, AAL0 and AAL5; with ATM Quality of Service classes of service for Constant Bit Rate (CBR), Unspecified Bit Rate (UBR) and Variable Bit Rate (VBR).

The *i*WARE Software Development Suite supplied with the 1635 module consists of software programs and utilities running on the host CPU, and embedded software ("firmware") which runs on the on-board 8260 networking processor.

Software elements are separated into four modules:

- The base drivers for each supported Operating System (executed by the host processor)
- The configuration and diagnostic utilities
- Sample programs
- The embedded firmware executed by the 8260 on the 1635 board

These modules interact with each other through well-defined and documented interfaces. A common *i*WARE WAN API (Wide-Area Network Application Programmer's Interface) is defined at the interface between the embedded firmware and the various drivers.

A complete documentation set is also provided describing Interphase's *i*WARE WAN API, the Base Driver's API, sample programs, and tool guides.

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Industry Standards Compliance

- PCI-SIG Peripheral Component Interconnect (PCI) Local Bus Specification, Rev 2.2
- CompactPCI 2.1
- CompactPCI PICMG 2.0 R3.0
- PCMIG 2.16

Physical Layer 1 and Protocol Standards Compliance

- ANSI T.403: Network and Customer Installations Interface - DS1 Electrical Interface
- ANSI T.107: Digital Hierarchy Format Specification
- AT&T TR 62411: Accunet T1.5 - Service description and Interface

Interface Specifications

- Telcordia SR-4994 Layer 1, National ISDN Primary Rate
- ITU-T G.703 General Aspects of Digital Transmission Systems
- ITU-T G.704 General Aspects of Digital Transmission Systems
- ANSI T1.403-1995
- ANSI T1.107-1995
- EIA 232-D Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange
- Bellcore TR-NWT-001089
- IEEE 802.3: Fast Ethernet
- ETS-300 046 Integrated Services Digital Network (ISDN); Primary rate access
- Japanese references: ITU-JT G.703, ITU-JT G.704, ITU-JT G.706

Agency Certifications

Safety + EMC:

- UL 1950
- UL 1459
- CSA/CAN C22.2 No. 950-95
- EN 60950
- IEC 60950 2nd Edition, 1991+Amd.1, 1992 + Amd.2, 1993 + Amd.3, 1995 + Amd.4, 1996

Emissions/Immunities:

- FCC, Part 15, Class A
- ICES-003, Class A (Canada EMC)
- EN 55022; CISPR 22, Class A (Europe EMC)
- EN 55024; CISPR 24 (Europe Immunity)
- VCCI, Class A

Markings:

- CE Mark

Interface:

- FCC Part 68
- CS-03, Issue 8, Part II (Canada)

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SPECIFICATIONS

Specifications

Bus Type ..... CompactPCI, H.110
Bus Access 32-bit, 33MHz
..... can be configured for 64-bit, 66MHz
Processor ..... 200MHz Motorola MPC8260
Memory ..... 128MB SDRAM

Mechanical

Form Factor..... 6U CompactPCI
Length..... 266.7 mm (10.5 in.)
Width ..... 215.9 mm (8.5 in.)
RTM Length ..... 266.7 mm (10.5 in)
RTM Width ..... 134.5 mm (5.3 in)

Operating Environment

Temperature ..... 0 to 55º C
Relative Humidity ..... 5% to 95% noncondensing
Altitude ..... 0 to 15,000 ft
Power Consumption 5V: 1.7A; 3.3V: 2.0A

Software Support

Board Development Kit (BDK)
*i*WARE Software Development Suite for Soliaris (refer to *i*WARE datasheet)

CONFIGURATION OPTIONS

The *i*SPAN 1635 CompactPCI T1/E1/J1 Communications Controller is available in the configurations listed below. Rear-access configurations include the Rear Transition Module.

1635-000: Front Access with ATM/IMA

1635-001: Rear Access with ATM/IMA

1635-002: Front Access with no ATM/IMA

1635-003: Rear Access with no ATM/IMA

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