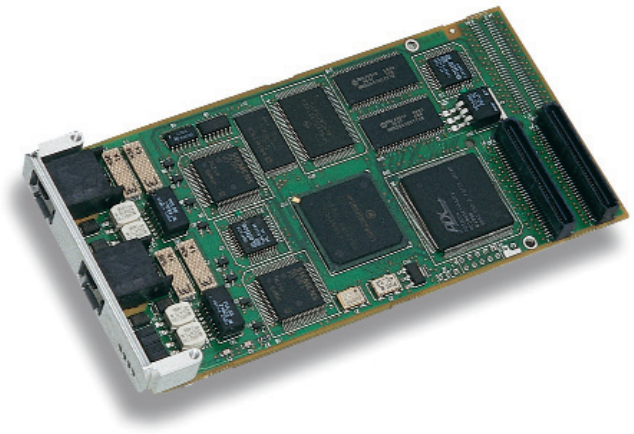
INTERPHASE

iSPAN

# iSPAN™ 4535 Multiprotocol WAN Communications Controller

## High Performance Mezzanine Card for Channelized T1/E1 Communications



**Wireless BSCs • Telecommunications Servers • Softswitches • Wireless Intelligent Networks • AIN SCPs and IPs • Computer Telephony • Interworking Units • Internet Access Servers • HLRs**

### FEATURES

Motorola's MPC860MH or MPC860SAR on-board processor featuring:
- 66 MHz RISC CPU
- 32-bit, 33 MHz local data bus
- Up to 100 Mbps CPM protocol engine

Two simultaneous software selectable T1/E1 line interfaces serve multiple national variants with one board

Integrated CSU on T1 lines eliminates the need and cost for additional communications equipment

Protocol support for SS7 (MTP 1 and MTP 2), ATM (AALO and AAL5), Frame Relay, X.25, HDLC, PPP, ISDN, and more

16 MB of shared Synchronous DRAM Memory assists on-board protocol processing to maximize system performance

Up to 1 MB Flash EEPROM

Both front and rear access options available
- Rear access via PMC P4 connection
- 6U CompactPCI Rear Transition Module

Optional Content Addressable Memory (CAM) for enhanced VC handling capacity

Configurable local TDM bus for add/drop and pass-through of individual DS0 channels

LynxOS® HA, Solaris™, and VxWorks® operating system support

Board Development Kit (BDK) and Software Developement Suites available for custom protocols, applications development, or driver development

SNMP Management MIBs

The *i*SPAN 4535 PMC Multiprotocol WAN Communications Controller from Interphase is the perfect complement for high availability CompactPCI®, VME or other customized telecom and WAN gateway systems. Its unique features are designed specifically for telecom applications that require flexible protocol support and multiple T1/E1 interfaces.

With an intelligent, high-performance architecture based on the MPC860 PowerQUICC™ processor, support for multiple frame-based protocols, such as ATM and SS7, front or rear I/O access, and an integrated CSU, the 4535 delivers the power and functionality needed for next-generation telecommunication applications. Also, robust software development tools help system designers and integrators meet the time-to-market requirements of today's competitive telecommunications demands.

# 4535 Hardware

## Dual Channel T1 and E1 Communications

The *i*SPAN 4535 Multiprotocol WAN Communications Controller from Interphase provides two fully channelized T1/E1 communication links. Each link can be independently programmed by the user for E1 or T1 operation and has an integrated short and long-haul line interface. In "direct mode", each framer is connected to a separate independent 2 Mbps TDM bus. In "switched mode", the two framers are tied to the same local 4 Mbps TDM bus. Each framer controls its own interrupt line to the local processor.

The 4535 controller supports a comprehensive suite of WAN protocols, providing a versatile "single architecture" platform for multiple telecommunications and data communications applications. Utilizing the Motorola MPC860 PowerQUICC microprocessor, the 4535 comes in several powerful configurations:

*Frame-based version:* Targeted for general purpose environments running Frame Relay or other frame-based protocols such as X.25, PPP, or HDLC over T1/E1 connections, this configuration utilizes the MPC860SAR version of the PowerQUICC. The use of the 860SAR CPU allows this version of the product to offer a seamless migration to ATM services when available or desired with a simple, user-installable software protocol upgrade.

*SS7 version:* Optimized for SS7 (Signaling System 7) applications, this configuration utilizes the MPC860MH version of the PowerQUICC and optionally includes Interphase's SS7 protocol software which provides the industry's highest channel density. The 4535 is also compatible with most third party Layer 3 SS7 protocol stacks.

*ATM version:* Intended for heavy usage ATM environments, this configuration includes an additional CAM (Content Addressable Memory) to support over 4000 ATM virtual connections.

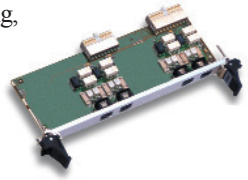
## Processor/Memory


- PowerQUICC (MPC860MH and MPC860SAR) 66 MHz, 32-bit RISC processor allows full support of various communication protocols – reducing host CPU processing
  - MPC860 CPM controls either a 32 channel or 64 channel TDM bus
  - 1 MB downloadable Flash EEPROM for boot memory
- 16 MB SDRAM memory
- 4 K CAM for ATM VC/VP sort, offering up to 4096 simultaneous virtual/circuit connections

For more demanding applications, refer to documentation for the Interphase *i*SPAN 4539 PMC T1/E1/J1 Communications Controller.

## Line Interfaces

- Two individually software selectable T1/E1 interfaces allow no component changes between T1 and E1 network terminations
- T1/E1 access is offered for both front access and rear-access termination via PMC P4 connector
- Optional passive CompactPCI® Rear Transition Module (RTM) for rear-access telco systems
- Two software configurable T1 or E1 ISDN PRI lines
- Each RJ-45 is configurable in LT or NT mode for flexibility of network or line clock synchronization
- QuadFALC™ framer supports framing, signaling and line control
- One asynchronous RS232 TTY port on the development board



## PMC Interfaces

The 4535 is connected to the host through a PCI V2.2 compliant 32-bit 33 MHz bus master interface. The interface features a 40 Mhz local bus with two DMA engines, enables PCI burst transfers up to 132 Mbps and has an enhanced direct-connect interface to the MPC860 to ensure superior performance.

- PMC connector 1 and 2 are used for 32-bit PCI signals
- PMC connector 4 is used for:
  - Access to asynchronous TTY port
  - T1/E1 line signals for rear-access
  - Synchronous TDM bus interface for expansion
  - An 8-bit UTOPIA bus allowing connection to an external ATM PHY device

## Telecom Clock Management

The line interface can be configured in LT (clock slave) or NT (clock master) modes.

- LT mode offers synchronization on the T1 lines
- NT mode offers synchronization on a reference clock

## Built-in TDM Telephony Bus Connectivity

All 4535 configurations come equipped with a built-in TDM (Time Division Multiplexer), allowing sharing of the DS0s load on multiple T1/E1 lines across multiple system slots and/or multiple resource modules. This provides an extremely high degree of flexibility in the allocation of line interfaces and resource modules within the same CompactPCI system.

## Integrated CSU

The 4535 also includes an integrated channel service unit that can be activated on each T1 line and saves the user the need for an external CSU device. The CSU fully supports Facility Data Link functionality for remote management and statistics collection.

## Reduce Time-to-Market with Robust Software Development Tools

Interphase offers a robust suite of software development tools to help shorten the learning curve and design cycle for integration projects based on the 4535 Communications Controller. Because integrators and equipment providers have diverse development environments, Interphase provides several development tools, each tailored to the needs of different integration environments. The Board Development Kit (BDK) facilitates development of device drivers, embedded protocol firmware and applications for the 4535 hardware module. *i*WARE™ Software Development Suites offer developers a set of Interphase-developed protocol firmware stacks, accessible via the Interphase OpenWAN Application Programming Interface (API).

### Board Development Kit

The 4535 BDK is specific to the 4535 hardware, but it is not tied to a particular operating system environment.

The kit contains the following main components:

- *Board Development Guide* - provides valuable information and software implementation directives, as well as source examples
- *Setup Utility* - allows the user to modify the content of the various programmable elements of the board, and especially the FLASH EEPROM memory
- *Interactive Utility* - allows management of the card such as reset/run action, memory and registers dump, memory and DMA tests, line parameters manipulation, and more.

### *i*WARE Software Development Suites

The 4535 is offered with the following *i*WARE Software Development Suites which are compatible with all available configurations:

*Solaris Software Development Suite* – Supports Solaris 2.6, 2.7, and 2.8. Provides protocol support for ATM (AAL0 and AAL5), SS7 (MTP1, MTP2), ISDN, Frame Relay, X.25, PPP, and HDLC. Includes User and Kernel API, SNMP sub-agent.

*VxWorks Software Development Suite* – Supports VxWorks 5.4 and Tornado 2. Provides protocol support for ATM (AAL0 and AAL5), SS7 (MTP1, MTP2), ISDN, Frame Relay, X.25, PPP, HDLC, and SNMP. Also includes User and Kernel API.

*LynxOS HA Software Development Suite* – Supports LynxOS v 3.0.1. Provides protocol support for ATM (AAL0 and AAL5), Frame Relay, X.25, PPP, and HDLC. High availability software support and User API.

The 4535 *i*WARE Software Development Suite reduces software development time and facilitates faster time to market by supplying embedded protocol support for ATM, SS7, Frame Relay, X.25, HDLC, PPP, and more; base drivers for a selected operating system; configuration and diagnostic utilities; and sample programs.

The *i*WARE Software Development Suites enable easy integration, and tools and diagnostics foster easier development. The *i*WARE Software Development Suites also provide Interphase's own protocol API for ATM, SS7, Frame Relay, X.25, HDLC, PPP, and more for on-board protocol processing.

The *i*WARE Software Development Suite supplied with the 4535 module consists of software programs and utilities running on the host CPU, and embedded software ("firmware") which runs on the on-board 860 networking processor.

Software elements are separated into four modules:

- The base drivers for each supported Operating System (executed by the host processor)
- The configuration and diagnostic utilities
- Sample programs
- The embedded firmware executed by the MPC860 on the 4535 controller

These modules interact with each other through well-defined and documented interfaces. A common *i*WARE WAN API is defined at the interface between the embedded firmware and the various drivers.

A complete documentation set is also provided describing the Interphase *i*WARE WAN API (Wide Area Network Application Programmer's Interface), the Base Driver's API, sample programs, and tool guides.

# *i*SPAN 4535 PMC Multiprotocol WAN Communications Controllers

## Industry Standards Compliance

Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.2

Common Mezzanine Card (CMC) IEEE P1386/Draft 2.1

PCI Mezzanine Card (PMC) IEEE P1386.1/Draft 2.0

## Telecom Standards Compliance

**ANSI T1.102-1993:** Digital Hierarchy - Electrical Interfaces.

**ANSI T1.107-1995:** Digital Hierarchy - Formats Specifications.

**ANSI T1.403-1995:** Network-to-customer Installation - DS1 Metallic interface

**ANSI T1.646-1995:** Broadband ISDN - Physical Layer Specification for User-Network Interfaces Including DS1/ATM

**ATM Forum:** ATM User-Network Interface Specification, V3.1, October, 1995

**AT&T TR54016:** Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Superframe Format, Sept 89

**AT&T TR62411:** ACCUNET® T1.5 Service Description and Interface Specification, Dec 90

**ETSI TBR 012 Ed1 (1993-12):** Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2048 kbit/s digital unstructured leased line (D2048U); Attachment requirements for terminal equipment interface

**ETSI TBR 013 (1996-01):** Business TeleCommunications (BTC); 2048 kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface

**ETSI ETS 300 011:** Integrated Services Digital Network (ISDN); Primary rate user-network interface Layer 1 specification and test principles

**ETSI ETS 300 166:** Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s - based plesiochronous or synchronous digital hierarchies

**ETSI ETS 300 233**: Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate

**ITU-T G.703:** Physical/Electrical Characteristics of Hierarchical Digital Interfaces, 1991 (includes 2.048 Mbps E1 and 1.56 Mbps T1 definitions)

**ITU-T G.704:** Terminal Equipments Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44736 kbit/s "Hierarchical Levels", July, 1995

**ITU-T I.431:** Primary rate user-network interface - Layer 1 specification, 1993

**ITU-T I.432:** B-ISDN User-Network Interface - Physical Layer Specification, 1993

**ITU-T G.804:** ATM Cell Mapping into Plesiochronous Digital Hierarchy (PDH), 1993.

**Other ITU-T references:** G.705, G.706, G.732, G.736, G.737, G.738, G.739, G775, G.823, O.151

## Agency Certifications

Emissions/Immunities

- FCC Part 15 Class A
- IECS-003; Class A
- EN 55022; CISPR 22, Class A
- EN 55024; CISPR 24

Markings

- CE Mark

Safety

- UL 1950
- CSA/CAN C22.2 No. 950-95
- EN 60950
- IEC 60950

Interface

- FCC Part 68
- CS-03

AUTHORIZED INTERPHASE REPRESENTATIVE

## SPECIFICATIONS

**Specifications**

Bus Type..... PMC-PCI 2.2 Compliant
Data Transfer.....Master Target Bus
Bus Access..... 32-bit
Processor..... 66 MHz Motorola MPC860
Memory.....16 MB 10 ns SDRAM

**Mechanical**

Form Factor .....Single width PMC, conforms to IEEE P.136.1
Length.....149 mm (5.9 in)
Width.....74 mm (2.9 in)

**Operating Environment**

Power Consumption..... 5 V: 1.1 A, 3.3 V: none
Power Dissipation..... 5 W Front, 0.5 W Rear
Temperature.....0 to 55° C
Relative Humidity..... 5% to 95%
Altitude.....0 to 15,000 ft.

**Resident Software Options**

- Support for ATM, SS7, Frame Relay, X.25, HDLC, and PPP protocols
- SNMP Management MIBs
- SynWatch Diagnostic Software
- Installation/configuration utilities

**Software Support**

Board Development Kit (BDK)
*i*WARE Software Development Suite for VxWorks (refer to the *i*WARE Datasheet)
*i*WARE Software Development Suite for Solaris (refer to the *i*WARE Datasheet)

## CONFIGURATION OPTIONS

The *i*SPAN 4535 PMC Multiprotocol WAN Communications Controller is available in the following configurations:

**4535-000:** 2 T1/E1 ports, 66 MHz MPC860 with SAR, includes BDK

**4535-001:** 2 T1/E1 ports, 66 MHz MPC860 with SAR and content addressable memory, includes BDK

**4535-014:** 2 T1/E1 ports, 66 MHz MPC860 with SAR, includes BDK, rear access

**4535-020:** 2 T1/E1 ports, 66 MHz MPC860 with SAR and content addressable memory, includes BDK, rear access

**4535-022:** 2 T1/E1 ports, 66 MHz MPC860 with SAR, includes BDK, and JTAG debug port

**453X-RTM:** 4 T1/E1 ports, 6U CompactPCI passive Rear Transition Module (RTM)

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