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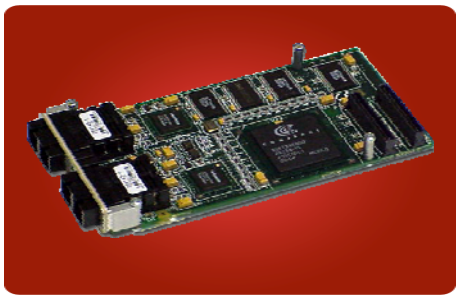
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INTERPHASE



*i*SPAN® 4576 PMC ATM OC-3/STM-1 Interface Card

Price/Performance-Maximized Wide Area ATM Connectivity

FEATURES

Single ATM connection or redundant two connections

32-bit, 33MHz PMC compliant adapter

Multimode/Single mode fiber

Automatic Protection Switching (APS) to ensure system availability

Mindspeed TM RS8234 155 Mbps ATM SAR

Mindspeed CX28250 PHY

Support for ATM AAL5 and AAL0 Adaptation Layers

Consistent Bit Rate (CBR), Variable Bit Rate (VBR), and Unspecified Bit Rate (UBR), services implemented in the hardware

Up to 32K Virtual Connections (VC) supports

OAM status notification supported

iSAR API command diagnostic utility

Classical IP (CLIP) Support

Software Support
- VxWorks
- Solaris
- Linux

APPLICATIONS

ATM Access Card
Video Conferencing
ATM Signaling Monitors
Test Equipment
Routers/Bridges
Signaling Gateways

High Performance
Designed especially for high-availability, high-bandwidth access applications, the ***i***SPAN 4576 provides ATM connectivity at 155 Mbps.

Reliable ATM Connectivity
Today's Networks require scalable, high-performance platforms with the flexibility to allow network capacity to keep pace with customer's demands. The ***i***SPAN 4576 controller meets the needs of the a variety of applications, including IP Switching and Routing, Internet connections and other applications that require the Quality of Service (QoS) guarantees provided by ATM.

Cost Effective
The low price and high performance qualities of the ***i***SPAN 4576 make it the best 155Mbps value in the industry.

12/18/09

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*i*SPAN 4576 OC-3/STM-1 Interface Card

Software

The 4576 is available with a Board Development Kit (BDK) for board & software development in Solaris™, VxWorks®, and Linux® environments. Included in this kit is the *i*SAR Application Programming Interface (API) to provide a seamless, consistent interface between the 4576 and supported operating systems. The Interphase-developed API and software layers enable application development without the need to be involved in low layer ATM driver development. The Automatic Protection Switching (APS) feature is hardware and software supported, enabling maximum uptime, reliability and network resiliency with software notification and PHYmodification support.

*i*SAR API

The *i*SAR API, included in the development kit, is an AAL layer API providing an efficient mechanism to enable configuration and control parameters for the driver, each adapter, and their respective Virtual Circuits (VCs). The API simplifies the development process by isolating the application from the complexities of the hardware while providing robust control of the hardware and data link.

Mindspeed RS8234 155 Mbps ATM SAR

Conforms to the ATM Forum recommendations

- 32-bit 33 MHz PCI 2.1 compliant with universal signaling
- UTOPIA 1 interface, with two PHY chip selects for APS capability
- 32-bit local bus interface
- Up to 32 K of total Virtual Channels bidirectional or 64 K uni-directional
- Hardware support of CBR, VBR and UBR services
- OAM functions support
- Up to 8 MB of control memory support

Mindspeed CX28250 PHY

- Meets ATM Forum standards
- 155 Mbps full duplex operations
- 16-bit UTOPIA2 interface (Interphase software kit allows user to select interface during 16-bit or 8-bit installation)
- 8-bit local bus interface (Interphase software kit allows user to select interface during 16-bit or 8-bit installation)
- Different levels of loopback control

PCI Bus

PCI bus master features:

- 32-bit, zero wait transfers for up to 132 Mbps burst DMA rate
- 512-word receive FIFO and 16-word transmit FIFO buffering

PCI bus slave features:

- Address decoded with medium speed device
- Memory and configuration read & write cycles supported

Memory

- Up to 8 MB SRAM control memory for up to 64 K VCs
- 1 KB of serial EEPROM

Automatic Protection Switching

The RS8234 SAR has a UTOPIA 1 bus, with two PHY chip selects. In conjunction with the CX28250 PHYs, the second PHY chip select allows the second PHY to share the same UTOPIA bus for APS capability. Both PHYs transmit and receive all data. Both PHYs receive data from the redundant network, but only the primary PHY transfers data back to the ATM SAR. APS operating parameters and event notification are available through the API, including the selection of active and/or protective PHY.

Clocks

The 4576 uses three clock sources: the PCI clock, the system clock and ATM front end clock.

Technical Specifications

Architecture	
Bus Type	PMC (PCI 2.1 Compliant)
Bus Data Transfer	32-bit, 33 MHz
Memory	4 or 8 MB control memory
Mechanical	
Length	5.87 in. / 149 mm
Width	2.91 in. / 74 mm
Operating Environment	
Temperature	0 to 55 °C (32 to 131 °F)
Relative Humidity	10% to 95% non-condensing
Altitude	0 to 15,000 ft
Power Consumption	

	3.3V	5.0V	Total
Single PHY	0.30 A	0.6 A	4.5W
Dual	0.35	1.07	7.0W

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About Interphase Corporation

Interphase Corporation (NASDAQ: INPH) delivers solutions for network connectivity, interworking, and packet processing for key applications for the communications, Mil/Aero, and enterprise markets. Founded in 1974, Interphase provides expert customization services and contract manufacturing, in addition to its COTS portfolio, and plays a leadership role in next generation AdvancedTCA® (ATCA), AdvancedMC™ (AMC), PCI-X, and PCIe standards and solutions. Interphase is headquartered in Plano, Texas, with sales offices across the globe.

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