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INTERPHASE
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*i*SPAN® 4539 PMC T1/E1/J1 Communications Controller

Multi-Protocol Communications Controller for CompactPCI and AdvancedTCA® Platforms

APPLICATIONS

Signaling Gateways (SG)

Media Gateways (MG)

Serving GPRS Support Nodes (SGSN)

Gateway GPRS Support Node (GGSN)

Home Subscriber Server (HSS) and Home Location Register (HLR)

Softswitches and Media

Gateway Controllers (MGC)

Short Message Service Controller

Application Servers

IP Service Control Points (SCPs)

The transformation from circuit to packet switched network is enabling service providers to provide advanced voice, video and data services seamlessly. Open systems architectures and standards are transforming the telecommunications marketplace, enabling delivery of cost-effective and rapid time-to-market solutions.

Interphase's broad portfolio of CompactPCI, PMC, PCI, AdvancedTCA® and AdvancedMC™ products are enabling our customers deliver high-performance and highly scalable network infrastructure solutions to the marketplace.

4539 Hardware

The *i*SPAN 4539 carrier-grade communications controller processor has at its core the Freescale MPC8264 PowerQUICC II™.

Key features of the board include:

- Processor/Memory Features
  - o 300 MHz core, 200 MHz CPM, 570MIPS CPU
  - o 64 bit data bus connecting the CPU to 64MB of SDRAM (upgradeable to 128MB)
  - o 64MB SDRAM memory
  - o 4MB of boot code 8-bit FLASH memory for boot and Power on Self Test
  - o 32 bit local CPM bus for software configurable-route establishment
  - o 2 Kb serial EEPROM
- Line Interfaces
  - o Four individual software selectable T1/E1/J1 interfaces
  - o Each RJ-48C software is configurable in line or network termination mode
  - o QuadFALC™ framer support long haul or short haul interfaces, AMI, HDB3 or B8ZS line coding or network termination mode
  - o Available with JTAG and TTY debug interfaces
- PCI Interface
  - o 32 bit 33MHz PCI 2.2 bus interface using Tundra PowerSpan™ PCI bridge on connectors P1 and P2 of the PMC
  - o PCI 2.2 master/target bus interface with I^2O line unit and 4 linked list DMA
  - o 32 bit DMA exchanges for high-transfer rates and performance
- Telecom Clock Management
  - o The line interface can be configured for Line termination – clock slave or Network Termination – clock master mode
  - o Recovered clock available via option P3 and P4 PCI interfaces
  - o Three line synchronization sources are supported
    - Free running internal clock
    - Recovered clock – loop timing
    - Network reference – through the optional P3 or P4 PCI interface

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4539 Software

Interphase offers a robust suite of software development tools to shorten the design cycle for systems integration.

The *i*Ware Software Development Suite (SDS) for the 4539 provides a broad suite of embedded layer 1 and layer 2 protocol software packages for use with a variety of telecommunications and networking applications. The SDS provides driver interfaces for many of the standard processors and operating systems and comes with an easy to use API for higher level application integration. The SDS software has also been integrated and tested with industry- standard 3rd party higher level software packages to ease system integration. The SDS package API also provides an easy-to-use configuration, diagnostic utilities and sample programs for stand-alone usage.

Processor and operating system combinations supported include:

- Intel®/Linux - RedHat, Montevista and SuSE Linux
- SPARC/Solaris - With Solaris 10 support
- AMD/Solaris - With Solaris 10 support
- PowerPC/Linux

Protocol support includes:

- Narrowband and Broadband SS7
  - o MTP1/MTP2 - Low Speed and High Speed Link
  - o Q/SAAL/Q.2140 - ATM High Speed Link
- Frame Relay
- LAPD
- HDLC

The tools suite includes the Board Development Kit (BDK) for the development of customer device drivers, embedded protocol firmware and applications for the 4539 hardware module. The *i*Ware® Software Development Suite (SDS) offers developers a set of Interphase-developed implementation of standards-based layer 1 and layer 2 protocol stacks accessible through API's using host drivers for most common processors and operating systems.

Tech Specs

Architecture

Bus Type	PMC (PCI 2.2 Compliant)
Bus Data Transfer	32-bit, 33 MHz
Open Boot Interface	IEEE 1275
Memory	64 MB SDRAM

Mechanical

Length	149 mm (5.86 in.)
Width	74 mm (2.9 in.)
Indicators	Board operational, link active

Operating Environment

Power Dissipation	3.3 V: 8.1 W maximum
Temperature	0 to 55 ˚C (32 to 131 ˚F)
Storage Range	–40 to 80 ˚C (–40 to 176 ˚F)
Relative Humidity	5% to 95% non-condensing
Altitude	0 to 15,000 ft

Environmental Power

- 3.3 V: 8.1 W maximum
- 5 V: less than 50 mW

Compliance

- FCC part 15 class A
- CE class A
- EN 55022
- EN 60950
- FCC part 68
- CS03

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About Interphase Corporation

Interphase Corporation (NASDAQ: INPH) is a leading provider of robust building blocks, highly integrated subsystems and innovative gateway appliances for the converged communications network. Building on a 30-year history of providing advanced I/O solutions for telecom and enterprise application, and addressing the need for high speed connectivity, Interphase has established a key leadership role in delivering next generation AdvancedTCA® and AdvancedMC™ solutions to the marketplace.

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