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V/SCSI-2 4220 Cougar II and 4220W Cougar Wide User's Guide

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Chapter 1
Introduction

Intended Audience

Interphase wrote this manual for its customers. It is intended for a highly technical audience, specifically, users who need to write their own software drivers.

Readers are assumed to have extensive knowledge of the following:

- The C programming language, including experience writing and installing interface software (drivers).
- The operating system of the host computer.
- SCSI specifications.
- VME specifications.

Scope Of Manual

The manual organization allows the user to focus on specific areas of interest, without giving more information than needed.

Specifically, this manual contains guidelines on:

- Installing the V/SCSI-2 4220 Cougar II.
- Programming the V/SCSI-2 4220 Cougar II, including Wide SCSI-2 operation.
- Determining the cause of any error messages generated by the board.

General Manual Information

You will find it very useful to read this *Introduction* completely. It contains information that will clarify many of your questions later. The *Conventions* section can be especially useful for later reference since it defines the presentation of certain topics.

Chapter 2, *Installation*, covers the procedure for installing the board. Chapter 3, *System Interface*, describes how to issue commands to the board, Chapter 4 discusses *VMEbus Interrupts*, Chapter 5, *Command Set: IOPBs and Commands*, documents the available commands, and Chapter 6 contains *Application Notes*. *Appendix A* covers Specifications, *Appendix B* discusses Connector Pinouts and Cabling, *Appendix C* covers the Error Codes, *Appendix D* defines the acronyms used in the manual, and *Appendix E* contains *Primary Base Addresses*.

Interphase can supply an example driver. If your system only requires minor modifications of this driver, then the source code provided gives a good base from which to start. If your system is radically different, then the example driver at least gives you ideas on what must functionally be contained in a driver.

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References

- ANSI x3T9.2/86-109 Revision 10g
- ANSI x3.131-1986 SCSI Specification
- ANSI x3.131-199x SCSI-II Specification, Draft Revision 10C
- VMEbus Specification, Revision C.1
- VMEbus Revision D, Draft 3.02, October 8, 1990

Conventions

This section details many of the writing conventions used throughout the manual. In addition, it gives many of the technical conventions.

- The SCSI channel provided by the motherboard is referred to as **Channel 0** or the **primary SCSI bus**. The channel provided by a SCSI daughter card (if installed) is called **Channel 1** or the **secondary SCSI bus**.
- The 4220 Fast and Wide Cougar II will be referred to as the **Wide** board or the **Cougar II Wide**. Differentiation of the Cougar II Wide will be made where appropriate. While the Cougar II Wide will function as a Cougar II, the Wide options are **only** available with a wide motherboard and/or a wide daughter card.
- **Byte** represents 8 bits; **word** represents 16 bits (2 bytes); and **longword** represents 32 bits (2 words, 4 bytes).
- Binary (single bit) data is represented as either *1* or *0*.
- To represent hexadecimal numbers, the manual adopts the C language notation. Decimal numbers are shown as decimal digits. For example:

  0x29 = 29 hex
  41 = 41 decimal

- Used in the context of a single bit of data, the term *set* means that the bit is a one ("1").
- Similarly, the term *cleared* means that the bit is a zero ("0").
- In many cases, bits, bytes, and words are marked *RESERVED*. If the value of the reserved bit, byte, or word is sent to the controller by the host, the value must be cleared to 0.
- If the reserved value is returned by the controller, it is reserved for future use by Interphase. The user should not rely on these values to be consistent through different revisions of the product.

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Overview

The V/SCSI-2 4220 Cougar II is available as a Fast or Fast and Wide SCSI-2 controller. The Cougar II is capable of controlling any combination of up to 14 SCSI-2 devices, seven on the primary SCSI channel and seven more if the optional secondary SCSI channel is installed. The Cougar II Wide is capable of controlling any combination of up to 15 Fast or Fast and Wide devices per channel.

If you have the Cougar II Wide product, the extensions to the MACSI SCSI interface necessary to support fast and wide SCSI operations are defined throughout this manual (identified with a W in the left margin). These extensions are defined to be fully upward compatible with existing drivers, therefore no changes are required to maintain the current level of functionality.

System Interface

The host processor communicates with the Cougar through 256, 512, 1K, or 2K bytes of onboard RAM. All commands and responses pass through this memory space which is referred to as *Short I/O* because it is mapped into the Short I/O space of the VMEbus.

Each command to the Cougar is specified using a host-generated software structure called an Input/ Output Parameter Block (IOPB). IOPBs can be built in either the Cougar's Short I/O space or offboard in system memory. In the latter case, command completions may optionally be posted to both onboard and offboard data structures.

The system-level interface, referred to as *MACSI* (Multiple Active Command Software Interface), is implemented in Short I/O. In addition to supporting command queuing, MACSI enables multiple commands to be active simultaneously. The Cougar accepts commands from the host and queues them internally. It then acts on each command as soon as possible within the confines of the SCSI bus. As commands are completed, the board notifies the host of each command's completion as well as the completion status.

Issuing Commands

The host submits commands to the Cougar by making an entry into a circular queue called the Command Queue. Each Command Queue entry is a 12-byte block containing a pointer to the IOPB and other control information.

The host may build IOPBs either onboard (in the Cougar's Host Usable Space in Short I/O) or offboard in system memory. Once it builds an IOPB, the host creates an entry for the IOPB in the next available slot in the Command Queue.

Work Queues

The concept of work queues is integral to the way that MACSI allows multiple commands to be active simultaneously. Information in the Command Queue entry determines the work queue into which a particular command is placed. At any time, there is an *In Progress* command for each work queue that has at least one entry. The *Next* command waits for the *In Progress* command from that work queue to complete.

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The Cougar II accommodates up to 14 work queues and the Cougar II Wide up to 255 work queues. This is not counting a special queue called *Work Queue 0*. Work queue 0 is intended for issuing special commands such as initialize controller or error recovery, etc. Cougar II Wide supports up to 255 work queues, numbered 0 through 255. Work queues are intended to be dedicated to a specific SCSI-2 device. Multiple work queues may be dedicated to the same device. The host sets the parameters of each work queue when it initializes the queue.

Since the SCSI bus allows many tasks to overlap on multiple devices, the MACSI interface allows for commands from all work queues to be interspersed. Assuming that the SCSI devices support overlapped activity on the SCSI bus (using Disconnect/Reconnect), one *In Progress* command for each attached SCSI device can be simultaneously active, resulting in overlapped data streams. Since the Cougar can have two fully independent SCSI buses, it can support two truly simultaneous data streams. If some devices do not support overlapped activity, they can be relegated to the optional second channel, allowing fully functioning devices on the primary channel unrestricted operation. Both channels can, of course, support full SCSI functionality.

Executing Commands

The Cougar reads the Command Queue, determines which entry to execute next, and moves the appropriate Command Queue entry and IOPB into one of its internal work queues. Commands intended for a specific device are sent to the work queue dedicated to that device.

After the Command Queue entry and IOPB are placed into a work queue, the slot in the Command Queue formerly filled by the command becomes available for re-use by the host. Even in the unlikely case that the Command Queue is full when the host tries to enter a command, the Cougar provides efficient operation by optionally interrupting the host when an entry becomes available in the Command Queue.

Once the command is moved to the appropriate work queue, it is executed at the first opportunity. The Cougar then posts command completion to the Command Response Block (CRB) in either Short I/O or system memory, and generates an optional interrupt. The host acknowledges the command completion by writing a word to the CRB, releasing it for further use.

Master Command Entry and Work Queue 0

In order to initialize the board, as well as to execute high priority commands, the Cougar provides two auto-initialized facilities: the **Master Command Entry and** the **Work Queue 0.**

The Master Command Entry and Work Queue 0 allow a single command to be issued and the host to poll for its completion before issuing the next one. This mechanism is used, upon power-up, to initialize the rest of the work queues for normal SCSI operations, and in error recovery operations.

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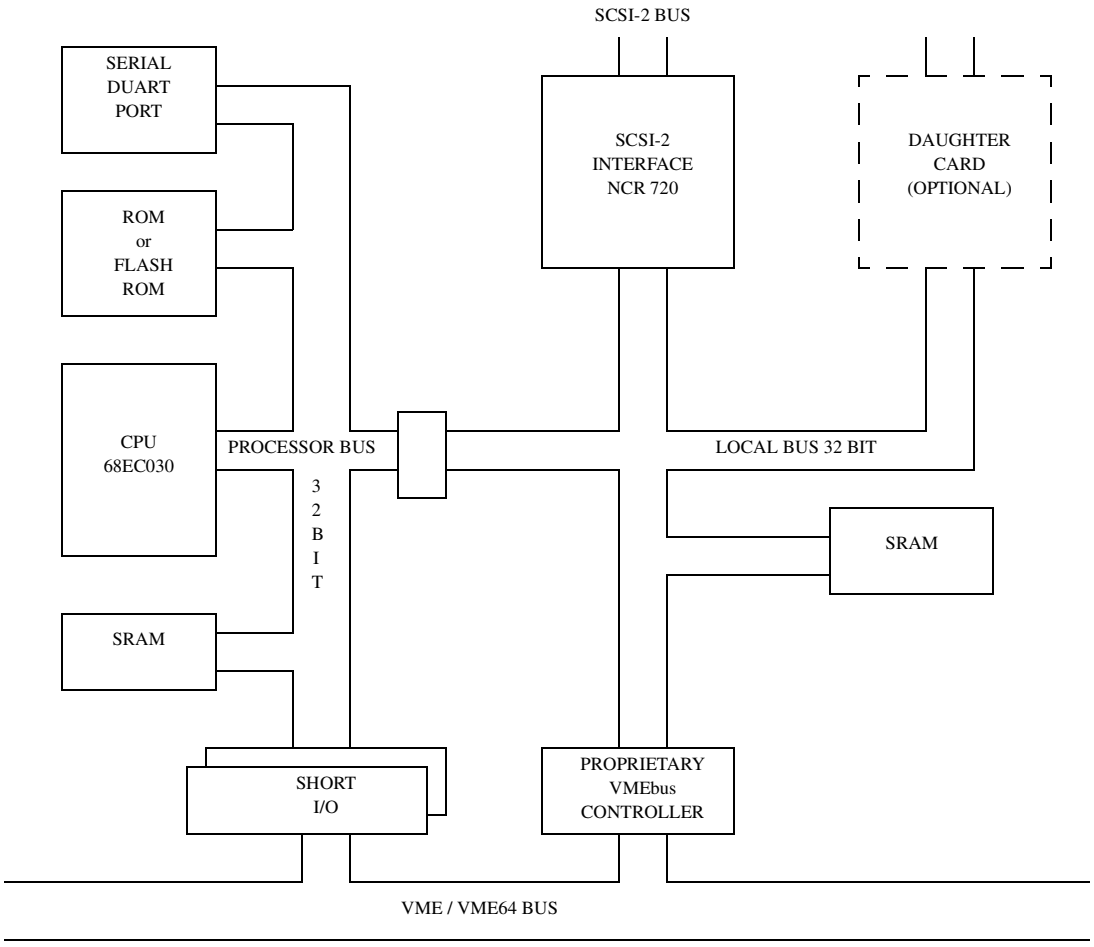


Figure 1-1. V/SCSI-2 Cougar II Block Diagram

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Chapter 2
Installation

Overview

To insure safe installation, read this chapter before attempting installation of either the V/SCSI-2 4220 Cougar II motherboard or the V/SCSI-2 4220 Cougar II Wide motherboard into your system. If you have any questions regarding installation which are not answered in this chapter, please contact Interphase Customer Service at (214) 919-9111.

The boards are installed into the VMEbus system using the following steps:

1. Visual Inspection
2. Fuse And Diagnostic LEDs
3. Set Motherboard Jumpers
   3a. Cougar II
   3b. Cougar II Wide
4. Set Motherboard Termination
5. Set Daughter Card Jumpers And Termination
   5a. Single-Ended SCSI-2 Daughter Card
   5b. Differential SCSI-2 Daughter Card
   5c. Differential SCSI-2 Wide Daughter Card
   5d. Printer (Short Line)
   5e. Printer (Long Line)
6. Cabling Procedure
7. Installing the Board

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WARNING

1. Catastrophic DAMAGE can result from improper connections. Therefore, those planning to connect power sources to the VMEbus to feed the user-defined 96 pins of P2 (Rows A and C) should FIRST CHECK to ensure that all boards installed are compatible with those connections.

2. Do NOT install or apply power to a damaged board. Failure to observe this warning could result in extensive damage to the board and/or system.

3. Caution! The controller is extremely sensitive to electrostatic discharge (ESD), and the board could be damaged if handled improperly. Interphase ships the board enclosed in a special anti-static bag. Upon receipt of the board, take the proper measures to eliminate board damage due to ESD (i.e., wear a wrist ground strap or other grounding device).

The installation procedure will vary depending on the desired configuration. Variables include:

- One or two SCSI channels (up to 7 devices per channel for a Fast SCSI-2 channel, and up to 15 devices for a Fast and Wide SCSI-2 channel)
- Single-ended vs. differential SCSI operation for each channel.
- Fast SCSI-2 vs. Fast and Wide SCSI-2 I/O for the SCSI daughter card, if any.
- Use of a printer port daughter card instead of a second SCSI channel.

Table 2-1 summarizes the 4220 Cougar II board products available from Interphase to implement various combinations of the above functions. The SCSI Bus drivers on the above products are not convertible. That is, a board with single-ended SCSI drivers cannot be converted to differential, and vice versa. However, a single-ended motherboard can have a differential daughter card, and a differential motherboard can have a single-ended daughter card.

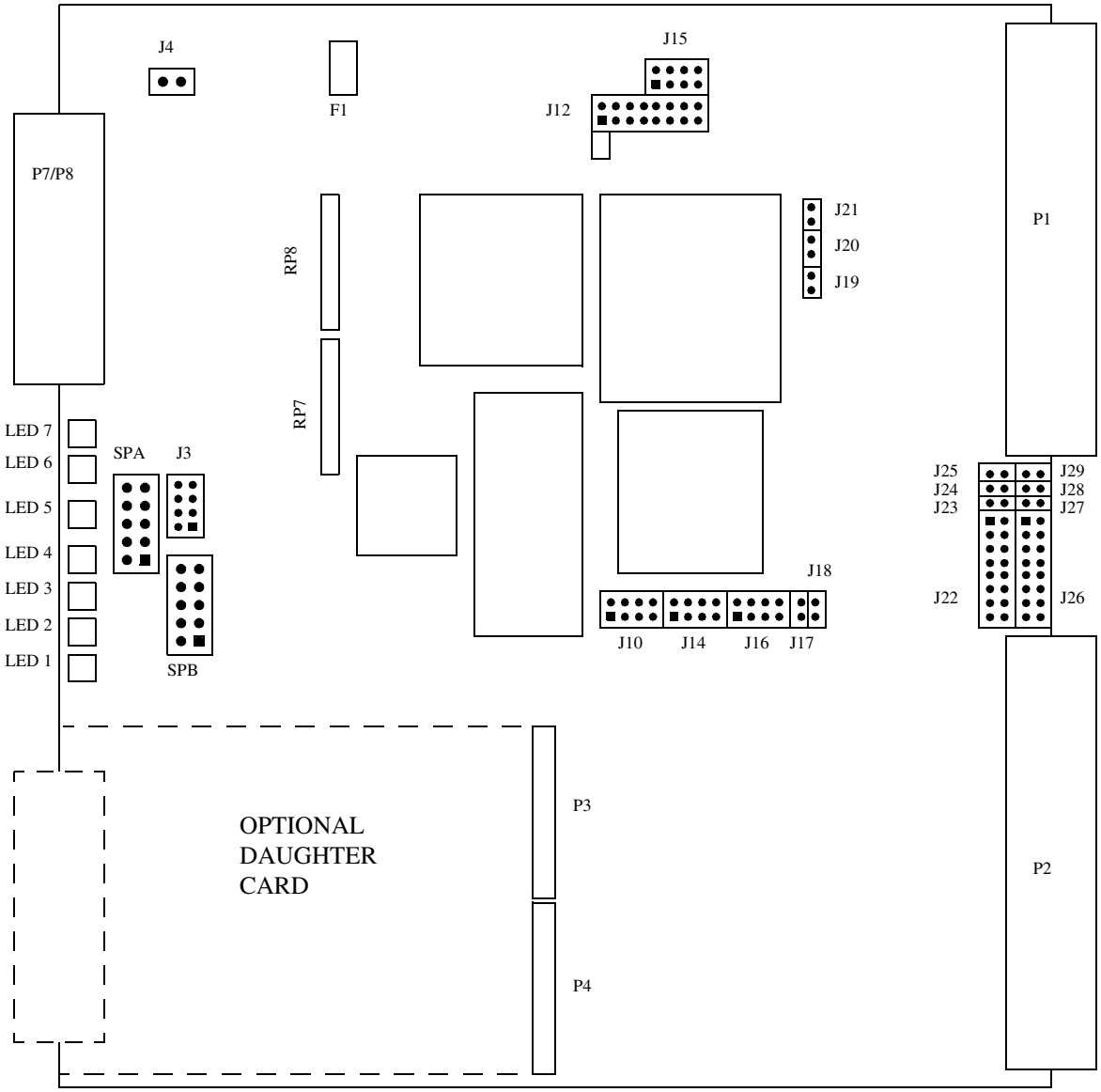
NOTE: The jumper designations differ on the Cougar II and the Cougar II Wide board layouts. Refer to page 2-4 for the Cougar II and page 2-6 for The Cougar II Wide.

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Table 2-1. 4220 Cougar II Wide Products

PRODUCT	DESCRIPTION
Single-ended V/SCSI-2 4220 Cougar II Motherboard	Provides one single-ended SCSI channel with 8-bit SCSI I/O. Signals are routed off P8.
Differential V/SCSI-2 4220 Cougar II Motherboard	Provides one differential SCSI channel with 8-bit SCSI I/O. Signals are routed off P8.
Single-ended V/SCSI-2 4220 Cougar II Wide Motherboard	Provides one single-ended SCSI channel with 16-bit SCSI I/O. Signals are routed off P8.
Differential V/SCSI-2 4220 Cougar II Wide Motherboard	Provides one differential SCSI channel with 16-bit SCSI I/O. Signals are routed off P8.
Fast and Wide Single-ended SCSI-2 Daughter Card	Adds one single-ended SCSI channel with 16-bit SCSI I/O to any 4220 motherboard. Signals are routed off P13.
Fast and Wide Differential SCSI-2 Daughter Card	Adds one differential SCSI channel with 16-bit SCSI I/O to any 4220 motherboard. Signals are routed off P13.
Fast Single-ended SCSI-2 Daughter Card	Adds one single-ended SCSI channel with 8-bit SCSI I/O to any 4220 motherboard. Signals are routed off P13.
Fast Differential SCSI-2 Daughter Card	Adds one differential SCSI channel with 8-bit SCSI I/O to any 4220 motherboard. Signals are routed off P13.
Centronics/Short Line Daughter Card	Adds one Centronics Short Line Printer Port to any 4220 motherboard. Signals are routed off P9.
Dataproducts Long Line Daughter Card	Adds one Dataproducts Long Line Printer Port to any 4220 motherboard. Signals are routed off P9.

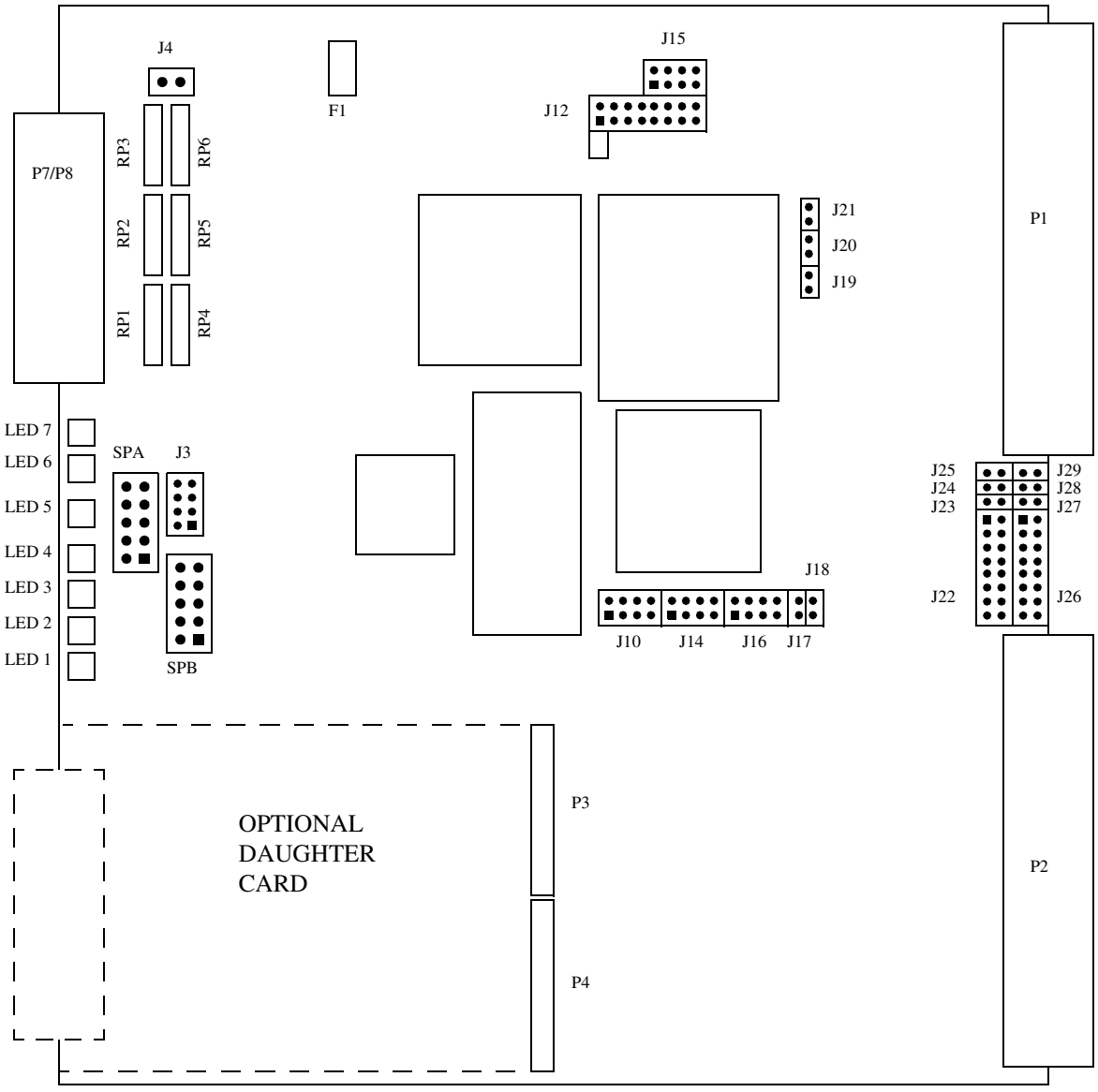
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P8 is a 68-pin micro D "P" connector
P7 is a 50-pin ribbon "A" connector

Figure 2-1. V/SCSI-2 4220 Cougar II Single-Ended Board Layout

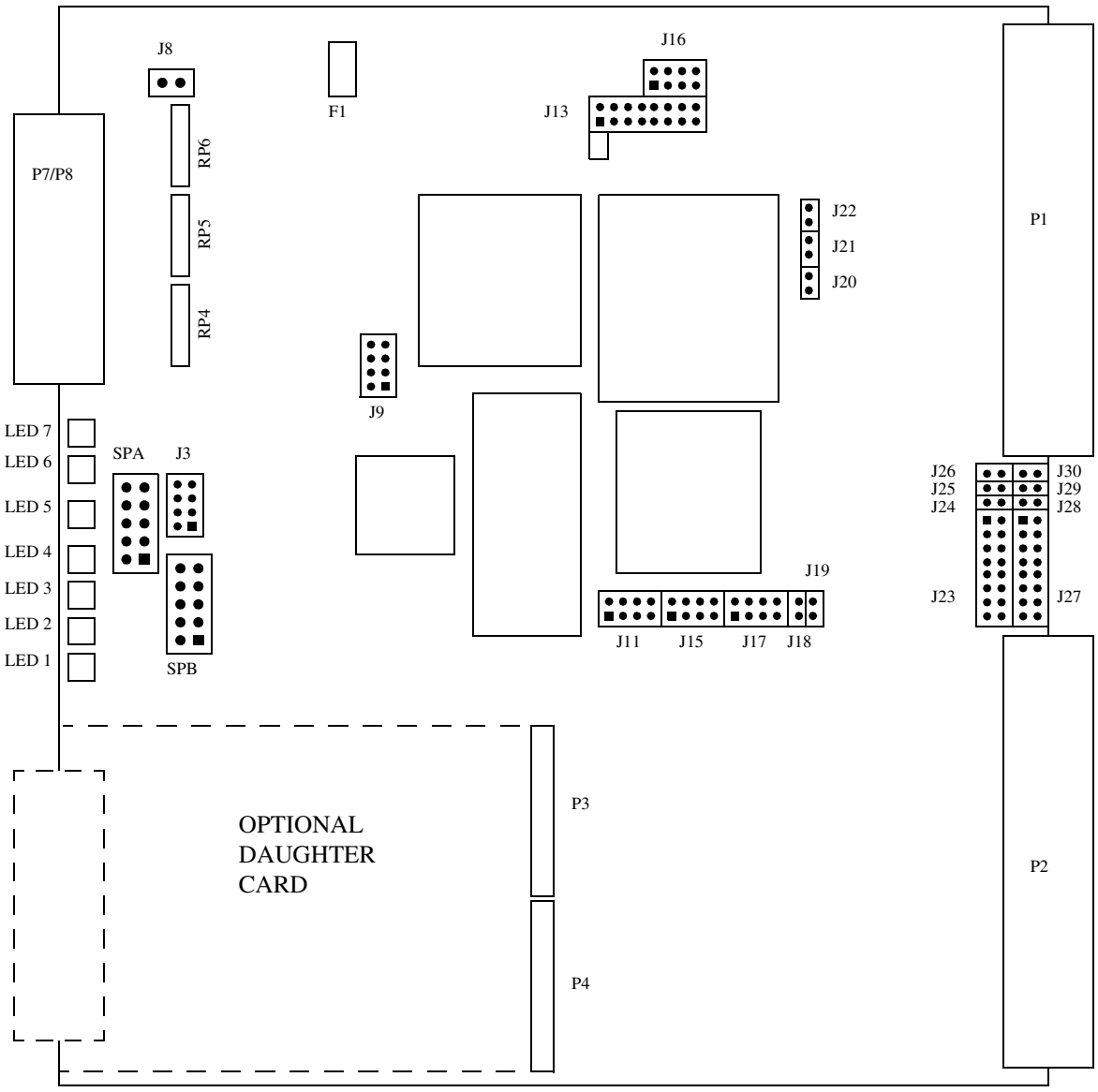
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NOTE: RP7 and RP9 (not pictured) are not SCSI Terminators. Do not remove.
P8 is a 68-pin micro D "P" connector
P7 is a 50-pin ribbon "A" connector

Figure 2-2. V/SCSI-2 4220 Cougar II Differential Board Layout

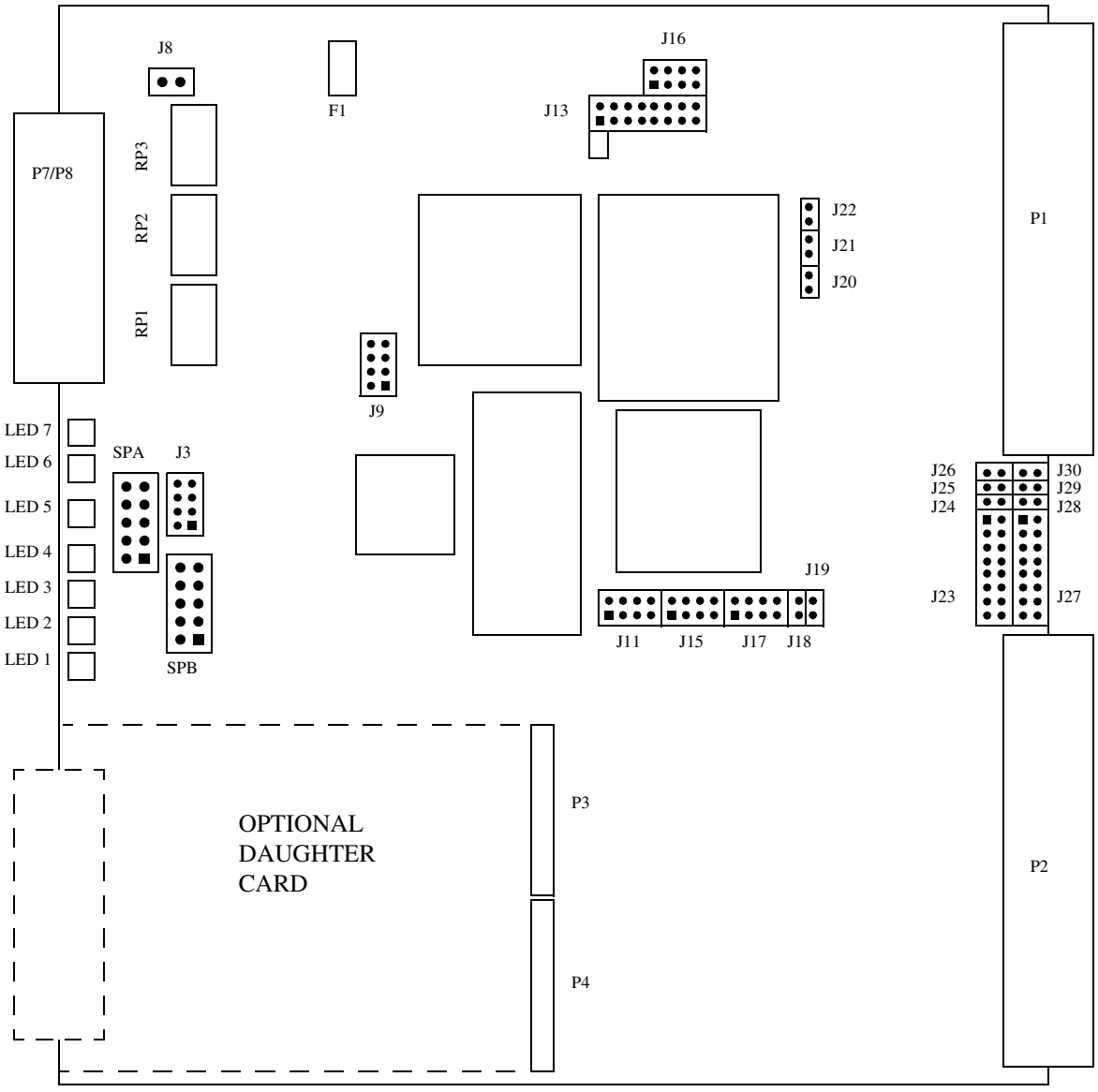
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NOTE: P8 is a 68-pin micro D "P" connector
P7 is a 50-pin ribbon "A" connector

Figure 2-3. V/SCSI-2 4220 Cougar II Wide Single-Ended Board Layout

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NOTE: P8 is a 68-pin micro D "P" connector
P7 is a 50-pin ribbon "A" connector

Figure 2-4. V/SCSI-2 4220 Cougar II Wide Differential Board Layout

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Installation Procedure: V/SCSI-2 4220 Cougar II Motherboard

Proper installation of the Cougar II motherboard (hereafter referred to as the Cougar II) requires the following seven step procedure. Follow step 3a for the Cougar II and step 3b for the Cougar II Wide motherboard. Skip step 5 if you do not have a daughter board.

Step 1. Visual Inspection

Always wear an anti-static or grounding device before attempting the installation of this board. Remove the board from the anti-static bag, and visually inspect it to ensure no damage has occurred during shipment. A visual inspection is usually sufficient, since Interphase thoroughly checks each board just prior to shipment. After verifying the presence of all parts and the condition of the board, proceed with the installation.

Step 2. Fuse And Diagnostic LEDs

Fuse

The Cougar II board uses a 1.5A fuse (part number LITTELFUSE 273-01.5) (F1) to protect the SCSI terminator power when provided by the Cougar. Refer to the board layout to determine the location of the fuse on the board.

Diagnostic LEDs

This motherboard has 7 board status LEDs mounted on the component side of the board. Refer to the board layout illustrations (Figures 2-1 and 2-2) on page 2-4 and page 2-5 for the location and identification of the LEDs. Table 2-2 on page 2-9 summarizes the function of these LEDs.

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Table 2-2. V/SCSI-2 4220 LEDs

DESIGNATOR	FUNCTION
LED1	Board Status 0 (LSB)
LED2	Board Status 1
LED3	Board Status 2
LED4	Board Status 3 (MSB)
LED5	Board OK (Red/Green) Green = Board OK
LED6	Term Power (On = OK)
LED7	SCSI Bus Busy (On = Busy)

Board Status LEDs

LEDs 1, 2, 3 and 4 are Board Status LEDs providing the following functions:

- Power On Self Test (POST) Mode
- Monitor Mode
- Run Mode

POST Mode: Provides diagnostics for the CPU and Buffer. Refer to Table 2-3 for a list of diagnostics performed while in this mode. The time required for the board to complete normal power-up diagnostics is approximately 200 milliseconds.

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Table 2-3. Board Status Diagnostics Used In POST Mode

HEX CODE	DIAGNOSTICS	DEFINITION	TYPE OF TEST
0x01	CPU Register Test	CPUFAIL	CPU Core Test
0x02	ROM Checksum Test	ROMFAIL	CPU Core Test
0x03	Walking 1's SRAM	STAT1FAIL	CPU Core Test
0x04	Walking 0's SRAM	STAT0FAIL	CPU Core Test
0x05	Decrementing Longwords	STATLFAIL	CPU Core Test
0x06	Word Access	STATWFAIL	CPU Core Test
0x07	Byte Access	STATBFAIL	CPU Core Test
0x08	Reserved	RESERVED	CPU Core Test
0x09	Walking 1's In Buffer	BUFFERFAIL1	Static Buffer Test
0x0a	Walking 0's In Buffer	BUFFERFAIL0	Static Buffer Test
0x0b	Decrementing Longwords	BUFFERFAIL	Static Buffer Test
0x0c	Walking 1's,0's VME DMA	VMEFAIL	Control Register Access
0x0d	Motherboard FEC Tests	FEC0 & 1	Control Register Access
0x0e	Daughter Card FEC Tests	FEC2 & 3	Control Register Access

Monitor Mode: LEDs sequentially flicker when Serial Port A is active and On-Board monitor controls the board.

Run Mode: The board accepts commands from the host. If all LEDs are extinguished, no commands are on the Cougar and the board is completely idle. Refer to Table 2-4 for a complete definition of the Board Status LEDs in the Run Mode.

Table 2-4. Run Mode LED Matrix

LED1	LED2	LED3	LED4	FUNCTION
ON	OFF	OFF	OFF	1-4 Commands On Board
ON	ON	OFF	OFF	5-16 Commands On Board
ON	ON	ON	OFF	17-64 Commands On Board
ON	ON	ON	ON	65 or More Commands On Board

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Step 3a. Check Cougar II Board Jumpers

Check all onboard, user-configurable jumpers for proper configuration for your system. The motherboard layouts on pages 2-4 and 2-5 show the jumper locations for the Cougar II Single-Ended and Differential motherboards. (For Cougar II Wide jumper settings, skip to step 3B).

Motherboard Jumper Settings

The following are jumpers and the default settings used on the motherboard.

NOTE: Jumpers which are not described are not user-configurable and should remain as set at the factory.

J3 REMOTE LED CONNECTOR: Used to cable LEDs to a 9U front panel (Optional).

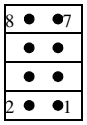


Table 2-5. J3 Remote LED Connector Pinout

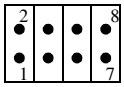
PIN	DESCRIPTION
1	LED 3
2	LED 2
3	LED 4
4	LED 1
5	LED 5 (Green)
6	LED 5 (Red)
7	+5V
8	LED 5 ANODE

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J4 Terminator Power to Primary SCSI Bus:

Connects terminator power to the primary SCSI bus. Placing a jumper on J4 connects the power. The Cougar II is shipped with the jumper installed on J4 (Default is ON).

J10 Firmware Options:



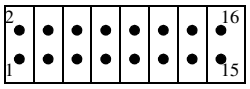
(Pins 1-2) 16-Bit Block Mode Enabled (Default is OFF)
ON: 16-Bit Block Mode Disabled
OFF: 16-Bit Block Mode Enabled

(Pins 3-4) SysFail (Default is OFF)
ON: Clear SysFail after passing Power-up Diagnostics
OFF: Clear SysFail before running Power-up Diagnostics

(Pins 5-6) Reset SCSI Bus on Powerup (Default is OFF)
ON: Disabled
OFF: Enabled

(Pins 7-8) GDB Debugger Enabled (Default is OFF)
ON: Debugger Enabled
OFF: Debugger Disabled

J12 SCSI ID & VME Bus Grant Level



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Primary SCSI Channel ID (J12 Pins 1-6)

Table 2-6. Primary SCSI Channel ID

PRIMARY SCSI ID	J12 PIN #		
	1-2	3-4	5-6
0	0	0	0
1	0	0	F
2	0	F	0
3	0	F	F
4	F	0	0
5	F	0	F
6	F	F	0
7*	F*	F*	F*

*=Factory Default
0=On
F=Off

Secondary SCSI Channel ID (J12 Pins 7-12)

Table 2-7. Secondary SCSI Channel ID

SECONDARYS CSI ID	J12 PIN #		
	7-8	9-10	11-12
0	0	0	0
1	0	0	F
2	0	F	0
3	0	F	F
4	F	0	0
5	F	0	F
6	F	F	0
7*	F*	F*	F*

*=Factory Default
0=On
F=Off

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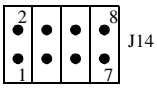
VME Bus Grant (J12 Pins 13-16)

Table 2-8. VME Bus Grant Settings

BUS GRANT	J12 PIN #	
	13-14	15-16
0	0	0
1	0	F
2	F	0
3*	F*	F*

*=Factory Default
0=On
F=Off

J14 Firmware Options/Secondary Short I/O Size



Firmware Options (J14 Pins 1-4)

(Pins 1-2) Load Firmware (Default is **OFF**)
ON: Load Firmware from on-board buffer
OFF: Load Firmware from EPROM

(Pins 3-4) On-board Monitor Enable (Default is **OFF**)
ON: Stop in monitor after loading firmware
OFF: Normal Run mode

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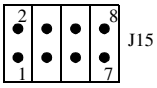
Secondary Short I/O Size (J14 Pins 5-8)

Table 2-9. Secondary Short I/O Size

J14 Pin #		Size (Bytes)
5-6	7-8	
F	F	256 bytes of Secondary Short I/O space
F	0	512 bytes of Secondary Short I/O space
0	F	1K bytes of Secondary Short I/O space
0*	0*	2K* bytes of Secondary Short I/O space

*=Factory Default
0=On
F=Off

J15 Firmware Options:



(Pins 1-2) Delayed Initialization of SCSI Bus (Default is **OFF**)
ON: Initialize only after IOPB Command (0x41)
OFF: Initialize after power-up self-test

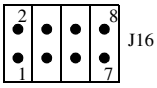
(Pins 3-4) Memory Test Enabled (Default is **OFF**)
ON: Disabled
OFF: Enabled

(Pins 5-6) Console Message Disable (Default is **OFF**)
ON: Disabled
OFF: Enabled

(Pins 7-8) GDB Enable Point (Default is **OFF**)
ON: GDB Initialized on Exit
OFF: GDB Initialized on Reset

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J16 Primary Short I/O Size/Reset Enable



Primary Short I/O Size (J16 Pins 1-4)

Table 2-10. Primary Short I/O Size

J16 Pin #		Size (Bytes)
1-2	3-4	
F	F	256 bytes of Secondary Short I/O space
F	0	512 bytes of Secondary Short I/O space
0	F	1K bytes of Secondary Short I/O space
0*	0*	2K* bytes of Secondary Short I/O space

*=Factory Default
0=On
F=Off

Reset Enable (J16 Pins 5-8)

(Pins 5-6) Secondary Master Control Register (Default is **OFF**)

(Pins 7-8) Primary Master Control Register (Default is **ON**)

J17 Secondary Channel Address Modifiers:

ON: Secondary Channel Address Modifiers 29 or 2D
OFF: Secondary Channel Address Modifiers 2D only (Default is **OFF**)

J18 Primary Channel Address Modifiers:

ON: Primary Channel Address Modifiers 29 or 2D
OFF: Primary Channel Address Modifier 2D only (Default is **ON**)

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J19 VME Bus Grant Input Level 2 Disable

ON: Enabled
OFF: Disabled (Default is **ON**)

J20 VME Bus Grant Input Level 0 Disable

ON: Enabled
OFF: Disabled (Default is **OFF**)

J21 VME Bus Grant Input Level 1 Disable

ON: Enabled
OFF: Disabled (Default is **OFF**)

J22/J23/J24/J25 Primary Short I/O Base Address

Table 2-11 shows the jumper settings for the Primary Short I/O base address for the default 2K Short I/O size. The tables for the other sizes are in *Appendix E, Primary Base Addresses for J22/J23/J24/J25, page E-1*.

NOTE: Setting jumper J22 pins 15-16 to ON (O) and all other pins to OFF (F) will disable Primary Short I/O.

J26/27/28/29 Secondary Short I/O Base Address

The factory default for these jumpers is J26 pins 15-16 ON, and all others OFF. Secondary Short I/O is disabled.

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Table 2-11. Base Address of Primary 2K Short I/O Space

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
0000	F	F	F	0	0	0	0	0	F	F	F
0800	F	F	F	F	0	0	0	0	F	F	F
1000	F	F	F	0	F	0	0	0	F	F	F
1800	F	F	F	F	F	0	0	0	F	F	F
2000	F	F	F	0	0	F	0	0	F	F	F
2800	F	F	F	F	0	F	0	0	F	F	F
3000	F	F	F	0	F	F	0	0	F	F	F
3800	F	F	F	F	F	F	0	0	F	F	F
4000	F	F	F	0	0	0	F	0	F	F	F
4800	F	F	F	F	0	0	F	0	F	F	F
5000	F	F	F	0	F	0	F	0	F	F	F
5800	F	F	F	F	F	0	F	0	F	F	F
6000	F	F	F	0	0	F	F	0	F	F	F
6800	F	F	F	F	0	F	F	0	F	F	F
7000	F	F	F	0	F	F	F	0	F	F	F
7800	F	F	F	F	F	F	F	0	F	F	F
8000	F	F	F	0	0	0	0	F	F	F	F
8800	F	F	F	F	0	0	0	F	F	F	F
9000	F	F	F	0	F	0	0	F	F	F	F
9800	F	F	F	F	F	0	0	F	F	F	F
A000	F	F	F	0	0	F	0	F	F	F	F
A800	F	F	F	F	0	F	0	F	F	F	F
B000	F	F	F	0	F	F	0	F	F	F	F
B800	F	F	F	F	F	F	0	F	F	F	F
C000	F	F	F	0	0	0	F	F	F	F	F
C800	F	F	F	F	0	0	F	F	F	F	F
D000	F	F	F	0	F	0	F	F	F	F	F
D800	F	F	F	F	F	0	F	F	F	F	F
E000	F	F	F	0	0	F	F	F	F	F	F
E800	F	F	F	F	0	F	F	F	F	F	F
F000	F	F	F	0	F	F	F	F	F	F	F
F800	F	F	F	F	F	F	F	F	F	F	F

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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W *Step 3b. Check Cougar II Wide Motherboard Jumpers*

Check all onboard user-configurable jumpers for proper configuration for operation within your system. The location of the jumpers is shown on the Cougar II Wide motherboard layouts, page 2-6 and page 2-7.

Motherboard Jumper Settings

The following are jumpers and the default settings used on the motherboards.

NOTE: Jumpers which are not described are not user-configurable and should remain as set at the factory.

J3 Remote LED Connector: Used to cable LEDs to a 9U front panel (Optional).

J5 (Default is **OFF**)

J6 (Default is **OFF**)

J7 (Default is **OFF**)

J8 TERMINATOR POWER:

ON: Supply SCSI terminator power to SCSI Bus (Default is **ON**)
OFF: Does not supply SCSI terminator power to SCSI bus

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J9 Primary SCSI Channel ID

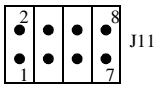
Table 2-12. Primary SCSI Channel ID

SCSI ID	J9 PIN #			
	1-2	3-4	5-6	7-8
0	0	0	0	0
1	0	0	0	F
2	0	0	F	0
3	0	0	F	F
4	0	F	0	0
5	0	F	0	
6	0	F	F	0
7*	0*	F*	F*	F*
8	F	0	0	0
9	F	0	0	F
10	F	0	F	0
11	F	0	F	F
12	F	F	0	0
13	F	F	0	F
14	F	F	F	0
15	F	F	F	F

*=Factory Default
0=On
F=Off

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J11 Firmware Options



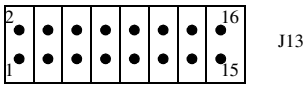
(Pins 1-2) 16-Bit Block Mode Enabled (Default is **OFF**)
ON: 16-Bit Block Mode Disabled
OFF: 16-Bit Block Mode Enabled

(Pins 3-4) SysFail (Default is **OFF**)
ON: Clear SysFail after passing Diagnostics
OFF: Clear SysFail before running Power-up Diagnostics

(Pins 5-6) Reset SCSI Bus on Power-up (Default is **OFF**)
ON: Reset Disabled
OFF: Reset Enabled

(Pins 7-8) GDB Debugger Enabled (Default is **OFF**)
ON: Debugger Enabled
OFF: Debugger Disabled

J13 Secondary SCSI ID/VME Bus Grant for SCSI-2 Fast Daughter card ONLY



(Pins 1-7) Reserved
(Pins 7-12) Secondary SCSI ID for SCSI-2 Fast daughter card

NOTE: Not used for SCSI-2 Wide daughter cards. If a Wide daughter card is used, do not populate pins 7-12.

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Table 2-13. Secondary SCSI Channel ID for SCSI-2 Fast Daughter Card

SCSI ID	J13 PIN #		
	7-8	9-10	11-12
0	0	0	0
1	0	0	F
2	0	F	0
3	0	F	F
4	F	0	0
5	F	0	F
6	F	F	0
7*	F*	F*	F*

*=Factory Default
0=On
F=Off

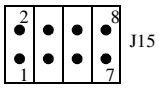
Table 2-14. VME Bus Grant

SCSI ID	J13 PIN #	
	13-14	15-16
0	0	0
1	0	F
2	F	0
3*	F*	F*

*=Factory Default
0=On
F=Off

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J15 Firmware Options/Secondary Short I/O Size:



(Pins 1-2) Load firmware (Default is **OFF**)
ON: Load firmware from onboard buffer
OFF: Load firmware from EPROM

(Pins 3-4) Onboard monitor enable (Default is **OFF**)
ON: Stop in monitor after loading firmware
OFF: Normal run mode

(Pins 5-8) Secondary Short I/O size

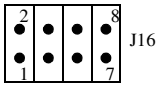
Table 2-15. Secondary Short I/O Size

J15 Pin #		Size (Bytes
5-6	7-8	
F	F	256
F	0	512
0	F	1K
0*	0*	2K*

*=Factory Default
0=On
F=Off

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J16 Firmware Options:



(Pins 1-2) Delayed initiation of SCSI Bus (Default is **OFF**)
ON: Initialize only after IOPB Command (0x41)
OFF: Initialize after power-up self test

(Pins 3-4) Memory test enable (Default is **OFF**)
ON: Disable
OFF: Enable

(Pins 5-6) Console message disable (Default is **OFF**)
ON: Disable
OFF: Enable

(Pins 7-8) GDB enable point (Default is **OFF**)
ON: GDB initialized on exit
OFF: GDB initialized on reset

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J17 Primary Short I/O Size/Reset Enable

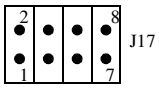


Table 2-16. Primary Short I/O Size

J17 Pin #		Size (Bytes
1-2	3-4	
F	F	256
F	0	512
0	F	1K
0*	0*	2K*

*=Factory Default
0=On
F=Off

(Pins 5-6) Secondary Master Control Register reset enable (Default is **OFF**)
ON: Reset enabled
OFF: Reset disabled

(Pins 7-8) Primary Master Control Register reset enable (Default is **ON**)
ON: Reset enabled
OFF: Reset disabled

J18 Secondary Channel Address Modifiers (Default is **OFF**):

ON: Secondary Channel Address Modifiers 29 or 2D
OFF: Secondary Channel Address Modifiers 2D only

J19 Primary Channel Address Modifiers (Default is **OFF**):

ON: Primary Channel Address Modifiers 29 or 2D
OFF: Primary Channel Address Modifiers 2D only

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J20/J21/J22 VME Bus Grant IN:

J20 (Default is **OFF**)

ON: VME Bus Grant IN 2 enabled
OFF: VME Bus Grant IN 2 disabled

J21 (Default is **OFF**)

ON: VME Bus Grant IN 1 enabled
OFF: VME Bus Grant IN 1 disabled

J22 (Default is **OFF**)

ON: VME Bus Grant IN 0 enabled
OFF: VME Bus Grant IN 0 disabled

J23/J24/J25/26 Primary Short I/O Base Address

Table 2-20 shows the base address jumper settings for the default 2K Short I/O size. The tables for the other sizes are in *Appendix E, Primary Base Address for J23/J24/J25/J26, page E-1*.

NOTE: Setting jumper J23 pins 15-16 to ON (O) and all other pins to OFF (F) will disable the Primary Short I/O.

J27/J28/J29/J30 Secondary Short I/O Base Address

The factory default for these jumpers is J27 pins 15-16 **ON** and all others **OFF**. Secondary Short I/O is disabled.

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Table 2-17. Base Address of Primary 2K Short I/O Space

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
0000	F	F	F	0	0	0	0	0	F	F	F
0800	F	F	F	F	0	0	0	0	F	F	F
1000	F	F	F	0	F	0	0	0	F	F	F
1800	F	F	F	F	F	0	0	0	F	F	F
2000	F	F	F	0	0	F	0	0	F	F	F
2800	F	F	F	F	0	F	0	0	F	F	F
3000	F	F	F	0	F	F	0	0	F	F	F
3800	F	F	F	F	F	F	0	0	F	F	F
4000	F	F	F	0	0	0	F	0	F	F	F
4800	F	F	F	F	0	0	F	0	F	F	F
5000	F	F	F	0	F	0	F	0	F	F	F
5800	F	F	F	F	F	0	F	0	F	F	F
6000	F	F	F	0	0	F	F	0	F	F	F
6800	F	F	F	F	0	F	F	0	F	F	F
7000	F	F	F	0	F	F	F	0	F	F	F
7800	F	F	F	F	F	F	F	0	F	F	F
8000	F	F	F	0	0	0	0	F	F	F	F
8800	F	F	F	F	0	0	0	F	F	F	F
9000	F	F	F	0	F	0	0	F	F	F	F
9800	F	F	F	F	F	0	0	F	F	F	F
A000	F	F	F	0	0	F	0	F	F	F	F
A800	F	F	F	F	0	F	0	F	F	F	F
B000	F	F	F	0	F	F	0	F	F	F	F
B800	F	F	F	F	F	F	0	F	F	F	F
C000	F	F	F	0	0	0	F	F	F	F	F
C800	F	F	F	F	0	0	F	F	F	F	F
D000	F	F	F	0	F	0	F	F	F	F	F
D800	F	F	F	F	F	0	F	F	F	F	F
E000	F	F	F	0	0	F	F	F	F	F	F
E800	F	F	F	F	0	F	F	F	F	F	F
F000	F	F	F	0	F	F	F	F	F	F	F
F800	F	F	F	F	F	F	F	F	F	F	F

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Step 4. Set Motherboard Termination

The SCSI specification requires the bus to be terminated at both ends of the SCSI cable. It does not allow any other termination; otherwise, a bus impedance mismatch occurs.

The primary channel (Channel 0) and optional secondary SCSI channel (Channel 1) are each provided with separate terminating resistors. The following statement applies to either channel: If the port is at either end of the SCSI cable, the channel's terminating resistors should be left in place. If the port is not at the end of the cable, the termination should be removed.

All versions of the 4220 Cougar II are shipped with termination installed. These resistors provide termination for Channel 0. If Channel 0 is not at one end of the SCSI cable, remove the indicated terminating resistors from the motherboard (Table 2-18).

Table 2-18. Motherboard Terminators

Cougar II Single-Ended	RP7, RP8	
Cougar II Differential	RP1-RP6	Do Not Remove RP7, RP9
Cougar II Wide Single-Ended	RP4-RP6	
Cougar II Wide Differential	RP1-RP3	

Step 5. Set Daughter Card Jumpers And Termination

If your setup includes a daughter card, it may be necessary to set the card's jumpers and/or termination. Skip to Step 6 if you do not have a daughter card.

Table 2-19. Single Ended Wide Daughter Card LEDs

DESIGNATOR	FUNCTION	DESCRIPTION
LED1	SCSI BUSY	When illuminated, indicates BSY is asserted on the secondary SCSI bus (channel 1).
LED2	TEMPWR	When illuminated, indicates TERMPWR is OK.

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5a. Single-Ended SCSI-2 Daughter Card

Jumpers Used On Single-Ended SCSI-2 Daughter Card

Component Side

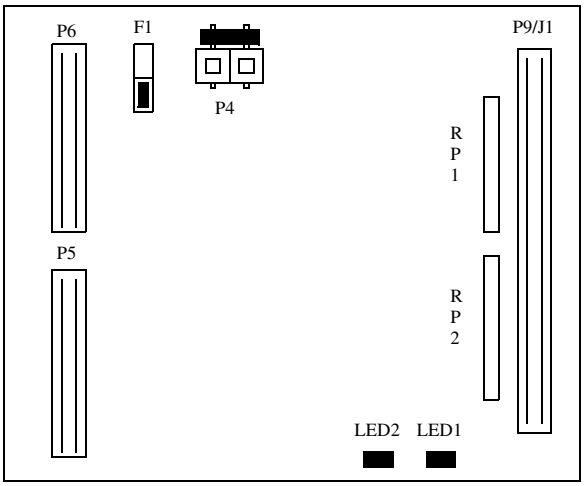
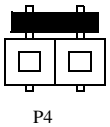


Figure 2-5. Single-Ended SCSI-2 Daughter Card

P4 - Terminator Power to Secondary Bus:

P4 is used to connect terminator power to the secondary SCSI bus. Placing a jumper in P4 connects the power. The card is shipped with a jumper installed in P4 (Factory Default Setting).



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Termination On Single-Ended SCSI-2 Daughter Card

On the Single-Ended Daughter Card, the SIP terminating resistors are labelled RP1 and RP2. If channel 1 is not at the end of the SCSI cable, **REMOVE THESE TERMINATORS** from the daughter card.

Fuse

The daughter card has a 1.5A fuse (F1) (part number LITTELFUSE 273-01.5), used to protect the SCSI terminator power when provided by the card.

LEDs on Single-Ended SCSI-2 Daughter Card

The Single-Ended Daughter Card has 2 LEDs. Refer to Table 2-20 for a description of the LEDs.

Table 2-20. Single-Ended Daughter Card LEDs

DESIGNATOR	FUNCTION	DESCRIPTION
LED2	SCSI BUSY	When illuminated, indicates BSY is asserted on the SCSI bus.
LED1	TEMPWR	When illuminated, indicates TERMPWR is OK.

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5b. Differential SCSI-2 Daughter Card

Jumpers Used On Differential SCSI-2 Daughter Card

Component Side

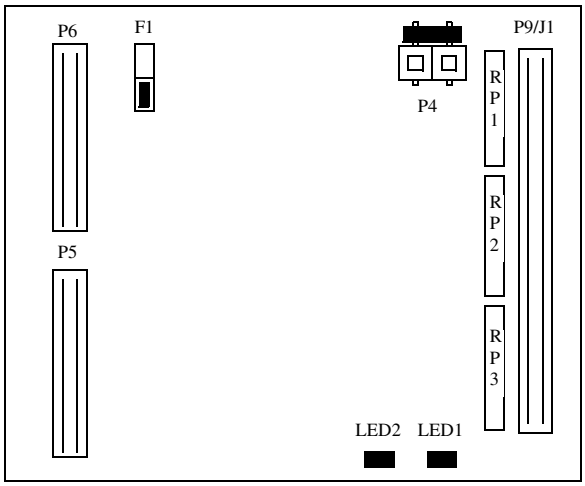
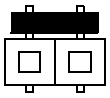


Figure 2-6. Differential SCSI-2 Daughter Card

P4 - Terminator Power to Secondary Bus:

P4 is used to connect terminator power to the secondary SCSI bus. Placing a jumper in P4 connects the power. The card is shipped with a jumper installed in P4.



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Termination On Differential SCSI-2 Daughter Card

On the Differential Daughter Card, the terminating resistors are labelled RP1, RP2, and RP3. If channel 1 is not at the end of the SCSI cable, **REMOVE THESE TERMINATORS** from the daughter card.

Fuse

The daughter card has a 1.5A fuse (F1) (part number LITTELFUSE 273-01.5), used to protect the SCSI terminator power when provided by the card.

LEDs on Differential Daughter Card

The Differential Daughter Card has 2 LEDs. Refer to Table 2-21 for a description of the LEDs.

Table 2-21. Differential Daughter Card LEDs

DESIGNATOR	FUNCTION	DESCRIPTION
LED2	SCSI BUSY	When illuminated, indicates BSY is asserted on the SCSI bus.
LED1	TEMPWR	When illuminated, indicates TERMPWR is OK.

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5c. Differential Wide SCSI-2 Daughter Card

Jumpers Used On Differential Wide SCSI-2 Daughter Card

If your setup includes a Wide differential daughter card, it may also be necessary to set some jumpers on the card. To determine the location of the jumpers, refer to Figure 2-7 .

Component Side

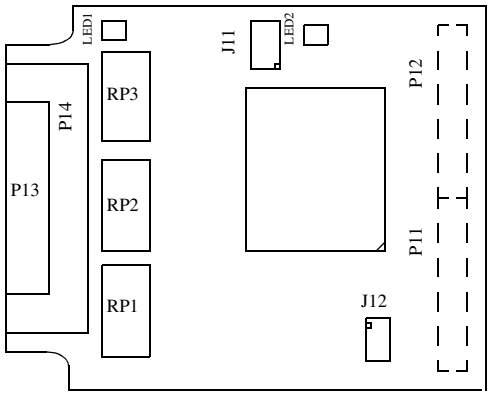
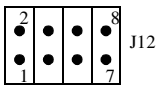


Figure 2-7. Differential Wide SCSI-2 Daughter Card

J11 - Terminator Power to Differential Wide Secondary Bus:

J11 is used to connect terminator power to the secondary SCSI bus. Placing a jumper in J11 connects the power. The daughter card is shipped with a jumper installed in J11.

J12 - SCSI ID of Differential Wide Secondary Bus



Pins 1-2: **(Jumper must be IN. Factory Default Do Not Alter)**

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Table 2-22. Secondary SCSI Channel ID (Differential Wide Channel)

SCSI ID	PIN #		
	3-4	5-6	7-8
0	O	O	O
1	O	O	F
2	O	F	O
3	O	F	F
4	F	O	O
5	F	O	F
6	F	F	O
7*	F*	F*	F*

*=Factory Default
0=On
F=Off

Termination On Differential Wide SCSI-2 Daughter Card

On the Differential Wide Daughter Card, the DIP terminating resistors are labelled RP1-RP3. If channel 1 is not at the end of the SCSI cable, **REMOVE THESE TERMINATORS** from the daughter card.

Fuse

The daughter card has a 1.5A fuse (F1) (part number LITTELFUSE 273-01.5), used to protect the SCSI terminator power when provided by the card.

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LEDs on Differential Wide SCSI-2 Daughter Card

The Differential Wide Daughter Card has 2 LEDs, as shown in 6. For a description of the LEDs, refer to Table 2-23 .

Table 2-23. Differential Wide Daughter Card LEDs

DESIGNATOR	FUNCTION	DESCRIPTION
LED1	SCSI BUSY	When illuminated, indicates BSY is asserted on the secondary SCSI bus (channel 1).
LED2	TEMPWR	When illuminated, indicates TERMPWR is OK.

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5d. Centronics/Dataproducts Short Line Printer Daughter Card

Jumpers Used On Centronics/Dataproducts Printer Daughter Card

If your setup includes a Centronics/Dataproducts Short Line daughter card, it may also be necessary to set some jumpers on the card.

Component Side

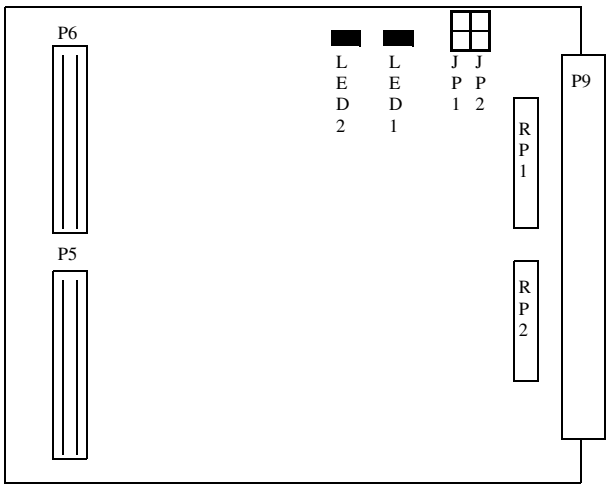


Figure 2-8. Centronics/Dataproducts Short Line Printer Daughter Card

JP1 and JP2 - Printer Type Selection:

Jumpers JP1 and JP2 are used to select the desired interface -- Centronics or Dataproducts Short Line Printer.

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The valid settings for JP1 and JP2 are as follows:

Centronics Printer: JP1: OUT
JP2: IN

Dataproducts Short Line Printer: JP1: IN
JP2: OUT

Termination On Centronics/Dataproducts Printer Daughter Card

Be sure to set the termination appropriately for the printer selected using jumpers JP1 and JP2.

Centronics Printer: RP1 = 470 Ohms
RP2 = Not Installed

Dataproducts Short Line Printer: RP1 = 390 Ohms
RP2 = 390 Ohms

LEDs on Centronics/Dataproducts Printer Daughter Card

Table 2-24. Centronics/Dataproducts Short Line LEDs

DESIGNATOR	FUNCTION	DESCRIPTION
LED1	GOT_LBUS	When illuminated, indicates the printer daughter card is driving the Local Bus.
LED2	COMMAND_IN_PROGRESS	When illuminated, indicates the printer daughter card is executing commands from the motherboard.

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5e. Dataproducts Long Line Printer Daughter Card

Jumpers Used On Dataproducts Long Line Printer Daughter Card

Component Side

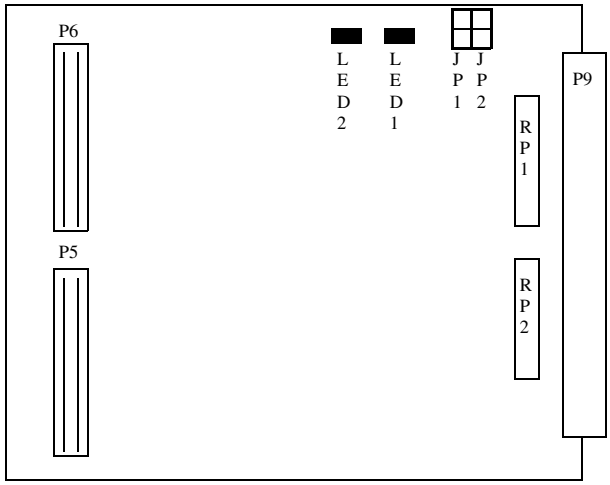


Figure 2-9. Long Line Printer Daughter Card

JP1 and JP2 - Printer Type Selection:

JP1 and JP2 are used to select the desired interface.

Dataproducts Long Line Printer:	JP1: IN
	JP2: IN

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Termination On Dataproducts Long Line Daughter Card

No termination is required for the Dataproducts Long Line printer daughter card.

LEDs on Dataproducts Long Line Daughter Card

Table 2-25. Dataproducts Long Line Daughter Card LEDs

DESIGNATOR	FUNCTION	DESCRIPTION
LED1	GOT_LBUS	When illuminated, indicates the printer daughter card is driving the Local Bus.
LED2	COMMAND_IN_PROGRESS	When illuminated, indicates the printer daughter card is executing commands from the motherboard.

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Step 6. Cabling Procedure

The cabling procedure depends on which 4220 Cougar II motherboard and optional daughter card (if installed) you are using. Refer to the *Appendix B, Connector Printouts and Cabling*, for details on the required cables.

CAUTION

> *System power and peripheral power must be turned **OFF** before attempting to install the controller. Failure to do so may result in severe damage to the board and/or system.*

Once the board is configured, ensure that the host system and peripherals are turned OFF.

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SCSI-2 Cabling Instructions

Table 2-26 summarizes the various SCSI-2 configurations of the 4220 Cougar II.

Table 2-26. SCSI-2 Cable Variations

To Implement:	**Cable the Board as Follows**:
A Single-ended SCSI bus on the primary SCSI channel	Connect a single-ended SCSI "A cable" to the motherboard's P7 connector.
A Differential SCSI bus on the primary SCSI channel	Connect a differential SCSI "A cable" to the motherboard's P7 connector.
A Single-Ended Wide SCSI bus on the primary SCSI channel	Connect a single-ended SCSI "P cable" to the motherboard's P8 connector.
A Differential Wide SCSI bus on the primary SCSI channel	Connect a differential SCSI "P cable" to the motherboard's P8 connector.
A Single-Ended Wide SCSI bus on the secondary SCSI channel card	Connect a single-ended SCSI "P cable" to the daughter card's P13 connector.
A Differential Wide SCSI bus on the secondary SCSI channel	Connect a differential SCSI "P cable" to the daughter card's P13 connector.
A Single-ended SCSI bus on the secondary SCSI channel	Connect a single-ended SCSI "A cable" to the daughter card's P14 connector.
A Differential SCSI bus on the secondary SCSI channel (provided by Fast differential daughter card, if installed)	Connect a differential SCSI "A cable" to the daughter card's P14 connector.

For a description of the "A" cable and "P" cable, refer to the appendices.

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Printer Cabling Instructions

Table 2-27 summarizes printer cabling requirements.

Table 2-27. Printer Cable Instructions

To Implement	Cabling Instructions
A Centronics Printer using the Printer Daughter Card	Connect a Centronics Printer cable to P9 on the Printer Daughter Card. Refer to the Appendices for the cable pinout.
A Dataproducts Short Line Printer	Connect a Dataproducts Printer cable to P9 on the Printer Daughter Card. Refer to the Appendices for the cable pinout.
A Dataproducts Long Line Printer	Connect a Dataproducts Printer cable to P9 on the Printer Daughter Card. Refer to the Appendices for the cable pinout.

RS232 Connectors And Cables

There are two 10 pin connectors (2x5 headers) used as the RS232 port cable connectors. These connectors are the same type used for the second serial port I/O Extension-X.2 of PC compatible machines.

The connectors are labeled "SPA" and "SPB" for Serial Port A and Serial Port B respectively. Refer to either motherboard layout in the front of this chapter for location. Both RS232 ports on the board are configured as Data Terminal Equipment (DTE).

As an option, a terminal may be connected to SPA to view debug information provided by the Cougar II. See Firmware Options jumper settings, in this chapter, to enable/disable the console messages. SPB is used for advanced debug operations, with factory assistance.

Step 7. Installing the Board

1. Carefully slide the board into the VMEbus card slot. It should slide all the way in without any difficulty. If it doesn't, pull it out and check to make sure that there are no cables in the way.

2. Once the board is properly seated in the slot, tighten the captive mounting screws on each end of the front panel.

3. Connect the SCSI devices to the SCSI cable(s), following the directions given by the device manufacturers.

4. Apply power to the system and peripherals. The board OK LED on the Cougar II should change from **red** to **green** when the power-on self test is complete and the board enters **Run** mode.

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Chapter 3
System Interface

Overview

The host communicates with the board through the onboard *Short I/O* space, mapped into the Short I/O space of the VMEbus. The MASCI system-level interface allows the board to reset and initialize the board, set up multiple work queues, queue multiple commands internally, read command responses and board configuration, and status information. Every location can be physically both written to and read from by the host at any time, but the protocol of the MACSI System Interface puts some restrictions upon when certain areas should be accessed. Also, some areas are logically write only or read only.

NOTE

When issuing commands or otherwise interacting with the board via the MACSI interface, the host must clear all bits and fields marked "RESERVED" to 0. For performance reasons, the board does not execute a sanity check on all reserved fields. Clearing these reserved fields helps avoid driver problems that may otherwise occur when a later firmware implementation is released.

MACSI partitions the Short I/O space into six major sections:

- Master Control/Status Block (MCSB)
- Master Command Entry (MCE)
- Command Queue (CQ)
- Host Usable Space (HUS)
- Command Response Block (CRB)
- Controller Specific Space (CSS)

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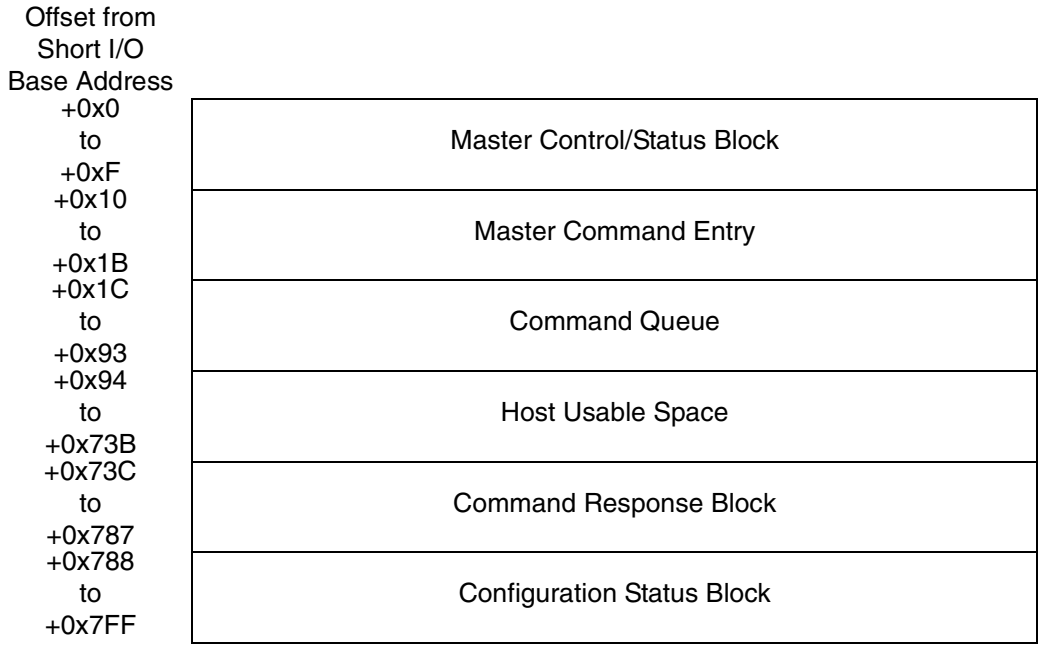


Figure 3-1. Typical Memory Map of 2K Short I/O Space

Master Control/Status Block (MCSB)

The *Master Control/Status Block* (MCSB) is used to exchange information relative to the overall operation of the board. The 16-byte MCSB consists of the *Master Status Register* (MSR), the *Master Control Register* (MCR), the *Interrupt on Queue Available Register* (IQAR), the *Queue Head Pointer* (QHP), and the *Thaw Work Queue Register* (TWQR).

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Table 3-1. Master Control/Status Block (MCSB)

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	MASTER STATUS REGISTER															
0x1	MASTER CONTROL REGISTER															
0x2	INTERRUPT ON QUEUE AVAILABLE REGISTER															
0x3	QUEUE HEAD POINTER															
0x4	THAW WORK QUEUE REGISTER															
0x5 To 0x7	RESERVED															

Master Status Register (MSR)

The board uses this register to report board level status. From the host point of reference, this is a READ ONLY register. However, the contents of this register are not valid for 100 microseconds following a controller reset. shows the bit definition.

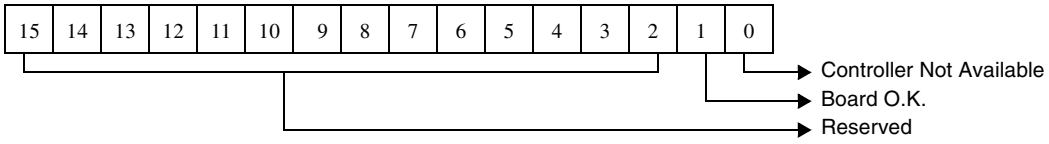


Figure 3-2. Master Status Register (MSR)

Bit 0 Controller Not Available (CNA):

The board sets this bit to 1 to indicate that it is Not Available to receive a command. This condition can be caused either by a controller reset or by the execution of controller diagnostics. CNA will also be set if a board initialization command fails to complete (see Chapter 5, Initialize Controller Command, page). The board will clear this bit when it is capable of accepting a command.

Bit 1 Board OK (BOK):

The board sets this bit to 1 when the power-up diagnostics are completed successfully. A 0 indicates that the board detected a failure during the power-up diagnostics. The host can start polling the Board OK bit 100 microseconds after the board has been powered up or reset, allowing approximately 200 milliseconds for normal power-up diagnostics to complete.

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Table 3-2. Board OK/Controller Not Available Relationship

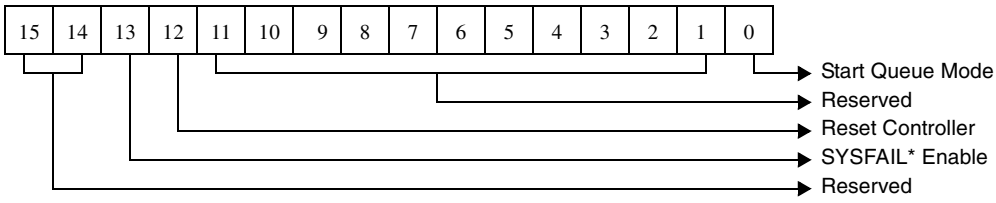
BOK	CNA	Description
0	0	The controller has failed to operate and is not capable of accepting a command.
0	1	Controller is Not Available. If the controller is not still executing power-up diagnostics, then it has either failed to execute power-up correctly or it has failed to complete a board initialize command.
1	1	The controller has successfully completed power-up diagnostics but it is not capable of accepting a command, because it is executing the diagnostics command.
1	0	The controller has completed diagnostics and is capable of receiving commands.

Bits 2-15 Reserved (RSRV):

These bits are reserved and are cleared to 0 by the board.

Master Control Register (MCR)

All bits in this register are both set and cleared by the host. From the board's point of reference, this is a **READ ONLY** register. The board does not ever set any of these bits. The bits are defined in.



NOTE: Reserved bits must be cleared to 0 by the host.

Figure 3-3. Master Control Register (MCR)

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Bit 0 Start Queue Mode (SQM):

Once the Command Queue and work queues are initialized, the SQM bit may be set to "1" by the host. The only operation performed by the 4220 board in response to the host setting this bit is to the *Queue Mode Started Bit* in the *Command Response Status Word* (see pages). The SQM bit is supported to provide backward compatibility with the V/SCSI 4210 Jaguar SCSI-1 controller.

Bits 1 - 11 Reserved (RSRV):

These bits are reserved and must be cleared to 0 by the host.

Bit 12 Reset Controller (RES):

The *RES* bit controls the microprocessor hardware reset line. It also causes a RESET on both of the SCSI buses, if the SCSI reset feature is enabled via jumper setting. The RES bit should be used only to recover from extreme error conditions. **To ensure proper operation, the host must leave this bit set for at least 70 microseconds**.

Bit 13 SYSFAIL* Enable (SFEN):

The *SFEN* bit enables the board to drive the SYSFAIL* signal on the VMEbus if it detects an internal failure during power-up diagnostics or if the firmware enters an unused exception vector. If this bit is *0*, the board will not drive the SYSFAIL* signal under any circumstances. The board initializes this bit to *0* after power-up.

The board does not read the SYSFAIL* Enable bit until detecting an error in the power-up test. After detecting an error, the firmware simply loops on setting the SYSFAIL* line to the level specified by the bit (provided that the board is sufficiently functional to have the bit cleared).

The host should wait until the BOK (Board OK) bit is set in the MSR before enabling this bit.The host may turn off SYSFAIL* from the board by clearing this bit. The host may enable SYSFAIL* after the board has been released from reset. This operation is performed by firmware, and it is possible the board may clear the bit if it is set too soon after power-up. The host should wait until the BOK (Board OK) bit is set in the MSR before modifying this bit.

NOTE: The board drives SYSFAIL* at system reset and immediately clears SYSFAIL* after reset if configured to do so via jumper setting.

Bits 14-15 Reserved (RSRV):

These bits are reserved and must be cleared to 0 by the host.

Interrupt On Queue Available Register (IQAR)

Each Command Queue entry only occupies a slot in the Command Queue until it is moved into a work queue. Thus, the host will almost always have slots available in the Command Queue for issuing commands. In the unlikely event that the Command Queue is full when the host attempts to enter a command, the host must wait until the board transfers a command from the Command Queue to an internal work queue before it can enter the next command.

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The host determines that the Command Queue is full by looking at the Go/Busy bit in the next available Command Queue entry. The Command Queue is full if the Go/Busy bit of the next available Command Queue entry is *1*. If the Command Queue becomes full, the host can poll the Go/Busy bit, waiting until the next Command Queue entry becomes available. The Interrupt on Queue Available Register (IQAR) provides a mechanism to generate an optional interrupt to the host when a entry becomes available in the Command Queue.

The IQAR feature is enabled by setting the Interrupt on Queue Entry Available (IQEA) bit in the register. If the Interrupt on Queue Half Empty Enable bit is also set, the board will not interrupt until the Command Queue is half empty. Otherwise, the interrupt will occur as soon as the board detects one empty entry in the Command Queue. The host should wait until encountering the Queue Full condition before setting the IQEA bit. Once the IQEA bit is set, the board generates an interrupt when the necessary queue conditions are satisfied. The board then clears the IQEA bit.

The level and vector for the IQEA interrupt are supplied by the host in the IQAR. When the necessary queue conditions are satisfied, the board clears the IQEA bit and sets the Queue Entry Available (CQA) bit, and the Command Response Block Valid (CRBV) bit, the Command Response Status Word (CRSW) of the CRB. Though the board provides this mechanism for interrupting the host when space becomes available in the Command Queue, it is preferable to set up a large enough Command Queue so that the full condition occurs infrequently. The number of entries in the Command Queue is set in the CIB (refer to Chapter 5, *Initialize Controller Command*, page).

Note that the generation of this interrupt is not real time. If the host fills in commands from completion interrupts, the queue may already have been filled in by the time the IQAR occurs. Therefore, the host must check the Go/Busy bit before issuing another command.

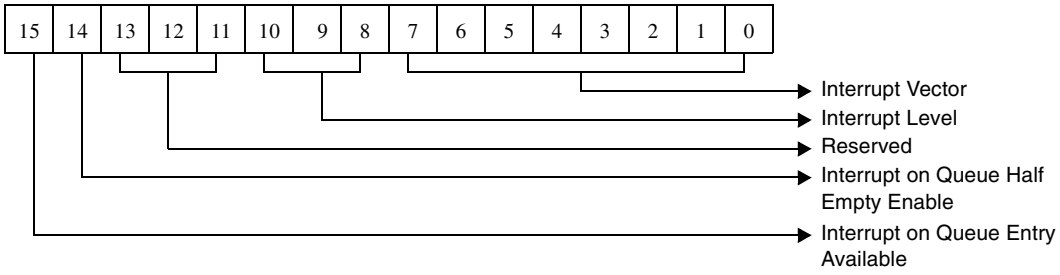


Figure 3-4. Interrupt On Queue Available Register (IQAR)

Bits 0-7 Interrupt Vector for the Interrupt on Queue Available (IV):

The board uses this byte as the interrupt vector when issuing an Interrupt on Queue Available interrupt. This byte is set by the host and is not modified by the board. The host must not modify this byte after setting the IQEA bit.

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Bits 8-10 Interrupt Level for the Interrupt on Queue Available (IL):

These three bits determine the interrupt level that the board will use when issuing an Interrupt on Queue Available interrupt. These bits are set by the host and are not modified by the board. The host must not modify these bits after setting the IQEA bit.

Values of 1 through 7 are allowed. An interrupt level of 0 is allowed only when the IQEA bit is cleared.

Bits 11-13 Reserved (RSRV):

These bits must be cleared to 0 by the host.

Bit 14 Interrupt on Queue Half Empty Enable (IQHE):

This bit is a flag which causes the board to generate the IQEA interrupt when the Command Queue becomes half empty (rather than as soon as one entry becomes available). The Interrupt on Queue Half Empty Enable (IQHE) bit is valid only when the IQEA bit is set. The IQHE bit is set by the host and is not modified by the board. The host must not modify this bit after it has set the IQEA bit.

Bit 15 Interrupt on Queue Entry Available (IQEA):

This bit is set by the host to request an IQEA. The interrupt is generated either when the queue is half empty or as soon as one entry is available, depending upon the state of the IQHE bit. The board clears this bit prior to generating the IQEA interrupt. After the host sets this bit, requesting an interrupt, it cannot change any of the other bits in the IQAR.

Queue Head Pointer (QHP)

The *QHP* provides a convenient place for the host to store the address of the next available entry in the Command Queue. The board will neither read nor write the QHP.

Thaw Work Queue Register (TWQR)

This field is used to restart a work queue that has been frozen due to a SCSI Pass-Through error or a SCSI bus reset when these options are enabled. A queue is thawed by writing the appropriate work queue number to the designated bits in the upper byte of the register and then setting the Thaw Work Queue bit (TWQ). An extension is defined to the Thaw Work Queue Register that allows work queues to be numbered from 1 to 255 for Cougar II Wide. Refer to Chapter 6, *Error Recovery Tools*, page 6-1, for additional information.

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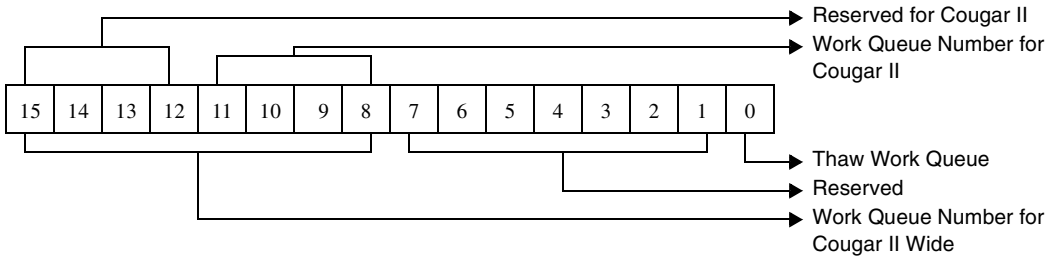


Figure 3-5. Thaw Work Queue Register

Bit 0 Thaw Work Queue (TWQ):

Setting this bit causes the board to resume execution of commands in the work queue specified in the upper byte of this word. The board then clears the TWQ bit to acknowledge that the queue has been thawed.

Bits 1-7 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bits 8-15 Work Queue Number for Cougar II Wide,
Bits 8-11 Work Queue Number for Cougar II:

This field specifies the work queue number to be thawed. Values range from 1 to 14 for Cougar II, and 1 to 255 for Cougar II Wide. It is an error to thaw work queue 0.

Bits 12-15 Reserved for Cougar II:

These bits are reserved for the Cougar II and must be cleared to 0 by the host.

Master Command Entry (MCE)

The *Master Command Entry* (MCE) is an auto-initialized facility through which commands are issued to the board before the Command Queue and work queues have been initialized. The single slot of the MCE has the same 12-byte format as any on-board Command Queue entry. Space must be reserved in the Host Usable Space (HUS) portion for the I/O Parameter Block (IOPB) that is pointed to by the MCE. Typically, it will be used only when initializing the Command Queue. It does, however, provide a mechanism to issue a command to the board even if the Command Queue and all work queues are full. It provides a way to get one command into the board even when the Command Queue is *locked up*.

Command Queue

The *Command Queue* (CQ) consists of a user-programmed number of Command Queue entries. The host sets the size of the Command Queue when via the Initialize Controller command. Each Command

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Queue entry includes all of the information needed for the board to find, execute and respond to the commands contained in the IOPB. The actual size of the Command Queue equals the number of entries times 12 bytes. The Command Queue must have at least one entry.

The Command Queue is circular, and it is up to the host to keep track of the next Command Queue entry that it can use. Because the queue is circular, the board infers chronological ordering of commands. Each Command Queue entry is *busy* only until the board can transfer the command to a work queue and then free its slot in the Command Queue.

Command Queue Entry (CQE)

A Command Queue entry is a 12-byte block containing all of the information needed for the host to find and execute a command. Each CQE is *busy* only until the board can transfer the command to a work queue and free the entry by clearing the Go/Busy bit. This mechanism allows a relatively small Command Queue to handle a large number of commands.

The purpose of the fields in a CQE will vary depending on whether onboard or offboard IOPBs are being used. shows the format of the two types of Command Queue entries.

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COMMAND QUEUE ENTRY FOR ONBOARD IOPBs:

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	QUEUE ENTRY CONTROL REGISTER															
0x1	IOPB ADDRESS															
0x2	COMMAND TAG															
0x3	COMMAND TAG															
0x4	IOPB LENGTH								WORK QUEUE NUMBER							
0x5	RESERVED															

COMMAND QUEUE ENTRY FOR OFFBOARD IOPBs:

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	QUEUE ENTRY CONTROL REGISTER															
0X1	RSRV				TT		MT		ADDRESS MODIFIER							
0X2	HOST ADDRESS (MSW)															
0X3	HOST ADDRESS (LSW)															
0X4	IOPB LENGTH								WORK QUEUE NUMBER							
0X5	RESERVED															

Figure 3-6. Command Queue Entry Format For Onboard And Offboard IOPBs and MCE

CQE Word 0: Queue Entry Control Register

The Queue Entry Control Register (QECR):

- Kicks off command execution.
- Acknowledges a command abort sequence.
- Flags a high priority command.
- Signals whether a command is located Short I/O or system memory.

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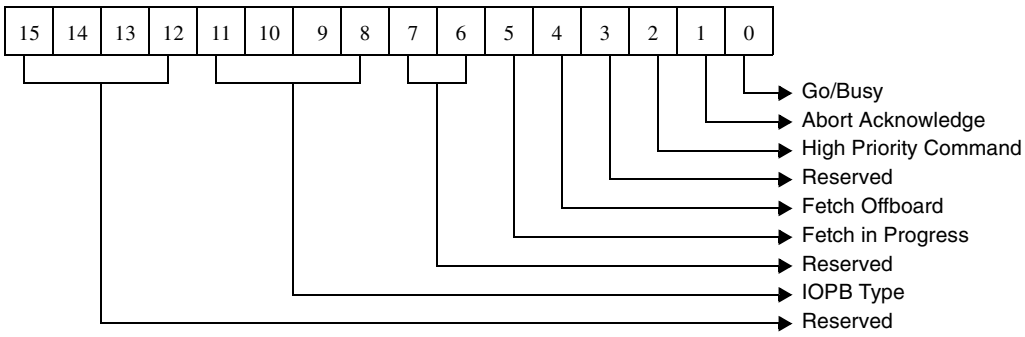


Figure 3-7. Queue Entry Control Register (QECR)

Bit 0 Go/Busy (GO):

The GO bit is set by the host to initiate action on a CQE. The host must assemble the IOPB in the Host Usable Space (HUS) and the CQE in the Command Queue before it sets this bit. When the GO bit is set, the board moves the CQE and IOPB into internal memory and clears the GO bit, releasing the CQE.

Bit 1 Abort Acknowledge (AA):

When a command completes with a SCSI Pass-Through error, all commands in, and destined for, that work queue can optionally be aborted. This option is specified when the work queue is initialized (see Chapter 5, Initialize Work Queue command).

The AA bit is used to end the command abort sequence, allowing the host to reissue the command that completed with error, and allowing commands that were aborted due to the error. The host issues the command that completed with error, after appropriate error recovery, with the AA bit set. Subsequent commands should be submitted with the AA bit cleared, and normal queue operation will resume until another Pass-Through error occurs.

Bit 2 High Priority Command (HPC):

The **HPC** bit flags a command so that the board places the command at the top of its work queue. If there are other commands in the work queue with the HPC bit set, the new command is queued up behind the other HPC.

Bit 3 Reserved (RSRV):

This bit is reserved and must be cleared to 0 by the host.

Bit 4 Fetch Offboard (FOB):

This bit is only used in applications involving offboard IOPBs. If this bit is set, then the corresponding IOPB will be fetched from the host memory. The only other bit in the Queue Entry Control Register that is valid when the FOB bit is set is the Go/Busy bit (Bit 0). For a discussion of

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offboard IOPBs, refer to Chapter 6, Offboard IOPBs, page 6-17.

Bits 5 Fetch In Progress:

This bit is for internal board use only.

Bits 6-7 (RSRV) Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bits 8-11 IOPB Type:

These bits describe the IOPB type. The board supports only type zero IOPBs, so this field should be cleared to 0.

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be cleared to 0 by the host.

CQE Word 1:

For onboard IOPBs, CQE Word 1 is used to store the IOPB Address. For offboard IOPBs, it holds the memory type, transfer type, and address modifier used by the board to DMA the offboard IOPB into onboard memory.

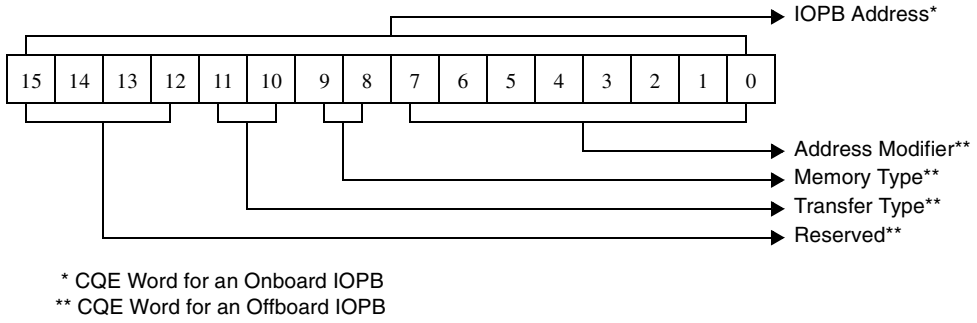


Figure 3-8. CQE Word for Onboard and Offboard IOPBs

IOPB Address

For an onboard IOPB, CQE Word 1 points to the location of the IOPB in Short I/O. The value is specified as an offset from the Short I/O base address. The board transfers the CQE and IOPB out of Short I/O when the host sets the Go/Busy bit.

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Memory Type/Transfer Type/Address Modifier

For an offboard IOPB, CQE Word 1 is used to specify the memory type, transfer type, and address modifier used to transfer the IOPB onboard ().

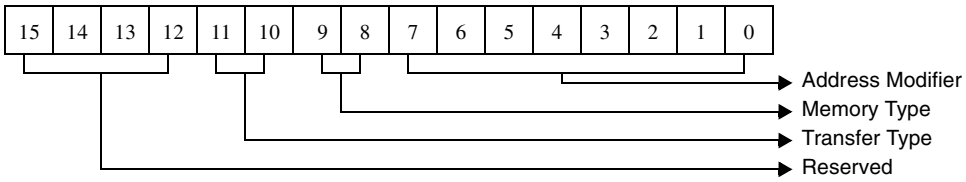


Figure 3-9. Memory Type/Transfer Type/Address Modifier

CQE Words 2-3:

For onboard IOPBs, CQE Word 2 is used to store a host-assigned command tag. For offboard IOPBs, it holds the physical address of the offboard CQE/IOPB.

Command Tag

For onboard IOPBs, Command Queue Entry Words 2-3 may be used to store a host-specified command tag. The board does not use or modify this field and returns the Command Tag as part of the Command Response. In a typical implementation, the host would use a unique value Command Tag for each operation to differentiate one command from another.

Host Address

For offboard IOPBs, CQE Words 2-3 are used to store the physical address in host memory of the offboard CQE/IOPB. Word 2 stores the most significant word of the address, and Word 3 stores the least significant word.

CQE Word 4: Work Queue Number and IOPB Length

CQE Word 4 consists of a Work Queue Number field and an IOPB Length field.

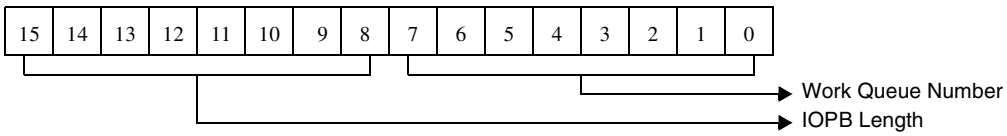


Figure 3-10. IOPB Length/Work Queue Number

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Bits 0-3 Work Queue Number:

This byte contains the number of the work queue in which to place the command in. Since the Cougar II supports 14 work queues, valid entries in this field are 0x0 to 0xE.

Cougar II Wide supports 255 work queues, plus work queue 0. Valid entries are 0x0 to 0xFF.

NOTE: Work Queues other than work queue 0 must be initialized via the Initialize Work Queue command before use. If the specified work queue has not been initialized, the command will return a Queue Uninitialized error.

Bits 4-7 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bits 8-15 IOPB Length:

The IOPB Length byte specifies the length in **words** of the IOPB to which the CQE is pointing. For onboard IOPBs, writing a 0 to this field indicates that the default length of the IOPB is being used.

NOTE: This field should only contain a non-zero value if the IOPB involves a user-defined SCSI command (Group 6 or 7). Refer to Chapter 5, SCSI Pass-Through IOPB, (page) for additional information.

CQE Word 5: Reserved

CQE Word 5 is reserved for both onboard and offboard IOPBs. This field should be cleared to 0 by the host.

Host Usable Space (HUS)

The *Host Usable Space* (HUS), typically used to pass the IOPB portion of a command, is freeform memory space accessible to both the host and the controller. No partitioning of the HUS is implied or required by the MACSI interface and the manner in which it is used is totally under the control of the host. In some multiprocessing applications, the HUS is a convenient place to post semaphores between CPUs.

The amount of HUS available is determined by three factors:

1.The size of the Short I/O

2.The number of Command Queue entries defined when the Command Queue is initialized

3.The length of the Command Response Block that is defined.

For example, the default 2K Short I/O space the Command Queue is initialized with ten entries (each Command Queue entry is 12 bytes long), and a Command Response Block of 76 bytes is defined, there will be 1704 bytes of HUS available. The Master Control/Status Block, Master Command Entry, and the Controller Specific Space always occupy a total of 148 bytes.

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Command Response Block (CRB)

The *Command Response Block* (CRB) is used by the board to post command completion status. The IOPB and related status information are returned in the CRB. The CRB is also used to return an error status block in the event of a controller interrupt. In addition, if enabled to do so, the board uses the CRB to signal a number of special conditions. See *Command Response Status Word* for details.

The CRB is made up of the:

- Command Response Status Word (CRSW)
- Command Tag
- Work Queue Number
- Returned IOPB.

The offset of the Command Response Block is defined when the controller is initialized using the Initialize Controller command (page). The length of the Command Response Block can be determined by subtracting the Command Response Block offset from the offset of the Controller Specific Space (+0x788). However, the length of the Command Response Block must be equal to the largest IOPB defined plus 12 bytes.

NOTE: If SCSI Autosense Error Recovery is to be enabled, additional space must be allocated in the CRB offset for the sense data. The sense data, if any, will be reported in the Returned IOPB of the SCSI command that caused the error. See Chapter 6, *Autosense Recovery*, page for more information.

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Table 3-3. Command Response Block (Sample Memory Map)

Offset From Short I/O Base Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x750	COMMAND RESPONSE STATUS WORD															
+0x752	RESERVED															
+0x754	COMMAND TAG															
+0x756	COMMAND TAG															
+0x758	IOPB LENGTH								WORK QUEUE NUMBER							
+0x75A	RESERVED															
+0x75C To +0x787	RETURNED IOPB															

NOTE: The above is the memory map of the Command Response Block (CRB) if the CRB offset has been set to +0x750 using the Initialize Controller command. With this setup, the maximum IOPB length is that of a SCSI Pass-Through IOPB used to issue a 12-byte SCSI command (i.e. maximum IOPB length = 44 bytes).

Command Response Status Word (CRSW)

The *Command Response Status Word* (CRSW) is the first word in the Command Response Block (CRB) and describes the nature of the Command Response. It also contains a handshake bit, the Command Response Block Valid/Clear Interrupt (CRBV) bit. The CRBV bit synchronizes the command interaction of the board and the host. shows the definition of the CRSW bits.

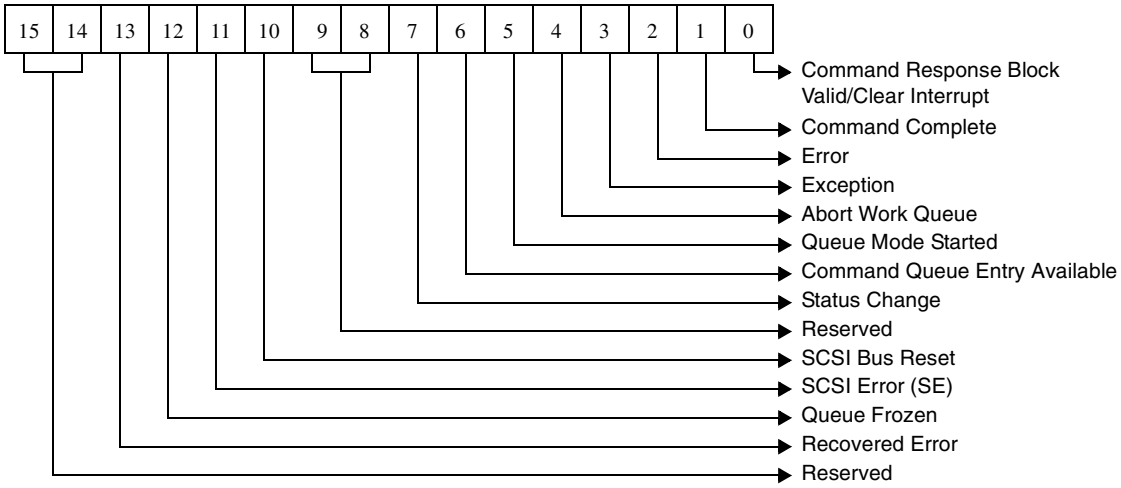


Figure 3-11. Command Response Status Word (CRSW)

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Bit 0 Command Response Block Valid/Clear Interrupt (CRBV):

The Command Response Block Valid/Clear Interrupt (CRBV) bit is set by the board after it loads the returned IOPB, the Work Queue Number, and the Command Tag into the Command Response Block (CRB). It remains set until cleared by the host.

The CRBV bit is also an Interrupt Pending bit because the board sets it immediately prior to issuing a Command Complete interrupt to the host. The board keeps the CRB stable while this bit is set.

After finishing with the information in the CRB, the host clears the interrupt by clearing the CRBV bit. Once this bit is cleared, the board can use the CRB to present the next command response.

Bit 1 Command Complete (CC):

The Command Complete (CC) bit is set by the board when the CRB contains the response to a command Completion, as opposed to a Queue Entry Available or Start Queue Mode started condition. The CC bit is set even when the command is completed with error or exception.

Bit 2 Error (ER):

The Error (ER) bit is set by the board when the CRB contains an IOPB that has completed with an error status. Examples of conditions that may cause an IOPB to complete with the Error bit set include:

- An incorrectly specified parameter which causes the board to misinterpret the command
- An invalid address leading to bus errors or timeouts
- A faulty device which causes a timeout

A Pass-Through command that returns any value other than zero in the Pass-Back Return Status.

The ER bit is valid only when Command Complete is set.

Bit 3 Exception (EX):

The Exception (EX) bit is set by the board when the CRB contains an IOPB that has completed with an exception.

A command completed with exception is one which completed without error, but has some IOPB parameter that has not been completely satisfied.

EXAMPLE: The board completes a Pass-Through SCSI command without transferring all of the data specified in the IOPB's transfer count field (for many SCSI commands, this is not an error condition, but rather something about which the host probably needs to be notified).

The EX bit is valid only when Command Complete is set.

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Bit 4 Abort Work Queue (AQ):

When work queues are initialized by the host, they can be set up, optionally, so that all of the commands in the queue can be aborted after a SCSI Pass-Through command completes with an error (see Initialize Work Queue Command, Chapter 5). The command that completed with an error is reported just like any other error, with the ER bit set in the CRSW.

With the Abort on Error option enabled, all commands following a command that completes with a SCSI Pass-Through error will be aborted. All commands in the Command Queue destined for that work queue will be aborted until a command with the Abort Acknowledge bit set in the QECR is encountered (see Queue Entry Control Register, page). All of the aborted commands are reported in the CRB with the CC, ER, and AWQ bits set. The Error Interrupt Vector of the command being aborted will be used to report this condition.

Bit 5 Queue Mode Started (QMS):

This bit indicates whether the board is in Queue Mode. The board sets this bit to 1 to indicate normal Queued IOPB operation.

The 4220 supports the Start Queue Mode bit to provide backward compatibility with the V/SCSI 4210 Jaguar. It is not needed by the Cougar to start executing queued IOPBs.

Bit 6 Command Queue Entry Available (CQA):

The Command Queue Entry Available (CQA) bit is set by the board when the CRB is presented in response to a Queue Entry Available condition. The CQA bit is mutually exclusive with the CC bit.

Bit 7 Status Change (SC):

This bit is set to indicate a condition such as:

- A printer status change has occurred.
- A device has connected for which no IOPB exists (IOPB type error).
- An IOPB has timed out.
- A device is requesting more data to be transferred than the IOPB allows.
- A device is requesting a data transfer of the opposite direction specified by the IOPB's direction bit.

If the SC bit is set, the board will return an error status block without returning the IOPB that caused the error. For more information, refer to the sections on the Controller Error Interrupt and Vector in Chapter 6.

Bits 8-9 Reserved (RSRV):

These bits are reserved and are cleared by the board.

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Bit 10 SCSI Bus Reset:

This bit is set to indicate a SCSI Bus Reset has occurred, when the Interrupt on SCSI Bus Reset option is enabled.

Bit 11 SCSI Error (SE):

This bit is set by the board to report a non-recoverable SCSI error. In this condition, the SCSI control hardware on the 4220 should be assumed to be in an unknown (but not desirable) condition, and will require a SCSI bus reset to return to a functional state. (See Appendix C).

Bit 12 Queue Frozen:

This bit is set by the board to indicate that a queue frozen status is being reported. This option is enabled via the Initialize Work Queue command. The Command Tag field will be cleared to zeros and the Work Queue Number field will contain the number of work queues being frozen. The CRSW is extended to provide for post back of queue frozen status. If enabled via the Initialize Work Queue command, this option allows the controller to report work queue status for the more than 15 work queues. When a command is returned with a SCSI error that causes a work queue to freeze, the queue frozen bit will be set in the Command Response Status Word:

Bit 13 Recovered Error:

When this bit is set, along with CC and CRBV, the command has completed in a recovered error state. The device completed the SCSI command with a check condition, an automatic SCSI request sense has been issued, and the resulting sense data has been returned in the CRB. This condition will be reported through the Error Completion Vector set in the IOPB for the command.

Bits 14-15 Reserved (RSRV):

These bits are reserved and are cleared to 0 by the board.

Command Tag

This Command Tag is the same 4-byte value that was provided in the Command Queue Entry when this command was originally issued to the board. The board does not use or modify the Command Tag. It simply returns the Command Tag as part of the Command Response. The Command Tag may be used by the host to determine to which command the board is responding.

IOPB Length Work Queue Number

The lower byte of this word specifies the number of the work queue to which the command was issued. The upper byte specifies the length of the returned IOPB. A length of zero indicates the IOPB is the default length. The entire IOPB Length/Work Queue Number word is returned from the Command Queue entry exactly as it was originally entered by the host.

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Returned IOPB

The Returned IOPB field of the Command Response Block is usually an image of the IOPB that was passed with the Command Queue Entry when the command was originally issued to the board.

In some cases, depending upon the specific IOPB, some of the parameters are modified to reflect Command Completion status or other information such as the maximum Transfer Length and the SCSI sense bytes if SCSI Autosense Error Recovery is enabled (see pages and).

The returned IOPB area is undefined for a response to a Queue Entry Available condition or for any other command response where the original command did not require an IOPB.

Controller Specific Space

The Controller Specific Space is a 120-byte space used by the board to post the Configuration Status Block (CSB). The board uses the 120-byte Controller Specific Space to post the Configuration Status Block. This space begins at an offset of +0x788 from the Short I/O base address (default Short I/O size of 2K bytes). shows a typical 2K Short I/O memory map.

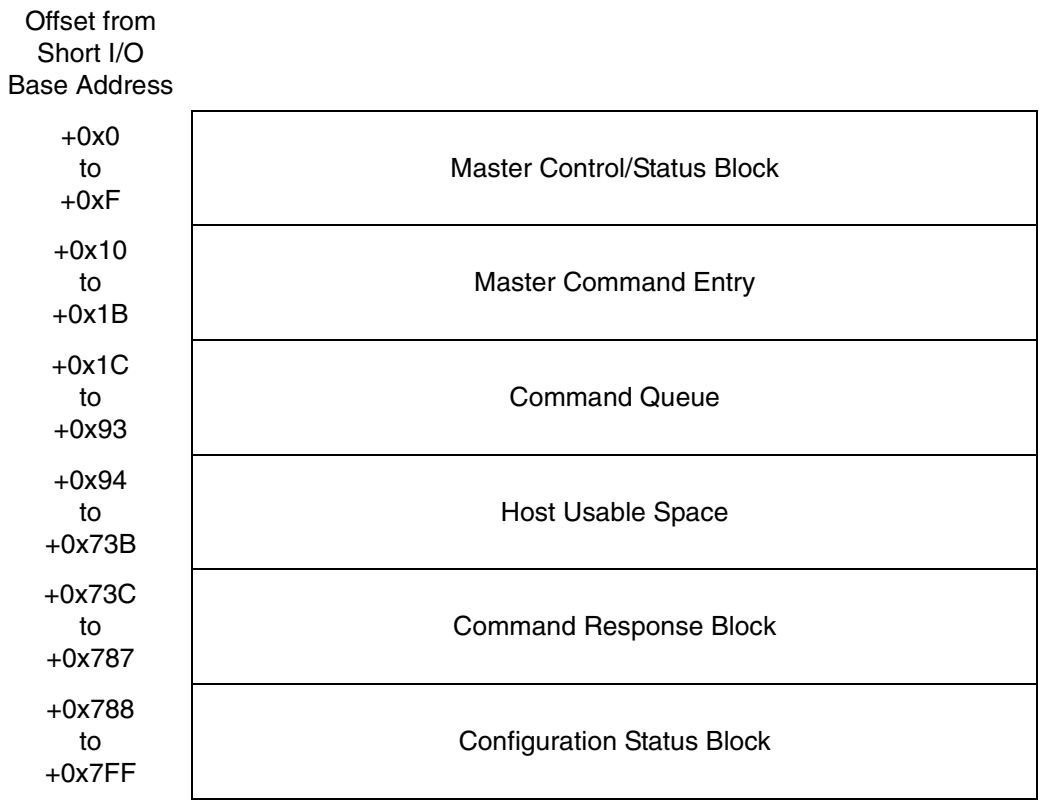


Figure 3-12. Typical Memory Map of 2K Short I/O Space

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Configuration Status Block (CSB)

The board uses the CSB to report its current configuration. This includes such information as the product code, firmware revision information, memory configuration, SCSI ID, jumper settings, SCSI synchronous negotiation rate, and Frozen Work Queues. CSS begins 120 bytes before the end of the Short I/O. The CSB values are valid after completion of a controller rest. The format of the CSB is shown in.

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OFFSET	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0x788	BOARD IDENTIFICATION															
+0x78A	EXTENDED BOARD ID								PRODUCT CODE							
+0x78C	PRODUCT CODE															
+0x78E	RESERVED															
+0x790	RESERVED								VARIATION							
+0x792	RESERVED															
+0x794	RESERVED								FIRMWARE REVISION LEVEL							
+0x796	FIRMWARE REVISION LEVEL															
+0x798	RESERVED															
+0x79A To +0x7A1	FIRMWARE RELEASE DATE															
+0x7A2	SIZE OF CPU RAM															
+0x7A4	SIZE OF DATA BUFFER															
+0x7A6	AVAILABLE WORK QUEUES															
+0x7A8	PRIMARY FRONT END CHANNEL ID								SECONDARY FRONT END CHANNEL ID							
+0x7AA	PRIMARY SCSI BUS ID								SECONDARY SCSI BUS ID							
+0x7AC	LAST PRIMARY DEVICE SELECTED								LAST SECONDARY DEVICE SELECTED							
+0x7AE	PRIMARY PHASE SENSE								SEC. PHASE SENSE/PRINT STATUS							
+0x7B0	RESERVED					EDCID **			DAUGHTER CARD ID							
+0x7B2	RESERVED								SOFTWARE JUMPER SETTINGS							
+0x7B4	PRIMARY DEVICE SYNC. NEGOTIATION RATE								SECONDARY DEVICE SYNC. NEGOTIATION RATE							
+0x7B6	FROZEN WORK QUEUES REGISTERS															
+0x7B8	RESERVED															
+0x7BA	RESERVED															
+0x7BC	RESERVED															

*EDCID = Extended Daughter Card ID

Figure 3-13. Configuration Status Block

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A description of the values found in the Configuration Status Block follows:

Board Identification (2 bytes):

The contents of this field is the value 0x4220, indicating to the host the presence of a Cougar II.

Extended Board ID (1 byte):

The hex code contents of this field indicate the revision control for board identification. 0x0 identifies the board as a Cougar I, 0x1 is reserved, and 0x2 identifies the board as a Cougar II.

Product Code (3 bytes):

The Interphase product code. This value is represented as a 3-character ASCII string. The most significant character appears first.

Product Variation (1 byte):

The Interphase product variation code. This value is represented as one ASCII character.

Firmware Revision Level (3 bytes):

The revision level of the installed firmware. This value is represented as a 3-character ASCII string. The most significant character appears first.

Firmware Release Date (8 bytes):

The release date of the installed firmware. This value is represented as an 8-character ASCII string in the format, MMDDYYYY. A January 15, 1995 release date would be 01151995.

Size of CPU RAM (2 bytes):

The amount of on-board CPU RAM expressed in 1K increments. This value is represented as a four-digit hexadecimal number.

Size of Data Buffer (2 bytes):

The amount of on-board data buffer RAM expressed in 1K increments. This value is represented as a four-digit hexadecimal number. For example, a 128K RAM data buffer would be 0x0080.

Available Work Queues:

The number of work queues available. With less than 256K of RAM the maximum number of work queues is 15. With 256K, or greater, of RAM the maximum number of work queues is 256. The only values reported are either 0xF or 0xFF.

Primary Front End Channel ID (1 byte):

The type of primary front end channel. lists the possible values.

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Table 3-4. Front End Channel Types Returned in the CSB

ID Number	Front End Channel Type
0x0	Single-ended Cougar II
0x1	Differential Cougar II
0x2	Single-ended Cougar II Wide
0x3	Differential Cougar II Wide
0x7	Printer
0xE	Differential Cougar II with RAID memory**

** This option requires customer-specific proprietary hardware

Secondary Front End Channel ID (1 byte):

This 1-byte hexadecimal value represents the secondary front-end channel type. Values are shown in.

Primary SCSI Bus ID (1 byte):

The current SCSI ID for the primary SCSI bus. This value is represented as a 1-byte hexadecimal number. This value will default to the SCSI ID encoded in the on-board switches at the completion of a reset. This value will be updated at the completion of an Initialize Controller command.

Secondary SCSI Bus ID (1 byte):

This 1-byte hexadecimal value is the current SCSI ID for the secondary SCSI bus. It defaults to the SCSI ID encoded in the jumpers on the SCSI daughter card at the completion of an Initialize Controller command.

Last Primary Device Selected (1 byte):

Contains the SCSI ID of the last primary SCSI bus device selected by the board. This field is updated every time the board selects or is reselected by a device on Channel 0.

Last Secondary Device Selected (1 byte):

Contains the SCSI ID of the last secondary bus device selected by the board. This field is updated every time the board selects or is reselected by a device on Channel 1.

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Primary Phase Sense (1 byte):

Contains the status of the primary SCSI bus. The primary phase sense register contains a copy of the phase sense register of the SCSI controller chip. This copy is updated on every SCSI interrupt. The signals in the register are shown in.

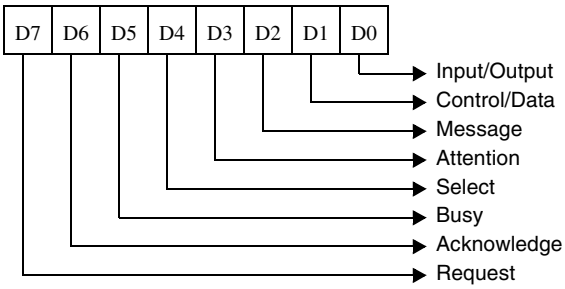


Figure 3-14. SCSI Bus Status Byte

Each of the above bits corresponds to a signal on the SCSI bus. If the bit is set, the corresponding SCSI signal is active. shows the meaning of the signals.

Table 3-5. Meaning of SCSI Signals in the Phase Sense Byte

SIGNAL	NAME	DESCRIPTION
REQ	Request	The target asserts REQ to start an asynchronous bus transfer.
ACK	Acknowledge	The initiator asserts ACK to indicate that it has sent (or received) data. This signal is used in tandem with REQ to handle all asynchronous data transfers.
BSY	Busy	This signal is driven by the initiator or target using the bus to indicate that the bus is busy.
SEL	Select	The initiator asserts SEL to indicate which target is to perform an upcoming operation. The ID of the target is simultaneously sent over the data lines. The target asserts SEL to reconnect during the Reselection phase.
ATN	Attention	The initiator asserts ATN to tell the target that there is a message waiting for it.
MSG	Message	The target drives this signal when it is transferring a message (as opposed to data).
C/D	Control/Data	The target uses this signal to indicate the type of information on the bus (asserted = command/message, negated = data).
I/O	Input/Output	The target drives this signal to control the direction in which data is moving on the bus (asserted = target-to-initiator transfer, negated = initiator-to-target transfer).

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For a complete description of the signals, please refer to the SCSI specification.

Secondary Phase Sense/Printer Status (1 byte):

If the board has a SCSI daughter card, this byte shows the status of the secondary SCSI bus and the format is the same as for the SCSI Bus Status Byte in If using a printer daughter card, this byte shows the status of the printer, and this register contains the printer status. This register will be updated at the completion of any print command or approximately every 27 to 35msec. The bit definition of this register is dependent on whether the interface is Dataproducts or Centronics type. The format of this register may be seen in.

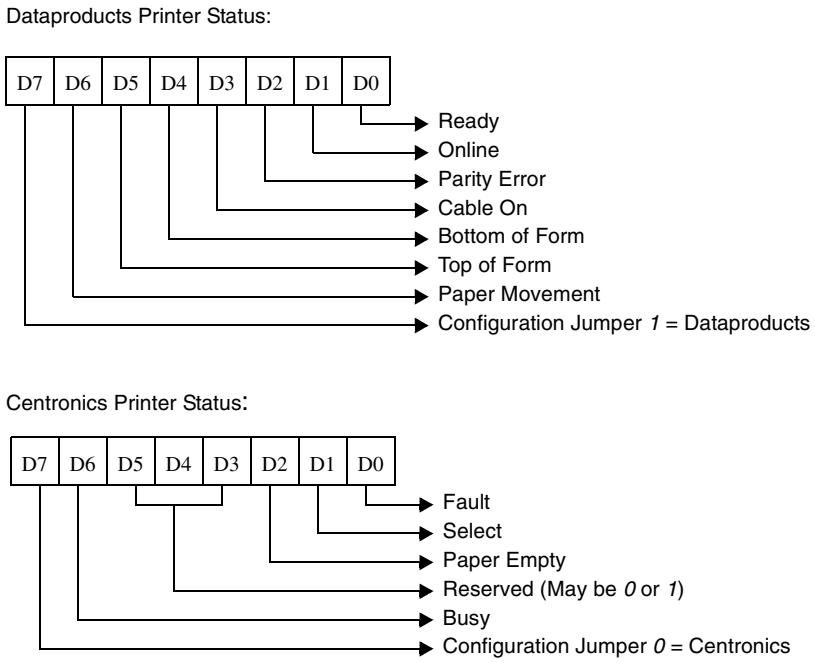


Figure 3-15. Printer Status Register

Extended Daughter Card ID (3 bits):

The *Extended Daughter Card ID* field may provide additional information about the optional daughter card. The values that appear in this field are shown in.

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Table 3-6. Extended Daughter Card ID

CODE	DESCRIPTION
0x0	No Daughter Card Present, or Unknown Daughter Card
0x1	Single-Ended Daughter Card
0x2	Differential Daughter Card
0x3 to 0x7	RESERVED

Daughter Card ID (1 byte):

The *Daughter Card ID* field indicates the type of optional daughter board installed. The meaning of the codes is shown in.

Table 3-7. Daughter Card ID

CODE	DESCRIPTION
0x7	No Daughter Card
0x6	SCSI Daughter Card
0x5	Reserved
0x4	Printer Daughter Card
0x3 to 0x0	Reserved

Software Jumper Settings (1 byte):

Reports the status of options enabled via jumper settings. The configurations reported in this field are shown in.

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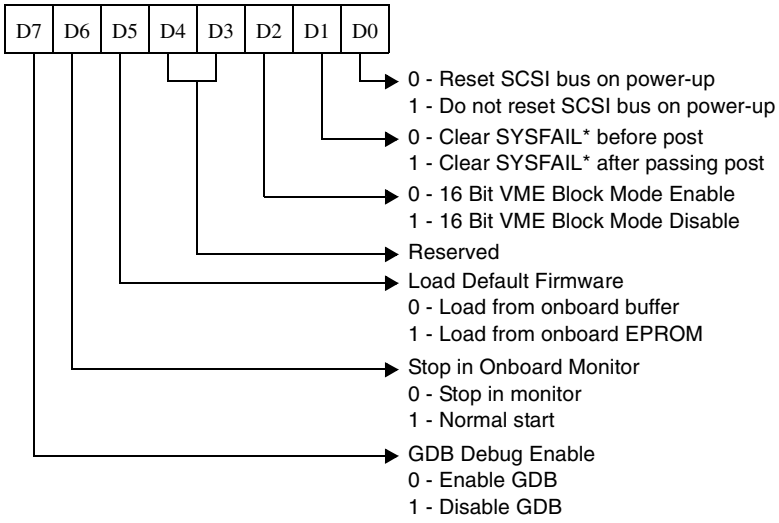


Figure 3-16. Software Configuration Jumper Settings Reported In Configuration Status Block

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Primary Device Synchronous Rate (1 Byte):

Provides synchronous negotiation rate in the CSS and a convenient way to determine the negotiated synchronous transfer rate for arbitrary SCSI devices. This field has the structure shown in.

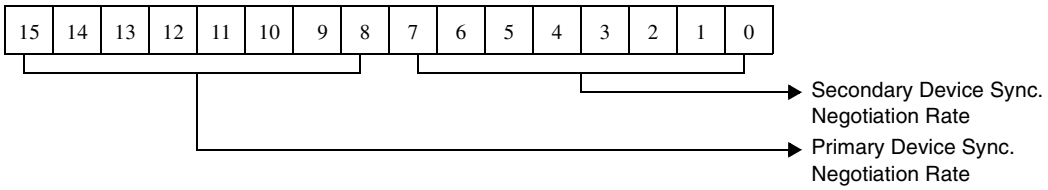


Figure 3-17. Synchronous Negotiation Rate

This value represents the request-request period, but is divided by four (as per SCSI specifications) to fit in a single byte. The board supports the values shown in.

Table 3-8. SCSI Device Synchronous Negotiation Rates

CONTENTS OF TRANSFER PERIOD FIELD		REQUEST-REQUEST PERIOD (Value x 4 NANOSEC = Request Period)	SYNCHRONOUS RATE (MBytes/Seconds)
HEX	DEC		
00	00	N/A	Asynchronous
19	25	100	10.0
1e	30	120	8.3
23	35	140	7.1
28	40	160	6.3
2d	45	180	5.6
32	50	200	5.0
37	55	220	4.5
3a	60	240	4.2
46	70	280	3.6
50	80	320	3.1
5a	90	330	2.8
64	100	400	2.5
6e	110	440	2.3

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Frozen Work Queues:

This register provides Frozen Work Queue status for work queues 1-15 (). Work Queues 16-255 are reported only through the CRSW (bit 12 Queue Frozen). Work Queues 16-255 will only be reported in the CRSW provided the option is enabled via the Initialize Work Queue command.

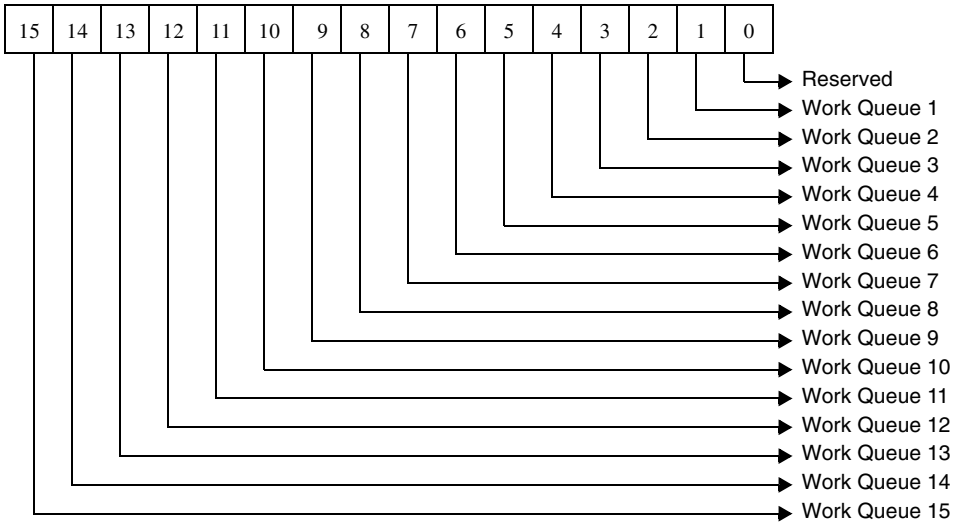


Figure 3-18. Frozen Work Queues Register (Work Queues 1-15)

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Issuing Commands to the Controller

The board supports two distinct types of IOPBs:

1. **SCSI IOPBs**: Commands sent to either the attached SCSI devices or to the printer port (if used) and issued through the Command Queue to a specific work queue.

2. **Control IOPBs**: Commands for the board itself, such as initialization commands, that result in local board action only. In general, control IOPBs are issued through the Master Command Entry to Work Queue 0.

Both the Master Command Entry and Command Queue entry are 12-byte blocks with the same format. The Go/Busy bit is a semaphore reflecting ownership of the Command Queue entry. Once the host sets the Go/Busy bit, the board owns the entry. The host must not modify the entry until the board clears the Go/Busy bit. The board clears the bit to indicate that the space is available to accept another command from the host.

Commands issued through the Master Command Entry (MCE) have precedence over those issued through the Command Queue. In general, the MCE is used to get the board up and running. The Command Queue is then used to handle the SCSI bus and, if the optional printer port is installed, printer operations. It should not be necessary to use the MCE again until there is a "break" in normal operations, such as a SCSI device error.

Notes On The Master Command Entry & Work Queue 0

In order to initialize the board, as well as to execute high priority commands, the board provides two auto-initialized facilities: the Master Command Entry (MCE) and Work Queue 0.

The MCE, a 12-byte structure, has exactly the same form as a Command Queue entry (i.e. control information and a pointer to an IOPB). It acts like a single-entry Command Queue.

The Cougar II accommodates up to 14 work queues and the Cougar II Wide up to 255 work queues. This is not counting a special queue called *Work Queue 0*. Work queue 0 is intended for issuing special commands such as initialize controller or error recovery, etc. Cougar II Wide supports up to 255 work queues, numbered 0 through 255. Work queues are intended to be dedicated to a specific SCSI device. Multiple work queues may be dedicated to the same device. The host sets the parameters of each work queue when it initializes the queue.

Work Queue 0 is the highest priority work queue, so any command sent to Work Queue 0 is executed immediately. Work Queue has a length of 1, so that only one high priority process can occur at a time. However, it is possible that a command from Work Queue 0 may require error recovery. To deal with this situation, certain commands (specifically, SCSI Bus Reset and Flush Work Queue) may always be issued through Work Queue 0. For all other commands, Work Queue 0 has a length of 1.

The MCE and Work Queue 0 allow the issuing of a single command then waiting for its completion before issuing the next one. A typical use for these facilities is, upon power-up, to initialize the rest of the work queues and begin normal SCSI operation.

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Note that the MCE and Work Queue 0 remain available for use even after the Command Queue and the other work queues are initialized and normal activity has begun, so that error recovery command may be issued through this mechanism.

Issuing A Command Via The Master Command Entry

The following is a summary of the sequence of events that need to take place in order to issue commands through the MCE:

- The host builds an IOPB for the command in Host Usable Space.
- The host fills in the Master Command Entry.
- The board copies command-related information from the IOPB into Work Queue 0.
- The board executes the command.
- The board writes the IOPB and command completion information to the Command Response Block. This returned IOPB contains command completion status, as well as information to enable the host to identify which command has completed.
- The board posts completion to the host by setting the Command Response Block Valid bit (bit 0) in the Command Response Status Word in the Command Response Block and optionally generating an interrupt.
- The host acknowledges the command's completion by clearing the Command Response Status Word. This frees the Command Response Block to receive information concerning the next completed command.

Notes On The Command Queue

The Command Queue is circular, and it is up to the host to keep track of the next Command Queue entry it can use. Because the queue is circular, the board infers chronological ordering of commands. Each Command Queue entry is "busy" only until the board can transfer the command to a work queue and free its slot in the Command Queue.

In the unlikely case that the Command Queue is full when the host tries to enter a command, the board provides an option to the host when an entry Command Queue becomes available (refer to *Interrupt on Queue Available Register*, page).

Issuing Commands Through The Command Queue

The standard procedure for issuing commands through the Command Queue is to write Command Queue entries and their corresponding IOPBs into the on-board shared memory space.

The host builds an IOPB for the desired command in Host Usable Space and then creates an entry in the next available slot in the Command Queue.

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When the host sets the Go/Busy bit in the QECR, an internal interrupt is generated to notify the board that the CQE is ready to be processed. The board also watches for the next available command by polling the CQE pointed to by the current Command Queue pointer.

The board copies the CQE and its corresponding IOPB into the appropriate internal work queue and clears the Go/Busy bit, freeing up that slot in the Command Queue for reuse by the host.

Commands issued through the Command Queue are executed in the same order issued, unless designated as high priority.

The board writes the Returned IOPB and command response into the CRB. The Returned IOPB contains command completion status, as well as information to enable the host to identify which command has completed. The board posts completion to the host by setting the CRBV bit in the CRSW of the CRB and optionally generating an interrupt.

The host acknowledges the command completion by clearing the CRBV Bit in the CRSW. This frees up the CRB to receive information concerning the next completed command.

Notes On Work Queue Usage

Work Queue 0 has a length of 1, so that only one error recovery process can occur at a time. However, it is possible that a command from Work Queue 0 may require error recovery. To deal with this situation, certain commands (specifically, SCSI Bus Reset and Flush Work Queue) may always be issued through Work Queue 0. For all other commands, Work Queue 0 has a length of 1.

SCSI Data Transfers

The SCSI Pass-Through command is used to issue all SCSI device commands except SCSI Reset. When the host builds an IOPB for the command, it provides all of the information the board needs to send a command to a specific SCSI peripheral.

The size of the SCSI Pass-Through IOPB can be adjusted to accommodate different SCSI command lengths. For example, to issue a 12-byte SCSI command, append the 12-byte SCSI Command Descriptor Block starting at word 0x10 of the IOPB.

To determine the length of the SCSI command, the board examines the Group Code field in Byte 0 of the Command Descriptor Block (CDB). shows the possible entries in this field:

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Table 3-9. Group Codes For SCSI Commands

GROUP	CDB LENGTH
0	6 bytes
1	10 bytes
2	10 bytes
3	(reserved)
4	(reserved)
5	12 bytes
6	User defined
7	User defined

If the command is a Group 0, 1, 2, or 5 SCSI command, the board will "know" the length of the Command Descriptor Block (6, 10, or 12 bytes, respectively) and the board will ignore the IOPB Length field of the corresponding Command Queue entry.

For a user-defined SCSI command (Group 6 or 7), the host must fill in the IOPB Length field of the corresponding Command Queue entry with the number of **words** in the IOPB. The board then calculates the CDB length by subtracting the overhead of the IOPB (0x10 words) from the length specified in the Command Queue entry (refer to Chapter 5, page 5-3 for details on the SCSI Pass-Through command).

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Chapter 4
VMEbus Interrupts

At the completion of a command (successful, terminated with an error, or an exception), the board notifies the host by generating a Command Complete interrupt on the VMEbus. The board can respond to the VMEbus Interrupt Acknowledge Cycle with different interrupt vectors, based on the cause of the interrupt. But for those VMEbus systems that allow only one interrupt vector per device, the host can still determine the source of the interrupt by checking the status bits in the Command Response Status Word and the Work Queue Number found in the Command Response Block.

The hardware driving the VMEbus interrupt line is cleared at the completion of the VMEbus Interrupt Acknowledge Cycle. However, a Clear Interrupt operation must also be executed by the host to notify the board that the interrupt has been properly serviced by the host and that the board may now post its next interrupt. The host does this by clearing the Command Response Block Valid/Clear Interrupt (CRBV) bit in the Command Response Block (see the CRBV bit in Chapter 3 for more information).

NOTE

> Any information that the host needs from the Command Response Block must be accessed before it clears the CRBV bit in the Command Response Status Word.

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Chapter 5
Command Set

Overview

Commands are issued to the controller using I/O Parameter Blocks (IOPBs). These fall into two basic groups: SCSI IOPBs, which are commands that are sent to the attached SCSI devices, and Control IOPBs, which result in local controller action only.

Table 5-1.V/SCSI-2 4220 Cougar II Command Set

SCSI IOPBs	COMMAND CODE	PAGE
SCSI Pass-Through	0x20	5-3
SCSI Reset	0x22	5-15
CONTROL IOPBs	**COMMAND CODE**	
Printer Port	0x23	5-19
Perform Diagnostics	0x40	5-27
Initialize Controller	0x41	5-30
Initialize Work Queue	0x42	5-50
Dump Initialization Parameters	0x43	5-57
Dump Work Queue Parameters	0x44	5-63
Bus Status Inquiry	0x45	5-67
Command Status Inquiry	0x46	5-72
Read/Write Buffer	0x47	5-77
Cancel Command Tag	0x48	5-84
Flush Work Queue	0x49	5-88
Initialize Printer Port	0x4A	5-93
Restart Controller	0x4B	5-98
Device Reinitialize	0x4C	5-101
Issue Bus Device Reset Message	0x4D	5-106
Issue Abort Message	0x4E	5-112
Download Firmware	0x4F	5-118
Set Serial Number	0x52	5-128
Buffer FIFO	0x53	5-133

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In general, **SCSI IOPBs** are issued to a specific device via its assigned work queue. Each work queue must be separately initialized before commands can be issued to it. **Control IOPBs** must be issued through the Master Command Entry to Work Queue 0. The SCSI Reset command can be issued to either a specific device or through the Master Command Entry. Refer to the individual command descriptions for details.

Commands are listed sequentially for easy reference.

NOTE

When issuing commands or otherwise interacting with the board via the MACSI interface, the host must clear all bits and fields marked "RESERVED" to 0. For performance reasons, the board does not execute a sanity check on all reserved fields. Clearing these reserved fields helps avoid driver problems that may otherwise occur when a later firmware implementation is released.

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SCSI PASS-THROUGH

Command ID: 0x20

The SCSI Pass-Through IOPB provides all of the information the board needs to send a command to a specific SCSI peripheral on either of the SCSI buses.

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x20)															
0x1	COMMAND OPTIONS															
0x2	RETURN STATUS															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6	RESERVED															
0x7	RESERVED				TT		MT		ADDRESS MODIFIER							
0x8	BUFFER ADDRESS (Or Scatter/Gather List Address)															
0x9																
0xA	MAXIMUM TRANSFER LENGTH (Or Scatter/Gather Element Count)															
0xB	**MAXIMUM TRANSFER LENGTH**															
0xC	RESERVED (Or Scatter/Gather Total Transfer length)															
0xD																
0xE	RESERVED															
0xF	UNIT ADDRESS															
0x10	SCSI BYTE 0 (or Sense Data Byte 0)								SCSI BYTE 1 (or Sense Data Byte 1)							
0x11	SCSI BYTE 2 (or Sense Data Byte 2)								SCSI BYTE 3 (or Sense Data Byte 3)							
0x12	SCSI BYTE 4 (or Sense Data Byte 4)								SCSI BYTE 5 (or Sense Data Byte 5)							
0x13	SCSI BYTE 6 (or Sense Data Byte 6)								SCSI BYTE 7 (or Sense Data Byte 7)							
0x14	SCSI BYTE 8 (or Sense Data Byte 8)								SCSI BYTE 9 (or Sense Data Byte 9)							
0x15	SCSI BYTE 10 (or Sense Data Byte 10)								SCSI BYTE 11 (or Sense Data Byte 11)							
0x16 : : 0x8f	(Additional Sense Data Bytes, if configured)															

NOTES: Fields set in bold letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-1. SCSI Pass-Through IOPB For 12-Byte SCSI Command

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SCSI PASS-THROUGH
Command ID: 0x20

The remainder of this section describes the function of each field in the SCSI Pass-Through IOPB.

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the SCSI Pass-Through command:

Command Code (2 Bytes)

This field must be set to 0x20 to execute the SCSI Pass-Through command.

Command Options (2 Bytes)

W This field contains the options for this command. The bits are defined as follows:

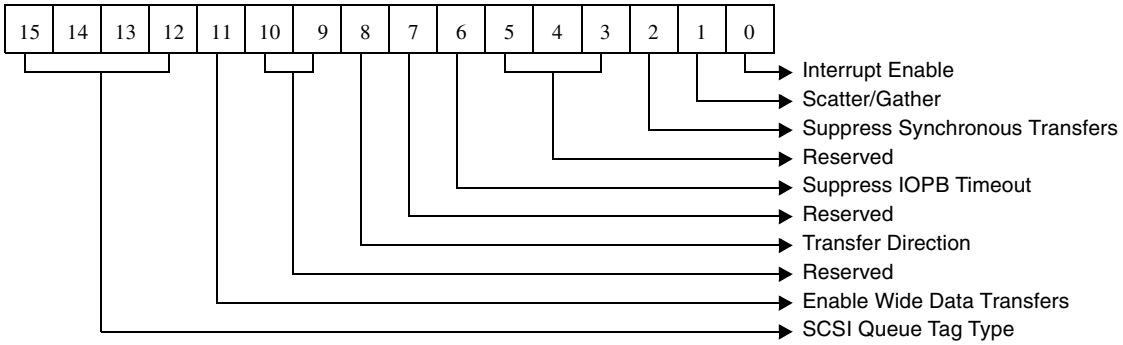


Figure 5-2. Command Options For SCSI Pass-Through Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bit 1 Scatter/Gather:

This bit should only be set if the command involves a scatter/gather operation. When scatter/gather is enabled, the following fields are defined differently than for non-scatter/gather: Address Modifier/Memory Type/Transfer Type, Buffer Address, Maximum Transfer Length, and the Reserved field at Words 0xC - 0xD. For a detailed discussion, please refer to *Scatter/Gather Operations* in Chapter 6.

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SCSI PASS-THROUGH
Command ID: 0x20

SCSI PASS-THROUGH
Command ID: 0x20

Bit 2 Suppress Synchronous Transfers:

Setting this bit in the *first* pass-through command sent to a device causes the board to disable synchronous transfers with that device. The first command issued to the board without this bit set will cause synchronous negotiation at selection. This bit is provided as a work around in the event a device does not process the SCSI synchronous data transfer request message correctly. Thus, the bit should be cleared for normal operations.

Bits 3-5 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 6 Suppress IOPB Timeout:

Setting this bit prevents a timeout from being generated by this IOPB, regardless of the value entered for the Command Timeout field in the Initialize Work Queue IOPB during initialization. This allows SCSI commands which exceed a normally useful timeout threshold, like Format, to be issued through the normal device work queue.

Bit 7 Reserved:

This bit is reserved and must be cleared to 0 by the host.

Bit 8 VMEbus Transfer Direction:

This bit specifies the direction of the data transfer over the VMEbus, as follows:

BIT 8	VMEbus DIRECTION
0	Write data to the VMEbus
1	Read data from the VMEbus

Figure 5-3. VMEbus Transfer Direction For SCSI Pass-Through Command

Bits 9-10 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 11 Enable Wide Data Transfers:

W

Setting this bit will cause the board to attempt communication with the device in wide (16-bit) SCSI data transfer mode. The first command issued to the board with this bit set will initiate Wide SCSI negotiation at selection. Once Wide SCSI data transfers are negotiated, the only way to switch back to 8-bit SCSI transfers will be to reset the SCSI bus. This bit is provided as a work around in the event a device does not process the SCSI wide data transfer request message correctly, and should be set for normal operations. See the Device Reinitialize command on page 5-102 for other uses of this bit.

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SCSI PASS-THROUGH
Command ID: 0x20

Bit 12-15 SCSI Queue Tag Type:

Refer to the SCSI-2 specification for detailed information on SCSI queue tags.

The host should determine, through the SCSI Inquiry Command, if a device supports queue tag messages prior to issuing a Pass-Through IOPB with a SCSI Queue Tag Type specified. Support for SCSI Queue Tag Messages must be handled by the host, since knowledge of the device type is required to select an appropriate Queue Tag type.

Bit 15	Bit 14	Bit 13	Bit 12	Meaning*
0	0	0	0	No Queue Tag Message sent to Target
0	0	0	1	Simple Queue Tag Message sent to Target
0	0	1	0	Ordered Queue Tag Message sent to Target
0	0	1	1	Head of Queue Tag Message sent to Target

* All bit combinations not listed above are reserved

Figure 5-4. SCSI Queue Tag Types

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

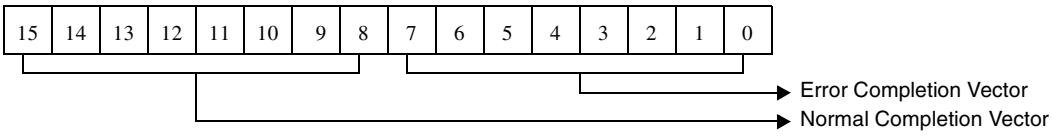


Figure 5-5. Normal/Error Completion Vector For SCSI Pass-Through Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

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SCSI PASS-THROUGH
Command ID: 0x20

SCSI PASS-THROUGH
Command ID: 0x20

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

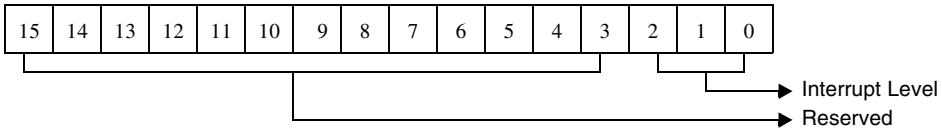


Figure 5-6. Interrupt Level For SCSI Pass-Through Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed with a level of 0 allowed only when interrupts are disabled by clearing the interrupt enable bit in the Command Options word.

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

VME Transfer Type (2 Bytes)

This field specifies the address modifier, memory type, and transfer type to be used for all VMEbus transfers associated with the command.

NOTE: As a slave, the board responds to either 0x2D *and* 0x29, or 0x2D VME address modifiers only. This depends on how the address modifier jumpers are set onboard. For a description of these jumpers, refer to chapter 2. As a master, the board will use whatever address modifier is in the IOPB. It is not checked. Some memory systems may not support all of the options discussed for this field.

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SCSI PASS-THROUGH
Command ID: 0x20

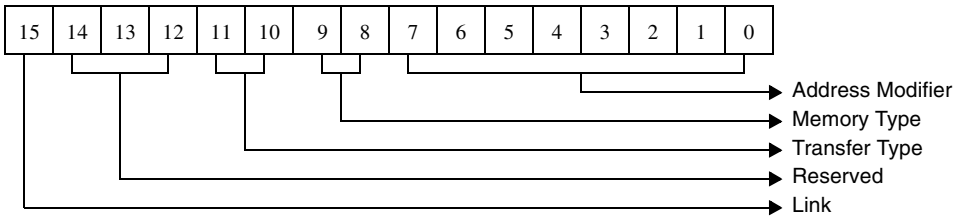


Figure 5-7. VME Transfer Types For SCSI Pass-Through Command

Bits 0-7 Address Modifier:

This byte specifies the address modifier used by the board for all VMEbus data transfers associated with this command.

Bits 8-9 Memory Type:

This 2-bit field specifies the width of the data transfers. Permitted values are shown below.

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	16-bit transfers
1	0	32-bit transfers
1	1	Scatter/gather list resides in short I/O*

* Valid only for Scatter/Gather operations

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SCSI PASS-THROUGH
Command ID: 0x20

SCSI PASS-THROUGH
Command ID: 0x20

Bits 10-11 Transfer Type:

This 2-bit field specifies the type of data transfer to be performed. Permitted values are shown below.

BIT 11	BIT 10	TRANSFER TYPE
0	0	NORMAL TYPE
0	1	BLOCK MODE
1	0	(RESERVED)
1	1	VME D64 BLOCK

Bits 12-14 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 15 Link:

This bit should only be set if you are linking scatter/gather lists. Refer to *Scatter/Gather List Linking* in Chapter 6 for details.

Buffer Address (4 Bytes)

This field specifies the address at which the board will begin the data transfer. If the board is addressing system memory, the value in the field is a VMEbus address. If scatter/gather is enabled, this field is the address of the scatter/gather list. If the scatter/gather list is in Short I/O, the value is an offset from the board's Short I/O base address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW BUFFER ADDRESS (or Address of Scatter/Gather List) LSW															

Figure 5-8. Buffer Address For SCSI Pass-Through Command

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SCSI PASS-THROUGH
Command ID: 0x20

Maximum Transfer Length (4 Bytes)

This field specifies the maximum number of bytes that may be transferred by the command. If no data is to be transferred, a Transfer Length of zero should be specified. When scatter/gather is enabled, this field contains the number of scatter/gather elements.

NOTE: In the returned IOPB of the the command response, this value reflects the actual number of bytes transferred.

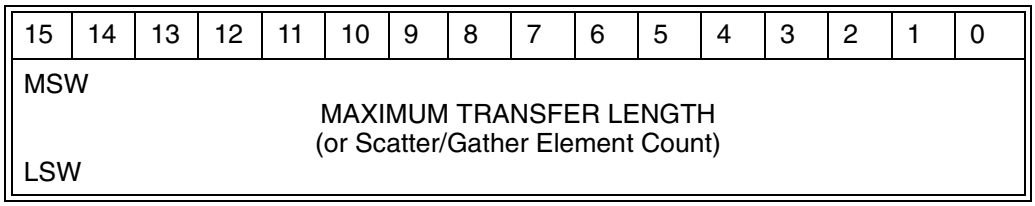


Figure 5-9. Maximum Transfer Length For SCSI Pass-Through Command

Reserved (4 Bytes)

Unless scatter/gather is enabled, words 0xC and 0xD of the SCSI Pass-Through IOPB are reserved and must be cleared by the host. For scatter/gather operations, this field specifies the sum of the individual element entry counts. See Chapter 6, *Scatter/Gather Operations*, for details.

Unit Address For SCSI-2 Operation (2 Bytes)

This field specifies the SCSI bus and the address of the target device for the Cougar II. (For Cougar II Wide operation, see *Extended Unit Address*, page.)

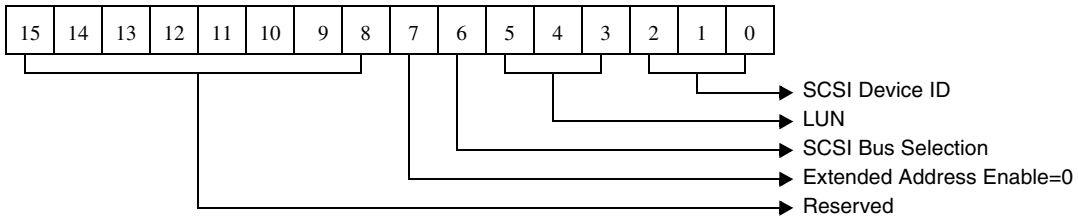


Figure 5-10. Unit Address For SCSI Pass-Through Command

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SCSI PASS-THROUGH
Command ID: 0x20

SCSI PASS-THROUGH
Command ID: 0x20

Bits 0-2 SCSI Device ID:

These bits contain the SCSI Device ID used when addressing the target. This value may range from 0 to 7.

Bits 3-5 Logical Unit Number:

This 3-bit field specifies the SCSI Logical Unit Number. will be defined in these three bits. Refer to the SCSI-2 specification for a detailed description of Logical Unit Numbers.

Bit 6 SCSI Bus Selection:

This bit selects which of the two SCSI buses the board uses when executing the command. When this bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, the board uses the secondary SCSI bus (Port 1).

Bit 7: Extended Address Enable:

This bit is cleared to 0 for SCSI-2 addressing (SCSI ID values 0-7). Extended addressing for SCSI-2 Wide operation is enabled when this bit is set to 1 (for up to 32 devices). See Extended Unit Address below.

Bits 8-15 Reserved:

When bit 7 is cleared, bits 8-15 are reserved, and must be cleared to 0 by the host.

W *Extended Unit Address For SCSI-2 Wide Operation*

This field specifies the SCSI bus and the address of the target device for SCSI-2 Wide operation.

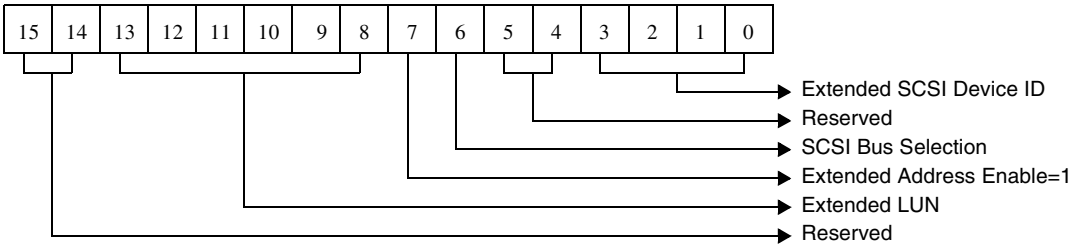


Figure 5-11. Extended Unit Address For SCSI Pass-Through Command

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SCSI PASS-THROUGH
Command ID: 0x20

Bits 0-3 Extended SCSI Device ID:

This 3-bit field contains the Extended SCSI ID used when addressing the target. This value may range from 0 to 15.

Bit 4-5 Reserved:

These bits are reserved and must be set to zero by the host.

Bit 6 SCSI Bus Selection:

This selects which of the two SCSI buses the board uses when executing the command. When this bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7 Extended Address Enable:

When this bit is set to 1, the LUN is taken from the 6-bit extended LUN field, and the SCSI device ID is taken from the 4-bit extended SCSI device ID field.

Bits 8-13 Extended LUN:

Setting Bit 7 enables the extension to both the LUN and the SCSI Device ID fields.

Bits 14-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

SCSI Command Bytes

The SCSI Command Bytes specify the bytes that the board passes unchanged across the SCSI bus to the selected SCSI device. The size of the SCSI Pass-Through IOPB can be adjusted to accommodate different SCSI command lengths. For example, to issue a 12-byte SCSI command, append the 12-byte SCSI Command Descriptor Block (CDB) starting at word 0x10 of the IOPB.

The board determines the length of the SCSI Command Descriptor Blocks by looking at the group code in SCSI Byte 0 of the IOPB ().

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SCSI PASS-THROUGH
Command ID: 0x20

SCSI PASS-THROUGH
Command ID: 0x20

Table 5-2.Group Codes For SCSI Commands

GROUP	CDB LENGTH
0	6 Bytes
1	10 Bytes
2	10 Bytes
3	(Reserved)
4	(Reserved)
5	12 Bytes
6	User Defined
7	User Defined

If the command is a Group 0, 1, 2, or 5 SCSI command, the board will "know" the length of the CDB (6, 10, or 12 bytes, respectively), and the board will ignore the IOPB Length field of the corresponding Command Queue entry.

The IOPB Length field of the Command Queue entry for a user-defined SCSI command (Group 6 or 7) must specify the length of the IOPB in **words**. The board calculates the CDB length by subtracting the overhead of the IOPB (0x10 words) from the length specified in the Command Queue entry.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB of the command response for the SCSI Pass-Through command.

Return Status (2 Bytes)

This field provides the return status for the command.

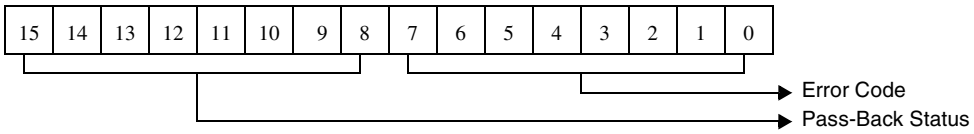


Figure 5-12. Return Status For SCSI Pass-Through Command

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SCSI PASS-THROUGH
Command ID: 0x20

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response. Any non-zero value is an error code. Appendix C contains the error codes.

Bits 8-15 Pass-Back Status:

This value is the SCSI status byte returned by the target device. It is not changed by the board. A value of 0x0 indicates Good Status. A non-zero value indicates that a SCSI device error has occurred.

NOTE: The board can be configured to respond to a non-zero pass-back status by:

- Freezing the queue,
- Aborting all commands in or destined for the queue, or
- Initiating autosense error recovery

The work queue options are set via the Initialize Work Queue command, and are mutually exclusive. (See Work Queue Options, page and Error Recovery Tools in Chapter 6 for details).

Maximum Transfer Length Field (4 Bytes)

This field, in the returned IOPB of the command response, reflects the actual number of bytes transferred.

Sense Data Bytes (Variable Length)

If the Autosense Error Recovery option is enabled and a SCSI check condition occurs, the sense data returned from the target device will be reported in the returned IOPB, overwriting the SCSI Command Descriptor Block (i.e. SCSI bytes 0-11) and possibly extending beyond. Autosense Recovery is enabled via the Initialize Work Queue command.

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SCSI RESET

Command ID: 0x22

The SCSI Reset IOPB instructs the board to reset the SCSI bus identified by the command. It terminates all pending commands on the SCSI bus. A Command Complete with Error will be issued for each command terminated as a result of the SCSI Reset command. Normally, this command is used only in an to attempt to recover from an unusual error condition.

When the host issues a Reset SCSI Bus IOPB through the Master Command Entry, *all* work queues with commands active on the specified SCSI bus will have those commands returned with a Command Aborted by Reset (during execution) or a SCSI Bus Reset Status Error.

The work queues corresponding to those commands may be optionally frozen if the Freeze Work Queue on Reset option is enabled via the Initialize Controller command. (See *Work Queue Options* [page and *Error Recovery Tools* in Chapter 6 for details).

NOTE: It may be necessary for the host to issue a SCSI Request Sense to on-line devices after executing the SCSI Reset command. This depends on what the device(s) require after a SCSI bus reset. Consult device manuals for details.

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x22)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xd	RESERVED															
0xE	SCSI BUS ID															

NOTES: Fields set in **Bold** letters are returned values. The host provides all other values.
Reserved fields must be set to 0 by the host.

Figure 5-13. SCSI Reset IOPB

The following section describes the function of each field in the SCSI Reset IOPB.

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SCSI RESET
Command ID: 0x22

SCSI RESET
Command ID: 0x22

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the SCSI Reset command:

Command Code (2 Bytes)

This field must be set to 0x22 to execute the SCSI Reset command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

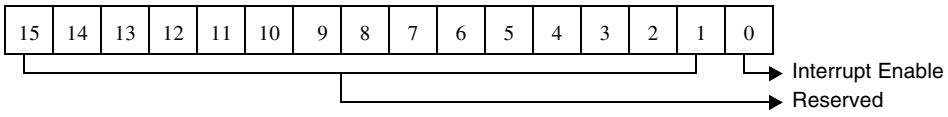


Figure 5-14. Command Options For SCSI Reset Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

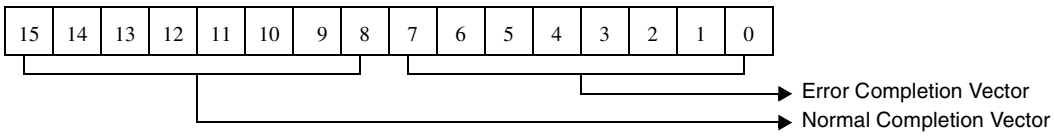


Figure 5-15. Normal/Error Completion Vector For SCSI Reset Command

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SCSI RESET
Command ID: 0x22

SCSI RESET
Command ID: 0x22

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

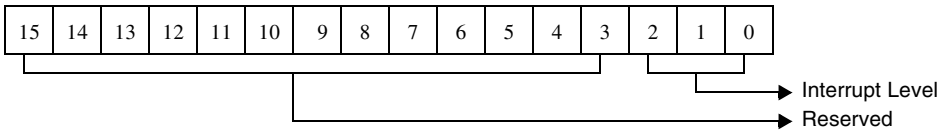


Figure 5-16. Interrupt Level For SCSI Reset Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed with a level of 0 allowed only when interrupts are disabled by clearing the interrupt enable bit in the Command Options word.

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

SCSI Bus ID (2 Bytes)

This field identifies which bus is to be reset.

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SCSI RESET
Command ID: 0x22

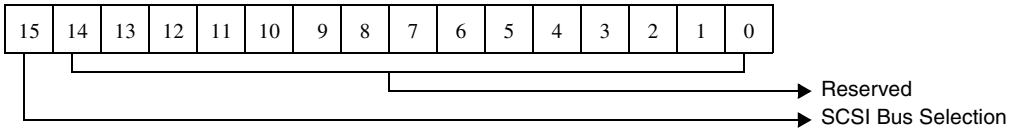


Figure 5-17. SCSI Bus ID For SCSI Reset Command

Bits 0-14 Reserved:

These bits are reserved and must be cleared to 0.

Bit 15 SCSI Bus Selection:

This bit selects which of the two SCSI buses the board uses when executing the command. When this bit is cleared to 0, the board executes the command over the primary SCSI bus (Channel 0). When set to 1, the board uses the secondary SCSI bus (Channel 1).

Returned Values

Upon command completion, the following information is provided by the board, in the returned IOPB of the command response, for the SCSI Reset command:

Return Status (2 Bytes)

Upon successful completion of the SCSI Bus Reset, these two bytes will hold the value 0x0011, indicating that the IOPB has completed successfully, and has generated a reset on the specified bus. If interrupts are enabled for this IOPB, the error interrupt vector will be used. (This behavior is compatible with the Jaguar 4210.)

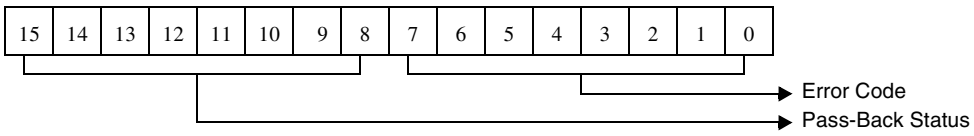


Figure 5-18. Return Status For SCSI Reset Command

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PRINTER PORT

Command ID: 0x23

The Printer Port command is used to issue instructions to a printer connected to the optional printer port. Before issuing a Printer Port IOPB, the host must initialize a work queue and issue the port using the Initialize Printer Port command. (See Initialize Printer Port (page), and Printer Port Operation in Chapter 6 for complete instructions on use of the printer port.)

The format of the Printer Port IOPB is shown in.

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x23)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6	RESERVED															
0x7	RESERVED					TT	MT		ADDRESS MODIFIER							
0x8	BUFFER ADDRESS															
0x9																
0xA	MAXIMUM TRANSFER LENGTH															
0xB																
0xC	PRINTER TRANSFER LENGTH															
0xD																
0xE	RESERVED								PRINTER STATUS							
0xF To 0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-19. Printer Port IOPB

The remainder of this section describes the function of each field in the Printer Port IOPB.

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PRINTER PORT
Command ID: 0x23

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Printer Port command:

Command Code (2 Bytes)

This field must be set to 0x23 to execute the Printer Port command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

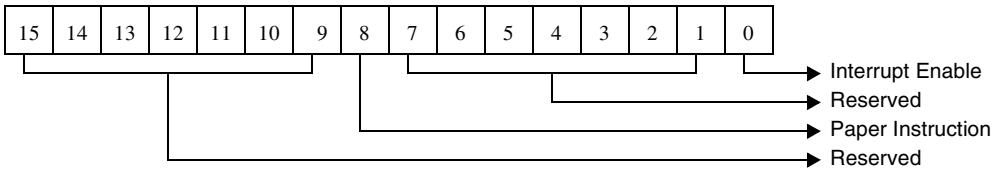


Figure 5-20. Command Options For Printer Port Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-7 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 8 Paper Instruction:

Setting this bit causes the board to transfer all of the data specified in this IOPB to the printer with the Paper Instruction interface signal active. The Paper Instruction signal is only supported by Dataproducts printers.

Bits 9-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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PRINTER PORT
Command ID: 0x23

PRINTER PORT
Command ID: 0x23

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

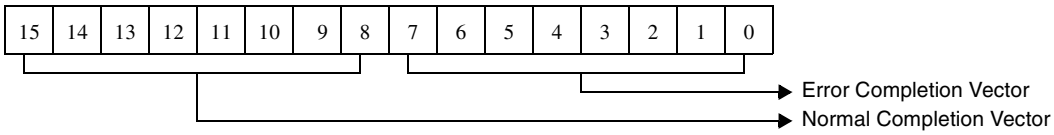


Figure 5-21. Normal/Error Completion Vector For Printer Port Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

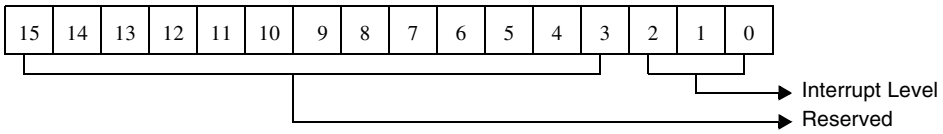


Figure 5-22. Interrupt Level For Printer Port Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed with a level of 0 allowed only when interrupts are disabled by clearing the interrupt enable bit in the Command Options word.

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PRINTER PORT
Command ID: 0x23

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

VME Transfer Type (2 Bytes)

This field specifies the address modifier, memory type, and transfer type to be used for all VMEbus transfers associated with the command.

NOTE: Some memory systems may not support all of the options discussed for this field.

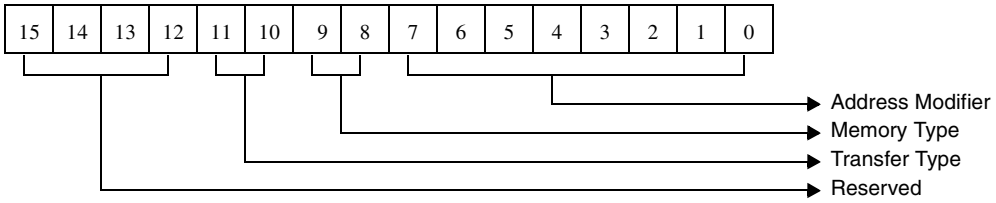


Figure 5-23. VME Transfer Types For Printer Port

Bits 0-7 Address Modifier:

This byte specifies the address modifier to be used by the board for all VMEbus data transfers associated with this command.

Bits 8-9 Memory Type:

This 2-bit field specifies the width of the data transfer. shows the permitted values.

Table 5-3.Memory Type For Printer Port Command

BIT 9	BIT 8	MEMORY TYPE
0	0	RESERVED
0	1	16-BIT TRANSFERS
1	0	32-BIT TRANSFERS
1	1	RESERVED

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PRINTER PORT
Command ID: 0x23

PRINTER PORT
Command ID: 0x23

Bits 10-11 Transfer Type:

This 2-bit field specifies the type of data transfer to be performed. shows the permitted values.

Table 5-4.Transfer Type For Printer Port Command

BIT 11	BIT 10	TRANSFER TYPE
0	0	NORMAL MODE
0	1	BLOCK MODE
1	0	RESERVED
1	1	VME D64 Block

Bits 12-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Buffer Address (4 Bytes)

This field specifies the address in system memory at which the board will begin the data transfer.

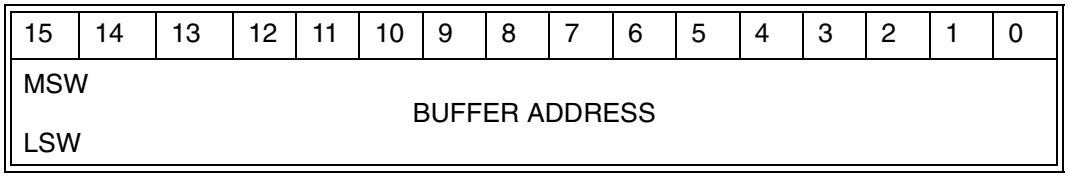


Figure 5-24. Buffer Address For Printer Port Command

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PRINTER PORT
Command ID: 0x23

Maximum Transfer Length (4 Bytes)

This field specifies the maximum number of bytes that may be transferred by the command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	MAXIMUM TRANSFER LENGTH														

Figure 5-25. Maximum Transfer Length For Printer Port Command

Printer Transfer Length (4 Bytes)

The Printer Transfer Length field is used to specify the exact number of bytes to be transferred to the printer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	PRINTER TRANSFER LENGTH														

Figure 5-26. Printer Transfer Length For Printer Port Command

NOTE: Entering a length of zero in both the Maximum Transfer Length field and in the Printer Transfer Length field causes the board to return the IOPB with the current printer status.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB, of the command response, for the Printer Port command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code.

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PRINTER PORT
Command ID: 0x23

PRINTER PORT
Command ID: 0x23

Printer Status (1 Byte)

This field contains the state of the printer status control lines at the completion of the data transfer. Only those lines which were enabled when the printer port was initialized will be reported. The definition of the bits in this field vary depending on the printer type, as listed in.

DATAPRODUCTS DEFINITION (ACTIVE HIGH)	
BIT 7	Software Readable Jumper 1 = Dataproducts, 0 = Centronics
BIT 6	Paper Movement
BIT 5	Top Of Form
BIT 4	Bottom Of Form
BIT 3	Cable On
BIT 2	Parity Error
BIT 1	Online
BIT 0	Ready
CENTRONICS STATUS DEFINITION (ACTIVE HIGH)	
BIT 7	Software Readable Jumper 1 = Dataproducts, 0 = Centronics
BIT 6	Busy
BIT 5	Reserved - value returned may be either 0 or 1
BIT 4	Reserved - value returned may be either 0 or 1
BIT 3	Reserved - value returned may be either 0 or 1
BIT 2	Paper Empty
BIT 1	Select
BIT 0	Fault

Figure 5-27. Definition Of Printer Status Bits

Returned Values For Printer Status Change Interrupt

If status change interrupts were enabled when the printer port was initialized, the board generates an interrupt and posts the information shown below to the Command Response Block when a status change occurs.

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PRINTER PORT
Command ID: 0x23

PRINTER PORT
Command ID: 0x23

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND RESPONSE STATUS WORD															
0x1 TO 0x5	(RESERVED)															
0x6	PRINTER STATUS								RETURN CODE							

Figure 5-28. Return Information For Printer Status Change Interrupt

The Status Change bit (Bit 7) in the Command Response Status Word is set, and an image of the printer's status lines is returned. The bits in the Printer Status field have the same definition as in the Printer Status field in the Printer Port IOPB (see above).

The value in the Return Code field should be 0x90 (Printer Status Change).

NOTE: More than one status line may change in a single interrupt, so the entire status should be verified by the host.

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PERFORM DIAGNOSTICS

Command ID: 0x40

The Perform Diagnostics command causes the board to perform a set of pass/fail self-diagnostic tests that are identical with those performed during the power-up self test. All of the tests are performed, and then the status of each test is reported back in the Command Response Block. Due to the nature of these tests, the Perform Diagnostics command cannot be executed while the board is operating. The board returns an error if this command is issued while ANY other command is queued.

The Perform Diagnostics command must be issued through the Master Command Entry to Work Queue 0.

This command cannot be reported back via an off-board Command Response Block, and no interrupt will be generated.

After executing this command, it is necessary to reset the 4220 before issuing additional commands to it.

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x40)															
0x1 To 0xD	RESERVED															
0xE	**ROM TEST RESULT**															
0xF	**SCRATCHPAD RAM TEST RESULT**															
0x10	**BUFFER RAM TEST RESULT**															
0x11	**DMA CONTROL REGISTER TEST RESULT**															
0x12	**PRIMARY SCSI CHANNEL REGISTER TEST**															
0x13	**SECONDARY SCSI CHANNEL REGISTER TEST**															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-29. Perform Diagnostic IOPB

The remainder of this section describes the function of each field in the Perform Diagnostics IOPB.

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PERFORM DIAGNOSTICS
Command ID: 0x40

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Perform Diagnostics command:

Command Code (2 Bytes)

This field must be set to 0x40 to execute the Perform Diagnostics command.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Perform Diagnostics command:

ROM Test Result (2 Bytes)

These bytes return the status of the ROM Test. A test result of 0xFFFF indicates that the test completed successfully. Any other value indicates that the test failed.

Scratchpad RAM Test Result (2 Bytes)

These bytes return the status of the Scratchpad RAM Test. A test result of 0xFFFF indicates that the test completed successfully. Any other value indicates that the test failed.

Buffer RAM Test Result (2 Bytes)

These bytes return the status of the Buffer RAM Test. A test result of 0xFFFF indicates that the test completed successfully. Any other value indicates that the test failed.

DMA Control Register Test (2 Bytes)

These bytes return the status of the DMA Control Register Test. A test result of 0xFFFF indicates that the test completed successfully. Any other value indicates that the test failed.

Primary SCSI Channel Register Test (2 Bytes)

These bytes return the status of the Primary SCSI Channel Register Test. A test result of 0xFFFF indicates that the test completed successfully. Any other value indicates that the test failed.

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PERFORM DIAGNOSTICS
Command ID: 0x40

PERFORM DIAGNOSTICS
Command ID: 0x40

SCSI Secondary Channel Register Test (2Bytes)

These bytes return the status of the SCSI Secondary Channel Register Test. A test result of 0xFFFF indicates that the test completed successfully. A status of PASS (0xFFFF) is also returned if this test is run on a motherboard with no daughter card installed. Any other value indicates that the test failed.

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INITIALIZE CONTROLLER

Command ID: 0x41

Initialize Controller configures the board for use in a particular system. The host must issue this command before the board can engage in any activity on the SCSI bus.

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the IOPB for the Initialize Controller command is:

Word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x41)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6	RESERVED															
0x7	RESERVED				TT		MT		ADDRESS MODIFIER							
0x8	BUFFER ADDRESS															
0x9																
0xA	MAXIMUM TRANSFER LENGTH															
0xB																
0xC	RESERVED															
0xD																

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-30. Initialize Controller IOPB

The remainder of this section describes the function of each field in the Initialize Controller IOPB.

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Initialize Controller command:

Command Code (2 Bytes)

This field must be set to 0x41 to execute the Initialize Controller command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

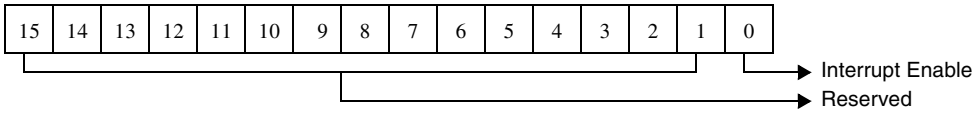


Figure 5-31. Command Options For Initialize Controller Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

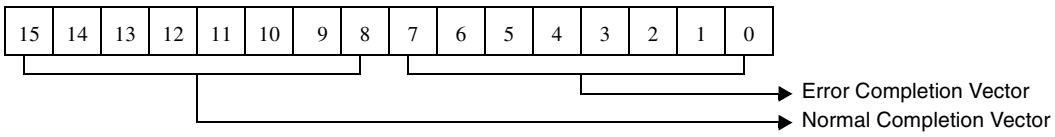


Figure 5-32. Normal/Error Completion Vector For Initialize Controller Command

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INITIALIZE CONTROLLER
Command ID: 0x41

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

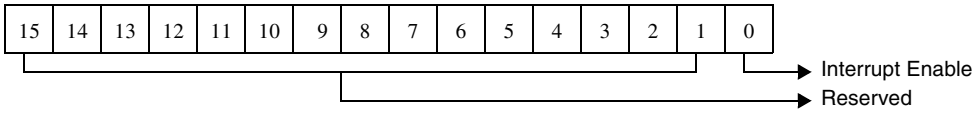


Figure 5-33. Interrupt Level For Initialize Controller Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Address Modifier/Memory Type Transfer Type (2 Bytes)

These bytes specify the address modifier, memory type, and transfer type to be used for all VMEbus transfers associated with the command.

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

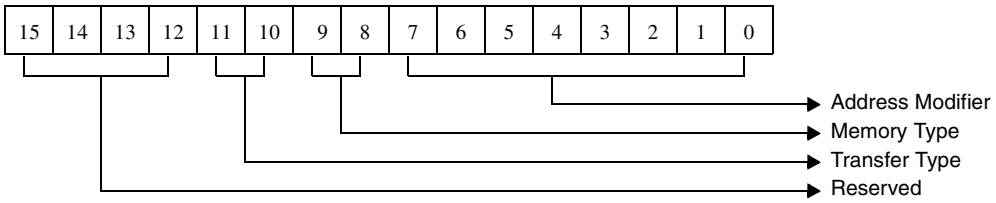


Figure 5-34. Address Modifier/Memory/Transfer Type For Initialize Controller Command

Bits 0-7 Address Modifier:

This byte must be cleared to 0x00 in the Initialize Controller Command.

Bits 8-9 Memory Type:

The only valid entry in this 2-bit field is 0x3 (data is located in Short I/O space).

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	(RESERVED)
1	0	(RESERVED)
1	1	Data is contained in Short I/O

Figure 5-35. Memory Type Field For Initialize Controller Command

Bits 10-11 Transfer Type:

This 2-bit field must be cleared to 0.

Bits 12-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Buffer Address (4 Bytes)

This field contains the offset of the Controller Initialization Block from the Short I/O base address.

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INITIALIZE CONTROLLER
Command ID: 0x41

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	BUFFER ADDRESS														

Figure 5-36. Buffer Address For Initialize Controller Command

Maximum Transfer Length (4 Bytes)

This field specifies the maximum number of bytes that may be transferred by the command, and represents the size of the Controller Initialization Block.

NOTE: An incorrect value in this field may cause the initialization parameters to be ignored.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	MAXIMUM TRANSFER LENGTH														

Figure 5-37. Maximum Transfer Length For Initialize Controller Command

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Controller Initialization Block

The Buffer Address of the Initialize Controller IOPB points to a list of initialization parameters called the Controller Initialization Block (CIB). The host must assemble the Controller Initialization Block in the Host Usable Space (HUS) before issuing the Initialize Controller command. Once it issues the Initialize Controller command, the host cannot modify the CIB until the Initialize Controller command has completed interrupt for the initialize command. The format is as follows:

Figure 5-38. Controller Initialization Block

WORD	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	NUMBER OF COMMAND QUEUE ENTRIES IN SHORT I/O															
0x1	DMA BURST COUNT															
0x2	CONTROLLER NORMAL COMPLETION LEVEL/VECTOR															
0x3	CONTROLLER ERROR COMPLETION LEVEL/VECTOR															
0x4	PRIMARY SCSI BUS ID															
0x5	SECONDARY SCSI BUS ID															
0x6	COMMAND RESPONSE BLOCK OFFSET															
0x7	SCSI SELECTION TIMEOUT (IN MILLISECONDS)															
0x8																
0x9	WORK QUEUE 0 COMMAND TIMEOUT															
0xA																
0xB	VMEBUS TIMEOUT (0 = 100msec TIMEOUT)															
0xC																
0xD	RESERVED															
0xE																
0xF	OFFBOARD CRB VME TRANSFER TYPE															
0x100	OFFBOARD COMMAND RESPONSE BLOCK ADDRESS (In Host Memory)															
0x11																
0x12	ERROR RECOVERY OPTIONS															
0x13	RESERVED															
0x14	RESERVED															
0x15	SCSI Bus Reset Interrupt Vector															
0x16	Synchronous Offset (Bus 0)								Synchronous Negotiation Rate (Bus 0)							
0x17	Synchronous Offset (Bus 1)								Synchronous Negotiation Rate (Bus 1)							

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INITIALIZE CONTROLLER
Command ID: 0x41

The following is a description of each field in the Controller Initialization Block.

Number of Command Queue Entries (2 Bytes)

This field sets the number of entries in the Command Queue. The Command Queue must have at least one entry. The maximum number of entries varies greatly depending on the application. If you are using onboard IOPBs, which require that both the Command Queue entry and its corresponding IOPB be written to Host Usable Space in Short I/O, the maximum number of entries is relatively limited. A typical setup for onboard IOPBs is a 10-entry Command Queue.

NOTE: Each CQE/IOPB only resides in Short I/O for a very short period of time before being transferred into the appropriate work queue.

A much larger Command Queue is allowed in applications using offboard IOPBs, in which the board DMAs IOPBs directly from system memory into the appropriate work queue. Nevertheless, the size of the Command Queue is still application-dependent. The maximum number of Command Queue entries in a setup using offboard IOPBs depends on the size of Short I/O and application requirements. See Offboard IOPBS in Chapter 6.

DMA Burst Count (2 Bytes)

The controller has two distinct burst modes – Burst Count Mode and Time On/Time Off Fair Arbitration Mode. This serves to retain backward compatibility as well as to provide more flexibility in controlling bursts on the VMEbus.

Burst Count Mode:

Burst Count Mode is enabled by clearing the bit 15 (Burst Mode) to 0.

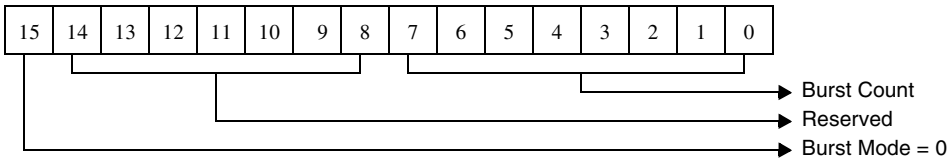


Figure 5-39. Burst Count Mode Enabled

When Burst Mode is enabled, the bits in this field have the following meaning.

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Bits 0-7 Burst Count:

This field defines how long the board will hold on to the VMEbus before releasing it.
If the burst count is 0, the board will request the bus, and upon being granted the bus will transfer data until there is no more data to be transferred.

If the burst count is greater than 0, but less than 0x21, the board will request the bus, and upon being granted the bus, will transfer data until there is no more data to be transferred, or 16 microseconds has elapsed since being granted the bus, or one of the bus request lines on the VMEbus is asserted.

If the burst count is greater than 0x20, but less than 0x41, the board will request the bus, and upon being granted the bus, will transfer data until there is no more data to be transferred, or 16 microseconds has elapsed since being granted the bus.

If the burst count is greater than 0x40, but less than 0x81, the board will request the bus, and upon being granted the bus, will transfer data until there is no more data to be transferred, or 32 microseconds has elapsed since being granted the bus.

If the burst count is greater than 0x80, the board will request the bus, and upon being granted the bus, will transfer data until there is no more data to be transferred, or 64 microseconds has elapsed since being granted the bus.

Burst Count	Function
0x00	Keep the VMEbus until done.
0x01-0x20	Keep the VMEbus 16 microseconds or until BRx is asserted by another board.
0x21-0x40	Keep the VMEbus 16 microseconds.
0x41-0x80	Keep the VMEbus 32 microseconds.
0x81-0xFF	Keep the VMEbus 64 microseconds.

Figure 5-40. VMEbus Burst Count Settings

Bits 8-14 Reserved:

These bits are reserved and must be set to zero.

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INITIALIZE CONTROLLER
Command ID: 0x41

Bit 15 Burst Mode:

The value of this bit determines how the CIB DMA Burst Count value is used. If the Burst Mode bit is set to 1, the Time On/Time Off and Fair Arbitration fields have meaning. If the Burst Mode bit is set to 0, the Burst Count field has meaning.

Time On/Time Off Fair Arbitration Mode

Setting the mode bit in bit 15 enables Time On/Time Off Fair Arbitration Mode instead of Burst Count Mode. This mode causes the bits in this field to be defined as follows:

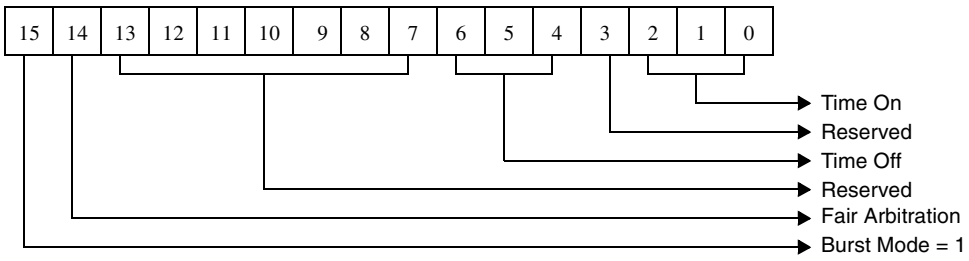


Figure 5-41. Time On/Time Off Fair Arbitration Mode Enabled

Bits 0-2 Time On

This field defines how long the board will hold on to the VMEbus before releasing it.

Bit 2	Bit 1	Bit 0	Elapsed Time
0	0	0	16 Microseconds
0	0	1	32 Microseconds
0	1	0	64 Microseconds
0	1	1	128 Microseconds
1	0	0	256 Microseconds
1	0	1	512 Microseconds
1	1	0	1024 Microseconds
1	1	1	When Done

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Bit 3 Reserved:

This bit is reserved and must be set to zero by the host.

Bits 4-6 Time Off:

This field defines how long the board will wait after releasing the VMEbus before requesting it again.

Bit 6	Bit 5	Bit 4	Elapsed Time
0	0	0	0 Microseconds
0	0	1	16 Microseconds
0	1	0	32 Microseconds
0	1	1	64 Microseconds
1	0	0	128 Microseconds
1	0	1	256 Microseconds
1	1	0	512 Microseconds
1	1	1	1024 Microseconds

Bits 7-13 Reserved:

These bits are reserved and must be set to 0 by the host.

Bit 14 Fair Arbitration:

Setting this bit will cause the board to sample the Bus Request (BRx) signal on the VMEbus before asserting BRx. If the BRx signal is already asserted, then the board will wait until BRx is negated before asserted BRx. If this bit is clear, the board will assert BRx whenever the board requires the VMEbus.

Bit 15 Burst Mode:

The value of this bit determines how the CIB DMA Burst Count value is used. If the Burst Mode bit is set to 1, the Time On/Time Off and Fair Attribute fields have meaning. If the Burst Mode bit is set to 0, the Burst Count field has meaning.

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INITIALIZE CONTROLLER
Command ID: 0x41

Controller Normal Completion Level/Vector (2 Bytes)

This field specifies the VMEbus interrupt level and vector that the board will use to report the normal command completion.

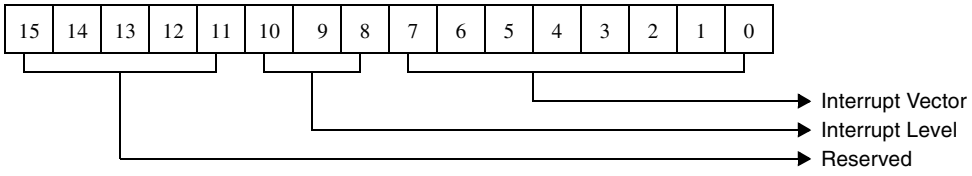


Figure 5-42. Controller Normal Completion Level/Vector For Controller Initialization Block

Bits 0-7 Interrupt Vector:

This level specifies the interrupt vector used by the board when reporting normal controller interrupts.

Bits 8-10 Interrupt Level:

This level specifies the interrupt level used by the board when reporting normal controller interrupts. The host sets these bits and the board does not modify them.

Bits 11-15 Reserved:

Bits 11 through 15 are reserved and should be cleared to 0 by the host.

Controller Error Completion Level/Vector (2 Bytes)

This field specifies the interrupt level and vector that the board will use when reporting a variety of controller errors. Such errors will not generate an interrupt if the interrupt level is set to 0. However, the board will still report such errors in the Command Response Block. For additional information on this field, refer to *Controller Error Interrupt and Vector*.

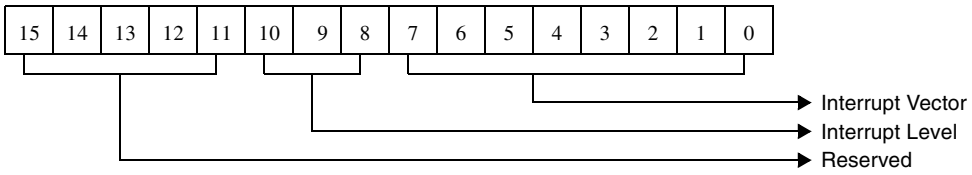


Figure 5-43. Controller Error Completion Level/Vector For Controller Initialization Block

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Bits 0-7 Interrupt Vector:

This byte is the Interrupt Vector used by the board when reporting Controller Error Interrupts.

Bits 8-10 Interrupt Level:

These bits set the Interrupt Level used by the board when reporting the Controller Error Interrupts.

Bits 11-15 Reserved:

Bits 11 through 15 are reserved and should be cleared to 0 by the host.

Primary SCSI Bus ID (2 Bytes)

The Primary SCSI Bus ID specifies the ID the board uses for its SCSI bus address on Channel 0. The board can either use its default ID, set via hardware jumpers, or it may use the value given in bits 0 through 2.

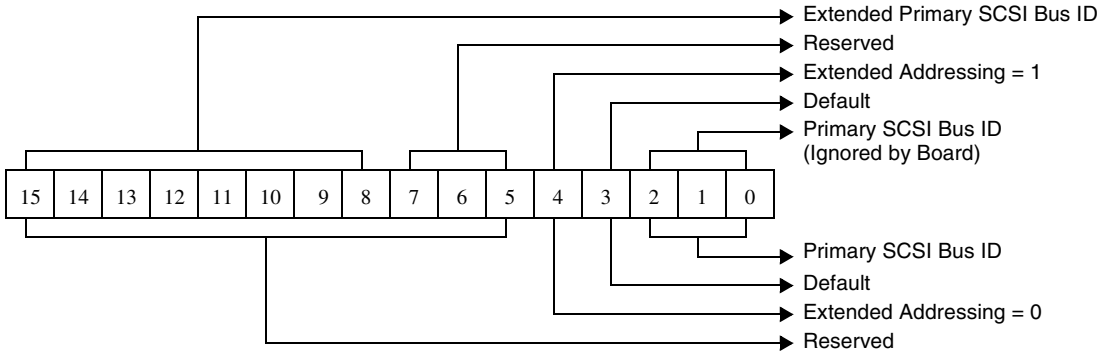


Figure 5-44. Primary SCSI Bus ID For Controller Initialization Block

Bits 0-2 Primary SCSI Bus ID (when Bit 3 = 0):

If Bit 3 is cleared, the value stored in this field will be used by the board as its Primary SCSI Bus ID. This field may have any value from 0x0 to 0x7. When Bit 3 is set to "1" the Primary SCSI Bus ID is determined by the Primary SCSI Bus ID hardware jumper. Refer to chapter 2 for the identification and location of this jumper.

Bit 3 Default:

Setting the DEFAULT bit to "1" enables the board to use its jumper-selected primary SCSI ID (Chapter 2). Clearing the DEFAULT bit to "0" causes the board to use the ID specified in the ID field (bits 0-2) of this word.

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INITIALIZE CONTROLLER
Command ID: 0x41

Bits 5-15 Reserved (when Bit 3 = 0):

When Bit 3 is cleared to "0" these bits are reserved and must be cleared to 0 by the host.

Bit 4 Extended Address Enable = 0:

When this bit is cleared, the fields of the Primary SCSI Bus ID are defined as indicated above. The primary SCSI Bus ID may contain values from 0x0 to 0x7. When this bit is set, a field large enough for wide SCSI Bus IDs is enabled.

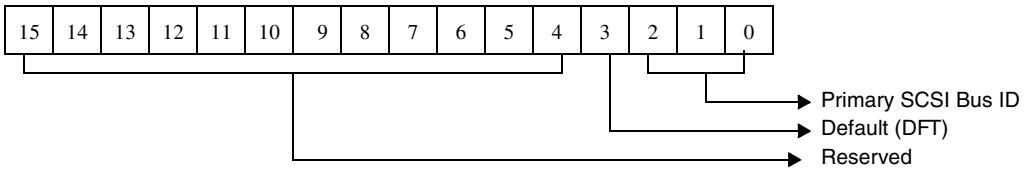


Figure 5-45. Primary SCSI Bus ID For Controller Initialization Block

Bits 0-3 Reserved (when Bit 4 = 1):

These bits are ignored by board when bit 4 (Extended Address Enable bit) is set to "1".

Bit 4 Extended Address Enable = 1

This bit is cleared to 0 for SCSI - 2 operation (values 0-7). Extended addressing for SCSI-2 wide operation is enabled when this bit is set to 1.

Bit 5-7 Reserved (when Bit 4 = 1)

These bits are cleared to "0" when bit 4 is set to "1".

Bits 8-15 (when Bit 4 = 1)

This field allows a range of values from 0 to 255.

When the Extended Address Enable bit is set to 1, and the Default bit is cleared to 0, the Cougar SCSI ID is defined by the value of bits 8-15. This value may range from 0 to 15.

NOTE: The Cougar II wide board currently supports 15 devices per SCSI channel, according to the SCSI-2 specification.

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Secondary SCSI Bus ID (2 Bytes)

The Secondary SCSI Bus ID specifies the ID the board uses for its SCSI bus address on Channel 1. The board can either use its default ID or it may use the value given in bits 0 through 2.

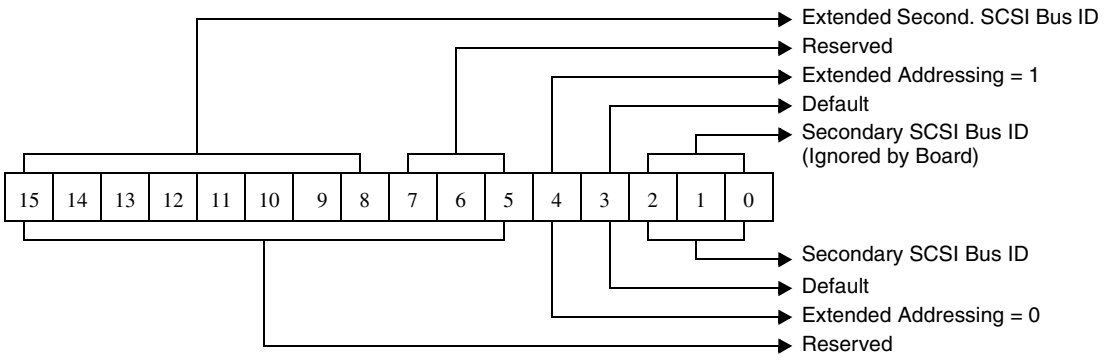


Figure 5-46. Secondary SCSI Bus ID For Controller Initialization Block

Bits 0-2 Secondary SCSI Bus ID (when bit 3 = 0):

The host uses these 3 bits to specify the SCSI ID the board is to use for Channel 1 when the Default bit (bit 3 = 0) is 0. This field may have any value from 0x0 to 0x7.

Bit 3 Default:

Setting the Default bit to "1" enables the board to use the default ID specified by the SCSI daughter card's jumpers. Clearing the Default bit to "0" causes the board to use the ID specified in the ID field (bits 0-2) of this word.

Bits 5-15 Reserved (when bit 4 = 0):

When bit 4 is cleared to "0" these bits are reserved and must be cleared to 0 by the host.

W ***Extended Secondary SCSI Bus ID***

Command Response Block Offset (2 Bytes)

The Command Response Block (CRB) Offset specifies the starting address of the CRB. By setting the CRB offset, the host is also specifying the length of the largest IOPB that can be transferred to the board. The largest IOPB is equal to the offset of the Controller Specific Space (0x788) minus the CRB offset, minus 12 bytes. If the CRB offset is 0x73C, for example, the largest IOPB cannot exceed 64 bytes (0x788 - 0x73C - 0xC).

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INITIALIZE CONTROLLER
Command ID: 0x41

The CRB offset must allow for a Command Response Block of at least 18 bytes so that there will always be enough room in the CRB to include the status bytes of the returned IOPB. Attempting to use a CRB offset that would result in a CRB of less than 18 bytes will result in the Initialize Controller Command completing with an error.

If SCSI Autosense Error Recovery is to be enabled, additional space must be allocated in the CRB offset for the SCSI sense data to be returned. The sense data will be returned in the Command Response Block starting with the first byte of the Command Descriptor Block in the returned IOPB. This data may extend to the beginning of the Configuration Status Block. The amount of sense data that the board requests from the device and returns in the CRB is determined by space from the CRB to the CSB, up to 255 bytes. If the data is being reported to an offboard CRB, the host must ensure that adequate space exists for this data to be written without generating system bus errors.

SCSI Selection Timeout (4 Bytes)

The SCSI Selection Timeout is 250 milliseconds and cannot be changed.

Work Queue 0 Command Timeout (4 Bytes)

This timeout specifies a timeout value for commands issued through Work Queue 0. This field is specified in increments of approximately 256msec. A value of 0 specifies no timeout. The board notifies the host of an IOPB timeout by use of the Controller Error interrupt. This interrupt will be used to return error status without returning the IOPB that caused the error. Bit 7 of the Command Response Status Word allows the allows the host to determine the source of the error. Also data returned in the command response block has been defined to specify the type of error that has occurred.

VMEbus Timeout (4 Bytes)

VMEbus Timeout is not supported by Cougar II. This field is reserved.

Offboard VME Transfer Type (2 Bytes)

This field is intended for applications which use the board's offboard IOPB feature (see *Offboard IOPBs* in Chapter 6). If this field and the Offboard Address field (below) are "0", the board will post the to the Short I/O space only. If these fields are non-zero, then the board will also post the to the specified offboard address.

The values in this field are used when writing the to system memory. The illustration below shows the format of this word:

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Bits 0-7 Address Modifier:

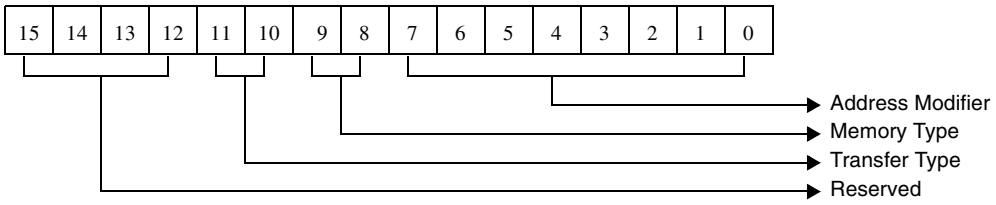


Figure 5-47. VME Transfer Type for Block Offboard Command Response

This byte is the VMEbus address modifier used for writing the to system memory. This byte is not changed by the board.

Bits 8-9 Memory Type:

This two-bit field specifies the width of the data transfer used to write to the offboard. Permitted values are as follows:

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	16-BIT TRANSFERS
1	0	32-BIT TRANSFERS
1	1	(RESERVED)

Figure 5-48. Memory Type Field For Offboard Command Response Block

Bits 10-11 Transfer Type:

This two-bit field specifies the type of transfer performed. Permitted values are as follows:

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INITIALIZE CONTROLLER
Command ID: 0x41

BIT 11	BIT 10	TRANSFER TYPE
0	0	NORMAL MODE
0	1	BLOCK MODE
1	0	(RESERVED)
1	1	VME D64 BLOCK

Figure 5-49. Transfer Type Field For Offboard Command Response Block

Bits 12-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Offboard Command Response Block Address (4 Bytes)

This field is intended for applications which use the board's offboard IOPB feature (see *Offboard IOPBs* in Chapter 6). This address is used to write the Command Response Block to host system memory. If this field and the Offboard Transfer Type field are both 0, the board will post IOPBs to the in Short I/O only.

Error Recovery Options (2 Bytes)

This field is used to enable error recovery options. The following options are supported:

- Freeze Work Queues on SCSI Reset
- Host Interrupt on SCSI Reset
- Report SCSI Error
- Freeze All on SCSI Reset

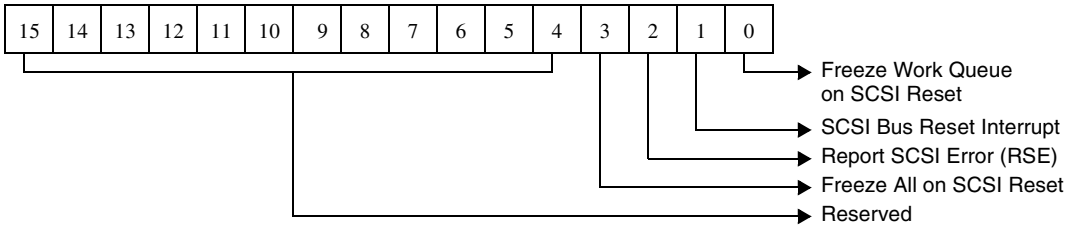


Figure 5-50. Error Recovery Options For Controller Initialization Block

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Bit 0 Freeze Work Queue On SCSI Bus Reset:

Setting this bit causes the board to freeze a work queue if a Reset occurs on the SCSI bus while a command from that work queue is active on the bus. With this feature enabled, the host "knows" the work queue is frozen if a command is returned from the queue with a SCSI bus reset error status. This allows the host to decide how to handle the SCSI reset before permitting new commands to be sent to the device. This is the preferred mode of operation. In general, this bit should only be cleared to maintain driver backward compatibility prior to implementation of this feature.

Bit 1 SCSI Bus Reset Interrupt:

Setting this bit causes the board to interrupt the host if a reset occurs on the SCSI bus while the board is idle. SCSI reset interrupts are generated when SCSI bus reset is detected. The SCSI reset bit in the Command Response Status Word (CRSW) is also set in the returned IOPB.

Bit 2 Report SCSI Errors:

Setting this bit causes the board to report non-recoverable SCSI errors via a controller error with the SCSI Error bit in the CRSW, providing additional diagnostic information about the nature of the error. After a non-recoverable SCSI error is reported, the SCSI channel may be returned to functional status by issuing a SCSI bus reset. When this bit is cleared, non-recoverable SCSI errors produce a controller panic, requiring a full controller re-initialization to return the system to functional status.

Bit 3 Freeze All on SCSI Bus Reset:

Setting this bit causes all work queues on a channel to be frozen in the event of a third-party SCSI bus reset.

Bits 4-12 Reserved:

These bits are reserved and must be cleared to 0 by the host.

SCSI Bus Reset Interrupt Vector/Level (2 Bytes)

This field specifies the interrupt level and vector that the board will use when reporting a SCSI bus reset. An interrupt will not be generated if the interrupt level is set to 0. However, the board will still report SCSI Bus Reset in the.

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INITIALIZE CONTROLLER
Command ID: 0x41

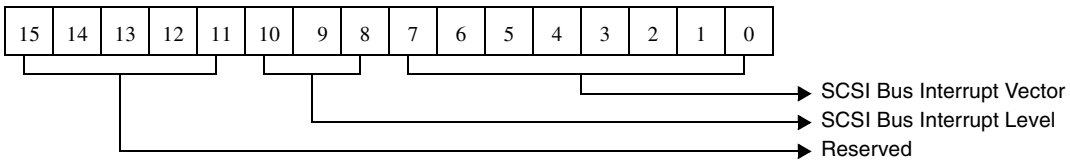


Figure 5-51. SCSI Bus Reset Interrupt Vector/Level for Controller Initialization Block

Bits 0-7 SCSI Bus Reset Interrupt Vector:

This byte is the VMEbus Interrupt Vector used by the board when reporting SCSI Bus Reset Interrupts.

Bits 8-10 SCSI Bus Interrupt Level:

This value specifies the VMEbus Interrupt Level used by the board when reporting the SCSI Bus Reset Interrupt.

Bits 11-15 Reserved:

Bits 11 through 15 are reserved and should be cleared to 0 by the host.

Synchronous Offset for Bus 0 (2 Bytes)

Referring to the SCSI-2 specification Synchronous Data Transfer Request table, this value is used for the REQ/ACK offset (byte 4) to set the maximum REQ/ACK offset that may be used on bus 0.

Synchronous Negotiation Rate for Bus 0 (2 Bytes)

Referring to the SCSI-2 Specification for Synchronous Data Transfer Request table, this value is used for byte 3. The transfer period to set the minimum transfer period in nanoseconds divided by 4 that may be used on bus 0.

Synchronous Offset for Bus 1 (2 Bytes)

Controls parameter for SCSI bus 1.

Synchronous Negotiation Rate for Bus 1 (2 Bytes)

Controls parameter for SCSI bus 1.

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INITIALIZE CONTROLLER
Command ID: 0x41

INITIALIZE CONTROLLER
Command ID: 0x41

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB of the command response for the Initialize Controller command:

Return Status (2 Bytes)

This field provides the return status of the command. Any non-zero value indicates an error code.

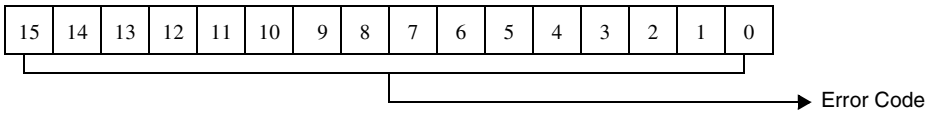


Figure 5-52. Return Status For Controller Initialization

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INITIALIZE WORK QUEUE

Command ID: 0x42

The Initialize Work Queue command is used to configure the work queues (Cougar II: 1 - 14, Cougar II Wide: 1 - 255). Each work queue must be initialized with a separate Initialize Work Queue command.

NOTE: Work Queue 0 is auto-initialized by the board upon power-up and cannot be reinitialized. This command must be issued through the Master Command Entry to Work Queue 0.

The format of the Initialize Work Queue IOPB is as follows:

WORD	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x42)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xD	RESERVED															
0xE	WORK QUEUE NUMBER															
0xF	WORK QUEUE OPTIONS															
0x10	NUMBER OF WORK QUEUE SLOTS															
0x11	UNIT ADDRESS															
0x12 & 0x13	COMMAND TIMEOUT															
0x14	RESERVED															

NOTES: Fields set in bold letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-53. Initialize Work Queue IOPB

The remainder of this section describes the function of each field in the Initialize Work Queue IOPB.

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INITIALIZE WORK QUEUE
Command ID: 0x42

INITIALIZE WORK QUEUE
Command ID: 0x42

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Initialize Work Queue command:

Command Code (2 Bytes)

This field must be set to 0x42 to execute the Initialize Work Queue command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

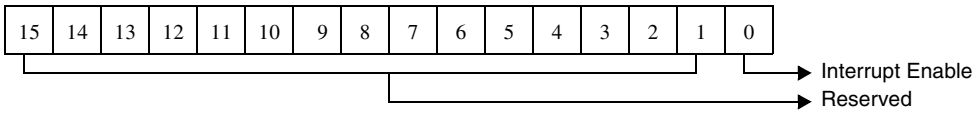


Figure 5-54. Command Options For Initialize Work Queue Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

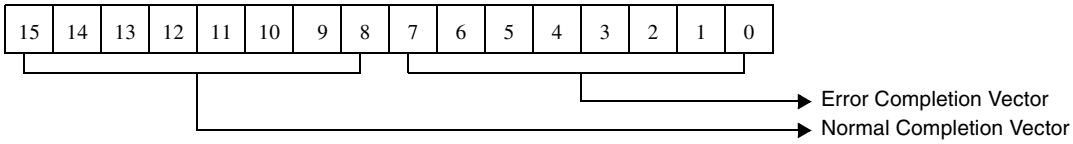


Figure 5-55. Normal/Error Completion Vector For Initialize Work Queue Command

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INITIALIZE WORK QUEUE
Command ID: 0x42

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

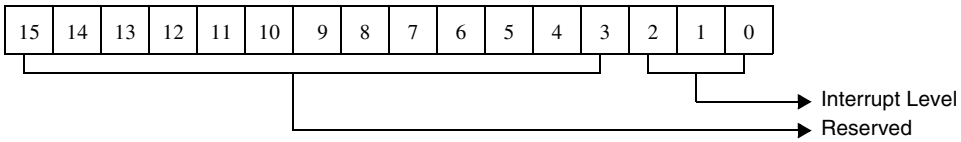


Figure 5-56. Interrupt Level For Initialize Work Queue Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, with a level of 0 is allowed only when interrupts are disabled by clearing the Interrupt Enable bit in the Command Options word.

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Work Queue Number (2 Bytes)

This number identifies which work queue to initialize. Each work queue must be assigned a unique number. Valid entries in this field are 0x1-0xE to initialize work queues 1-14, for Cougar II, and 0x1 -Oxff to initialize work queues 1 - 255 for Cougar II Wide.

Work Queue Options (2 Bytes)

This field is used to set a variety of options that apply ONLY to the work queue being initialized.

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INITIALIZE WORK QUEUE
Command ID: 0x42

INITIALIZE WORK QUEUE
Command ID: 0x42

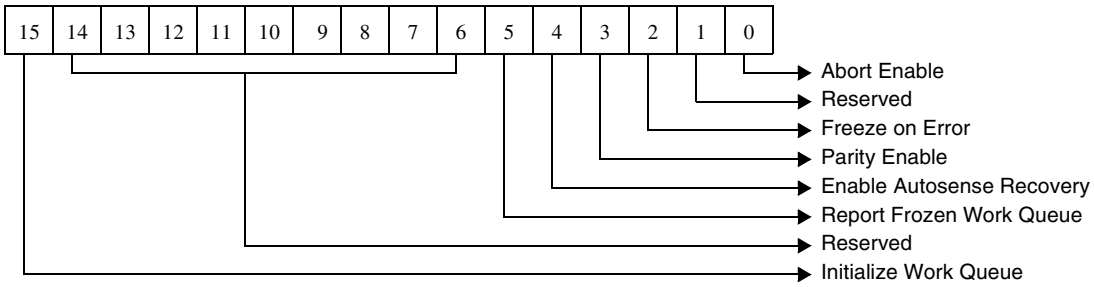


Figure 5-57. Work Queue Options For Initialize Work Queue Command

Bit 0 Abort Enable:

Setting this bit enables the board to abort all IOPBs in the work queue, and all IOPBs in the Command Queue destined for the work queue, when an IOPB from this queue completes with a SCSI Pass-Through error.

Clearing this bit disables the option. See Queue Entry Control Register, Abort Acknowledge bit.

Bit 1 Reserved:

This bit is reserved and must be cleared to 0 by the host.

Bit 2 Freeze on Error:

Setting this bit causes the queue to "freeze" if a SCSI Pass-Through IOPB sent to this queue fails to return a good status (0x0) in the Pass-Back status byte of the Return Status word.

When the host sees a command return from a work queue that has Freeze on Error enabled with a SCSI pass-through error, the host must unfreeze (thaw) the work queue after taking the error handling steps needed for that particular error.

The frozen work queue is thawed by selecting that work queue number in the Thaw Queue Register and then setting Bit 0 of that register. The board will clear the register to acknowledge the thawing of the work queue. The Thaw Work Queue Status Register is located in the Master Control/Status Block. For details on using the freeze work queue feature, see Chapter 6, Error Recovery Tools (Chapter 6).

Bit 3 Parity Enable:

The Parity Enable bit enables SCSI bus parity checking for commands issued from the work queue.

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INITIALIZE WORK QUEUE
Command ID: 0x42

Bit 4 Enable Autosense Recovery:

Setting this bit configures the board to send an automatic SCSI request sense command to a device, associated with this queue, from which a command is returned with a SCSI Check Condition in the pass-back status. The sense data is reported in the returned IOPB of the SCSI Pass-Through command that completed with a pass-through error.

Setting this bit takes precedence over the "Freeze on Error Option", in the Work Queue Options field.

Bit 5 Report Frozen Work Queue:

When this bit is set and a queue is frozen, the frozen queue status will be reported with the Queue Frozen bit set in the CRSW of the command response of the command causing the queue to freeze.

Bits 6-14 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 15 Initialize Work Queue:

The Initialize Work Queue bit causes the board to initialize the work queue even if it has previously been initialized. If commands are pending when the board attempts to execute an Initialize Work Queue command, the Initialize Work Queue IOPB will not be executed, and the IOPB will return with error status.

Number Of Slots (2 Bytes)

This field is retained for backward compatibility with the 4210 Jaguar. It is not used by the 4220, and will only be passed back in the command response for the Dump Work Queue Parameters command.

Unit Address

This field specifies the SCSI bus and the address of the target device.

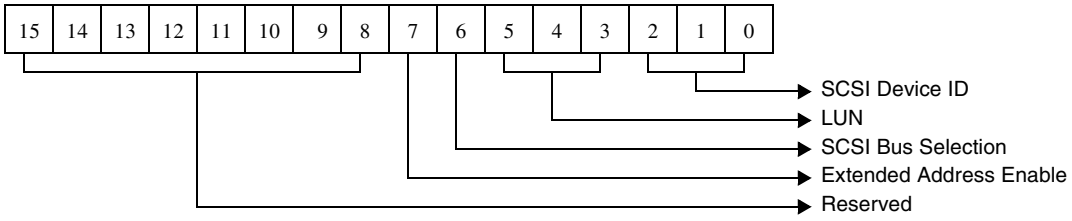


Figure 5-58. Initialize Work Queue Command

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INITIALIZE WORK QUEUE
Command ID: 0x42

INITIALIZE WORK QUEUE
Command ID: 0x42

W ***Extended Unit Address For SCSI-2 Wide Operation***

This field specifies the SCSI bus and the address of the target device for SCSI-2 Wide operation.

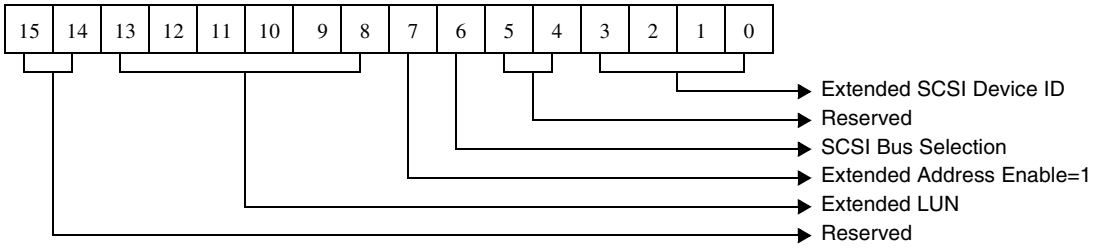


Figure 5-59. Extended Unit Address For Initialize Work Queue

Bits 0-3 Extended SCSI Device ID:

This 3-bit field contains the Extended SCSI ID used when addressing the target. This value may range from 0 to 15.

Bit 4-5 Reserved:

These bits are reserved and must be set to zero by the host.

Bit 6 SCSI Bus Selection:

This selects which of the two SCSI buses the board uses when executing the command. When this bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7 Extended Address Enable:

When this bit is set to 1, the LUN is taken from the 6-bit extended LUN field, and the SCSI device ID is taken from the 4-bit extended SCSI device ID field.

Bits 8-13 Extended LUN:

Setting Bit 7 enables the extension to both the LUN and the SCSI Device ID fields.

Bits 14-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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INITIALIZE WORK QUEUE
Command ID: 0x42

Command Timeout (2 Bytes)

This field specifies the maximum time that a command issued to this work queue should take to execute after the device has been selected, allowing each work queue a unique timeout value. The timeout period is from the successful completion of the selection phase until the completion of the command on the SCSI bus, including disconnect periods and is specified in increments of approximately 256 milliseconds. That is, a value of 0x1 in this field specifies a timeout period of approximately 256 milliseconds.

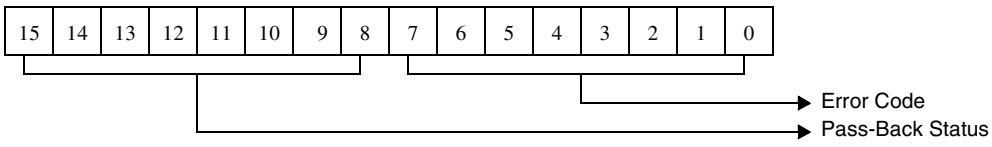
If the timeout value is non-zero, the board will notify the host of the command timeout by use of the Controller Error Interrupt. This interrupt returns an error status without returning the IOPB that caused the error. Bit 7 allows the host to determine the source of the error. Also, the data returned can be used to help determine the type of error that has occurred.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Initialize Work Queue command.

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code.



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INITIALIZE WORK QUEUE
Command ID: 0x42

INITIALIZE WORK QUEUE
Command ID: 0x42

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response. Any non-zero value is an error code. Appendix C contains a complete list of error codes.

Bits 8-15 Pass-Back Status:

This value is the SCSI status byte returned by the target device.

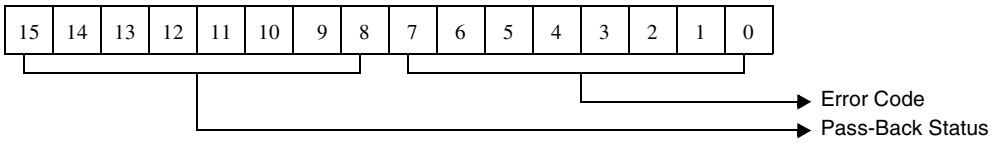


Figure 5-60. Pass Back Status For Initialize Work Queue

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DUMP INITIALIZATION PARAMETERS

Command ID: 0x43

The Dump Initialization Parameters command causes the board to report its current initialization/setup information to the host. This command is intended to be used primarily for diagnostic purposes.

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the IOPB for the Dump Initialization Parameters command is shown below:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x43)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6	RESERVED															
0x7	RESERVED				TT		MT		ADDRESS MODIFIER							
0x8	BUFFER ADDRESS															
0x9																
0xA	MAXIMUM TRANSFER LENGTH															
0xB																
0xC	RESERVED															
0xD																

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-61. Dump Initialize Parameters IOPB

The remainder of this section describes the function of each field in the Dump Initialization Parameters IOPB.

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DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Dump Initialization Parameters command:

Command Code (2 Bytes)

This field must be set to 0x43 to execute the Dump Initialization Parameters command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

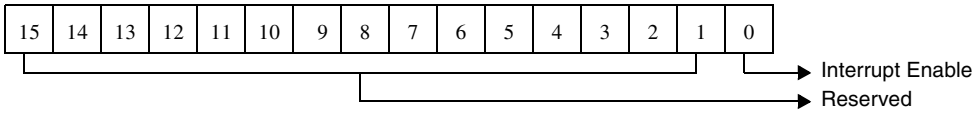


Figure 5-62. Command Options For Dump Initialization Parameters Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

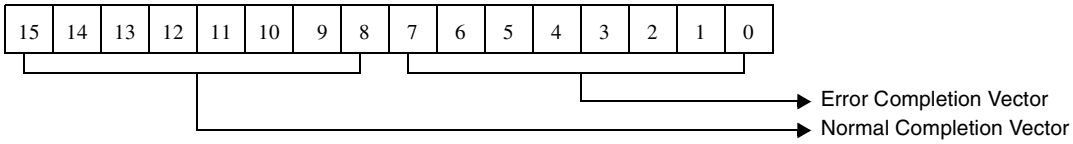


Figure 5-63. Normal/Error Completion Vector For Dump Initialization Parameters Commands

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DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

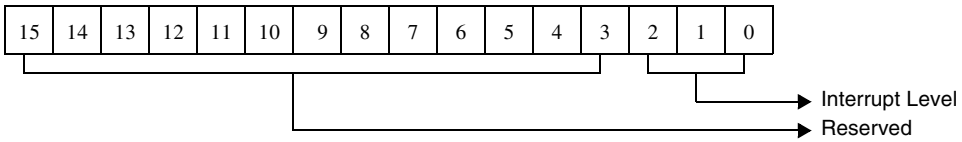


Figure 5-64. Interrupt Level For Dump Initialization Parameters Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Memory Type/Transfer Type/Address Modifier (2 Bytes)

This specifies the memory type and address modifier to be used for any VMEbus transfers associated with the Dump Initialization Parameters command.

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DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

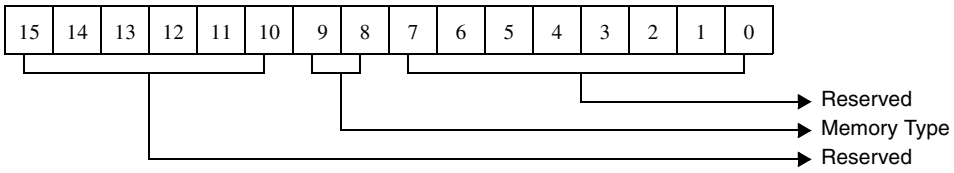


Figure 5-65. Memory/Transfer/Address Modifier For Dump Initialization Parameters Command

Bits 0-7 Address Modifier:

This byte must be cleared for the Dump Initialization Parameters command.

Bits 8-9 Memory Type:

The only valid entry in this 2-bit field is 0x3, indicating that the data for this command is located in Short I/O.

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	(RESERVED)
1	0	(RESERVED)
1	1	Data is contained in Short I/O

Figure 5-66. Memory Type (MT) Field For Dump Initialization Parameters Command

Bits 10-11 Transfer Type:

These bits must be cleared to 0.

Bits 12-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Buffer Address (4 Bytes)

This field specifies the offset into Short I/O in Host Usable Space at which the board is to start writing the initialization parameter list.

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DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	BUFFER ADDRESS														

Figure 5-67. Buffer Address For Dump Initialization Parameters Command

Maximum Transfer Length (4 Bytes)

This field specifies the maximum number of bytes that may be transferred by the command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	MAXIMUM TRANSFER LENGTH														

Figure 5-68. Maximum Transfer Length For Dump Initialization Parameters Command

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Dump Initialization Parameters command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

The board also writes the Initialization Parameters Block to the section of Short I/O specified by the host, as discussed below.

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DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

DUMP INITIALIZATION PARAMETERS
Command ID: 0x43

Initialization Parameters Block

When it executes the Dump Initialization Parameters command, the board writes the parameter list into Short I/O, starting at the offset provided in the Buffer Address field of the IOPB.

The parameter list has the same format as the Controller Initialization Block. For an explanation of the fields in the Initialization Parameters Block, please refer to the Controller Initialization Block (Figure 5-7).

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DUMP WORK QUEUE PARAMETERS

Command ID 0x44

The Dump Work Queue Parameters command causes the board to report the current parameters of an individual work queue to the host. The host provides the work queue number. Note that a work queue must be initialized before its parameters can be dumped.

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the IOPB for the Dump Work Queue Parameters command is shown below:

WORD	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x44)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xD	RESERVED															
0xE	WORK QUEUE NUMBER															
0xF	**WORK QUEUE OPTIONS**															
0x10	**NUMBER OF WORK QUEUE SLOTS**															
0x11	RESERVED															
0x12 & 0x13	**COMMAND TIMEOUT**															

NOTES: Fields set in bold letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-69. Dump Work Queue Parameter IOPB

The remainder of this section describes the function of each field in the Dump Work Queue Parameters IOPB.

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DUMP WORK QUEUE PARAMETERS
Command ID: 0x44

DUMP WORK QUEUE PARAMETERS
Command ID: 0x44

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Dump Work Queue Parameters command:

Command Code (2 Bytes)

This field must be set to 0x44 to execute the Dump Work Queue Parameters command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

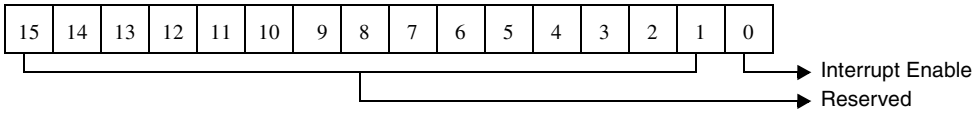


Figure 5-70. Command Options For Dump Work Queue Parameters Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

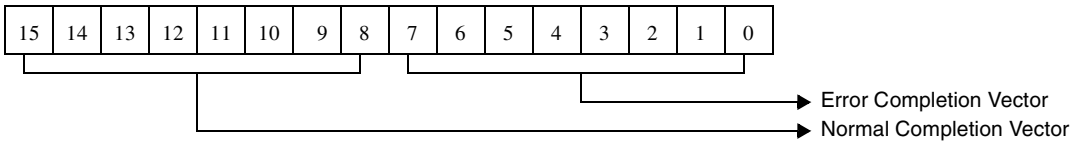


Figure 5-71. Normal/Error Completion For Dump Work Queue Parameters

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DUMP WORK QUEUE PARAMETERS
Command ID: 0x44

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

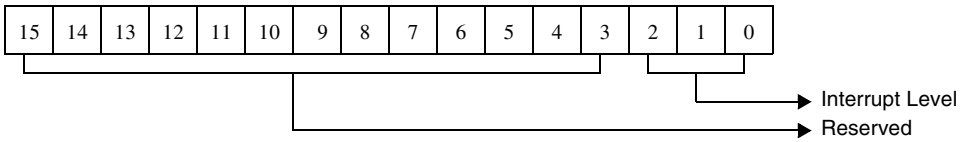


Figure 5-72. Interrupt Level For Dump Work Queue Parameters

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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DUMP WORK QUEUE PARAMETERS
Command ID: 0x44

DUMP WORK QUEUE PARAMETERS
Command ID: 0x44

W ***Work Queue Number (2 Bytes)***

This value may range from 0x1-0xE (work queues 1-14) for the Cougar II, and from 0x1-0xff (work queues 1-255) for the Cougar II Wide. If an uninitialized work queue is specified, the command will complete with an illegal parameter status.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Dump Work Queue Parameters command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

Work Queue Options (2 Bytes)

This field contains the work queue options specified by the host when it initialized the work queue.

Number Of Work Queue Slots (2 Bytes)

This field contains the number of work queue slots specified by the host when it initialized the work queue.

Command Timeout (4 Bytes)

This field contains the command timeout specified by the host when it initialized the work queue.

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BUS STATUS INQUIRY

Command ID: 0x45

The Bus Status Inquiry command returns the command tag of any IOPB currently executing on the selected SCSI bus. In addition, it returns the command tags of any in-progress IOPBs. An in-progress IOPB is one which has been sent to a device but is not completed yet. Information in the returned IOPB can be used to identify which IOPB and device is causing an error condition.

During execution of this command, the board will stop all internal operations so that the response will reflect the state of the board at the time the Bus Status Inquiry IOPB is executed.

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the Bus Status Inquiry IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x45)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0X5	INTERRUPT LEVEL															
0x6	**ACTIVE COMMAND TAG**															
0x7																
0x8 To 0xE	**BUSY COMMAND TAGS**															
0xF	BUS SELECTION / **BUSY COMMAND TAGS (cont.)**															
0x10 To 0x15	**BUSY COMMAND TAGS (cont.)**															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Note that word 0xF in the above IOPB is issued with a host-provided value, but returned with a board-provided value. Reserved fields must be cleared to 0 by the host.

Figure 5-73. Bus Status Inquiry IOPB

The remainder of this section describes the function of each field in the Bus Status Inquiry IOPB.

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Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Bus Status Inquiry command:

Command Code (2 Bytes)

This field must be set to 0x45 to execute the Bus Status Inquiry command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

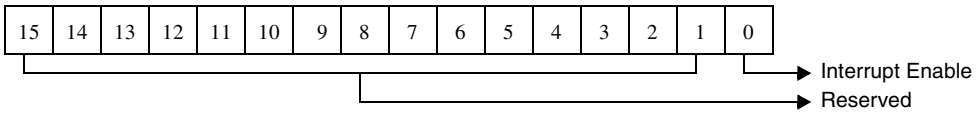


Figure 5-74. Command Options For Bus Status Inquiry Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

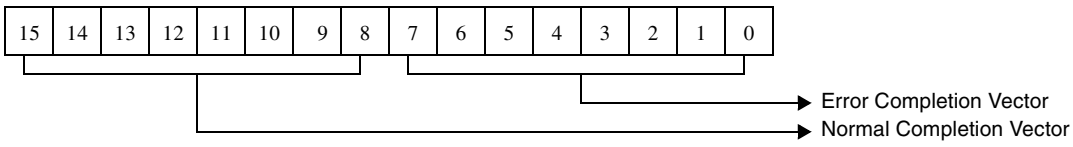


Figure 5-75. Normal/Error Completion Vector For Bus Status Inquiry Command

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BUS STATUS INQUIRY
Command ID: 0x45

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

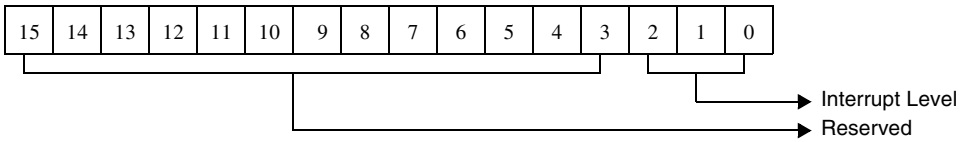


Figure 5-76. Interrupt Level For Bus Status Inquiry Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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BUS STATUS INQUIRY
Command ID: 0x45

BUS STATUS INQUIRY
Command ID: 0x45

Bus Selection (2 Bytes)

This field specifies which SCSI bus is the subject of the Bus Status Inquiry.

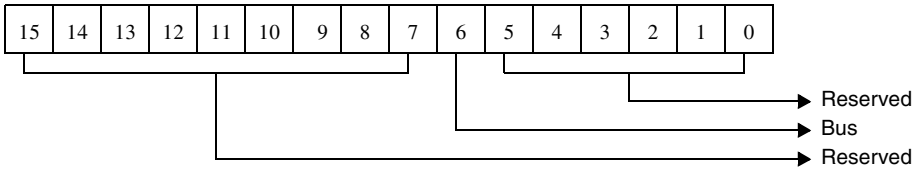


Figure 5-77. Bus Selection For Bus Status Inquiry Command

Bits 0-5 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 6 Bus:

Clearing this bit selects the primary SCSI bus (Channel 0). Setting the bit selects the secondary SCSI bus (Channel 1).

Bits 7-15 Reserved;

These bits are reserved and must be cleared to 0 by the host.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Bus Status Inquiry command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

Active Command Tag (4 Bytes)

The Active Command Tag field contains the command tag of a SCSI Pass-Through IOPB, if the command is being executed on the bus at the time that the Bus Status Inquiry is issued.

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BUS STATUS INQUIRY
Command ID: 0x45

Busy Command Tags

The Busy Command Tags fields will contain any other currently "in-progress" IOPBs that may not be able to complete due to the "hung" active command. There can be up to seven busy commands per channel (words 0x8—0x9, 0xA—0xB, 0xC—0xD, 0xE -0xF, 0x10—0x11, 0x12—0x13, 0x14—0x15).

NOTE: The host-provided value in word 0xF (Bus Selection) will be overwritten.

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COMMAND STATUS INQUIRY

Command ID: 0x46

The Command Status Inquiry IOPB returns the state of a previously issued IOPB based on the command tag field. If the IOPB specified by the command tag is active on the bus, information will be returned to help identify the state of the SCSI activity. The board will suspend hardware operations until the status of the command is found and posted.

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x46)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xF	RESERVED															
0x10	COMMAND TAG															
0x11																
0x12	**COMMAND STATUS CODE**															
0x13	**LAST COMMAND ISSUED**															
0x14	**PHASE SENSE**															
0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-78. Command Status Inquiry IOPB

The remainder of this section describes the function of each field in the Command Status Inquiry IOPB.

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COMMAND STATUS INQUIRY
Command ID: 0x46

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Command Status Inquiry:

Command Code (2 Bytes)

This field must be set to 0x46 to execute the Command Status Inquiry command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

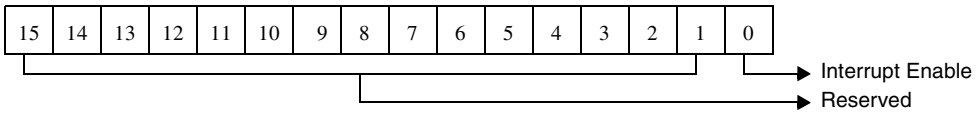


Figure 5-79. Command Options For Command Status Inquiry Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector /Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

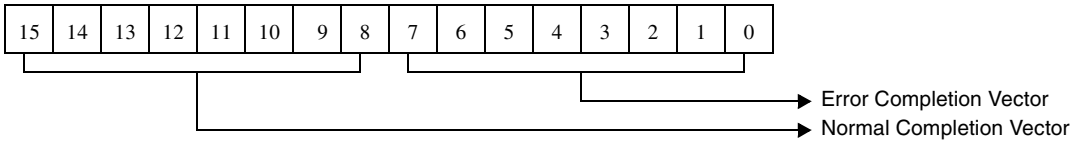


Figure 5-80. Normal/Error Completion Vector For Command Status Inquiry Command

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COMMAND STATUS INQUIRY
Command ID: 0x46

COMMAND STATUS INQUIRY
Command ID: 0x46

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

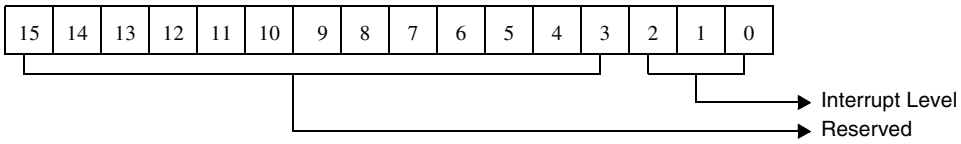


Figure 5-81. Interrupt Level For Command Status Inquiry Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Command Tag (4 Bytes)

This field specifies command tag of the IOPB.

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COMMAND STATUS INQUIRY
Command ID: 0x46

COMMAND STATUS INQUIRY
Command ID: 0x46

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	COMMAND TAG														

Figure 5-82. Command Tag For Command Status Inquiry

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Command Status Inquiry:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

Command Status Code (2 Bytes)

This field contains the returned command status. If the command is active, additional information is returned in the next 2 fields: Last Command Issued and Phase Sense.

Valid returned values for the Command Status Code are defined as follows:

CODE	EXPLANATION
0x0001	Command not found (command tag did not match)
0x0002	Command not in work queue (not executing yet)
0x0003	Command currently active (currently on SCSI bus)
0x0004	Command busy (currently disconnected)
0x0005	Command on Done Queue (The command is on the board's internal Done Queue and will have been received by the host before the response to the inquiry)
0x0006	Command in command queue (still in short I/O)

Figure 5-83. Returned Values for Command Status Code

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COMMAND STATUS INQUIRY
Command ID: 0x46

COMMAND STATUS INQUIRY
Command ID: 0x46

Last Command Issued:

This field indicates the last address given to the SCSI chip as a starting address.

Phase Sense:

This field indicates the current SCSI bus status. Valid returned values are shown below:

BIT #	EXPLANATION
7	Request
6	Acknowledge
5	Busy
4	Select
3	Attention
2	Message
1	Command/Data
0	Input/Output

Figure 5-84. Returned Values in Phase Sense Field

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READ/WRITE BUFFER

Command ID: 0x47

The Read/Write Buffer command provides compatibility for drivers and diagnostic routines that previously used the 4210 Jaguar Read/Write Buffer command. This command provides a mechanism to test the integrity of the DMA transfer mechanism of the board, without involving data transfers through the front end channel(s). This command must be issued through the Master Command Entry to work queue 0. The format of the IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	COMMAND CODE (0x47)															
0x01	OPTIONS															
0x02	RETURN STATUS															
0x03	RESERVED															
0x04	NORMAL VECTOR								ERROR VECTOR							
0x05	INTERRUPT LEVEL															
0x06	RESERVED															
0x07	ADDRESS MODIFIER															
0x08	BUFFER ADDRESS MSB															
0x09	BUFFER ADDRESS LSB															
0x0A	MAX LENGTH MSB															
0x0B	MAX LENGTH LSB															
0x0C	**ONBOARD BUFFER ADDRESS MSB**															
0x0D	**ONBOARD BUFFER ADDRESS LSB**															
0x0E	RESERVED															
0x0F	**ONBOARD BUFFER COUNT**															
0x10 To 0x15	RESERVED															

Figure 5-85. Read/Writer Buffer Command

The remainder of this section describes the function of each field in the Read/Write Buffer IOPB.

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READ/WRITE BUFFER
Command ID: 0x47

READ/WRITE BUFFER
Command ID: 0x47

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Read/Write Buffer command:

Command Code

The command code for this IOPB is 0x47.

W

This field contains the options for this command. The bits are defined as follows:

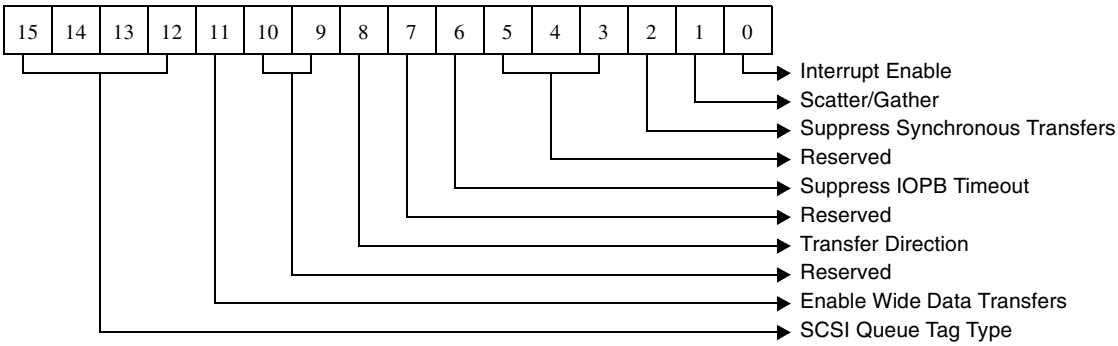


Figure 5-86. Command Options For Read/Write Buffer Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bit 8 VMEbus Transfer Direction:

When this bit is set, data will be transferred from the host to the board. When this bit is cleared, data will be transferred from the board to the host.

For a write to the VMEbus, the board will allocate and fill its local buffers with the amount of data specified. If sufficient buffers cannot be allocated, the IOPB will be returned with an error, and no data will be transferred.

For a read from the VMEbus, the board will attempt to return data previously transferred via the write command. If less data has been written than requested by the read command, the data that exists will be transferred, and the IOPB returned with a Transfer Length Exception.

Normal Error Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

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READ/WRITE BUFFER
Command ID: 0x47

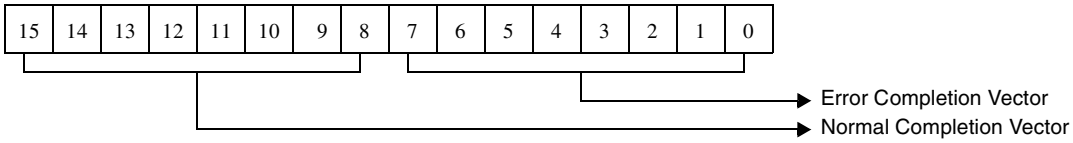


Figure 5-87. Normal/Error Completion Vector For Read/Write Buffer Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

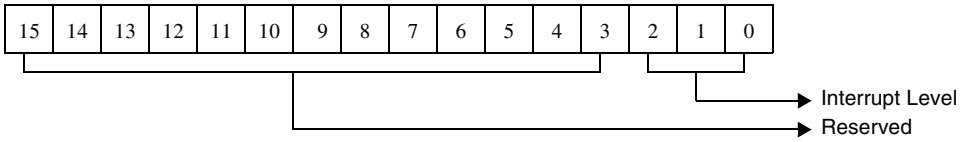


Figure 5-88. Interrupt Level For SCSI Pass-Through Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed with a level of 0 allowed only when interrupts are disabled by clearing the interrupt enable bit in the Command Options word.

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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READ/WRITE BUFFER
Command ID: 0x47

READ/WRITE BUFFER
Command ID: 0x47

VME Transfer Type (2 Bytes)

This field specifies the address modifier, memory type, and transfer type to be used for all VMEbus transfers associated with the command.

NOTE: As a slave, the board responds to either 0x2D *and* 0x29, or 0x2D VME address modifiers only. This depends on how the address modifier jumpers are set onboard. For a description of these jumpers, refer to chapter 2. As a master, the board will use whatever address modifier is in the IOPB. It is not checked. Some memory systems may not support all of the options discussed for this field.

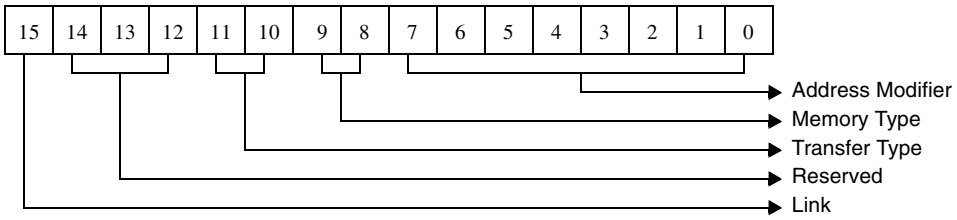


Figure 5-89. VME Transfer Types For Read/Write Buffer Command

Bits 0-7 Address Modifier:

This byte specifies the address modifier used by the board for all VMEbus data transfers associated with this command.

Bits 8-9 Memory Type:

This 2-bit field specifies the width of the data transfers. Permitted values are shown below.

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	16-bit transfers
1	0	32-bit transfers

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READ/WRITE BUFFER
Command ID: 0x47

READ/WRITE BUFFER
Command ID: 0x47

Bits 10-11 Transfer Type:

This 2-bit field specifies the type of data transfer to be performed. Permitted values are shown below.

BIT 11	BIT 10	TRANSFER TYPE
0	0	NORMAL TYPE
0	1	BLOCK MODE
1	0	(RESERVED)
1	1	VME D64 BLOCK

Bits 12-14 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Buffer Address (4 Bytes)

This field specifies the address at which the board will begin the data transfer. If the board is addressing system memory, the value in the field is a VMEbus address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW LSW	BUFFER ADDRESS														

Figure 5-90. Buffer Address For Read/Write Buffer Command

Maximum Transfer Length

This field specifies the maximum number of bytes that may be transferred by the command. When multiple read and write commands are interspersed, the data stream will resemble a FIFO. No partial buffers will be written back; an error will be returned.

Note: Consistent block sizes, in multiples of 2K bytes, should be used for both reads and writes.

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READ/WRITE BUFFER
Command ID: 0x47

READ/WRITE BUFFER
Command ID: 0x47

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB of the command response for the SCSI Pass-Through command.

Return Status (2 Bytes)

This field provides the return status for the command.

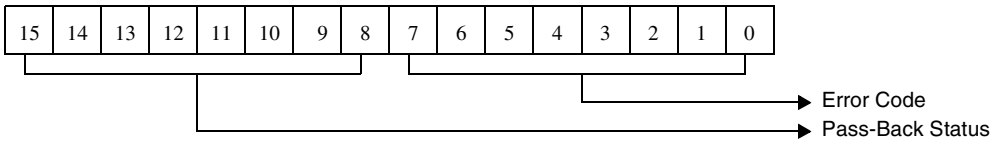


Figure 5-91. Return Status For Read/Write Buffer Command

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response. Any non-zero value is an error code. Appendix C contains the error codes.

POSSIBLE ERRORS		
0x19	ILLEGAL IOPB PARAMETER	COUNT IS NOT A MULTIPLE OF 2K BYTES, OR MORE DATA WAS REQUESTED TO BE WRITTEN THAN COULD BE ACCOMMODATED BY THE BOARD'S INTERNAL BUFFER.
0x20	VMEbus BUS ERROR	DATA CANNOT BE TRANSFERRED BACK TO THE HOST. THIS MAY LIKELY BE CAUSED BY REQUESTING A READ FOR WHICH NO WRITE HAS OCCURRED.
0x34	TRANSFER COUNT EXCEPTION	INSUFFICIENT DATA EXISTS TO SATISFY A READ REQUEST.

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READ/WRITE BUFFER
Command ID: 0x47

Onboard Buffer Address

This field will contain the address of the first buffer that was returned. For requests larger than 2K, multiple, non-contiguous buffers will be used.

Onboard Buffer Count

This field will contain the number of buffers used to satisfy the read or write request.

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CANCEL COMMAND TAG

Command ID: 0X48

The Cancel Command Tag IOPB cancels the execution of a previously issued IOPB, based on the command tag specified in the Cancel Command Tag IOPB. Issuing the command causes the board to find and cancel the *first* command tag that matches the one given in the IOPB. If multiple IOPBs exist with the same command tag, only the first one found will be canceled. If the board is unable to locate a command whose tag matches the one in the IOPB, it will return the Cancel Command Tag IOPB with an error.

This command must be issued through the Master Command Entry to Work Queue 0.

If an IOPB is canceled and subsequent SCSI activity attempts to complete the command, the board will return a controller error indicating that a device has connected for which there is no IOPB.

NOTE: Use of this command implies that the host uses unique command tags for all IOPBs on the board.

The format of the Cancel Command Tag IOPB is shown below.

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x48)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xF	RESERVED															
0x10	COMMAND TAG															
0x11																
0x12 To 0x15	RESERVED															

NOTES Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-92. Cancel Command Tag IOPB

The remainder of this section describes the function of each field in the Cancel Command Tag IOPB.

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CANCEL COMMAND TAG
Command ID: 0x48

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Cancel Command Tag command:

Command Code (2 Bytes)

This field must be set to 0x48 to execute the Cancel Command Tag command

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

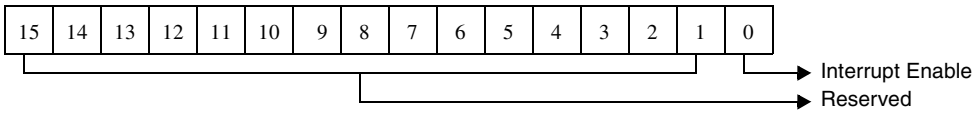


Figure 5-93. Command Options For Cancel Command Tag Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

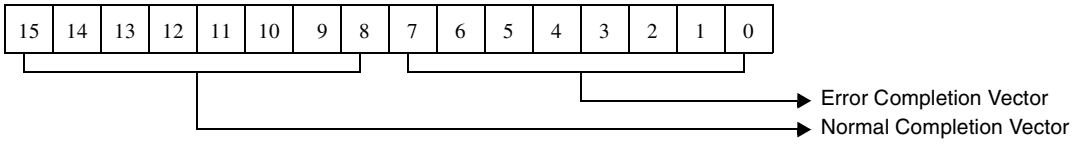


Figure 5-94. Normal/Error Completion Vector For Cancel Command Tag Command

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CANCEL COMMAND TAG
Command ID: 0x48

CANCEL COMMAND TAG
Command ID: 0x48

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

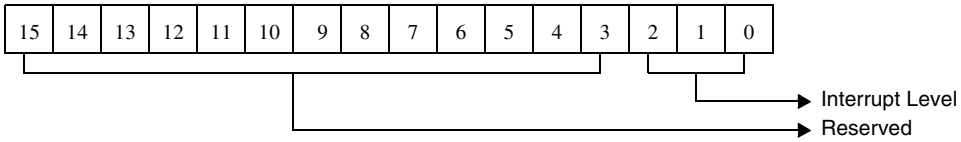


Figure 5-95. Interrupt Level For Cancel Command Tag Command

Bits 0-2 Interrupt Level (LVL):

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Command Tag (4 Bytes)

This field specifies command tag of the IOPB to be canceled.

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CANCEL COMMAND TAG
Command ID: 0x48

CANCEL COMMAND TAG
Command ID: 0x48



Figure 5-96. Command Tag For Cancel Command Tag Command

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Cancel Command Tag command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

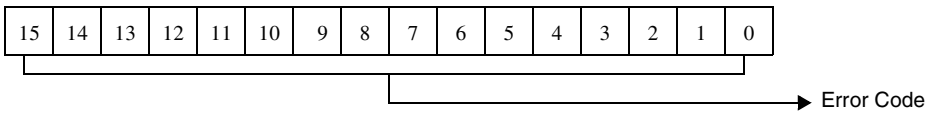


Figure 5-97. Return Status For Cancel Command Tag

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FLUSH WORK QUEUE

Command ID: 0X49

The Flush Work Queue command flushes all commands that have been placed in the work queue, as well as any commands in the Command Queue destined for the work queue. This command flushes only the specified work queue and, optionally will report completion of each entry in the queue.

This command must be issued through the Master Command Entry to Work Queue 0.

At the completion of the Flush Work Queue command, the number of entries flushed from the queue will be returned. The returned IOPB will also report whether any commands were "In Progress" when the Flush Work Queue command was executed.

If any of the flushed commands are "In Progress", it may be necessary to reset the SCSI bus in order to clear the effects of the command with respect to the target. To do so, issue a Reset SCSI Bus IOPB.

The format of the IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x49)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xD	RESERVED															
0xE	WORK QUEUE NUMBER															
0xF	SIP	PIP	**NUMBER OF ENTRIES FLUSHED**													

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host. Flush Work Queue IOPB

The remainder of this section describes the function of each field in the Flush Work Queue IOPB.

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FLUSH WORK QUEUE
Command ID: 0x49

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Flush Work Queue command:

Command Code (2 Bytes)

This field must be set to 0x49 to execute the Flush Work Queue command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

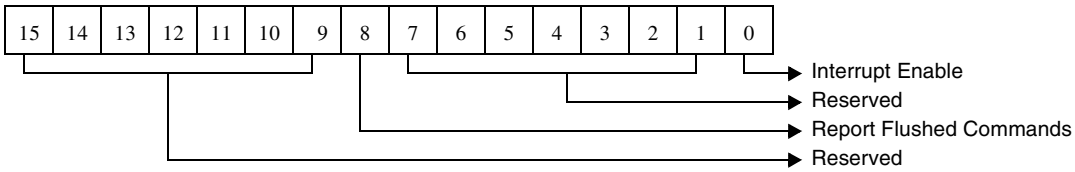


Figure 5-98. Command Options For Flush Work Queue Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt. Note that it is not necessary to enable this bit in order to report flushed commands.

Bits 1-7 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 8 Report Flushed Commands:

Setting this bit causes the board to report each command as it is flushed with a Command Complete Interrupt and an Error Status. Clearing the bit disables this function.

NOTE: Only the commands that have the Interrupt Enable bit set in the Command Options word of their individual IOPBs will generate an interrupt as they are flushed.

Bits 9-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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FLUSH WORK QUEUE
Command ID: 0x49

FLUSH WORK QUEUE
Command ID: 0x49

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

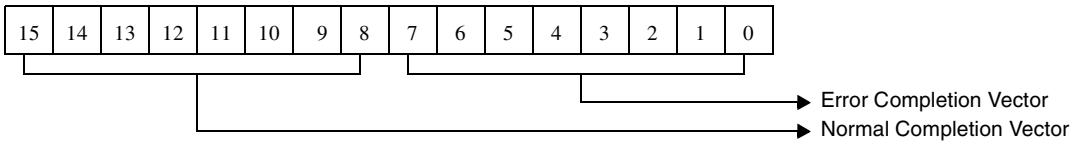


Figure 5-99. Normal/Error Completion Vector For Flush Work Queue Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

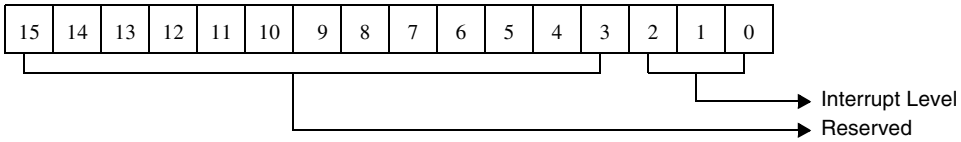


Figure 5-100. Interrupt Level For Flush Work Queue Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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FLUSH WORK QUEUE
Command ID: 0x49

Work Queue Number (2 Bytes)

This is the number of the work queue to be flushed.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Flush Work Queue command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains error codes.

Number Of Commands Flushed/In Progress (2 Bytes)

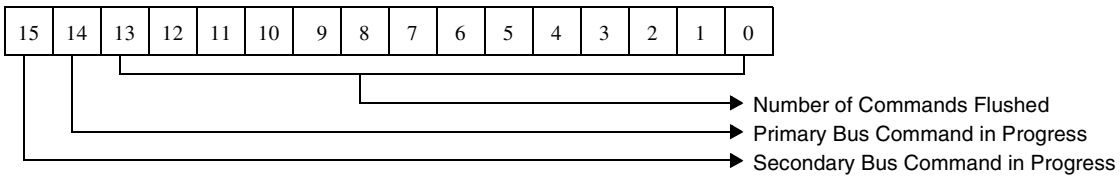


Figure 5-101. Commands Flushed In Progress Commands

Bits 0-13 Numbers of Entries Flushed:

This is the number of entries that were flushed from the work queue.

Bit 14 Primary Bus (Channel 0) Command In Progress:

The board sets this bit in the returned IOPB when an In-Progress command is present on the primary SCSI bus. There can never be more than one In-Progress command for any one work queue, but because the SCSI bus allows targets to disconnect, there can be multiple In-Progress commands on each SCSI bus.

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FLUSH WORK QUEUE
Command ID: 0x49

FLUSH WORK QUEUE
Command ID: 0x49

Bit 15 Secondary Bus (Channel 1) Command In Progress:

The board sets this bit in the returned IOPB when an In-Progress command is present on the secondary SCSI bus.

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INITIALIZE PRINTER PORT

Command ID: 0X4A

The Initialize Printer Port command is used to configure the printer port for the interface being used (Dataproducts or Centronics). In addition, it enables/disables status change interrupts.

The Initialize Printer Port command can be issued at any time to reset the printer port. The command is issued with the reset bit set to clear the printer port hardware. It should never be necessary to reset the hardware.

The command may also be issued at any time to assert a buffer clear to the printer. Since the time required for holding this signal varies from printer to printer, the board will leave the line set until the host issues another Initialize Printer Port command with the bit cleared.

NOTE: The vector used for status change interrupts is stored in word 0x2 of the Controller Initialization Block (the lower byte of the Controller Normal Completion Level/Vector field).

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the Initialize Printer Port IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x4A)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xD	RESERVED															
0xE	PRINTER OPTIONS															
0xF To 0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-102. Initialize Printer Port IOPB

The remainder of this section describes the function of each field in the Initialize Printer Port IOPB.

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INITIALIZE PRINTER PORT
Command ID: 0x4A

INITIALIZE PRINTER PORT
Command ID: 0x4A

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Initialize Printer Port command:

Command Code (2 Bytes)

This field must be set to 0x4A to execute the Initialize Printer Port command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

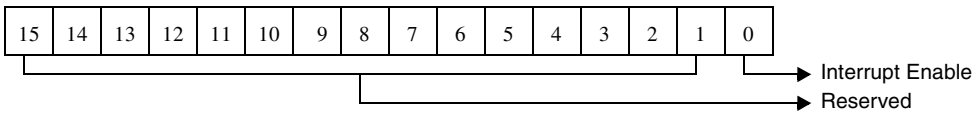


Figure 5-103. Command Options For Initialize Printer Port Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

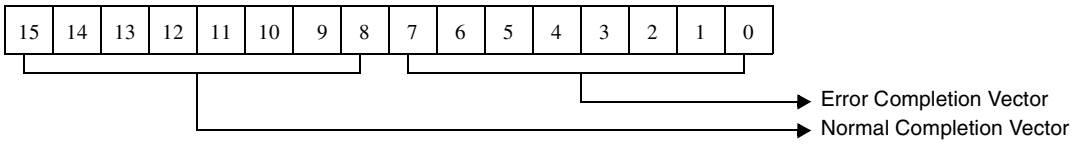


Figure 5-104. Normal/Error Completion Vector For Initialize Printer Port

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INITIALIZE PRINTER PORT
Command ID: 0x4A

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

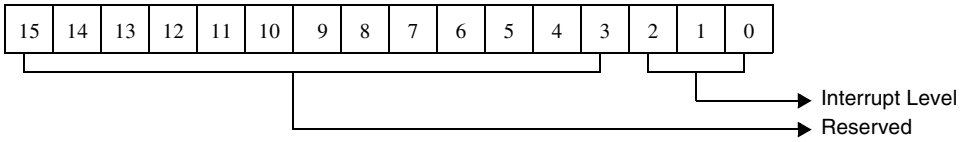


Figure 5-105. Interrupt Level For Initialize Printer Port Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Printer Options (2 Bytes)

The field the available options for the command:

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INITIALIZE PRINTER PORT
Command ID: 0x4A

INITIALIZE PRINTER PORT
Command ID: 0x4A

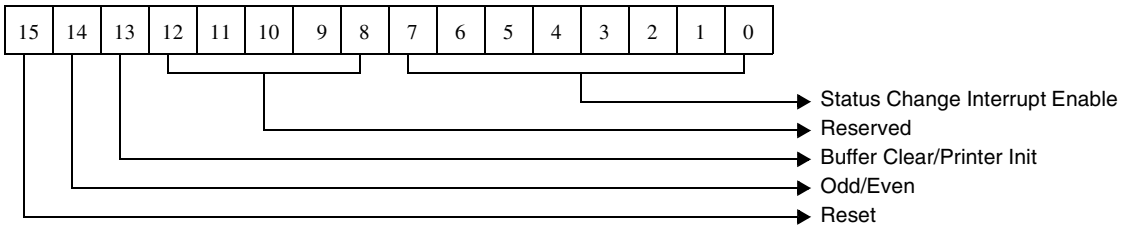


Figure 5-106. Printer Options For Initialize Printer Port Command

Bits 0-7 Status Change Interrupt Enable:

This field is used to enable interrupts from the printer status lines which the host is to monitor. To enable a specific status line, set the appropriate bit. The field's bit definitions vary depending the printer type, as listed below:

Dataproducts Printers:	Centronics Printers:
Bit 7 - Reserved - 0	Bit 7 - Reserved - 0
Bit 6 - Reserved - 0	Bit 6 - Reserved - 0
Bit 5 - Reserved - 0	Bit 5 - Reserved - 0
Bit 4 - Reserved - 0	Bit 4 - Reserved - 0
Bit 3 - Cable On	Bit 3 - Reserved - 0
Bit 2 - Parity Error	Bit 2 - Paper Empty
Bit 1 - Online	Bit 1 - Select
Bit 0 - Ready	Bit 0 - Fault

NOTE: These signals are active high.

Figure 5-107. Printer Status Change Interrupt Field

Bits 8-12 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 13 Buffer Clear/Printer Init:

Issuing the Initialize Printer Port command with this bit set causes the board to assert a Buffer Clear to a Dataproducts printer or a Print Init to a Centronics printer.

NOTE: After using Bit 13 to issue a Buffer Clear/Print Init instruction, the host must issue another Initialize Printer Port command with this bit cleared to return to normal printer operations.

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INITIALIZE PRINTER PORT
Command ID: 0x4A

Bit 14 Odd/Even:

This bit applies to **Dataproducts printers only**. It specifies the parity polarity, as follows:

0 = Even Parity
1 = Odd Parity

Bit 15 Reset:

Setting this bit set causes the board to reset the printer port. The port will be ready to receive new print commands after the completion status has been returned to the host.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB, of the command response, for the Initialize Printer Port command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

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RESTART CONTROLLER

Command ID: 0x4B

The Restart Controller command provides a method of resetting the controller and bypassing the power-up diagnostics. This command is analogous to a soft reset that tells the board to clear all current operations.

The first action the board takes is to reset the SCSI ports. It then flushes all internal commands, with the exception of the Restart Controller command. Next, the Command Queue pointer is reset to the base of the Command Queue. Finally, the Restart Controller command completion is returned to the Command Response Block. All Controller Initialization Block and work queue parameters remain intact. The host is responsible for resulting its Command Queue pointers.

This command must be issued through the Master Command Entry to Work Queue 0.

NOTE: It may be necessary for the host to issue a Request Sense to on-line devices after executing the Restart Controller command. This depends on what the devices require after a SCSI bus reset. Consult your device manuals for details.

The format of the Restart Controller IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x4B)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-108. Restart Controller IOPB

The remainder of this section describes the function of each field in the Restart Controller IOPB.

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RESTART CONTROLLER
Command ID: 0x4B

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Restart Controller command:

Command Code (2 Bytes)

This field must be set to 0x4B to execute the Restart Controller command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

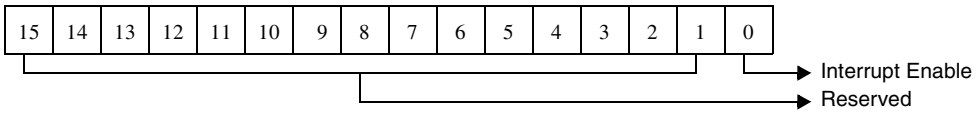


Figure 5-109. Command Options For Restart Controller Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

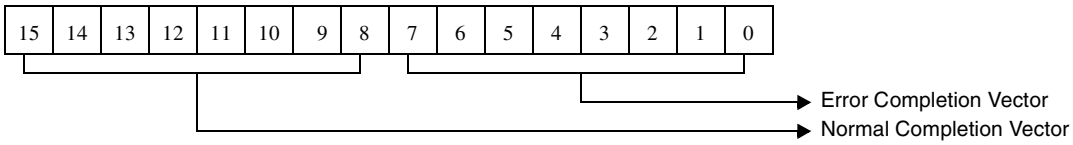


Figure 5-110. Normal/Error Completion for Restart Controller Command

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RESTART CONTROLLER
Command ID: 0x4B

RESTART CONTROLLER
Command ID: 0x4B

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

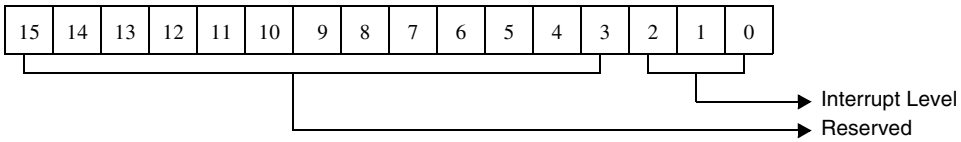


Figure 5-111. Interrupt Level For Restart Controller Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the Jaguar to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB of the command response, for the Restart Controller command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains error codes.

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DEVICE REINITIALIZE

Command ID: 0x4C

The Device Reinitialize command clears the first connection (synchronous and wide negotiation state) of a device. This causes the board to re-negotiate the synchronous transfer rate on the next selection to the target. This command is only necessary when a device has been disconnected from the bus or power removed from a device. If the device has been previously negotiated to Wide, the next command issued to the device, after the Device Reinitialize command, should have the Wide Options bit set in the IOPB command option field.

The format of the Device Reinitialize IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x4C)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xE	RESERVED															
0xF	UNIT ADDRESS															
0x10 To 0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-112. Device Reinitialize IOPB

The remainder of this section describes the function of each field in the Device Reinitialize IOPB.

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Device Reinitialize command:

Command Code (2 Bytes)

This field must be set to 0x4C to execute the Device Reinitialize command.

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RESTART CONTROLLER
Command ID: 0x4B

RESTART CONTROLLER
Command ID: 0x4B

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

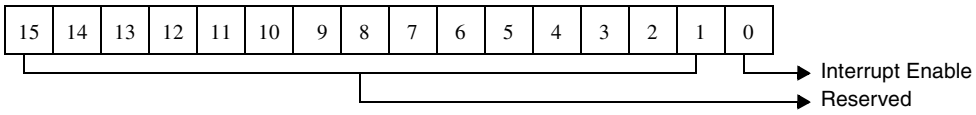


Figure 5-113. Command Options For Device Reinitialize Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

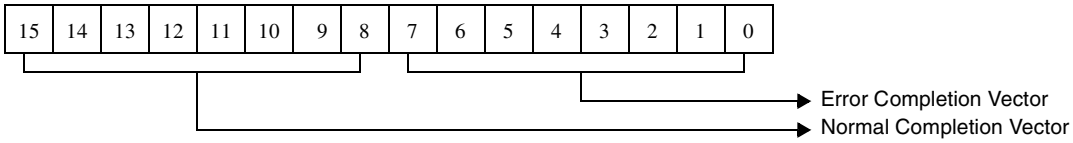


Figure 5-114. Normal/Error Completion Vector For Device Reinitialize Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

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DEVICE REINITIALIZE
Command ID: 0x4C

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

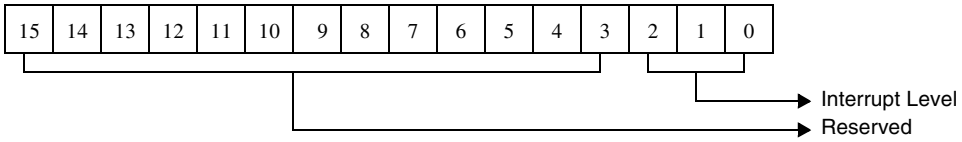


Figure 5-115. Interrupt Level For Device Reinitialize Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Unit Address (2 Bytes)

This field specifies the SCSI bus and the address of the target device.

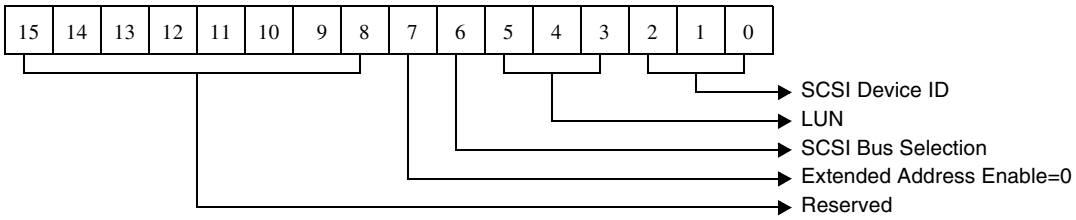


Figure 5-116. Unit Address For Device Reinitialize Command

Bits 0-2 SCSI Device ID (SCSI ID):

These bits contain the SCSI ID that is used when addressing the target. This value may range from 0 to 7.

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DEVICE REINITIALIZE
Command ID: 0x4C

DEVICE REINITIALIZE
Command ID: 0x4C

Bits 3-5 Logical Unit Number (LUN):

The SCSI Logical Unit Number will be defined in these three bits. Refer to ***American National Standard Institute X3.131-199X*** for a detailed description of Logical Unit Numbers.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the board uses when executing the command. When the BUS bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7: Extended Address Enable

Normal addressing is used when this bit is set to zero. Extended addressing is enabled when this bit is set to 1.

Bits 8-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

NOTE: When bit 7 is cleared bits 8-15 are reserved.

Extended Unit Address (2 Bytes)

This field specifies the SCSI bus and the address of the target device.

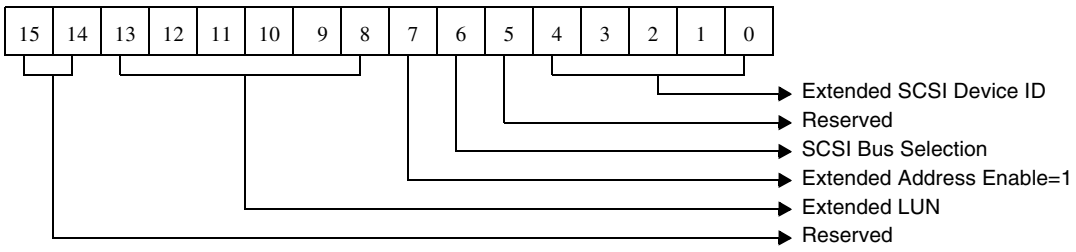


Figure 5-117. Extended Unit Address For Device Reinitialize Command

Bits 0-4 SCSI Device ID (SCSI ID):

These bits contain the SCSI ID that is used when addressing the target. This value may range from 0 to 31.

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DEVICE REINITIALIZE
Command ID: 0x4C

Bit 5 Reserved:

This bit is reserved and must be set to zero by the host.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the board uses when executing the command. When the BUS bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7 Extended Address Enable:

Setting this bit enables the extensions to both the LUN's and the SCSI ID. When this bit is set (1), the SCSI device ID shall be extended by two bits into the old LUN field. Bits 0-4 will now be utilized for the SCSI device ID.

Bits 8-13 Extended LUN (EXT LUN):

The LUN will be taken from the 6 bit field Extended LUN.

Bits 14-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Device Reinitialize command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

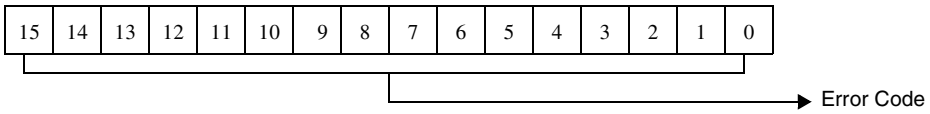


Figure 5-118. Return Status For Device Reinitialize

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ISSUE BUS DEVICE RESET MESSAGE

Command ID: 0x4D

The Issue Bus Device Reset Message command causes the board to issue a SCSI Bus Device Reset message to the selected SCSI device. This command enables the host to reset individual devices on the bus. The host should issue this command after insuring that no commands are currently being executed on this device. The Bus Device Reset message is sent from the initiator to direct a target to clear all current commands on a SCSI device. This message forces the SCSI device to an initial state with no operations pending for any initiator. Upon recognizing this message, the target goes to the Bus Free phase. The device must be able to respond to selection and receive message bytes.

This command must be issued through the Master Command Entry to Work Queue 0.

Note: It may be necessary for the host to issue a Request Sense to on-line devices after executing an Issue Bus Device Reset Message IOPB. This depends on what the devices require after a SCSI bus reset. Consult your device manuals for details.

The format of the IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x4D)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xE	RESERVED															
0xF	UNIT ADDRESS															
0x10 To 0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-119. Issue Bus Device Reset Message IOPB

The remainder of this section describes the function of each field in the Issue Bus Device Reset Message IOPB.

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ISSUE BUS DEVICE RESET MESSAGE
Command ID: 0x4D

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Issue Bus Device Reset Message command:

Command Code (2 Bytes)

This field must be set to 0x4D to execute the Issue Bus Device Reset Message command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

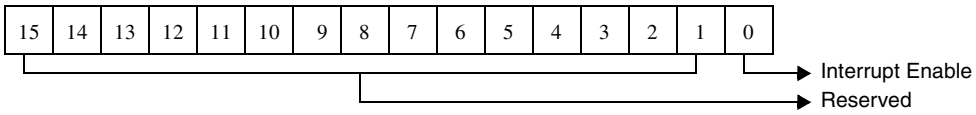


Figure 5-120. Command Options For Issue Bus Device Reset Message Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

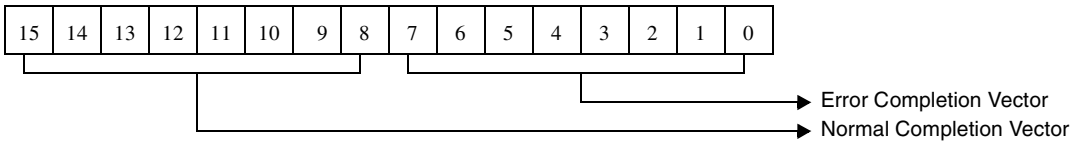


Figure 5-121. Normal/Error Completion For Issue Bus Device Message

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ISSUE BUS DEVICE RESET MESSAGE
Command ID: 0x4D

ISSUE BUS DEVICE RESET MESSAGE
Command ID: 0x4D

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

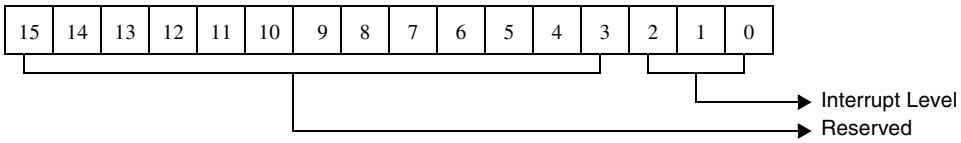


Figure 5-122. Interrupt Level For Issue Bus Reset Message Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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Unit Address (2 Bytes)

This field specifies the SCSI bus and the address of the target device.

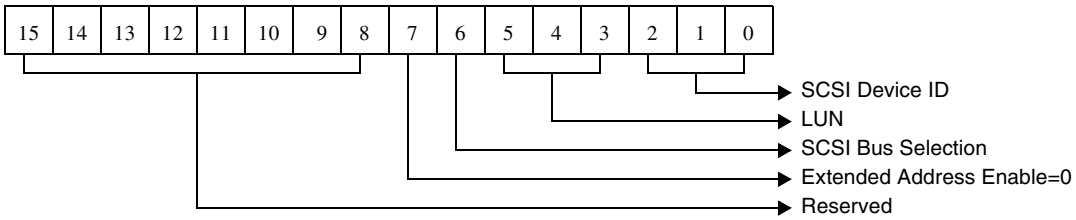


Figure 5-123. Unit Address For Issue Bus Device Reset Message Command

Bits 0-2 SCSI Device ID (SCSI ID):

These bits contain the SCSI ID that is used when addressing the target. This value may range from 0 to 7.

Bits 3-5 Logical Unit Number (LUN):

The SCSI Logical Unit Number will be defined in these three bits. Refer to ***American National Standard Institute X3.131-199X*** for a detailed description of Logical Unit Numbers.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the board uses when executing the command. When the BUS bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7: Extended Address Enable

Normal addressing is used when this bit is set to zero.

Bits 8-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

NOTE: When bit 7 is cleared bits 8-15 are reserved.

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ISSUE BUS DEVICE RESET MESSAGE **ISSUE BUS DEVICE RESET MESSAGE**
Command ID: 0x4D Command ID: 0x4D

W ***Extended Unit Address (2 Bytes)***

This field specifies the SCSI bus and the address of the target device.

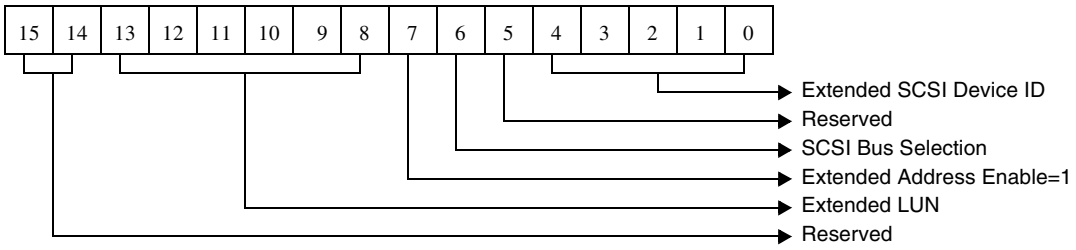


Figure 5-124. Extended Unit Address For SCSI Target Device

Bits 0-4 SCSI Device ID (SCSI ID):

These bits contain the SCSI ID that is used when addressing the target. This value may range from 0 to 31.

Bit 5 Reserved:

This bit is reserved and must be set to zero by the host.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the board uses when executing the command. When the BUS bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7 Extended Address Enable:

Setting this bit enables the extensions to both the LUN's and the SCSI ID. When this bit is set (1), the SCSI device ID shall be extended by two bits into the old LUN field. Bits 0-4 will now be utilized for the SCSI device ID.

Bits 8-13 Extended LUN (EXT LUN):

The LUN will be taken from the 6 bit field Extended LUN.

Bits 14-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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ISSUE BUS DEVICE RESET MESSAGE
Command ID: 0x4D

ISSUE BUS DEVICE RESET MESSAGE
Command ID: 0x4D

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Issue Bus Device Reset Message command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

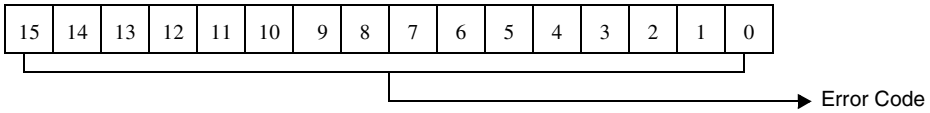


Figure 5-125. Return Status For Device Reset

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ISSUE ABORT MESSAGE

Command ID: 0x4E

Issue Abort Message command causes the board to issue a SCSI Abort message to the selected SCSI device. An Abort message is sent from the initiator to direct a target to clear the present operation. If a logical unit has been identified, all pending status for this initiator is cleared from the affected logical unit, and the target goes to the Bus Free phase. Pending data and status for other initiators is not cleared. If a logical unit has not been identified, the target goes to the Bus Free phase. No status or ending message is sent for the operation.

It is not an error to issue this message to a logical unit that is not currently performing an operation for the initiator. This command can be used to terminate an operation that is no longer required (killing a Format command to a drive, for example).

This command must be issued through the Master Command Entry to Work Queue 0.

The format of the Issue Abort Message IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND CODE (0x4E)															
0x1	COMMAND OPTIONS															
0x2	**RETURN STATUS**															
0x3	RESERVED															
0x4	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x5	INTERRUPT LEVEL															
0x6 To 0xE	RESERVED															
0xF	UNIT ADDRESS															
0x10 To 0x15	RESERVED															

NOTES: Fields set in bold capital letters are returned values. All other values are host provided. Reserved fields must be cleared to 0 by the host.

Figure 5-126. Issue Abort Message IOPB

The remainder of this section describes the function of each field in the Issue Abort Message IOPB.

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ISSUE ABORT MESSAGE
Command ID: 0x4E

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Issue Abort Message command:

Command Code (2 Bytes)

This field must be set to 0x4E to execute the Issue Abort Message command.

Command Options (2 Bytes)

This field contains the options for this command. The bits are defined as follows:

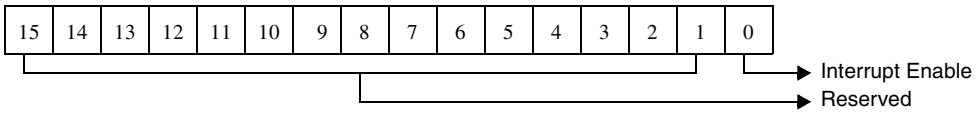


Figure 5-127. Command Options For Issue Abort Message Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to interrupt the host upon command completion. Clearing the bit disables the Command Complete interrupt.

Bits 1-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

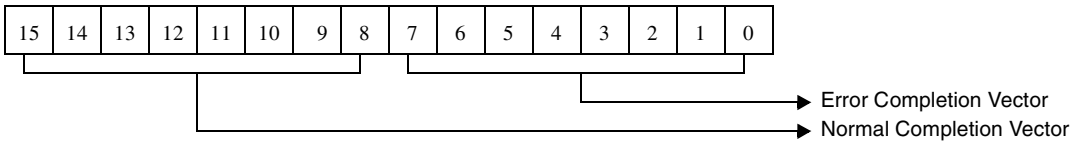


Figure 5-128. Normal/Error Completion For Issue Abort Message

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ISSUE ABORT MESSAGE
Command ID: 0x4E

ISSUE ABORT MESSAGE
Command ID: 0x4E

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

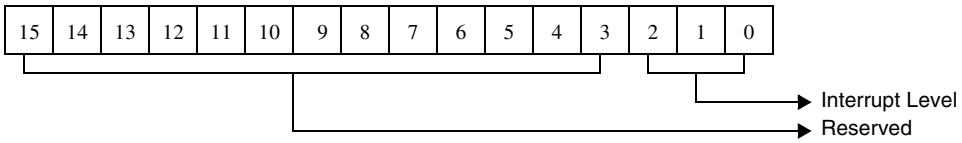


Figure 5-129. Interrupt Level For Issue Abort Message Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Unit Address (2 Bytes)

This field specifies the SCSI bus and the address of the target device.

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ISSUE ABORT MESSAGE
Command ID: 0x4E

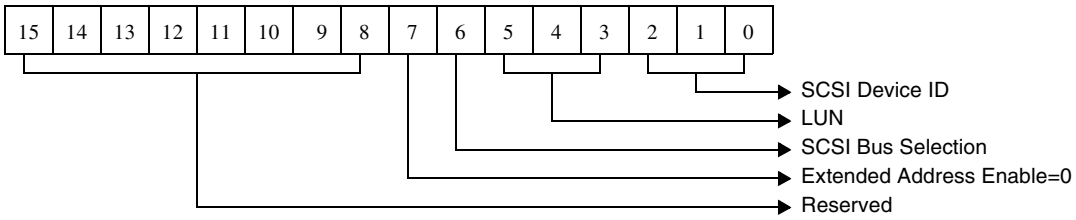


Figure 5-130. Unit Address For Issue Abort Message Command

Bits 0-2 SCSI Device ID (SCSI ID):

These bits contain the SCSI ID that is used when addressing the target. This value may range from 0 to 7.

Bits 3-5 Logical Unit Number (LUN):

The SCSI Logical Unit Number will be defined in these three bits. Refer to ***American National Standard Institute X3.131-199X*** for a detailed description of Logical Unit Numbers.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the board uses when executing the command. When the BUS bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7 Extended Address Enable:

Normal addressing is used when this bit is set to zero.

Bits 8-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

NOTE: When bit 7 is cleared bits 8-15 are reserved.

Extended Unit Address (2 Bytes)

This field specifies the SCSI bus and the address of the target device.

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ISSUE ABORT MESSAGE
Command ID: 0x4E

ISSUE ABORT MESSAGE
Command ID: 0x4E

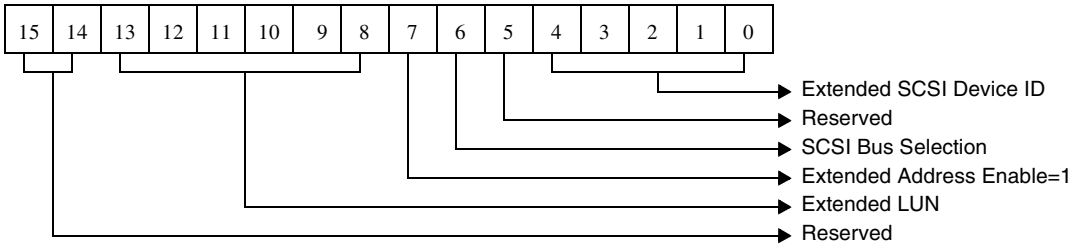


Figure 5-131. Extended Unit Address For Issue Abort Message Command

Bits 0-4 SCSI Device ID (SCSI ID):

These bits contain the SCSI ID that is used when addressing the target. This value may range from 0 to 31.

Bit 5 Reserved:

This bit is reserved and must be set to zero by the host.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the board uses when executing the command. When the BUS bit is cleared to 0, the board executes the command over the primary SCSI bus (Port 0). When set to 1, it uses the secondary SCSI bus (Port 1).

Bit 7 Extended Address Enable:

Setting this bit enables the extensions to both the LUN's and the SCSI ID. When this bit is set (1), the SCSI device ID shall be extended by two bits into the old LUN field. Bits 0-4 will now be utilized for the SCSI device ID.

Bits 8-13 Extended LUN (EXT LUN):

The LUN will be taken from the 6 bit field EXT_LUN

Bits 14-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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ISSUE ABORT MESSAGE
Command ID: 0x4E

ISSUE ABORT MESSAGE
Command ID: 0x4E

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Issue Abort Message command:

Return Status (2 Bytes)

These two bytes hold the returned status of the command. Any non-zero value indicates an error code. Appendix C contains the error codes.

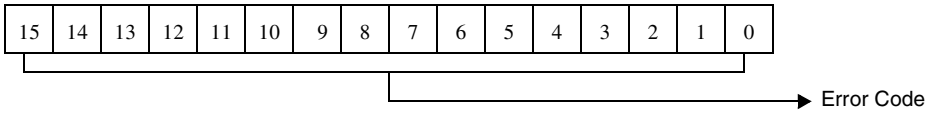


Figure 5-132. Return Status For Abort Message

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DOWNLOAD FIRMWARE

Command ID: 0x4F

The Download Firmware command provides a mechanism for firmware to be downloaded to the board. The image is then programmed into FLASH EPROM, or the currently executing memory image. This allows firmware to be upgraded without physically replacing the EPROM.

To complete the firmware download requires the following steps:

- Initiate the Firmware Download, by issuing the Download Firmware command with the Initialize Flash bit set in the Command Options.
- Transfer the new firmware to the board by issuing a series of Download Firmware commands with the Download Packet bit set in the Command Options.
- Program the new firmware into either Flash EPROM or Memory, by issuing the Download Firmware command with either the Program Flash or Program memory bit set in the Command Issues.

This command may only be submitted through the Master Command Entry to Work Queue 0.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	COMMAND CODE (0x4F)															
0x01	COMMAND OPTIONS															
0x02	**RETURN STATUS**															
0x03	RESERVED															
0x04	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x05	INTERRUPT LEVEL															
0x06	RESERVED															
0x07	RESERVED				TT		MT		ADDRESS MODIFIER							
0x08	BUFFER ADDRESS (MSW)															
0x09																
0x0A	TRANSFER LENGTH (MSW)															
0x0B																
0x0C	CHECK SUM (MSW)															
0x0D																
0x0E	RESERVED															
0x0F	SEQUENCE NUMBER															
0x10	RESERVED															
0x11																
0x12																
0x13																
0x14																
0x15																

NOTES: Reserved fields must be cleared to 0 by the host.

Figure 5-133. Download Firmware IOPB

Host-Provided IOPB Fields

The following information must be provided in the IOPB for the Download Firmware command.

Command Code

This field must be set to 0x4F to execute the Download Firmware command.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

DOWNLOAD FIRMWARE
Command ID: 0x4F

Command Options

This field contains the options for this command. The bits are defined as follows:

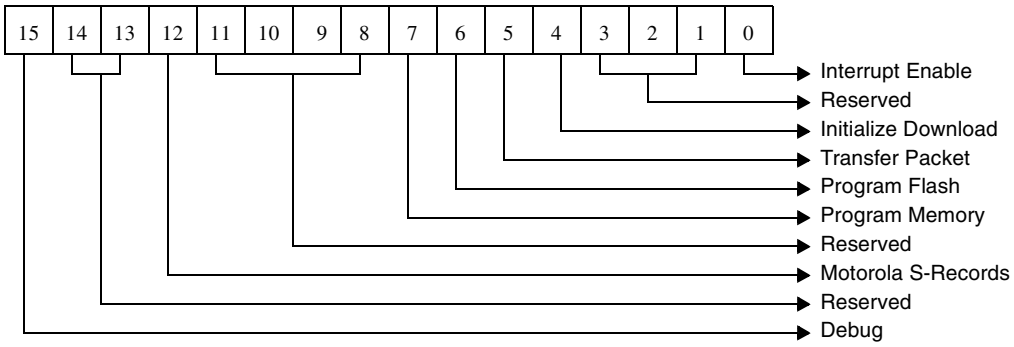


Figure 5-134. Command Options For Download Firmware Command

Bit 0 Interrupt Enable:

Setting this bit enables the board to generate and interrupt to the host upon command completion. Clearing this bit disables the Command Complete Interrupt. Setting this bit in conjunction with the Program Memory bit has no effect: no interrupt will be generated, and no IOPB returned.

Bits 1-3 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 4 Initialize Download:

Setting this bit causes the command to initiate the download process. A command with this option bit set will be referred to as an Initialize Download sub-command.

If the firmware to be downloaded is Motorola S-Record (subtype S3), bit 12 should also be set for the Initialize Download sub-command.

Bit 5 Transfer Packet:

Setting this bit causes this command to download to the board one in a sequence of packets containing the new firmware. A command with this option bit set will be referred to as a Transfer Packet sub-command.

Bit 6 Program Flash:

Setting this bit causes this command to program the Flash EPROM with the newly downloaded firmware. A command with this option bit set will be referred to as a Program Flash sub-command.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

Bit 7 Program Memory:

Setting this bit causes this command to replace the currently executing program image with the newly, downloaded firmware. A command with this option bit set will be referred to as a Program Memory sub-command.

This sub-command does not return. In all cases, the board will require re-initialization. If the command succeeds, the board will first report Controller Not Available through the Master Status Register, which will change to Board OK status when the new executing image is fully running. Then, the host will need to reinitialize the controller, using the Initialize Controller IOPB, and all of the work queues, using the Initialize Work Queue IOPB, exactly as was done in system startup.

If the command fails, the board will remain in the Controller Not Available state, and will require a Controller Reset to be issued through the Master Command Register, which will cause the previous version of firmware stored in EPROM to be re-loaded, and then the controller and work queues will need to be initialized

Bits 8-11 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 12 Motorola S-Records:

Setting this bit causes the board to interpret the downloaded firmware as Motorola S-Records, subtype S3, which use 4-byte addresses. This bit must be set on the Initialize Download sub-command.

Bits 13-14 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Bit 15 Debug:

Setting this bit causes the board to print debugging messages to the Controller Console during the process, which can be quite useful during driver development. Failing to set this bit will turn off debug printing, until an subsequent IOPB is received with this bit set.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

DOWNLOAD FIRMWARE
Command ID: 0x4F

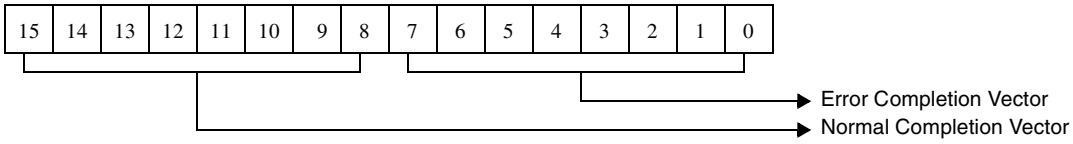


Figure 5-135. Normal/Error Completion For Download Firmware Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

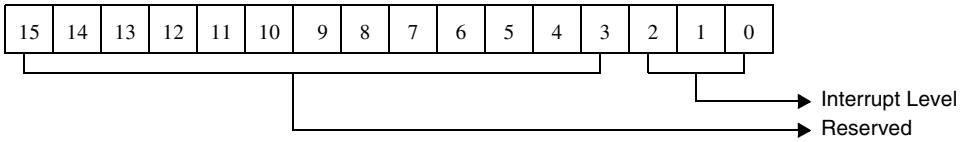


Figure 5-136. Interrupt Level For Download Firmware Command

Bits 0-2 Interrupt Level (LVL):

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed, but a level of 0 is allowed only when interrupts are disabled (Interrupt Enable bit = 0 in the Command Options word).

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

VME Transfer Type (2 Bytes)

These bytes specify the address modifier, memory type, and transfer type to be used for all VMEbus transfers associated with the command.

NOTE: Some memory systems may not support all of the options discussed for this field.

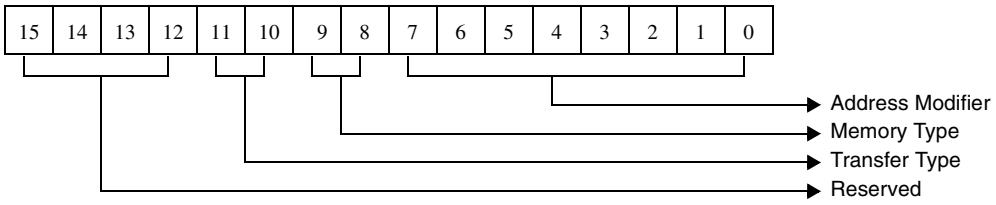


Figure 5-137. VME Transfer Types For Download Firmware Command

Bits 0-7 Address Modifier:

This byte specifies the address modifier to be used by the board for all VMEbus data transfers associated with this command.

Bits 8-9 Memory Type:

This 2-bit field specifies the width of data transfers. Permitted values are as follows:

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	16-BIT TRANSFERS
1	0	32-BIT TRANSFERS
1	1	SCATTER/GATHER LIST RESIDES IN SHORT I/O*

* Valid only for Scatter/Gather operations

Figure 5-138. Memory Type For Download Firmware Command

Bits 10-11 Transfer Type:

This 2-bit field specifies the type of data transfer to be performed. Permitted values are as follows:

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DOWNLOAD FIRMWARE
Command ID: 0x4F

DOWNLOAD FIRMWARE
Command ID: 0x4F

BIT 11	BIT 10	TRANSFER TYPE
0	0	NORMAL TYPE
0	1	BLOCK MODE
1	0	(RESERVED)
1	1	VME D64 BLOCK

Figure 5-139. Transfer Type For Download Firmware Command

Bits 12-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Buffer Address

In the Initialize Download sub-command this field must be set to zero.

In the Transfer Packet sub-command, this field specifies the address in host memory where the board will begin the data transfer for the packet.

In the Program Flash and Program Memory sub-commands this field must be set to zero.

Transfer Length

In the Initialize Download sub-command, this field must be set to zero.

In the Transfer Packet sub-command, this field specifies the total number of bytes to be transferred for the packet.

In the Program Flash sub-command, this field contains the total number of bytes transferred to the board. If this value fails to match the actual number of bytes received, an error will be returned.

In the Program Memory sub-command, this field must be set to zero.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

Check Sum Value

In the Initialize Download sub-command this field must be set to zero.

In the Transfer Packet sub-command, this field contains a calculated error checking value for the packet.

In the Program Flash and Program Memory sub-commands this field must be set to zero.

Sequence Number

In the Initialize Download sub-command this field must be set to zero.

In the Transfer Packet sub-command, this field specifies the total number of Transfer Packet sub-commands. The first Transfer Packet sub-command sets this value to 1, the next to 2, and so forth. Packets must be received by the board in order.

In the Program Flash sub-command this field contains the total number of packets submitted using the Transfer Packet sub-command.

In the Program Flash sub-command this field must be set to zero.

Return Status Error Codes

The following error codes may be returned in the Return Status field for each of the following commands:

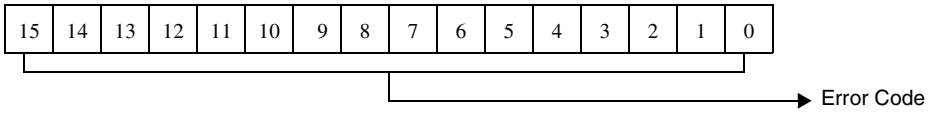


Figure 5-140. Return Status For Download Firmware

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DOWNLOAD FIRMWARE
Command ID: 0x4F

DOWNLOAD FIRMWARE
Command ID: 0x4F

HEX CODE	DESCRIPTION	COMMANDS		
		INITIALIZE DOWNLOAD	TRANSFER PACKET	PROGRAM FLASH
0x90	Incorrect Hardware	X		
0x91	Invalid Record Format	X		
0x92	Illegal IOPB Value	X	X	X
0x94	Invalid Download Operation		X	X
0x95	Bad Sequence Number		X	
0x96	Bad CRC		X	
0x97	Translation Error		X	X
0x99	Bad Packet Count			X
0x9A	Bad Transfer Count			X
0x9B	Bad EPROM Checksum			X
0x9C	Illegal Image			X
0x9D	Bad EPROM Image			X

Table 5-5.Download Firmware Error Codes

All of the error returns except the last (0x9D, Bad EPROM Image) are recoverable: the download process is aborted, no change is made to the EPROM. However, after the process of programming the EPROM has started, any error will leave the EPROM in a totally useless state, and it will have to be physically replaced.

The only other action that can be taken after the recoverable errors is to restart the process from the Initialize Download sub-command.

After the FLASH has been programmed, all subsequent SCSI Pass-Through IOPB's will be returned to the host with the exception code.

0x9F In-Core Memory Fails To Match EPROM Image. This will be reported as an Exception, using the Normal Completion Vector, but setting the EX bit in the CRSW.

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DOWNLOAD FIRMWARE
Command ID: 0x4F

DOWNLOAD FIRMWARE
Command ID: 0x4F

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB for the Download Firmware command. Transfer length reflects the number of bytes transferred.

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SET SERIAL NUMBER

Command ID: 0x52

The Set Serial Number command provides a mechanism by which the host can install two (2) 6-byte serial numbers on the board in non-volatile RAM (NVRAM). One use for this command is to provide host system software the opportunity to limit access to boards obtained through a particular distribution channel.

There are four (4) serial numbers, two (2) user serial numbers and two (2) Factory Serial Numbers set by the manufacturer. The serial numbers are reported in Controller Specific Space immediately following the Configuration Status Block. The Primary User Serial Number is at offset 0x7E8, the Secondary at offset 0x7EE. The Primary Factory Serial Number is at offset 0x7F4, the Secondary at offset 0x7FA.

Note: The Factory Serial Numbers are in the format of an Ethernet MAC node address, and cannot be altered by the host.

This command must be issued through the Master Command Entry to work queue 0. The format of the IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	COMMAND CODE (0x52)															
0x01	COMMAND OPTIONS															
0x02	**RETURN STATUS**															
0x03	RESERVED															
0x04	NORMAL COMP VECTOR								ERROR COMP VECTOR							
0x05	INTERRUPT LEVEL															
0x06	RESERVED															
0x07	RESERVED															
0x08	SERIAL NUMBER (BYTES 1,2)															
0x09	(BYTES 3,4)															
0x0A	BYTES (5,6)															

Figure 5-141. Set Serial Number Command

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SET SERIAL NUMBER
Command ID: 0x52

Command Code

This field must be set to 0x52 to install the Host Serial Number.

Command Options

This field contains the options for this IOPB. The bits are defined as follows:

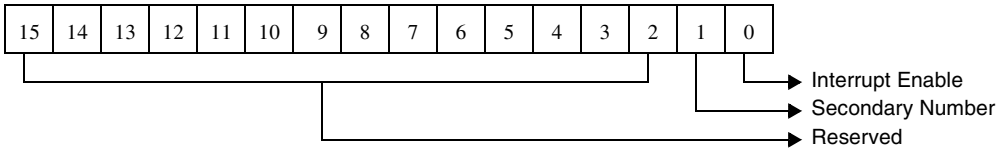


Figure 5-142. Command Options For Set Serial Number Command

Bit 0 Interrupt Enable

Setting this bit enables the Cougar to generate an interrupt to the host upon command completion.

Bit 1 Secondary Number

Setting this bit causes the specified Host Serial Number to be installed in the secondary, rather than the primary, location.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two bytes specify the VMEbus interrupt vectors that the board will use to report normal command completion and command completion with error.

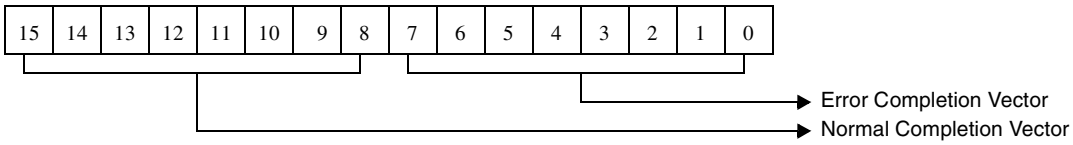


Figure 5-143. Normal/Error Completion Vector For Set Serial Number Command

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

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SET SERIAL NUMBER
Command ID: 0x52

SET SERIAL NUMBER
Command ID: 0x52

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used to notify the host of a command completion (normal or with error).

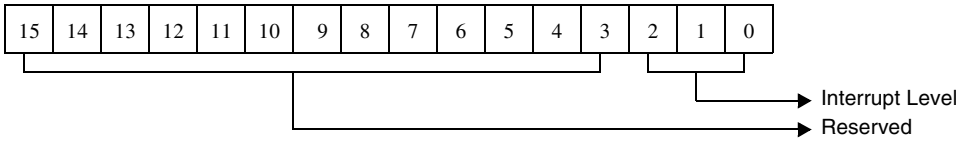


Figure 5-144. Interrupt Level For Set Serial Number Command

Bits 0-2 Interrupt Level:

These bits set the interrupt level used by the board to assert a Command Complete interrupt on the VMEbus. Values of 0 through 7 are allowed with a level of 0 allowed only when interrupts are disabled by clearing the interrupt enable bit in the Command Options word.

Bits 3-15 Reserved:

These bits are reserved and must be cleared to 0 by the host.

Serial Number

These six bytes contain the Host Serial Number to be installed in NVRAM, and displayed in CSS.

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SET SERIAL NUMBER
Command ID: 0x52

Return Status (2 Bytes)

This field provides the return status for the command.

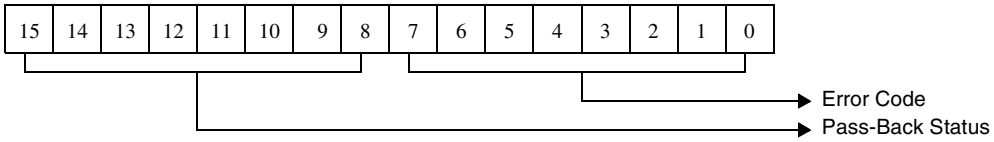


Figure 5-145. Return Status For Set Serial Number Command

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response. Any non-zero value is an error code. Appendix C contains the error codes.

Bits 8-15 Pass-Back Status:

This value is the SCSI status byte returned by the target device. It is not changed by the board. A value of 0x0 indicates Good Status. A non-zero value indicates that a SCSI device error has occurred.

NOTE:The board can be configured to respond to a non-zero pass-back status by:

- Freezing the queue,
- Aborting all commands in or destined for the queue, or
- Initiating autosense error recovery

The work queue options are set via the Initialize Work Queue command, and are mutually exclusive. (See Work Queue Options, page and Error Recovery Tools in Chapter 6 for details).

Serial Numbers Reported in CSS.

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SET SERIAL NUMBER
Command ID: 0x52

SET SERIAL NUMBER
Command ID: 0x52

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x788 To 0x7e6	CONTROLLER STATUS BLOCK															
0x7e8	OEM INSTALLED SERIAL NUMBER (BYTES 1,2) (PRIMARY)															
0x7ea	(BYTES 3,4)															
0x7ec	(BYTES 5,6)															
0x7ee	OEM INSTALLED SERIAL NUMBER (BYTES 1,2) (SECONDARY)															
0x7f0	(BYTES 3,4)															
0x7f2	(BYTES 5,6)															
0x7f4	MFR INSTALLED SERIAL NUMBER (BYTES 1,2) (PRIMARY)															
0x7f6	(BYTES 3,4)															
0x7f8	(BYTES 5,6)															
0x7fa	MFR INSTALLED SERIAL NUMBER (BYTES 1.2) (SECONDARY)															
0x7fc	(BYTES 3,4)															
0x7fe	(BYTES 5,6)															

Figure 5-146. Controller Serial Number

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BUFFER FIFO

Command ID: 0x53

The Buffer FIFO command provides backward compatibility for drivers and diagnostic routines that previously used the 4210 Jaguar Buffer FIFO command. This command may be used for testing various transfer options and boundary conditions, as well as fault isolation.

This command turns onboard data buffer memory into a large FIFO (First-In-First-Out) buffer that the host can read and write. Since no constraints are imposed on the structure of the data requests, transfer counts may be even or odd and starting buffer addresses in host memory may be aligned or unaligned.

The structure of the read and write commands used are independent. For example, the host may write 128K of data with a single command, then read it with 64 2K commands. A scatter/gather operation may be used to write, and a non-scatter/gather operation to read.

This command must be issued through the Master Command Entry to work queue 0. The format of the IOPB is as follows:

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	COMMAND CODE															
0x01	COMMAND OPTIONS															
0x02	RETURN STATUS															
0x03	RESERVED															
0x04	NORMAL COMPLETION VECTOR								ERROR COMPLETION VECTOR							
0x05	INTERRUPT LEVEL															
0x06	RESERVED															
0x07	DMA TRANSFER CONTROL WORD															
0x08	BUFFER ADDRESS (MSW)															
0x09	(OR SCATTER/GATHER LIST ADDRESS) (LSW)															
0x0A	MAX TRANSFER LENGTH (MSW)															
0x0B	(OR SCATTER/GATHER ELEMENT COUNT) (LSW)															
0x0C	RESERVED (MSW)															
0x0D	(OR SCATTER/GATHER TRANSFER COUNT) (LSW)															
0x0E To 0x15	RESERVED (16 BYTES)															

Figure 5-147. Buffer FIFO Command

The remainder of this section describes the function of each field in the Buffer FIFO IOPB.

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BUFFER FIFO
Command ID: 0x53

BUFFER FIFO
Command ID: 0x53

Host Provided IOPB Fields

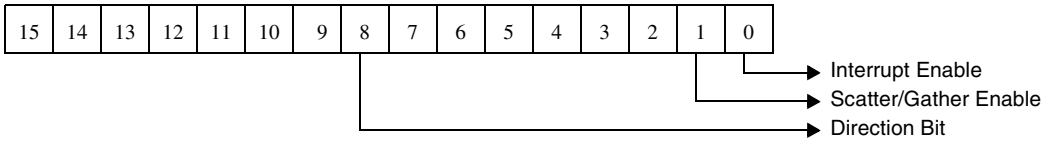
The following information must be provided in the IOPB for the Buffer FIFO command:

Command Code

This field must contain the value 0x53 to execute the Buffer FIFO command.

Command Options

This field defines options for this command. The following sub-fields are defined:



Bit 0 Interrupt Enable:

Setting this bit causes the controller to generate an interrupt to the host upon command completion.

Bit 1 Scatter/Gather Enable:

Bit 8 Direction Bit:

Setting this bit allows the host to write data to the controller. Clearing this bit allows the host to read data from the controller.

Normal Completion Vector/Error Completion Vector (2 Bytes)

These two fields specify the VMEbus interrupt vectors that the controller will use to report normal or error command completion status back to the host.

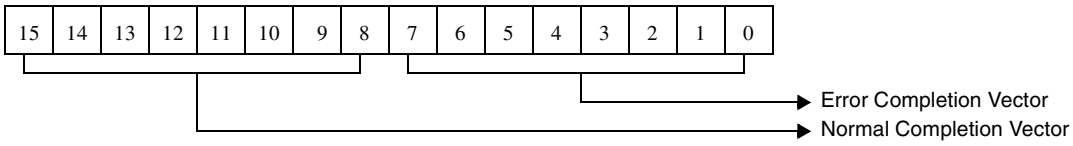


Figure 5-148. Normal/Error Completion Vector For Buffer FIFO Command

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BUFFER FIFO
Command ID: 0x53

Bits 0-7 Error Completion Vector:

This value specifies the interrupt vector used when notifying the host of command completion with error.

Bits 8-15 Normal Completion Vector:

This value specifies the interrupt vector used when notifying the host that the command completed without error.

Interrupt Level (2 Bytes)

This field specifies the VMEbus interrupt level used by the controller to notify the host of command completion, if the Interrupt Enable bit is set in the Command options field. Legitimate values for this field range from 1 to 7.

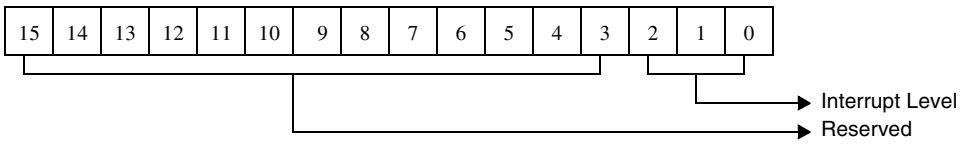


Figure 5-149. Interrupt Level For Buffer FIFO Command

VME Transfer Type (2 Bytes)

This field defines the parameters for the DMA transfer associated with the command. If scatter/gather is enabled, this applies to the DMA transfer of the scatter/gather list from the host memory. Transfer words for the actual data elements are then contained in each scatter/gather list element. If scatter/gather is not enabled, this applies to the actual transfer of data associated with this command.

Bits 0-7 Address Modifier:

This sub-field specifies the VMEbus address modifier to be used with the transfer.

Bits 8-9 Memory Type:

This sub-field specifies the width of the data transfers, as follows:

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BUFFER FIFO
Command ID: 0x53

BUFFER FIFO
Command ID: 0x53

BIT 9	BIT 8	MEMORY TYPE
0	0	(RESERVED)
0	1	16-bit transfers
1	0	32-bit transfers
1	1	Scatter/gather list resides in short I/O*

* Valid only for Scatter/Gather operations

Bits 10-11 Transfer Type:

This sub-field defines the type of the data transfer, as follows:

BIT 11	BIT 10	TRANSFER TYPE
0	0	NORMAL TYPE
0	1	BLOCK MODE
1	0	(RESERVED)
1	1	VME D64 BLOCK

Buffer Address (4 Bytes)

This field specifies the address at which the controller will begin the data transfer. If the controller is addressing system memory, the value in the field is a VMEbus address. If the address is in short I/O, the value is an offset from the short I/O base address. If scatter/gather is enabled, this field is the address of the scatter/gather list.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSW BUFFER ADDRESS (or Address of Scatter/Gather List) LSW															

Figure 5-150. Buffer Address For Buffer FIFO Command

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BUFFER FIFO
Command ID: 0x53

Maximum Transfer Length (4 Bytes)

This field specifies the maximum number of bytes that may be transferred by the command. If this field is zero, and the Command specifies a write, all accumulated data will be flushed from the controller FIFO.

NOTE:In the returned IOPB of the the command response, this value reflects the actual number of bytes transferred.

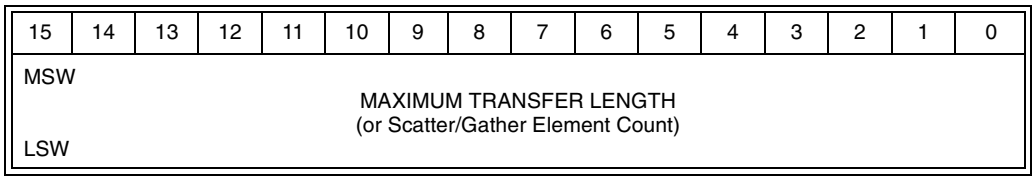


Figure 5-151. Maximum Transfer Length For Buffer FIFO Command

Reserved (4 Bytes)

Unless scatter/gather is enabled, words 0xC and 0xD of the SCSI Pass-Through IOPB are reserved and must be cleared by the host. For scatter/gather operations, this field specifies the sum of the individual element entry counts. See the *Scatter/Gather Operations* in Chapter 6 for details.

The Buffer FIFO command can be used to generate certain error conditions, by setting the value of the following fields to produce the corresponding errors:

MAX TRANSFER	BUFFER ADDRESS	S/G COUNT	RETURNED EVENT
0	0	0	NO-OP
0	NON-ZERO	0	FORCE ERROR
0	NON-ZERO	NON-ZERO	CONTROLLER PANIC

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BUFFER FIFO
Command ID: 0x53

BUFFER FIFO
Command ID: 0x53

Returned Values

Upon command completion, the following information is provided by the board in the returned IOPB of the command response for the SCSI Pass-Through command.

Return Status (2 Bytes)

This field provides the return status for the command.

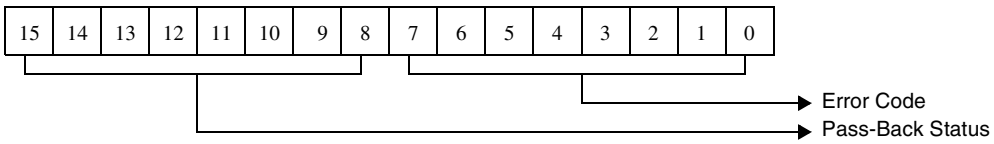


Figure 5-152. Return Status For Buffer FIFO Command

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response. Any non-zero value is an error code. Appendix C contains the error codes.

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BUFFER FIFO
Command ID: 0x53

BUFFER FIFO
Command ID: 0x53

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Chapter 6
Application Notes

This chapter contains application notes on the following:

- Error Recovery Tools
- Scatter/Gather Operations
- Printer Port Operations
- Offboard IOPBs
- Considerations For Maximizing SCSI Synchronous Data Transfers
- Download Firmware
- MACSI SCSI Synchronous Options
- Board Identification In MACSI CSS

Error Recovery Tools

The board supports a variety of tools for dealing with two basic types of errors that can occur - SCSI device errors and controller errors. These error recovery tools are described in the following subsections. They are also documented where appropriate in the MACSI and command set sections of the manual.

SCSI Device Errors

A SCSI device error is defined to be the completion of a SCSI Pass-Through IOPB with a value other than 0x0 (Good Status) in the Pass-Back status byte of the IOPB Return Status word (see Chapter 5). The controller supports a variety of tools for dealing with device errors, including:

- Autosense recovery
- Freeze/Thaw Work Queue
- Abort Work Queue on Error
- Fields in the Configuration Status Block for determining SCSI bus status and the last device on the bus
- Several error recovery commands

These tools are described in the following subsections.

Autosense Recovery

The Autosense Recovery feature can be used to obtain the sense data (if any) reported by a SCSI device after executing a SCSI command that returns pass-through error status indicating a SCSI check condition. This feature is enabled on a per-work queue basis by setting the Enable Autosense Recovery bit in the Work Queue Options field of the Initialize Work Queue command. When this feature is enabled, a work queue will NOT freeze and thaw.

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When the host issues a SCSI Pass-Through command to a work queue with Autosense Recovery enabled and a SCSI check condition is returned by the device, the board follows the command with an automatic Request Sense to the target device. The target device responds to the Request Sense by sending the board its sense data reported in the SCSI command's returned IOPB, starting at the CDB field (i.e. SCSI bytes 0-11).

Since the sense data may extend past the boundaries of the original IOPB, additional space must be allocated to the Command Response Block (CRB) for returned sense data. If the data is being reported to an offboard CRB, the host must ensure that adequate space exists for this data to be written without generating system bus errors. For details on setting the onboard CRB size, refer to Chapter 5, *Initialize Controller Command*. For a discussion of setting up an offboard CRB.

Freeze/Thaw Work Queue And Abort Work Queue On Error

Since a device may have many commands queued for it when an error occurs, SCSI device errors require a mechanism which allows the host to alter the order in which commands are executed. The Freeze/Thaw Work Queue and Abort Work Queue on Error options are provided for this purpose.

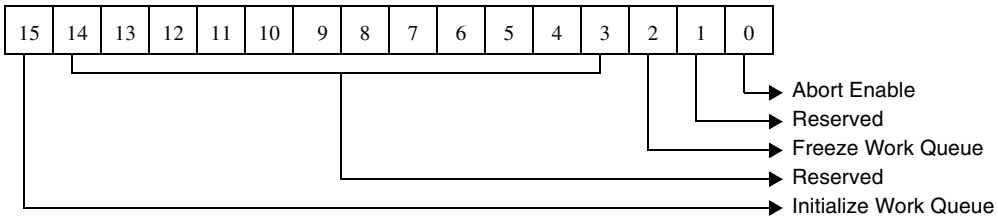
NOTE: The Freeze/Thaw Work Queue and Abort Work Queue on Error options are mutually exclusive. That is, a given work queue cannot be both frozen *and* aborted in the event of an error. Autosense recovery and Freeze/Thaw Work Queue are also mutually exclusive. If the Autosense Recovery is enabled for a work queue, the queue will not freeze.

Freeze Work Queue on SCSI Error

The Freeze Work Queue option provides a mechanism for freezing the state of a work queue when an error occurs. Error handling can be accomplished by passing one or more corrective commands to the device (such as Request Sense or a diagnostic command). Such commands must be issued to the device through the Master Command Entry via Work Queue 0. After the error handling has been completed, the work queue can be unfrozen.

The Freeze Work Queue option is enabled on a per-queue basis when the queues are initialized. To enable the Freeze option for a given queue, set Bit 2 (FZE) in the Work Queue Options field of the Initialize Work Queue IOPB (see Chapter 5, *Initialize Work Queue Command*).

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(Word 0xF In The Initialize Work Queue IOPB)

Figure 6-1. Freeze Work Queue Option

If a work queue is dedicated to a specific SCSI device, enabling the Freeze bit halts all further commands to that device (and no other) in the event of a SCSI device error. As noted previously, a device error occurs when the host issues a SCSI Pass-Through IOPB that completes with any value other than 0x00 (Good Status) in the Pass-Back Status byte of the IOPB Return Status word.

In addition, a bit will be set in the Frozen Work Queues Register of the Configuration Status Block (see discussion below).

Commands sent to a "frozen" work queue will not be executed until the work queue is "thawed", as discussed below.

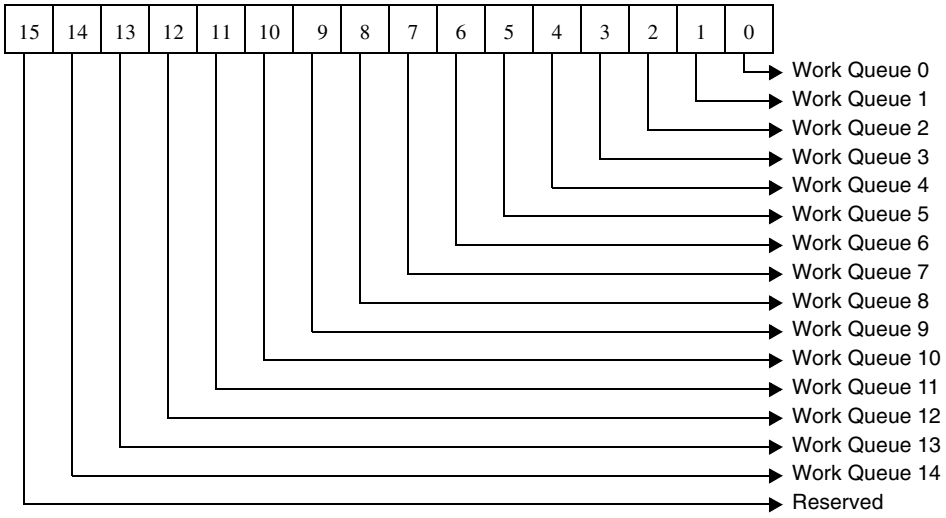
NOTE: Since the Freeze Work Queue option is intended to support error handling as a part of normal SCSI operations, queues are **not** frozen for controller errors.

The Freeze Work Queue or Freeze Reset Work Queue operation may also be enabled using the Initialize Controller command to freeze a work queue that has an active command upon receiving a SCSI reset. The host will "know" a Work Queue is frozen if it receives a command returned from the queue with a SCSI bus reset error status. **It is recommended that you enable this option when initializing the board.** The default setting (i.e. do not freeze queue if command is returned with SCSI bus reset status) is provided for backward compatibility.

NOTE: The Freeze Work Queue on Error bit is *not* enabled for Work Queue 0. This is because it is defined to have a length of 1. This is done to ensure that only one error recovery process occurs at a time. However, it is possible that a command from Work Queue 0 may require error recovery itself. To allow this to take place, the SCSI Bus Reset and Flush Work Queue commands may always be issued through the Master Command Entry to Work Queue 0. For all other commands Work Queue 0 has a length of one.

Frozen Work Queues Register. Located in the Configuration Status Block, this register identifies which work queues are frozen (if any). For Work Queues 1 to 14, if a given queue is frozen, then the corresponding bit position is set in the register. As noted before, Work Queue 0 cannot be frozen. The format of the register is repeated below for your reference:

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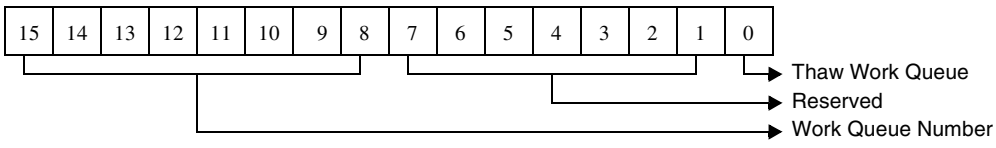


NOTE: Work Queue 0 cannot be frozen. Therefore, Bit 0 in the Frozen Work Queues Register is always cleared.

Figure 6-2. Frozen Work Queues Register

Thaw Work Queue. After the SCSI error condition has been cleared, the queue can be unfrozen by use of the Thaw Work Queue bit in the Master Control/Status Block (MCSB). Execution of commands in the frozen queue is restarted by setting the least significant bit of the Thaw Work Queue Register Word 0x4 (see Chapter 3, *System Interface*, for further details).

The frozen work queue is unfrozen by writing the appropriate work queue number into the upper byte of the Thaw Work Queue Register and then setting the Thaw Work Queue Bit 0 (THW) of that register. The board will clear Bit 0 of the register to acknowledge the thawing of the work queue. The Thaw Work Queue Register is defined as follows:



(Word 0x4 in the Master Control/Status Block)

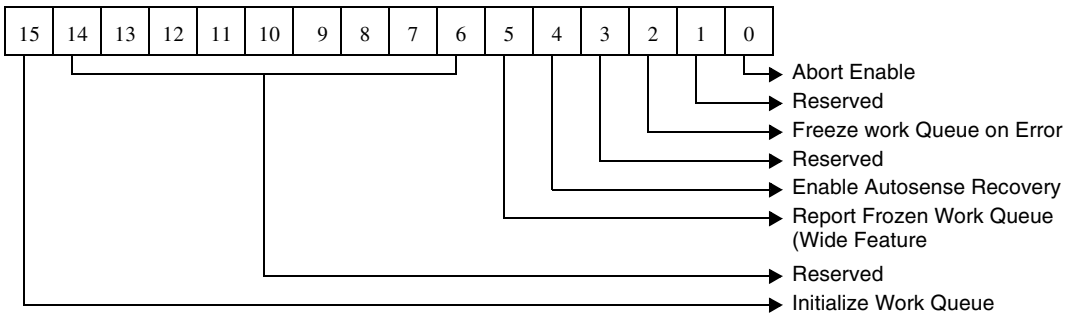
Figure 6-3. Thaw Work Queue Register

Abort Work Queue On Error

The Abort Work Queue on Error option causes the board to abort all commands for that work queue until a command is issued with the Abort Acknowledge bit set to 1 in the

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command's Queue Entry Control Register. This option is mutually exclusive with the freeze/thaw work queue feature described in the preceding subsections. A given work queue cannot be both frozen and aborted in the event of an error.



(Word 0xF in the Initialize Work Queue IOPB)

Figure 6-4. Abort Work Queue On Error Option

To enable Abort Work Queue on Error for a given work queue, set Bit 0 of the Work Queue Options field when you initialize the work queue.

When a SCSI Device error occurs, the failing IOPB will be returned with the bad (non-zero) pass-back status. All other commands for that work queue will be returned with a Command Complete and Abort Queue set to 1 in the Command Response Status Word. This will continue until a command is submitted with the Abort Acknowledge bit in the command's Queue Entry Control Register set to 1. This applies not only to the commands in the queue when the abort was activated, but to all commands issued to that queue until the abort is acknowledged.

Registers For Determining SCSI Bus Status And Last Device On Bus

The Configuration Status Block contains two registers that provide the current SCSI bus status. Information in these registers can be used in conjunction with the Command Status Inquiry and Bus Status Inquiry commands to determine the type of error that has occurred.

ID Of Last Device Connected To SCSI Bus. The Last Device ID bytes contain the SCSI Bus Ids of the last devices connected to Port 0 and Port 1. Bits 8-15 contain the Primary SCSI Bus ID last connected, and Bits 0-7 contain the Secondary Bus ID last connected.

SCSI Bus Status. The SCSI Bus Status field describes the status of the primary and secondary SCSI buses. Bits 8-15 contain the primary bus status. Bits 0-7 contain the status of the secondary bus (if used). Both bytes are images of the SCSI processor phase sense register.

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Error Recovery Commands

Normal SCSI check condition errors are handled very simply via SCSI protocol. However, there are other types of errors from which it can be difficult to recover, such as errors due to a bad device or bug in the device driver program.
The board provides three commands that can be used to determine what type of error has occurred without having to reset the board. They are:

- The **Command Status Inquiry** command reports the status of a command, identified by its command tag.

- The **Bus Status Inquiry** command reports the state of all IOPBs requesting the SCSI Bus. It is used to find the command that is active on the bus at the time an IOPB timeout (discussed below) occurred. This is important because a command may cause another command to time out by blocking use of the SCSI bus by other devices.

- **Cancel Command Tag** removes a command from the board. This command is provided for systems that can reset devices in error without resetting the SCSI bus.

- The above commands must be issued through the Master Command Entry to Work Queue 0. They may be issued at any time.

For additional information on commands, refer to the descriptions of the individual commands in Chapter 5.

Selection And Command Timeouts

The board provides two (2) features to signal unusual errors:

- Selection timeout

- Command timeout

Selection timeouts prevent the board from becoming locked up while trying to select a device that does not respond to SCSI selection. Command timeouts let the board notify the host that a user-programmed period of time has expired since a device was successfully selected.

Selection Timeout

The selection timeout causes an IOPB to be terminated with an error status if a device does not respond to selection within a set period of time (250 milliseconds).

Command Timeout

The command timeout is specified in the Initialize Controller command for Work Queue 0, and in the Initialize Work Queue command for all other queues. All IOPBs issued through a work queue will use the timeout value specified for that work queue.

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- For Work Queue 0, words 0x9 of the Controller Initialization Block are used for the Work Queue 0 command timeout. This field (word 9) is specified in increments of 256 msec. A value of 0 specifies no timeout.

- The timeout values used for commands issued through Work Queues 1 - 14 are set when the queues are initialized. The words 0x12-0x13 of the Initialize Work Queue command contains the timeout value, which is specified in increments of approximately 256 milliseconds. Thus, each work queue (device) is able to run a unique timeout value. A value of 0 specifies no timeout.

  To determine whether or not a command has timed out, the board measures how much time has elapsed between the successful completion of the selection phase to the completion of the command on the SCSI bus (including all disconnect periods).

  When a command timeout occurs, the board uses the Controller Error Interrupt and Vector to inform the host of the condition (see discussion in next subsection). This mechanism returns an error status without returning the IOPB that caused the error. Command timeouts invoke a Controller Error Vector Status Block with Error Code 0xC1 (IOPB Timeout) in the Error Code byte of the IOPB Return Status field. If the command subsequently completes correctly, the original IOPB will complete properly. The host may attempt to cancel the IOPB with the Cancel Command Tag IOPB. This will cause the board to terminate any further execution. The canceled IOPB will not be posted back to the host. If the IOPB is active on the SCSI bus, the command cannot be canceled and the host must either reset the SCSI bus or remove the device from the bus in some external manner. The command will then be posted with a Canceled Due to Bus Reset Status or Invalid Sequence error if it abruptly disconnects from the bus.

  The board *must* retain the IOPB which caused the timeout until the error condition has been cleared. This is necessary for two reasons. First, it allows the command to be completed if the device responds before error recovery can take place. Second, it prevents new commands from being issued from the queue until the host can handle the error condition.

  The usual technique for clearing errors is to issue a Reset SCSI Bus IOPB. This causes all of the commands currently active on that bus to be returned with a bus reset status. However, if your system is capable of removing individual devices from the bus, you have an alternative to resetting the entire bus. The alternative is to remove the device in error and then issue a Cancel Command Tag IOPB to clear the IOPB which is waiting for a response from the removed device.

  If a command other than the command that timed out is active on the bus, it will be necessary to determine which command actually caused the error. There are a number of methods for determining the device in error. One technique is to have the host wait an additional period of time and check the board again to see that the state is the same as the previous check. This type of error is due either to incorrect programming or to a failed device and should be a rare occurrence.

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Controller Error Interrupt And Vector

Controller errors are generated when an error occurs on the board that is not related to a specific IOPB. This can be due to a variety of unusual board-related conditions. They may also be generated if the host issues an IOPB that lacks the proper information needed for the command to be processed normally.

The interrupt level and vector used to signal such errors are set in the Controller Error Completion Level/Vector field of the Controller Initialization Block.

Controller errors will not generate an interrupt if the controller error interrupt level is cleared to 0 in the Initialize Controller IOPB. However, the board will report controller errors to the Command Response Block even if interrupts are not enabled. Controller errors will not cause work queues to freeze or abort commands.

The board flags a controller error by setting the following bits in the Command Response Status Word: bit 7 (Status Change), bit 2 (Error), and bit 0 (Command Response Block Valid). Thus, the Command Response Status Word will read 0x0085 to signal the error.

The Controller Error Vector enables the host to determine the source of a variety of errors. These include:

- IOPB type error
- IOPB timeout
- A device has connected for which no IOPB exists
- A device is requesting a data transfer of the opposite direction specified by the direction bit of the IOPB

The above-listed error conditions cause the board to return a Controller Error Vector Status Block to the Command Response Block. This returned structure does not contain an IOPB. Instead, it contains an error code indicating what has happened, along with information from the Command Queue Entry that was being executed when the error occurred (command tag, IOPB length, and work queue number).

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Table 6-1. Controller Error Vector Status Block

WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	COMMAND RESPONSE STATUS WORD															
0x1	IOPB TYPE								RESERVED							
0x2	COMMAND TAG															
0x3																
0x4	IOPB LENGTH								WORK QUEUE NUMBER							
0x5	RESERVED															
0x6	RESERVED								ERROR CODE							

Controller Error Codes

The valid error codes which may be returned in word 0x6 of the above block are as follows:

Table 6-2. Returned Error Codes For Controller Error Vector

CODE	DEFINITION
0xC0	IOPB Type Error.
0xC1	IOPB Timeout.
0x82	A target has reconnected for which no IOPB exists.
0x83	A target is requesting more data to be transferred than the IOPB transfer count allows.
0x84	A target is requesting a data transfer of the opposite direction specified in the direction bit of the IOPB.
0x86	Non-Recoverable SCSI Error.
0xFF	A controller error which indicates that a panic has occurred on the board. Immediately following the error code in short I/O, an ASCII string will indicate the file, line number, and a brief description of the panic. This information will only be posted in short I/O, if offboard CRBs are being used, the information in the offboard memory will not be updated.

NOTE: These Error Codes will not freeze the work queue.

IOPB Type Error (0xC0). The board only supports type zero IOPBs. If the IOPB type field (bits 8 - 11 in word 0 of the Command Queue entry) contains any value other than 0, the board will not "know" the overall structure of the IOPB and will therefore be unable to process it. This error code indicates that the Command Queue entry contains invalid information.

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IOPB Timeout Error (0xC1). An IOPB has timed out. The IOPB will remain active until it completes properly or is canceled explicitly. The status of the IOPB may be determined with the Command Status Inquiry IOPB. With this error code, the Controller Error Vector Status Block information is valid.

Unknown Device Reconnection (0x82). A SCSI device for which no current IOPB exists has re-selected the board. This code indicates that the Controller Error Vector Status Block contains invalid information.

Data Transfer Count Mismatch (0x83). Data counters have been exhausted, but the device is requesting more data than the current IOPB can transfer. With this error code, the Controller Error Vector Status Block information is valid. The suggested recovery for this error is to reset the SCSI code.

Data Direction Errors (0x84). The direction bit in the IOPB does not match the data transfer direction requested on the SCSI bus. This error code indicates that the Controller Error Vector Status Block information is valid.

Non-Recoverable SCSI Error (0x86) An error has occurred which has left the SCSI hardware in an unknown state. With this error, the information in the Controller Response Block (particularly the Command Tag field) is valid if not zero's. Refer to the following section on reporting Non-recoverable SCSI Errors for details on additional diagnostic information returned.

Reporting Non-Recoverable SCSI Errors

A number of environmental causes can force the board's SCSI subsystem into a non-recoverable state. Typically, these causes are related to the electrical characteristics or behaviors associated with devices attached to the SCSI bus. Normally, these errors are detected and corrected during systems integration and qualification.

The occurrence of these errors under normal operating conditions indicates a serious malfunction.

If enabled at initiation, the Non-Recoverable SCSI error will be reported as a controller error, using the Controller Error Interrupt Level and Vector. The following bits will be set in the Command Response Status Word (CRSW).

- CRBV (Command Response Block Valid), bit 0
- RE (Error), bit 2
- SC (Status Change), bit 7
- SE (SCSI Error), bit 11

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Thus, the value of the CRSW for this error will be 0x0885. To enable this error recovery feature, set bit 2 of the Error Recovery Options word in the Controller Initialization Block at Controller Initialization.

The controller error returned will be error code 0x86 and the 16-bit word following this error code will contain the following information:

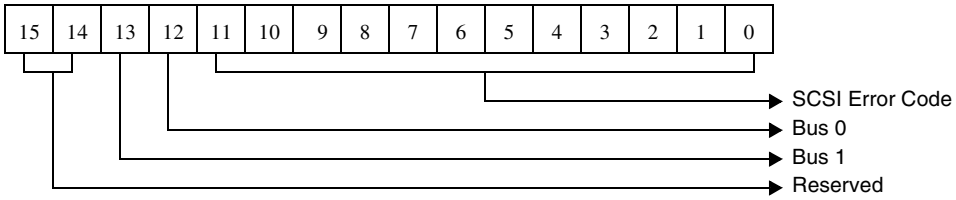


Figure 6-5. SCSI Error Code 16 Bit Word

Bits 0-11 SCSI Error:

This field contains the actual SCSI error code.

Bit 12 Bus 0:

This bit will be set when the error occurred on the primary SCSI channel.

Bit 13 Bus 1:

This bit will be set when the error occurred on the secondary SCSI channel.

Bits 14-15 Reserved:

These bits are reserved and must be set to zero.

Once in this condition, the SCSI bus must be reset in order to return the SCSI subsystem to functional status.

If this option is not enabled, non-recoverable SCSI errors will produce a controller panic, requiring reinitialization of the controller.

Suggested Error Recovery Sequence

The following is a suggested series of steps which may be taken by the host to recover from an error:

- The host issues a Bus Status Inquiry to examine the status of commands executing on the bus. This enables the host to determine which command caused the error. Note that the command which timed out may not be one that is actually blocking the SCSI bus. The command that is most likely in error will be the one active on the bus when the Bus Status Inquiry is executed.

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- If a device is found to be connected on the SCSI bus indefinitely, there is no way to clear the error without resetting the bus. When this is the case, the host should issue the Reset SCSI Bus IOPB through the Master Command Entry. All work queues with commands active on the bus will have those commands returned with a SCSI Reset Error status, and the work queue will be frozen (if the Freeze Work Queue on Reset option was selected in the Initialize Controller Command).

- The device which caused the error should either be removed or tested before restarting normal operation. The host can then reissue the commands and thaw the work queues.

- For systems that have the ability to power down individual devices, the Flush Work Queue command can be used to prevent new commands from being issued to the device after the error has been cleared. It is not mandatory to flush the work queue before restoring the device, but be aware that the board will begin processing the commands from the queue as soon as: 1) the bus becomes available, and 2) the command that was being executed is cleared.

  After powering down the device, the host should issue a Cancel Command Tag IOPB to clear the command which caused the error (i.e. the IOPB that was not completed by either a normal SCSI completion or by a SCSI reset).

  NOTE: The Flush Work Queue Command does not flush commands that are presently active on the bus. These may only be canceled by: 1) a normal command completion, 2) a SCSI reset, or 3) a Cancel Command Tag IOPB.

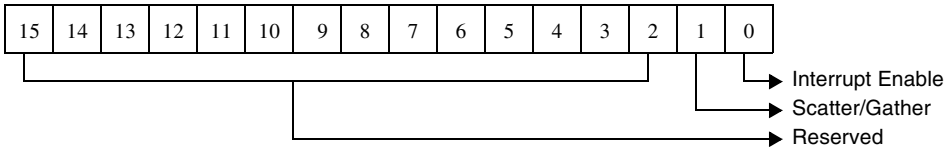
Scatter/Gather Operations

The scatter/gather option allows contiguous peripheral data to be written to non-contiguous areas in system memory ("scatter"), or moved from non-contiguous blocks of system memory into contiguous ones ("gather"). Scatter/gather operations can only be performed with SCSI peripheral data. They cannot be used in conjunction with the printer port.

By allowing multiple blocks of data to be transferred using only one command, scatter/gather frees the host from having to process multiple transactions when transferring non-contiguous blocks. This improves system performance by minimizing both the number of VMEbus interrupts and the number of bus transactions associated with common peripheral activity.

To enable scatter/gather, set bit 1 of the Command Options word in the SCSI Pass-Through IOPB.

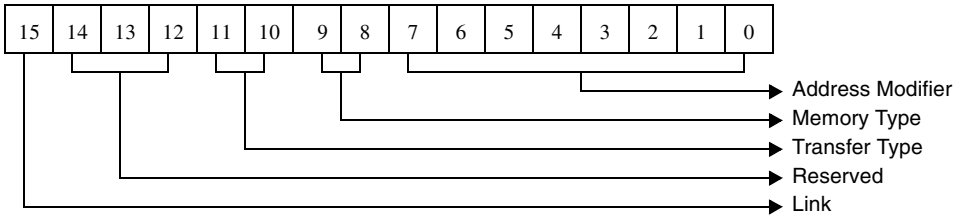
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(Word 0x1 In The SCSI Pass-Through IOPB)

Figure 6-6. Command Options Word In The SCSI Pass-Through IOPB

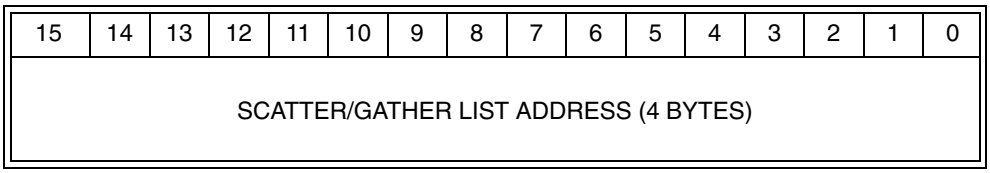
With scatter/gather enabled, the following three IOPB fields reference the Scatter/Gather Element List: 1) Memory Type/Transfer Type/Address Modifier, 2) Buffer Address, and 3) Transfer Length. The Memory Type/Transfer Type/Address Modifier field has the same definition as it does for IOPBs which do not perform scatter/gather operations, except for the Link bit (Bit 15). For an explanation of this bit, see "Scatter/Gather List Linking" below.



(Word 0x7 In The SCSI Pass-Through IOPB)

Figure 6-7. Memory/Transfer Type/Address Modifier For Scatter/Gather Operations

When scatter/gather is used, words 0x8 - 0x9 of the IOPB contain the address of the scatter/gather list. If the Memory Type is 0x1 or 0x2, the value is interpreted as an address in system memory.

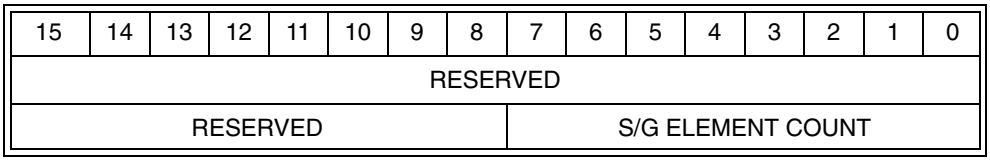


(Words 0x8-0x9 In The SCSI Pass-Through IOPB)

Figure 6-8. Scatter/Gather List Address

Words 0xA - 0xB contain the number of elements in the scatter/gather list. Valid entries in this field are 1 to 256 (decimal).

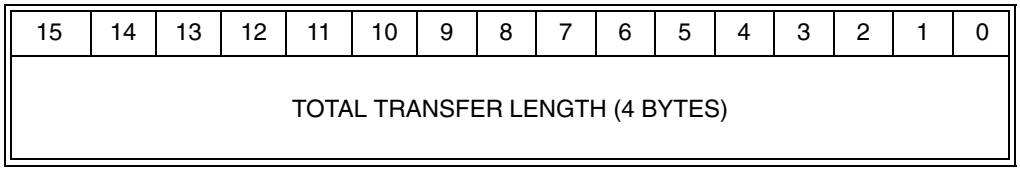
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(Words 0xA-0xB In The SCSI Pass-Through IOPB)

Figure 6-9. Scatter/Gather Element Count

Words 0xC - 0xD of the IOPB specify the sum of the individual element entry counts.



(Words 0xC-0xD In The SCSI Pass-Through IOPB)

Figure 6-10. Total Transfer Length For Scatter/Gather Operations

Scatter/Gather List

The scatter/gather option uses a list of elements to control the scatter/gather operation. Each element in the list specifies the byte count, address, memory type, and address modifier for each block of data in system memory that is to be transferred by one SCSI Pass-Through command. Each element in the list is an 8-byte entry. The format is as follows:

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WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ELEMENT 1 BYTE COUNT (2 BYTES)															
1 2	ELEMENT 1 BUFFER ADDRESS (4 BYTES)															
3	LNK	RESERVED					TT		MT		ADDRESS MODIFIER					



WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
n*4	ELEMENT N BYTE COUNT (2 BYTES)															
(n*4) +1 (n*4) +2	ELEMENT N BUFFER ADDRESS (4 BYTES)															
+3	LNK	RESERVED					TT		MT		ADDRESS MODIFIER					

Figure 6-11. Scatter/Gather Element List Format

This scatter/gather list can have from 1 to 255 elements. Using scatter/gather for lists with just one element, however, would be inefficient.

Scatter/Gather List Linking

To facilitate larger scatter/gather lists, any element in the scatter/gather list may contain a LINK bit. When LINK (bit 15) is set, the element structure will contain information that points to the next group of scatter/gather elements. An element that forms a link should have the following structure:

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WORD #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	RESERVED								SCATTER/GATHER COUNT							
0x1 0x2	SCATTER/GATHER LIST ADDRESS															
0x3	LNK	RESERVED			TT		MT		ADDRESS MODIFIER							

LNK == 1

Figure 6-12. Link Element Structure

The scatter/gather count field contains the number of elements in the next link to be gathered by the board. Valid Counts are 1 to 256.

If scatter/gather list linking is used, all lists must be built at the time the IOPB is issued. In addition, the Total Transfer Count field in the IOPB must be contain the sum of all individual data element counts (it should not contain the link element counts).

Printer Port Operation

The board's printer port allows the host to transfer data to either a Centronics or Dataproducts short line interface printer. A version is also available for use with a Dataproducts Long Line interface.

The printer port is a daughter card that attaches to the board. To execute a print command, the host issues an IOPB to Port 1 in much the same fashion as it would to a SCSI device. With the printer port installed, Port 1 is dedicated to the printer and cannot be used for SCSI transactions.

When sending data to the printer, the board DMAs the printer data from host memory, transfers it to the printer via Port 1, and then returns a completion status. Printer status may be monitored a synchronously at any time by the host. The host may also request that the board interrupt the host when a status change occurs. The printer port does not affect the normal operation of the primary SCSI port (Port 0).

Verifying Printer Port Installation

Once the host has initialized the board, it can verify that the printer port is installed by checking the Daughter Card ID field in Configuration Status Block. The printer port identification code (0x04) should be stored in this field. For information on setting the port's jumpers and termination, refer to the installation chapter.

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Initializing The Port

The printer port requires a separate work queue. It will therefore be necessary to create a work queue for it using the Initialize Work Queue command, just as you would for a SCSI device. This work queue must be exclusively used for the printer port.
The first command to the printer work queue should be the Initialize Printer Port command. This command sets a variety of parameters, including: 1) the polarity of parity for Dataproducts printers, and 2) which printer status lines may generate a status change interrupt.

The Initialize Printer Port command can be issued at any time to reset the printer port. The command is issued with the reset bit set to clear the printer port hardware. It should never be necessary to reset the hardware. The command may also be issued at any time to assert a buffer clear to the printer. Since the time required for holding this signal varies from printer to printer, the board will leave the line set until the host issues another Initialize Printer Port command with the bit cleared.

Issuing Printer Commands

The board will queue printer commands (see Printer Port IOPB) as received and work on each command in a FIFO manner as the previous command completes. When the Go/Busy bit for a printer command is set, the command will be copied from short I/O space into the internal printer port work queue. After the IOPB has been parsed for correctness, the data will be simultaneously DMA'd from system memory. When all the data has been transferred to the printer, a copy of the IOPB modified with the current printer status and return code will be placed in the Command Response Block.

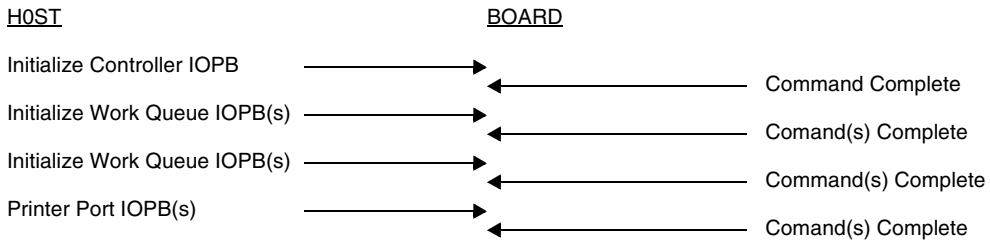


Figure 6-13. Example Of Printer Port Operation

If the printer port is configured for the Dataproducts interface, the host may want to send special font or control characters to the printer using the Paper Instruction control line of the Dataproducts interface. The board supports this with the Paper Instruction option in the IOPB. When the Paper Instruction option is set to 1, the board will transfer all of the data specified in this IOPB to the printer with the Paper Instruction interface signal active. Paper Instruction is only supported by Dataproducts printers.

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Status Reporting

The printer status may be accessed in three ways from the board:

- The state of the status lines is updated periodically in Configuration Status Block for asynchronous monitoring by the host. This status is stored in the Secondary Phase Sense/ Printer Status field of the Configuration Status Block. For a Dataproducts interface, this byte is updated whenever Online, Ready, Parity Error, or Cable On changes state. For a Centronics interface, it is updated anytime Select, Fault, or Paper Empty changes state. For all interfaces, it is also updated approximately every 30 msec, as well as at the completion of a print command.

- The second method is for the board to use the Controller Normal Interrupt Vector specified in word 0x2 of the Controller Initialization Block. The host may select which status lines can generate an interrupt in the Initialize Printer Port IOPB. An interrupt is generated when an enabled status line (except parity) toggles either active or inactive. Parity error is only reported when it becomes active. The complete status word will be updated in Configuration Status Block, and a Command Response Block will be posted. This returned structure is shown in Chapter 3.

- The third method for accessing printer information is to issue a Printer Port IOPB with both the Maximum Transfer Length and the Printer Transfer Length fields set to zero. This causes the printer port to update the Printer Status field of the IOPB and immediately return it as command completed.

Offboard IOPBs

The board's MACSI interface is optimum for systems that have quick host access to the VME Short I/O space. In some systems, however, reading and writing data to/from this space can be quite time consuming. To speed up I/O in such systems, the board supports a technique that enables the host to control the board with just two reads and two writes into the board's short I/O space for each command. This technique involves building Offboard Command Queue entries, IOPBs, and an Offboard Command Response Block.

NOTE: In order execute Offboard IOPBs, the board must be able to access the host memory using its DMA facility.

Overview

In order to implement Offboard IOPBs, you will need to allocate one or more blocks of system memory for sole use by these structures. The board's onboard Command Queue entries can then be initialized to point to these fixed areas of memory. The host builds offboard IOPBs and Command Queue entries in this space. The only time it accesses the board's onboard Command Queue entry is to set the Go/Busy bit.

NOTE: These pointers should not be changed once normal board operation has begun.

The board then DMAs the offboard CQE/IOPB onboard and executes the command. Upon completion of this command fetch, the board clears the Go/Busy bit in the onboard Command Queue entry.

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Building Offboard IOPBs

To build an offboard IOPB, set the Fetch Offboard IOPB bit (bit 4) in the Queue Entry Control Register. This is the first word of the onboard Command Queue entry. Setting this bit changes the purpose of the fields within the Command Queue entry, but it does not change the size of the Command Queue entry.

When bit 4 is set, the board interprets the address in the onboard Command Queue entry as a pointer to a block of offboard memory consisting of an external Command Queue and one or more Command Queue entries.

Offboard Command Queue entries and IOPBs have the same structure as their onboard counterparts, except that the IOPB Address field in an offboard Command Queue entry has no meaning.

The format of an offboard Command Queue entry is shown below:

WORK #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	QUEUE ENTRY CONTROL REGISTER															
0x1	RESERVED						TT		MT		ADDRESS MODIFIER					
0x2 0x3	HOST MEMORY ADDRESS															
0x4	IOPB LENGTH								RESERVED							
0x5	RESERVED															

Figure 6-14. Format Of Offboard Command Queue Entry

Note the following important restrictions when building offboard Command Queue entries/IOPBs:

- Each offboard Command Queue entry must be contiguous with its corresponding offboard IOPB in system memory (with the Command Queue entry residing in the *lower* portion of the block of memory).

- Because a single DMA operation of the board cannot cross nonadjacent page boundaries, an offboard Command Queue entry and its corresponding IOPB cannot be spread across two nonadjacent pages in physical memory.

The host may mix onboard and offboard commands by setting (or clearing) the FOB Bit in the Queue Entry Control Register of individual commands. However, this is not recommended for normal operation. It may be useful for handling errors or when operating the board in a stand alone fashion.

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Initializing Offboard Commands

To initiate a command, the host: 1) reads the Go/Busy bit of the next Command Queue entry to ensure that the entry is available, and 2) sets that same Go/Busy bit after it has assembled the offboard Command Queue entry and IOPB.

If there is no external memory at the location specified in the Command Queue entry, the board will get a VME bus error (BERR*) when it tries to read the offboard Command Queue entry/IOPB. In this event, the board uses the default Error Level/Vector in the Controller Initialization Block and places the Command Queue entry/IOPB at the normal Command Response Block (CRB) location in short I/O.

Offboard Command Response Block

In order for the board to write a returned IOPB offboard, you need to designate a block of system memory for use as an offboard Command Response Block. Then, write a pointer to the block in the Controller Initialization Block, and execute the Initialize Controller command. Any non-zero value in the pointer field instructs the board to write returned IOPBs to the offboard address.

Refer to Chapter 3 for additional information on the Command Response Block and *Controller Initialization* in Chapter 5 for additional information on the Controller Initialization Block.

Once you have initialized the board to write command responses to an offboard Command Response Block, all responses will be written to this structure unless a bus error occurs during the write operation.

Posting Command Completion

If the pointer to the external Command Response Block in the Controller Initialization Block is zero, then the board posts command response information in the Command Response Block section of its own short I/O space.

Once it completes a command, the board DMAs the command response information into external memory and then generates a Command Complete Interrupt.

NOTE: Before reading the command response information in its own memory, the host should first read error status in the board's onboard Command Response Block (this information is inaccessible once the board's CRBV bit is cleared.) If an error occurs, the location of the Command Response Block will depend on the type of error. If the error is a SCSI device error, the Command Response Block/returned IOPB will be written offboard to the address specified in the Controller Initialization Block.

On the other hand, if the error status shows that a bus error (BERR*) occurred when attempting to move the information into the offboard Command Response Block, then the host can find the Command Response Block and IOPB in short I/O at the address specified in the Command Response Block specified in Word 0x6 of the Controller Initialization Block offset).

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After checking the error status, the host can respond to the interrupt by clearing the CRBV bit (Command Response Block Valid) in the Command Response Status Word of the board's onboard Command Response Block.

Considerations For Maximizing SCSI Synchronous Data Transfers

Synchronous data throughput in a SCSI system can be significantly improved by better matching the data transfer rates of the host adapter and SCSI devices. This is because SCSI devices support specific data transfer rates within the broad SCSI spectrum. When a synchronous data transfer takes place between two SCSI devices, these devices must negotiate between themselves to select a compatible transfer rate. If the devices have incompatible transfer rates, the result is significantly lower cable bandwidth.

This section describes the key factors determining the actual speed at which two SCSI devices will perform a synchronous data transfer (as opposed to the rated maximum speeds of the individual devices). Since SCSI data transfer rates are negotiated in terms of *nanoseconds (ns) per period* instead of *frequency*, this discussion uses the SCSI transfer period to describe transfer rates. The SCSI transfer period is measured in 4 nanosecond increments. A resolution of 4ns results in some strange and difficult to read numbers when converted to the equivalent frequency. Just remember that a smaller period means a higher frequency, and a larger period means a lower frequency (F=1/T)

Negotiation Process For Synchronous Transfer Rates

As noted above, the host adapter and target negotiate the maximum transfer rate that may be used in data transfers. The negotiation process, which usually occurs the first time the host adapter communicates with a target, is essentially as follows:

1. The host adapter tells the target the smallest transfer period at which the host adapter is able to operate.

2. The target evaluates the received value.

    - If the proposed value is acceptable, the target returns it to the host adapter and the negotiation process is finished.

    - If the value is less than the target can handle, the target sends the host adapter the smallest transfer period at which it can function. The host adapter then accepts that as the correct value, and the negotiation is finished.

Once a data transfer rate has been determined, all subsequent data transfers between the host adapter and target have a transfer period greater than or equal to the agreed-upon value.

For example, consider a 4 Mbyte/sec. host adapter connected to a 4 Mbyte/sec. disk drive. A problem arises in that a 250ns period is not evenly divisible into the 4ns increments required by SCSI. Therefore, some devices express this value as 248ns, while others use 252ns.

Assume that both devices use a 248ns period. In this case, the pair will communicate at 4 Mbytes/sec., because both devices are allowed to transfer at a period greater than the agreed-upon value.

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On the other hand, if the host adapter uses 248ns and the drive uses 252ns, the cable rate must be less than 4 Mbytes/sec. The 4-nanosecond difference in periods is significant because devices do not actually support 4ns steps in transfer rates. The transfer rate is usually determined by some division of the oscillator which drives the SCSI controller of the device. Assuming that the SCSI controller is driven by a frequency that is twice the agreed-upon transfer rate, the next lower rate will be three times the input oscillator. In the example we are currently considering, this would mean that the host adapter must operate at 375ns periods or 2.66 Mbytes/sec., considerably less than the 4 Mbyte/sec. maximum rate.

The matching of device data transfer rates becomes particularly important when using the same cable to interconnect targets that have different maximum speeds. With this setup, the overall system transfer rate is determined by the transfer rates negotiated between the host adapter and each of the devices connected to it. The table below lists a variety of "typical" SCSI drives and host adapters, along with their associated transfer rates. It is followed by examples of the actual transfer rates that would be negotiated between different host adapters and drives in the following table.

Table 6-3. Transfer Periods Of Example SCSI Host Adapters And Drives

SCSI Device	Maximum Transfer Rate of Device	Transfer Rate if Target Device Cannot Transfer at Maximum Rate
Drive 1	212ns (4.72 Mhz)	252ns (3.97 Mhz)
Drive 2	208ns (4.81 Mhz)	248ns (4.03 Mhz)
Host Adapter 1	248ns (4.03 Mhz)	375ns (2.66 Mhz)
Host Adapter 2	200ns (5.00 Mhz)	300ns (3.33 Mhz)
Host Adapter 3	208ns (4.81 Mhz)	312ns (3.21 Mhz)
Host Adapter 4	212ns (4.72 Mhz)	318ns (3.14 Mhz)

Example 1: Host Adapter 1, Drive 1 Transfer Rate 252ns:

The host adapter requests 248ns, which the drive accepts as this is greater than the drive's minimum 212ns period. The actual transfer rate paced by the drive is 252ns.

Example 2: Host Adapter 1, Drive 2 transfer rate 248ns:

The host adapter requests 248ns, which the drive accepts as this is greater than the drive's minimum 208ns period. The actual transfer rate paced by the drive is 248ns.

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Example 3: Host Adapter 2, Drive 1 transfer rate 300ns:

The host adapter requests 200ns, which the drive rejects as this is less than the drive's minimum 212ns period. The drive responds with 212ns. The host adapter must then transfer at its next greater period of 300ns.

Example 4: Host Adapter 2, Drive 2 transfer rate 300ns:

The host adapter requests 200ns, which the drive rejects as this is less than the drive's minimum 208ns period. The drive then responds with 208ns. The host adapter must then transfer at its next greater period of 300ns.

The resulting transfer rates for the remaining combinations are as follows:

- Host Adapter 3, Drive 1 transfer rate 312ns
- Host Adapter 3, Drive 2 transfer rate 208ns
- Host Adapter 4, Drive 1 transfer rate 212ns
- Host Adapter 4, Drive 2 transfer rate 248ns

The above examples show that it is possible to achieve similar performance from the two example drives with a 4 Mbyte/sec. host adapter. However, if the speed of the host adapter is increased, it is not possible to achieve greater performance from both drives on the same cable. Some combinations actually hurt performance for some drives.

This problem is the result of devices having a finite number of actual transfer rates while the SCSI specification allows a large number of legal values. It is therefore very important that the system integrator carefully choose devices with compatible transfer rates to achieve maximum performance.

Downloading Firmware

The Download Firmware command allows systems incorporating the controller to update controller firmware without physically replacing the EPROM, either by reprogramming a flash EPROM, or by replacing the currently executing firmware memory image.

This command allows systems to update the firmware on a controller that is concurrently running systems level activity, such as filesystem reads, and writes. This allows the firmware to be updated on the same controller that is hosting the storage media containing the new image.

This command will reduce the chances of attempting to load an incorrect image, since failure to program the flash EPROM correctly requires replacement of the part: there is no way to recover from errors once the part has been misprogrammed. Thus, it is necessary to take extreme caution to ensure the integrity of the new firmware load, as well as the correct sequencing of the steps necessary to achieve a download.

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Using this command, the host computer first informs the board that it intends to download new firmware. It then transfers the new firmware one packet at a time. The board takes these packets, verifies the integrity of each one, and constructs a new memory image in the local buffer memory area. After the entire image has been constructed, the host issues a command to either program the flash EPROM, or to replace the currently executing program image with the downloadable image. If the board has detected no internal inconsistencies in the buffer memory image that has been created, it performs either the Program Flash or Program Memory command.

Upon receiving a Program Flash command, the board loads the new image into flash EPROM. The next time the board is reset, execution will occur from this new image. Until the board is reset, execution will occur from the old image, with all commands returned with an appropriate exception notification that the executing image fails to match the stored EPROM image. This allows filesystems to be mounted on a board that has been updated, which can be shut down in an orderly fashion, and the system reset.

Upon receiving a Program Memory command, the board will replace the currently executing image with the new image, which will effect a "warm boot", which will appear to the host identical to a Reset Controller command, issued through the Master Control Register. At this point, the host will need to initialize the controller again, and all work queues before submitting additional commands.

This command (facility) requires the following:

- Minimum of 256K of Local Buffer Memory
- Installation of flash EPROM, with associated hardware change (zero ohm register installed), for Program Flash capability only.

To download new firmware to the board, the host needs to start with a file containing an encoded copy of the firmware image. Currently, the only encoding format supported is Motorola S-records. Since the download facility allows the board to support normal operations while performing the host download, it is possible to access this image from a device currently running on the board to be updated.

First, the host initiates the download by submitting the Host Download command specifying the Initialize Download sub-command and set Initialize Download (ID) Bit 4:

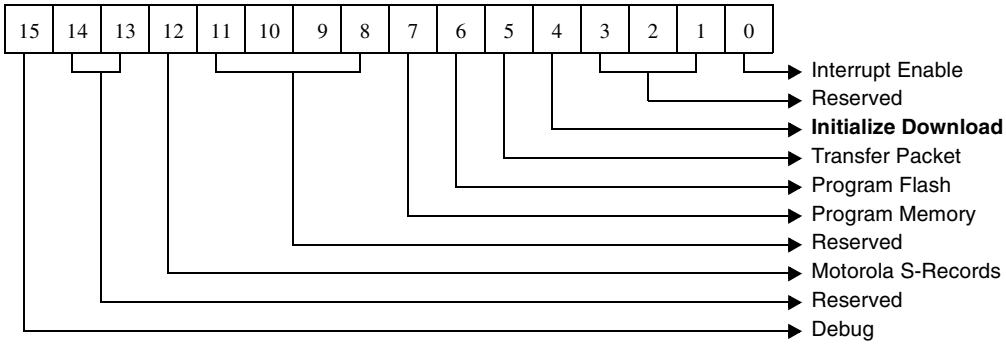


Figure 6-15. Command Options For Download Firmware Command (Bit 4).

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If this command is successful, the board will return the IOPB using the Normal Completion Vector (assuming that Interrupts are enabled). If the board does not have the correct hardware support for Host Download, the IOPB will be returned with the Incorrect Hardware error code.

Next the host downloads the code, using a series of Transfer Packet sub-commands (Set Transfer Packet (TP) Bit 5):

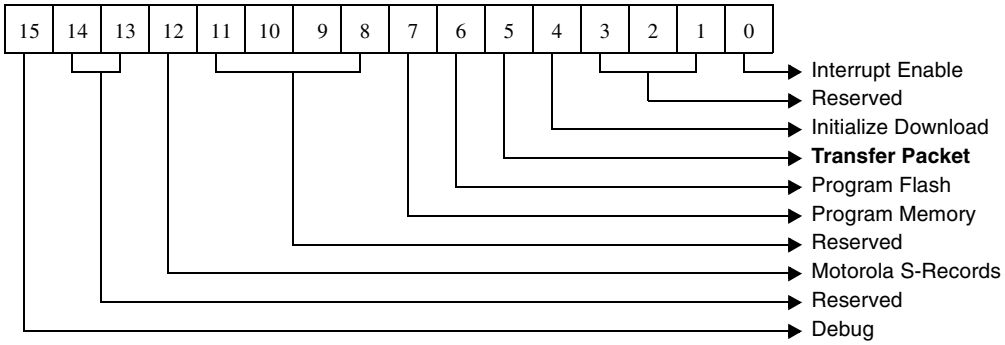


Figure 6-16. Command Options For DownLoad Firmware Command (Bit 5).

Transfer Count: Fill in the number of bytes to be transferred in this packet.

Buffer Address: Fill in the starting physical (VMEbus) address location of the data. Note that this address plus the transfer length must exist in a contiguous space; this IOPB does not support scatter/gather lists.

Check Sum: This field is set to zero.

Sequence Number: Fill in the packet sequence number. All packets must be submitted to the board in order, with the first Transfer Packet sub-command employing sequence number one (1).

A Transfer Packet sub-command may fail for a number of reasons. Refer to Chapter 5 (Command Set) for details on the types of errors returned and associated conditions. Once an error has occurred, the board will abort the entire download procedure, and reset all internal state associated with the process. At this point, the only Host Download sub-command with meaning is the Initialize Download sub-command, errors are recoverable, and no permanent damage has been done to the electrical system requiring physical intervention.

After all packets have been transferred, the host may begin loading the transferred image into Flash EPROM by issuing a Program Flash sub-command (Set Program Flash (PF) Bit 6):

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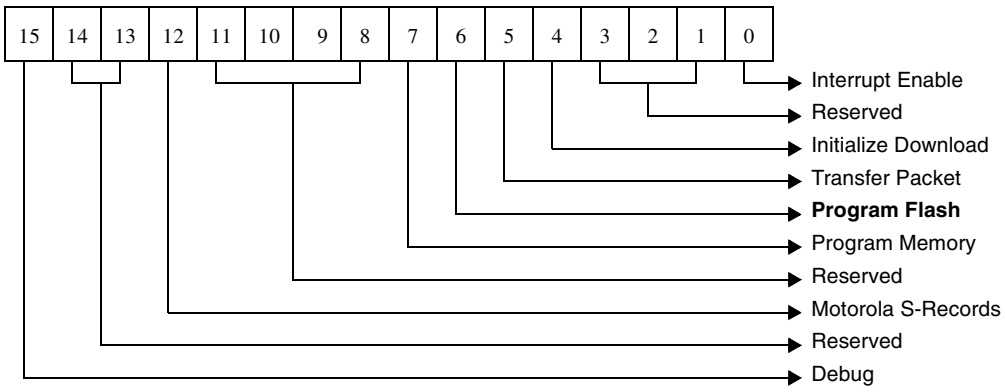


Figure 6-17. Command Options For Download Firmware Command (Bit 6)

Transfer Count: Fill in the total number of bytes in the firmware load file that were transferred to the board.

Sequence Number: Fill in the total number of packets sent.

If there are any detectable errors up to this point, the board will return the IOPB with an error status code: if that code is not Bad EPROM Load (0x9c), the process will be aborted, and the board remains intact, but as yet, not updated.

If, however, the Bad EPROM Load error code is returned, the board attempted to program the flash EPROM, and failed. In this case, the EPROM has been damaged beyond recovery, and the physical replacement of this part is required. With the error detection and protocol constraints imposed on this process, this failure should only occur as a result of internal hardware problems within the board which would require direct attention. However, the board will continue to operate, using the old version of firmware currently running in static RAM memory, until the next board reset.

After transferring the data, the host may issue a Program Memory sub-command. The image file for this is different than that for Program Flash (Set Program Memory (PM) Bit 7):

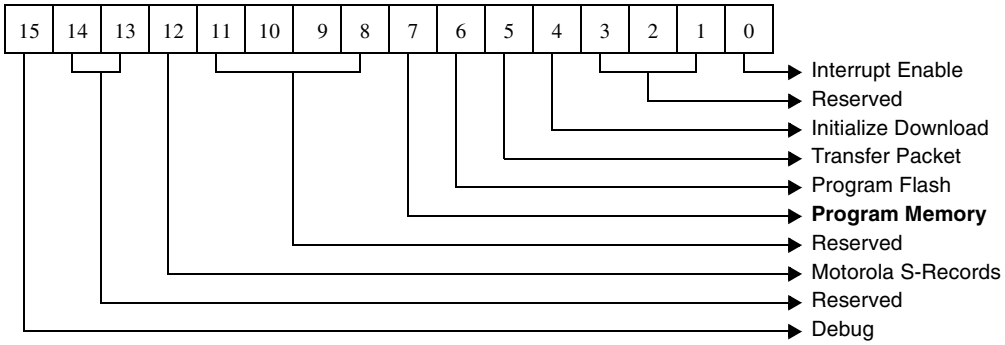


Figure 6-18. Command Options For Download Firmware Command (Bit 6).

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Since there is no return from this command, there is no reason to fill in the other fields required by the Program Flash command. Errors for this command are not fatal; issuing a Reset Controller will reload the old version of firmware from the EPROM, and restart the controller using the same firmware that was used to download the code.

After the Program Memory sub-command, the board will attempt to replace the currently executing program image with the new downloaded image. In all cases, the contents of the Short I/O will be invalidated. The Host Download IOPB encapsulating this sub-command will not be returned to the host. If the board successfully loads the new program image, the Board OK bit will be set in the Master Status Register, and the host will be able to initialize the controller, just as was done during system initialization. If the image load fails, the Controller Not Available bit will remain set in the Master Status Register. In this case, issuing a Controller Reset, through the Master Control Register will cause the old program image to be loaded from EPROM.

System Interface

This command fully employs the normal CQE/IOPB command mechanism provided by the board. This includes off-board location of both the IOPB and the returned CRB.

This Host Download IOPB does not support scatter/gather lists, but requires all data associated with a single IOPB to be located in contiguous memory locations. Since the memory image may be transferred using multiple transactions between the host and the board, it is not necessary for the entire image to reside in contiguous memory.

All Host Download IOPB's are returned as any other IOPB, using the normal or error vector and interrupt level if specified, except the IOPB associated with the Program Memory sub-command. When issuing a Program Memory sub-command, no IOPB will be returned, nor interrupt issued. The board will appear to have been reset, and will need to be initialized again.

MACSI SCSI Synchronous Options

Since these parameters are at the end of the CIB, the CIB length parameters, Maximum Transfer Length in the Initialize Controller command must be specified correctly. The board will use this value to tell whether or not to interpret the extra two words as SCSI control parameters.

The host may read the Device Negotiation Rate information in CSS to verify the results of setting the Negotiation Rate parameter.

There is no way other than using a SCSI bus analyzer to evaluate the effect of setting the Synchronous Offset parameter. It is assumed that this would not be set without first consulting such a device.

Board Identification In MACSI CSS

The host may use the contents of this field to determine if a particular installed controller is a 4220 Cougar II controller.

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Appendix A
Specifications

VMEbus Specifications

DTB Master	A16, A24, A32, D08 (EO), D16, D32: BLT, D64: BLT
DTB Slave	A16, D08 (EO), D16
Requester	Any of R (0-3), Static RWD, ROR
Interrupter	Any of I (1-7), Dynamic D08 (0)

SCSI Bus Specifications

Peripheral Data Rate	Up to 10Mbytes/sec synchronous Up to 5Mbytes/sec asynchronous

Power Requirements

Single-Ended V/SCSI-2 4220 Wide Motherboard	5.8A typical @ +5V DC (+/- 5%) 6.8A maximum @ +5V DC (+/- 5%) 7.0mA maximum @ +12V DC (+/- 5%) 30mA maximum @ -12V DC (+/- 5%)
Differential V/SCSI-2 4220 Wide Motherboard	6.0A typical @ +5V DC (+/- 5%) 7.00A maximum @ +5V DC (+/- 5%) 7.0mA maximum @ +12V DC (+/- 5%) 30mA maximum @ -12V DC (+/- 5%)
Single-ended V/SCSI-2 4220 Wide Daughter Card	TBD
Differential V/SCSI-2 4220 Wide Daughter Card	.65A typical @ +5V DC (+/- 5%) .90A maximum @ +5V DC (+/- 5%)
Single-ended V/SCSI-2 4220 Daughter Card	.08A typical @ +5V DC (+/- 5%) .15A maximum @ +5V DC (+/- 5%)
Differential V/SCSI-2 4220 Daughter Card	.65A typical @ +5V DC (+/- 5%) .90A maximum @ +5V DC (+/- 5%)
Centronics/Dataproducts Shortline Printer Port Daughter Card	.70A typical & +5V DC (+/- 5%) 1.0A maximum & +5V DC (+/- 5%)

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Dataproducts Longline Printer Port Daughter Card	0.9A typical 1.3A maximum

Mechanical (Nominal)

Length	233 mm
Width	160 mm
Thickness	20 mm
Weight	.45 Kg

Operating Environment

Temperature	0-55 degrees Centigrade
Relative Humidity	10% - 90% Noncondensing
Air Flow	250 CFM Minimum

Reliability

MTBF per Bellcore 3.0 TSY-000332

Single-Ended V/SCSI-2 4220 Wide Motherboard	214.5K Hours
Differential V/SCSI-2 4220 Wide Motherboard	203.3K Hours
Single-Ended V/SCSI-2 4220 Cougar II Motherboard	238K Hours
Differential V/SCSI-2 4220 Cougar II Motherboard	169.4K Hours

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Appendix B
Connector Pinouts and Cabling

Overview

This appendix contains the connector pinouts and cabling information needed for various Cougar II configurations. Please refer to the SCSI-2 Specification for more information on cabling. The tables in this appendix are listed below.

SCSI Channels

- Single-Ended Contact Assignments - SCSI "A" Cable
- Single-Ended Contact Assignments - SCSI "P" Cable
- Differential Contact Assignments - SCSI "A" Cable
- Differential Contact Assignments - SCSI "P" Cable

RS232 Connector And Cable Pinouts

- Serial Connector Pinouts (SPA And SPB)
- Suggested RS232 Cable Pinout

P1 and P2 Connectors

- P1 Connector Signal Descriptions
- P2 Connector Signal Descriptions

P9 Connectors And Cable Pinouts

- Cable Pinouts For P9 Connector To Dataproducts Short Line Printer
- Cable Pinouts For P9 Connector To Dataproducts Long Line Printer
- Cable Pinouts For P9 Connector To Centronics Printer

Description of SCSI Cables

SCSI "P" Cable

The Cougar II Wide motherboard and optional Cougar II Wide SCSI daughter card require a standard SCSI-2 "P" cable. The single-ended pinout of the cable is shown on page and the differential is on page .

The cable must have a 68-pin subminiature "D" style connector that mates with the same type connector (P8) on the motherboard (or daughter card). Both 8- and 16-bit SCSI devices can be connected to the "P" cable.

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SCSI "A" Cable

If the board has a Cougar II SCSI daughter card, use a standard SCSI "A" cable to connect it to the devices on channel 1. Only 8-bit SCSI devices can be connected to the "A" cable. The single-ended pinout of the cable is shown on page and the differential is on page .

The SCSI "A" cable is either a 50-conductor flat cable or a 25-signal twisted-pair cable. It is one-to-one, with 50-pin connectors on both ends. As per SCSI specifications, the cable can be up to 20 feet long (6 meters) for a single-ended SCSI bus and 82 feet long (25 meters) for a differential bus.

Below is a list of sample part numbers for the SCSI "A" cable which you may find to be useful in cabling your system. **Interphase assumes no responsibility regarding the functionality of the parts listed below. If you need more information concerning the parts, contact the manufacturer directly.**

SCSI "A" Cable Component	Sample Part No.
Flat Cable	3M-3365-50
Connectors	
• End of cable connector	
– Without strain relief; no center key	3M-3425-7000
– With strain relief; no center key	3M-3425-7050
– Without strain relief; with center key	Dupont 66900-290
• Daisy Chain	
– Without strain relief; no center key	3M-3425-6000
– With strain relief; no center key	3M-3425-6050
– Without strain relief; with center key	Dupont 66900-250

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Single-Ended SCSI Cable Pinout

Table B-28. Single-Ended Contact Assignments - SCSI "A" Cable

Pin	Mnemonic	Pin	Mnemonic
1	GND	2	DB0-
3	GND	4	DB1-
5	GND	6	DB2-
7	GND	8	DB3-
9	GND	10	DB4-
11	GND	12	DB5-
13	GND	14	DB6-
15	GND	16	DB7-
17	GND	18	DBP-
19	GND	20	GND
21	GND	22	GND
23		24	
25		26	TERMPWR
27		28	
29	GND	30	GND
31	GND	32	ATN-
33	GND	34	GND
35	GND	36	BSY-
37	GND	38	ACK-
39	GND	40	RST-
41	GND	42	MSG-
43	GND	44	SEL-
45	GND	46	C/D-
47	GND	48	REQ-
49	GND	50	I/O-

NOTE: If no signal is referenced, the Cougar does not use that pin.

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Table B-29. Single-Ended Contact Assignments - SCSI "P" Cable

SIGNAL NAME	CONNECTOR CONTACT NUMBER	CABLE CONDUCTOR NUMBER		CONNECTOR CONTACT NUMBER	SIGNAL NAME
GROUND	1	1	2	35	-DB (12)
GROUND	2	3	4	36	-DB (13)
GROUND	3	5	6	37	-DB (14)
GROUND	4	7	8	38	-DB (15)
GROUND	5	9	10	39	-DB (P1)
GROUND	6	11	12	40	-DB (0)
GROUND	7	13	14	41	-DB (1)
GROUND	8	15	16	42	-DB (2)
GROUND	9	17	18	43	-DB (3)
GROUND	10	19	20	44	-DB (4)
GROUND	11	21	22	45	-DB (5)
GROUND	12	23	24	46	-DB (6)
GROUND	13	25	26	47	-DB (7)
GROUND	14	27	28	48	-DB (P)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	-BSY
GROUND	24	47	48	58	-ACK
GROUND	25	49	50	59	-RST
GROUND	26	51	52	60	-MSG
GROUND	27	53	54	61	-SEL
GROUND	28	55	56	62	-C/D
GROUND	29	57	58	63	-REQ
GROUND	30	59	60	64	-I/O
GROUND	31	61	62	65	-DB (8)
GROUND	32	63	64	66	-DB (9)
GROUND	33	65	66	67	-DB (10)
GROUND	34	67	68	68	-DB (11)

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NOTES

(1) The minus sign next to a signal indicates active low.
(2) The conductor number refers to the conductor position when using 0.025 inch centerline flat ribbon cable. Other cable types may be used to implement equivalent contact assignments.
(3) Devices which connect to the P-cable shall leave the following signals open: -DB(12), -DB(13), -DB(14), -DB(15), -DB(P1), -DB(8),-DB(9), -DB(10), and -DB(11).

All other signals shall be connected as defined.

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Differential SCSI Cable Pinout

Table B-30. Differential Contact Assignments - SCSI "A" Cable

Pin	Mnemonic	Pin	Mnemonic
1	SHIELD	2	GND
3	DB0+	4	DB0-
5	DB1+	6	DB1-
7	DB2+	8	DB2-
9	DB3+	10	DB3-
11	DB4+	12	DB4-
13	DB5+	14	DB5-
15	DB6+	16	DB6-
17	DB7+	18	DB7-
19	DBP+	20	DBP-
21		22	GND
23		24	
25	TERMPWR	26	TERMPWR
27		28	
29	ATN+	30	ATN-
31	GND	32	GND
33	BSY+	34	BSY-
35	ACK+	36	ACK-
37	RST+	38	RST-
39	MSG+	40	MSG-
41	SEL+	42	SEL-
43	C/D+	44	C/D-
45	REQ+	46	REQ-
47	I/O+	48	I/O-
49	GND	50	GND

NOTE: If no signal is referenced, the Cougar does not use that pin.

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Table B-31. Differential Contact Assignments - SCSI "P" Cable

SIGNAL NAME	CONNECTOR CONTACT NUMBER	CABLE CONDUCTOR NUMBER		CONNECTOR CONTACT NUMBER	SIGNAL NAME
+DB (12)	1	1	2	35	-DB (12)
+DB (13)	2	3	4	36	-DB (13)
+DB (14)	3	5	6	37	-DB (14)
+DB (15)	4	7	8	38	-DB (15)
+DB (P1)	5	9	10	39	-DB (P1)
GROUND	6	11	12	40	GROUND
+DB (0)	7	13	14	41	-DB (0)
+DB (1)	8	15	16	42	-DB (1)
+DB (2)	9	17	18	43	-DB (2)
+DB (3)	10	19	20	44	-DB (3)
+DB (4)	11	21	22	45	-DB (4)
+DB (5)	12	23	24	46	-DB (5)
+DB (6)	13	25	26	47	-DB (6)
+DB (7)	14	27	28	48	-DB (7)
+DB (P)	15	29	30	49	-DB (P)
DIFFSENS	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
+ATN	20	39	40	54	-ATN
GROUND	21	41	42	55	GROUND
+BSY	22	43	44	56	-BSY
+ACK	23	45	46	57	-ACK
+RST	24	47	48	58	-RST
+MSG	25	49	50	59	-MSG
+SEL	26	51	52	60	-SEL
+C/D	27	53	54	61	-C/D
+REQ	28	55	56	62	-REQ
+I/O	29	57	58	63	-I/O
GROUND	30	59	60	64	GROUND
+DB (8)	31	61	62	65	-DB (8)
+DB (9)	32	63	64	66	-DB (9)
+DB (10)	33	65	66	67	-DB (10)
+DB (11)	34	67	68	68	-DB (11)

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NOTES

(1) The conductor number refers to the conductor position when using 0.025- inch centerline flat ribbon cable. Other cable types may be used to implement equivalent contact assignments.

(2) 8 bit devices which connected to the P-cable shall leave the following signals open: -DB(12), -DB(13), -DB(14), -DB(15), -DB(P1), -DB(8),-DB(9), -DB(10), -DB(11), +DB(12), +DB(13), +DB(14), +DB(15), +DB(P1), +DB(8), +DB(9), +DB(10) and +DB(11)

All other signals shall be connected as defined.

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RS232 Connector and Cable

Table B-32. Serial Connector Pinouts (SPA and SPB)

PIN	MNEMONIC	TYPE	DESCRIPTION
1	-	-	Unconnected (DCD)
2	DSR	I	Data Set Ready
3	RXD	I	Receiver Data Input
4	RCTS	I/O	RTS/CTS, (shorted to pin 6)
5	TXD	O	Transmitter Data Output
6	RCTS	I/O	RTS/CTS, (shorted to pin 4)
7	DTR	O	Data Terminal Ready
8	-	-	Unconnected (RI)
9	GND	-	Signal Ground
10	-	-	Unconnected

The same cable for the second Serial Port for PC compatible systems can be used for the V/SCSI-2 4220 Cougar II. This cable can be built or bought off-the-shelf from many computer stores. The cable pinout is shown in the following table:

Table B-33. Suggested RS232 Cable Pinout

10-PIN	DB-25 PIN	MNEMONIC	DESCRIPTION
1	8	DCD	Data Carrier Detect
2	6	DSR	Data Set Ready
3	3	RXD	Receiver Data Input
4	4	RTS	Request to Send
5	2	TXD	Transmitter Data
6	5	CTS	Clear To Send
7	20	DTR	Data Terminal Ready
8	22	RI	Ring Indicator
9	7	GND	Signal Ground
10	-	-	Unconnected

Both RS232 ports on the Cougar are configured as Data Terminal Equipment (DTE). With this connector and cable configuration, a NULL modem cable may be required to connect a terminal to the board.

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P1 Connector

Table B-34. VMEbus P1 Connector

Pin	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	DOO	BBSY*	DO8
2	DO1	BCLR*	DO9
3	DO2	ACFAIL*	D1O
4	DO3	BG0IN*	D11
5	DO4	BG0OUT*	D12
6	DO5	BG1IN*	D13
7	DO6	BG1OUT*	D14
8	DO7	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE	BR2*	AM5
15	GND	BR3*	A23
16	DTACK	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	AO6	IRQ6*	A13
26	AO5	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V DC		+12V DC
32	+5V DC	+5V DC	+5V DC

NOTE: If no signal is referenced, the Cougar does not use that pin. A "*" denotes an active low signal.

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P2 Connector

Table B-35. VMEbus P2 Connector (Row B Only Motherboards)

Pin	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1		+5V DC	
2		GND	
3			
4		A24	
5		A25	
6		A26	
7		A27	
8		A28	
9		A29	
10		A30	
11		A31	
12		GND	
13		+5V DC	
14		D16	
15		D17	
16		D18	
17		D19	
18		D20	
19		D21	
20		D22	
21		D23	
22		GND	
23		D24	
24		D25	
25		D26	
26		D27	
27		D28	
28		D29	
29		D30	
30		D31	
31		GND	
32		+5V DC	

NOTE: If no signal is referenced, then the board does not use that pin. Variations of the Cougar II that use P2 rows A and C are not currently available.

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Dataproducts Printer Cabling

This section applies only to motherboards which are set up to use the secondary channel (port 1) with a short line or long line Dataproducts printer. The printer port daughter card is installed and configured as described in the Installation chapter. This section does not apply to boards with a SCSI daughter card or no daughter card.

Dataproducts Cable Description

To connect a Dataproducts printer to the board, use a 50-conductor flat ribbon cable with a 50-pin connector that mates with the J9 connector of the printer daughter card installed on the board. Refer to the list below for sample cable/connector part numbers.

The cable pinouts depend on the type of Dataproducts printer being used: short line or long line. The pinout for Short Line printers is shown in. The Longline pinout appears in.

The following is a list of sample part numbers which you may find to be useful to make the printer cable. **Interphase assumes no responsibility regarding the functionality of the parts listed below. If you need more information concerning the parts, contact the part manufacturer directly.**

Component	Sample Part No.
Flat Cable	3M-3365-50
Connectors	
• Motherboard End without strain relief; with center key	Dupont 66900-290
• Dataproducts End	T&B Ansley 609-50P

NOTE

The connector type needed for your specific Dataproducts printer may be different from that given above. Be sure to verify your printer's connector requirements before making the cable.

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Table B-36. Cable Pinouts for P9 Connector to Dataproducts Short Line Printer

4220 P9	Dataproducts (Short Line)	Function	4220 P9	Dataproducts (Short Line)	Function
6	19	DATA 1	11	37	RETURN
7	3	RETURN	42	31	BUFFER CLEAR
9	20	DATA 2	43	15	RETURN
10	4	RETURN			
1	1	DATA 3	15	22	READY
4	2	RETURN	16	6	RETURN
23	41	DATA 4	12	21	ON LINE
20	40	RETURN	13	5	RETURN
2	34	DATA 5	18	23	DEMAND
3	18	RETURN	19	7	RETURN
29	43	DATA 6	30	27	PARITY ERROR
26	42	RETURN	31	11	RETURN
8	36	DATA 7	24	25	BOTTOM OF FORM
5	35	RETURN	25	9	RETURN
33	28	DATA 8	27	26	PAPER MOVING
32	44	RETURN	28	10	RETURN
36	29	DATA PARITY	17	39	GROUND
37	13	RETURN	21	24	TOP OF FORM
39	30	PAPER INSTRUCTIONS	22	8	RETURN
40	14	RETURN	38	46	INTERFACE CONNECTED
14	38	DATA STROBE	35	45	INTERFACE CONNECTED RETURN

NOTE: If no signal is referenced, that pin is not used.

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Table B-37. Cable Pinouts For P9 Connector To Dataproducts Long Line Printer

4220 P9	Dataproducts (Long Line)	Function	4220 P9	Dataproducts (Long Line)	Function
6	19	DATA 1+	11	37	DATA STROBE-
7	3	DATA 1-	42	31	BUFFER CLEAR+
9	20	DATA 2+	43	15	BUFFER CLEAR-
10	4	DATA 2-			
1	1	DATA 3+	15	22	READY+
4	2	DATA 3-	16	6	READY-
23	41	DATA 4+	12	21	ON LINE+
20	40	DATA 4-	13	5	ON LINE-
2	34	DATA 5+	18	23	DEMAND+
3	18	DATA 5-	19	7	DEMAND-
29	43	DATA 6+	30	27	PARITY ERROR+
26	42	DATA 6-	31	11	PARITY ERROR-
8	36	DATA 7+	24	25	BOTTOM OF FORM+
5	35	DATA 7-	25	9	BOTTOM OF FORM-
33	28	DATA 8+	27	26	PAPER MOVING+
32	44	DATA 8-	28	10	PAPER MOVING-
36	29	DATA PARITY+	17	39	GROUND
37	13	DATA PARITY-	21	24	TOP OF FORM+
39	30	PAPER INSTRUCTIONS+	22	8	TOP OF FORM-
40	14	PAPER INSTRUCTION-	38	46	INTERFACE CONNECTED
14	38	DATA STROBE+	35	45	INTERFACE CONNECTED RETURN

NOTE: If no signal is referenced, that pin is not used.

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Centronics Printer Cabling

Table B-38. Cable Pinouts For P9 Connector To Centronics Printer

4220 P9	Centronics	Function	4220 P9	Centronics	Function
6	2	DATA 1	11	19	RETURN
7	20	RETURN	42	31	PRINTER INITIALIZE
9	3	DATA 2	43	30	RETURN
10	21	RETURN	34	NU	NOT USED
1	4	DATA 3	15	32	FAULT
4	22	RETURN	16	NU	NOT USED
23	5	DATA 4	12	13	SELECT
20	23	RETURN	13	NU	NOT USED
2	6	DATA 5	18	10	ACKNOWLEDGE
3	24	RETURN	19	28	RETURN
29	7	DATA 6	30	12	PAPER EMPTY
26	25	RETURN	31	NU	NOT USED
8	8	DATA 7	24	NU	NOT USED
5	26	RETURN	25	NU	NOT USED
33	9	DATA 8	27	11	BUSY
32	27	RETURN	28	29	RETURN
36	NU	NOT USED	17	NU	NOT USED
37	NU	NOT USED	21	NU	NOT USED
39	NU	NOT USED	22	NU	NOT USED
40	NU	NOT USED	38	NU	NOT USED
14	1	DATA STROBE	35	NU	NOT USED

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Appendix C
Error Codes

The Return Status word in the command response contains information pertaining to the status of the IOPB returned in the Command Response Block. Error codes have been separated into logical groups and are reported in hexadecimal format.

MACSI/Controller Error Codes

HEX CODE	**DESCRIPTION**
0x00	GOOD STATUS: The controller has completed the command and no errors were detected. The Pass-Back status field contains the SCSI Pass-Through status.
0x01	QUEUE FULL: The work queue specified for this command is full and cannot receive another entry. The command is not executed and is moved directly to the Command Response Block with this status set. The queue can receive another entry after a currently active command has completed or if the queue is flushed.
0x02	WORK QUEUE INITIALIZATION ERROR: The work queue specified has not been initialized. The command is not executed and is moved directly to the Command Response Block with this status set. The Work Queue should be initialized with an Initialize Work Queue Command.
0x05	QUEUE NUMBER ERROR: The work queue number specified in the Command Queue entry is invalid. Valid work queue numbers are 0 to 14 for Cougar II and 0 to 255 for Cougar II Wide.
0x06	QUEUE ALREADY INITIALIZED: The work queue specified to be initialized has already been initialized. To re-initialize a queue, set the Initialized Work Queue bit in the options field of the Initialize Work Queue Command.
0x07	QUEUE UNINITIALIZED: An IOPB was issued to a work queue that has not been initialized. Work queues must be initialized with operating parameters before usage. The Work Queue should be initialized with an Initialize Work Queue Command.
0x08	QUEUE MODE NOT READY: The Start Queue Mode bit was set before the Initialize Controller Command was issued. The Initialize Controller Command should be the first board operation after power up to configure the MACSI interface.

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0x09 COMMAND UNAVAILABLE:

The command specified has not been implemented in the current firmware.

General Error Code Information

0x10 RESERVED FIELD ERROR:

A reserved field in the IOPB has non-zero data in it.

0x11 RESET BUS STATUS:

The SCSI Reset IOPB has executed successfully and generated a Reset on the bus.

0x12 SECONDARY PORT UNAVAILABLE:

An IOPB has been issued to the secondary port (Port 1), but the daughter card is not installed.

0x13 SCSI ID ERROR:

The SCSI device ID requested is the board's own device ID. All devices on the bus require unique SCSI Device IDs.

0x14 SCSI BUS RESET STATUS:

The command could not execute because the SCSI bus is held in the reset state. This may be caused by an unpowered device on the bus, improper termination, or an inverted cable.

0x15 COMMAND ABORTED BY RESET:

The command has been aborted due to a SCSI reset condition received during execution of the command.

0x16 PAGE SIZE ERROR:

The page size specified in the Page Size field of the Controller Initialization Block (words 0xD - 0xE) is invalid. For most applications, this field must be 0.

0x17 INVALID COMMAND TAG:

Command tags must be non-zero for successful searches.

0x18 BUSY COMMAND TAG:

Command is on the bus.

0x19 IOPB PARAMETER ERROR:

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The IOPB contains a value in one of its parameter fields which prevents the proper execution of the IOPB (e.g. invalid memory type, illegal address, etc.).

VMEbus Errors

0x20 VMEbus BUS ERROR:

This error indicates that a bus error occurred during the DMA transfer of the data to or from the buffer or the bus. This is typically caused by a nonexistent address or address modifier in the IOPB.

0x24 IOPB PARAMETER ERROR:

The IOPB contains a value in one of its parameter fields which prevents the execution of the IOPB (e.g. invalid memory type, illegal address, etc.).

0x26 VMEbus FETCH ERROR:

A VMEbus error occurred during an offboard IOPB fetch.

0x28 VMEbus POST ERROR:

A VMEbus error occurred on an offboard Command Response Block post.

0x2C VMEbus SCATTER/GATHER FETCH:

VMEbus error on scatter/gather list fetch.

0x2E INVALID SCATTER/GATHER COUNT:

An invalid number of scatter/gather elements has been specified. Valid element counts are 1 to 256.

SCSI Errors

0x30 SCSI SELECTION TIMEOUT ERROR:

The selection phase of the SCSI device has failed. The error may occur due to an incorrect SCSI Target ID.

0x31 SCSI DISCONNECT TIMEOUT ERROR:

A disconnected device has not re-selected the board in the timeout period. This may be caused by a hardware error, or a command that may take a very long period of time to execute.

0x32 ABNORMAL SCSI SEQUENCE:

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The SCSI operation did not complete successfully due to a hardware error or an abnormal operation sequence.

0x33 SCSI DISCONNECT ERROR:

An invalid SCSI bus sequence has been detected. This usually indicates a device has disconnected without either issuing the disconnect or command complete message.

0x34 SCSI TRANSFER COUNT EXCEPTION:

The SCSI data transfer Count did not match the count specified in the Maximum Count Length field of the IOPB. The amount of data actually transferred on the SCSI bus will be returned in the Maximum Transfer Length field. This status may not be considered an error for commands that intentionally allocate more buffer than the SCSI command uses.

0x35 SCSI PARITY ERROR:

A parity error occurred during the Information Transfer phase on the SCSI bus.

0x36 GROSS SCSI ERROR

The SCSI controller has detected an anomalous condition. A SCSI bus reset is required.

0x37 SCRIPT ILLEGAL INSTRUCTION

The SCSI controller has detected an illegal instruction. REQ may have been asserted when a disconnect was expected. A SCSI bus reset is required.

0x38 INVALID CDB LENGTH

Calculated CDB Length for user-defined command (group 6 or 7) is less than 1 or greater than 24.

0x39 INVALID WIDE SCSI ID

Valid SCSI IDs for this board are 0-7 only.

Scatter/Gather Errors

0x40 0 COUNT SCATTER/GATHER DETECTED

Scatter/Gather elements with 0 count detected.

0x41 ILLEGAL SCATTER/GATHER MEMORY TYPE

Illegal memory type in scatter/gather list.

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0x43 SCATTER/GATHER ELEMENT COUNTS < TOTAL TRANSFER COUNT

Error Handling Codes

0x50 READ/WRITE BUFFER COUNT ERROR:

Buffer count is too large.

0x51 ILLEGAL READ/WRITE:

Can't execute because of offboard Command Response Block.

0x80 FLUSH ON ERROR IN PROGRESS:

This status is set when the IOPB is flushed because an error condition has occurred and the work queue has the abort enable option set. This causes all queued IOPBs to be flushed until the abort acknowledge has been received.

0x81 FLUSH WORK QUEUE STATUS:

The queued IOPB is being flushed in response to a Flush Work Queue Command.

0x82 MISSING COMMAND:

A device has reselected the board for which there is no currently pending command.

0x83 COUNTER EXHAUSTED:

The transfer counter has exhausted but more data is being requested by the target device. A SCSI bus reset is required.

0x84 DATA DIRECTION ERROR:

A data phase is being requested opposite the direction set in the IOPB. A SCSI bus reset is required.

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Firmware Download Errors

0x90 INCORRECT HARDWARE:

Returned if the board either has insufficient memory, or is not populated with FLASH EPROM.

0x91 INVALID RECORD FORMAT:

Returned if the Command Options word fails to specify a supported record type encoding. Currently, the only format supported is Motorola S-records.

0x92 ILLEGAL IOPB VALUE:

Returned if any one of the IOPB fields contains an obviously incorrect value.

0x94 INVALID DOWNLOADED OPERATION:

A Transfer Packet sub-command has been received after a download process has been correctly executed.

0x95 BAD SEQUENCE NUMBER:

The board has received a packet from the host out of sequence.

0x96 BAD CRC:

The calculated checksum for the packet fails to match the value specified in the IOPB.

0x97 TRANSLATION ERROR:

The board encountered an error translated the downloaded data into an actual memory image.

0x99 BAD PACKET COUNT:

The number of packets received via Transfer Packet sub-commands does not match the count specified in the Transfer Count field of the IOPB.

0x9A BAD TRANSFER COUNT:

The total number of bytes received via Transfer Packet commands does not match the total byte count specified in the Transfer Count field of the Initialize Flash sub-command.

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0x9B BAD EPROM CHECKSUM:

After translating the downloaded data into a memory image, the internal checksum of the EPROM image failed.

0x9C ILLEGAL IMAGE:

Returned if the submitted image fails to match the requested action. The Program Flash request requires a different image than a Program Memory request.

0x9D BAD EPROM LOAD:

The board failed to program the FLASH EPROM. The error is not recoverable, and the EPROM must be replaced.

Other Errors

0xC0 BAD IOPB TYPE:

The IOPB type field does not match a currently supported IOPB type.

0xC1 IOPB TIMEOUT ERROR

The IOPB has timed out due to some type of serious error.

Non-Recoverable SCSI Errors

ERROR DURING MESSAGE IN PHASE

0X800 ILLEGAL FATAL SCSI ERROR CODE

This error should not occur.

0x801 BAD SYNCHRONOUS MESSAGE:

The message received in response to a synchronous negotiation did not contain a synchronous negotiation message.

0x802 BAD WIDE MESSAGE:

The message received in response to a wide negotiation did not contain a wide negotiation message.

0x803 UNKNOWN MESSAGE REJECT:

The board received a message reject for a message that is mandatory for the target to implement.

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0x804 MESSAGE REJECT IN COMMAND PHASE:
The board received a message reject in response to a command byte.

0x805 MESSAGE REJECT NOT IN MESSAGE OUT PHASE:

The board received a message reject in response to something other than a message out.

0x806 UNIMPLEMENTED MESSAGE:

The board received a message that has not been implemented.

TARGET SEQUENCE ERRORS

0x820 RESELECTION, NO IDENTIFY:

The target did not send an identify message after reselecting the board.

0x821 RESERVED PHASE DETECTED:

The target switched into a reserved phase.

SCSI Bus Interruptions

0x840 INVALID MESSAGE OUT PHASE:

The target switched to message out phase without the board asserting ATN.

0x841 EXTRA SCSI STATUS AFTER SELECTION:

After the board selected a device, but before the identify message out, the board detected anomalies on the SCSI bus.

0x842 GLITCH IN NON-DATA PHASE:

The SCSI phase lines glitched while REQ was asserted in a phase other than data in or data out.

0x843 INVALID TIMEOUT:

The SCSI selection timer expired on the board for some reason other than selection time-out.

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Appendix D
Acronyms Used In This Manual

AA	Abort Acknowledge
AE	Abort Enable
BOK	Board OK
CC	Command Complete
CDB	Command Descriptor Block
CIB	Controller Initialization Block
CNA	Controller Not Available
CQ	Command Queue
CQE	Command Queue Entry
CRB	Command Response Block
CRBV	Command Response Block Valid
CRSW	Command Response Status Word
CSB	Configuration Status Block
CSS	Controller Specific Space
DIR	VMEbus Transfer Direction
ER	Error
EX	Exception
GO	Go/Busy
HUS	Host Usable Space
IE	Interrupt Enable
IOPB	Input/Output Parameter Block
IQAR	Interrupt on Queue Available Register
IQEA	Interrupt on Queue Entry Available
IQHE	Interrupt on Queue Half Empty Enable
LSW	Least Significant Word
LUN	Logical Unit Number
MACSI	Multiple Active Command Software Interface
MCE	Master Command Entry
MCR	Master Control Register
MCSB	Master Control/Status Block
MSR	Master Status Register
MSW	Most Significant Word
MT	Memory Type
QECR	Queue Entry Control Register
QFC	Queue Flush Complete
QHP	Queue Head Pointer
QMS	Queue Mode Started
RES	Reset Controller
RSRV	Reserved
SCSI	Small Computer System Interface
SCSI ID	SCSI Device ID
SFEN	SYSFAIL Enable
SG	Scatter/Gather
SQM	Start Queue Mode
TT	Transfer Type
TWQR	Thaw Work Queue Register

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Appendix E
Primary Base Address: J23/J24/J25/J26

This appendix contains tables which specify the jumper settings used to set the base address of the controller's primary short I/O space. The tables include:

- Base Address of Primary 2K Short I/O Space
- Base Address of Primary 1K Short I/O Space
- Base Address of Primary 512-Byte Short I/O Space
- Base Address of Primary 256-Byte Short I/O Space

NOTES: To disable the Primary Short I/O set pins 15-16 of Jumper J23 to ON (logical 0), and all other pins of J23 to OFF (logical 1).

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Table E-1. Base Address of Primary 2K Short I/O Space

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
0000	F	F	F	0	0	0	0	0	F	F	F
0800	F	F	F	F	0	0	0	0	F	F	F
1000	F	F	F	0	F	0	0	0	F	F	F
1800	F	F	F	F	F	0	0	0	F	F	F
2000	F	F	F	0	0	F	0	0	F	F	F
2800	F	F	F	F	0	F	0	0	F	F	F
3000	F	F	F	0	F	F	0	0	F	F	F
3800	F	F	F	F	F	F	0	0	F	F	F
4000	F	F	F	0	0	0	F	0	F	F	F
4800	F	F	F	F	0	0	F	0	F	F	F
5000	F	F	F	0	F	0	F	0	F	F	F
5800	F	F	F	F	F	0	F	0	F	F	F
6000	F	F	F	0	0	F	F	0	F	F	F
6800	F	F	F	F	0	F	F	0	F	F	F
7000	F	F	F	0	F	F	F	0	F	F	F
7800	F	F	F	F	F	F	F	0	F	F	F
8000	F	F	F	0	0	0	0	F	F	F	F
8800	F	F	F	F	0	0	0	F	F	F	F
9000	F	F	F	0	F	0	0	F	F	F	F
9800	F	F	F	F	F	0	0	F	F	F	F
A000	F	F	F	0	0	F	0	F	F	F	F
A800	F	F	F	F	0	F	0	F	F	F	F
B000	F	F	F	0	F	F	0	F	F	F	F
B800	F	F	F	F	F	F	0	F	F	F	F
C000	F	F	F	0	0	0	F	F	F	F	F
C800	F	F	F	F	0	0	F	F	F	F	F
D000	F	F	F	0	F	0	F	F	F	F	F
D800	F	F	F	F	F	0	F	F	F	F	F
E000	F	F	F	0	0	F	F	F	F	F	F
E800	F	F	F	F	0	F	F	F	F	F	F
F000	F	F	F	0	F	F	F	F	F	F	F
F800	F	F	F	F	F	F	F	F	F	F	F

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-2. Base Address of Primary 1K Short I/O Space

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
0000	F	F	0	0	0	0	0	0	F	F	0
0400	F	F	F	0	0	0	0	0	F	F	0
0800	F	F	0	F	0	0	0	0	F	F	0
0C00	F	F	F	F	0	0	0	0	F	F	0
1000	F	F	0	0	F	0	0	0	F	F	0
1400	F	F	F	0	F	0	0	0	F	F	0
1800	F	F	0	F	F	0	0	0	F	F	0
1C00	F	F	F	F	F	0	0	0	F	F	0
2000	F	F	0	0	0	F	0	0	F	F	0
2400	F	F	F	0	0	F	0	0	F	F	0
2800	F	F	0	F	0	F	0	0	F	F	0
2C00	F	F	F	F	0	F	0	0	F	F	0
3000	F	F	0	0	F	F	0	0	F	F	0
3400	F	F	F	0	F	F	0	0	F	F	0
3800	F	F	0	F	F	F	0	0	F	F	0
3C00	F	F	F	F	F	F	0	0	F	F	0
4000	F	F	0	0	0	0	F	0	F	F	0
4400	F	F	F	0	0	0	F	0	F	F	0
4800	F	F	0	F	0	0	F	0	F	F	0
4C00	F	F	F	F	0	0	F	0	F	F	0
5000	F	F	0	0	F	0	F	0	F	F	0
5400	F	F	F	0	F	0	F	0	F	F	0
5800	F	F	0	F	F	0	F	0	F	F	0
5C00	F	F	F	F	F	0	F	0	F	F	0
6000	F	F	0	0	0	F	F	0	F	F	0
6400	F	F	F	0	0	F	F	0	F	F	0
6800	F	F	0	F	0	F	F	0	F	F	0
6C00	F	F	F	F	0	F	F	0	F	F	0
7000	F	F	0	0	F	F	F	0	F	F	0
7400	F	F	F	0	F	F	F	0	F	F	0
7800	F	F	0	F	F	F	F	0	F	F	0
7C00	F	F	F	F	F	F	F	0	F	F	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 1K Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
8000	F	F	0	0	0	0	0	F	F	F	0
8400	F	F	F	0	0	0	0	F	F	F	0
8800	F	F	0	F	0	0	0	F	F	F	0
8C00	F	F	F	F	0	0	0	F	F	F	0
9000	F	F	0	0	F	0	0	F	F	F	0
9400	F	F	F	0	F	0	0	F	F	F	0
9800	F	F	0	F	F	0	0	F	F	F	0
9C00	F	F	F	F	F	0	0	F	F	F	0
A000	F	F	0	0	0	F	0	F	F	F	0
A400	F	F	F	0	0	F	0	F	F	F	0
A800	F	F	0	F	0	F	0	F	F	F	0
AC00	F	F	F	F	0	F	0	F	F	F	0
B000	F	F	0	0	F	F	0	F	F	F	0
B400	F	F	F	0	F	F	0	F	F	F	0
B800	F	F	0	F	F	F	0	F	F	F	0
BC00	F	F	F	F	F	F	0	F	F	F	0
C000	F	F	0	0	0	0	F	F	F	F	0
C400	F	F	F	0	0	0	F	F	F	F	0
C800	F	F	0	F	0	0	F	F	F	F	0
CC00	F	F	F	F	0	0	F	F	F	F	0
D000	F	F	0	0	F	0	F	F	F	F	0
D400	F	F	F	0	F	0	F	F	F	F	0
D800	F	F	0	F	F	0	F	F	F	F	0
DC00	F	F	F	F	F	0	F	F	F	F	0
E000	F	F	0	0	0	F	F	F	F	F	0
E400	F	F	F	0	0	F	F	F	F	F	0
E800	F	F	0	F	0	F	F	F	F	F	0
EC00	F	F	F	F	0	F	F	F	F	F	0
F000	F	F	0	0	F	F	F	F	F	F	0
F400	F	F	F	0	F	F	F	F	F	F	0
F800	F	F	0	F	F	F	F	F	F	F	0
FC00	F	F	F	F	F	F	F	F	F	F	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-3. Base Address of Primary 512-Byte Short I/O Space

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
0000	F	0	0	0	0	0	0	0	F	0	0
0200	F	F	0	0	0	0	0	0	F	0	0
0400	F	0	F	0	0	0	0	0	F	0	0
0600	F	F	F	0	0	0	0	0	F	0	0
0800	F	0	0	F	0	0	0	0	F	0	0
0A00	F	F	0	F	0	0	0	0	F	0	0
0C00	F	0	F	F	0	0	0	0	F	0	0
0E00	F	F	F	F	0	0	0	0	F	0	0
1000	F	0	0	0	F	0	0	0	F	0	0
1200	F	F	0	0	F	0	0	0	F	0	0
1400	F	0	F	0	F	0	0	0	F	0	0
1600	F	F	F	0	F	0	0	0	F	0	0
1800	F	0	0	F	F	0	0	0	F	0	0
1A00	F	F	0	F	F	0	0	0	F	0	0
1C00	F	0	F	F	F	0	0	0	F	0	0
1E00	F	F	F	F	F	0	0	0	F	0	0
2000	F	0	0	0	0	F	0	0	F	0	0
2200	F	F	0	0	0	F	0	0	F	0	0
2400	F	0	F	0	0	F	0	0	F	0	0
2600	F	F	F	0	0	F	0	0	F	0	0
2800	F	0	0	F	0	F	0	0	F	0	0
2A00	F	F	0	F	0	F	0	0	F	0	0
2C00	F	0	F	F	0	F	0	0	F	0	0
2E00	F	F	F	F	0	F	0	0	F	0	0
3000	F	0	0	0	F	F	0	0	F	0	0
3200	F	F	0	0	F	F	0	0	F	0	0
3400	F	0	F	0	F	F	0	0	F	0	0
3600	F	F	F	0	F	F	0	0	F	0	0
3800	F	0	0	F	F	F	0	0	F	0	0
3A00	F	F	0	F	F	F	0	0	F	0	0
3C00	F	0	F	F	F	F	0	0	F	0	0
3E00	F	F	F	F	F	F	0	0	F	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 512 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
4000	F	0	0	0	0	0	F	0	F	0	0
4200	F	F	0	0	0	0	F	0	F	0	0
4400	F	0	F	0	0	0	F	0	F	0	0
4600	F	F	F	0	0	0	F	0	F	0	0
4800	F	0	0	F	0	0	F	0	F	0	0
4A00	F	F	0	F	0	0	F	0	F	0	0
4C00	F	0	F	F	0	0	F	0	F	0	0
4E00	F	F	F	F	0	0	F	0	F	0	0
5000	F	0	0	0	F	0	F	0	F	0	0
5200	F	F	0	0	F	0	F	0	F	0	0
5400	F	0	F	0	F	0	F	0	F	0	0
5600	F	F	F	0	F	0	F	0	F	0	0
5800	F	0	0	F	F	0	F	0	F	0	0
5A00	F	F	0	F	F	0	F	0	F	0	0
5C00	F	0	F	F	F	0	F	0	F	0	0
5E00	F	F	F	F	F	0	F	0	F	0	0
6000	F	0	0	0	0	F	F	0	F	0	0
6200	F	F	0	0	0	F	F	0	F	0	0
6400	F	0	F	0	0	F	F	0	F	0	0
6600	F	F	F	0	0	F	F	0	F	0	0
6800	F	0	0	F	0	F	F	0	F	0	0
6A00	F	F	0	F	0	F	F	0	F	0	0
6C00	F	0	F	F	0	F	F	0	F	0	0
6E00	F	F	F	F	0	F	F	0	F	0	0
7000	F	0	0	0	F	F	F	0	F	0	0
7200	F	F	0	0	F	F	F	0	F	0	0
7400	F	0	F	0	F	F	F	0	F	0	0
7600	F	F	F	0	F	F	F	0	F	0	0
7800	F	0	0	F	F	F	F	0	F	0	0
7A00	F	F	0	F	F	F	F	0	F	0	0
7C00	F	0	F	F	F	F	F	0	F	0	0
7E00	F	F	F	F	F	F	F	0	F	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 512 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
8000	F	0	0	0	0	0	0	F	F	0	0
8200	F	F	0	0	0	0	0	F	F	0	0
8400	F	0	F	0	0	0	0	F	F	0	0
8600	F	F	F	0	0	0	0	F	F	0	0
8800	F	0	0	F	0	0	0	F	F	0	0
8A00	F	F	0	F	0	0	0	F	F	0	0
8C00	F	0	F	F	0	0	0	F	F	0	0
8E00	F	F	F	F	0	0	0	F	F	0	0
9000	F	0	0	0	F	0	0	F	F	0	0
9200	F	F	0	0	F	0	0	F	F	0	0
9400	F	0	F	0	F	0	0	F	F	0	0
9600	F	F	F	0	F	0	0	F	F	0	0
9800	F	0	0	F	F	0	0	F	F	0	0
9A00	F	F	0	F	F	0	0	F	F	0	0
9C00	F	0	F	F	F	0	0	F	F	0	0
9E00	F	F	F	F	F	0	0	F	F	0	0
A000	F	0	0	0	0	F	0	F	F	0	0
A200	F	F	0	0	0	F	0	F	F	0	0
A400	F	0	F	0	0	F	0	F	F	0	0
A600	F	F	F	0	0	F	0	F	F	0	0
A800	F	0	0	F	0	F	0	F	F	0	0
AA00	F	F	0	F	0	F	0	F	F	0	0
AC00	F	0	F	F	0	F	0	F	F	0	0
AE00	F	F	F	F	0	F	0	F	F	0	0
B000	F	0	0	0	F	F	0	F	F	0	0
B200	F	F	0	0	F	F	0	F	F	0	0
B400	F	0	F	0	F	F	0	F	F	0	0
B600	F	F	F	0	F	F	0	F	F	0	0
B800	F	0	0	F	F	F	0	F	F	0	0
BA00	F	F	0	F	F	F	0	F	F	0	0
BC00	F	0	F	F	F	F	0	F	F	0	0
BE00	F	F	F	F	F	F	0	F	F	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 512 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J26	J25
C000	F	0	0	0	0	0	F	F	F	0	0
C200	F	F	0	0	0	0	F	F	F	0	0
C400	F	0	F	0	0	0	F	F	F	0	0
C600	F	F	F	0	0	0	F	F	F	0	0
C800	F	0	0	F	0	0	F	F	F	0	0
CA00	F	F	0	F	0	0	F	F	F	0	0
CC00	F	0	F	F	0	0	F	F	F	0	0
CE00	F	F	F	F	0	0	F	F	F	0	0
D000	F	0	0	0	F	0	F	F	F	0	0
D200	F	F	0	0	F	0	F	F	F	0	0
D400	F	0	F	0	F	0	F	F	F	0	0
D600	F	F	F	0	F	0	F	F	F	0	0
D800	F	0	0	F	F	0	F	F	F	0	0
DA00	F	F	0	F	F	0	F	F	F	0	0
DC00	F	0	F	F	F	0	F	F	F	0	0
DE00	F	F	F	F	F	0	F	F	F	0	0
E000	F	0	0	0	0	F	F	F	F	0	0
E200	F	F	0	0	0	F	F	F	F	0	0
E400	F	0	F	0	0	F	F	F	F	0	0
E600	F	F	F	0	0	F	F	F	F	0	0
E800	F	0	0	F	0	F	F	F	F	0	0
EA00	F	F	0	F	0	F	F	F	F	0	0
EC00	F	0	F	F	0	F	F	F	F	0	0
EE00	F	F	F	F	0	F	F	F	F	0	0
F000	F	0	0	0	F	F	F	F	F	0	0
F200	F	F	0	0	F	F	F	F	F	0	0
F400	F	0	F	0	F	F	F	F	F	0	0
F600	F	F	F	0	F	F	F	F	F	0	0
F800	F	0	0	F	F	F	F	F	F	0	0
FA00	F	F	0	F	F	F	F	F	F	0	0
FC00	F	0	F	F	F	F	F	F	F	0	0
FE00	F	F	F	F	F	F	F	F	F	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-4. Base Address of Primary 256-Byte Short I/O Space

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
0000	0	0	0	0	0	0	0	0	0	0	0
0100	F	0	0	0	0	0	0	0	0	0	0
0200	0	F	0	0	0	0	0	0	0	0	0
0300	F	F	0	0	0	0	0	0	0	0	0
0400	0	0	F	0	0	0	0	0	0	0	0
0500	F	0	F	0	0	0	0	0	0	0	0
0600	0	F	F	0	0	0	0	0	0	0	0
0700	F	F	F	0	0	0	0	0	0	0	0
0800	0	0	0	F	0	0	0	0	0	0	0
0900	F	0	0	F	0	0	0	0	0	0	0
0A00	0	F	0	F	0	0	0	0	0	0	0
0B00	F	F	0	F	0	0	0	0	0	0	0
0C00	0	0	F	F	0	0	0	0	0	0	0
0D00	F	0	F	F	0	0	0	0	0	0	0
0E00	0	F	F	F	0	0	0	0	0	0	0
0F00	F	F	F	F	0	0	0	0	0	0	0
1000	0	0	0	0	F	0	0	0	0	0	0
1100	F	0	0	0	F	0	0	0	0	0	0
1200	0	F	0	0	F	0	0	0	0	0	0
1300	F	F	0	0	F	0	0	0	0	0	0
1400	0	0	F	0	F	0	0	0	0	0	0
1500	F	0	F	0	F	0	0	0	0	0	0
1600	0	F	F	0	F	0	0	0	0	0	0
1700	F	F	F	0	F	0	0	0	0	0	0
1800	0	0	0	F	F	0	0	0	0	0	0
1900	F	0	0	F	F	0	0	0	0	0	0
1A00	0	F	0	F	F	0	0	0	0	0	0
1B00	F	F	0	F	F	0	0	0	0	0	0
1C00	0	0	F	F	F	0	0	0	0	0	0
1D00	F	0	F	F	F	0	0	0	0	0	0
1E00	0	F	F	F	F	0	0	0	0	0	0
1F00	F	F	F	F	F	0	0	0	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
2000	0	0	0	0	0	F	0	0	0	0	0
2100	F	0	0	0	0	F	0	0	0	0	0
2200	0	F	0	0	0	F	0	0	0	0	0
2300	F	F	0	0	0	F	0	0	0	0	0
2400	0	0	F	0	0	F	0	0	0	0	0
2500	F	0	F	0	0	F	0	0	0	0	0
2600	0	F	F	0	0	F	0	0	0	0	0
2700	F	F	F	0	0	F	0	0	0	0	0
2800	0	0	0	F	0	F	0	0	0	0	0
2900	F	0	0	F	0	F	0	0	0	0	0
2A00	0	F	0	F	0	F	0	0	0	0	0
2B00	F	F	0	F	0	F	0	0	0	0	0
2C00	0	0	F	F	0	F	0	0	0	0	0
2D00	F	0	F	F	0	F	0	0	0	0	0
2E00	0	F	F	F	0	F	0	0	0	0	0
2F00	F	F	F	F	0	F	0	0	0	0	0
3000	0	0	0	0	F	F	0	0	0	0	0
3100	F	0	0	0	F	F	0	0	0	0	0
3200	0	F	0	0	F	F	0	0	0	0	0
3300	F	F	0	0	F	F	0	0	0	0	0
3400	0	0	F	0	F	F	0	0	0	0	0
3500	F	0	F	0	F	F	0	0	0	0	0
3600	0	F	F	0	F	F	0	0	0	0	0
3700	F	F	F	0	F	F	0	0	0	0	0
3800	0	0	0	F	F	F	0	0	0	0	0
3900	F	0	0	F	F	F	0	0	0	0	0
3A00	0	F	0	F	F	F	0	0	0	0	0
3B00	F	F	0	F	F	F	0	0	0	0	0
3C00	0	0	F	F	F	F	0	0	0	0	0
3D00	F	0	F	F	F	F	0	0	0	0	0
3E00	0	F	F	F	F	F	0	0	0	0	0
3F00	F	F	F	F	F	F	0	0	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
4000	0	0	0	0	0	0	F	0	0	0	0
4100	F	0	0	0	0	0	F	0	0	0	0
4200	0	F	0	0	0	0	F	0	0	0	0
4300	F	F	0	0	0	0	F	0	0	0	0
4400	0	0	F	0	0	0	F	0	0	0	0
4500	F	0	F	0	0	0	F	0	0	0	0
4600	0	F	F	0	0	0	F	0	0	0	0
4700	F	F	F	0	0	0	F	0	0	0	0
4800	0	0	0	F	0	0	F	0	0	0	0
4900	F	0	0	F	0	0	F	0	0	0	0
4A00	0	F	0	F	0	0	F	0	0	0	0
4B00	F	F	0	F	0	0	F	0	0	0	0
4C00	0	0	F	F	0	0	F	0	0	0	0
4D00	F	0	F	F	0	0	F	0	0	0	0
4E00	0	F	F	F	0	0	F	0	0	0	0
4F00	F	F	F	F	0	0	F	0	0	0	0
5000	0	0	0	0	F	0	F	0	0	0	0
5100	F	0	0	0	F	0	F	0	0	0	0
5200	0	F	0	0	F	0	F	0	0	0	0
5300	F	F	0	0	F	0	F	0	0	0	0
5400	0	0	F	0	F	0	F	0	0	0	0
5500	F	0	F	0	F	0	F	0	0	0	0
5600	0	F	F	0	F	0	F	0	0	0	0
5700	F	F	F	0	F	0	F	0	0	0	0
5800	0	0	0	F	F	0	F	0	0	0	0
5900	F	0	0	F	F	0	F	0	0	0	0
5A00	0	F	0	F	F	0	F	0	0	0	0
5B00	F	F	0	F	F	0	F	0	0	0	0
5C00	0	0	F	F	F	0	F	0	0	0	0
5D00	F	0	F	F	F	0	F	0	0	0	0
5E00	0	F	F	F	F	0	F	0	0	0	0
5F00	F	F	F	F	F	0	F	0	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
6000	0	0	0	0	0	F	F	0	0	0	0
6100	F	0	0	0	0	F	F	0	0	0	0
6200	0	F	0	0	0	F	F	0	0	0	0
6300	F	F	0	0	0	F	F	0	0	0	0
6400	0	0	F	0	0	F	F	0	0	0	0
6500	F	0	F	0	0	F	F	0	0	0	0
6600	0	F	F	0	0	F	F	0	0	0	0
6700	F	F	F	0	0	F	F	0	0	0	0
6800	0	0	0	F	0	F	F	0	0	0	0
6900	F	0	0	F	0	F	F	0	0	0	0
6A00	0	F	0	F	0	F	F	0	0	0	0
6B00	F	F	0	F	0	F	F	0	0	0	0
6C00	0	0	F	F	0	F	F	0	0	0	0
6D00	F	0	F	F	0	F	F	0	0	0	0
6E00	0	F	F	F	0	F	F	0	0	0	0
6F00	F	F	F	F	0	F	F	0	0	0	0
7000	0	0	0	0	F	F	F	0	0	0	0
7100	F	0	0	0	F	F	F	0	0	0	0
7200	0	F	0	0	F	F	F	0	0	0	0
7300	F	F	0	0	F	F	F	0	0	0	0
7400	0	0	F	0	F	F	F	0	0	0	0
7500	F	0	F	0	F	F	F	0	0	0	0
7600	0	F	F	0	F	F	F	0	0	0	0
7700	F	F	F	0	F	F	F	0	0	0	0
7800	0	0	0	F	F	F	F	0	0	0	0
7900	F	0	0	F	F	F	F	0	0	0	0
7A00	0	F	0	F	F	F	F	0	0	0	0
7B00	F	F	0	F	F	F	F	0	0	0	0
7C00	0	0	F	F	F	F	F	0	0	0	0
7D00	F	0	F	F	F	F	F	0	0	0	0
7E00	0	F	F	F	F	F	F	0	0	0	0
7F00	F	F	F	F	F	F	F	0	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
8000	0	0	0	0	0	0	0	F	0	0	0
8100	F	0	0	0	0	0	0	F	0	0	0
8200	0	F	0	0	0	0	0	F	0	0	0
8300	F	F	0	0	0	0	0	F	0	0	0
8400	0	0	F	0	0	0	0	F	0	0	0
8500	F	0	F	0	0	0	0	F	0	0	0
8600	0	F	F	0	0	0	0	F	0	0	0
8700	F	F	F	0	0	0	0	F	0	0	0
8800	0	0	0	F	0	0	0	F	0	0	0
8900	F	0	0	F	0	0	0	F	0	0	0
8A00	0	F	0	F	0	0	0	F	0	0	0
8B00	F	F	0	F	0	0	0	F	0	0	0
8C00	0	0	F	F	0	0	0	F	0	0	0
8D00	F	0	F	F	0	0	0	F	0	0	0
8E00	0	F	F	F	0	0	0	F	0	0	0
8F00	F	F	F	F	0	0	0	F	0	0	0
9000	0	0	0	0	F	0	0	F	0	0	0
9100	F	0	0	0	F	0	0	F	0	0	0
9200	0	F	0	0	F	0	0	F	0	0	0
9300	F	F	0	0	F	0	0	F	0	0	0
9400	0	0	F	0	F	0	0	F	0	0	0
9500	F	0	F	0	F	0	0	F	0	0	0
9600	0	F	F	0	F	0	0	F	0	0	0
9700	F	F	F	0	F	0	0	F	0	0	0
9800	0	0	0	F	F	0	0	F	0	0	0
9900	F	0	0	F	F	0	0	F	0	0	0
9A00	0	F	0	F	F	0	0	F	0	0	0
9B00	F	F	0	F	F	0	0	F	0	0	0
9C00	0	0	F	F	F	0	0	F	0	0	0
9D00	F	0	F	F	F	0	0	F	0	0	0
9E00	0	F	F	F	F	0	0	F	0	0	0
9F00	F	F	F	F	F	0	0	F	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
A000	0	0	0	0	0	F	0	F	0	0	0
A100	F	0	0	0	0	F	0	F	0	0	0
A200	0	F	0	0	0	F	0	F	0	0	0
A300	F	F	0	0	0	F	0	F	0	0	0
A400	0	0	F	0	0	F	0	F	0	0	0
A500	F	0	F	0	0	F	0	F	0	0	0
A600	0	F	F	0	0	F	0	F	0	0	0
A700	F	F	F	0	0	F	0	F	0	0	0
A800	0	0	0	F	0	F	0	F	0	0	0
A900	F	0	0	F	0	F	0	F	0	0	0
AA00	0	F	0	F	0	F	0	F	0	0	0
AB00	F	F	0	F	0	F	0	F	0	0	0
AC00	0	0	F	F	0	F	0	F	0	0	0
AD00	F	0	F	F	0	F	0	F	0	0	0
AE00	0	F	F	F	0	F	0	F	0	0	0
AF00	F	F	F	F	0	F	0	F	0	0	0
B000	0	0	0	0	F	F	0	F	0	0	0
B100	F	0	0	0	F	F	0	F	0	0	0
B200	0	F	0	0	F	F	0	F	0	0	0
B300	F	F	0	0	F	F	0	F	0	0	0
B400	0	0	F	0	F	F	0	F	0	0	0
B500	F	0	F	0	F	F	0	F	0	0	0
B600	0	F	F	0	F	F	0	F	0	0	0
B700	F	F	F	0	F	F	0	F	0	0	0
B800	0	0	0	F	F	F	0	F	0	0	0
B900	F	0	0	F	F	F	0	F	0	0	0
BA00	0	F	0	F	F	F	0	F	0	0	0
BB00	F	F	0	F	F	F	0	F	0	0	0
BC00	0	0	F	F	F	F	0	F	0	0	0
BD00	F	0	F	F	F	F	0	F	0	0	0
BE00	0	F	F	F	F	F	0	F	0	0	0
BF00	F	F	F	F	F	F	0	F	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
C000	0	0	0	0	0	0	F	F	0	0	0
C100	F	0	0	0	0	0	F	F	0	0	0
C200	0	F	0	0	0	0	F	F	0	0	0
C300	F	F	0	0	0	0	F	F	0	0	0
C400	0	0	F	0	0	0	F	F	0	0	0
C500	F	0	F	0	0	0	F	F	0	0	0
C600	0	F	F	0	0	0	F	F	0	0	0
C700	F	F	F	0	0	0	F	F	0	0	0
C800	0	0	0	F	0	0	F	F	0	0	0
C900	F	0	0	F	0	0	F	F	0	0	0
CA00	0	F	0	F	0	0	F	F	0	0	0
CB00	F	F	0	F	0	0	F	F	0	0	0
CC00	0	0	F	F	0	0	F	F	0	0	0
CD00	F	0	F	F	0	0	F	F	0	0	0
CE00	0	F	F	F	0	0	F	F	0	0	0
CF00	F	F	F	F	0	0	F	F	0	0	0
D000	0	0	0	0	F	0	F	F	0	0	0
D100	F	0	0	0	F	0	F	F	0	0	0
D200	0	F	0	0	F	0	F	F	0	0	0
D300	F	F	0	0	F	0	F	F	0	0	0
D400	0	0	F	0	F	0	F	F	0	0	0
D500	F	0	F	0	F	0	F	F	0	0	0
D600	0	F	F	0	F	0	F	F	0	0	0
D700	F	F	F	0	F	0	F	F	0	0	0
D800	0	0	0	F	F	0	F	F	0	0	0
D900	F	0	0	F	F	0	F	F	0	0	0
DA00	0	F	0	F	F	0	F	F	0	0	0
DB00	F	F	0	F	F	0	F	F	0	0	0
DC00	0	0	F	F	F	0	F	F	0	0	0
DD00	F	0	F	F	F	0	F	F	0	0	0
DE00	0	F	F	F	F	0	F	F	0	0	0
DF00	F	F	F	F	F	0	F	F	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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Table E-9. Base Address of Primary 256 Byte Short I/O Space (Continued)

ADDRESS	J23 PIN SETTINGS								J24,J25,J26 PIN SETTINGS		
	15-16	13-14	11-12	9-10	7-8	5-6	3-4	1-2	J24	J25	J26
E000	0	0	0	0	0	F	F	F	0	0	0
E100	F	0	0	0	0	F	F	F	0	0	0
E200	0	F	0	0	0	F	F	F	0	0	0
E300	F	F	0	0	0	F	F	F	0	0	0
E400	0	0	F	0	0	F	F	F	0	0	0
E500	F	0	F	0	0	F	F	F	0	0	0
E600	0	F	F	0	0	F	F	F	0	0	0
E700	F	F	F	0	0	F	F	F	0	0	0
E800	0	0	0	F	0	F	F	F	0	0	0
E900	F	0	0	F	0	F	F	F	0	0	0
EA00	0	F	0	F	0	F	F	F	0	0	0
EB00	F	F	0	F	0	F	F	F	0	0	0
EC00	0	0	F	F	0	F	F	F	0	0	0
ED00	F	0	F	F	0	F	F	F	0	0	0
EE00	0	F	F	F	0	F	F	F	0	0	0
EF00	F	F	F	F	0	F	F	F	0	0	0
F000	0	0	0	0	F	F	F	F	0	0	0
F100	F	0	0	0	F	F	F	F	0	0	0
F200	0	F	0	0	F	F	F	F	0	0	0
F300	F	F	0	0	F	F	F	F	0	0	0
F400	0	0	F	0	F	F	F	F	0	0	0
F500	F	0	F	0	F	F	F	F	0	0	0
F600	0	F	F	0	F	F	F	F	0	0	0
F700	F	F	F	0	F	F	F	F	0	0	0
F800	0	0	0	F	F	F	F	F	0	0	0
F900	F	0	0	F	F	F	F	F	0	0	0
FA00	0	F	0	F	F	F	F	F	0	0	0
FB00	F	F	0	F	F	F	F	F	0	0	0
FC00	0	0	F	F	F	F	F	F	0	0	0
FD00	F	0	F	F	F	F	F	F	0	0	0
FE00	0	F	F	F	F	F	F	F	0	0	0
FF00	F	F	F	F	F	F	F	F	0	0	0

NOTE: 0= ON (Logical 0), F= OFF (Logical 1)

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