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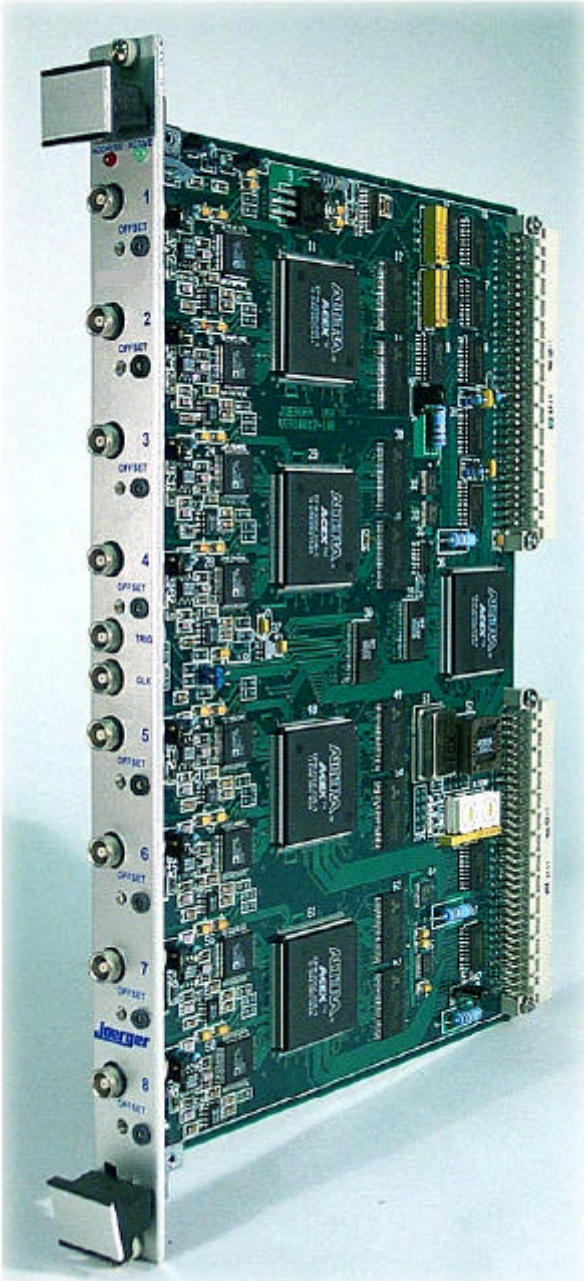
Find the *Joerger Enterprises VTR10012* at our website: *Click HERE*

Joerger ENTERPRISES, INC.

MODEL VTR10012

EIGHT CHANNEL, 100 MHZ, 12 BIT "VME" ANALOG DIGITIZER WITH OSCILLOSCOPE CHARACTERISTICS

FEATURES:



- 1, 2, 4 or 8 INDIVIDUAL CHANNELS
- 100 MHZ CLOCK SPEED
- 12 BIT RESOLUTION PLUS SIGNAL AVERAGING FOR IMPROVED SNR
- ***"OSCILLOSCOPE"*** TYPE INPUTS FEATURING:
  - HIGH INPUT IMPEDANCE, 10 MΩ's
  - FULL SCALE OFFSET CONTROL
  - SINGLE ENDED OR DIFFERENTIAL INPUTS
  - WIDE INPUT BANDWIDTH FOR GOOD WAVEFORM TRACKING
- 256K SAMPLES OF SRAM PER CHANNEL, 2MSAMPLES TOTAL
- CHANNELS CAN BE READ AT ANY TIME PROVIDING:
  - SIGNAL MONITORING
  - OFFSET ADJUST AND TEST
  - GAIN TESTING
- READ OUT OF MODULE TYPE AND IT'S SERIAL NUMBER
- RECORDING MODES:
  - POST TRIGGER
  - MULTIPLE POST TRIGGER
  - PRE/POST TRIGGER
  - MULTIPLE PRE/POST TRIGGER
- GLOBAL COMMANDS FOR MULTIPLE MODULE OPERATION
- ALL TRIGGER ADDRESSES STORED
- REAL TIME TRIGGER ARRIVAL STORED
- TRIGGER COUNTER PROVIDED
- NUMBER OF EVENTS REGISTER
- INDIVIDUAL FILTERING OF EACH CHANNELS POWER AND GROUND
- HIGH NOISE IMMUNITY AND LOW CHANNEL CROSSTALK

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- ***"SPARSE"*** SCAN MODE FOR IMPROVED READOUT SPEED
- LOW POWER CONSUMPTION, 13 WATTS TOTAL AT 100MHZ, GREATLY IMPROVING CRATE COOLING AND MODULE RELIABILITY
- 64 BIT DATA READOUT AVAILABLE USING MBLT64, 4 DATA WORDS PER READ
- ACTIVE MODE CAN BE DELAYED FROM TRIGGER SIGNAL, PROGRAMMABLE
- INTERNAL CRYSTAL CLOCK OR EXTERNAL CLOCK
- INTERRUPT STRUCTURE
- BLOCK TRANSFER MODE
- ***"EPICS "*** AND ***"LABVIEW"*** SOFTWARE AVAILABLE

APPLICATIONS:

- HIGH SPEED, ACCURATE, ANALOG TO DIGITAL RECORDING
- ***OSCILLOSCOPES:*** USING ITS HIGH IMPEDANCE FRONT END, FULL SCALE OFFSET AND MEMORY PROVIDE FAST, ACCURATE RECORDING AND READOUT OF ANALOG DATA, ESPECIALLY USEFUL IN SINGLE SHOT EVENTS
- COMMUNICATIONS: USING THE REAL TIME ADC OUTPUT
- RADAR AND SATELLITE SYSTEMS

The ***JOERGER ENTERPRISES, INC.*** MODEL VTR10012 is available with 1, 2, 4 or 8 individual 100Mhz analog digitizers with a resolution of 12 bits plus signal averaging for improved SNR in a 6U, VME module. In addition to waveform recording the input has the same features as an oscilloscope, 10MΩ input impedance, full scale offset and single ended or differential inputs. This provides the ability to record a single shot event with high speed and resolution and read it out quickly. This simplifies system analysis and trouble shooting. High resolution and accuracy have been attained with the use of ADC's designed to run at 100Mhz with 12 bit resolution. To further improve performance the input signals can be averaged to improve signal to noise response. From 2 to 128 input samples can be selected for averaging and the results stored in memory. Each channel is completely self contained and can store up to 256k samples per channel in SRAM, 2M total in a single width module. The latest ADC's, amplifiers, memory and the use of high speed programmable logic devices make all these features possible. While many high speed modules require a great deal of power, the VTR10012 uses only 13 watts while running at 100Mhz. This is often an important consideration when many of these may be used in a single crate. The ADC uses a pipeline converter with the delay handled internally and is invisible to the user.

To insure high performance each channel contains a wide bandwidth amplifier section. To provide good ADC performance it is driven with a buffered amplifier with a differential input and a differential output which is internally offset to provide an input designed especially for these latest type converters. This isolates the ADC and provides a 10MΩ input impedance with either a single ended or a true differential input. The high input impedance affords the ability to monitor an input signal without loading it down. This type input coupled with its large memory provides the ability to monitor a wave shape over a long period of time. Even when trouble shooting a slow speed system it provides a high speed, high-resolution picture. A difficult feature to accomplish with an analog oscilloscope. When required a lower input impedance can be selected with an on board jumper.

To provide a versatile input range full scale offset is provided using a front panel potentiometer. This allows either bipolar or unipolar input ranges. A test point is included to monitor the offset. The offset can be readout on the VME bus. To make the module even more useful data may be read out while active or idle without disrupting the operation. This allows the data from the ADC to be monitored while active. It provides the ability to operate the module as an ADC or to check each channel's offset and gain.

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The input is digitized using an internal crystal oscillator or an external clock and loads the data into its internal SRAM. To insure high-speed readout, data can be read out 4 samples at a time from 2 channels using BLT64 onto 64 lines. To increase overall data readout speed a "SPARSE" scan mode is provided. Each channel has a 12 bit register that can be set with a minimum input level. Its output is compared to the converted input level and if it is not exceeded the data is considered invalid. This valid data word can be read out indicating which channels should be read. All channels use a common clock, address, control signals and operate simultaneously. Special care has been extended to insure accurate timing.

The analog inputs have been designed to handle a wide variety of signals. Each channels analog power and analog ground are individually filtered. This special care in the layout and filtering provide both low channel cross talk and low noise, often a problem with multi-channel analog input modules. When an application requires filtering, external filters are recommended.

Control and status registers are accessed via short addressing. The control registers select the operating parameters for the module. The gate duration register contains the number of samples to be taken after a trigger.

To facilitate data readout two additional memories are provided. One records the memory address at the end of each cycle. The second memory records the time each trigger was received and is taken from the 32 bit real time counter. A trigger counter is provided to record the number of complete triggers received. This information allows the user the ability to know how many triggers were received, their memory addresses and the time the triggers occurred. An event register is also provided that selects the number of triggers to accept and disarm the cycle.

The Model VTR10012 can operate in post trigger, multiple post trigger, pre/post and multiple pre/post trigger modes. The post trigger mode starts digitizing on receipt of a trigger, takes the number of samples set by the gate duration register then stops and sets an interrupt. If Auto Reset is on, the next trigger will reset the location counter to zero and overwrite the previous samples. For multiple post trigger operation, Auto Reset is turned off and each following trigger will not reset the location counter and the samples will be stored sequentially until the memory is full. To account for the timing in multiple trigger operations a 32 bit “real time” counter is provided. The time each trigger is received is stored in memory. This can be readout along with the number of triggers received. If the "Memory Wrap" is off and the cycle is complete, an interrupt is set and further triggers are ignored. If the Wrap mode is on, when the memory fills it will start overwriting data and accept triggers until the module is disarmed.

In the pre/post trigger mode the module starts taking data when the unit is armed and cycles through the memory overwriting old data. Upon receipt of a trigger the module takes the number of samples set by the gate duration register, stops and sets an interrupt. The complete memory is used with the post trigger samples preset by the gate duration. The balance of the memory contains pre-trigger information. For multiple pre/post trigger operation the memory is divided programmably into sections of up to 16. Now each section operates as a pre/post trigger cycle with its address and time stored. At the completion of operation an interrupt is set. This then provides the user a complete picture of the data recorded. The memory addresses, the time the triggers were received and the number of triggers are available. All recording cycles are triggered, either internally or externally. As an added feature this trigger can be delayed digitally by programmable setting of a counter and its clock speed. This could prove useful in operations where there is a time gap when the trigger appears and active recording should begin. In pre/post modes a register is provided to require to set a number of samples to be stored after arm before a trigger is recognized.

To control multiple module operation global commands are available that can be used for commands like arm/disarm, and to enable/disable triggers. This allows the user the ability to control a group of modules and have them work together. “LABVIEW” and “EPICS” software is available.

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SPECIFICATIONS (per channel)

ANALOG INPUT	±1 Volts, single ended, Differential input optional
INPUT OFFSET ADJUST	Full scale front panel input offset adjustment and test point
GAIN STABILITY	7ppm/ °C
INPUT IMPEDANCE	10 MΩ's, jumper selectable to 50Ω's, other impedance's optional
CHANNEL CROSSTALK	<1 LSB typical at 10Mhz input rate
BANDWIDTH	100Mhz Minimum
DIFFERENTIAL LINEARITY	±.3LSB, Typ., No missing codes
CONVERSION RATE	1Mhz to 100Mhz, programmable
RESOLUTION	12 Bits + over-range
SIGNAL AVERAGING	Select number of samples to be averaged, 2, 4, 8, 16, 32, 64, 128
MEMORY	256k samples/channel in SRAM, 2M samples total
TRIGGER/GATE INPUT	TTL Level, Operating mode internally selectable
CLOCK INPUT	TTL Level
VME INTERFACE	D16, D32, D32:BLT, MBLT64, A16, A24, A32
CONTROL/STATUS REG.	Read/Write: select clock rate, disarm at cycle completion, bus trigger, external clock, external trigger/gate, reset on trigger, wrap, post, multiple post, pre/post, and multiple pre/post trigger modes, arm, active, channel data addresses, real time trigger addresses, trigger delay, trigger counter, trigger selection register, global arm/enable
GATE DURATION REGISTER	Read/Write: select the number of conversions to perform after a trigger.
REAL TIME ADDRESS	Read real time trigger addresses
TRIGGER DELAY	Read/Write active trigger delay
PRE/POST SELECTION	Read/Write, select number of multiple pre/post cycles
EVENT REGISTER	Read/Write, number of trigger events for interrupt and/or disarm
MIN PRETRIGGER SAMPLE REGISTER	Read/Write, minimum number of samples needed before a trigger will be accepted in pre/post trigger modes
INTERRUPT ID REGISTER	Read/Write Status/ID word
IRQ LEVEL REGISTER	Read/Write IRQ levels
SYSRESET, INT. RESET	Resets module and control register, aborts recording cycle
SOFTWARE	“LABVIEW” and “EPICS” software is available
POWER REQUIREMENTS:	+5V, 2A; -12V, 250ma, 13 watts total at 100Mhz
SIZE:	Single width "VME" 6U card
CONNECTORS:	Lemo ERA 00.250 standard Lemo ERA 0S.302, for differential inputs
OPTIONS	1) Single channel 2) 2 channels 3) 4 channels 4) 8 channels 5) Differential Inputs 6) SMA connectors 7) SMB connectors 8) Signal averaging 64 bit data read out

JEI0203

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PLEASE NOTE: When choosing an analog input module many factors should be considered. It is recommended reading "SELECTING AN ANALOG INPUT MODULE" on our web site: www.joergerinc.com , under "What's New"

166 LAUREL ROAD • EAST NORTHPORT, NY 11731, USA
1-631-757-6200 • FAX 1-631-757-6201 • Email: joerger@joergerinc.com • web: www.joergerinc.com

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