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Data Sheet

JTAGTAPS™ High-Performance Boundary-Scan Controllers

Product Overview

The JTAG Technologies products perform printed circuit board testing and in-system programming in compliance with the IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture. This IEEE standard defines a standard 4- or 5-wire electrical interface and control protocol to communicate with the target board, providing improved access to complex, high-density PCBs.

The system includes JTAGTAPS™, a family of robust, highly reliable boundary-scan controllers, serving as the hardware interface between the test and/or programming system and the target assembly that is to be tested or programmed. Figure 1 depicts a typical boundary-scan application. The controller sends a sequence of serial data vectors to the target board and receives serial data back from the target. On the board, the data input causes electrical testing and device programming to be performed, while the results of the operations are reported via the output stream.

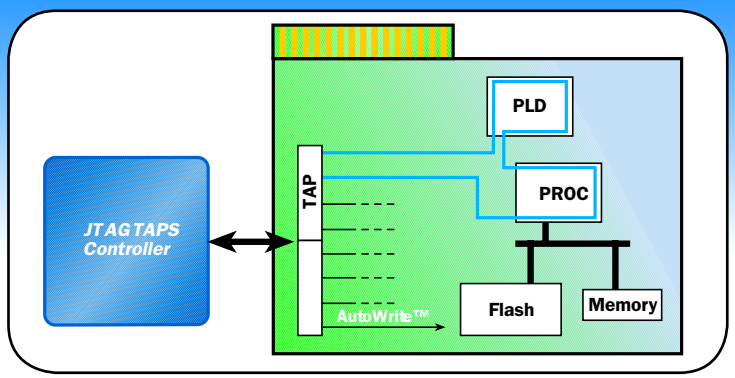


Figure 1. Example Configuration of Controller and Target PCB

The JTAGTAPS controllers support a broad range of operating environments in engineering, manufacturing, and service, as determined by the host computer and the application requirements. Regardless of the controller selected, all JTAGTAPS products are designed by and built exclusively for JTAG Technologies for assured system compatibility and life cycle support.

Available in three hardware architectures and performance levels:

- **DataBlaster** - highest performance, suitable for all applications including in-system programming of flash memories and PLDs, and for board test in manufacturing and debugging environments.
- **DataBlasterLite** - mid-performance, suitable for board testing and PLD programming, and for less demanding flash applications.
- **Explorer** - suitable for board testing and PLD programming applications in engineering and low-volume production environments.

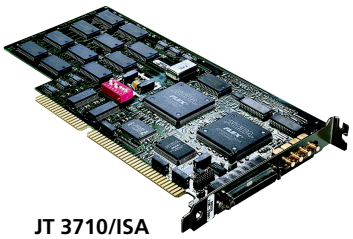
The architecture of the hardware and software products permits applications to be easily ported between development and production, regardless of the controller types. Compilation of an application targets a specific controller architecture, and driver selection determines which hardware form factor is to be used. This portability is valuable in multi-user and multi-department environments.

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High-Performance Boundary-Scan Controllers

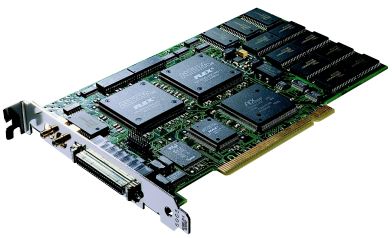
JT 3710 DataBlaster



JT 3710/ISA DataBlaster

The JT 3710 DataBlaster is available in ISA, PCI, VXI, and USB form factors, all of which offer the same set of high-performance features. The ISA and PCI versions are PC plug-ins to the ISA and PCI bus slots, respectively. The VXI version is implemented as a C-size card, based on the dedicated VXI instrumentation bus, and may be controlled by a PC or Workstation via MXI interfaces, or via embedded controllers. The USB version is a self-contained module that connects via a standard USB cable with the high-speed plug-and-play USB port of a PC or laptop.

Each of the versions of the JT 3710 includes a separate POD that provides four parallel TAP output channels, allowing a single JT 3710 controller to drive and sense up to four boundary-scan chains simultaneously. In flash programming applications, the JT 3710 POD allows gang programming of up to four flash memories. The same POD may be used for all of the JT 3710 controller types.



JT 3710/PCI DataBlaster

The POD provides active line terminations, maintaining the integrity of critical signals at the point of test. Four connectors on the POD allow easy interconnection via short cables to the target board(s). Three types of PODs are available: the PF 2137/10 for bench top use, and the PF 2137/12 and PF 2137/13 for industrial applications where rugged construction, integration within a test fixture, and easy interchangeability between fixtures are required.

The POD may be separate from the controller module in which case it is connected via a SCSI-2 type cable up to 4 meters in length. An alternate arrangement is offered with the USB in which the active terminations and connectors for cabling to the targets are integrated within the USB module itself. This version is applicable in cases where the USB is located close to the target(s) such as in desktop use.



JT 3710/VXI DataBlaster

The TAPs driven by the JT 3710 support test frequencies from 100 kHz up to 25 MHz, in 100 kHz increments. For maximum performance, dedicated hardware within the JT 3710 delivers test and programming files to the target in a continuous fashion, rather than in a burst mode. The DataBlaster performs data compression and de-compression on the fly and is capable of autonomous operation, allowing it to control the boundary-scan operation without intervention from the host computer. Control returns to the host upon completion of the operation (See Figure 2).

The JT 3710 supports JTAG Technologies' AutoWrite™ (patent pending) feature that reduces flash programming time by a factor of 2 to 3. This is accomplished by real-time hardware control of the flash write enable line instead of via the boundary-scan chain. DataBlaster also supports other flash-specific control signals, including Vpp Enable (to control optional programming voltages on the target), User0/User1 (user-definable, software-controlled eg. watchdog) and Ready (for optional use to verify completion of an operation).

JT 3707 DataBlasterLite



JT 3710/USB-4T DataBlaster

The JT 3707 DataBlasterLite is available in the PCI format. It connects to the target boundary-scan(s) via the same POD types as with the JT 3710, allowing the JT 3707 to support simultaneous control of up to four boundary-scan chains. The DataBlasterLite does not provide gang programming of flash memories.

The JT 3707 provides many of the same features as the JT 3710. The principal difference between the two hardware architectures is the absence of specific on-board image memory in the JT 3707 to support high-speed flash programming. For this reason, the JT 3707 is primarily targeted at test and PLD programming applications.

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PM 3705 Explorer

The PM 3705 Explorer connects to the PC via a standard parallel interface and operates at the inherent speed of the PC parallel port, typically 150 kHz. It provides two parallel TAP output channels allowing two boundary-scan chains to be driven and observed simultaneously.

The Explorer is available in a self-contained, connectorized desktop unit for cabling to the PC parallel port PC and the target boards. The Explorer is used primarily in testing and PLD programming.



PM 3705
Explorer Controller

JTAGTAPS™ Controller Features

Feature	Description	JT 3710 DataBlaster	JT 3707 DataBlasterLite	PM 3705 Explorer
Programmable Clock	Programmable in 100 kHz increments from 100 kHz to 25 MHz	Yes	Yes	No
On-board Image Memory	32 Mbit buffer stores data file to be programmed into flash memory, avoids need to repeat downloading the same file repeatedly for multiple boards.	Yes	No	No
Autonomous Operation	Self-contained local memory and execution control hardware. Controller manages the operation and signals host when complete.	Yes	Yes	No
AutoWrite™ Support	Hardware control of flash memory Write Enable signal allows programming to occur 2 to 3 times faster. AW is generated automatically on flash memory write operation, synchronous to TCK and active low for 3 clock periods.	Yes	Yes	Optional
Number of TAP Channels	Allow access to multiple scan chains.	4	4	2
Flash Programming Signals	Control of Vpp Enable, Busy/Ready and other user-defined signals	Yes	Yes	Optional
Throughput	Maximum throughput is provided by data compression allowing sustained data transmission rather than burst mode operation. (Refer to Figure 2)	Sustained TCK at 25 MHz		PC parallel port speed
Target Voltage	Drives voltage / tolerant voltage	3.3V / 5V		5V / 5V

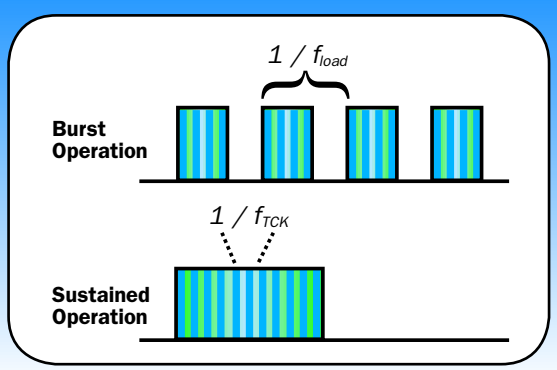
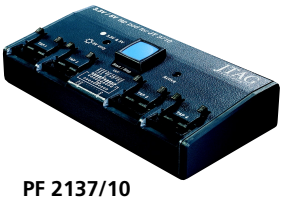


Figure 2. Burst Operation vs. Sustained

The effective operating frequency in burst mode, f_{eff} , is given by $f_{TCK} * f_{load} / (f_{TCK} + f_{load})$. f_{TCK} is the frequency of the boundary-scan clock and f_{load} is the frequency of the re-loading of memory in a burst type of operation. f_{eff} for burst mode is slower than both f_{TCK} and f_{load}.

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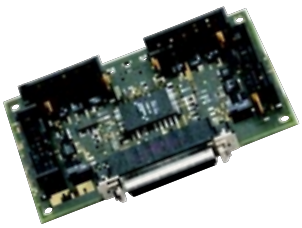


PF 2137/10

TAP PODs

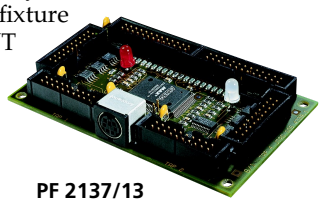
The JT 3710 and JT 3707 employ a 4-channel POD, located near the target, to distribute the boundary-scan signals to up to four targets for parallel programming and testing. The POD contains active line terminations necessary to maintain signal integrity in high-frequency applications.

There are three alternate POD packages for desktop use and for integration within a fixture in production situations:

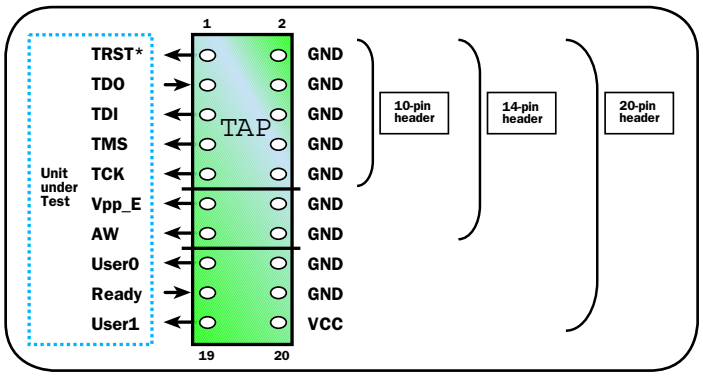


PF 2137/12

- **PF 2137/10:** Self-contained module with SCSI connector for cabling to the JT 3710 and JT 3707. Contains 4 TAP connectors for cabling to target boundary-scan chains.
- **PF 2137/12:** Ruggedized circuit board for mounting within a test fixture or other assembly, and directly connected via a SCSI-2 cable to the JT 3710 or JT 3707 controller.
- **PF 2137/13:** Ruggedized circuit board for mounting within a test fixture or other assembly, and arranged for cabling via standard IDC and D-connectors and a SCSI splitter to the front of the fixture.



PF 2137/13



Connection to the target printed circuit board can be made using an industry-standard 10-, 14-, or 20 pin connector as shown in Figure 3.

TDI on the header connects to the TDI pin of first device in the target scan chain. TDO on the header connects to the TDO pin of last device in the chain.

Figure 3. Pinout of 10-pin, 14-pin, and 20-pin Connector on TAP POD

Header Types

Number of Pins	Pitch	Used On	Part Numbers
10	0.1 inch	PM 3705 Explorer PF 2152 Evaluation Board	AMP 281279-1 T&B 609-1027 3M 2510-6002
14 (Same as above plus pins for AW and VPP_E)	0.1 inch	JTAGTECH demo board	AMP 281280-1 T&B 609-1427 3M 2514-6002
20	0.05 inch (Fine-pitch)	POD PF 2137/10	AMP 104068-1 T&B 311-020D272
20	0.1 inch	PODs PF 2137/12 and PF 2137/13	3M 2520-6002

Note: *The standard boundary-scan signals, TRST*, TDO, TDI, TMS, and TCK are on pins 1, 3, 5, 7, and 9, respectively, of all header types. For the 14-pin header, Vpp_E and AW are added. Vpp_E allows an on-board programming voltage to be applied to a flash or EEPROM device under control of the Vpp_E signal. AW (AutoWrite) is used to speed-up flash memory programming by driving the WE signal of a device directly . For the 20-pin header, two additional user signals are added plus a Ready pin to monitor a Ready_Busy signal present on some flash parts.*

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Interconnection Information

Connecting the JT 3710 and JT 3707 to the target follows three possible configurations, depending on the type of POD in use, as depicted in Figure 4:

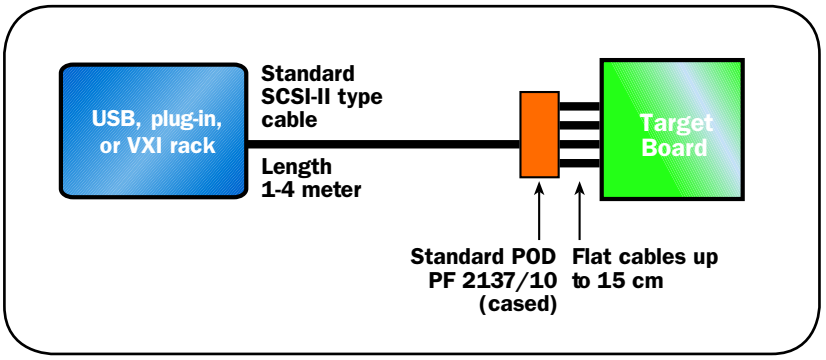


Figure 4a. Standard configuration for desktop use

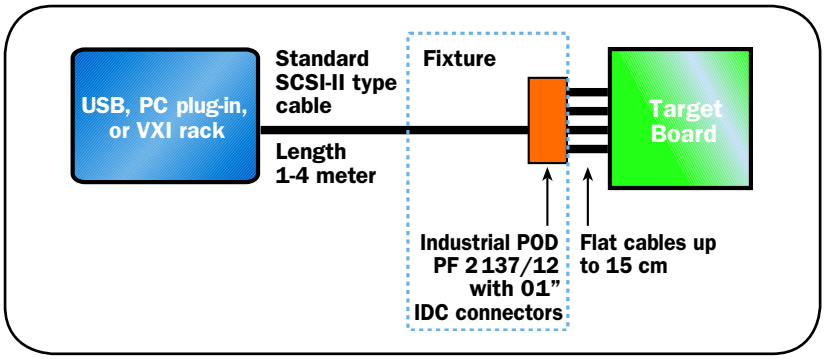


Figure 4b. Fixed configuration for integration in fixture using commercial connectors

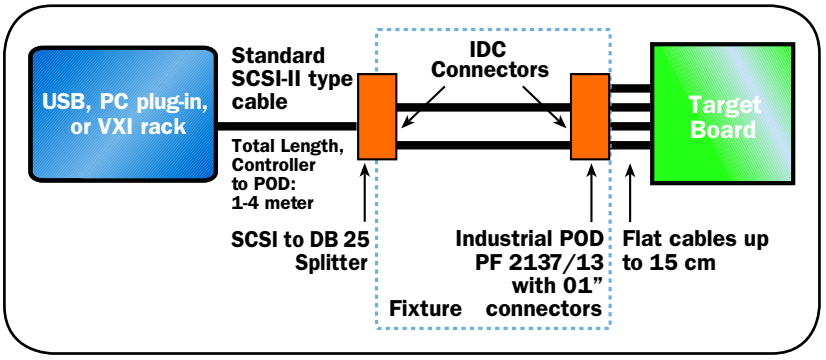


Figure 4c. Configuration for interchangeable fixture using commercial connectors

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Detailed Specifications

Controller Specifications

	ISA (JT 3710 only)	PCI (JT 3707 and JT 3710)	VXI (JT 3710 only)	USB (JT 3710 only)	PM 3705
Form Factor/ Dimensions	Standard ISA form factor 115 mm (H) 227 mm (L) 1 ISA slot	Standard PCI form factor 115 mm (H) 180 mm (L) 1 PCI slot	C-size VXI form factor 262 mm (H) 360 mm (L) 1 VXI slot	220 mm (L) 140 mm (W) 33 mm (H)	85 mm (L) 152 mm (W) 40 mm (H)
Weight	0.200 kg	0.148 kg	1.706 kg	0.824 kg	0.3 kg
Connectivity	Plugs into PC-AT 16-bit slot on ISA bus	Plugs into 32-bit slot on PCI bus	VXI slot Register-based	Connects to USB port on PC, via standard USB cable or hub	Parallel port of PC
Hot Insertion, Controller to Host	No	No	No	Yes	Yes
Hot Connection to Target	Yes	Yes	Yes	Yes	No
POD Type	External			2 types: External and integrated	N/A: POD not required
Cabling to POD	Up to 4-meter standard SCSI cable from controller board to TAP POD. Longer cable possible at slower TCK rates.				N/A: POD not required
Cabling to Target	Up to 15 cm, standard at 25 MHz (longer than 15 cm when board design for TAP is matched with POD characteristics or at lower frequencies)				Flat cable from Explorer to target, typically up to 50 cm
Installation	Base address is set using on-board switches	Plug-and-play	Logical address is set using on-board switches	Plug-and-play	Plug-and-play
TCK Maximum Clock Frequency	25 MHz	25 MHz	25 MHz	25 MHz	Typically 150 kHz, determined by the PC parallel port capability
Power	5 VA	5 VA	5 VA	5 VA	15V ± 20%, 300 mA, unstabilized from mains adapter. See note (*)
Standards	MIL-T-28800D, Type III, Class 5, Style E				Style EP
Environmental Specifications	Temperature, operating Temperature, limited operation Temperature, storage Temperature, transport Relative humidity, operating Relative humidity, storage and transport Altitude, operating Altitude, storage and transport Vibration		5° C to 40° C 0° C to 55° C -40° C to 70° C -40° C to 158° C 15% to 90% non-condensing 5% to 95% non-condensing 4500 m (15,000 ft.) 12000 m (40,000 ft.) Swept sine resonance search 5-55 Hz, 2 g (rms), 15 minutes per axis, 10 minutes resonance dwell		
Safety	IEC publication 348, Safety Requirements for Electrical Measuring Apparatus		IEC 1010 Class 2, VDE 0411, CSA-C22.2 No. 231		
TAP Signal Levels	Refer to DC Operating Conditions				TRST*,TCK,TMS, TDI: TTL (tri-state 25 mA sink, 15 mA drive) TDO: TTL(1 load)

Note (*) Power adapters: *European* *220 V, 50 – 400 Hz, 10 VA*
UK *240 V, 50 – 400 Hz, 10 VA*
USA *90 – 130 V, 50 – 400 Hz, 10 VA*

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TAP POD Specifications

	PF 2137/10	PF 2137/12	PF 2137/13
Type	Bench top, enclosed in plastic case	Ruggedized, for use in circuit board fixture	Ruggedized, for use in circuit board fixture
Dimensions	54 mm (L) 127 mm (W) 25 mm (H)	100 mm (L) 12 mm (W) 60 mm (H)	100 mm (L) 12 mm (W) 60 mm (H)
Weight	0.12 kg	0.54 kg	0.48 kg
Connector toward Controller	50-pin SCSI-2	50-pin SCSI-2	50-pin SCSI-2 (2) 25-pin sub-D-type connectors
Connectors toward Targets	(4) 20-pin, 0.05" pitch: AMP 104068-1 T&B 311-020D272	(4) 20-pin, 0.1" pitch: 3M 2520-6002 T&B 609-2027	(4) 20-pin, 0.1" pitch: 3M 2520-6002 T&B 609-2027
Power	Powered from the controller		
Signal Specifications	See following tables		
Environmental Specifications	Same as controller specifications		

DC Operating Conditions, PF 2137 TAP Outputs

Pin	Name	Description	I_{OL}	I_{OH}
1	TRST*	Test Logic Reset (optional hardware reset)	12 mA @ VOL = 0.45V	-4 mA @ VOH = 2.4V
5	>TDI	Test Data In, an output signal from the controller		
7	TMS	Test Mode Select		
9	TCK	Test Clock		
11	Vpp_E	Optional. Programming voltage enable. Controls application of programming voltage by the target.		
13	AW	Optional AutoWrite signal allows programming of flash memory to take place up to 3 times as fast		
15	User0	Optional programmable output		
19	User1	Optional programmable output		

Note: *TAP output is tri-stated when shifting is not taking place.*

DC Operating Conditions, PF 2137 TAP Inputs

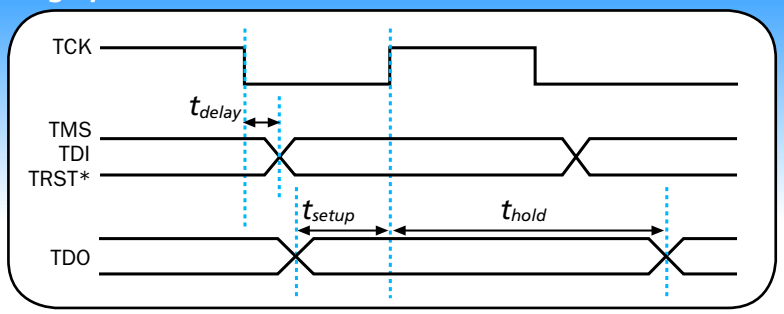
Pin	Name	Description	I_{IH}	I_{IH}	I_{OZ}	I_{OZ}
3	<TDO	Test Data Out, an input signal to the controller	+10mA @ Vin = 5.25V	-10mA @ Vin = GND	+40µA @ Vin = 5.25V	-40µA @ Vin = GND
17	Ready	Optional input to the controller for synchronizing purposes	+10mA @ Vin = 5.25V	-10mA @ Vin = GND	+40µA @ Vin = 5.25V	-40µA @ Vin = GND

Note: *All signals should be tri-stated when not in boundary-scan mode.*

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Timing Specification for PF 2137 POD for JT 3710 and JT 3707:



Symbol	Timing parameter	Min	Max
tdelay	TCK⬇ to output delay		0.6 ns
tsetup	TDO to TCK⬆ setup time	11.4 ns	
thold	TDO to TCK⬆ hold time	0 ns	

Note 1: *In IEEE Specification 1149.1 requires that TDI is stable on the low to high transition of TCK and changes on TDI must occur after the high-to-low transition of TCK.*
Note 2: *TDO of POD connects to TDI of target (See also Figure 3).*

Ordering Information

Order Number	Product Description	Principal Applications	Form Factor	POD (See notes)
PM 3705	Explorer Boundary-Scan Controller	Testing and PLD on-board programming	PC parallel port-based module	N/A
JT 3707/PCI	DataBlasterLite high speed Boundary-Scan Controller		PCI card	1
JT 3710/ISA	DataBlaster highest-speed Boundary-Scan Controller	Testing, PLD and flash memory on-board programming	ISA card	1
JT 3710/PCI			PCI card	1
JT 3710/VXI			C-sized VXI card	1
JT 3710/USB			USB module	1
JT 3710/USB-4T				2

Note 1: *Controller includes one of the versions of the actively-terminated PF 2137 TAP POD with four channels for multi-chain testing, SCSI cable to connect the controller to the POD, and two cables for connecting the POD to the target.*

Note 2: *Controller includes an integrated POD with four channels for multi-chain testing and parallel flash memory programming, and two cables for connecting to the target.*

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