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TIME & FREQUENCY SOLUTIONS

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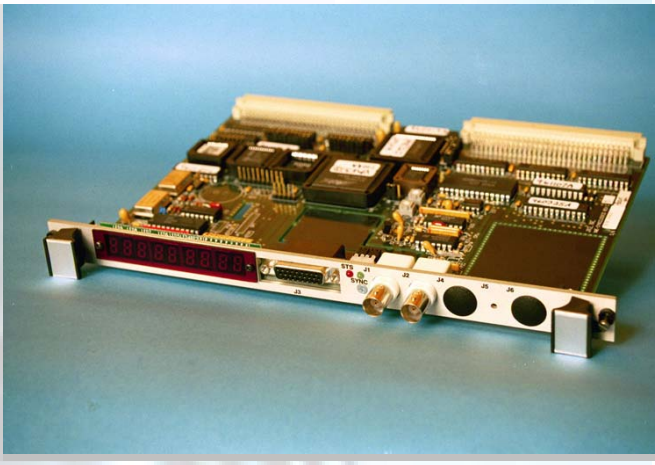
VME-SyncClock32

Board-Level Timing

The VME-SyncClock32 provides precision timing to a host computer through the VME bus. The on-board microprocessor automatically synchronises the clock to a range of signal inputs, such as 1PPS, IRIG and NASA time codes.

Features

- **Continual time error measurement between on-board clock and the reference input signals and adjusts the error measurement of propagation delay.**
- **Range of input and output options, including IRIG timecodes**
- **Optional disciplined TXCO or OXCO.**
- **3 user-programmable pulse rates**
- **Optional GPS receiver**
- **Time-tagging of external events**
- **Match Time feature, from which Internal or External processes may be automatically initiated or terminated.**



Optional Disciplined Oscillator

Enhance performance by selecting optional disciplined TXCO or OXCO. .By locking the oscillator to the synchronising time source, the oscillator is automatically calibrated, ensuring that a precise timebase is always available. During periods where there is no synchronising time source, the performance of the module reverts to the oscillator specification. When the input signal is available the oscillator will return to normal disciplining.

58 bits of BCD time data are available to the host computer using two zero latency time reads. The time message contains units of microseconds through units. A status word is available using an additional read.

Pulse Rates

The VME–SyncClock32 provides three user programmable pulse rates. Two pulse rates, Clock Low and Clock High, are available on the multi-pin connector. The third rate generator provides heartbeat timing to the host computer.

Optional GPS Receiver

The optional on-board GPS Receiver receives and decodes transmissions from GPS satellites, allowing the timing system to accurately synchronise to Universal Coordinated Time (UTC). Automatic leap year, leap second correction and accurate positional information are additional benefits provided by the GPS option.

N.B. Software packages are available as options. C language examples are supplied as standard.

Specifications

Input Specification

Timecodes:	IRIG A & B, NASA 36
1 PPS Input:	TTL positive edge, 1μ Second accuracy
External Event:	TTL positive or negative edge. Resolution – 100ns-unit year

Output Specification

IRIG-B DC Level Shift:	TTL
Match Pulse:	TTL level at Start-Stop time
Clock Low Pulse:	TTL negative going
Clock High Pulse:	TTL negative going
Heartbeat Rate:	Interrupt, flag, TTL negative going
BCD Time:	μs-unit year on demand, no latency, 58 bits in two 28-bit words
Status Word:	8 bits
Interrupts:	External event, RAM FIFO, Heartbeat, Match Time
Flags:	Dual Port RAM data ready, FIFO data ready, In sync, Heartbeat, Match Time, External Event
Connectors:	BNC, high density DB-26
Host Interface:	Single-slot 32 VME

Environmental (Operating & Storage)

Temperature:	0°C to +55°C
Humidity:	Up to 95% RH (non condensing)
EMC:	CE Compliant

As we are always seeking to improve our products, the information in this document only provides general indications of product capability, suitability and performance, none of which shall form any part of any contract.

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