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Measures C-V and C-t characteristics

SEMICONDUCTOR

590 C-V Analyzer



- 100kHz, 1MHz, or 100kHz/1MHz test frequencies
- Measures capacitance (10fF–20nF) and conductance (0.1nS–1µS)
- Internal correction for errors due to cables, connections, and switching paths
- Built-in test setup and correction value storage, analysis, and plotter control to minimize computer programming

Ordering Information

590/100k
100kHz C-V Analyzer with IEEE-488 Interface

590/1M
1MHz C-V Analyzer with IEEE-488 Interface

590/100k/1M
100kHz/1MHz C-V Analyzer with IEEE-488 Interface

590/100k/4
100kHz C-V Analyzer with Calibrated 5904 Adapter and IEEE-488 Interface

590/100k/1M/4
100kHz/1mHz C-V Analyzer with Calibrated 5904 Adapter and IEEE-488 Interface

This product is available with an Extended Warranty.

Accessories Supplied

Two Model 7051-5 BNC Interconnect Cables, 1.5m (5 ft)

The Keithley 590 C-V Analyzer measures capacitance versus voltage (C-V) and capacitance versus time (C-t) characteristics of semiconductor devices. Unlike other capacitance measurement instruments, the 590 has been tailored to the requirements of semiconductor device testing.

High frequency (100kHz or 1MHz) C-V measurements are commonly applied to test p-n or schottky junction and Metal-Insulator-Semiconductor (MIS) devices for device characterization and process control. C-V results are highly correlated with performance parameters of functional devices such as FETs, memory cells, CCDs, and isolation structures.

Specifically, the Model 590 provides:

- 0.1fF sensitivity to test small devices.
- Ranges up to 20nF (at 100kHz, using 5904 adapter) to test large, leaky, or forward biased devices.
- Test signal voltage of 15mV rms.
- Choice of 1MHz frequency for compliance with existing test standards or 100kHz for improved resolution, range, and accuracy.
- Selectable measurement rate (1 to 1000 readings per second) and filter to optimize speed/resolution trade-offs.
- Sophisticated correction for transmission line errors due to device connections.
- Built-in test setup and correction value storage, analysis, and plotter control to minimize computer programming.

Measure C-V and C-t, Not Just Capacitance

C-V and C-t data are used to determine important characteristics such as semiconductor doping profiles, threshold voltage, oxide characteristics, mobile ion density, interface trap density, and minority carrier lifetime. The internal voltage source can supply up to 50mA from –20V to 20V with 5mV resolution in the waveforms C-V and C-t measurements require: DC, Stair, Dual Stair, and Pulse. Up to 200V can be supplied and monitored using an external source. Rear panel BNC trigger connectors can be used to coordinate timing with external sources such as the Keithley Model 230.

Excellent Sensitivity and Measurement Range

The excellent sensitivity (0.1fF and 0.1nS) and measurement range (20nF and 20mS) of the Model 590 meet test requirements of demanding applications such as characterization of very small, very large, leaky, or forward biased devices.

The Model 590 is available with test frequencies of 1MHz (590/1MHz) or 100kHz (590/100k). The dual frequency Model 590/100k/1M provides the flexibility to select the required measurement frequency at the time of measurement.

All three 590 models use a 15mV rms test signal. Testing semiconductor devices with larger test signals can cause curve shape distortion and loss of detail.

A 1MHz test frequency is traditionally specified in C-V test procedures requiring "high-frequency" device characteristics. In many cases 100kHz C-V measurements are replacing 1MHz as the standard, offering better accuracy (0.12% vs. 0.29%) and reduced errors due to cabling or device series resistance.

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Verify Accuracy to the DUT

The Model 590 achieves its specified measurement accuracy despite the effects of the cables and switching between the C-V instrument and the device-under-test (DUT). The Model 590 offers ZERO to suppress "probes up" offsets as well as sophisticated compensation for device connections.

By measuring the precise values of calibration capacitors connected through the measurement pathway, the Model 590 adjusts its display and bus readings to compensate for transmission line errors. Only the linearity, not the characteristic impedance, of the 2-port connection system is assumed.

Up to seven sets of correction values may be stored internally, and an unlimited number may be transferred through IEEE-488, to correct for each pathway in multiple pin systems.

Dual Reading Buffer with Analysis

Acquired readings are stored in the internal 450 point data buffer. A second 450-point data buffer is used for data analysis or output. Built-in analysis routines include Parallel/Series Model, C_{MAX}, C/C_O, $1/C^2$, C_A–C_B, and V_A–V_B (see specifications for details).

The rate at which readings are acquired and transferred into the buffer is selectable to address the variety of test requirements encountered in C-V and permit optimization of speed/resolution tradeoffs.

BUFFERED READINGS	RESOLUTION (digits)	MEASUREMENT RATE (rdg/s)
C	3½	488
C, G, V	3½	75
C, G, V	4½	1, 10, or 16

Minimize Computer Programming

Seven different complete front panel setups can be saved and recalled from the internal non-volatile memory to speed changes between setups and assure setup accuracy. For setting measurement parameters using IEEE-488, the Model 590's TRANSLATOR capability allows the user to define his own command syntax, replacing long command strings with simple user-defined names such as "CV1."

There is no need to tie up a computer to plot results either. With the Model 590, completely labelled plots of acquired or analyzed data can be sent to an HPGL plotter using the IEEE-488 bus. No software or computer is needed.

Rear panel analog outputs are also provided for the raw (uncorrected and unanalyzed) C or G values. These analog signals can be viewed on an oscilloscope or analog plotter.

FIGURE 1: Model 590 Block Diagram

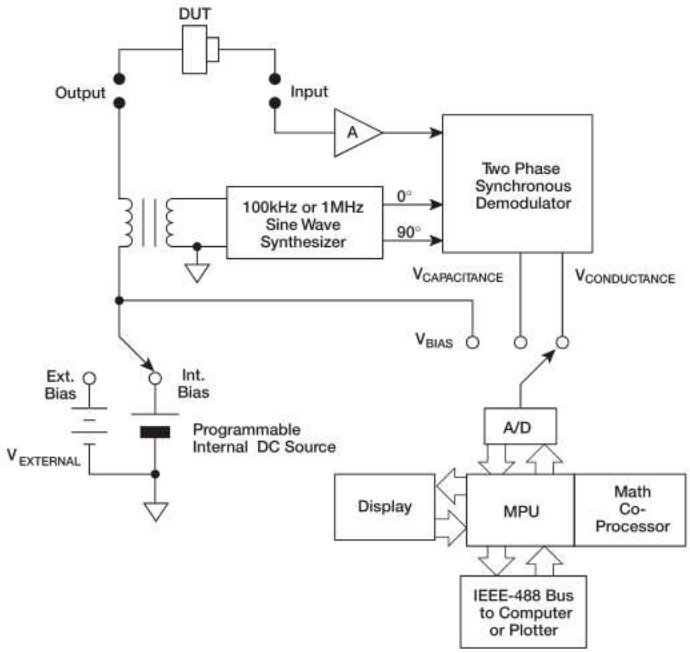


FIGURE 3: Model 590 Connection Correction Methods

METHOD	DESCRIPTION	TYPICAL ACCURACY	COMMENTS
1	Driving point (front panel or bus)	2%	Cables only
2	Transmission line parameters (bus only)	1.5%	Can be used with complex paths
3	Calibration capacitor (bus only)	0.5%	Can be used with complex paths



Model 590 rear panel

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C-V Analyzer

100 kHz (4½ Digits)

RANGE	RESOLUTION	ACCURACY (1 Year)[2] 18°–28°C ±(%rdg + counts)	P-P NOISE[5] FILTER ON	TEMPERATURE COEFFICIENT 0°–18°C & 28°–50°C ±(%rdg + counts)/°C	SHUNT CAPACITANCE LOADING EFFECT[4] ±(%rdg + counts)
2 pF	0.1 fF	0.12% + (500 × G/G_{FS} + 200)	6 fF	0.02% + (20 × G/G_{FS})	0.1 % + (3 × G/G_{FS})
2 μS	0.1 nS	0.12% + (50 × C/C_{FS} + 200)	4 nS	0.02% + (7 × C/C_{FS})	0.1 % + (3 × C/C_{FS})
20 pF	1 fF	0.12% + (260 × G/G_{FS} + 10)	6 fF	0.02% + (20 × G/G_{FS})	0.1 % + (3 × G/G_{FS})
20 μS	1 nS	0.12% + (22 × C/C_{FS} + 10)	4 nS	0.02% + (7 × C/C_{FS})	0.1 % + (3 × C/C_{FS})
200 pF	10 fF	0.12% + (260 × G/G_{FS} + 5)	90 fF	0.02% + (20 × G/G_{FS})	0.1 % + (3 × G/G_{FS})
200 μS	10 nS	0.12% + (22 × C/C_{FS} + 5)	60 nS	0.02% + (7 × C/C_{FS})	0.1 % + (7 × C/C_{FS})
2 nF	100 fF	0.12% + (260 × G/G_{FS} + 5)	900 fF	0.02% + (20 × G/G_{FS})	0.02% + (2 × G/G_{FS})
2 mS	100 nS	0.12% + (22 × C/C_{FS} + 5)	0.6 μS	0.02% + (7 × C/C_{FS})	0.02% + (3 × C/C_{FS})
20 nF *	1 pF	0.25% + (260 × G/G_{FS} + 5)[3]	9 pF	0.1 % + (30 × G/G_{FS})	0.02% + (2 × G/G_{FS})
20 mS	1 μS	0.25% + (22 × C/C_{FS} + 5)	6 μS	0.1 % + (10 × C/C_{FS})	0.02% + (2 × C/C_{FS})

Accuracy is maximum limit for Q≥20; typical for Q<20.

*Using Model 5904 20nF/20mS Input Adapter.

1 MHz (4½ Digits)

RANGE	RESOLUTION	ACCURACY (1 Year)[2] 18°–28°C ±(%rdg + counts)	P-P NOISE[5] FILTER ON	TEMPERATURE COEFFICIENT 0°–18°C & 28°–50°C ±(%rdg + counts)/°C	SHUNT CAPACITANCE LOADING EFFECT[4] ±(%rdg + counts)
20 pF	1 fF	0.29% + (300 × G/G_{FS} + 10)	6 fF	0.02% + (20 × G/G_{FS})	0.5 % + (25 × G/G_{FS})
200 μS	10 nS	0.29% + (120 × C/C_{FS} + 10)	40 nS	0.02% + (8 × C/C_{FS})	0.5 % + (10 × C/C_{FS})
200 pF	10 fF	0.29% + (300 × G/G_{FS} + 5)	100 fF	0.02% + (20 × G/G_{FS})	0.35% + (40 × G/G_{FS})
2 mS	100 nS	0.29% + (120 × C/C_{FS} + 5)	700 nS	0.02% + (8 × C/C_{FS})	0.35% + (16 × C/C_{FS})
2 nF	100 fF	0.29% + (300 × G/G_{FS} + 5)	200 fF	0.02% + (20 × G/G_{FS})	0.35% + (40 × G/G_{FS})
20 mS	1 μS	0.29% + (120 × C/C_{FS} + 5)	1 μS	0.02% + (8 × C/C_{FS})	0.35% + (16 × C/C_{FS})

Accuracy is maximum limit for Q≥20; typical for Q<20.

NOTES:

1. G = conductance reading; C = capacitance reading; G_{FS} = full scale conductance; C_{FS} = full scale capacitance. Range and accuracy designations based on parallel RC model.
2. Front panel accuracy is relative to calibration source accuracy. Add front panel accuracy and source accuracy for total accuracy. Factory calibration source accuracy is 0.06% for 100kHz and 0.08% for 1MHz. CAL is used to cancel initial zero, gain, and phase error terms within 8 hours of measurement or whenever ambient temperature changes by more than 2°C.
3. The 5904 must be calibrated with a particular 590/100k to achieve specified accuracy.
4. "Shunt Capacitance Loading" is additional accuracy with equal shunt load on Output and Input, per 100pF shunt load.
5. Noise specified with 500pF shunt loading on Output and Input. Noise on 2pF and 20pF ranges is typical with 100pF shunt load; 500pF will increase noise no more than ×2. Measured at 10 rdg/s rate.

CAPACITANCE NON-LINEARITY: <0.1% of range, for Q > 20 or D < 0.05, 18°–28°C.

TEST VOLTAGE: 15mV rms ±10%.

TEST FREQUENCY: 590/100k: 100kHz. 590/1M: 1MHz. Tolerance: ±0.1%.

ANALYSIS CAPABILITY

(Programming & output available from front panel or IEEE-488 bus)

READING BUFFERS A and B: Two data buffers allow storage and mathematical manipulation on up to 450 measurement triplets: capacitance, conductance, and voltage. In C vs. t, capacitance and index only are stored (up to 1350 points).

1/C2: Performs the inverse of C^2 on the capacitance data stored in reading buffer.

C/CO: Allows normalization of capacitance readings stored in reading buffer to a user-programmable reference value C_O.

CMAX: Searches reading buffer for the maximum capacitance value.

CA–CB: Sequentially computes the difference between corresponding capacitance readings stored in reading buffer A and reading buffer B.

|VA–VB|: Calculates the corresponding difference in applied voltage for values of capacitance in reading buffer B equal to each value in reading buffer A.

C vs. t: Allows fast measurement of capacitance vs. time (1000 rdg/s).

CABLE COMPENSATION

(Up to 8 setups can be stored in non-volatile memory.)

CALIBRATION CAPACITOR COMPENSATION: Corrects for errors due to cables or switching matrix up to 5 meters effective (electrical equivalent) length. Two measurements are made with cables and matrix terminated with precision reference capacitors in place of the DUT. Model 5907 Cable/Matrix Calibration Capacitor Set required. Bus programmable only. Accuracy: ±(0.5% + applicable front panel specification), typical.

SINGLE-ENDED CABLE and S-PARAMETER COMPENSATION can also be made. See manual for detailed information.

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C-V Analyzer

ACCESSORIES AVAILABLE

CABLES

7007-1	Shielded IEEE-488 Digital Cable, 1m (3.3 ft)
7007-2	Shielded IEEE-488 Digital Cable, 2m (6.6 ft)
7051-2	BNC Interconnect Cable, 0.6m (2 ft)
7051-5	BNC Interconnect Cable, 1.5m (5 ft)
7051-10	BNC Interconnect Cable, 3m (10 ft)

ADAPTER

5904	20nF/20mS Adapter

CALIBRATION

5905	Calibration Sources for 590/1M
5906	Calibration Sources for 590/100k/1M/4
5907	Cable/Matrix Calibration Sources
5909	Model 82 Calibration Sources

SOFTWARE

Metrics-ICS	Windows-based software for controlling Model 590
Metrics-ICS-CV	Analysis Libraries
TESTPOINT	Graphical programming environment for test

RACK MOUNT KITS

2288	Fixed Rack Mount Kit
2289A	Slide Rack Mount Kit

BIAS SOURCE

INTERNAL BIAS SOURCE OUTPUT: –20.000V to +20.000V in 5mV steps.

ACCURACY (1 Year, 18°–28°C): ±(0.05% setting + 10mV) exclusive of loading errors.

DC OUTPUT RESISTANCE: 5Ω maximum.

TEMPERATURE COEFFICIENT (0°–18°C & 28°–50°C): ±(0.005% + 1mV)/°C.

MAXIMUM OUTPUT CURRENT: ±50mA.

SETTLING TIME: <1ms to 1% of final value.

NOISE: Typically <200μV p-p, 0.1Hz-1MHz; 3mV p-p to 75MHz.

BIAS WAVEFORM:

DC: Outputs the programmed value.

STAIR: Output changes in increments of BIAS STEP V from FIRST BIAS V to LAST BIAS V.

DUAL STAIR: Output changes in increments of BIAS STEP V from FIRST BIAS V to LAST BIAS V, then back to FIRST BIAS V.

PULSE: Outputs pulse train; amplitude increments by BIAS STEP V from FIRST BIAS V to LAST BIAS V (each pulse is from DEFAULT BIAS V to FIRST BIAS V for duration of STEP TIME, then back to DEFAULT BIAS V). Also programmable for single pulse.

EXT: Allows application of external bias source (via VOLTAGE BIAS INPUT).

BIAS PARAMETERS: FIRST BIAS V, LAST BIAS V, DEFAULT BIAS V, BIAS STEP V, START TIME, STOP TIME, STEP TIME, COUNT.

BIAS STEP V: Programmable in 5mV steps to 20V. Polarity selectable + or –.

START TIME: After transition from DEFAULT BIAS V to FIRST BIAS V, START TIME must elapse before first measurement. Programmable in increments of 1024μs from 1 to 65,536 increments. Accuracy: ±(0.1% + 1ms).

STEP TIME: The period between the transition of BIAS STEP V and the start of the next measurement. Programmable in increments of 1024μs from 1 to 65,536 increments. Accuracy: ±(0.1% + 1ms).

STOP TIME: The period between the end of the final measurement and the transition from LAST BIAS V to DEFAULT BIAS V. Programmable in increments of 1024μs from 1 to 65,536 increments. Accuracy: ±(0.1% + 1ms).

VOLTAGE BIAS MONITOR: Rear panel output terminals allow monitoring of the DC BIAS SOURCE output or externally applied VOLTAGE BIAS INPUT. Level: 1V = 1V out. Output Resistance: 1kΩ.

VOLTAGE BIAS DISPLAY: Front panel 4½-digit display allows direct readback of the DC BIAS SOURCE output or externally applied VOLTAGE BIAS INPUT. Accuracy: ±(0.05% + 5 counts). Temperature Coefficient: ±(0.005% + 0.1 count)/°C.

IEEE-488 BUS IMPLEMENTATION

MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, SPE, SPD.

UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.

INTERFACE FUNCTIONS: SH1, AH1, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, E1, C0 (for stand alone plotting C28 is used).

PROGRAMMABLE PARAMETERS: Range, Function, Zero, Filter, Frequency, Bias Waveform, Bias Parameters, Plotting, Plotter Parameters, EOI, Trigger, Terminator, 450 Data Point Storage, Calibration, Cable Correction, Display, Status, Service Request, Self Test, Output Format.

TRANSLATOR: Up to 250 bytes of definitions allow variable passing, definition decomposition and listing.

GENERAL

DISPLAY: Three 4½-digit displays for capacitance, conductance, and voltage bias.

RANGE: Manual or autoranging (for rates up to 18 rdg/s); 10% overrange allowable.

OVERRANGE INDICATION: Display reads OFLO.

AVAILABLE MEASUREMENT RATES (to internal buffer): 4½-Digit: 1, 10, and 16 rdg/s. **3½-Digit:** 75 and 488 rdg/s.

FILTER: 1-pole analog; pole at 37Hz. Filters both capacitance and conductance signals. For FILTER off, multiply p-p noise specification by 5. **CAL:** Initiates self-calibration to internal reference capacitor. Used to cancel initial zero, gain, and phase errors.

ZERO: Allows zeroing of on range readings. Allows relative readings to be made with respect to a baseline value.

MAXIMUM OVERLOAD:

OUTPUT, Voltage Bias Input: 200V internally fused at 1/8A.

Input: Clamped by diodes to ±0.7V.

Maximum Current: 200mA.

Analog Outputs: 15V.

MAXIMUM COMMON MODE VOLTAGE (INPUT and OUTPUT, Voltage Bias Input): 30V rms, DC to 60Hz. Rear panel switch allows connection of INPUT low to chassis.

ANALOG OUTPUTS (Capacitance and Conductance):
Level: 2V output at full range.
Initial Offset: ±25mV
Output Resistance: 1kΩ.
Response Time: 1ms to 1% of final value with filter off; 25ms maximum with filter on.

PLOTTER: Digital plotter output controls HP7470A plotter or equivalent using HPGL® via IEEE-488 for real-time plotting of all measurements as well as results of math computations, with grids and labels. Talks to plotter on address 05. HPGL commands used are IN, IP, IW, PA, PD, PU, SC, SI, SP.

FRONT PANEL SETUPS: Up to 7 front panel setups can be stored in nonvolatile memory.

EXTERNAL TRIGGER: TTL compatible External Trigger Input and Output.

INPUT CONNECTORS: Isolated BNC for INPUT and Voltage Bias Input.

OUTPUT CONNECTORS: Isolated BNCs for OUTPUT, Voltage Bias Monitor, Analog Outputs, and External Trigger.

ENVIRONMENT: Operating: 0°–50°C, relative humidity 70% non-condensing up to 35°C. **Storage:** –25° to +65°C.

WARM-UP: 1 hour to rated accuracy.

COOLING: Internal fan and filter for forced air cooling.

POWER: 105–125V or 210–250V (external switch selected), 50Hz to 60Hz, 100VA maximum. 90–110V and 180–220V version available upon request.

DIMENSIONS, WEIGHT: 133mm high × 435mm wide × 448mm deep (5¼ in × 17⅛ in × 17¼ in). Net weight 9.1kg (20 lb).

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