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KPCI-PIO24 Parallel Digital I/O Board

User's Manual



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KPCI-PIO24
Parallel Digital I/O Board
User's Manual

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Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read and follow all installation, operation, and maintenance information carefully before using the product. Refer to the manual for complete product specifications.

If the product is used in a manner not specified, the protection provided by the product may be impaired.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating properly, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Keithley products are designed for use with electrical signals that are rated Installation Category I and Installation Category II, as described in the International Electrotechnical Commission (IEC) Standard IEC 60664. Most measurement, control, and data I/O signals are Installation Category I and must not be directly connected to mains voltage or to voltage sources with high transient over-voltages. Installation Category II connections require protection for high transient over-voltages often associated with local AC mains connections. Assume all measurement, control, and data I/O connections are for connection to Category I sources unless otherwise marked or described in the Manual.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Operators of this product must be protected from electric shock at all times. The responsible body must ensure that operators are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product operators in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

When installing equipment where access to the main power cord is restricted, such as rack mounting, a separate main input power disconnect device must be provided, in close proximity to the equipment and within easy reach of the operator.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

The instrument and accessories must be used in accordance with its specifications and operating instructions or the safety of the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If  or  is present, connect it to safety earth ground using the wire recommended in the user documentation.

The  symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The  symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

To clean an instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

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1
Overview

This manual contains descriptive information and installation and use instructions for the KPCI-PIO24 digital interface board.

The manual is intended for data acquisition system designers, engineers, technicians, scientists, and other users responsible for setting up, cabling, and wiring signals to KPCI-PIO24 boards. It is assumed that users are familiar with data acquisition principles and with their particular application.

In addition to this Overview, the manual is organized as follows:

- Section 2 briefly describes features and characteristics of the KPCI-PIO24.
- Section 3 describes how to unpack, install, and connect the board and outlines software options and installation.
- Section 4 provides the following information:
  a. Describes KPCI-PIO24 interrupt characteristics.
  b. Describes memory-mapping information for special situations; you normally can and should skip that information. Use the DriverLINX driver provided with your board for virtually all programming situations.
- Section 5 describes how to troubleshoot your system and obtain technical support.
- Appendix A contains KPCI-PIO24 specifications.
- Appendix B is a glossary of some terms used in this manual.

2
General Description

Specifications

General specifications are listed in Appendix A. I/O connections are identified in Section 3, and I/O addresses are defined in Section 4.

System requirements

The system capabilities required to run the KPCI-PIO24 board, and to use the DriverLINX software supplied with the board, are listed in Table 2-1.

Table 2-1
System requirements

CPU Type	Pentium or higher processor on motherboard with PCI bus version 2.1
Operating system	Windows® 95 or higher
	Windows® NT version 4.0 or higher
Memory	16 MB or greater RAM when running Windows® 95 or 98
	32 MB or greater RAM when running Windows® NT
Hard disk space	4 MB for minimum installation
	50 MB for maximum installation
Other	A CD ROM drive*
	A free PCI bus expansion slot
	Enough reserve computer power supply capacity to power the KPCI-PIO24 board, which draws 25 W at 5 VDC

* Any CD ROM drive that came installed with the required computer should be satisfactory. However, if you have post-installed an older CD ROM drive or arrived at your present system by updating the microprocessor or replacing the motherboard, be aware that some early CD ROM drives do not support the long file names often used in 32 bit Windows files.

Functional description

The KPCI-PIO24 is a 24-bit parallel digital interface board designed for the PCI bus. The KPCI-PIO24 works in a Windows 95/98/NT environment and takes advantage of the 32 bit width and the Plug and Play feature of the PCI bus. The KPCI-PIO24 also has an easily accessible interrupt configuration. The KPCI-PIO24 meets a wide variety of parallel I/O requirements, including communicating with peripherals, operating relays, and reading switch inputs. All I/O lines are TTL compatible.

Standard digital I/O emulation

The 24 I/O lines emulate the I/O lines of an Intel 8255 Programmable Peripheral Interface (PPI) chip configured for control register mode 0, as follows:

- For the emulated 8255 chip there is a PA port, a PB port and a PC port.
- The PA and PB ports are byte-wide (8-bits) and can be set independently under software control as inputs or outputs.
- The PC port is byte-wide but can be divided into two separate 4-bit ports: PC lower and PC upper, each of which can be set up as either inputs or outputs.

Most existing application software and data acquisition packages work with the KPCI-PIO24 board. If you wish to reuse existing port I/O programs previously designed for ISA boards, refer to information about the Hardware I/O Emulation driver included on your DriverLINX CD-ROM. The Hardware I/O Emulation driver may be used only with Windows 95/98. Refer also to "Setting control and data registers" in Section 4 of this manual.

Other I/O characteristics

Additional I/O port characteristics are summarized below:

- The KPCI-PIO24 can output higher currents than the industry standard 8255 chip. Output current capabilities of 15mA (source) and 64mA (sink) allow it to control many LEDs, Opto 22 modules, and relays directly.
- The PA, PB, and PC ports can always be read/write accessed, regardless of the direction they were initially configured for, without the external signal level being affected. For example, when a port is configured as an output, it is still possible to execute a read of that port. The data returned by the read is the data latched in the I/O register.
- On power-up or whenever the computer's hardware reset line is asserted, all ports are cleared and set as inputs.
- The PA, PB and PC ports interface to user I/O connections via a standard 37-pin connector.
- Two externally accessible inputs allow for flexible interrupt configuration: $\overline{\text{INT_EN}}$ (external interrupt enable, active low) and INT_REQ (external interrupt request, edge triggered).
- Computer power supply voltages are made available at the I/O connector for use in external circuits.

Bus control

The KPCI series of data acquisition boards use the AMCC S5933 PCI bus controller, which is universally recognized as an industry standard. Its PCI bus interface includes all the components necessary for optimal PCI bus utilization. The AMCC S5933 provides two modes of operation: bus mastering and target. The KPCI-PIO24 normally only implements the target mode. The target mode, also referred to as passthrough operation, provides a simple register access port to the PCI bus. High speed data transfer via bus mastering is unnecessary for the simple digital I/O of the KPCI-PIO24 board.

The KPCI-PIO24 maps these AMCC S5933 registers as a memory mapped peripheral, though not all are used for operation of the KPCI-PIO24:

- All sixteen 32 bit operation registers (64 bytes total)
- All eight 32 bit specific functional registers

All memory addresses of registers are automatically assigned by the PCI bus Plug and Play feature upon system power-up.

Software

The user can select a fully integrated data acquisition software package (e.g., TestPoint or LabVIEW) or write a custom program supported by DriverLINX. DriverLINX software is included with the hardware.

DriverLINX supports programmers who wish to create custom applications using Visual C/C++, Visual Basic, or Delphi. DriverLINX accomplishes foreground and background tasks to perform data acquisition. TestPoint is a fully featured, integrated application package with a graphical drag-and-drop interface, which can be used to create data acquisition applications without programming. LabVIEW is a fully featured graphical programming language used to create virtual instrumentation.

Refer to Section 3, "Installation," for more information about those programs.

3
Installation

This section describes:

- Software options and how to install them.
- Unwrapping the KPCI-PIO24 board to avoid static damage; inspection of the board before installation.
- Locating connectors, connecting the board to I/O cables and interface accessories, installing the board, and connecting to external circuits.

Installing the software

NOTE *Install the DriverLINX software before installing the KPCI-PIO24 card. Otherwise, the device drivers will be more difficult to install.*

Software options

The KPCI-PIO24 has two software options. The user can select a fully integrated data acquisition software package (e.g., TestPoint or LabVIEW). The user can also run a custom program in Visual C/C++, Visual Basic, or Delphi using DriverLINX (included with the hardware). A summary of the pros and cons of using integrated packages or writing custom programs is provided in the Keithley Full Line Catalog. The KPCI-PIO24 has fully functional driver support for use under Windows 9X/NT/2K/XP.

DriverLINX driver software for Windows 9X/NT/2K/XP

DriverLINX software, supplied by Keithley with the KPCI-PIO24 board, provides convenient interfaces to configure and set I/O bits without register-level programming.

Most importantly, however, DriverLINX supports those programmers who wish to create custom applications using Visual C/C++, Visual Basic, or Delphi. DriverLINX accomplishes foreground and background tasks to perform data acquisition. The software includes memory and data buffer management, event triggering, extensive error checking, and context sensitive online help.

More specifically, DriverLINX provides application developers a standardized interface to over 100 services for creating foreground and background tasks for the following:

- Analog input and output
- Digital input and output
- Time and frequency measurement
- Event counting
- Pulse output
- Period measurement

In addition to basic I/O support, DriverLINX also provides:

- Built-in capabilities to handle memory and data buffer management
- A selection of starting and stopping trigger events, including pre-triggering, mid-point triggering and post-triggering protocols
- Extensive error checking
- Context-sensitive on-line help system

DriverLINX is essentially hardware independent, because its portable APIs work across various operating systems. This capability eliminates unnecessary programming when changing operating system platforms.

TestPoint

TestPoint is a fully featured, integrated application package that incorporates many commonly used math, analysis, report generation, and graphics functions. TestPoint's graphical drag-and-drop interface can be used to create data acquisition applications, with minimal programming, for IEEE-488 instruments, data acquisition boards, and RS232-485 instruments and devices.

TestPoint includes features for controlling external devices, responding to events, processing data, creating report files, and exchanging information with other Windows programs. It provides libraries for controlling most popular GPIB instruments. ActiveX controls plug directly into TestPoint, allowing additional features from third party suppliers.

LabVIEW

LabVIEW is a fully featured graphical programming language used to create virtual instrumentation. It consists of an interactive user interface, complete with knobs, slides, switches, graphs, strip charts, and other instrument panel controls. Its data driven environment uses function blocks that are virtually wired together and pass data to each other. The function blocks, which are selected from palette menus, range from arithmetic functions to advanced acquisition, control, and analysis routines. Also included are debugging tools, help windows, execution highlighting, single stepping, probes, and breakpoints to trace and monitor the data flow execution. LabVIEW can be used to create professional applications with minimal programming.

Check www.keithley.com for current LabVIEW drivers.

Installing DriverLINX

Refer to the manual that accompanies your DriverLINX software for installation instructions.

NOTE *Always install DriverLINX before installing the LabVIEW VIs. Both TestPoint and the LabVIEW VIs use DriverLINX to access the board's hardware resources.*

Using TestPoint with your hardware

TestPoint's Digital I/O object (DIO) cannot be used with the KPCI-PIO96 (KPCI-PIO24) board. Instead, TestPoint provides a user defined object (UDO) for access to digital I/O channels on plug-in boards supported by DriverLINX.

This UDO (DL_DIO) is installed when the TestPoint application is installed and can be found in the Dldio.tst example program. This example program is located in the same directory as the TestPoint application (c:\testpt).

Since this UDO makes calls into the DriverLINX driver, DriverLINX must be installed and functional.

Once the Dldio.tst example has been opened, either use the 'Save As' feature to create your own application or copy and paste the UDO from the example into your own application.

Unwrapping and inspecting the KPCI-PIO24 board

CAUTION **Discharge static voltage differences between the wrapped board and the handling environment before removing the board from its protective wrapper. Failure to discharge static electricity before handling may damage semiconductor circuits on the board.**

Handle the board using the mounting bracket. Do not touch the circuit traces or connector contacts when handling the board.

After you remove the wrapped board from its outer shipping carton, proceed as follows:

1. Your board is packaged at the factory in an anti-static wrapper. Do not remove the anti-static wrapper until you have discharged any static electricity voltage differences between the wrapped board and the environment. Use one of the following methods:
   - Preferably, wear a grounded wrist strap. A grounded wrist strap discharges static electricity from wrapped board as soon as you hold it. Keep the wrist strap on until you have finished installing the board.
   - If you do not have a grounded wrist strap, discharge static electricity by holding the wrapped board in one hand while placing your other hand firmly on a grounded metal portion of the computer chassis. Your computer must be turned off and be plugged into a grounded receptacle or otherwise grounded. Touch the computer chassis again periodically while installing the board.
2. Remove the KCPI-PIO24 board from its anti-static wrapping material. (You may wish to store the wrapping material for future use.)
3. Inspect the board for damage. If damage is apparent, arrange to return the board to the factory. Refer to "Technical support."
4. Check the remaining contents of your package against the packing list, and report any missing items immediately.
5. If the inspection is satisfactory, proceed to "Installing and connecting the KPCI-PIO24 board."

NOTE *Install the DriverLINX software before installing the KPCI-PIO96 board.Otherwise, the device drivers will be more difficult to install.*

Installing and connecting the KCPI-PIO24 board

The following sections describe how to install and connect the KCPI-PIO24 board. The sections are ordered in the recommended installation sequence.

Installing the board

CAUTION **Ensure that the computer is turned off before installing or removing a board. Installing or removing a board while power is ON can damage your computer, the board, or both.**

Handle the board at the mounting bracket, using a grounded wrist strap. Do not touch the circuit traces or connector contacts. If you do not have a grounded wrist strap, periodically discharge static electricity by placing one hand firmly on a grounded metal portion of the computer chassis.

Use the following steps to install a KCPI-PIO24 board in a PCI expansion slot on your computer:

1. Turn power OFF to the computer, and to all external circuits if any are attached to the board.
2. Remove the computer chassis cover.
3. Select an unoccupied PCI expansion slot in the rear panel, and remove the corresponding dummy mounting plate.
4. Insert and secure the board in the selected PCI expansion slot.

Identifying the I/O connector and pin assignments

Figure 3-1 and Table 3-1 show and describe the pin assignments for the I/O connector, a standard 37-pin D type.

Figure 3-2 shows the location of the I/O connector on the board.

Figure 3-1
Pin assignments for I/O connector on the KPCI-PIO24 board

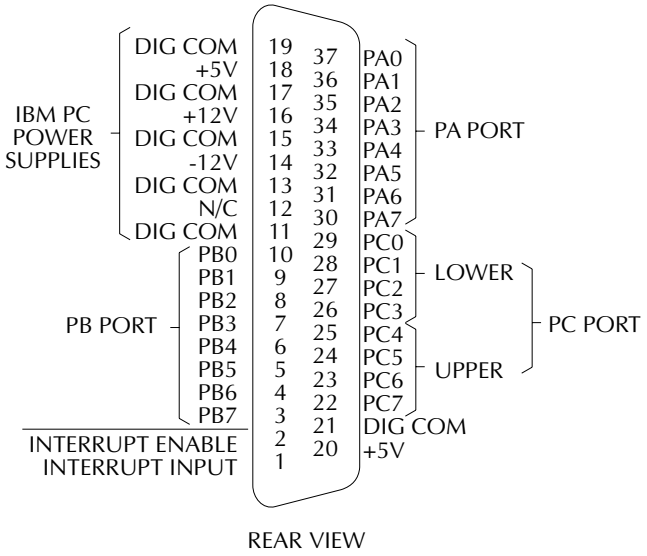
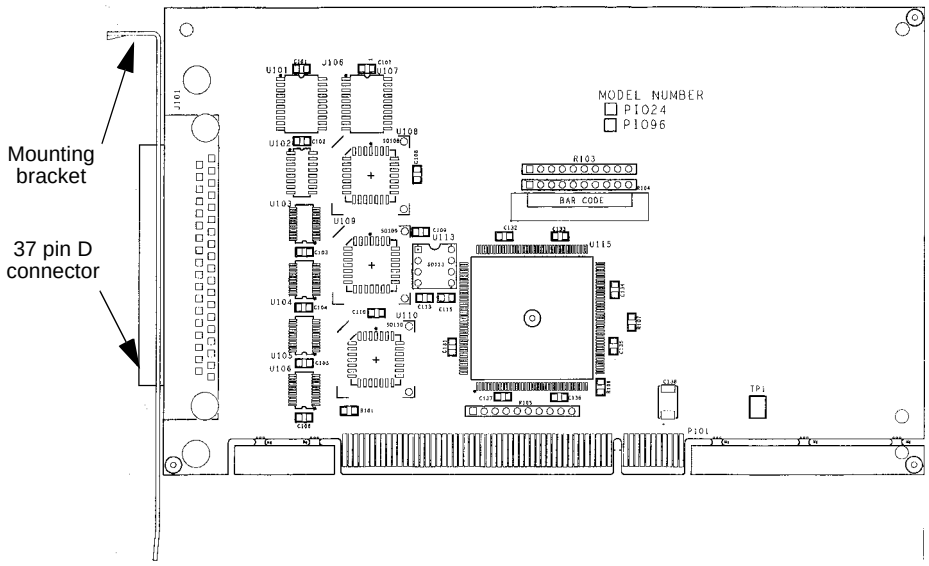


Table 3-1
Pin descriptions for KPCI-PIO24 I/O connector

Pin No.	Pin label	Description
1	INTERRUPT INPUT	External interrupt, edge triggered. By default, triggered by the rising edge of a TTL signal. Can set it to be triggered by the falling edge of a TTL signal. Refer also to "Interrupts" in section 4. Latching of input data is available through DriverLINX[1].
2	$\overline{\text{INTERRUPT ENABLE}}$	External interrupt enable, active low. To enable the interrupt at pin 1, connect pin 2 to digital common (pin 11, 13, 15, 17, 19, or 21).
3 to 10	PB0 to PB7	The eight I/O bits of port B. PB0 is the least significant bit (LSB) of port B and PB7 is the most significant bit (MSB).
11, 13, 15, 17, 19, 21	DIG COM	Digital common from the PCI bus.
12	N/C	No connection
14	-12 V	-12 V power from the PCI bus.
16	+12 V	+12 V power from the PCI bus
18, 20	+5 V	+5 V power from the PCI bus.
22 to 29	PC0 to PC7	The eight I/O bits of port C. PC0 is the least significant bit (LSB) of port C and PC7 is the most significant bit (MSB).
30 to 37	PA0 to PA7	The eight I/O bits of port A. PA0 is the least significant bit (LSB) of port A and PA7 is the most significant bit (MSB).

[1]Refer to "Advanced Digital I/O Configuration" in the DriverLINX on-line help and to "Interrupts" in section 4 of this manual. For additional information, search your DriverLINX manuals for the term "latching."

Figure 3-2
Board layout



Connecting I/O cables and interface accessories

The KPCI-PIO24 I/O connectors can be mated directly to your external circuits using a locally fabricated cable assembly. Alternatively, the connectors can be mated to your circuits via a manufactured cable assembly and interface accessories, such as screw terminal boards and relay circuits.

CAUTION **If a cable is connected to any external circuits, make sure power to all external circuits is turned OFF before connecting this cable to the KPCI-PIO24 board. Connecting a powered external cable to the board can damage the board, the external circuit, or both.**

Handle the board at the mounting bracket, using a grounded wrist strap. Do not touch the circuit traces or connector contacts. If you do not have a grounded wrist strap, periodically discharge static electricity by placing one hand firmly on a grounded metal portion of the computer chassis.

Using locally fabricated cable assemblies

To mate a locally fabricated cable to an I/O connector, install a female 37-pin "D" type mating connector (Keithley part no. SFC-37) on the cable.

Using manufactured cables and accessories

Using manufactured cables and accessories is illustrated in Figure 3-3. Each item is described in Table 3-2. For more information about these products, refer to your Keithley data acquisition or full line catalog or consult with your Keithley dealer.

Figure 3-3
Using manufactured cables and accessories

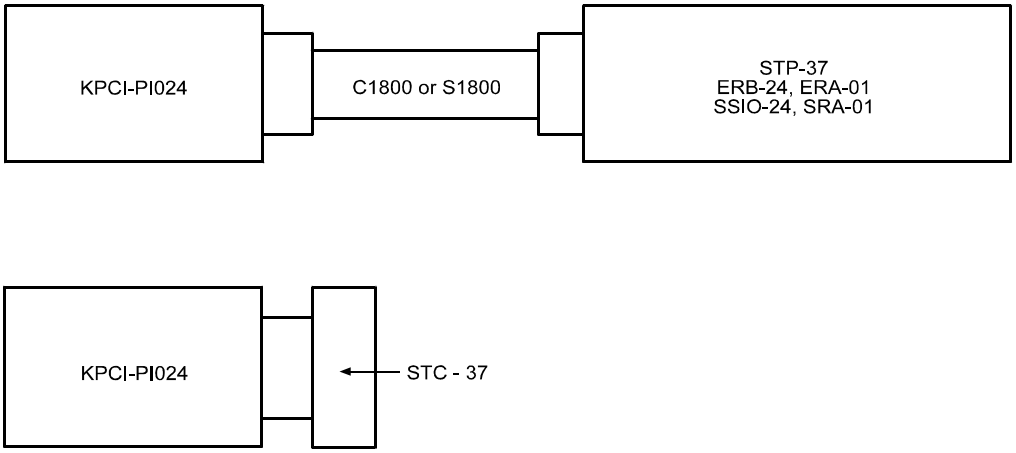


Table 3-2
Description of manufactured cables and accessories

Cable/accessory	Description
C1800	Ribbon cable, 18 in, with two 37-pin female connectors.
S1800	Shielded version of C1800.
C1800/M	Ribbon cable, 18 in, with one 37-pin female connector and one 37-pin male connector.
S1800/M	Shielded version of C1800/M.
STA-U	Universal screw terminal board in a box, with female 37 pin connector. Requires a C1800/M or S1800/M cable.
STP-37	Screw terminal panel. Requires a C1800 or S1800 cable.
STC-37	Screw terminal connector that plugs directly into the KPCI-PIO24.
ERB-24	24-channel DPDT relay output board. Requires a C1800 or S1800 cable.
ERA-01	8-channel SPDT relay output board. Requires a C1800 or S1800 cable.
SSIO-24	24-channel solid state I/O module board. Requires a C1800 or S1800 cable.
SRA-01	8-channel solid state I/O module board. Requires a C1800 or S1800 cable.

NOTE ***C****ompliance to CE Mark emission levels requires use of shielded versions of Keithley cables, S1800 and S1800/M.*

Standard C1800, C-1800/M, S1800, S-1800/M 2000 cables are 18 inches long. Longer cables are available. If you need a longer cable, refer to the accessories section of your Keithley catalog.

Connecting I/O cables to your external circuit

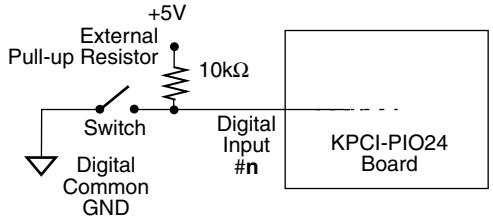
CAUTION **Ensure that both the computer and the external circuit are turned OFF before making any connections. Making connections while the computer and external circuits are powered can damage the computer, the board, and the external circuit.**

External circuits must properly match the input and output requirements of the card. For example, input signals often require pull-up resistors and elimination of contact bounce; output signals must not draw excessive current. The following section presents pull-up, de-bounce and relay drive circuits and discusses using +5 VDC power from the board for these and other applications.

Monitoring contact closure at an input

To ensure that the KPCI-PIO24 reliably monitors an open contact as an input-high condition, connect a 10 kΩ pull-up resistor between the input line and a +5 VDC source. See Figure 3-4.

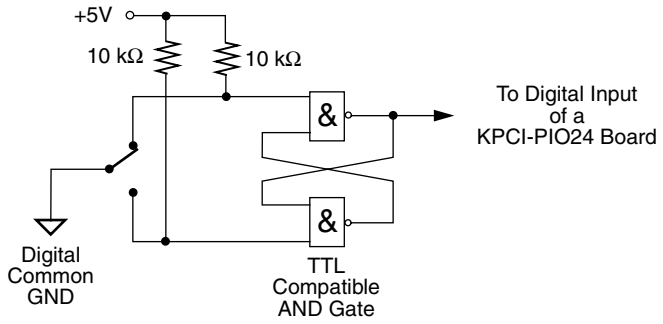
Figure 3-4
Contact-closure monitoring at a KPCI-PIO24 board input System connections



Eliminating contact bounce

The effects of contact bounce may be eliminated by programming in your application software. However, it is often desirable to eliminate contact bounce from the signal, using a de-bounce circuit between the contacts and the KPCI-PIO24 input. Figure 3-5 shows a typical de-bounce circuit that can be used with Form C contacts.

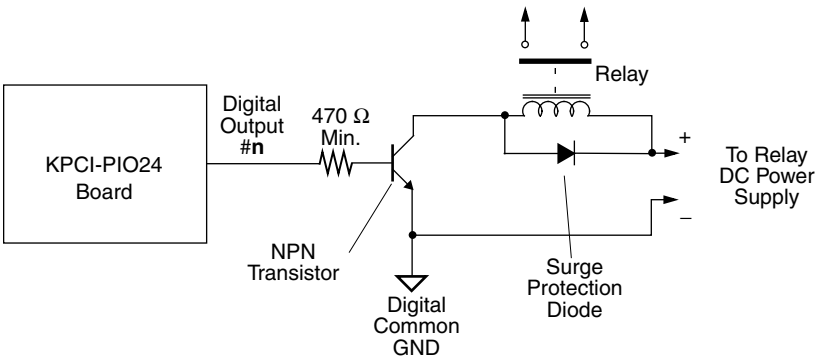
Figure 3-5
De-bounce circuit for an input of a KPCI-PIO24 board



Boosting relay drive current

Some relays require higher drive currents than standard solid-state relays. The maximum output low sink current for each I/O line of a KPCI-PIO24 board is 64mA at 5V. If your relay requires more than 64mA or more than 5V, you can boost the drive current and/or voltage for relay control using the circuit shown in Figure 3-6.

Figure 3-6
NPN transistor relay control for an output of a KPCI-PIO24 board



For drive-current requirements between 15mA and 100mA, select an NPN transistor with appropriate current capacity. The power transistor must be rated for the required supply voltage and must have a collector current rating no higher than 0.5A. If higher current is needed, substitute a Darlington NPN transistor.

Using +5 VDC from the computer power supply

CAUTION **Do not connect the +5 VDC outputs to an external +5VDC supply. This may damage the external supply, the board, and the computer.**

Do not draw more than 1.0 A, total, from the board to power external circuits. Drawing more than 1.0 A may damage the board.

The board extends power from the +5 VDC computer supply to the I/O connector (see Figure 3-1). This power is convenient for use in light external circuits, such as pull-up resistors. If you ensure that the following conditions are maintained, this power may also be used to energize external accessories:

- The total current drawn to power the board and all external circuits must not overload the computer power bus.
- The total current drawn to power all external circuits must be less than 1A.

4
Interrupts and I/O Address Mapping

Interrupts

Two externally accessible inputs allow for flexible interrupt configuration: $\overline{\text{INT_EN}}$ (external interrupt enable, active low) and INT_REQ (external interrupt request, edge triggered). The interrupt pins on the I/O connector are identified in Figure 3-1.

The external interrupt request line can be set in software to trigger on either the positive (rising) edge or the negative (falling) edge of the signal; positive edge triggering is the default upon power-up or reset. Also, when one or more ports are configured as inputs, the interrupt request line can be simultaneously programmed to latch incoming data on this edge. Refer to the KPCI-PIO24 software manual for more information on setting and configuration of the external interrupts.

The PCI bus shares a single interrupt line for all cards, INTA, which interrupts the host computer every time a transfer is occurring. This interrupt is internal to the PCI bus. It must not be confused with the external interrupt line, INT_REQ, even though INT_REQ and INTA are linked by software.

I/O address mapping

NOTE *A typical user of the KPCI-PIO24 board does not need to read this section. Register level programming of your board is neither practical nor necessary for most users. Register level interfacing with the PCI bus is more complex than with the ISA bus. PCI board addresses are mapped automatically in general memory, whereas ISA board addresses are assigned by the user to memory reserved for I/O.*

The DriverLINX driver shipped with your board provides a user-friendly Application Programming Interface (API) that supports Visual C++, Visual Basic, and Delphi programming languages under Windows 95/98 and Windows NT 4.0. You are strongly encouraged to use the capabilities of DriverLINX and ignore the rest of the information in this chapter.

However, there are circumstances in which advanced uses may desire or need to bypass DriverLINX entirely and write their own drivers. Alternatively, advanced users may wish to use DriverLINX with programming languages other than Visual C++, Visual Basic, or Delphi.

Ways to accomplish these tasks are referenced under "Setting control and data registers." The remainder of the chapter summarizes general and relative register addresses and register assignments.

General memory assignments

The PCI specification allows each card to be assigned up to five distinct memory regions. The first region, BADDR 0, is mandatory per the PCI specification, as published by the PCI Special Interest Group (PCISIG). BADDR 0 contains all information needed to identify a PCI device. BADDR 0 also contains specific operation registers for the AMCC S5933 bus controller. These operation registers hold all control and status information, as well as FIFOs, for PCI-initiated bus mastering. The other four memory regions are BADDR1, BADDR2, BADDR3, and BADDR4. These regions are left for custom designs and operate only in the target mode, also called passthrough operation (memory access through the CPU). High speed data transfer via bus mastering is unnecessary for the simple digital I/O of the KPCI-PIO24 board.

Control and data register memory assignments

The KPCI-PIO24 normally operates in the target mode and uses eight consecutive memory mapped locations at BADDR1 for its control and data ports. The base address for these locations is automatically assigned by the Plug and Play feature upon power up. Each offset from the base address is specified as a multiple of four bytes (modulo 4 addressing), because each offset specifies a four byte (32 bit) wide register. Refer to Table 4-1; the prefix '0x' in Table 4-1 designates hexadecimal.

NOTE *The term "Base" address in Table 4-1 does not have the same meaning for a PCI board, such as the KPCI-PIO24, as for an ISA board. The base address for your KPCI-PIO24 is a memory mapped address, BADDR1, that is assigned by Plug and Play. It is not a fixed, user assigned I/O address such as 0x300 or 0x310.*

Table 4-1
Data and control register addresses

	Address	Contents	I/O Function
*	Base + 0x0 offset	Port group[1] 0 data	Read/Write
	Base + 0x4 offset	Not used	N/A
	Base + 0x8 offset	Not used	N/A
	Base + 0xC offset	Not used	N/A
	Base + 0x10 offset	Control register bits for port group 0	Write only
	Base + 0x14 offset	Not used	N/A
	Base + 0x18 offset	Not used	N/A
	Base + 0x1C offset	Not used	N/A

[1]Contains a PA port, a PB port and a PC port, as in the emulated 8255 chip.

*** Data Register Format, 32 Bit**

4 High Bits of Port C	Not Used	Not Used	4 Low Bits of Port C	8 Bits of Port B	8 Bits of Port A

MSB LSB

The control register bit assignments for each port are listed in Table 4-2.

Table 4-2
Control register bit assignments for each port group

Bit Number	Function	Variable name for bit	Configuration for this port	
			When bit value = 0[1]	When bit value = 1
Bit 7	Transfer method bit 1	ACCESSMODE1	See Table 4-3	See Table 4-3
Bit 6	Transfer method bit 0	ACCESSMODE2	See Table 4-3	See Table 4-3
Bit 5	External interrupt polarity	INT_POLARITY	See footnote[2]	See footnote[3]
Bit 4	Nonlatching/latching ports	BUFF_LATCH	See footnote[4]	See footnote[5]
Bit 3	I/O direction for PC port, upper half	PCHI0_DIR	Input	Output
Bit 2	I/O direction for PC port, lower half	PCLO0_DIR	Input	Output
Bit 1	I/O direction for PB port	PB0_DIR	Input	Output
Bit 0	I/O direction for PA port	PA0_DIR	Input	Output

[1]All bit values default to '0' upon computer reset or power-up.

[2]When INT_POLARITY = 0, an interrupt is triggered by the positive (rising) edge of the external interrupt signal at pin 1 of the I/O connector.This is the default upon reset or power-up.

[3]When INT_POLARITY = 1, an interrupt is triggered by the negative (falling) edge of the interrupt signal.

[4]When BUFF_LATCH = 0, ports configured for input act as transparent buffers; data is read from the ports in real time. This is the default upon reset or power-up.

[5]When BUFF_LATCH = 1, ports configured for input act as latches; data is latched when an external interrupt signal is received, at pin 1 of the I/O connector. The polarity is defined by INT_POLARITY.

Three different data transfer modes can be specified via appropriate combinations of bits 6 and 7. Refer to Table 4-3.

NOTE *Some of the terms that follow may not be fully understood without referring to the AMCC S5933 PCI Bus Controller manual.*

Table 4-3
Data transfer mode selection

Bit combinations		Data transfer mode	Notes
Bit 7 ACCESSMODE1	**Bit 6 ACCESSMODE0**		
0	0	Data is accessed via the target (pass-through) mode of the AMCC S5933 bus controller. No bus mastering.	Default upon reset or power-up
0	1	Data is accessed via the target (pass-through) mode of the AMCC S5933 bus controller. No bus mastering	
1	0	Data is accessed via the FIFO of the AMCC S5933 bus controller. The FIFO is accessible by the host as programmed I/O or via bus mastering.	All ports, of port group 0, must be configured as **inputs**
1	1	Data is accessed via the FIFO of the AMCC S5933 bus controller. The FIFO is accessible by the host as programmed I/O or via bus mastering.	All ports, of port group 0, must be configured as **outputs**

When bus mastering is not invoked:

- An interrupt is always generated on the edge of every external interrupt request signal, as defined by the INT_POLARITY bit.
- An interrupt can be used to interrupt the host computer during the target mode (pass-through) access or be used to service the FIFOs for programmed I/O accesses.

When bus mastering is invoked:

- An interrupt is not generated on the edge of an interrupt request signal.
- Only one PCI board can take control of the PCI bus at any given time during a bus-mastered data transfer, and only one interrupt is permitted during this transfer. Therefore, an interrupt cannot be generated at an arbitrary time. An interrupt is generated only after a predefined number of data points have been transferred.

Setting control and data registers

The control registers must first be set by software statements to set each group of A, B, and C ports for the desired direction (input or output). This is performed by writing to the control registers located at the Base Address + 0x10, Base Address + 0x14, Base Address + 0x18, and Base Address + 0x1C. In most applications all 8 bits in each port will be set as either input or output.

Thereafter, data can be input to or output from the data registers. Data registers configured as outputs are set by writing ones and zeros to these registers with software statements. Data registers configured as inputs are set by applying logical high and low signals to the input terminals; the set values in these registers are retrieved by software statements.

Software manipulation of data registers for an ISA board, via I/O port calls, is straightforward. However, software manipulation of data registers for a PCI board, such as the KPCI-PIO24, is more involved. As mentioned in the chapter introduction, DriverLINX eliminates the need for user interaction with control and data registers. However, control and data registers can be manipulated in the following special situations:

- You are an advanced user needing to use the KPCI-PIO24 with an operating system other than Microsoft Windows 95/98 or Windows NT 4.0 or greater. In this situation, you must write a new driver, bypassing DriverLINX entirely. This task requires an in-depth knowledge both of the AMCC S5933 PCI Bus Controller and your development operating system.
- You wish to program in an ActiveX hosting language other than Visual C++, Visual Basic, or Delphi. In this situation, you may need to use the "Direct I/O ActiveX Automation Object" that comes with DriverLINX. The Direct I/O ActiveX Automation Object allows you to set the control and data registers directly and bypass the DriverLINX API, yet avoids the full complexities of PCI bus interfacing and the AMCC S5933 PCI Bus Controller. Refer to your DriverLINX manual for more information.
- You wish to reuse an existing program that makes port I/O calls to an ISA-bus digital I/O board, such as the PIO-96 or PIO-24. In this situation, you can reuse your existing program with the KPCI-PIO24, in Windows 95/98 only, via the Hardware I/O Emulation driver included on your DriverLINX CD ROM. The Hardware I/O Emulation driver traps the port I/O calls and applies them properly to the KPCI-PIO24 board. Refer to your DriverLINX manual for more information.

5
Troubleshooting

If your KPCI-PIO24 board is not operating properly, use the information in this section to isolate the problem before calling Keithley Applications Engineering. If you then need to contact an applications engineer, refer to "Technical support."

Identifying symptoms and possible causes

Try to isolate the problem using Table 5-1, which lists general symptoms and possible solutions for KPCI-PIO24 board problems.

Table 5-1
Basic troubleshooting information

Symptom	Possible cause	Possible cause validation/solution
Computer does not boot when board is installed	Resource conflict. KPCI-PIO series board is conflicting with other boards in the system.	1. Validate the cause of the conflict. Temporarily unplug boards —especially ISA boards[1]—one at a time, and try booting the computer. Repeat until a boot is attained. 2. Try resolving conflicts by reinstalling one PCI board at a time and rebooting after each reinstallation.[2] However, you may ultimately need to change ISA board resource allocations, such as base address or interrupt assignments.
	Board not seated properly.	Check the installation of the board.
	The power supply of the host computer is too small to handle all the system resources.	Check the needs of all system resources and obtain a larger power supply.
After board & software are installed, mouse control is lost or system freezes.	An interrupt conflict occured.	Unplug the board to regain mouse control. Look closely at the COM ports and at the interrupts of other devices.
Board does not respond to the PIO Test Panel.	DriverLINX is not installed properly.	Check the Windows® Device Manager and follow the installation troubleshooting instructions in the DriverLINX on-line help.
	The board is incorrectly aligned in the expansion slot.	Check the board for proper seating.
	The board is damaged.	Contact Keithley Applications Engineering.
Data appears to be invalid.	An open connection exists.	Check screw terminal wiring.
	Transducer is not connected to channel being read.	Check the transducer connections.
	One or more external circuits are not TTL compatible	Check external circuit schematics. Test external circuits with a logic probe.
Intermittent operation.	Vibrations or loose connections exist.	Cushion source of vibration and tighten connections.
	The board is overheating.	Check environmental and ambient temperature. See your computer documentation.
	Electrical noise exists.	Provide better shielding or reroute unshielded wiring.
System lockup during operation.	A timing error occurred.	Restart your computer. Then analyze your program by debugging and narrowing the list of possible failure locations.

[1]Plug and Play cannot tell if an ISA board already uses an address it assigns to a PCI board.
[2]Plug and Play may then assign different, nonconflicting addresses to the PCI boards.

If your board is not operating properly after using the information in Table 5-1, continue with the next section to further isolate the problem.

Systematic problem isolation

General problem isolation procedure

If you were unable to isolate the problem using Table 5-1, then follow Figure 5-1 and the accompanying written procedure. The flowchart in Figure 5-1 summarizes how to systematically check and eliminate some problem causes. The corresponding written procedure amplifies the flowchart steps with more detail.

CAUTION **Always turn OFF your computer and any external circuits connected to the KPCI-PIO24 board before removing or replacing the board. Removing or replacing a board with the power ON can damage the board, the computer, the external circuit, or all three.**

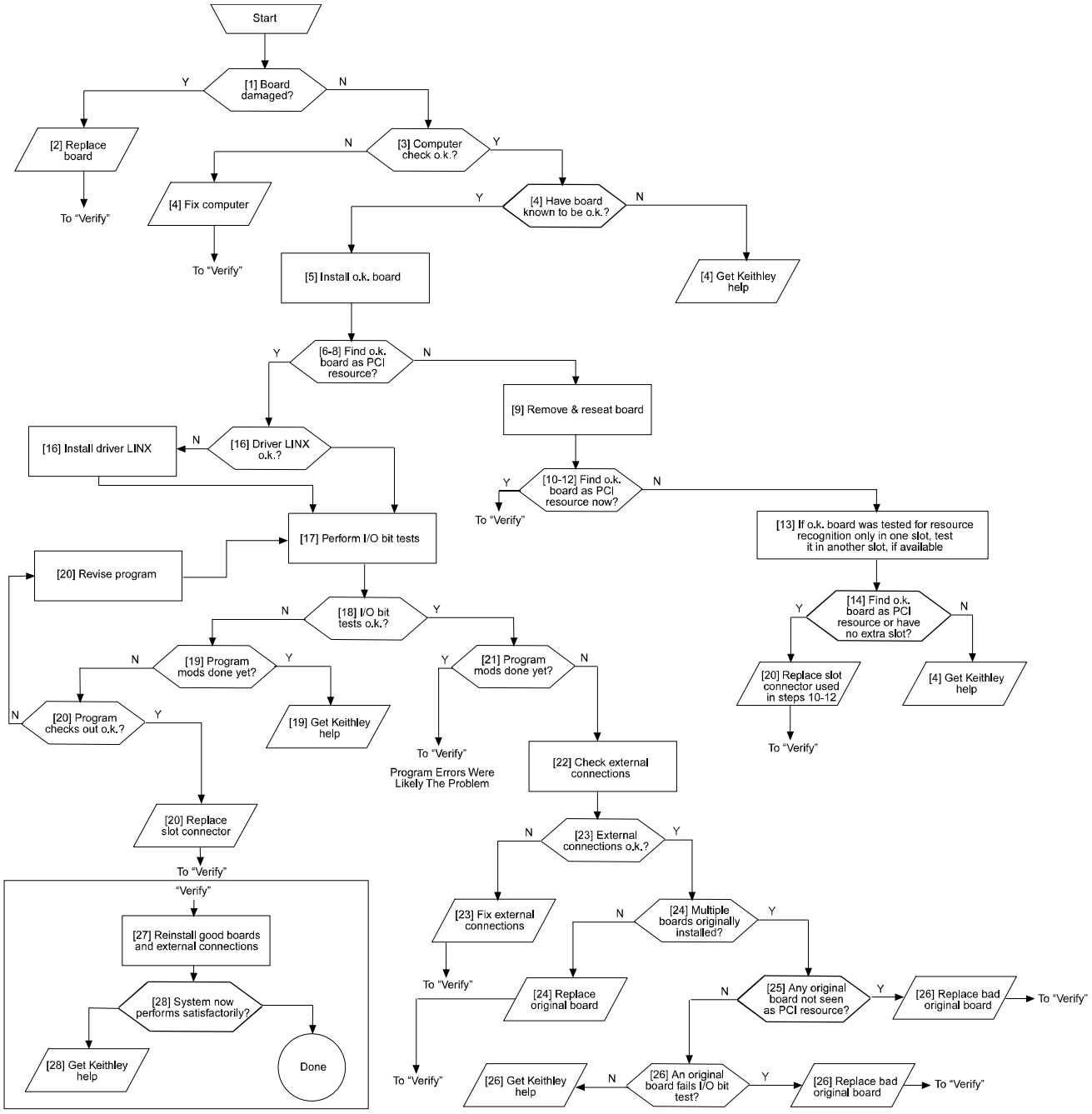
Handle the board at the mounting bracket, using a grounded wrist strap. Do not touch the circuit traces or connector contacts. If you do not have a grounded wrist strap, periodically discharge static electricity by placing one hand firmly on a grounded metal portion of the computer chassis.

NOTE *In the following procedure, the term "board" always refers to a KPCI-PIO24 board. The procedure never directs you to install or remove any type of PCI board other than a KPCI-PIO24 board.*

In Figure 5-1 the number in brackets in each flowchart block (e.g. [21]) refers to the corresponding step number in the verbal procedure. If multiple blocks in the flowchart have the same number, each of those blocks is part of a single verbal step. Conversely, if there is a range of numbers in the brackets (e.g. [4, 5, 6]), the block summarizes multiple verbal steps.

The logic in this procedure assumes that the problem has only one cause. Therefore, once a cause is found and corrected, the reader is instructed to reassemble the system and verify proper operation.

Figure 5-1
Problem isolation flowchart



To further isolate the problem to the KPCI-PIO24 board or to the host computer, use the following steps:

1. Check if board damage is seen on inspection. Proceed as follows:

NOTE *If more than one KPCI-PIO24 board is installed in your computer, disconnect, remove, and check all KPCI-PIO24 boards.*

   a. Turn power OFF to the host computer.
   b. Turn power OFF to all external circuits and accessories connected to the KPCI-PIO24 board.
   c. Unplug all I/O cables from all external circuits or unplug I/O cables from accessory boards connected to external circuits.
   d. Remove the KPCI-PIO24 board from the computer.
   e. Visually inspect the KPCI-PIO24 board for damage.

2. Based on the results of step 1, do the following:
   - If the board is not obviously damaged, skip to step 3 and check for host computer malfunction.
   - If a board is obviously damaged on inspection, repair or replace the board. Refer to "Technical support" for information on returning the board for repair or replacement. Skip to step 27.

3. Check if the computer functions satisfactorily by itself. Proceed as follows:
   a. Remove the KPCI-PIO24 board from the host computer.

NOTE *If more than one KPCI-PIO24 board is installed in your computer, remove all KPCI-PIO24 boards before testing the host computer.*

   b. Turn ON power to the host computer.
   c. Perform any necessary diagnostics to the computer hardware and operating system.

4. Based on the results of step 3, do one of the following:
   - If the computer functions satisfactorily, the problem must lie elsewhere; do the following steps:
     a. If you have another KPCI-24 board that you know is OK, i.e. works properly, then proceed to step 5.
     b. If you do not have another KPCI-24 board that you know is OK, i.e. works properly, read the instructions in "Technical support." Then contact Keithley for help in isolating the cause of your problem.
   - If the computer does not function satisfactorily, do the following steps:
     a. Diagnose and fix the computer malfunction.
     b. Assume that fixing the computer malfunction has solved your problem, and skip to step 27.

5. Install a board known to be OK, as follows:
   a. Turn OFF power to the host computer.
   b. Install a KPCI-PIO24 board that you know is OK, i.e. fully functional. Refer to Section 3, "Installation."

NOTE *Do not make any I/O connections at this point.*

6. Check if the computer finds the OK board to be a PCI resource.
   If an OK board is properly installed electrically and the PCI expansion slot is functional, then Windows 95 Plug and Play should configure the board as a PCI resource. Proceed as follows:
   a. Determine the number of the expansion slot used by the OK KPCI-PIO24 board. Refer to the slot numbering information in your motherboard manual.
   b. Turn ON the power to reboot the computer and, during boot, determine whether your operating system has identified the board as a PCI resource. During boot, the Windows 95 Plug and Play should list the PCI resources found. The board should be listed, likely as an unidentified peripheral, with same slot number as identified in step 6a.
7. If you had originally installed additional KPCI-PIO24 boards in other PCI slots, then repeat steps 5 and 6 with the OK board in each of these other slots.
8. Based on the results of steps 5 through 7, do one of the following:
   a. If the board is recognized as a PCI component in all slots tested, then there may be software issues. Skip to step 16.
   b. If the OK board is not recognized as a PCI component in a slot(s), then the PCI slot connector(s) is suspect. Continue with step 9.
9. Make sure that slot and board contacts have wiped adequately and are properly mated. Do the following:
   a. Turn OFF power to the host computer.
   b. Remove and reseat the board a few times in the PCI slot connector. This creates a wiping action to improve the probability of good contact.
   c. Make sure that the board is firmly seated in the PCI slot connector.
   d. Turn ON power to the host computer.
10. Check if the computer now finds the OK board to be a PCI resource.
    Proceed as follows (refer back to similar step 6 for more description):
    a. Determine the number of the expansion slot used by the OK board.
    b. Boot the computer and, during boot, determine whether your operating system has identified the OK board as a PCI resource.
11. If KPCI-PIO24 boards were originally installed in other PCI slots, then repeat steps 9 and 10 with the OK board in each of these slots.
12. Based on the results of steps 9 through 11, do one of the following:
    - If the board is recognized as a PCI resource in all slots tested, then the cause of the problem was probably high contact resistance, which apparently has been corrected by the wiping action. Skip to step 27.
    - If the OK board is not identified as a PCI resource in all slots tested, then any slot in which it is not identified is suspect. Continue with step 13.
13. Based on the history of steps 6 through 12, do one of the following actions, to further determine whether a bad slot connector is causing your problem:
    - If, at this point, you've only tested the OK board in one slot on this computer AND you have another slot available, test it in another slot now. Proceed as follows:
      a. Turn OFF power to the host computer.
      b. Move the OK KPCI-PIO24 board to another available slot.
      c. Determine the number of the expansion slot used by the OK board.
      d. Turn ON power to the host computer.
      e. During boot, determine whether your operating system has identified the board as a PCI resource. (Refer to step 6 for more information.)
      f. Continue with step 14.

- If, at this point, you've tested the OK board in more than one slot on this computer, continue with step 14.

14. Based on the history of steps 6 through 13, do one of the following:
    - If, at any point in this procedure, the OK board was identified as a PCI resource in at least one slot on the host computer, then any slot in which it did not work is likely defective. Continue with step 15.
    - If you only had one slot in which to install the OK board, assume that this slot is defective. Continue with step 15.
    - However, if you have installed the OK board in more than one slot and the board has not been identified as a PCI resource in at least one slot, then the cause of your problem may be outside the scope of these diagnostics: two or more slots are assumed unlikely to be defective in the same computer. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.
15. Replace the defective slot connector, as follows:
    a. Turn OFF the computer.
    b. Remove the OK board.
    c. Have a qualified service person replace the defective PCI slot connector.
    d. Skip to step 27.
16. Continuing from step 8, verify that DriverLINX is installed properly:
    - If DriverLINX is installed properly, continue with step 17.
    - If DriverLINX is not installed properly, do the following:
        a. Install it now, referring to the DriverLINX installation instructions. Make sure that DriverLINX installs smoothly and completely.
        b. Continue with step 17.
17. Perform I/O bit tests to determine whether you can write and read all I/O bits to and from the OK board: the I/O loop-back test and the output set test. Perform either or both of these tests, outlined separately under the headings "I/O loop-back test" and "Output set test." However, only the I/O loop-back test is conclusive and is therefore preferred.
18. Based on the results of step 17, do one of the following:
    - If you can write and read all I/O bits to and from the OK board, skip to step 21.
    - If you cannot write and read all I/O bits to and from the OK board, there may be data acquisition program errors or defective I/O slot contacts in the slot; continue with step 19.
19. If you cannot write and read all I/O bits to and from the OK board do the following:
    - If you have arrived at step 19 before making corrections, there may be data acquisition program errors; continue with step 20.
    - If you have arrived again at step 19 after apparently correcting all program errors in the data acquisition program, the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.
20. Check if all data acquisition program lines are OK.

    Check the program documentation or use a debugger to look for programming errors that may be causing the problem.
    - If no programming errors are found, then some of the slot connector contacts corresponding to the I/O bits are likely defective, given that the board is known to be OK. Do the following:
        a. Turn OFF the computer.
        b. Remove the OK board.

c. Have a qualified service person replace the defective PCI slot connector.

d. Skip to step 27.

- If programming errors are found, do the following:

a. Debug and fix all known data acquisition program errors.

b. Repeat steps 17 and 18.

21. Continuing from steps 17 and 18, if you can write and read all I/O bits to and from the OK board, do the following:
    - If you have arrived at step 21 after program corrections have been made, and you can now write and read all I/O bits to and from the OK board, then the problem has apparently been resolved. Skip to step 27.
    - If you have arrived at step 21 without making data acquisition program corrections and can write and read all I/O bits to and from the OK board, then faulty external I/O connections may have caused your problem. Continue with step 22.
22. Check each external I/O connection, one at a time, for short circuits and open circuits. If KPCI-PIO24 boards were installed in more than one PCI slot, check the I/O connections for all boards.
23. Based on the results of step 22, do the following:
    - If any external I/O connections are found to be faulty, assume that the problem was caused by the faulty connections, then proceed as follows:

      a. Correct the faulty external connections.

      b. Skip to step 27.
    - If all external I/O connections are found to be normal, then, by process of elimination, the KPCI-PIO24 board(s) originally installed in the computer is likely the cause of the problem. Continue with step 24.
24. Replace the faulty board. Do one of the following:
    - If only one KPCI-PIO24 board was installed when the problem occurred, proceed as follows:

      a. Leave the OK board in the expansion slot as a replacement. To repair or replace the faulty board, contact Keithley as described in "Technical support."

      b. Skip to step 27.
    - If more than one board was installed when the problem occurred, determine which one is faulty, starting with step 25.
25. Check if one of the original boards is not detected as a PCI resource. Proceed as follows

    a. Turn OFF the computer.

    b. Remove the OK board.

    c. Install one of the original boards in a slot known to be satisfactory.

    d. Turn ON the computer and, during boot, determine whether your operating system has identified the board as a PCI resource. See step 6 for more information.

    e. Based on the results of step 25d, do one of the following:
       - If, in step 25d, the board is not recognized as a PCI resource, you have located the faulty board; replace it with the OK board. (To repair the faulty board or obtain a new one, contact Keithley as described in "Technical support.") Then skip to step 27.
       - If, in step 25d, the board is recognized as a PCI resource, repeat steps 25a through 25e for each board. If you have reached this point after trying multiple boards, and each board has been recognized as a PCI resource, then continue with step 26.
26. Determine which board has faulty I/O. If the faulty board survived the PCI resource test in step 25, it should fail the I/O test.

a. If an original board remains installed following step 25, then skip to step 26e.
b. Turn OFF the computer.
c. Install one of the original boards in a slot known to be satisfactory.
d. Turn ON the computer.
e. Perform the I/O tests outlined in the "I/O bit tests" section. Then return to this step (26e).
f. Based on the results of step 26e, do one of the following:
   - If, in step 26e, you cannot write and read all I/O bits to and from the board, you have located the faulty board; replace it with the OK board. (To repair the faulty board or obtain a new one, contact Keithley as described in "Technical support.") Then skip to step 27.
   - If, in step 25e, you can write and read all I/O bits to and from the board, repeat steps 25b through 25e for each board until you find a faulty board. Replace the faulty board with the OK board. (To repair the faulty board or obtain a new one, contact Keithley as described in "Technical support.") Then continue with step 27.
   - However, if you have reached this point after trying all boards, and the I/O on each board has been found satisfactory, then the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.

27. Assuming the problem has been resolved, do the following:
    a. Turn OFF the computer.
    b. Install the good KPCI-PIO24 boards in good slots.
    c. Reconnect all external circuits as discussed in Section 3, "Installation."
    d. Turn ON the computer.
    e. Verify that the system now performs satisfactorily.
28. Based on the results of step 27e, do one of the following:
    - If the system now performs satisfactorily, you have successfully isolated and corrected the problem.
    - If the system still does not perform satisfactorily, then the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.

I/O bit tests

The I/O bit tests check whether the input and output functions of the board are operating properly. They also act as backup tests for a defective slot connector. Of the two tests outlined below, only the I/O loop-back test is conclusive and is therefore preferred.

These tests are intended to be used when requested in the "General problem isolation procedure." However, they may also be used for general performance checks.

CAUTION **The tests outlined in the next two sections involve handling of the KPCI-PIO24 circuit board. Handle the board at the mounting bracket, using a grounded wrist strap. Do not touch the circuit traces or connector contacts. If you do not have a grounded wrist strap, periodically discharge static electricity by placing one hand firmly on a grounded metal portion of the computer chassis.**

Ensure that the computer is turned OFF before installing or removing a board. Installing or removing a board while power is ON can damage your computer, the board, or both.

I/O loop-back test

The I/O loop-back test checks input and output bit performance.

You prepare a specially wired loop-back connector that connects the bits of port A to the corresponding bits of ports B and C. These connections are summarized in Table 5-2.

Table 5-2
Loop-back connection summary

Connect these bits configured as an output	PA0 ↓	PA1 ↓	PA2 ↓	PA3 ↓	PA4 ↓	PA5 ↓	PA6 ↓	PA7 ↓
to these bits configured as inputs	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
	PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7

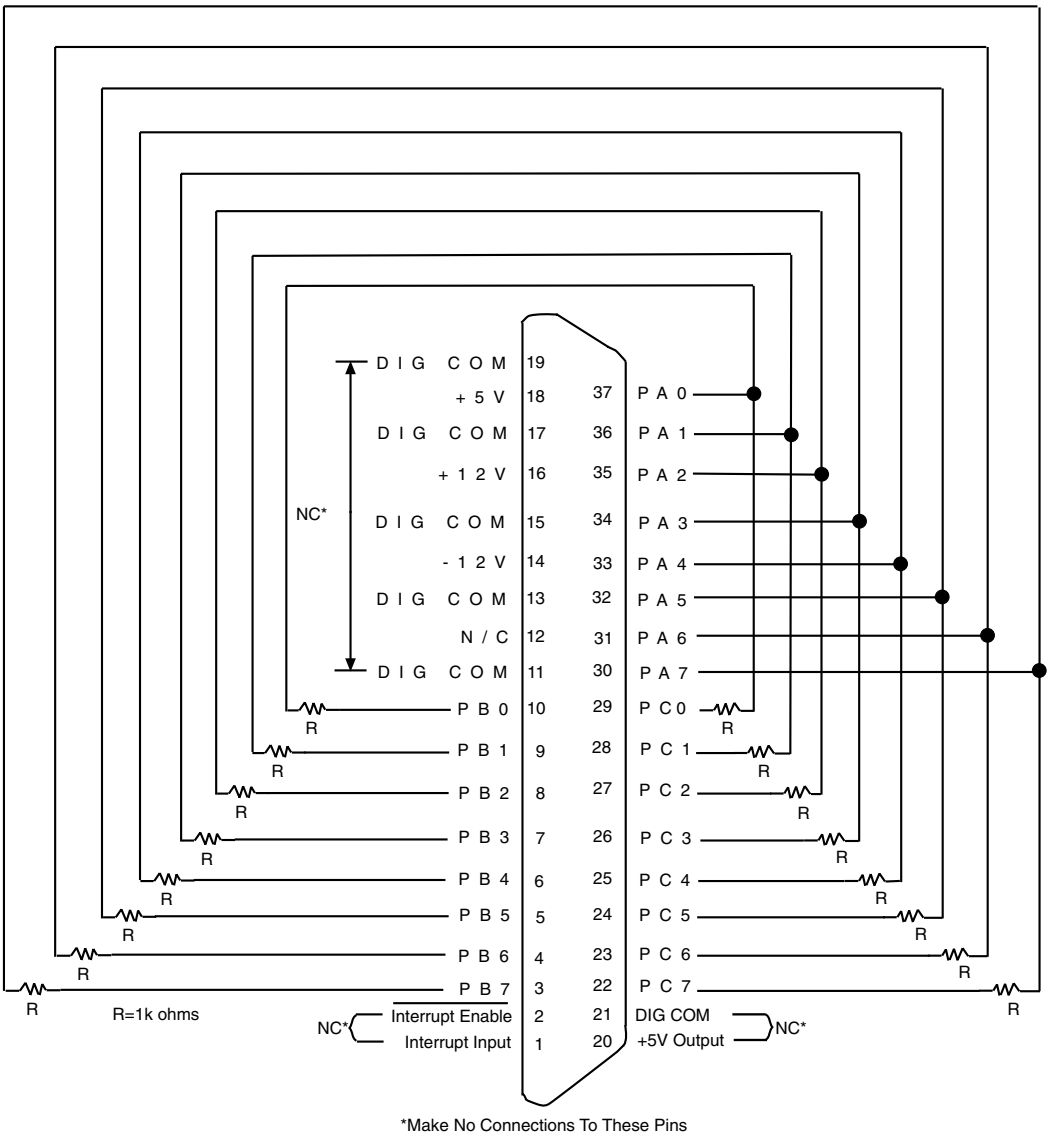
You insert this connector into the KPCI-PIO24 I/O connector. Then, you use a DriverLINX graphical interface to configure the bits of port A as outputs and ports B and C as inputs. Thereafter, you use this same DriverLINX graphical interface to set two different bit patterns at port A and to check in each case for corresponding bit patterns at ports B and C.

The card is performing satisfactorily if all 24 bits respond appropriately.

Perform the loop-back test as follows:

1. Prepare a loop-back test connector, using a female 37-pin 'D' connector that mates with the I/O connector on your board. This can be purchased as Keithley part no. SFC-37. Wire the connector as shown in Figure 5-2.

Figure 5-2
Mating connector wiring for loop-back test



NOTE *Resistors in the loops are specified for safety. During the loop-back procedure, some of the interconnected bits could temporarily or inadvertently be configured both as outputs, and the board could be easily damaged. These 1K ohm resistors limit the currents between bits to below 15 mA, which is within the source and sink current specifications for the board. If you wish to use a different resistance value, the substitute resistance value must be at least 700 ohms.*

2. Turn OFF the host computer.
3. Insert the loop-back test connector, prepared in step 1, into the board connector.
4. Turn ON the host computer and boot Windows 95, 98, or NT.
5. Click the Windows **Start** tab.
6. Start the PIO Control Panel as follows:

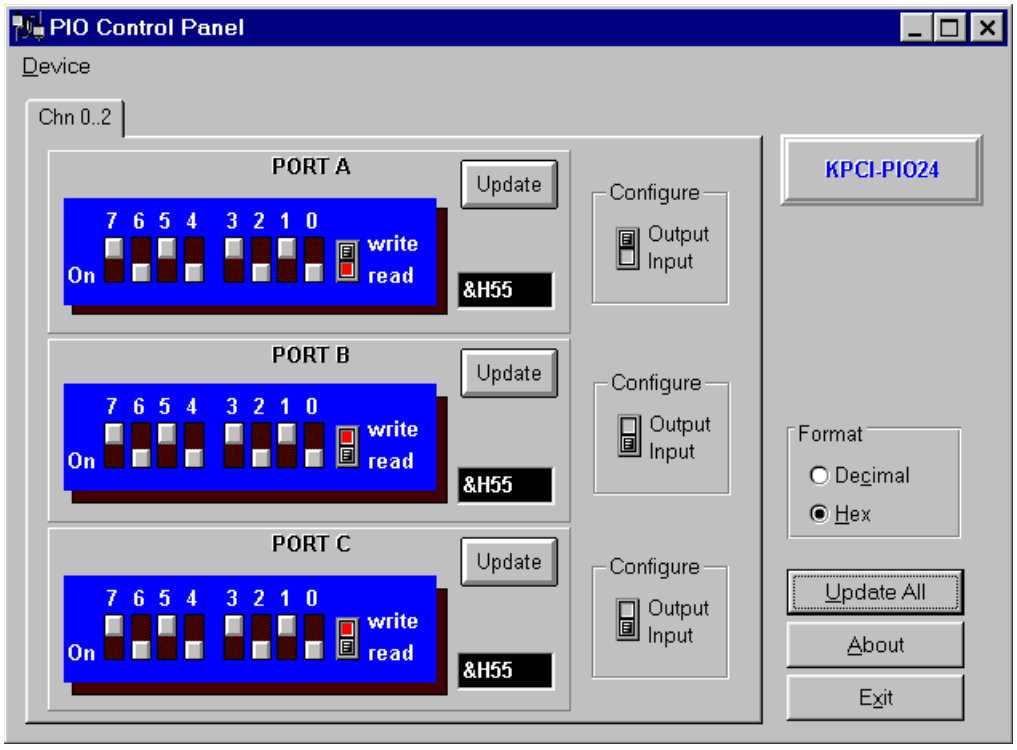
a. In the **Start** menu, click **Programs**.

b. Find the **DriverLINX ⏵ Test Panels** folder, under which you should find the **PIO Panel** entry.

c. Click on the **PIO Panel** entry.

The **PIO Control Panel** should appear. See the example in Figure 5-3.

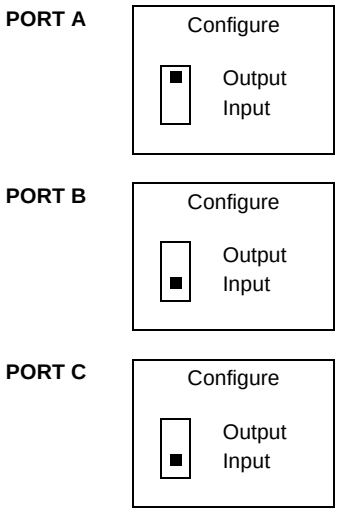
Figure 5-3
IO Control Panel example



NOTE *In following steps 7 through 9, graphical slide switches on the PIO Control Panel are used for all settings. Each click on the button of a slide switch toggles the button up or down.*

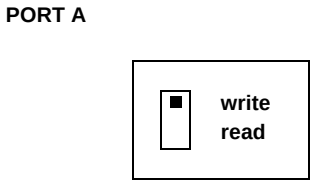
7. Using the 'Configure' switches on the PIO Control Panel, configure ports A, B, and C for input or output as shown in Figure 5-4.

Figure 5-4
Setting port input and output 'Configure' switches



8. Using the port A 'write/read' switch on the PIO Control Panel, set port A to 'write' as shown in Figure 5-5.

Figure 5-5
Port A 'write/read' switch setting

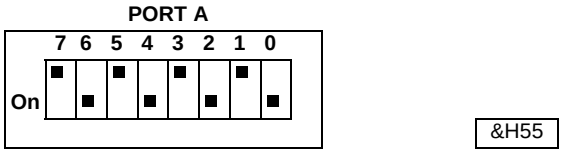


NOTE *A port configured for output, such as port A in this case, can be set for either read or write mode. In write mode, you may toggle bit settings high or low by clicking the DIP switches. In read mode, however, DIP switches only monitor the bit settings currently in the I O register; you cannot change bit settings.*

A port configured for input, such as port B or C in this case, can only be used in the read mode. DriverLINX selects the read mode automatically when the port is configured for input.

9. Using the DIP switches on the PIO Control Panel, set port A to bit pattern 1, shown in Figure 5-6. Bit pattern 1 corresponds to a byte value of 55 in hexadecimal.

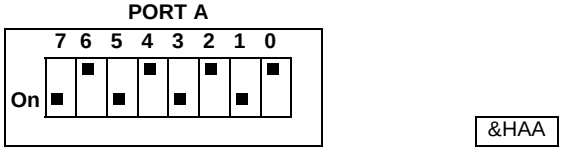
Figure 5-6
Port A output settings, bit pattern 1



NOTE *Note that the bit is ON when the switch button is DOWN.*

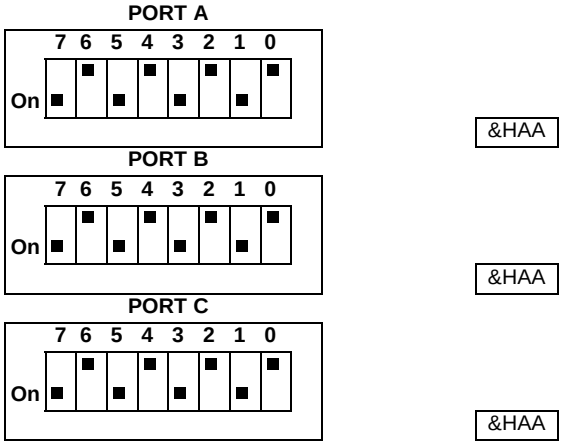
10. Click the 'Update All' button on the PIO Control Panel.
11. Observe the PIO Control Panel DIP switches for ports B and C, which in this case monitor bit patterns instead of set them. The bit patterns for ports A, B, and C should all be the same, because the output bits of port A are connected to the corresponding input bits of ports B and C. The PIO Control Panel example, Figure 5-3, shows the results of a successful loop-back test for bit pattern 1.
    - If the bit patterns for ports A, B, and C do not agree, the board is not functioning properly. Stop here, and return to the step in the "General problem isolation procedure" where you were directed to do I/O bit tests (step 17 or step 26e in the "General problem isolation procedure").
    - If the bit patterns for ports A, B, and C do all agree, continue with step 12.
12. Using the DIP switch on the PIO Control Panel, set port A to the bit pattern 2, as shown in Figure 5-7. Bit pattern 2 corresponds to a byte value of AA in hexadecimal.

Figure 5-7
Port A output settings, bit pattern 2



13. Click the 'Update All' button on the PIO Control Panel.
14. Again, observe the PIO Control Panel DIP switches for ports B and C. The bit patterns for ports A, B, and C should again all be the same, as illustrated in Figure 5-8.

Figure 5-8
Correct bit patterns when port A is set to bit pattern 2.



15. Based on the observations in step 14, do the following:
    - If the bit patterns for ports A, B, and C do not all agree, the board is not functioning properly. Stop here, and return to the step in the "General problem isolation procedure" where you were directed to do I/O bit tests (step 17 or step 26e in the "General problem isolation procedure").
    - If the bit patterns for ports A, B, and C do all agree, the board is functioning properly. Stop here, and return to the step in the "General problem isolation procedure" where you were directed to do I/O bit tests (step 17 or 26e in the "General problem isolation procedure"). Or, optionally, now perform the output set test, as discussed in the next section, if you have not already done so.

Output set test

The output set test checks whether logic levels measured at all KPCI-PIO24 output pins agree with output bit patterns set by software, using a DriverLINX graphical interface.

NOTE *This test is performed without user circuits being connected to the outputs.*

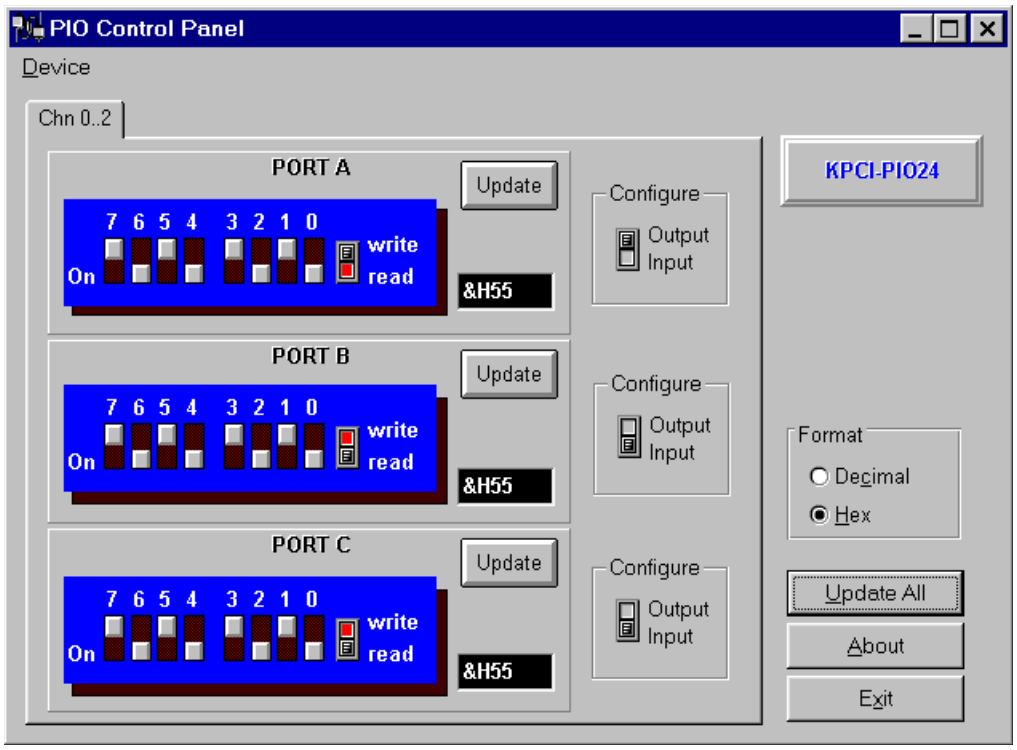
Perform the output set test as follows:

1. Ready the following equipment:
    - A digital voltmeter (DVM) or a digital multimeter (DMM) set to measure voltages, or a logic probe capable of reading TTL logic levels.
    - A means to reliably and safely connect the DMM/DVM or logic probe input to each I/O pin. The following alternatives are suggested:
        a. A screw terminal-female connector combination, Keithley part number STC-37, that plugs directly into the I/O connector on your board. Refer to your Keithley catalog for more information.
        b. A cable assembly and terminal accessory (refer to "Using manufactured cables and accessories" in Section 3).
        c. A female 37-pin 'D' connector that mates with I/O connector on your board and is wired such that the meter or logic probe can be clipped to exposed conductors. An appropriate connector can be purchased as Keithley part no. SFC-37.

2. Turn OFF the host computer.
3. Insert the test connector or cable assembly/terminal accessory into the board connector.
4. Turn ON the host computer and boot Windows 95, 98 or NT.
5. Click the Windows **Start** tab.
6. Start the PIO Control Panel as follows:
   a. In the **Start** menu, click **Programs**.
   b. Find the **DriverLINX ▸ Test Panels** folder, under which you should find the **PIO Panel** entry.
   c. Click on the **PIO Panel** entry.

   The **PIO Control Panel** should appear. See the example in Figure 5-9.

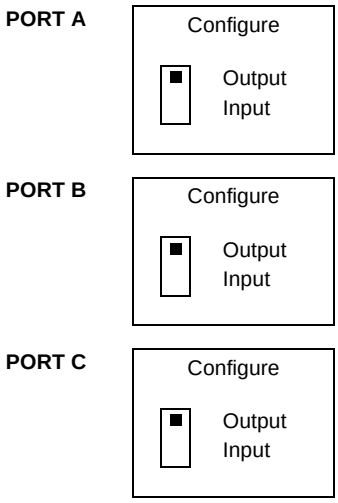
Figure 5-9
PIO Control Panel example



NOTE *In the following steps 7 through 10, graphical slide switches on the PIO Control Panel are used for all settings. Each click on the button of a slide switch toggles the button up or down.*

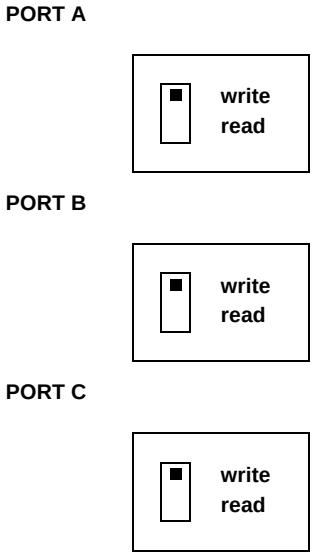
7. Using the 'Configure' switches on the PIO Control Panel, configure ports A, B, and C for output as shown in Figure 5-10.

Figure 5-10
Setting port 'Configure' switches



8. Using the port 'write/read' switches on the PIO Control Panel, set ports A, B and C to 'write' as shown in Figure 5-11.

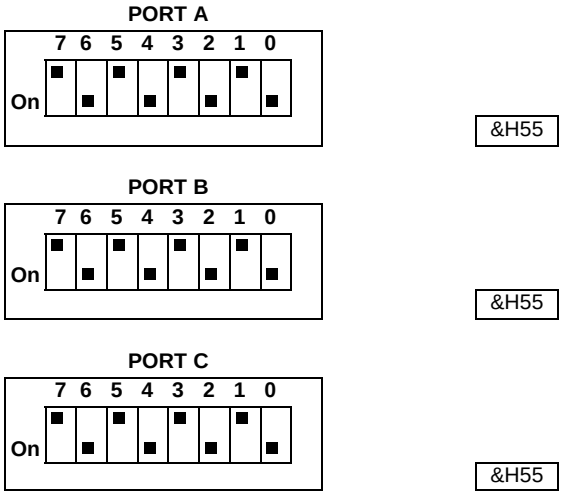
Figure 5-11
Port 'write/read' switch settings



NOTE *A port configured for output, such as port A in this case, can be set for either read or write mode. In write mode, you may toggle bit settings high or low by clicking the DIP switches. In read mode, however, DIP switches only monitor the bit settings currently in the I/O register; you cannot change bit settings.*

9. Using the DIP switches on the PIO Control Panel, set ports A, B, and C to bit pattern 1, as shown in Figure 5-12. Bit pattern 1 corresponds to a byte value of 55 in hexadecimal.

Figure 5-12
Port output settings, bit pattern 1



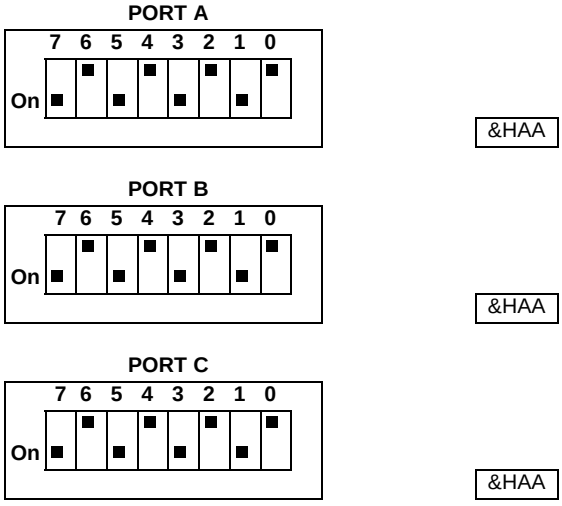
NOTE *Note that the bit is ON when the switch button is DOWN.*

10. Click the 'Update All' button on the PIO Control Panel.
11. Measure the voltage between signal ground and each bit of ports A, B, and C with a DMM or DVM or check the logic level for each bit of ports A, B, and C bit with a TTL logic probe. Connect these instruments to the terminal accessory or ribbon cable that is connected to the selected KPCI-PIO I/O connector.

    Each bit set to ON in the PIO Control Panel should output a logic-high signal at the corresponding I/O terminal, corresponding roughly to 4 volts at a DMM/DVM. Each bit set to OFF in the PIO Control Panel should output a logic-low signal at the corresponding I/O terminal, corresponding roughly to 0 volts at a DMM/DVM.

    - If the bit patterns set on the PIO Control Panel do not agree with the logic levels measured at the I/O terminals, the board is not functioning properly. Stop here, and return to the step in the "General problem isolation procedure" where you were directed to do I/O bit tests (step 17 or step 26e in the "General problem isolation procedure").
    - If the bit patterns set on the PIO Control Panel agree with the logic levels measured at the I/O terminals, then continue with step 12.
12. Using the DIP switches on the PIO Control Panel, set ports A, B, and C to the bit patterns shown in Figure 5-13, which correspond to byte values of AA in hexadecimal.

Figure 5-13
Port output settings, bit pattern 2



13. Click the 'Update All' button on the PIO Control Panel.
14. Again, measure the voltage between signal ground and each bit of ports A, B, and C with a DMM or DVM or check the logic level for each bit of ports A, B, and C bit with a TTL logic probe. Connect these instruments to the terminal accessory or ribbon cable that is connected to the selected KPCI-PIO I/O connector.

    Again, each bit set to ON in the PIO Control Panel should output a logic-high signal at the corresponding I/O terminal, corresponding roughly to 4 volts at a DMM/DVM. Each bit set to OFF in the PIO Control Panel should output a logic-low signal at the corresponding I/O terminal, corresponding roughly to 0 volts at a DMM/DVM.

    - If the bit patterns set on the PIO Control Panel do not agree with the logic levels measured at the I/O terminals, the board is not functioning properly. Stop here, and return to the step in the "General problem isolation procedure" where you were directed to do I/O bit tests (step 17 or step 26e in the "General problem isolation procedure").
    - If the bit patterns set on the PIO Control Panel do agree with the logic levels measured at the I/O terminals, and you have performed an output set test for all four port groups, the board is functioning properly. Stop here, and return to the step in the "General problem isolation procedure" where you were directed to do I/O bit tests (step 17 or step 26e in the "General problem isolation procedure"). Or, optionally, perform the I/O loop-back test, as discussed in the previous section, if you have not already done so.

Technical support

Before returning any equipment for repair, call Keithley for technical support at:

1-888-KEITHLEY
Monday - Friday, 8:00 a.m. - 5:00 p.m., Eastern Time

An applications engineer will help you diagnose and resolve your problem over the telephone. Please make sure that you have the following information available before you call:

KPCI-PIO24 board configuration	Model	_____
	Serial #	_____
	Revision code	_____
	Base address setting	_____
	Interrupt level setting	_____
	Number of channels	_____
Computer	Manufacturer	_____
	CPU type	_____
	Clock speed (MHz)	_____
	KB of RAM	_____
	Video system	_____
	BIOS type	_____
Operating system	DOS version	_____
	Windows version	_____
	Windows mode	_____
Software package	Name	_____
	Serial #	_____
	Version	_____
	Invoice/Order #	_____
Compiler (if applicable)	Language	_____
	Manufacturer	_____
	Version	_____
Accessories	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____

If a telephone resolution is not possible, the applications engineer will issue you a Return Material Authorization (RMA) number and ask you to return the equipment. Include the RMA number with any documentation regarding the equipment.

When returning equipment for repair, include the following information:

- Your name, address, and telephone number.
- The invoice or order number and date of equipment purchase.
- A description of the problem or its symptoms.
- The RMA number on the **outside** of the package.

Repackage the equipment, using the original anti-static wrapping, if possible, and handle it with ground protection. Ship the equipment to:

ATTN: RMA #_____
Repair Department
Keithley Instruments, Inc.
28775 Aurora Road
Cleveland, Ohio 44139

Telephone 1-888-KEITHLEY
FAX (440) 248-6168

NOTE *If you are submitting your equipment for repair under warranty, you must include the invoice number and date of purchase.*

To enable Keithley to respond as quickly as possible, you must include the RMA number on the outside of the package.

A
Specifications

Specifications for the KPCI-PIO24 board are listed in the following table.

Table A-1
KPCI-PIO24 Specifications

Number of I/O Lines		24, bi-directional, non-isolated, TTL compatible				
I/O interface		The group of 24 I/O lines, emulates one 8255A chip configured for Mode O				
External connections		One 37 pin 'D' type connector				
Signal parameters		**Parameter Descriptions**	**Min.**	**Typ.**	**Max.**	**Unit**
Data lines	V_{IH}	Voltage, Input High	2.0	-	-	V
	V_{IL}	Voltage, Input Low	-	-	0.8	V
	I_{IH}	Current, Input High, at V_{IN} = 2.7V	-	-	±1	µA
	I_{IL}	Current, Input Low, at V_{IN} = 0.5V	-	-	±1	µA
	I_{OZH}	High Impedance Output Current, at V_{out} = High	-	-	±1	µA
	I_{OZL}	High Impedance Output Current, at V_{out} = Low	-	-	±1	µA
	V_{OH}	Voltage, Output High, at I_{OH} = -8mA	2.4	3.3	-	V
	V_{OH}	Voltage, Output High, at I_{OH} = -15mA	2.0	3.0	-	V
	V_{OL}	Voltage, Output Low, at I_{OL} = 64mA	-	0.3	0.55	V
	I_{OL}	Current, Output Low	-	-	64	mA
	I_{OH}	Current, Output High	-	-	-15	mA
	I_{OS}	Short Circuit Current	-60	-120	-225	mA
	I_{OFF}	Input/Output Power-Off Leakage	-	-	±1	µA
Interrupt lines	I_{IL}	Current, Input Low	-	-	-100	µA
	I_{IH}	Current, Input High	-	-	-10	µA
	V_{OL}	Voltage, Output Low, at I_{OL} = Maximum	-	0.3	0.5	V
	V_{OH}	Voltage, Output High, at I_{OH} = Maximum	2.4	3.3	-	V
	I_{OL}	Current, Output Low	-	-	16	mA
	I_{OH}	Current, Output High	-	-	-3.2	mA
Power Requirements		+5 VDC, 25 W maximum				
Additional power to external circuits		+5 VDC, 1A maximum, total				
Environmental		Operating temperature	0 to 50° C			
		Storage temperature	0 to 70° C			
		Relative humidity	20 to 90% noncondensing			
Physical dimensions		175 mm long × 107 mm wide × 19 mm high (6.88 in × 4.2 in × 0.75 in)				
Weight		116 g (4.1 oz)				

B
Glossary

Address[1]

A number specifying a location in memory where data is stored.

API

See application programming interface.

Application programming interface[1]

A set of routines used by an application program to direct the performance of a procedure by the computer's operating system.

Bus mastering

On a microcomputer bus such as the PCI bus, the ability of an expansion board to take control of the bus and transfer data to memory at high speed, independently of the CPU. Replaces direct memory access (DMA).

Bus

An interconnection system that allows each part of a computer to communicate with the other parts.

Byte

A group of eight bits.

Contact bounce

The intermittent and undesired opening of relay contacts during closure, or closing of relay contacts during opening.

Crosstalk

The coupling of a signal from one input to another (or from one channel to another or to the output) by conduction or radiation. Crosstalk is expressed in decibels at a specified load and up to a specific frequency.

Darlington

A high gain current amplifier composed of two bipolar transistors, typically integrated in a single package.

DLL

See Dynamic Link Library.

Direct memory access

See DMA mode.

DMA mode

Direct memory access mode. Mode in which data transfers directly between an I/O device and computer memory. In the most general sense, PCI bus mastering is a DMA mode. More commonly, however, DMA mode refers to data transfers across the ISA bus, using a special circuitry on the computer motherboard. *See also* bus mastering.

Driver

Software that controls a specific hardware device, such as a data acquisition board.

Dynamic Link Library (DLL)

A software module in Microsoft Windows containing executable code and data that can be called or used by Windows applications or other DLLs. DLL functions and data are loaded and linked at run time when they are referenced by a Windows application or other DLLs.

Expansion slot[1]

A socket in a computer designed to hold expansion boards and connect them to the system bus (data pathway).

External trigger

An analog or digital hardware event from an external source that starts an operation. *See also* internal trigger.

Foreground task

An operation, such as a task that occurs in the single or synchronous mode, that cannot take place while another program or routine is running.

FIFO

First-in/first-out memory buffer. The first data into the buffer is the first data out of the buffer.

GPIB

Abbreviation for General Purpose Interface Bus. It is a standard for parallel interfaces.

IEEE-488

See GPIB.

Input/Output (I/O)

The process of transferring data to and from a computer-controlled system using its communication channels, operator interface devices, data acquisition devices, or control interfaces.

Input/output port[1]

A channel through which data is transferred between an input or output device and the processor.

Internal tigger

A software-generated event that starts an operation. *See also* external trigger.

Interrupt

A signal to the CPU indicating that the board detected the occurrence of a specified condition or event.

Interrupt level

A specific priority that ensures that high priority interrupts get serviced before low priority interrupts.

Interrupt-mode operation

Mode in which a data acquisition board acquires or generates samples using an Interrupt Service Routine (ISR).

Interrupt service routine (ISR)

A software program that handles interrupts.

ISA Bus

Industry Standard Architecture. The 16-bit wide bus architecture used in most MS-DOS and Windows computers. Sometimes called the AT bus.

Map[1]

Any representation of the structure of an object. For example, a memory map describes the layout of objects in an area of memory, and a symbol map lists the association between symbol names and memory addresses in a program.

OCX

Abbreviation for OLE Custom Control.

Pass-through operation

See target mode.

PCI

Abbreviation for Peripheral Component Interconnect. It is a standard for a local bus.

Port

See input/output port.

Port group

For digital I/O emulating the I/O of an 8255 programmable peripheral interface chip, a group of three 8 bit ports, commonly labeled PA, PB and PC. Digital I/O that emulates multiple 8255 chips is typically divided into multiple port groups.

Port I/O call

A software program statement that assigns bit values to an I/O port or retrieves bit values from an I/O port. Examples include a C/C++ statement containing an `inp` or `outp` function or a Basic statement containing a `peek` or `poke` function.

Register[1]

A set of bits of high speed memory within a microprocessor or other electronic device, used to hold data for a particular purpose.

Shielding

A metal enclosure for the circuit being measured or a metal sleeve surrounding wire conductors (coax or triax cable) to lessen interference, interaction, or current leakage. The shield is usually grounded.

Target mode

A PCI bus mode in which data from a data acquisition card is transferred indirectly to the computer memory in the foreground, via the host computer CPU, instead of directly, via Bus mastering. Sometimes referred to as pass-through operation. *See also* bus mastering and foreground task.

Trap[1] **(*verb*)**

To intercept an action or event before it occurs, usually in order to do something else.

TTL

Abbreviation for transistor-transistor-logic. A popular logic circuit family that uses multiple-emitter transistors. A low signal state is defined as a signal 0.8 V and below. A high signal state is defined as a signal +2.0 V and above.

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[1] *Microsoft Press® Computer Dictionary, Third Edition*. Refer to "Sources" below.

Sources:

Keithley Instruments, Inc., *Catalog and Reference Guide* (full line catalog), glossary, 1998

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