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PCIP-SCOPE

USER'S GUIDE

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PCIP-SCOPE User's Guide

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Preface

This manual is designed for users responsible for setting up, installing, and using the PCIP-SCOPE board.

The information in this manual assumes that you are familiar with your computer and its operation and that you are familiar with data acquisition principles.

This manual is organized as follows:

- Chapter 1 provides an introduction to the features of the PCIP-SCOPE board, supported software, and accessories.
- Chapter 2 describes how to unpack and inspect the board, set the base address, install the board, and connect signals to the board.
- Chapter 3 provides a functional description of the board.
- Chapter 4 describes how to calibrate the board.
- Chapter 5 describes how to troubleshoot problems and how to return the board should it be necessary.
- Chapter 6 describes the register map for the board.
- Appendix A lists the specifications for the board.
- Appendix B provides the information for CE mark certification.
- An index completes this manual.

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1

Introduction

The PCIP-SCOPE is a dual-trace, digital sampling oscilloscope board that plugs directly into any I/O slot of an IBM® PC/XT™, PC AT®, or ISA bus-compatible computer. This chapter describes the following aspects of the board:

- Major features
- Supported software
- Available accessories

Features

The major features of the PCIP-SCOPE board are as follows:

- Provides two channels, each with a 20 MHz sampling rate; 500 MHz interlace sampling for repetitive waveforms.
- Provides alternate and chopped modes, which allow a wide range of horizontal time scales.
- Supports an input voltage range of less than 5 mV to 175 V.
- Supports AC or DC coupling.
- Supports internal and external triggering on positive and negative edges.
- Uses an 8-bit analog-to-digital converter.
- Measures 1024 samples/channel in dual channel mode or 2048 samples/channel in single channel mode.
- Supports 1:1 and 10:1 probes.

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- Provides a bandwidth for DC coupling of DC to 10 MHz (using 10:1 probes) and a bandwidth for AC coupling of 10 Hz to 10 MHz (using 10:1 probes).
- Operates in two ways:
  - As a standard bench instrument - In this mode, the board functions like a standard bench-top instrument, except that the readings are displayed on the computer screen, not on CRTs or LCDs, and the channel selected, trigger level, and so on, are selected using the keyboard or mouse.
  - Under program control - This mode allows you to write programs that control the board directly, which is useful when using the board in automated tests or experiments.
- Provides BNC connectors for all inputs.

Supported Software

VisualSCOPE software is provided for the PCIP-SCOPE board. VisualSCOPE includes a Windows™ interface similar to that of a standard benchtop oscilloscope; this software allows you to capture and analyze waveforms, and transfer data and graphic images to other Windows applications without programming. VisualSCOPE is described in a separate manual, shipped with the software.

Accessories

The following accessories are optional for the PCIP-CNTR board:

- **C-BMM-5** cable - 5-foot BNC-to-BNC cable.
- **C-BMM-15** cable - 15-foot BNC-to-BNC cable.
- **PRB-110x** probe - 1:1 (x1) or 10:1 (x10) scope probe and cable; the use of probes with the PCIP-SCOPE board is recommended for best performance.

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2

Setup and Installation

This chapter describes how to set up and install the PCIP-SCOPE board. The following procedures are provided:

- Unpacking and inspecting
- Setting the base address
- Installing the board
- Connecting signals

Unpacking and Inspecting the Board

After you remove the wrapped board from its outer shipping carton, proceed as follows:

1. Your board is packaged at the factory in an anti-static wrapper that must not be removed until you have discharged any static electricity by either of the following methods:
   - If you are equipped with a grounded wrist strap, you discharge static electricity as soon as you hold the wrapped board.
   - If you are not equipped with a grounded wrist strap, discharge static electricity by holding the wrapped board in one hand while placing your other hand firmly on a metal portion of the computer chassis (your computer must be turned off but grounded).
2. Carefully unwrap your board from its anti-static wrapping material. (You may wish to store the wrapping material for future use.)
3. Inspect the board for signs of damage. If damage is apparent, arrange to return the board to the factory (see page 5-7).

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4. Check the remaining contents of your package against the packing list to be sure your order is complete. Report any missing items, immediately.
5. When you are satisfied with the inspection, proceed with setting the base address.

Setting the Base Address

The PCIP-SCOPE has a default base address setting of 300h; this address is typically free in most computers. However, no two boards can use the same base address. If you are using more than one board, you must assign each board a unique base address. Base addresses range from 000h to 3FFh (0 to 1023 decimal) on an 8-byte boundary.

A seven-position DIP switch on the board selects where in the computer's I/O space the board resides. Figure 2-1 shows the address values corresponding to each of the seven switches.

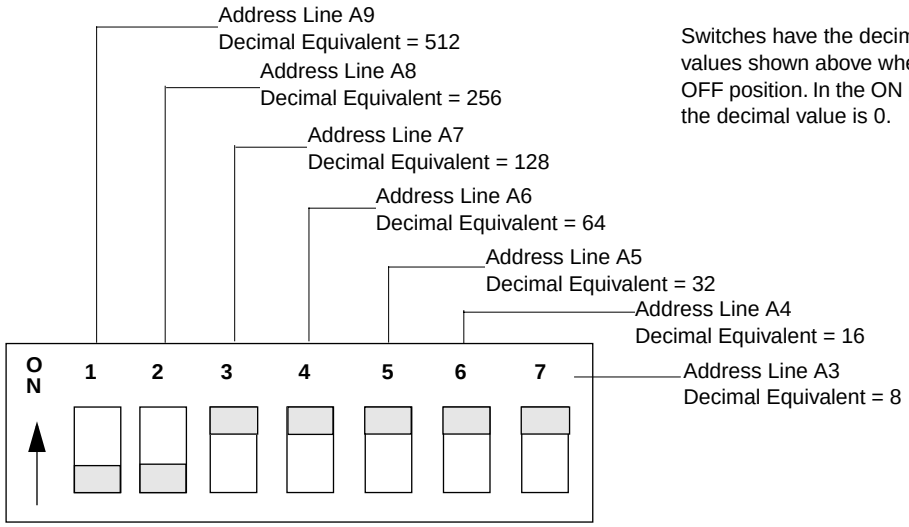


Figure 2-1. The Base Address Select Switch (Default Base Address of 300h Shown)

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Installing the Board

This section provides general instructions for installing the PCIP-SCOPE board. For more detailed information on installing peripheral boards, consult the documentation provided with your computer.

Caution: Do not insert or remove any peripheral board with the computer power on. This could cause damage to your computer.

Use the following steps to install the PCIP-SCOPE board in an accessory slot of your computer:

1. Turn off power to the computer and all attached equipment.
2. Remove the computer chassis cover.
3. Select an unoccupied accessory slot, and remove the corresponding blank plate from the I/O connector panel.
4. Make sure the setting of the base address switch is correct for your board.
5. Insert and secure the board in the selected slot.
6. If you are using probes, you are advised to adjust the frequency response of the probes and the PCIP-SCOPE board; refer to Chapter 4. However, at first you may prefer to become familiar with PCIP-SCOPE operation before making frequency adjustments.
7. Replace the computer cover.
8. Turn on power to the computer.

You are now ready to connect signals to the board, as described in the following section.

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Connecting Signals

Generally, you will use a probe to connect signals to the PCIP-SCOPE board. Probes are either 1:1 (x1), meaning the connection is direct, or 10:1 (x10), meaning the connection passes through a 10:1 attenuator. An 10:1 probe increases the input range by a factor of ten and also offers better high-frequency response.

BNC plugs are provided to connect probes to Channel A and Channel B on the PCIP-CNTR board; note that Channels A and B also accept a trigger. The External Trigger BNC connector is provided to connect an external trigger signal only.

Figure 2-2 shows the location of the BNC connectors.

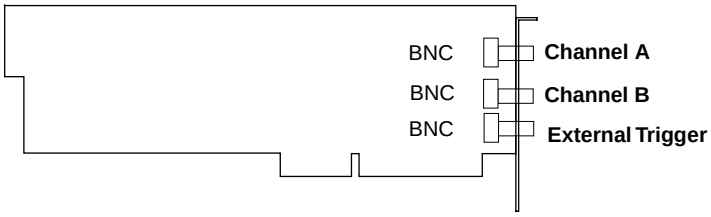


Figure 2-2. The Board I/O Connectors

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3

Functional Description

This chapter describes the functionality of the PCIP-SCOPE board. Many users of the PCIP-SCOPE will not need to refer to this chapter. However, in certain circumstances it may be important to know the technical details of the board's operation. This chapter describes the following:

- Block diagram
- Bus interface
- Signal input channels
- Triggering
- Data conversion and storage

Block Diagram

PCIP-SCOPE circuits are arranged as shown in the block diagram in Figure 3-1. Use the block diagram as a reference for the descriptions presented in the rest of this chapter.

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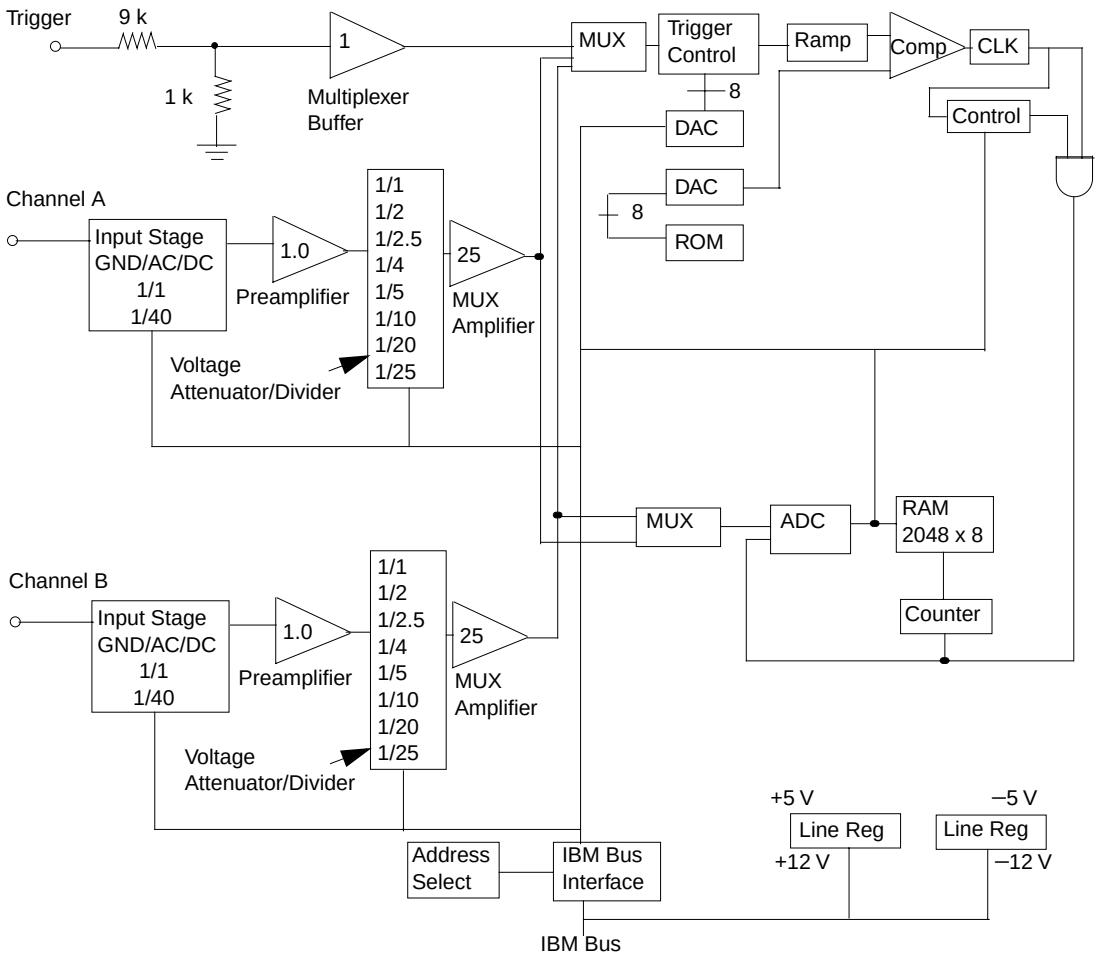


Figure 3-1. Block Diagram of PCIP-SCOPE Circuitry

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Bus Interface

An onboard microcontroller manages the acquisition and storage of data. To set the appropriate vertical sensitivity, horizontal time scale, coupling, and trigger parameters and to initiate the acquisition and retrieve the data from memory, the computer must communicate with the microcontroller and other onboard components. The computer communicates with the PCIP-SCOPE through eight registers, starting at a base address. The base address for these registers can be any available number in the computer's I/O address space and is set with a DIP switch on the board. Refer to page 2-2 for more information on setting the base address.

Signal Input Channels

Channel A and Channel B of the PCIP-SCOPE board accept input signals. Signals entering either channel normally pass through a series of attenuator/amplifier stages before arriving at the analog-to-digital converter (ADC).

The first input stage combines a divide-by-one feed-through and a divide-by-40 attenuator. An input relay routes signals directly to this stage for DC coupling or through a capacitor for AC coupling. At the output of the first stage, a relay controlling both channels switches one signal to ground and the other to the preamplifier stage; note that with the ground setting, both channels are grounded.

Preamplifier circuitry provides a gain of 1.25 and is buffered against excessive signal levels by an 0.8 attenuator. This stage presents a high impedance to the input signal while driving a low impedance voltage attenuator/divider.

A tap at each stage of the voltage attenuator/divider provides eight levels of output. These outputs pass to the inputs of a video multiplexer (MUX) amplifier. The multiplexer amplifier, along with a gain stage that follows the voltage divider, provides a gain of 25.

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Proper attenuation of a full-scale input signal at any vertical sensitivity holds the multiplexer amplifier output to within ±0.5 V. To sustain this output range, the attenuator settings required for each level of vertical sensitivity are shown in Table 3-1.

Table 3-1. Input Stage Divider and Voltage/Attenuator Divider Settings for Vertical Sensitivity

Vertical Sensitivity	Input Stage Divider	Voltage/ Attenuator Divider
5 mV/division	1	1
10 mV/division	1	2
20 mV/division	1	4
50 mV/division	1	10
100 mV/division	1	20
200 mV/division	40	1
500 mV/division	40	2.5
1 V/division	40	5
2 V/division	40	10
5 V/division	40	25

Notes: The greater the vertical sensitivity, the greater the height of the waveform.

When you measure an unknown voltage, you should select the lowest sensitivity (5.0 V/division) and increase the sensitivity a step at a time until you fill the display.

Keep in mind that the PCIP-SCOPE, like all oscilloscopes, is sensitive to noise when using smaller voltages; attaching a probe's ground lead close to the measuring point helps to reduce this noise.

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Triggering

Using some feature of the input waveform, the trigger-control circuit synchronizes data collection. You can select an input from Channel A, Channel B, or the External Trigger connector as the trigger source.

An 8-bit digital-to-analog converter (DAC) sets the level of the signal initiating the trigger. The output of the DAC ranges between the ±0.5 V full-scale input of the ADC.

The polarity (slope) of the signal (the rise or fall) is also a triggering parameter. When the signal voltage passes through the level set by the DAC, the polarity of the signal must match the selected value before the trigger-control circuit generates an output.

The trigger starts the 20 MHz onboard clock, which times data collection. Because of delays that are inherent in the circuitry and components, a delay of about 150 ns occurs between the time the trigger is initiated and the time the trigger takes effect.

Data Conversion and Storage

The core of data acquisition is an 8-bit flash ADC. An onboard clock times the ADC to cause a conversion; it also clocks the transfer of converted data to a 2048-by-8 bit static memory RAM.

The clock runs at 20 MHz, which is the fastest rate at which the converter can be clocked. A 20 MHz sampling rate corresponds to a sample of 50 ns, which corresponds to a horizontal time scale of 5 µs/division. For longer time scales, the clock is counted down. For shorter time scales, you can use an interlaced equivalent-time technique on repetitive waveforms. The following subsections describe these two techniques in more detail.

Notes: Ensure that the time scale you choose does not cause aliasing problems. See page 5-5 for more information on aliasing.

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As data is transferred from the ADC to memory, the memory address must be incremented. Incrementing is accomplished using counter outputs to address the RAM. Before an acquisition sequence starts, the counter is reset to zero. After a sample is clocked into RAM, the counter is clocked to increment the memory address for the next sample.

Counting Down - Chopped and Alternate Mode

Clocking the ADC directly causes data to be acquired every 50 ns. At that rate, 1000 acquisitions take 50 µs; this data can then be displayed. Spreading the 50 µs display across ten horizontal divisions results in a time scale of 5 µs/division. The same clock works for a time scale of 10 µs/division, provided an acquisition occurs with every other clock pulse. Similarly, counting down the clock even more generates longer time scales.

Note: The time scale multiplied by ten horizontal divisions is known as the *sweep time.*

Channel A and Channel B share the board's single ADC. To acquire data from both channels, the multiplexer (also shared by the two channels) must be switched. The total time required for the multiplexer to switch and the signals to stabilize enough for a valid conversion is about 500 ns. With time scales of 100 µs/division and longer, it is possible to acquire both channels with a single sweep. For the 100 µs/division rate, the trigger starts an acquisition of Channel A and switches the multiplexer. After ten clocks (500 ns), the data for Channel B is acquired and the multiplexer switches back to Channel A. This technique for acquiring two channels is called *chopped mode*.

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For time scales shorter than 50 µs/division, the time between acquisitions is not sufficient for switching and settling. In these cases, it is necessary to acquire all the samples (1024) for Channel A after the first trigger occurs, then switch the multiplexer. After a delay of 500 ns, the PCIP-SCOPE board waits for a second trigger, then acquires 1024 samples from Channel B. This technique for acquiring two channels is called *alternate mode*.

Table 3-2 shows the relationship of the horizontal time scales to the sampling technique used for two channels.

Table 3-2. Relationship of Horizontal Time Scale to Sampling Technique

Horizontal Time Scale	Sweep Time	Sampling Period	Clocks/ Sample	Technique for Sampling Two Channels
5 µs/division	50 µs	50 ns	1	Alternate
10 µs/division	100 µs	100 ns	2	Alternate
20 µs/division	200 µs	200 ns	4	Alternate
50 µs/division	500 µs	500 ns	10	Alternate
100 µs/division	1 ms	1 µs	20	Chopped
200 µs/division	2 ms	2 µs	40	Chopped
500 µs/division	5 ms	5 µs	100	Chopped
1 ms/division	10 ms	10 µs	200	Chopped
2 ms/division	20 ms	20 µs	400	Chopped
5 ms/division	50 ms	50 µs	1000	Chopped
10 ms/division	100 ms	100 µs	2000	Chopped
20 ms/division	200 ms	200 µs	4000	Chopped
50 ms/division	500 ms	500 µs	10000	Chopped
100 ms/division	1 s	1 ms	20000	Chopped
200 ms/division	2 s	2 ms	40000	Chopped
500 ms/division	5 s	5 ms	100000	Chopped

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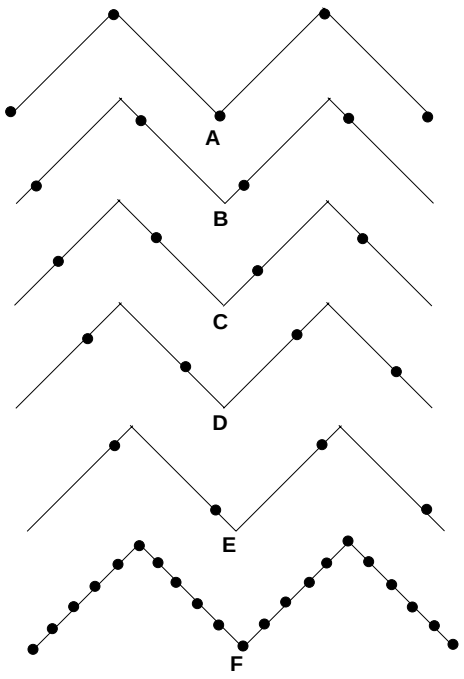
Interlace Mode

The four shortest horizontal time scales require the sampling periods shown in the Table 3-3. The periods shown are shorter than the standard 50 ns used for other time scales.

Table 3-3. Horizontal Time Scales for Interlace Mode

Horizontal Time Scale	Sweep Time	Sampling Period
200 ns/division	2 µs	2 ns
500 ns/division	5 µs	5 ns
1 µs/division	10 µs	10 ns
2 µs/division	20 µs	20 ns

Periods shorter than 50 ns are achieved for repetitive waveforms, as illustrated in Figure 3-2.



This diagram shows five stages of 50 ns sampling.

In each consecutive stage, sampling is delayed 10 ns.

When the results of the five samples are properly interlaced, the waveform of Stage F is obtained.

Note that the dots show sampling data points for each waveform.

Figure 3-2. Interlace Mode

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Figure 3-2 illustrates a time scale of 1 µs/division; in this case, the waveform is sampled five times more closely than the capability of the board's ADC.

If the waveform is sampled once as shown in Stage A, the sampling may be a bit coarse. If those samples are saved and combined with samples from latter repetitions of the same waveform, however, a finer equivalent sampling occurs.

Suppose the board was triggered at the negative peak of the waveform and sampled every 50 ns as shown in Stage A. Next, assume the board was triggered again at a negative peak but that the sampling was delayed for 10 ns. This time the results of Stage B are obtained. If this process is repeated three more times with delays of 20 ns, 30 ns, and 40 ns between the trigger and the start of sampling, the results of Stages C, D, and E are obtained. If the results from these five samplings are properly interlaced, the display of Stage F can be produced, which has a resolution five times that of the base rate of the ADC.

The trigger-control and clock circuitry of the PCIP-SCOPE board generate the variable delays required for equivalent time sampling. The trigger-control circuit actually starts a ramp generator, which generates a voltage that increases linearly in time. When this voltage exceeds the other comparator input, the clock is started. Normally, the DAC input to the comparator is low, which causes the clock to start almost immediately. For the second and subsequent sampling cycles of an equivalent time sample, the ROM address is changed so that the ROM output (the input to the DAC) is changed and the DAC output to the comparator is increased. Thus, the ramp generator must run longer before its output exceeds the DAC output and sampling begins.

The 1 µs/division time scale requires five sample cycles and a delay between the trigger and the start of sampling for each cycle (after the first is increased by 10 ns over that of the previous cycle), as shown in Figure 3-2. If one channel is being sampled, a total of 2048 samples are acquired. The first three cycles acquire 410 samples and the last two cycles acquire 409 samples. If both channels are sampled, the first 1024 samples are acquired for Channel A and the second 1024 samples are acquired for Channel B. The 1024 samples are obtained from four cycles of 205 samples each and one last cycle of 204 samples.

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The 2 µs/division time scale is handled similarly to the 1 µs/division time scale except that the clock is divided by two, making the basic sampling period 100 ns. For the 2 µs/division time scale, five cycles with 20 ns increments are used.

The 500 ns/division time scale uses 10 cycles with 5 ns delay increments; the 200 ns/division time scale requires 25 cycles with 2 ns delay increments. Table 3-4 summarizes the data acquisition scheme for one channel; Table 3-5 summarizes the data acquisition scheme for two channels.

Table 3-4. Data Acquisition Scheme for One Channel

Horizontal Time Scale	First Cycles		Last Cycles	
	Cycles	Samples	Cycles	Samples
200 ns/division	23	82	2	81
500 ns/division	8	205	2	204
1 µs/division	3	410	2	409
2 µs/division	3	410	2	409

Table 3-5. Data Acquisition Scheme for Two Channels

Horizontal Time Scale	First Cycles		Last Cycles	
	Cycles	Samples	Cycles	Samples
200 ns/division	24	41	1	40
500 ns/division	4	103	6	102
1 µs/division	4	205	1	204
2 µs/division	4	205	1	204

Potentiometer R11 adjusts the interlace ramp generator to produce smoother waveform displays.

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4

Calibration

The PCIP-SCOPE board is calibrated at the factory prior to shipment. You are advised to recalibrate the PCIP-SCOPE board every six months.

To calibrate the board, use the software utility PSCOPECAL.EXE provided with the board to make the following adjustments:

1. Adjust the DC offset of Channel A and Channel B.
2. Adjust the gain of Channel A and Channel B.
3. Adjust the frequency response (preamplifier and attenuator) of Channel A and Channel B.
4. Adjust the probe frequency response of Channel A and Channel B.
5. Adjust interlace mode.

Table 4-1 lists the components that must be adjusted to calibrate the board. Refer to Figure 4-1 on page 4-2 for the location of these components.

Table 4-1. Adjustment Components

Adjustments	Components for Channel A	Components for Channel B
Amplifier DC Offset	R3	R7
Preamplifier DC Offset	R1	R5
Gain	R2	R6
Preamplifier Frequency Response	C3	C7
Attenuator Frequency Response	C2	C6

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Table 4-1. Adjustment Components (cont.)

Adjustments	Components for Channel A	Components for Channel B
10:1 Probe Frequency Response (Divide-by-1)	Probe	Probe
10:1 Probe Frequency Response (Divide-by-40)	C1	C5
Interlace mode	R11	R11

Notes: It is especially important that you do not remove the cover on the board when making these adjustments.

Trim resistors are 20-turn potentiometers but trim capacitors vary over their full range in one half turn. Use a nonmetallic adjustment tool to adjust the capacitors.

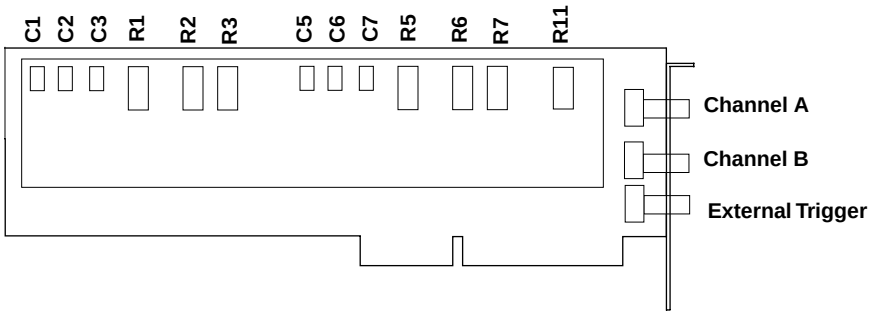


Figure 4-1. Location of the Adjustment Components

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5

Troubleshooting

If your PCIP-SCOPE board is not operating properly, use the information in this chapter to isolate the problem. If the problem appears serious enough to warrant technical support, refer to page 5-7 for information on how to contact an applications engineer.

Problem Isolation

If you encounter a problem with a PCIP-SCOPE board, use the instructions in this section to isolate the cause of the problem before calling for technical support.

Identifying Symptoms and Possible Causes

Use the troubleshooting information in Table 5-1 to try to isolate the problem. Table 5-1 lists general symptoms and possible solutions for problems with PCIP-SCOPE boards.

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Table 5-1. Troubleshooting Information

Symptom	Possible Cause	Possible Solution
Board does not respond	Base address is incorrect or not consistent with what the software is addressing.	Check the base address switch setting on the board. If the base address is set correctly, make sure no other computer device is using the I/O locations beginning at the specified base address. If necessary, reconfigure the base address. Refer to page 2-2 for instructions on setting the base address.
	The board is incorrectly aligned in the accessory slot.	Check the board for proper seating.
	The board is damaged.	Contact Keithley MetraByte for technical support; see page 5-7.
Intermittent operation	The most common cause of this problem is that the I/O bus speed is in excess of 8 MHz.	Reduce I/O bus speed to a maximum of 8 MHz (to change the I/O bus speed, run BIOS setup). See your computer documentation for instructions on running BIOS setup.
	Vibrations or loose connections exist.	Cushion source of vibration and tighten connections.
	The board is overheating.	Check environmental and ambient temperature. See the documentation for your computer.
	Electrical noise exists.	Provide better shielding or reroute unshielded wiring.

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Table 5-1. Troubleshooting Information (cont.)

Symptom	Possible Cause	Possible Solution
Data appears to be invalid	The most common cause of this problem is that the I/O bus speed is in excess of 8 MHz.	Reduce I/O bus speed to a maximum of 8 MHz (to change the I/O bus speed, run BIOS setup). See the documentation for your computer for instructions on running BIOS setup.
	An open connection exists.	Check wiring.
	Another system resource is using the specified base address.	Reconfigure the base address of the PCIP-SCOPE board; refer to page 2-2 for more information. Check the I/O assignments of other system resources and reconfigure, if necessary.
	An aliasing problem exits.	Shift the time scale; see page 5-5.
Computer does not boot.	Board not seated properly.	Check the installation of the board.
	The base address setting of the PCIP-SCOPE board conflicts with that of another system resource.	Check the base address settings of your system resources; each address must be unique.
	The power supply of the host computer is too small to handle all the system resources.	Check the needs of all system resources and obtain a larger power supply.
System lockup	A timing error occurred.	Press **Ctrl + Break**.

If your board is not operating properly after using the information in Table 5-1, continue with the next two sections to further isolate the problem.

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Testing the Board and Host Computer

To isolate the problem to the PCIP-SCOPE board or to the host computer, use the following steps:

Caution: Removing a board with the power ON can cause damage to your board and/or computer.

---

1. Turn off power to the host computer and remove power connections to the computer.
2. While keeping connections to accessories intact, unplug the cables to the PCIP-SCOPE board.
3. Remove the board from the computer and visually check for damage. If a board is obviously damaged, refer to page 5-7 for information on returning the board.
4. With the PCIP-SCOPE board out of the computer, check the computer for proper operation. Power up the computer and perform any necessary diagnostics.

At this point, if you have another PCIP-SCOPE board that you know is functional, you can test the slot and I/O connections using the instructions in the next section. If you do not have another board, refer to the instructions on page 5-7 before calling Keithley MetraByte for technical support.

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Testing the Accessory Slot and I/O Connections

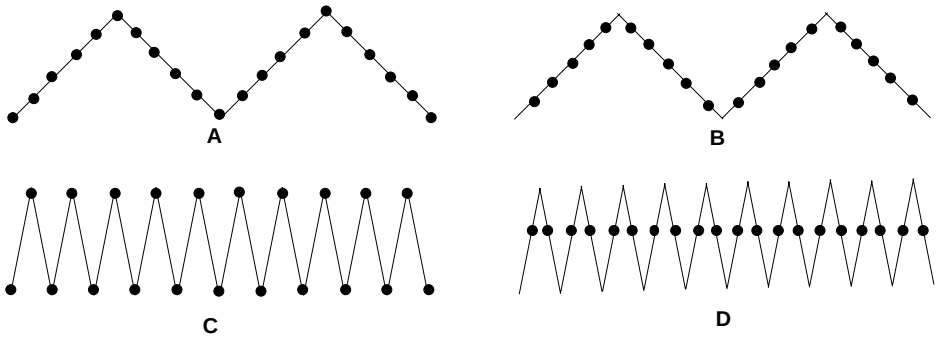
When you are sure that the computer is operating properly, test the computer accessory slot and I/O connections using another PCIP-SCOPE board that you know is functional. To test the computer accessory slot and the I/O connections, follow these steps:

1. Remove computer power again and install a PCIP-SCOPE board that you know is functional. Do not make any I/O connections.
2. Turn on power to the computer and check operation with the functional board in place. This test checks the computer accessory slot. If you were using more than one board when the problem occurred, use the functional board to test the other slot, as well.
3. If the accessory slots are functional, use the functional board to check the I/O connections. Reconnect and check the operation of the I/O connections, one at a time.
4. If operation fails for an I/O connection, check the individual inputs one at a time for shorts and opens.
5. If operation remains normal to this point, the problem is in the PCIP-SCOPE board(s) originally in the computer. If you were using more than one board, try each board one at a time in the computer to determine which is faulty.
6. If you cannot isolate the problem, refer to the page 5-7 for instructions on obtaining assistance.

Dealing with Aliasing Problems

Sampling scopes are sometimes subject to a property known as aliasing. Normally, these scopes sample a waveform periodically and reconstruct the waveform from the series of samples; in addition, reconstruction is normally a simple interpolation between adjacent samples. A good reconstruction occurs if samples are taken much more rapidly than the waveform changes in time. However, when the waveform changes appreciably between samples, the reconstruction may bear little resemblance to the original waveform. In fact, the reconstruction of many different waveforms or aliases is possible with such samples. Figure 5-1 illustrates aliasing possibilities with a given sampling.

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Note that the dots show sampling data points for each waveform.

Figure 5-1. Aliasing

In the diagram, the dots show acquired samples. In Figure 5-1A and C, the triangular waveforms would be recreated exactly by connecting the dots. In Figure 5-1B and D, the samples are taken at the same rate but are shifted slightly with respect to the waveform. In Figure 5-1B connecting the dots would give a slightly distorted triangle with the peaks clipped. In Figure 5-1D, however, the reconstructed waveform would be a constant value. Indeed for Figure 5-1C, if the sampling time relative to the waveform is shifted continuously, one would obtain a triangular waveform with an amplitude varying from the maximum of Figure 5-1C to zero for Figure 5-1D.

You can check for an aliasing by shifting time scales. Shifting to the next shorter time scale should spread the waveform out by a factor of 2 or 2.5, depending on the range. Therefore, if multiple repetitions of the waveform were previously observed, roughly half as many should exist when the next shorter time scale is used. Similarly, in shifting to a longer time scale, the display should compress the waveform by a factor of 2 or 2.5 depending on the range; therefore, you should see approximately twice as many repetitions.

If an entirely different waveform appears when the time scale is changed, an aliasing problem exists. You should eliminate the aliasing problem by shifting to a shorter time scale until the problem disappears.

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Technical Support

Before returning any equipment for repair, call Keithley MetraByte for technical support at:

(508) 880-3000

Monday - Friday, 8:00 A.M. - 6:00 P.M., Eastern Time

An applications engineer will help you diagnose and resolve your problem over the telephone. Please make sure that you have the following information available before you call:

PCIP-SCOPE Board Configuration	Model	_____
	Serial #	_____
	Revision code	_____
	Base address setting	_____
Computer	Manufacturer	_____
	CPU type	_____
	Clock speed (MHz)	_____
	KB of RAM	_____
	Video system	_____
	BIOS type	_____
Operating System	DOS version	_____
	Windows version	_____
Software Package	Name	_____
	Serial #	_____
	Version	_____
	Invoice/Order #	_____
Compiler (if applicable)	Language	_____
	Manufacturer	_____
	Version	_____
Accessories	Type	_____
	Type	_____
	Type	_____

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If a telephone resolution is not possible, the applications engineer will issue you a Return Material Authorization (RMA) number and ask you to return the equipment. Include the RMA number with any documentation regarding the equipment.

When returning equipment for repair, include the following information:

- Your name, address, and telephone number.
- The invoice or order number and date of equipment purchase.
- A description of the problem or its symptoms.
- The RMA number on the **outside** of the package.

Repackage the equipment, using the original anti-static wrapping, if possible, and handling it with ground protection. Ship the equipment to:

ATTN: RMA #_____
Repair Department
Keithley MetraByte
440 Myles Standish Boulevard
Taunton, Massachusetts 02780

Telephone (508) 880-3000
FAX 508/824-5517

Notes: If you are submitting your equipment for repair under warranty, you must include the invoice number and date of purchase.

To enable Keithley MetraByte to respond as quickly as possible, you must include the RMA number on the outside of the package.

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6

Register Map

For those who require more specific control over the PCIP-SCOPE than their software provides, this chapter describes how to use the register map to control the PCIP-SCOPE board. The following information is provided:

- Register map description
- Programming sequence using the registers

Register Map Description

The PCIP-SCOPE responds to eight addresses, described in Table 6-1. Each of these addresses is discussed in the following subsections.

Table 6-1. Register Map Summary

Location	Register	Read/Write
Base Address +0	Memory	Read/Write
Base Address +1	Clock Controller	Read/Write
Base Address +2	Trigger Level	Write only
Base Address +3	Channel_A	Write only
Base Address +4	Channel_B	Write only
Base Address +5	Trig/Time	Write only
Base Address +6	Reset	Read/Write
Base Address +7	Status	Read/Write

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Memory Register (Read/Write)

The 2048 bytes of memory can be read or written through Base Address +0. Note that writing to memory is never done except as a memory check. Normally, the onboard controller fills the memory with data during data acquisition and the computer reads the memory in order to display or process the acquired waveform.

Onboard memory is addressed by a counter that can be set to zero by writing to the Status register (Base Address + 7). Each read or write increments the counter so that the next read or write accesses the next location in the onboard memory.

Data from a single channel acquisition on the 5 µs/division through 500 ms/division time scales is stored directly to onboard memory. The data is acquired sequentially from the waveform and stored in PCIP-SCOPE memory in the same order.

For interlaced mode (200 ns/division through 2 µs/division time scales), data is acquired in a number of cycles, as explained on page 3-8. Data storage to onboard memory follows the order in which it was acquired; however, the data has to be reconstituted properly from onboard memory to computer memory before it can be displayed. For a single-channel acquisition on the 1 µs/division time scale (which requires five acquisition cycles), the first 410 values stored in PCIP-SCOPE memory are taken from the first sampling cycle. These samples correspond to the first, sixth, eleventh, and so on, values of the reconstituted waveform. The second point of the displayed waveform is the 411th value in PCIP-SCOPE memory and comes from the first sample of the second acquisition cycle. Similarly, the first point of the third cycle is the third point of the display; the first point of the fourth cycle is the fourth point of the display; and the first point of the fifth cycle is the fifth point of the display. The sixth through tenth points of the display come from the corresponding second acquisitions of the five acquisition cycles, and so on.

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When both channels are acquired, two modes (chopped and alternate) are used, as described on page 3-6. In chopped mode (for the 100 µs/division through 500 ms/division time scales), the first value in onboard memory is from Channel A; the second value in onboard memory is from Channel B. In alternate mode (for the 5 µs/division through 50 µs/division time scales), the first 1024 values in onboard memory are from Channel A and the second 1024 values in onboard memory are from Channel B.

Clock Controller Register (Read/Write)

During data acquisition, the PCIP-SCOPE board clocks the onboard controller. However, for it to initialize, the controller must receive a start address and it must be clocked until it is ready to start an acquisition. The computer clocks the controller by writing to the Clock Controller register at Base Address +1. When required, the start address is written to this register. The computer tests the Status register to determine the appropriate action.

In the absence of a trigger signal, reading the Clock Controller register initiates data acquisition.

Trigger Level Register (Write Only)

You can program the trigger level by writing to Base Address +2.

The trigger level is determined by the vertical sensitivity and is controlled by an 8-bit DAC on the board. The 8-bit range allows a level of 0 to 255, with 0 corresponding to the negative limit, 255 corresponding to the positive limit, and 127 corresponding to zero.

Channel_A Register (Write Only)

Base Address +3 controls the coupling and the vertical sensitivity of Channel A.

Coupling is either AC or DC. With DC coupling, a signal feeds directly to the first attenuator section; with AC coupling, a signal feeds through a coupling capacitor. The path is chosen by the ACUP relay. The first attenuator section either passes the signal directly to the second attenuator

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section or divides the signal by 40 before passing it to the second attenuator section.

The bit map for the Channel_A register is shown in Table 6-2.

Table 6-2. Bit Map of the Channel_A Register

Bit Number	Bit Name	Description
D7	ACUP	Ch A Coupling: AC (Low); DC (High)
D6	A1	Ch A Divide-by-1 Input Ground; Ground (Low)
D5	A40	Ch A Div-by-40 Input Ground; Ground (Low)
D4	AA1	Ch A Div-Select: Divide-by-1 (High); Divide-by-40 (Low)
D3	Unused	Unused
D2	A22	High Bit of A Attenuator Decode
D1	A21	Medium Bit of A Attenuator Decode
D0	A20	Low Bit of A Attenuator Decode

The input to the divide-by-1 or divide-by-40 path can be grounded by bits A1 or A40 respectively. Bit AA1 determines whether the signal feeds around or through the divide-by-40 attenuator on its way to the second attenuator section. Bits A20, A21, and A20 determine the attenuation of the second stage.

Table 6-3 shows the bit values that you should use for Channel A depending on the input stage divider selected.

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Table 6-3. Bit Values Corresponding to the Input Stage Divider - Channel A

Input Stage Divider	Bit A1	Bit A40	Bit AA1
1	high	low	high
40	low	high	low
Ground	low	low	don't care

Table 6-4 shows the values for the voltage/attenuator divider stage (the second attenuator stage) for Channel A.

Table 6-4. Values for the Voltage/Attenuator Divider Stage - Channel A

Voltage/ Attenuator Divider	Bit A22	Bit A21	Bit A20
25	low	low	low
20	low	low	high
10	low	high	low
5	low	high	high
4	high	low	low
2.5	high	low	high
2	high	high	low
1	high	high	high

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These results translate into the bit values shown in Table 6-5 for the vertical sensitivities provided on Channel A.

Table 6-5. Bit Values for Vertical Sensitivities on Channel A

Vertical Sensitivity	Input Stage Divider	Voltage/ Attenuator Divider	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0
5 mV/division	1	1	high	low	high	don't care	high	high	high
10 mV/division	1	2	high	low	high	don't care	high	high	low
20 mV/division	1	4	high	low	high	don't care	high	low	low
50 mV/division	1	10	high	low	high	don't care	low	high	low
100 mV/division	1	20	high	low	high	don't care	low	low	high
200 mV/division	40	1	low	high	low	don't care	high	high	high
500 mV/division	40	2.5	low	high	low	don't care	high	low	high
1 V/division	40	5	low	high	low	don't care	low	high	high
2 V/division	40	10	low	high	low	don't care	low	high	low
5 V/division	40	25	low	high	low	don't care	low	low	low

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Channel_B Register (Write Only)

Writing to Base Address +4 controls the coupling and the vertical sensitivity of Channel B.

Coupling is either AC or DC. With DC coupling, the signal feeds directly to the first attenuator section; with AC coupling the signal first feeds through a coupling capacitor. The path to the attenuator is chosen by the BCUP relay. The first attenuator section either passes the signal directly to the second attenuator section or divides the signal by 40 before passing it to the second attenuator section.

The bit map for the Channel_B register is shown in Table 6-6.

Table 6-6. Bit Map of the Channel_B Register

Bit Number	Bit Name	Description
D7	BCUP	Ch B Coupling: AC (Low); DC (High)
D6	B1	Ch B Divide-by-1 Input Ground; Ground (Low)
D5	B40	Ch B Divide-by-40 Input Ground; Ground (Low)
D4	BB1	Ch B Divisor-Select: Divide-by-1 (High); Divide-by-40 (Low)
D3	Unused	Unused
D2	B22	High Bit of B Attenuator Decode
D1	B21	Medium Bit of B Attenuator Decode
D0	B20	Low Bit of B Attenuator Decode

The input to the divide-by-1 or divide-by-40 path can be grounded by bits B1 or B40, respectively. Bit BB1 determines whether the signal will feed through or around the divide-by-40 attenuator to the second attenuator section. Bits B20, B21, and B20 determine the attenuation of the second attenuation stage.

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Table 6-6 shows the bit values that you should use for Channel B depending on the input stage divider selected.

Table 6-7. Bit Values Corresponding to the Input Stage Divider - Channel B

Input Stage Divider	Bit B1	Bit B40	Bit BB1
1	high	low	high
40	low	high	low
GND	low	low	don't care

Table 6-8 shows the values for the voltage/attenuator divider stage (the second attenuator stage) for Channel B.

Table 6-8. Values for the Voltage/Attenuator Divider Stage - Channel B

Voltage/ Attenuator Divider	Bit B22	Bit B21	Bit B20
25	low	low	low
20	low	low	high
10	low	high	low
5	low	high	high
4	high	low	low
2.5	high	low	high
2	high	high	low
1	high	high	high

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These results translate into the bit values shown in Table 6-9 for the vertical sensitivities provided on Channel B.

Table 6-9. Bit Values for Vertical Sensitivities on Channel B

Vertical Sensitivity	Input Stage Divider	Voltage/ Attenuator Divider	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0
5 mV/division	1	1	high	low	high	don't care	high	high	high
10 mV/division	1	2	high	low	high	don't care	high	high	low
2 mV/division	1	4	high	low	high	don't care	high	low	low
50 mV/division	1	10	high	low	high	don't care	low	high	low
100 mV/division	1	20	high	low	high	don't care	low	low	high
200 mV/division	40	1	low	high	low	don't care	high	high	high
500 mV/division	40	2.5	low	high	low	don't care	high	low	high
1 V/division	40	5	low	high	low	don't care	low	high	high
2 V/division	40	10	low	high	low	don't care	low	high	low
5 V/division	40	25	low	high	low	don't care	low	low	low

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Trig/Time Register (Write Only)

Writing to Base Address +5 determines the trigger source and trigger level. The bit map of the Trig/Time Register is shown in Table 6-9.

Table 6-10. Bit Map of the Trig/Time Register

Bit Number	Bit Name	Description
D7	TR1	High bit of trigger select
D6	TR0	Low bit of trigger select
D5	Unused	-
D4	Unused	-
D3	Slope	High to trigger on positive polarity
D2	Unused	-
D1	Flag2	Input for microcontroller
D0	Flag1	Input for microcontroller

Table 6-8 shows the bit values corresponding to the trigger source you want to use.

Table 6-11. Trigger-Source Decode Values

Trigger Source	Bit TR1	Bit TR0
Channel B	low	low
Channel A	low	high
External	high	low
Unused	high	high

Set SLOPE high to trigger on a positive (rising) polarity or low to trigger on a negative (falling) polarity.

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FLAG1 and FLAG2 are flags for the microcontroller that help decode the horizontal time scale; these bits are set as shown in Table 6-12.

Table 6-12. Flag Values Corresponding to the Horizontal Time Scale

Horizontal Time Scale	Bit Flag2	Bit Flag1
200 ns/division	low	low
500 ns/division	low	high
1 µs/division	high	low
2 µs/division	high	high
5 µs/division	low	low
10 µs/division	low	high
20 µs/division	high	low
50 µs/division	high	high
100 µs/division	low	low
200 µs/division	low	high
500 µs/division	high	low
1 ms/division	high	high
2 ms/division	low	low
5 ms/division	low	high
10 ms/division	high	low
20 ms/division	high	high
50 ms/division	low	low
100 ms/division	low	high
200 ms/division	high	low
500 ms/division	high	high

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Reset Register (Read/Write)

Base Address +6 corresponds to the Reset register.

Writing to the Reset Register stops the onboard oscillator from clocking the microcontroller and raises a reset line on the microcontroller.

Reading the Reset Register clears the onboard reset line.

Status Register (Read/Write)

Base Address + 7 corresponds to the Status register.

The Status register uses four bits, which can be read or written. The bit map of the Status register is shown in Table 6-13.

Table 6-13. Bit Map of the Status Register

Bit Number	Write Description	Read Description
D7	Unused	Unused
D6	Unused	Unused
D5	Unused	Unused
D4	Unused	Unused
D3	Unused	AWAITING_TRIGGER (low)
D2	SAM_A (high)	LOAD_ADD (low)
D1	SAM_B (high)	START (low)
D0	CLR_MEM_ADD (high)	DONE (low)

Status bits are active-low when read and active-high when written. The DONE bit indicates that the onboard microcontroller is not active and, therefore, is not using the onboard data bus. The other registers of the board can be written to or read from only when the DONE bit is low.

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Note: The onboard data bus is shared by the onboard microcontroller and the computer. To prevent contentions on the bus, interlock hardware prevents the computer from accessing the bus while the DONE bit of the Status register is high, indicating that the microcontroller is active. Nothing prevents you from writing or reading any of the registers while the DONE bit is high, however, only reading the Status register and writing to the Reset register are significant.

When the LOAD_ADD bit is low, the microcontroller is in its reset state and is ready to accept a starting address from the data bus. After clocking in the address, a number of additional clock cycles is required before the controller is ready to start running under onboard control. The program should alternate between clocking the controller and reading the Status register.

When the START bit goes low, the controller is ready to start on the next clock. One more clock causes the controller to start operating internally and the START and DONE bits to go high.

The PCIP-SCOPE requires a trigger to start data acquisition. While waiting for a trigger, the AWAITING_TRIGGER bit is low. The DONE bit goes low when the conversion is completed.

Only one of the SAM_A and SAM_B bits should be written high. Writing both bits high will lead to an indeterminate condition. Normally SAM_A is written high, indicating that you want to sample Channels A and B or Channel A only. If you want to sample Channel B only, SAM_B should be written high.

Writing high to the CLR_MEM_ADD bit causes the memory address counter to reset to zero.

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Programming Sequence Using the Registers

To program the board, use the following sequence:

1. Initialize the controller
2. Initialize the board parameters
3. Perform data acquisition
4. Read data from onboard memory
5. Repeat data acquisition
6. Reinitialize the controller

These steps are described in detail in the following subsections.

Step 1. Initialize the Controller

When the DONE bit of the Status register is high, the computer cannot clock the controller chip or access the data bus. You can seize control of the PCIP-SCOPE by initializing the controller.

To initialize the controller, perform the following procedure at power up; to abort an acquisition, perform this procedure any time:

1. Write any value to Base Address +6 (Reset register).

   This causes the controller to receive its clocks from writes to the Clock Controller register (rather than from the 20 MHz oscillator) and asserts the Reset input of the controller.

2. Write any eight values to Base Address +1 (Clock Controller register).

   Clocking the controller eight times with Reset asserted causes the controller to go to a known state.

3. Read Base Address +6 (Reset register; the read value is not significant).

   This causes the Reset input to the controller to be unasserted.

4. Read Base Address +7 (Status register).
5. Logically AND the Status result with 5 (that is, look for the LOAD_ADD and DONE bits of the Status register to be low).

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6. *If the result equals 0,* skip the remaining steps; you are now ready to initialize the board parameters, as described in the next section.

   If the result does not equal 0, write any value to Base Address +1 (Clock Controller register) and read Base Address +7 (Status register) again. Writes to the Clock Controller register clock the controller chip to the state where its DONE and LOAD_ADD outputs are low.

7. *If the result still does not equal 0,* write any value to Base Address +1 (Clock Controller register) and read Base Address +7 (Status register) up to five times until the result is 0.

Note: Be sure to stop when the AND result is 0 because an additional write to the Clock Controller register causes the LOAD_ADD bit of the Status register to go high again.

---

8. *If, after five repetitions, the result is still not 0,* repeat steps 1 to 8.

   Two or more failures of the overall sequence to achieve the low LOAD_ADD and DONE bits of the Status register indicate a board failure; refer to Chapter 5 for troubleshooting information.

Step 2. Initialize the Board Parameters

The DONE bit of the Status register must be low in order to initialize the board parameters. The initialization information written to the Trigger Level, Channel_A, Channel_B, and Trig/Time registers is latched and need not be rewritten for each acquisition unless you want to change these settings.

To initialize the board parameters, perform the following procedure:

1. Set the trigger level by writing a value of 0 to 255 to Base Address +2 (Trigger Level register).

   A value of 255 corresponds to the maximum positive value (4 x voltage/division for an internal source or 5 V for an external source); 0 corresponds to the most negative value (– 4 x voltage/division for an internal source or –5 V for an external source); 127 corresponds to a value of 0.

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2. Set up the sensitivity of Channel A by writing the appropriate value to Base Address +3 (Channel_A register). Refer to Table 6-4 on page 6-5 to choose a value. If you are not using Channel A, write 0 to Base Address +3.
3. Set up the sensitivity of Channel B by writing the appropriate value to Base Address +4 (Channel_B register). Refer to Table 6-9 on page 6-9 to choose a value. If you are not using Channel B, write 0 to the Channel_B register.
4. Set up the trigger and time base by writing the appropriate value to Base Address +5 (Trig/Time register). Refer to Table 6-10 on page 6-10 to choose a value.

Step 3. Perform Data Acquisition

Once set up for an acquisition, the board waits for a trigger signal to start the onboard 20 MHz oscillator; the oscillator acts as the clock that causes the control circuit to step through the complete acquisition sequence, including acquiring data with the ADC and clocking the data from the ADC over the PCIP-SCOPE data bus to the memory chip. A counter addresses the memory chip and is incremented by the controller following each transfer; therefore, the next transfer goes to a new memory location.

If a trigger source is not present, the 20 MHz oscillator is off and the PCIP-SCOPE will hang. You can check for this condition by logically ANDing the Status register with 8 (the AWAITING_TRIGGER bit of the Status register). You can force the oscillator on (thus providing a software trigger and allowing the acquisition to proceed) by reading the Clock Controller register; the value read has no significance.

Only one trigger is required for time scales of 100 µs and longer because Channel B is acquired in chopped mode. For the 5µs/division to 50 µs/division time scale (alternate mode), one trigger is required for each channel acquired. For the 2 µs/division and shorter time scales (interlace mode), multiple triggers are required for each channel.

Note: Depending on the number of triggers required, the PCIP-SCOPE can hang more than once during data acquisition.

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To perform data acquisition, perform the following procedure:

1. Initialize the memory addressing counter and the source channel:
   - *To acquire data from Channel B only*, write 3 to Base Address +7 (Status register).
   - *To acquire data from Channel A only or from Channels A and B*, write 5 to Base Address +7 (Status register). Note that if you are acquiring data from both channels, the controller switches the multiplexer at the appropriate time.
2. Initialize the acquisition sequence:

Note: The LOAD_ADD bit of the Status register must be low and will go high after this write. This is the only step where the value written to the Clock Controller register is significant.

   - Write a value (3 through 12) from Table 6-14 to Base Address +1 (Clock Controller register). The value depends on the horizontal time scale and whether you are acquiring data from one channel or both channels.

     Note that on the 5 µs/division time scale, acquisitions are made at the maximum 20 MHz rate (every 50 ns). For longer time scales, the controller counts down the clocks so that acquisitions are made less frequently. For shorter time scales, acquisitions are made on multiple repetitions of the signal so that a faster effective sampling rate is achieved. The control sequence depends on the time scale and whether data from one or two channels is acquired.

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Table 6-14. Values to Write to the Clock Controller Register

Acquisition Mode	Horizontal Time Scale	Sampling Rate	Value to Write if Acquiring One Channel	Value to Write if Acquiring Two Channels
Interlace Mode	200 ns/division	500 MHz (2 ns)	3	4
	500 ns/division	200 MHz (5 ns)	3	4
	1 µs/division	100 MHz (10 ns)	3	4
	2 µs/division	50 MHz (20 ns)	3	4
Alternate Mode	5 µs/division	20 MHz (50 ns)	5	6
	10 µs/division	10 MHz (100 ns)	5	6
	20 µs/division	5 MHz (200 ns)	5	6
	50 µs/division	2 MHz (500 ns)	5	6
Chopped Mode	100 µs/division	1 MHz (50 ns)	7	8
	200 µs/division	500 kHz (2 µs)	7	8
	500 µs/division	200 kHz (5 µs)	7	8
	1 ms/division	100 kHz (10 µs)	7	8
	2 ms/division	50 kHz (20 µs)	9	10
	5 ms/division	20 kHz (50 µs)	9	10
	10 ms/division	10 kHz (100 µs)	9	10
	20 ms/division	5 kHz (200 µs)	9	10
	50 ms/division	2 kHz (500 µs)	11	12
	100 ms/division	1 kHz (1 ms)	11	12
	200 ms/division	500 Hz (2 ms)	11	12
	500 ms/division	200 Hz (5 ms)	11	12

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3. Start data acquisition:
   - Read Base Address +7 (Status register).
   - Logically AND the result of the Status register with 2 (if the START bit in the Status register is low) or 3 (if the DONE bit in the Status register is also low) and look for 0.
   - *If the result is not 0,* write any value to Base Address +1 (Clock Controller register) and check the Status register again.

     Note that each write to the Clock Controller register (with "DONE" low) clocks the controller chip; when the controller is clocked with the LOAD_ADD bit low, the controller reads the data and raises its LOAD_ADD output. The value read by the controller causes the controller to select the acquisition sequence appropriate for the specified situation.
   - Repeat writing to the Clock Controller register and reading the Status register until the START bit of the Status register goes low.
   - When the START bit of the Status register goes low, write once more to Base Address +1 (Clock Controller register).

     The acquisition will begin and the DONE bit of the Status register will go high (at least momentarily).
4. Wait for data acquisition to end by reading Base Address +7 (Status register) and logically ANDing with 1 (check that the DONE bit of the Status register is low) until 0 is obtained.

   When the DONE bit of the Status register goes low, the acquisition is finished and the computer can read the results from onboard memory, as described in the following section.

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Step 4. Read Data from Onboard Memory

The computer can read data from the PCIP-SCOPE only when the DONE bit of the Status register is low. To read data from onboard memory, perform the following procedure:

1. Initialize the memory addressing counter to the first memory location by writing 1 to Base Address +7 (Status register).
2. Read the desired number of bytes (up to 2048) by reading Base Address + 0 (Memory register).

   A value of 0 to 255 is returned: 255 corresponds to the maximum positive value (4 x volts/division), 0 to the most negative value (–4 x volts/division), and 127 corresponds 0.

   Note that each time the Memory register is read, the counter is automatically incremented so that the next read accesses the next acquired value.

Once the data is read, you can repeat the data acquisition sequence by following the procedure in the next section.

Step 5. Repeat Data Acquisition

To repeat data acquisition, perform the following procedure:

1. Logically AND the last read of the Status register with 5 (LOAD_ADD and DONE bits of the Status register are low) and test for 0.
2. *If the result is 0*, reset the memory addressing counter and the source channel:
   - *To acquire data from Channel B only*, write 3 to Base Address +7 (Status register).
   - *To acquire data from Channel A only or from Channels A and B*, write 5 to Base Address +7 (Status register).
3. *If the result is not 0*, reinitialize the controller as described in the next subsection.

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Step 6: Reinitialize the Controller

To complete the data acquisition sequence, additional controller chip clock pulses have to be supplied by writing to the Clock Controller register. The value of the data written is unimportant; the number of clocks required depends on the data acquisition sequence.

To reinitialize the controller, perform the following procedure:

1. Write any value to Base Address +6 (Reset register).

   This causes the controller to receive its clocks from writes to the Clock Controller register (rather than from the 20 MHz oscillator) and asserts the Reset input of the controller.

2. Write any eight values to Base Address +1 (Clock Controller register).

   Clocking the controller eight times with Reset asserted causes the controller to go to a known state.

3. Read Base Address +6 (Reset register; the read value is not significant).

   This causes the Reset input to the controller to be unasserted.

4. Read Base Address +7 (Status register).

5. Logically AND the Status result with 5 (that is, look for the LOAD_ADD and DONE bits of the Status register to be low).

6. *If the result is 0 and the board settings are the same*, continue to perform data acquisition by following the procedure on page 6-16.

   If the result is 0 and the board settings are different, reinitialize the board parameters by following the procedure on page 6-15, then continue data acquisition by following the procedure on page 6-16.

   If the result does not equal 0, write any value to Base Address +1 (Clock Controller register) and read Base Address +7 (Status register) again. Writes to the Clock Controller register clock the controller chip to the state where its DONE and LOAD_ADD outputs are low.

7. *If the result still does not equal 0*, write any value to Base Address +1 (Clock Controller register) and read Base Address +7 (Status register) up to five times until the result is 0.

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Note: Be sure to stop when the AND result is 0 because an additional write to the Clock Controller register causes the LOAD_ADD bit of the Status register to go high again.

8. *If, after five repetitions, the result is still not 0*, repeat steps 1 to 8.

   Two or more failures of the overall sequence to achieve the low LOAD_ADD and DONE bits of the Status register indicate a board failure; refer to Chapter 5 for troubleshooting information.

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A

Specifications

This appendix contains the specifications for the PCIP-SCOPE board.

Table A-1. Vertical Input Specifications

Feature	Specification
Maximum input magnitude	175 V (for the 5 mV/division sensitivity) Below 1 kHz (combined AC and DC) (40 x Time Scale over Frequency)
Bandwidth	With DC Coupling: DC to 10 MHz (using 10:1 probes) With AC Coupling: 10 Hz to 10 MHz (using 10:1 probes)
Overshoot	< 5%
Risetime	< 40 ns
Input impedance	1 MΩ shunted by 40 pF (dependent on probe used)
Vertical resolution	8 bits

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Table A-1. Vertical Input Specifications (cont.)

Feature	Specification
Accuracy	1% of full scale
Vertical sensitivity[1]	Vertical range
5.0 V/division	± 20.0 V
2.0 V/division	± 8.0 V
1.0 V/division	± 4.0 V
500.0 mV/division	± 2.0 V
200.0 mV/division	± 800.0 mV
100.0 mV/division	± 400.0 mV
50.0 mV/division	± 200.0 mV
20.0 mV/division	± 80.0 mV
10.0 mV/division	± 40.0 mV
5.0 mV/division	± 20.0 mV

Notes

[1] Determined with a 1:1 probe and with the software set in the vertical position. If you are using a 10:1 probe, multiply by 10.

Table A-2. Horizontal Input Specifications

Feature	Specification
Number of samples	Dual channel mode: 1024 samples/channel Single channel mode: 2048 samples/channel
Sample rate	Maximum: 20 MHz Minimum: 50 ns

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Table A-3. Horizontal Sweep Specifications

Time Scale	Sweep Time[1]	Sample Period[2]	Sample Mode[3]
200 ns/division	2 µs	2 ns	Interlace
500 ns/division	5 µs	5 ns	Interlace
1.0 µs/division	10 µs	10 ns	Interlace
2.0 µs/division	20 µs	20 ns	Interlace
5.0 µs/division	50 µs	50 ns	Alternate
10.0 µs/division	100 µs	100 ns	Alternate
20.0 µs/division	200 µs	200 ns	Alternate
50.0 µs/division	500 µs	500 ns	Alternate
100.0 µs/division	1 ms	1 µs	Chopped
200.0 µs/division	2 ms	2 µs	Chopped
500.0 µs/division	5 ms	5 µs	Chopped
1 ms/division	10 ms	10 µs	Chopped
2 ms/division	20 ms	20 µs	Chopped
5 ms/division	50 ms	50 µs	Chopped
10 ms/division	100 ms	100 µs	Chopped
20 ms/division	200 ms	200 µs	Chopped
50 ms/division	500 ms	500 µs	Chopped
100 ms/division	1 s	1 ms	Chopped
200 ms/division	2 s	2 ms	Chopped
500 ms/division	5 s	5 ms	Chopped

Notes

[1] Sweep time is defined as the time scale multiplied by 10 divisions.
[2] Sample time is defined as the time between samples.
[3] Sample mode is defined as either interlace mode (repetitive waveforms only between 200 ns/division to 2 µs/division), chopped mode (samples acquired from both channels in 500 ns), or alternate mode (500 ns delay between channels).

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Table A-4. Trigger Specifications

Feature	Specification
Internal trigger	Access: Channel A, B, or External Trigger BNC connector Polarity: Positive or Negative Level: ±Full-scale (8-bit resolution) Delay to first sample: 150 ns maximum
External trigger	Access: External Trigger BNC connector Maximum value: ±25 V Coupling: DC Polarity: Positive or Negative Level: ±5 V (8-bit resolution) Input resistance: 10 kΩ maximum

Table A-5. Power Specifications

Feature	Specification
+5 V	1.45 A typical; 1.8 A maximum
+12 V	315 mA typical; 425 mA maximum
–12 V	185 mA typical; 235 mA maximum

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B

CE Information

Note: Products that contain the CE mark are certified to meet European EMC directive 89/336 EEC. If this directive is not of importance to your application, please disregard the information in this document.

Keithley MetraByte certifies that this product has been tested and found to be in compliance with the EMC directive and relevant harmonized standards.

This document describes the limitation of certification, the declaration of conformity, and the cabling required for the CE configuration.

Limitation of Certification

This certification applies only to the operation of the product (with specified cables and accessories) in the stated configuration and under the stated operational and environmental specifications. Any modification, misuse, or improper or inadequate maintenance of the product by the user voids this certification.

Any deviation from the specific configuration may cause emissions or susceptibility not within the allowed limits required by the stated directive. It is the user's responsibility to demonstrate and maintain compliance with the directive and standards.

Please read the next section, "Declaration of Conformity," for the specific testing configuration for this product. Consult the Keithley Instruments GMBH office (European importer) or Technical Support in Taunton, MA, USA, for further information regarding the exact configuration details and testing.

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Declaration of Conformity

Application of Council Directive(s)	89/336/EEC
Standard(s) to which Conformity is Declared	EN50081-1, EN50082-1
Manufacturer's Name	Keithley MetraByte
Importer's Name	Keithley Instruments GMBH
Importer's Address	Landsberger Str.65 D-82110 Germering, Munich
Type of Equipment	Data Acquisition Plug-in Boards
Model Numbers	PCIP-SCOPE and C-BMM-5 cable
Year of Manufacture	1996

I, the undersigned, hereby declare that the equipment specified above conforms to the above Directive(s) and Standard(s).

Place: Taunton, MA USA

(Signature)

Date: 01 February 1996

Mark Urban
(Name)

Quality Assurance Manager
(Position)

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Cabling Instructions for the CE Configuration

Connect the C-BMM-5 cable to the PCIP-SCOPE, as shown in Figure B-1.

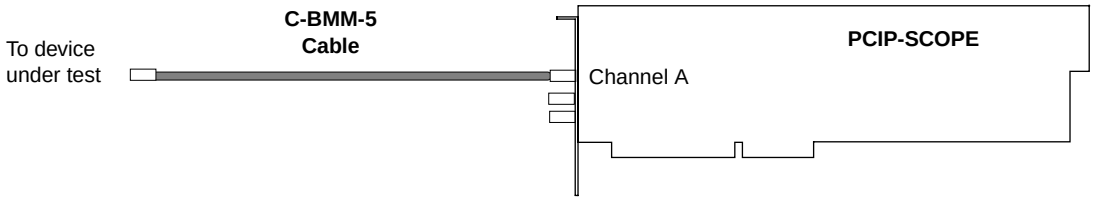


Figure B-1. PCIP-SCOPE CE Configuration

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