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KEYENCE

Laser Displacement Meter

LC series

Technical Manual

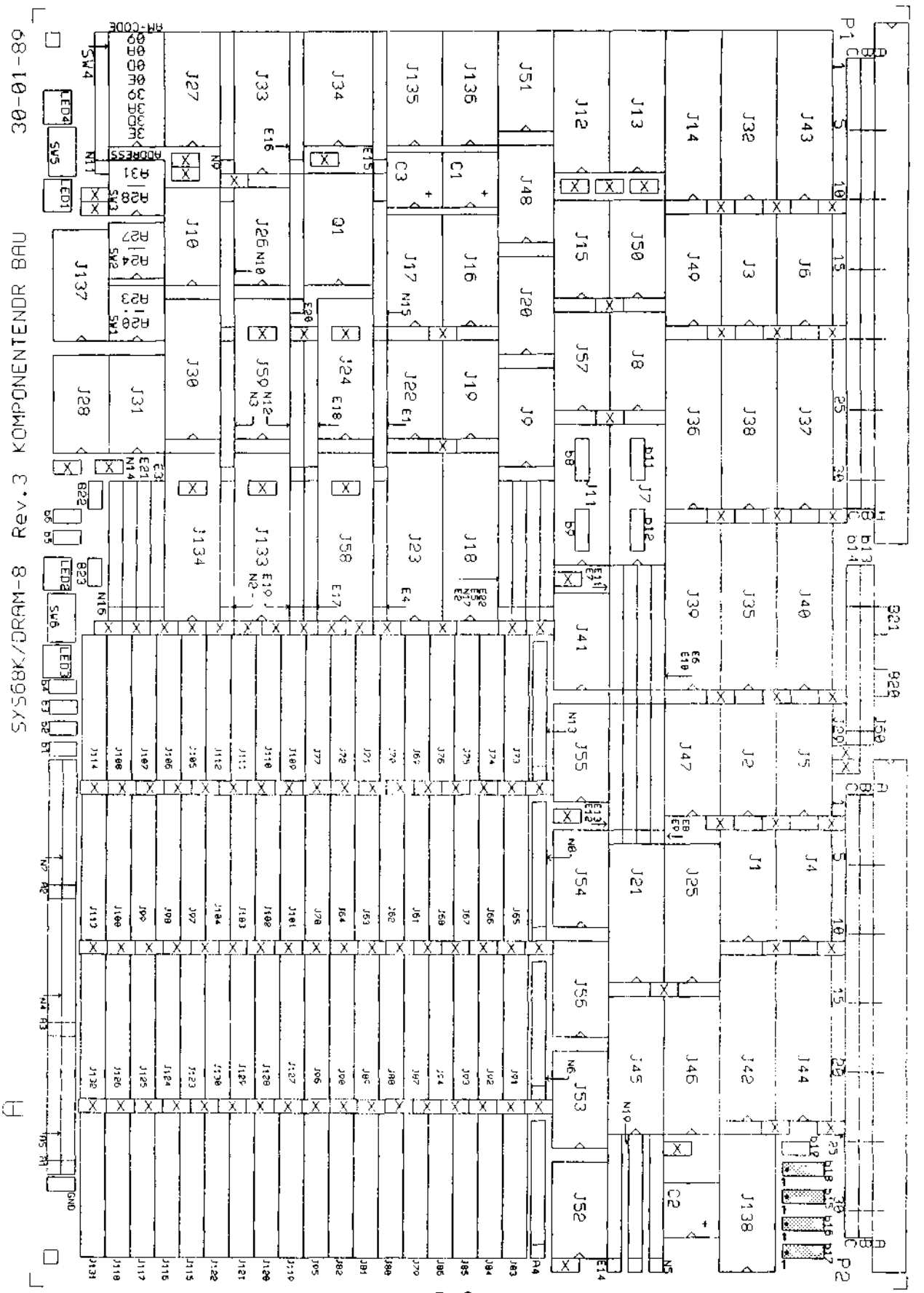
KEYENCE

LC SERIES
TECHNICAL MANUAL

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Figure 5-1: Location Diagram for Power Supply Solder Bridges



5. WIRING OF POWER SUPPLY SOLDER BRIDGES

All solder bridges are wired for use of the board under standard conditions.

The following picture shows the default setting of the power supply bridges. The battery backup option is not installed per default.

Table 5-1: Default Connection of the Power Supply Solder Bridges

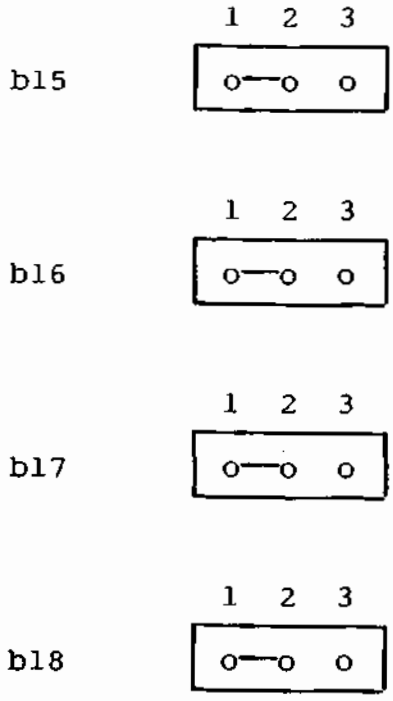
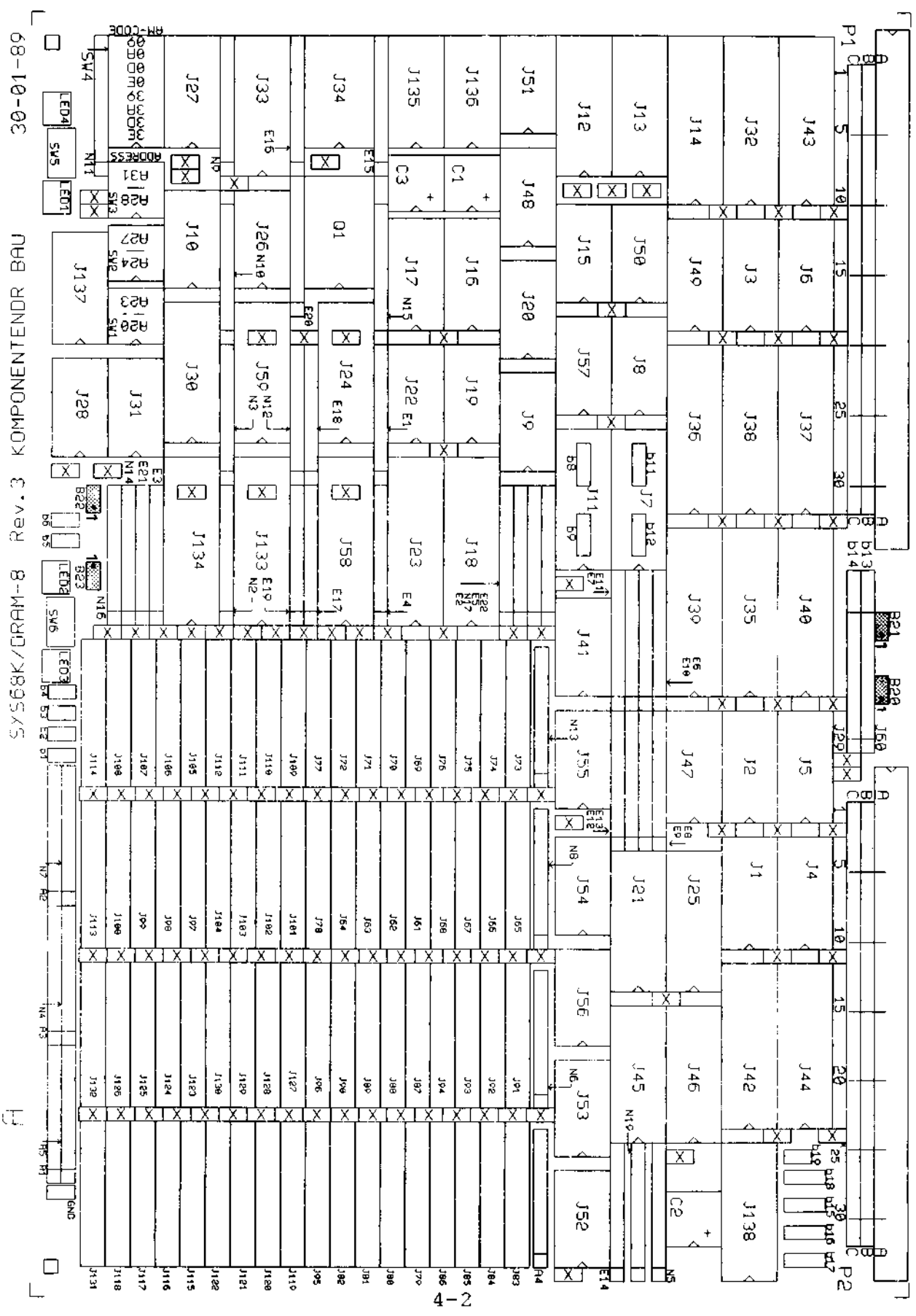


Figure 5-1 shows the location of the power supply solder bridges.

Figure 4-1: Location Diagram of Jumpers B20 to B23



4. JUMPER SETTINGS

Jumper B23 is closed per default.

Jumpers B20, B21 and B22 are open per default.

The reset voltage is set to 4.8V if the jumpers B20 and B21 are open.

Jumper B22 parity check enable is a default condition.

Jumper B23 only exists for DRAM-8A/C/E. This jumper drives a refresh every 15μs for both RAM banks when closed.

The default jumper settings are as shown below:

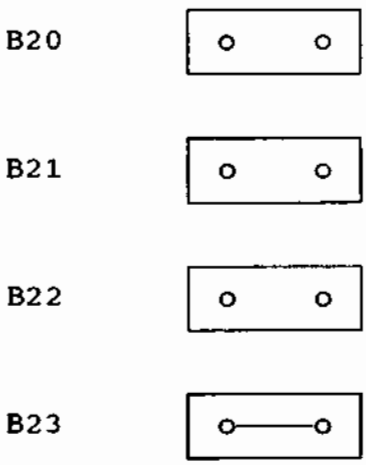


Figure 4-1 shows the location of the jumpers.

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3. DEFAULT ADDRESS RANGE SELECTION

Per default the start address is $00100000 for all types of the DRAM-8x. The following table shows the default end address of the different types of the DRAM-8x.

Table 3-1: Default Address Range

Board	Start Addr.	End Addr.
DRAM-8A	$00100000	$002FFFFF
DRAM-8B	$00100000	$004FFFFF
DRAM-8C	$00100000	$008FFFFF
DRAM-8D	$00100000	$010FFFFF
DRAM-8E	$00100000	$020FFFFF

The location of the DIP and Rotary Switches is shown in Figure 2-1.

Figure 2-2 shows the default DIP-Switch (AM-Code) and Rotary Switch (Start address) settings.

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Figure 2-2: Default Switch Setting

The Default Switch Setting consists of:

Start Address: $00100000

Enabled AM-Codes: $09, $0A, $0D, $0E

Observe the diagram below:

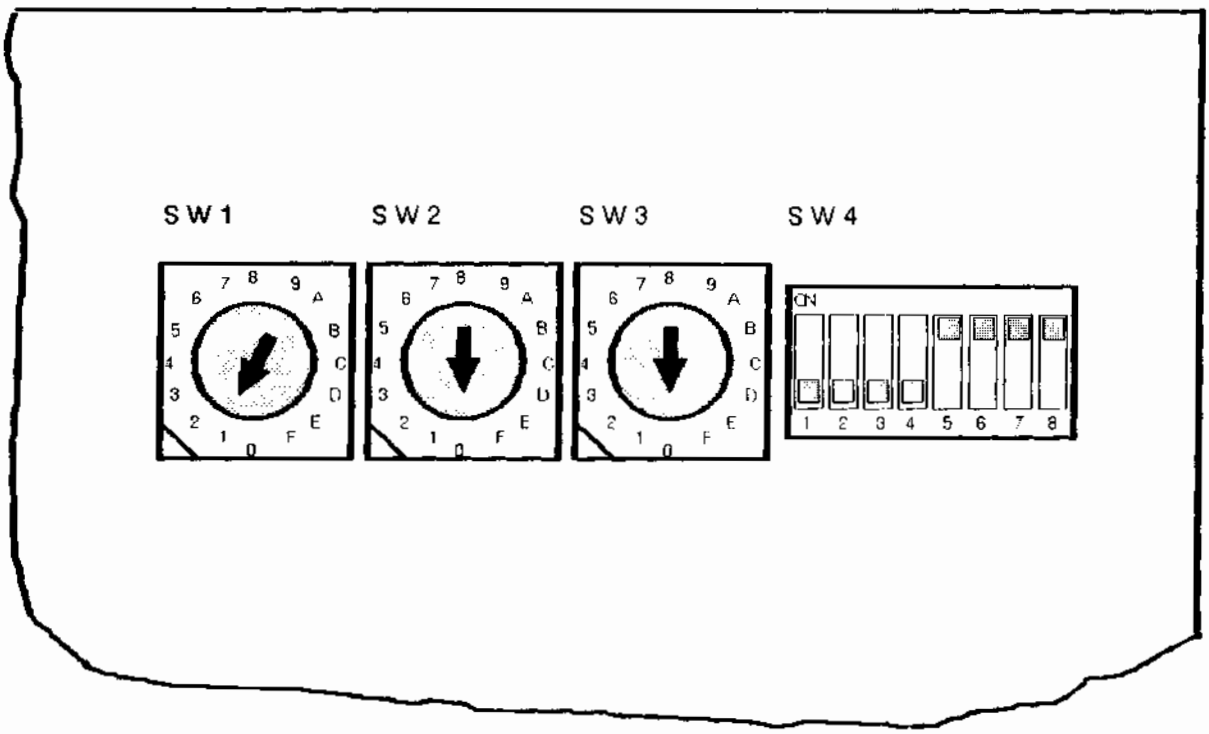
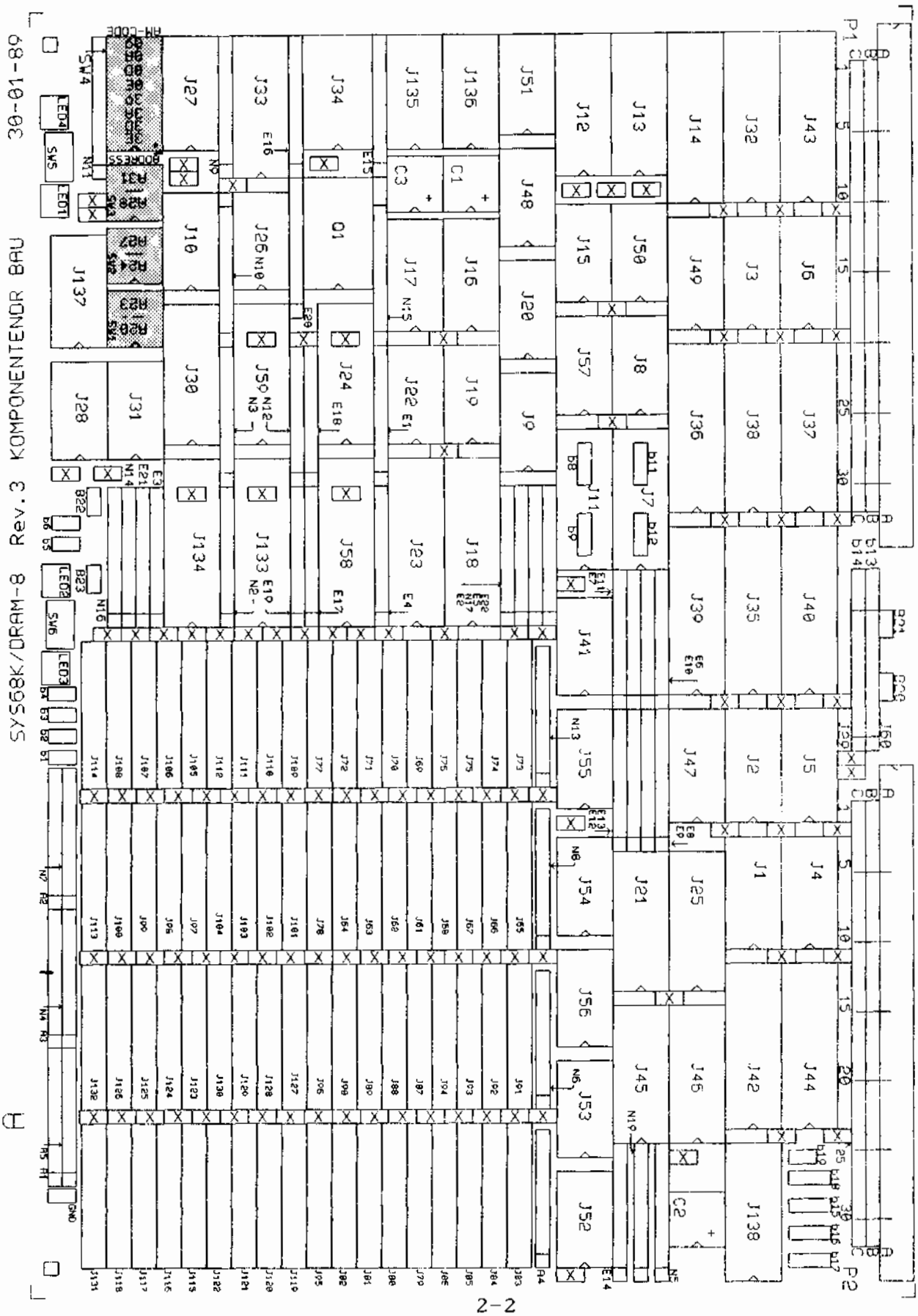


Figure 2-1: Location Diagram of the On-board Switches



2. DEFAULT AM-CODE SELECTION

The following table shows the default enabled AM-Codes.

Table 2-1: Default Enabled AM-Codes

HEX-Code	AM-CODE 543210	FUNCTION	AM-CODE SWITCH-POSITION	DEFAULT
3E	HHHHHL	Standard Supervisory Program Access	SW4-1	OFF
3D	HHHHLH	Standard Supervisory Data Access	SW4-2	OFF
3A	HHHLHL	Standard Non-Privileged Program Access	SW4-3	OFF
39	HHHLLH	Standard Non-Privileged Data Access	SW4-4	OFF
0E	LLHHHL	Extended Supervisory Program Access	SW4-5	ON
0D	LLHHLH	Extended Supervisory Data Access	SW4-6	ON
0A	LLHLHL	Extended Non-Privileged Program Access	SW4-7	ON
09	LLHLLH	Extended Non-Privileged Data Access	SW4-8	ON

Figures 2-1 and 2-2 show the AM-Code switch setting and the location of this switch.

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1. DEFAULT SETUP

Per default the four extended AM-Codes are enabled as well as the parity error check and the start address is switched to $00100000.

Furthermore the power down modules are jumpered at a reset transition voltage of 4.8V and the refresh is pending every 15us.

The address range starts at $00100000 and warrants maximal possible size. The power is wired to a normal VMEbus source.

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DEFAULT JUMPER SETTINGS

APPENDIX I

PRODUCT ERROR REPORT

DEAR CUSTOMER,

WHILE FORCE COMPUTERS HAS ACHIEVED A VERY HIGH STANDARD OF QUALITY IN OUR PRODUCTS AND DOCUMENTATION, WE CONTINUALLY SEEK SUGGESTIONS FOR IMPROVEMENTS.

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SINCERELY

FORCE COMPUTERS, GmbH

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APPENDIX H

LITERATURE REFERENCE

Please refer to the following book for further more detailed information.

VMEbus Specifications and Standards:

2618 S Shannon
Tempe Arizona 85282
(602) 966-5936

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UAT

A MASTER that sends or receives data in an unaligned fashion, or a SLAVE that sends and receives data in an unaligned fashion.

UTILITY BUS

One of the four buses provided by the 1014 backplane. This bus includes signals that provide periodic timing and coordinate the power up and power down of 1014 systems.

WRITE CYCLE

A DTB cycle used to transfer 1, 2, or 4 bytes from a MASTER to a SLAVE. The cycle begins when the MASTER broadcasts an address and address modifier and places data on the DTB. Each SLAVE captures this address and address modifier, and checks to see if it is to respond to the cycle. If so, it stores the data and then acknowledges the transfer. The MASTER then terminates the cycle.

REQUESTOR

A functional module that resides on the same board as a MASTER or INTERRUPT HANDLER and requests use of the DTB whenever its MASTER or INTERRUPT HANDLER needs it.

SERIAL CLOCK DRIVER

A functional module that provides a periodic timing signal that synchronizes operation of the VMSbus. (Although the 1014 specification defines a SERIAL CLOCK DRIVER for use with the VMSbus, and although it reserves two backplane signal lines for use by that bus, the VMSbus protocol is completely independent of the 1014.)

SLAVE

A functional module that detects DTB cycles initiated by a MASTER and, when those cycles specify their participation, transfers data between itself and the MASTER.

SLOT

A position where a board can be inserted into a 1014 backplane. If the 1014 system has both a J1 and a J2 backplane (or a combination J1/J2 backplane) each slot provides a pair of 96-pin connectors. If the system has only a J1 backplane, then each slot provides a single 96-pin connector.

SUBRACK

A rigid framework that provides mechanical support for boards inserted into the backplane, ensuring that the connectors mate properly and that adjacent boards do not make contact with each other. It also guides the cooling airflow through the system, and ensures that inserted boards do not disengage themselves from the backplane due to vibration or shock.

SYSTEM CLOCK DRIVER

A functional module that provides a 16 MHz timing signal on the UTILITY BUS.

SYSTEM CONTROLLER BOARD

A board which resides in slot 1 of a 1014 backplane and has a SYSTEM CLOCK DRIVER, a DTB ARBITER, an IACK DAISY CHAIN DRIVER, and a BUS TIMER. Some also have a SERIAL CLOCK DRIVER, a POWER MONITOR or both.

INTERRUPT HANDLER

A functional module that detects interrupt requests generated by INTERRUPTERS and responds to those requests by asking for STATUS/ID information.

LOCATION MONITOR

A functional module that monitors data transfers over the DTB in order to detect accesses to the locations it has been assigned to watch. When an access occurs to one of these assigned locations, the LOCATION MONITOR generates an on-board signal.

MASTER

A functional module that initiates DTB cycles in order to transfer data between itself and a SLAVE module.

OBO

A SLAVE that sends and receives data 8 bits at a time over D00-D07.

POWER MONITOR MODULE

A functional module that monitors the status of the primary power source to the 1014 system and signals when that power has strayed outside the limits required for reliable system operation. Since most systems are powered by an AC source, the power monitor is typically designed to detect drop-out or brown-out conditions on AC lines.

READ CYCLE

A DTB cycle used to transfer 1, 2, or 4 bytes from a SLAVE to a MASTER. The cycle begins when the MASTER broadcasts address and an address modifier. Each SLAVE captures this address and address modifier, and checks to see if it is respond to the cycle. If so, it retrieves the data from its internal storage, places it on the data bus, and acknowledges the transfer. Then the MASTER terminates the cycle.

READ-MODIFY-WRITE CYCLE

A DTB cycle that is used to both read from, and write to a SLAVE location without permitting any other MASTER to access that location. This cycle is most useful in multiprocessing systems where certain memory locations are used to control access to certain systems resources. (For example, semaphore locations.)

DATA TRANSFER BUS

One of the four buses provided by the 1014 backplane. The DATA TRANSFER BUS allows MASTERS to direct the transfer of binary data between themselves and SLAVES. (DATA TRANSFER BUS is often abbreviated to DTB).

DATA TRANSFER BUS CYCLE

A sequence of level transitions on the signal lines of the DTB that result in the transfer of an address or an address and data between a MASTER and a SLAVE. There are seven types of data transfer bus cycles.

DTB

An acronym for DATA TRANSFER BUS.

FUNCTIONAL MODULE

A collection of electronic circuitry that resides on one 1014 board and works together to accomplish a task.

IACK DAISY CHAIN DRIVER

A functional module which activates the interrupt acknowledge daisy chain whenever an INTERRUPT HANDLER acknowledges an interrupt request. This daisy chain ensures that only one INTERRUPTER will respond with its STATUS/ID when more than one has generated an interrupt request.

INTERRUPT ACKNOWLEDGE CYCLE

A DTB cycle, initiated by an INTERRUPT HANDLER that reads a "STATUS/ID" from an INTERRUPTER. An INTERRUPT HANDLER generates this cycle when it detects an interrupt request from an INTERRUPTER and it has control of the DTB.

INTERRUPT BUS

One of the four buses provided by the 1014 backplane. The INTERRUPT BUS allows INTERRUPTER modules to send interrupt requests to INTERRUPT HANDLER modules.

INTERRUPTER

A functional module that generates an interrupt request on the INTERRUPT BUS and then provides STATUS/ID information when the INTERRUPT HANDLER requests it.

BUS TIMER

A functional module that measures how long each data transfer takes on the DTB, and terminates the DTB cycle if a transfer takes too long. If the MASTER tries to transfer data to or from a nonexistent SLAVE location, it might wait forever. The BUS TIMER prevents this by terminating the cycle.

D08(O)

A SLAVE that sends and receives data 8 bits at a time over D00-D07, or an INTERRUPT HANDLER that receives 8 bit STATUS /IDs over D00-D07, or an INTERRUPTER that sends 8 bit STATUS/IDs over D00-D07.

D08(EO)

A MASTER that sends or receives data 8 bits at a time over either D00-D07 or D08-D15, or A SLAVE that sends and receives data 8 bits at a time over either D00-D07 or D08-D15, or an INTERRUPT HANDLER that receives 8 bit STATUS/IDs over D00-D07, or an INTERRUPTER that sends 8 bit STATUS/IDs over D00-D07.

D16

A MASTER that sends and receives data 16 bits at a time over D00-D15, or A SLAVE that sends and receives data 16 bits at a time over D00-D15, or an INTERRUPT HANDLER that receives 16 bit STATUS/IDs over D00-D15, or an INTERRUPTER that sends 16 bit STATUS/IDs over D00-D15.

D32

A MASTER that sends and receives data 32 bits at a time over D00-D31, or A SLAVE that sends and receives data 32 bits at a time over D00-D31, or an INTERRUPT HANDLER that receives 32 bit STATUS/IDs over D00-D31, or an INTERRUPTER that sends 32 bit STATUS/IDs over D00-D31.

DAISY CHAIN

A special type of 1014 signal line that is used to propagate a signal level from board to board, starting with the first slot and ending with the last slot. There are four bus grant daisy chains and one interrupt acknowledge daisy chain on the 1014.

BACKPLANE (1014)

A printed circuit (PC) board with 96-pin connectors and signal paths that bus the connector pins. Some 1014 systems have a single PC board, called the J1 backplane. It provides the signal paths needed for basic operation. Other 1014 systems also have an optional second PC board called a J2 backplane. It provides the additional 96-pin connectors and signal paths needed for wider data and address transfers. Additional systems have a single PC board which provides the signal conductors and connectors of both the J1 and J2 backplanes.

BACKPLANE INTERFACE LOGIC

Special interface logic that takes into account the characteristics of the backplane: its signal line impedance, propagation time, termination values, etc. The 1014 specification prescribes certain rules for the design of this logic based on the maximum length of the backplane and its maximum number of board slots.

BLOCK READ CYCLE

A DTB cycle used to transfer a block of 1 to 256 bytes from a SLAVE to a MASTER. This transfer is done using a string of 1, 2, or 4 byte data transfers. Once the block transfer is started, the MASTER does not release the DTB until all of the bytes have been transferred. It differs from a string of read cycles in that the MASTER broadcasts only one address and address modifier (at the beginning of the cycle). Then the SLAVE increments this address on each transfer so that the data for the next cycle is retrieved from the next higher location.

BLOCK WRITE CYCLE

A DTB cycle used to transfer a block of 1 to 256 bytes from a MASTER to a SLAVE. The block write cycle is very similar to the block read cycle. It uses a string of 1, 2, or 4 byte data transfers and the MASTER does not release the DTB until all of the bytes have been transferred. It differs from a string of write cycles in that the MASTER broadcasts only one address and address modifier (at the beginning of the cycle). Then the SLAVE increments this address on each transfer so that the next transfer is stored on the next higher location.

BOARD

A printed circuit (PC) board, its collection or electronic components, and either one or two 96-pin connectors that can be plugged into 1014 backplane connectors.

APPENDIX G

GLOSSARY OF VME/1014 TERMS

A16

A type of module that provides or decodes an address on address line A01 through A15.

A24

A type of module that provides or decodes an address on address lines A01 through A23.

A32

A type of module that provides or decodes an address on address lines A01 through A31.

ADDRESS-ONLY CYCLE (ADO)

A DTB cycle that consists of an address broadcast, but no data transfer. SLAVES do not acknowledge ADDRESS-ONLY cycles and MASTERS terminate the cycle without waiting for an acknowledgment.

ARBITER

A functional module that accepts bus requests from REQUESTOR modules and grants control of the DTB to one REQUESTOR at a time.

ARBITRATION

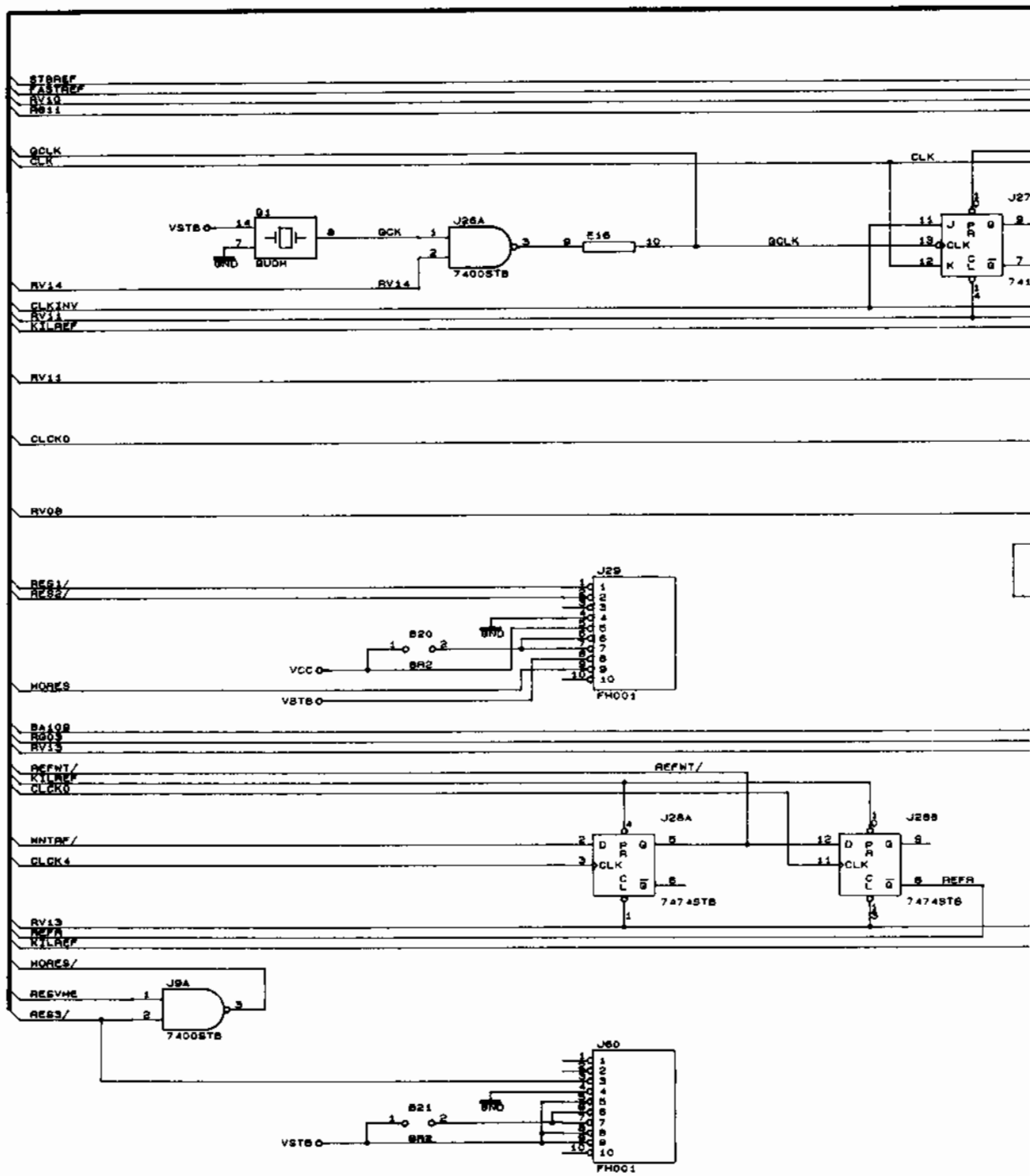
The process of assigning control of the DTB to a REQUESTOR.

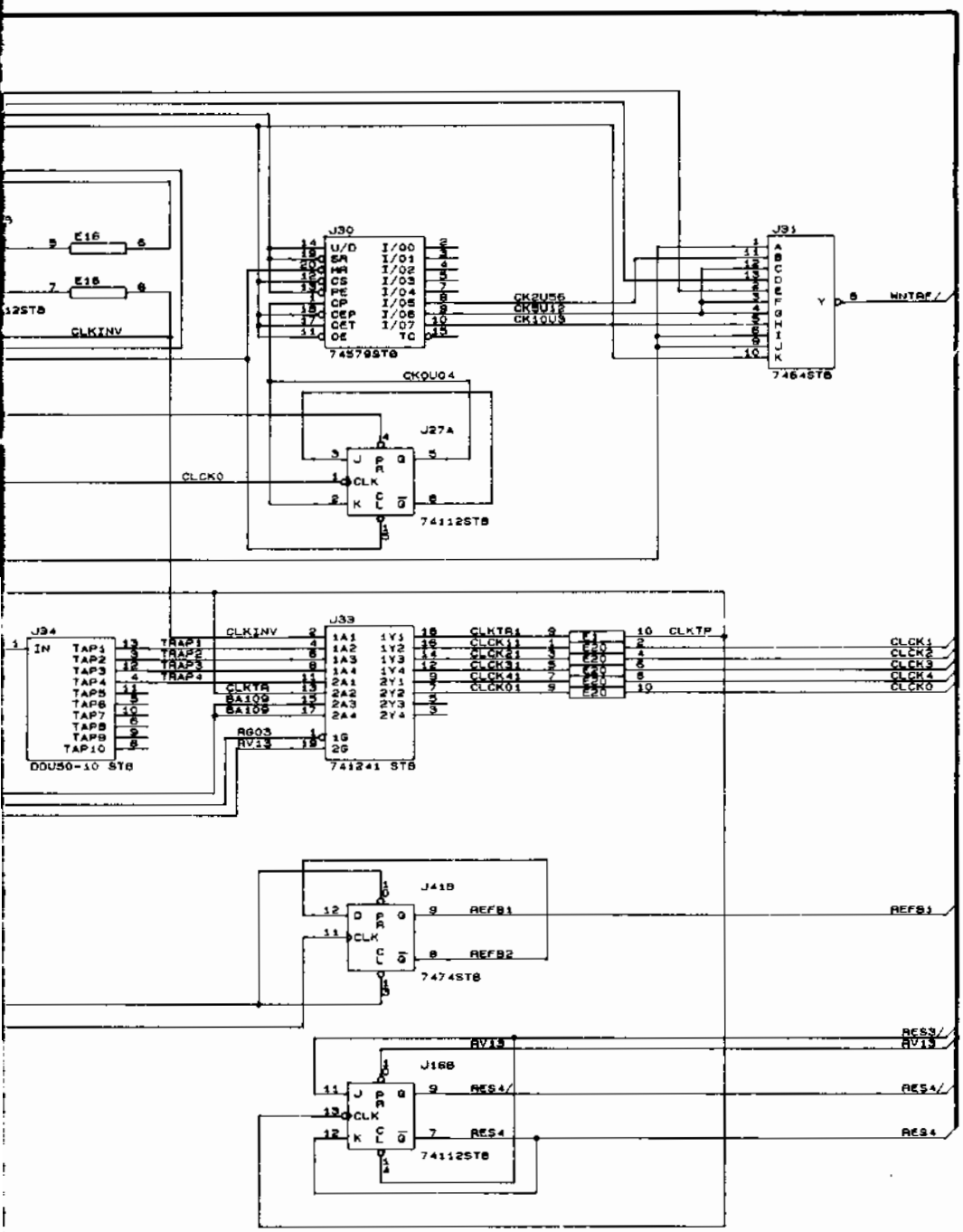
ARBITRATION BUS

One of the four buses provided by the 1014 backplane. This bus allows an ARBITER module and several REQUESTOR modules to coordinate use of the DTB.

ARBITRATION CYCLE

An ARBITRATION CYCLE begins when the ARBITER senses a bus request. The ARBITER grants the bus to a REQUESTOR, which signals that the DTB is busy. The REQUESTOR terminates the cycle by taking away the bus busy signal which causes the ARBITER to sample the bus requests again.


STOREF
FASTREF
RV10
RV11
QCLK
CLK
VSTB
Q1
GND
QUSH
QCK
J26A
7400STB
E16
RV14
CLKINV
RV11
KILREF
CLOCK0
RV08
REG1/
REG2/
J29
B20
B22
VCC
MORES
FH001
BA1Q8
RQQ3
RV13
REFWT/
CLOCK4
J28A
J28B
7474STB
REFA
RV13
MORES/
REGVME
REG3/
J9A
J60
B21
B22



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				FORCE COMPUTERS		
Rev	Aender.-Nr.	Tag	Name			

Benennung

DRAM 8 B/C/D/E REV.3

TIMING GENERATOR
RESET LOGIC

Zeichn.-Nr.

195fo30-0

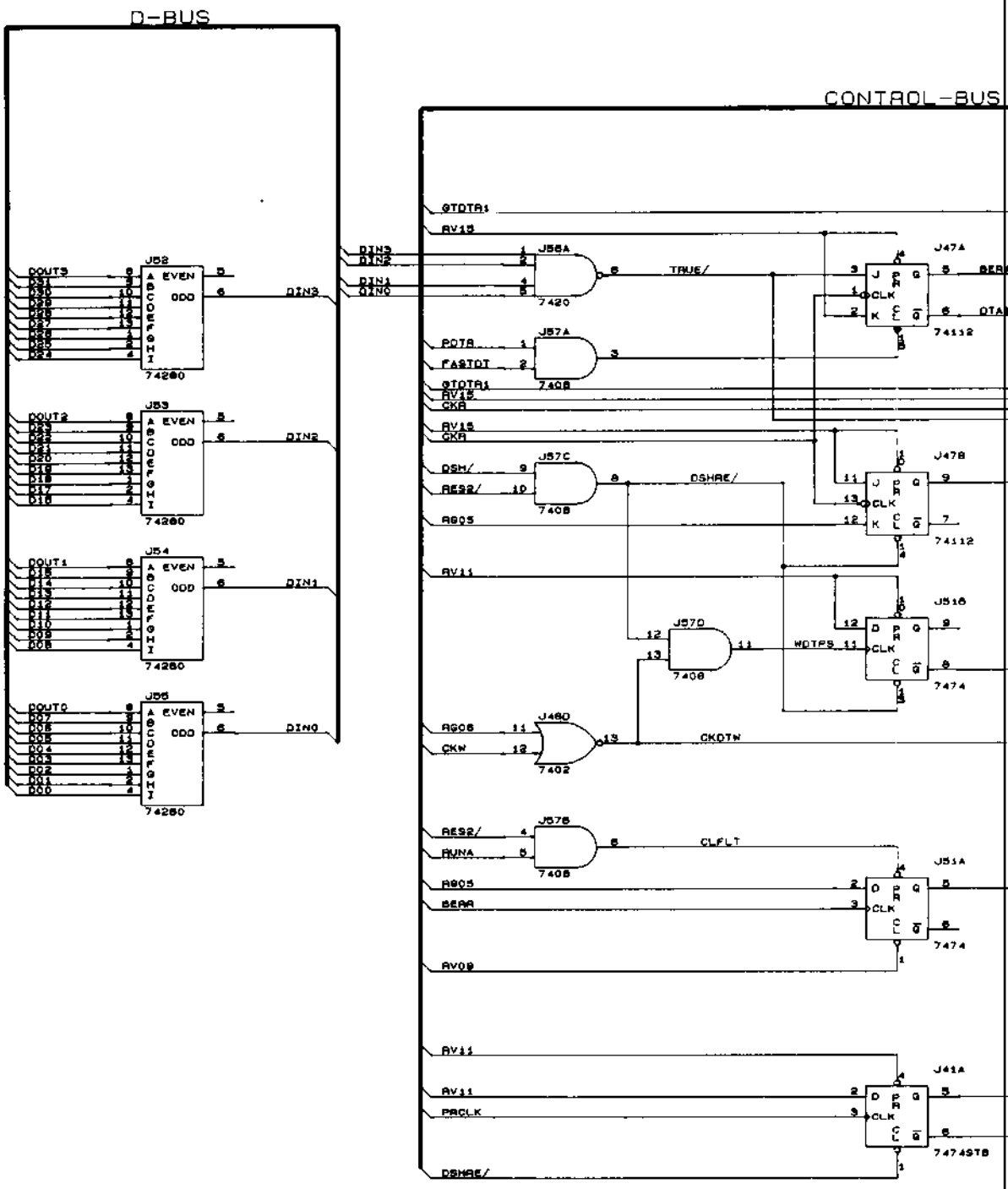
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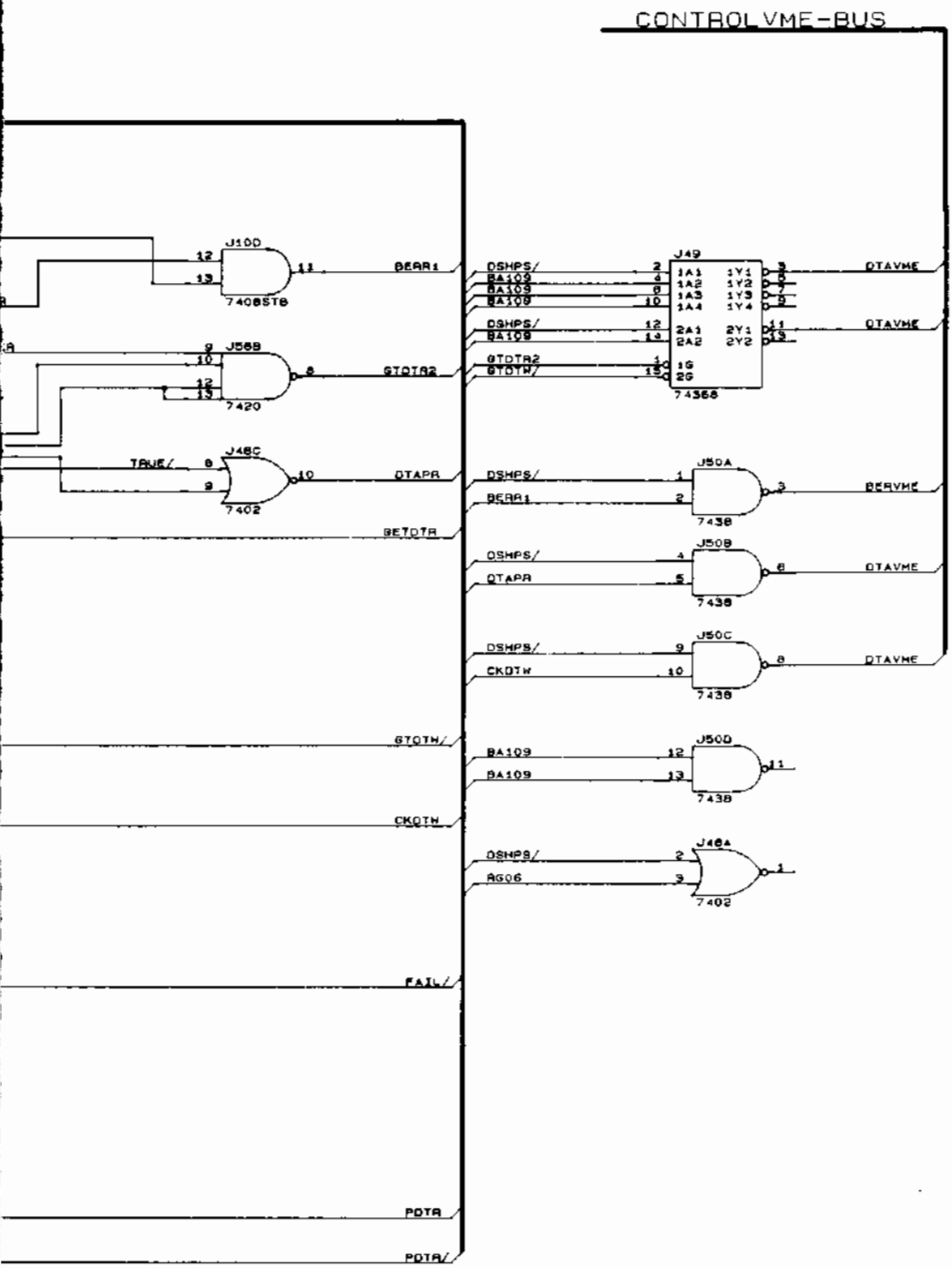
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V.1481

zu Gerast

zu Anlage


D-BUS
CONTROL-BUS
DOUT3
DOUT2
DOUT1
DOUT0
J52
J53
J54
J55
EVEN
ODD
74280
DIN3
DIN2
DIN1
DIN0
@TDTA1
AV15
CKA
J58A
7420
TRUE/
J47A
74112
PDTA
FASTDT
J57A
7408
J57C
DSM/
RES2/
DSHAE/
J47B
A905
AV11
J57D
WDTPS
J51B
7474
A906
CKW
CKDTW
7402
J57B
RUNA
CLFLT
J51A
BEAR
AV09
J41A
PRCLK
7474STB



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				Gepr.		
Rev	Aender.-Nr.	Tag	Name			

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Stand : 07.04 89

Benennung

DRAM 8 B/C/D/E REV.3

PARITY GENERATOR

DTACK*/BERR*- CONTROL

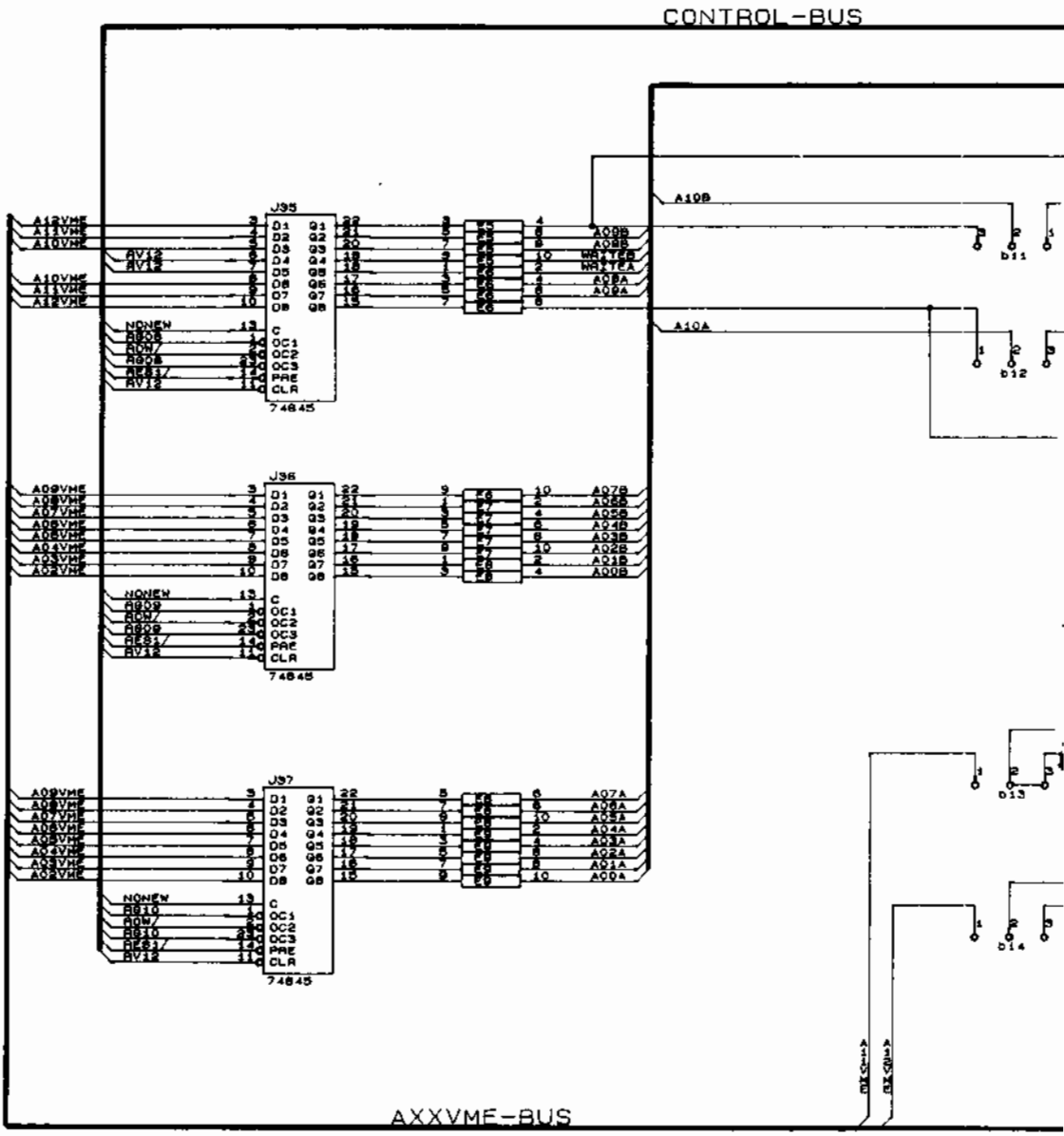
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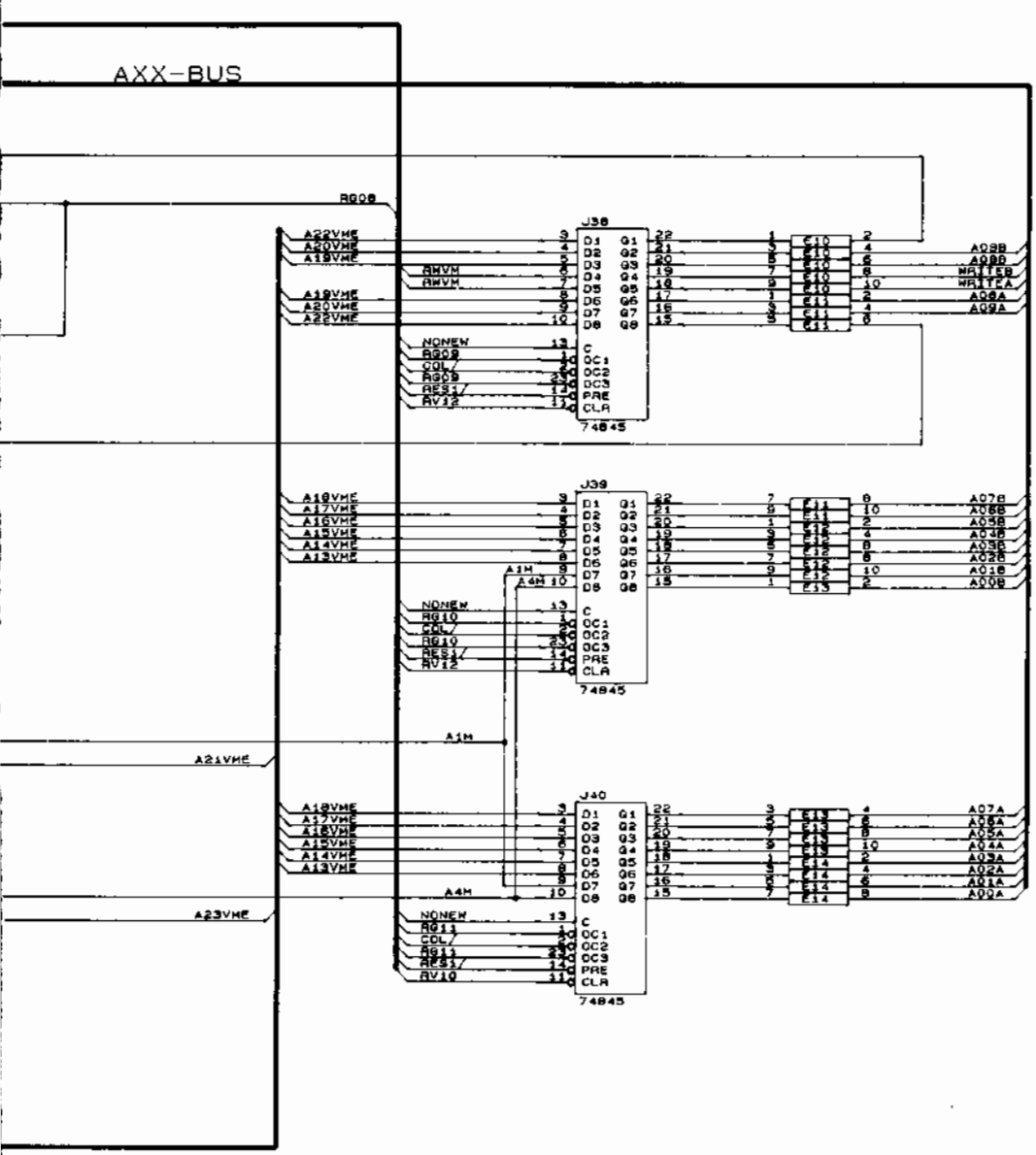
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zu Gerset | zu Anlage


CONTROL-BUS
AXXVME-BUS
J35
J36
J37
74845
A10B
A10A
D11
D12
D13
D14



Stand : 07.04.89

	Tag	Name
Bearb	31.01.89	
Gepr.		

Benennung

DRAM 8 B/C/D/E REV.3

ADDRESS LATCH/MUX

FORCE COMPUTERS

Zeichn.-Nr.

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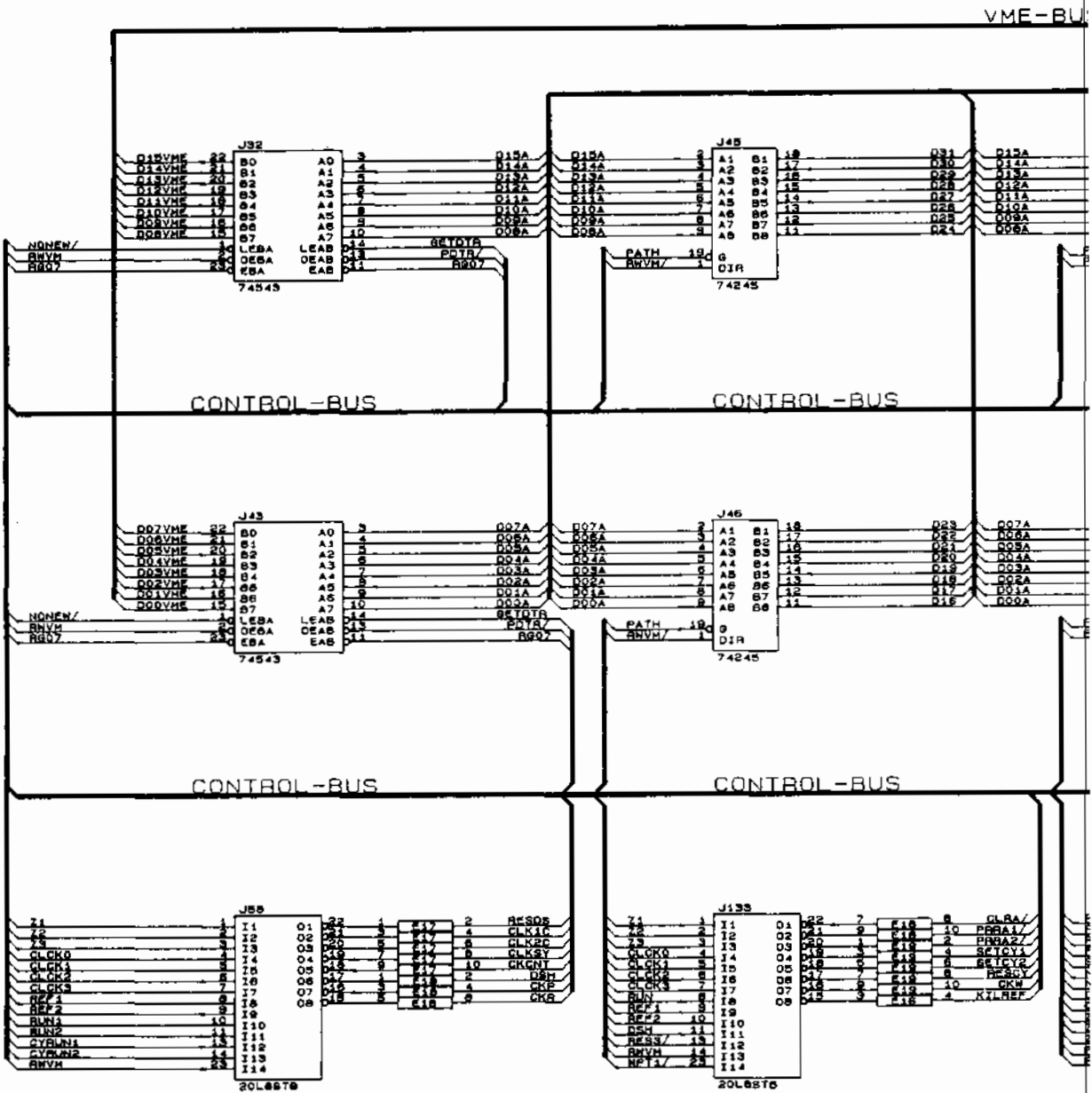
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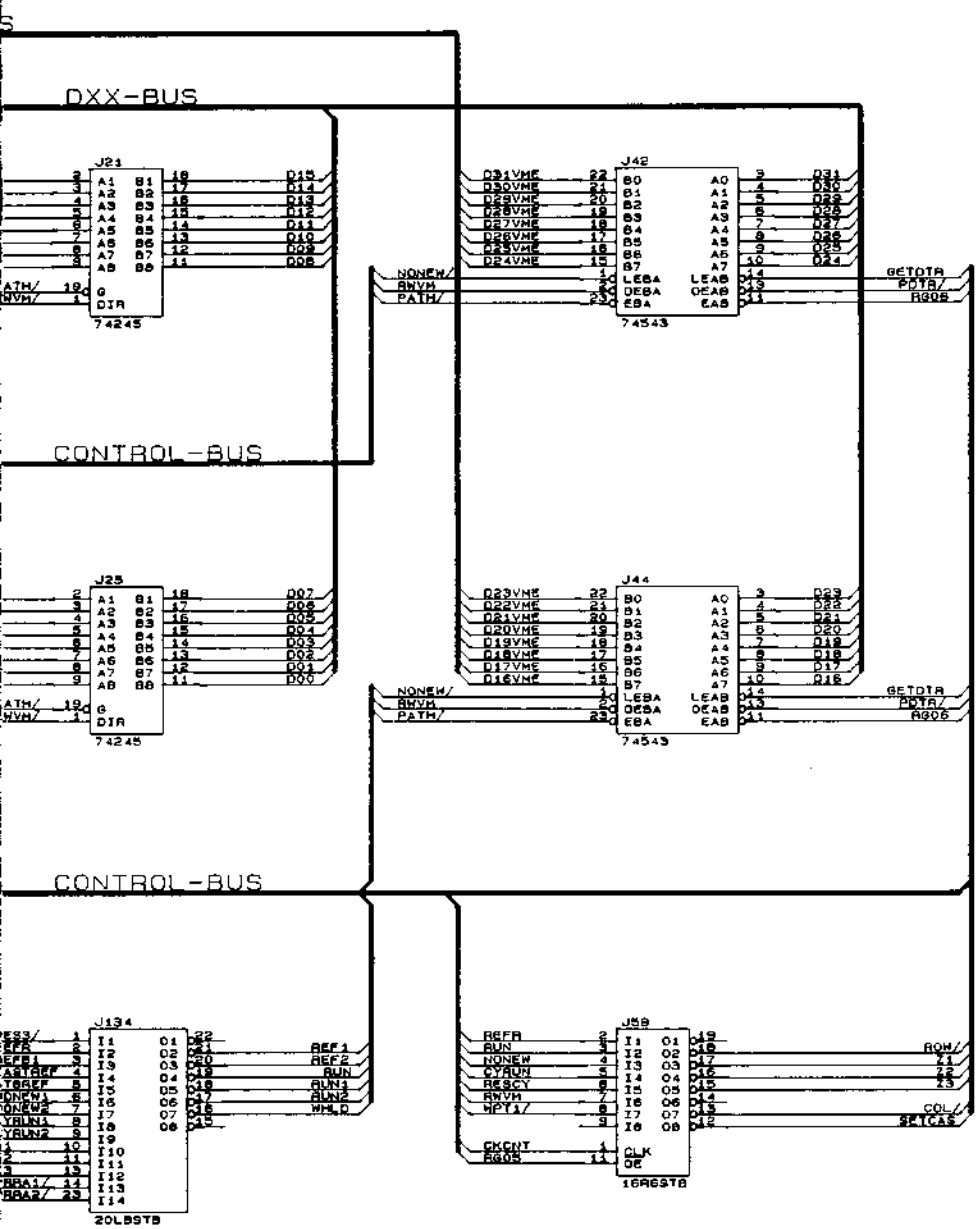
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Rev	Aender.-Nr.	Tag	Name

zu Gerset

zu Anlage


VME-BU
J32
74543
J45
74245
CONTROL-BUS
CONTROL-BUS
J43
74543
J46
74245
CONTROL-BUS
CONTROL-BUS
J58
20L8STD
J133
20L8STD



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				Gepr.		
Rev	Aender.-Nr.	Tag	Name			

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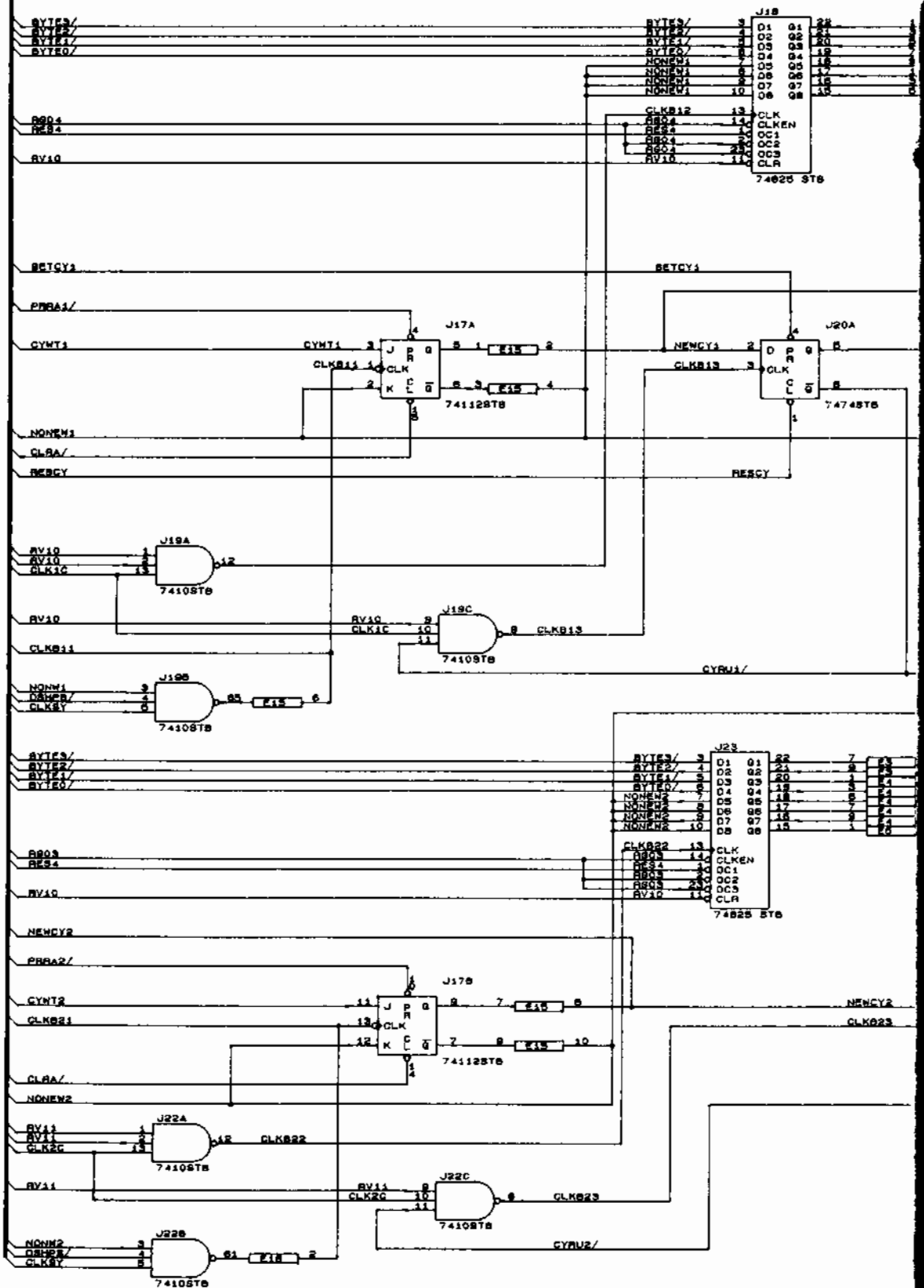
Benennung: DRAM 8 B/C/D/E REV.3
DATA-PATH/REFRESH AND CONTROL LOGIC

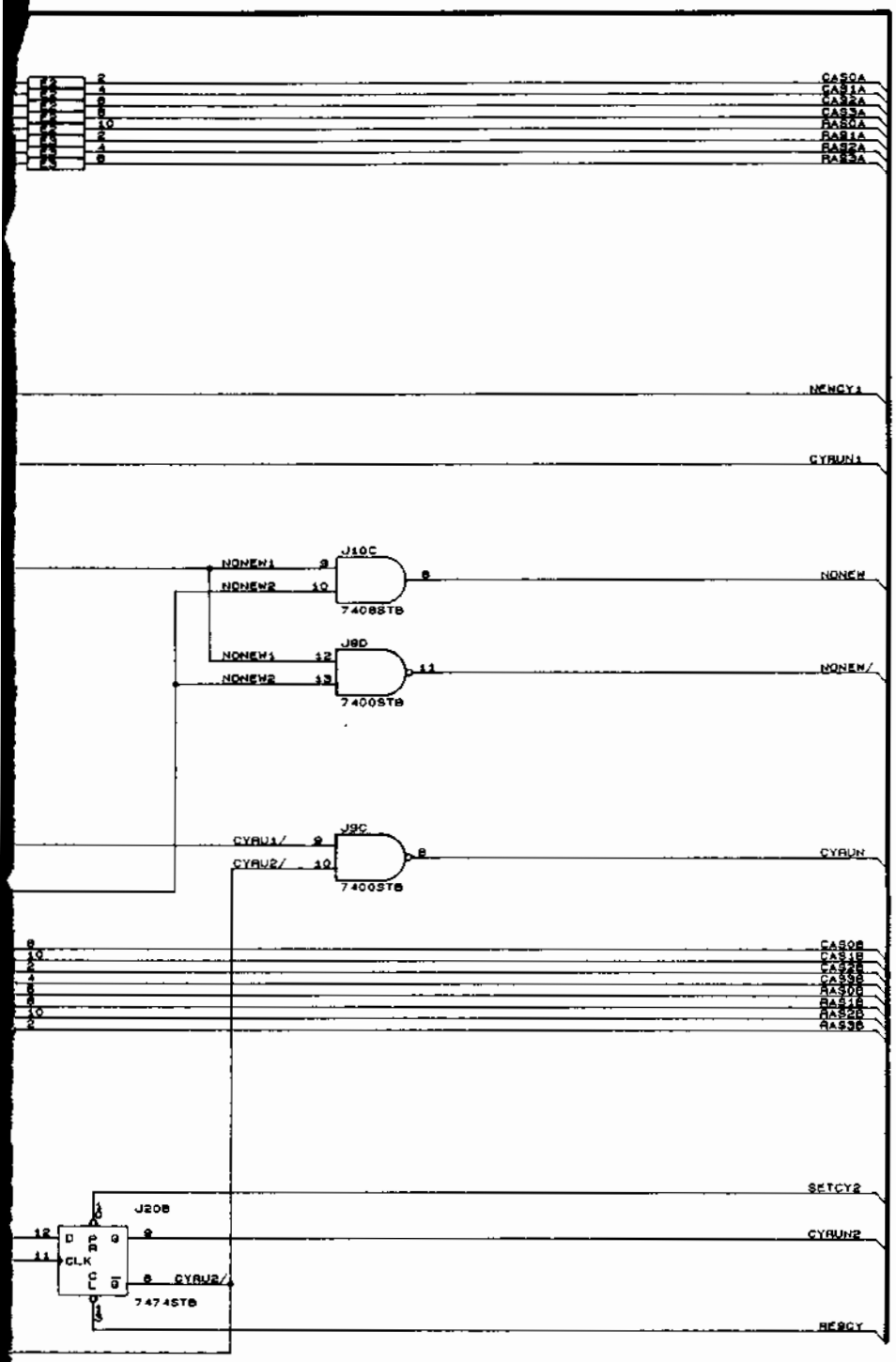
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J18
74825 ST6
J17A
74112ST6
J20A
74745T6
J19A
7410ST6
J19C
7410ST6
J19B
7410ST6
J23
74825 ST6
J17B
74112ST6
J22A
7410ST6
J22C
7410ST6
J22B
7410ST6
BYTE3/
BYTE2/
BYTE1/
BYTE0/
NONEW1
NONEW2
A803
AES4
AV10
AV11
BETCY1
PRBA1/
CYNT1
NENCY1
CLKB11
NONEW1
CLRA/
RESCY
CLKB13
CYAU1/
PRBA2/
CYNT2
NENCY2
CLKB21
CLKB22
CLKB23
CLK2C
NONW1
NONW2
DSHPB/
CLKSY
CYAU2/



Rev	Aenderungs-Nr.	Tag	Name

	Tag	Name
Bearb	31.01.89	
Gepr.		

FORCE COMPUTERS

Benennung

DRAM 8 B/C/D/E REV.3

RAS/CAS-GENERATION

Zeichn.-Nr.

195fo30-0

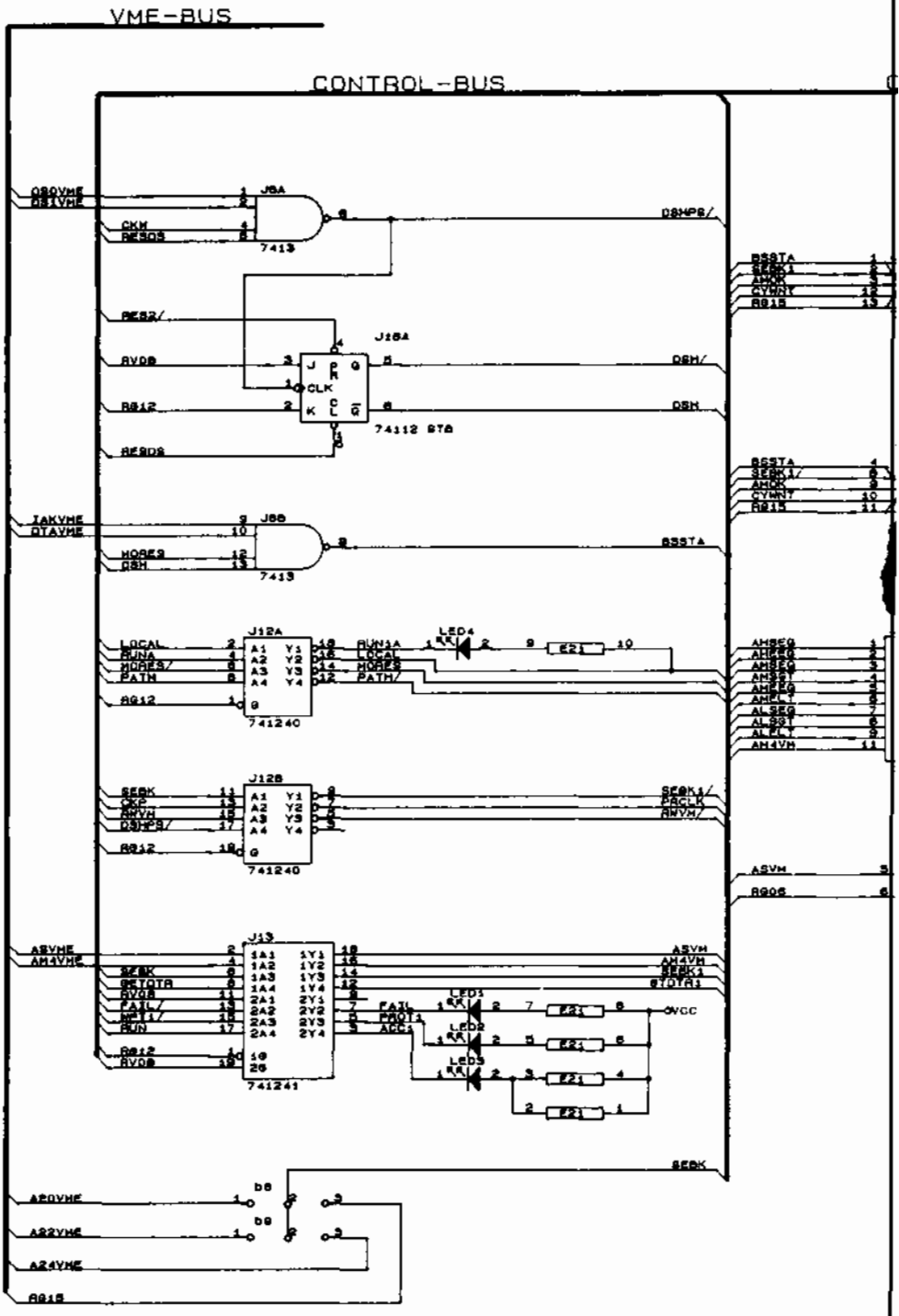
Blatt 3

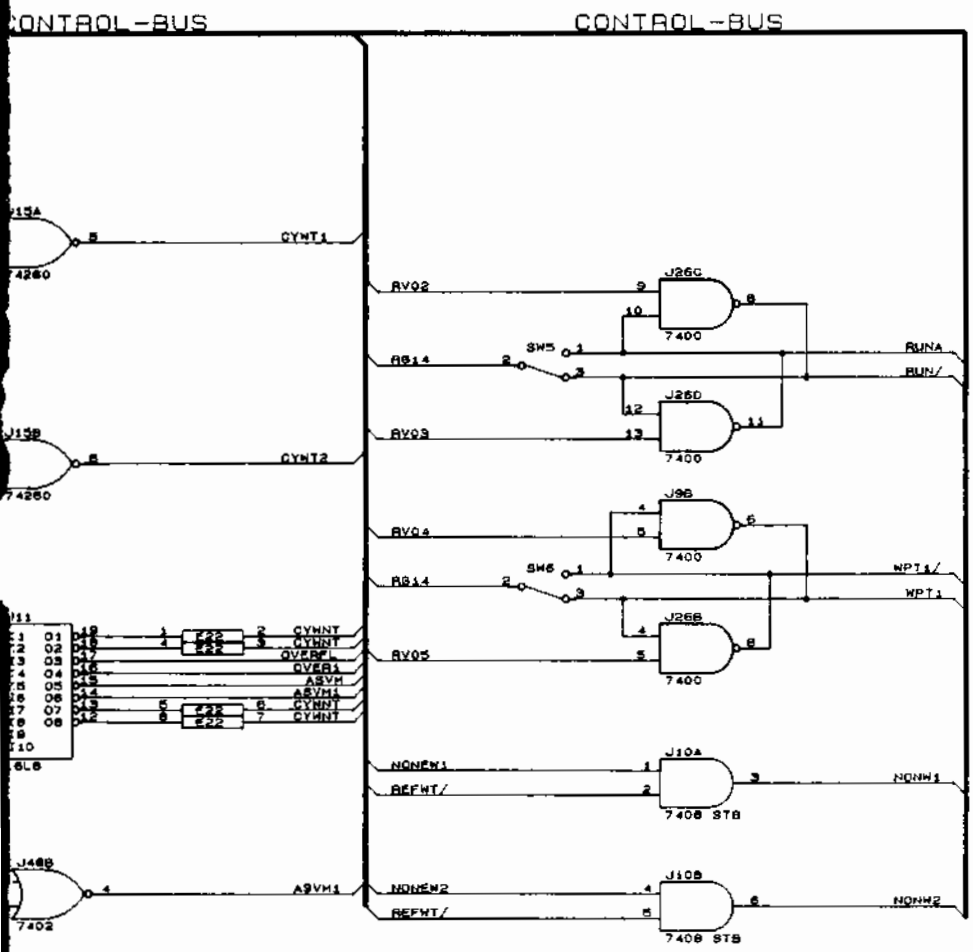
Stand : 07.04.89

zu Gerät

zu Anlage

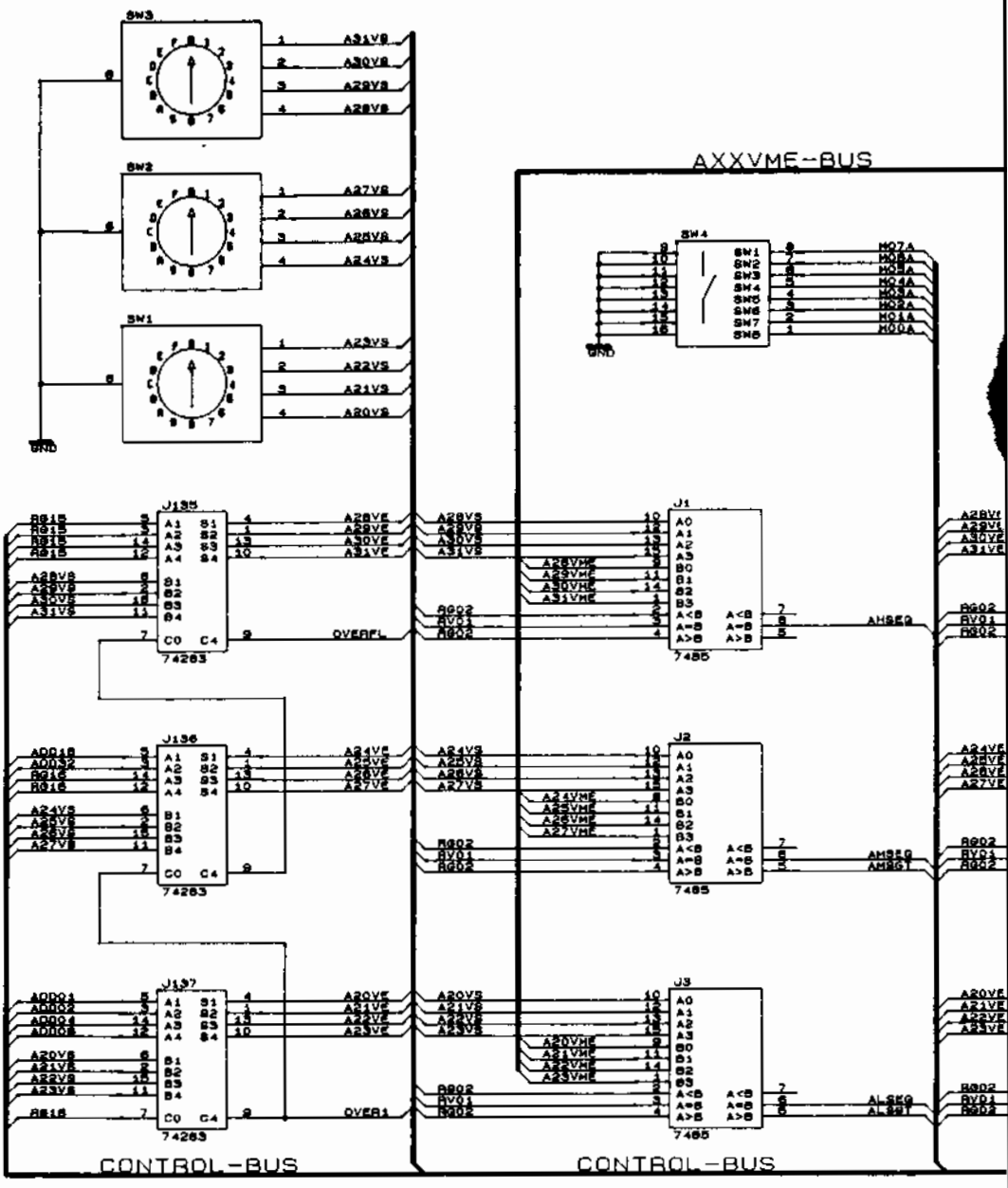
v.1481

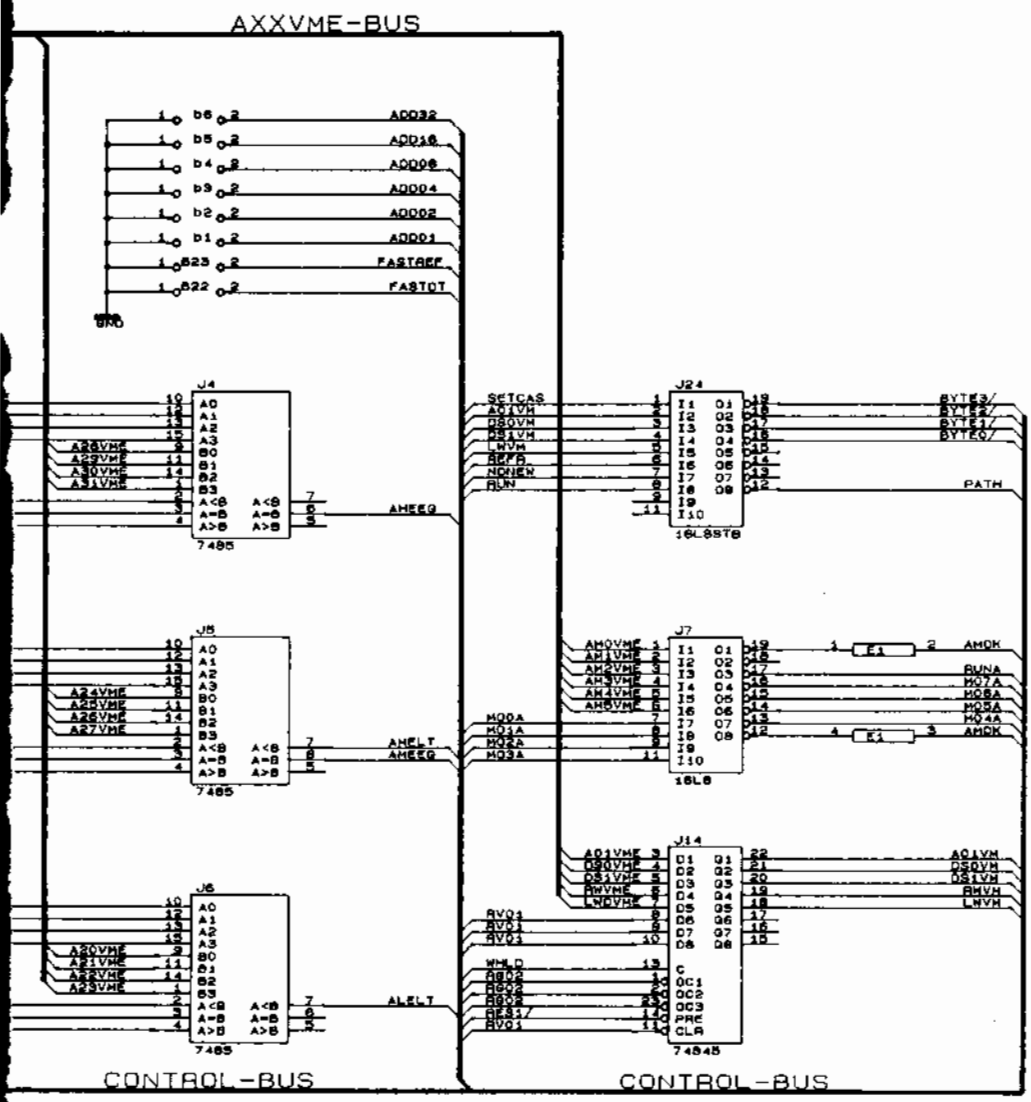

VME-BUS
CONTROL-BUS
J6A
7413
DSMPS/
J16A
74112 STA
DSM/
DSM
J6B
7413
BSSTA
J12A
741240
LED4
J12B
741240
J13
741241
LED1
LED2
LED3
VCC
b8
b9
A20VME
A22VME
A24VME
A01S



				Bearb	Tag 31.01.89	Name	Bezeichnung DRAM 8 B/C/D/E REV.3
				Gepr.			BOARD SELECT LOGIC
				FORCE COMPUTERS			Zeichn.-Nr. 195fo30-0 Blatt 2
Rev	Aender.-Nr.	Tag	Name				zu Gerset zu Anlage v.1481

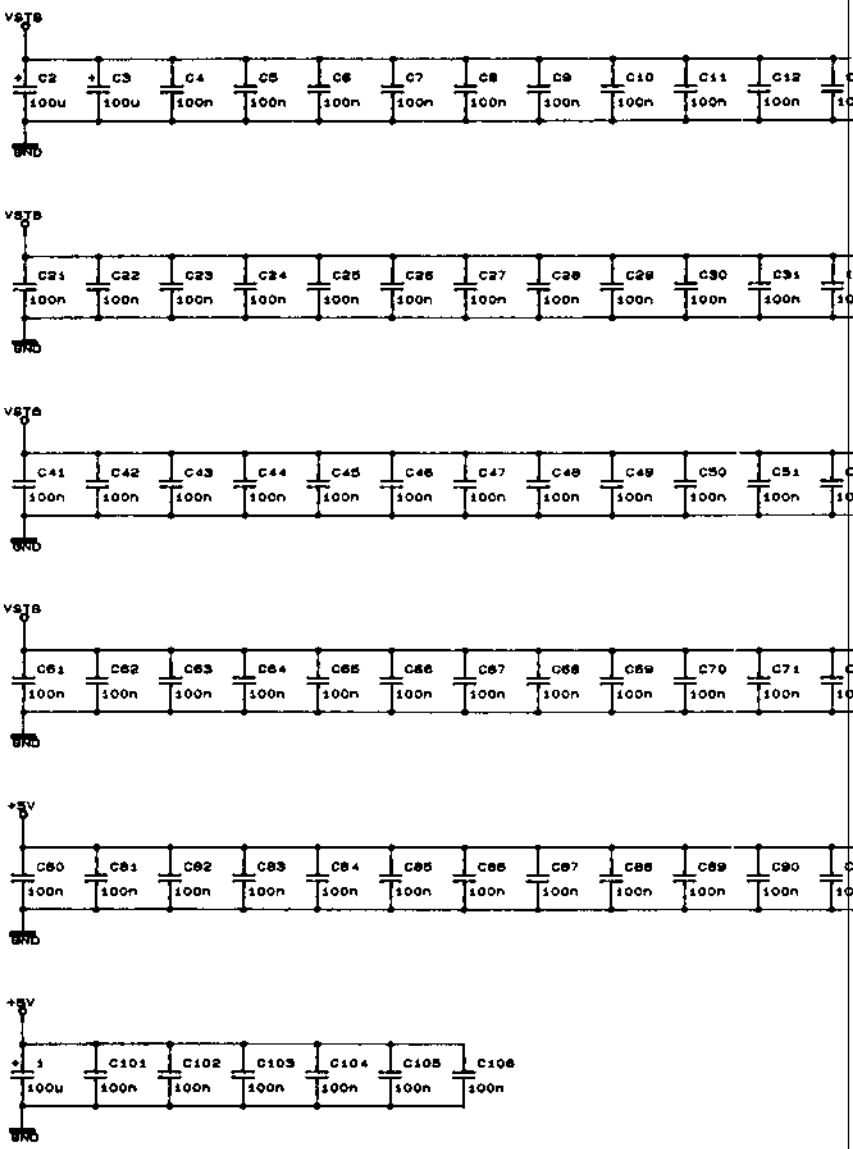
Stand : 07.04.89

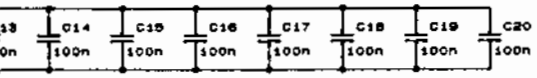

AXXVME--BUS
SW3
SW2
SW1
SW4
GND
A31VS
A30VS
A29VS
A28VS
A27VS
A26VS
A25VS
A24VS
A23VS
A22VS
A21VS
A20VS
J1
J2
J3
J135
J136
J137
74283
7485
OVERFL
OVER1
AHSEQ
AHSGT
ALSEQ
ALSGT
CONTROL-BUS
CONTROL-BUS

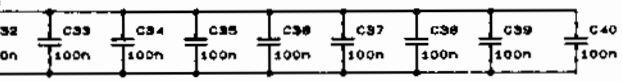


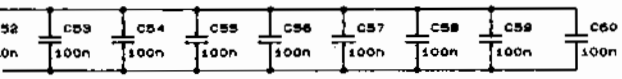
				Stand : 07.04.89	
		Bearb	31.01.89	Bezeichnung	
		Gepr.		DRAM 8 B/C/D/E REV.3	
				ADDRESS / AM-DECODING	
		FORCE COMPUTERS		Zeichn.-Nr. 195fo30-0	Blatt 1
Rev	Aender.-Nr. Tag Name			zu Gerset zu Anlage	V.1101

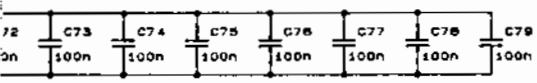
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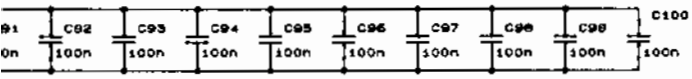

VSTB
C2 100u
C3 100u
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 100n
C11 100n
C12 100n
GND
VSTB
C21 100n
C22 100n
C23 100n
C24 100n
C25 100n
C26 100n
C27 100n
C28 100n
C29 100n
C30 100n
C31 100n
GND
VSTB
C41 100n
C42 100n
C43 100n
C44 100n
C45 100n
C46 100n
C47 100n
C48 100n
C49 100n
C50 100n
C51 100n
GND
VSTB
C61 100n
C62 100n
C63 100n
C64 100n
C65 100n
C66 100n
C67 100n
C68 100n
C69 100n
C70 100n
C71 100n
GND
+5V
C80 100n
C81 100n
C82 100n
C83 100n
C84 100n
C85 100n
C86 100n
C87 100n
C88 100n
C89 100n
C90 100n
GND
+5V
1 100u
C101 100n
C102 100n
C103 100n
C104 100n
C105 100n
C106 100n
GND





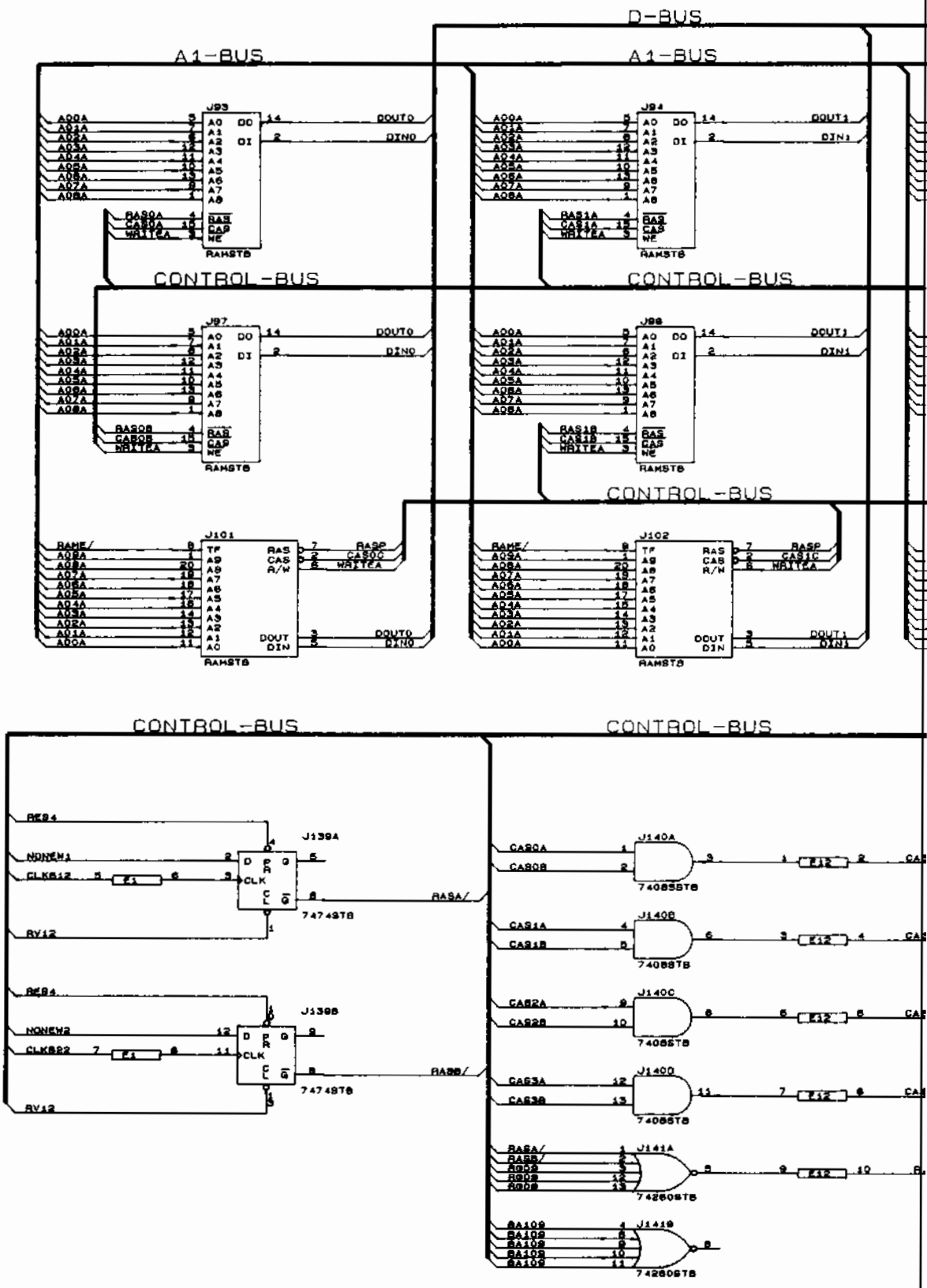


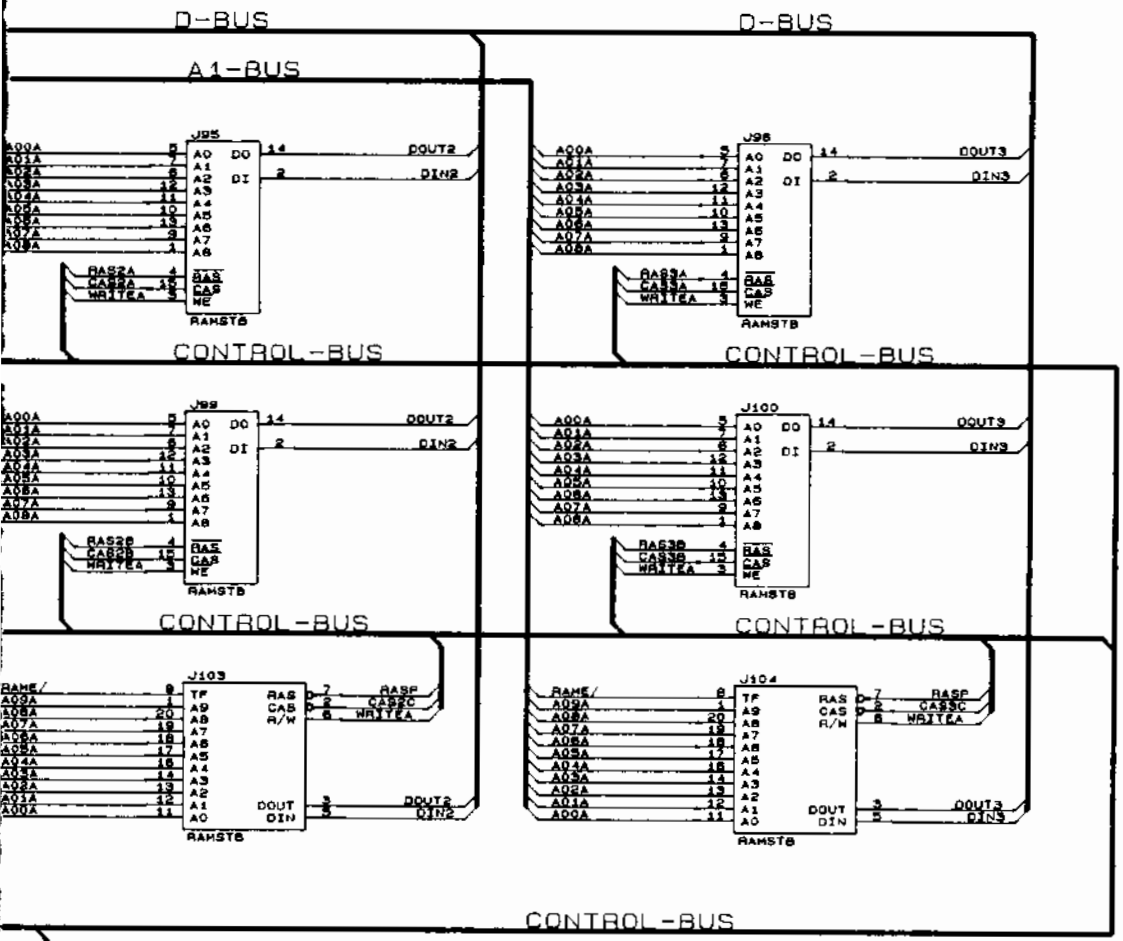




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				Gearb	31.01.89		DRAM 8 A REV.0
				Gepr.			CAPACITORS
				FORCE COMPUTERS			Zeichn.-Nr. 195fo30-0 Blatt 13
Rev	Aender.-Nr.	Tag	Name				zu Gerät zu Anlage V.1301

Stand : 07.04.89


D-BUS
A1-BUS
A1-BUS
CONTROL-BUS
CONTROL-BUS
CONTROL-BUS
CONTROL-BUS
CONTROL-BUS
J93
J94
J97
J98
J101
J102
RAMSTB
DOUT0
DIN0
DOUT1
DIN1
RASP
CASP0
CASP1
WRITEA
RASA/
RASB/
J139A
J139B
J140A
J140B
J140C
J140D
J141A
J141B
74085STB
74086STB
74260STB
74748TB
F12
F1



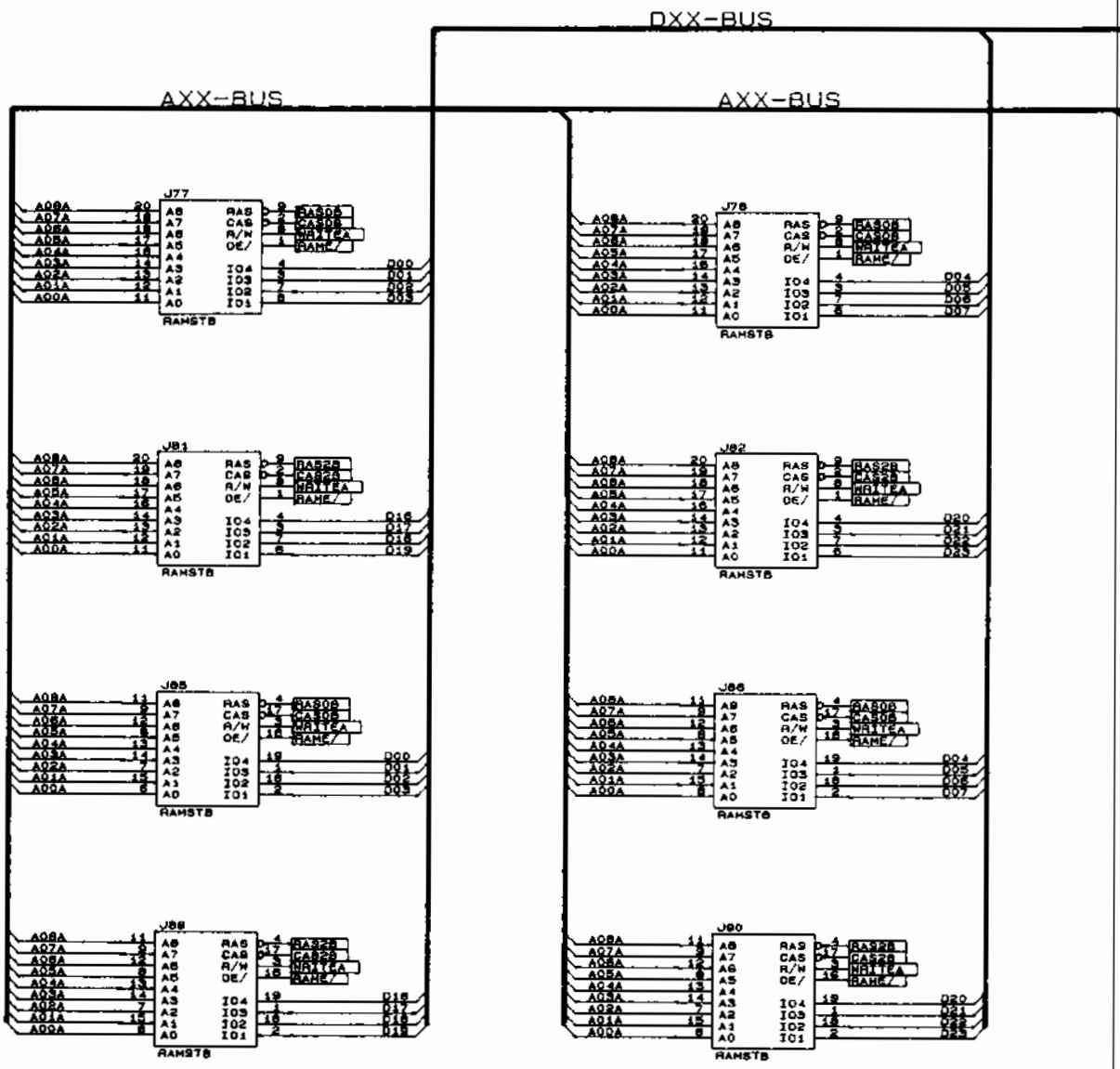
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				Gepr.		RAM AREA
				FORCE COMPUTERS		Zeichn.-Nr. 195f030-0
Rev.	Aenderg.-Nr.	Tag	Name			Zu Gerael.

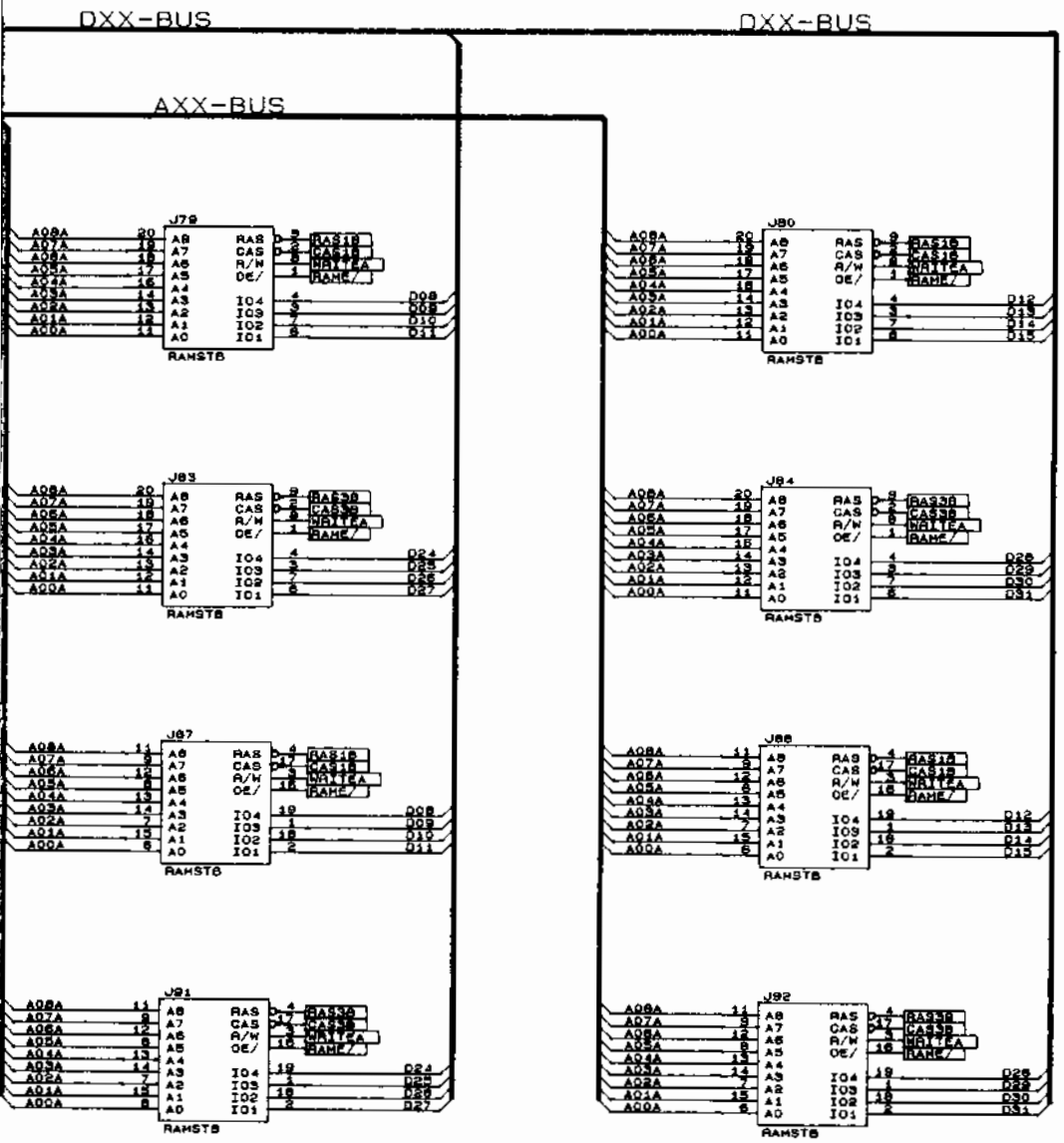
Stand : 07.04.89

REV.0

Blatt 12

Y.1381


DXX-BUS
AXX-BUS
AXX-BUS
J77
J78
J81
J82
J85
J86
J89
J90
RAMSTB



				Bearb	Tag 31.01.89	Name
				Gepr.		
				FORCE COMPUTERS		
Rev.	Aenderungs-Nr.	Tag	Name			

Benennung

DRAM 8 A

RAM AREA

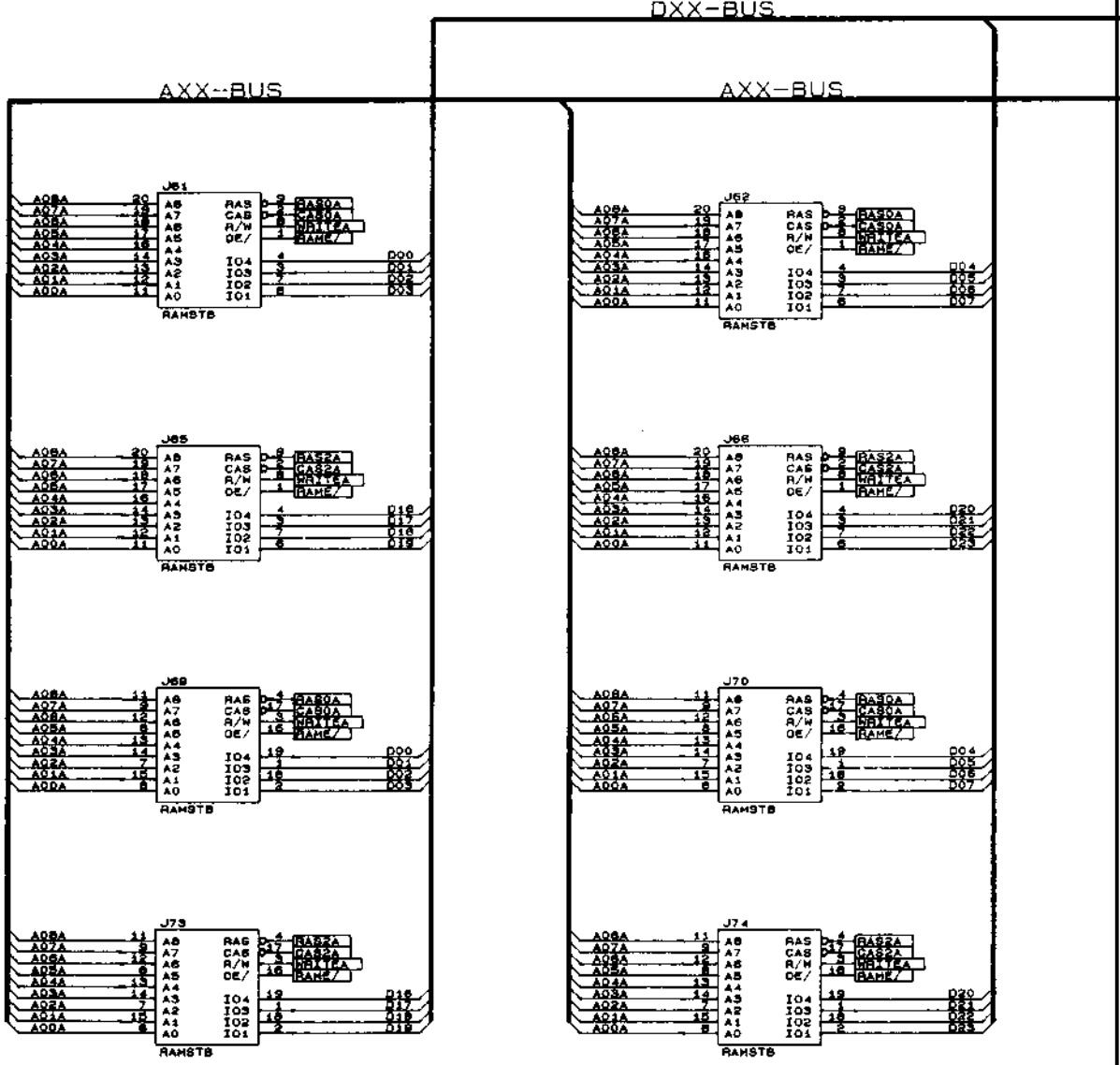
REV.0

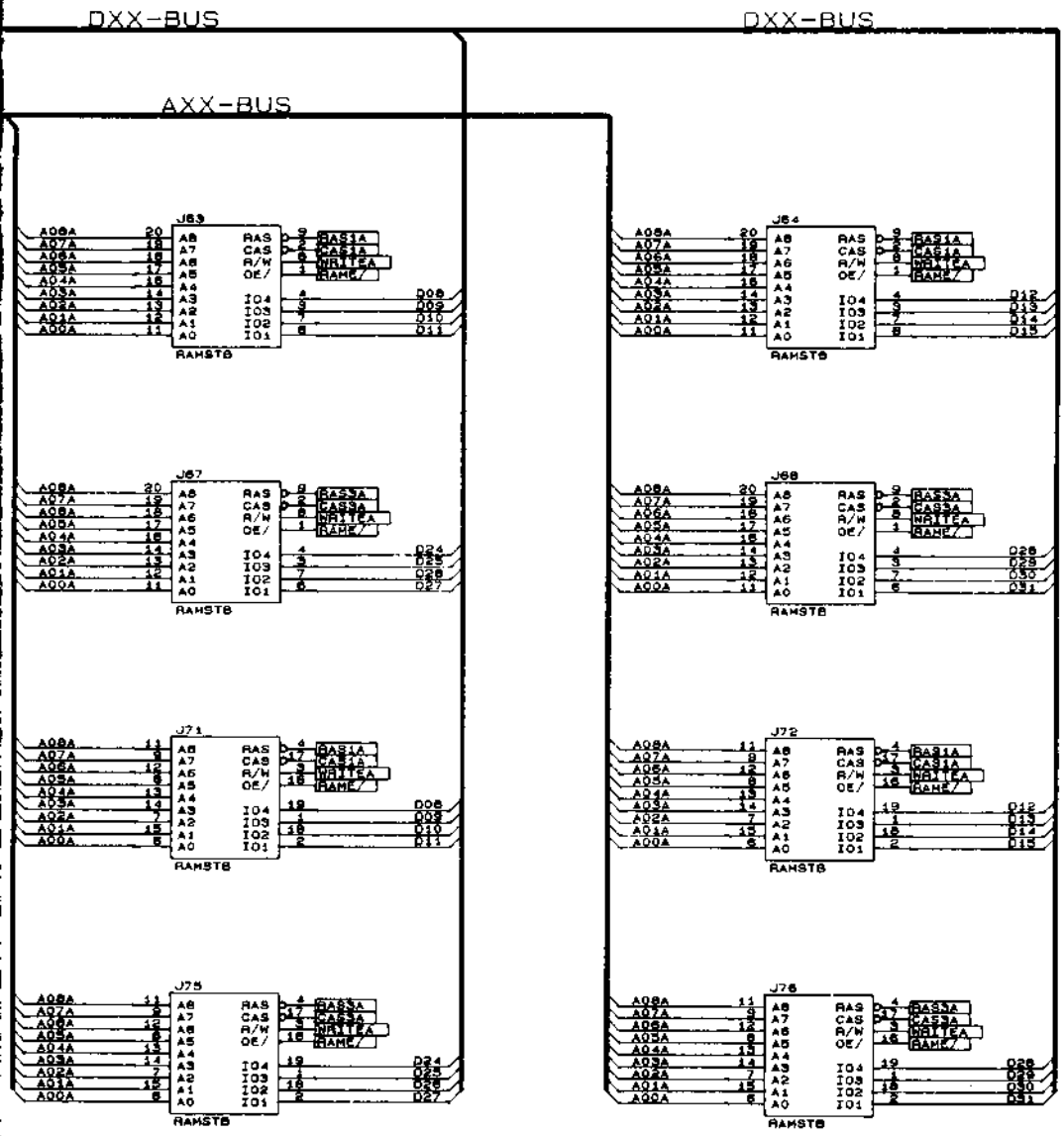
Zeichn.-Nr.: 195fo30-0

Blatt 11

Stand : 07.04.89

zu Bereich: zu Anlage:


DXX-BUS
AXX-BUS
AXX-BUS
J61
J62
J65
J66
J69
J70
J73
J74
RAMSTB



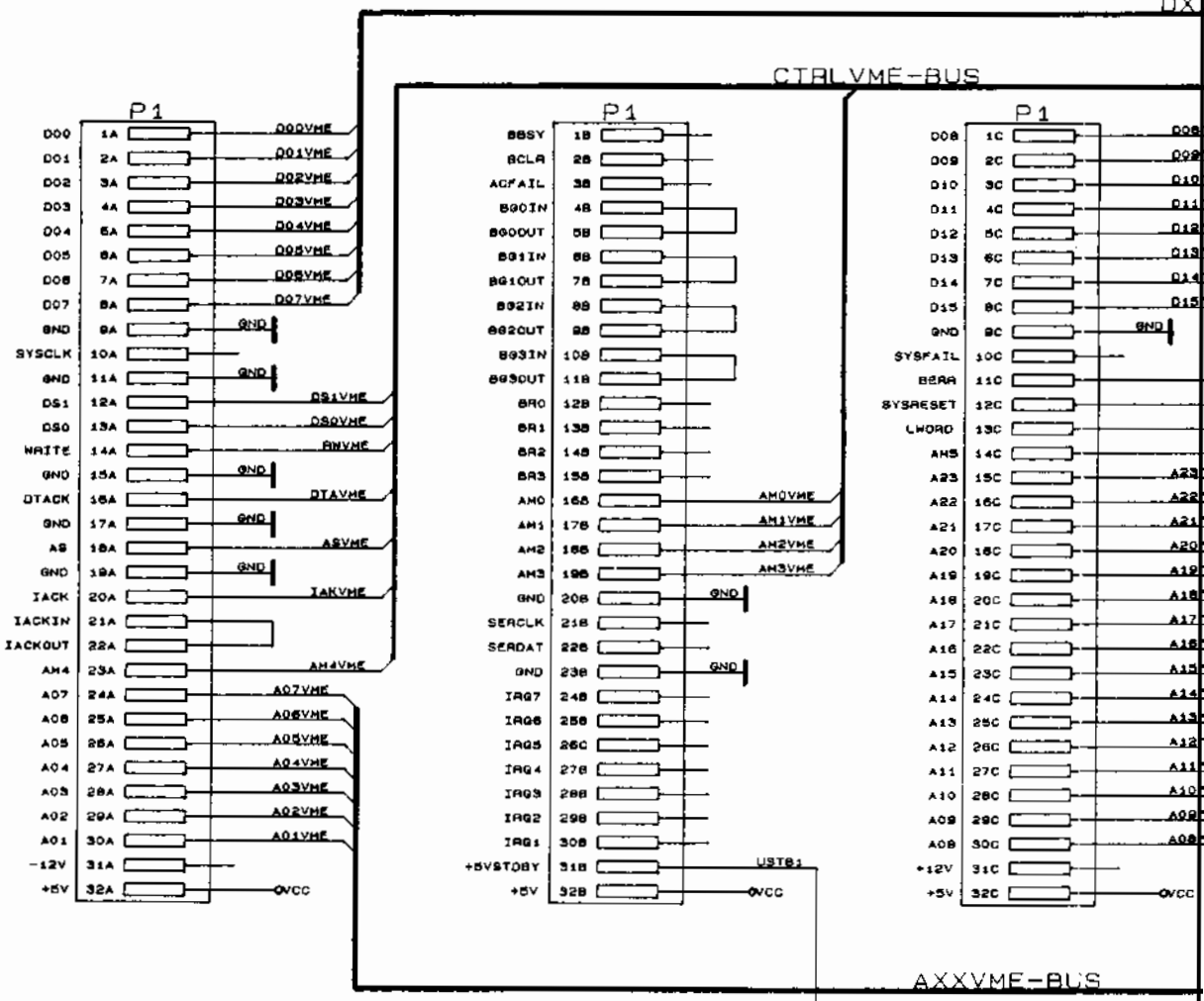
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				Bearb.	31.01.89	DRAM 8 A
				Gepr.		RAM AREA
				FORCE COMPUTERS		Zeichn.-Nr. 195fo30-0
Ers.	Aenderung-Nr.	Tag	Name	zu Gerät		zu Anlage

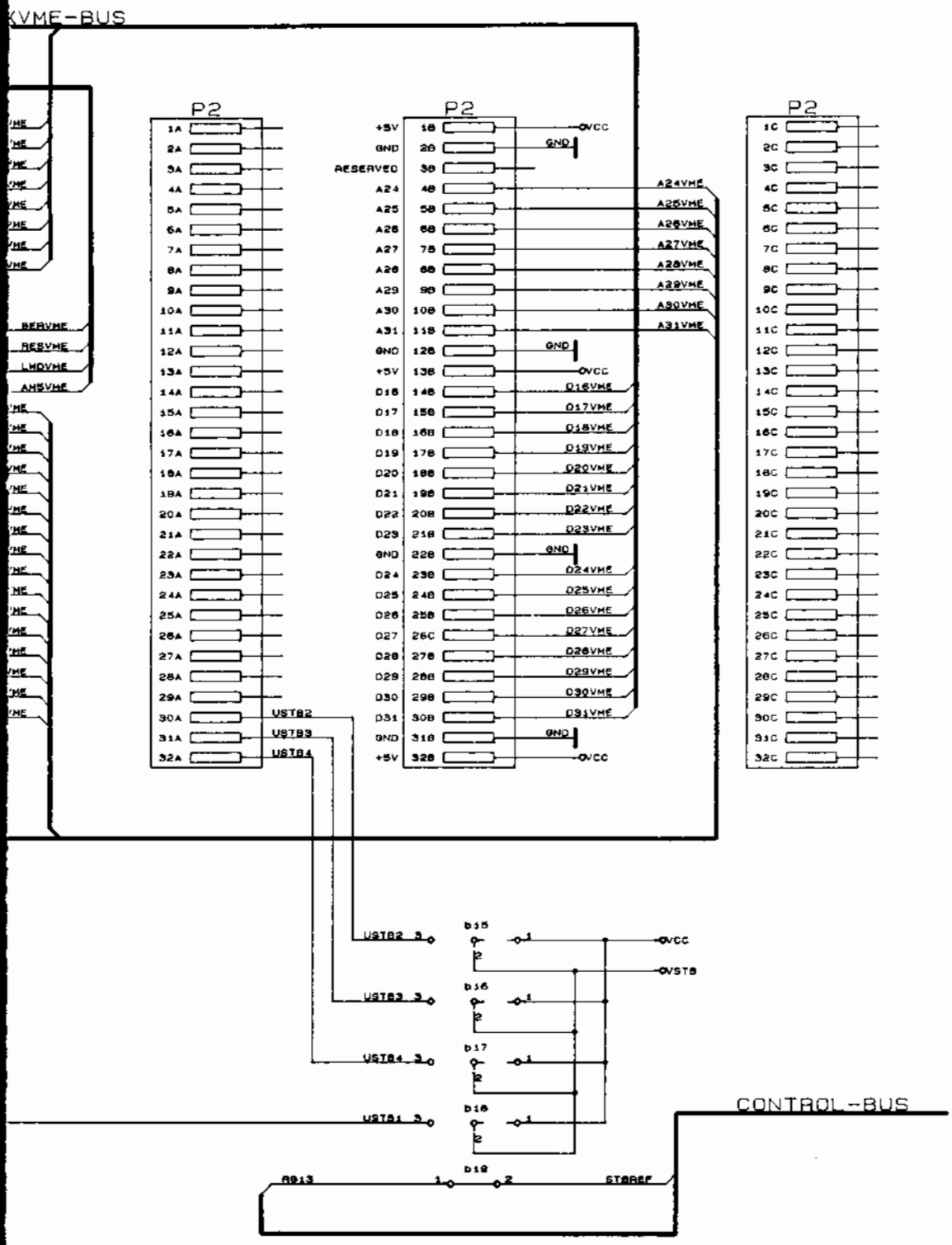
Stand : 07.04.89

REV.0

Blatt 10

V.1301


CTRLVME-BUS
P1
D00 1A
D01 2A
D02 3A
D03 4A
D04 5A
D05 6A
D06 7A
D07 8A
GND 9A
SYSCLK 10A
GND 11A
DS1 12A
DS0 13A
WRITE 14A
GND 15A
DTACK 16A
GND 17A
AS 18A
GND 19A
IACK 20A
IACKIN 21A
IACKOUT 22A
AM4 23A
A07 24A
A06 25A
A05 26A
A04 27A
A03 28A
A02 29A
A01 30A
-12V 31A
+5V 32A
D00VME
D01VME
D02VME
D03VME
D04VME
D05VME
D06VME
D07VME
GND
GND
DS1VME
DS0VME
AMVME
GND
DTAVME
GND
ASVME
GND
IAKVME
AM4VME
A07VME
A06VME
A05VME
A04VME
A03VME
A02VME
A01VME
VCC
P1
BBSY 1B
BCLR 2B
ACFAIL 3B
BG0IN 4B
BG0OUT 5B
BG1IN 6B
BG1OUT 7B
BG2IN 8B
BG2OUT 9B
BG3IN 10B
BG3OUT 11B
BR0 12B
BR1 13B
BR2 14B
BR3 15B
AM0 16B
AM1 17B
AM2 18B
AM3 19B
GND 20B
SERCLK 21B
SERDAT 22B
GND 23B
IRQ7 24B
IRQ6 25B
IRQ5 26B
IRQ4 27B
IRQ3 28B
IRQ2 29B
IRQ1 30B
+5VSTDBY 31B
+5V 32B
AM0VME
AM1VME
AM2VME
AM3VME
GND
GND
USTB1
VCC
P1
D08 1C
D09 2C
D10 3C
D11 4C
D12 5C
D13 6C
D14 7C
D15 8C
GND 9C
SYSFAIL 10C
BERR 11C
SYSRESET 12C
LWORD 13C
AM5 14C
A23 15C
A22 16C
A21 17C
A20 18C
A19 19C
A18 20C
A17 21C
A16 22C
A15 23C
A14 24C
A13 25C
A12 26C
A11 27C
A10 28C
A09 29C
A08 30C
+12V 31C
+5V 32C
GND
VCC
AXXVME-BUS

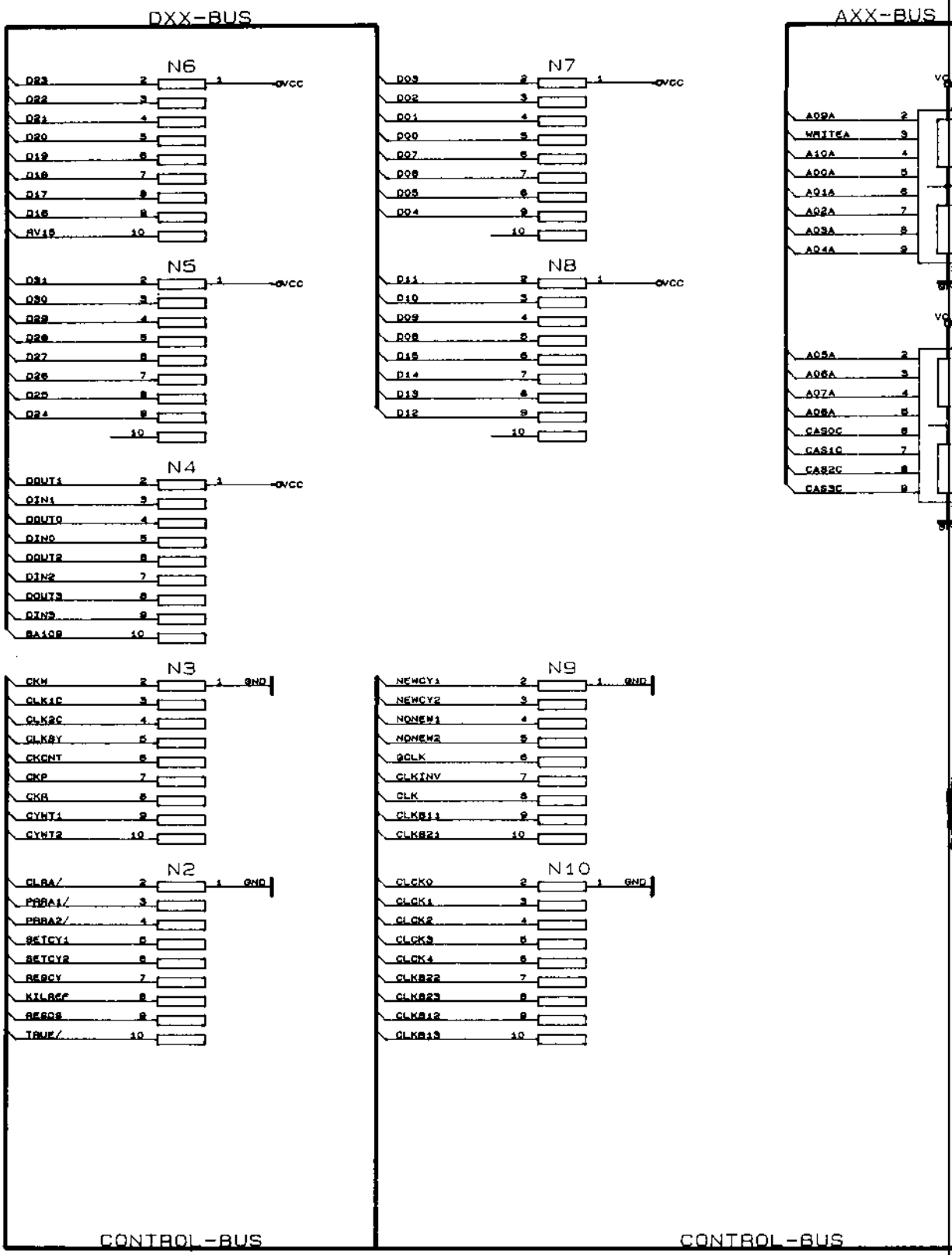


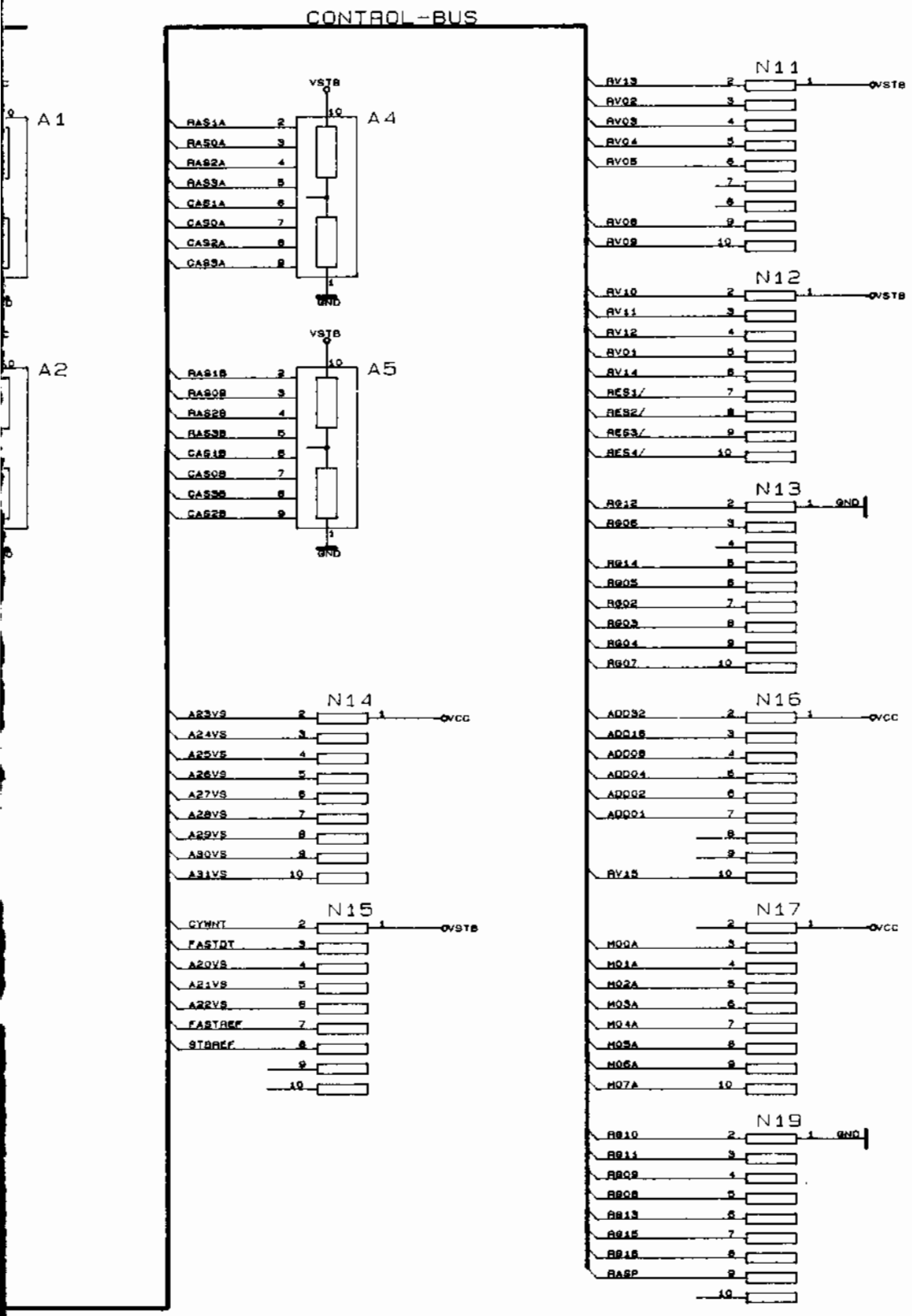
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				Bearb	31.01.89	DRAM 8 A REV.0
				Gepr.		CONNECTORS
				FORCE COMPUTERS		Zeichn.-Nr. 195fo30-0
Rev	Aender.-Nr.	Tag	Name	zu Gerael		zu Anlage

Stand : 07.04.89

Blatt 9

V.1381


DXX-BUS
N6
D23
D22
D21
D20
D19
D18
D17
D16
AV16
VCC
N5
D31
D30
D29
D28
D27
D26
D25
D24
VCC
N4
DOUT1
DIN1
DOUT0
DIN0
DOUT2
DIN2
DOUT3
DIN3
BA10B
VCC
N7
D03
D02
D01
D00
D07
D06
D05
D04
VCC
N8
D11
D10
D09
D08
D15
D14
D13
D12
VCC
N3
CKM
CLK1C
CLK2C
CLK8Y
CKCNT
CKP
CKB
CYNT1
CYNT2
GND
N2
CLBA/
PABA1/
PABA2/
SETCY1
SETCY2
REGCY
KILAGF
REGDS
TRUE/
GND
CONTROL-BUS
N9
NEWCY1
NEWCY2
NONEW1
NONEW2
QCLK
CLKINV
CLK
CLKB11
CLKB21
GND
N10
CLCK0
CLCK1
CLCK2
CLCK3
CLCK4
CLKB22
CLKB23
CLKB12
CLKB13
GND
CONTROL-BUS
AXX-BUS
A09A
WRITEA
A10A
A00A
A01A
A02A
A03A
A04A
A05A
A06A
A07A
A08A
CAS0C
CAS1C
CAS2C
CAS3C



					Bearb	31.01.89	Name
					Gepr.		
Rev	Aender.-Nr.	Tag	Name				

Benennung

DRAM 8 A REV.0

RESISTORS

Stand : 07.04.89

FORCE COMPUTERS

Zeichn.-Nr.

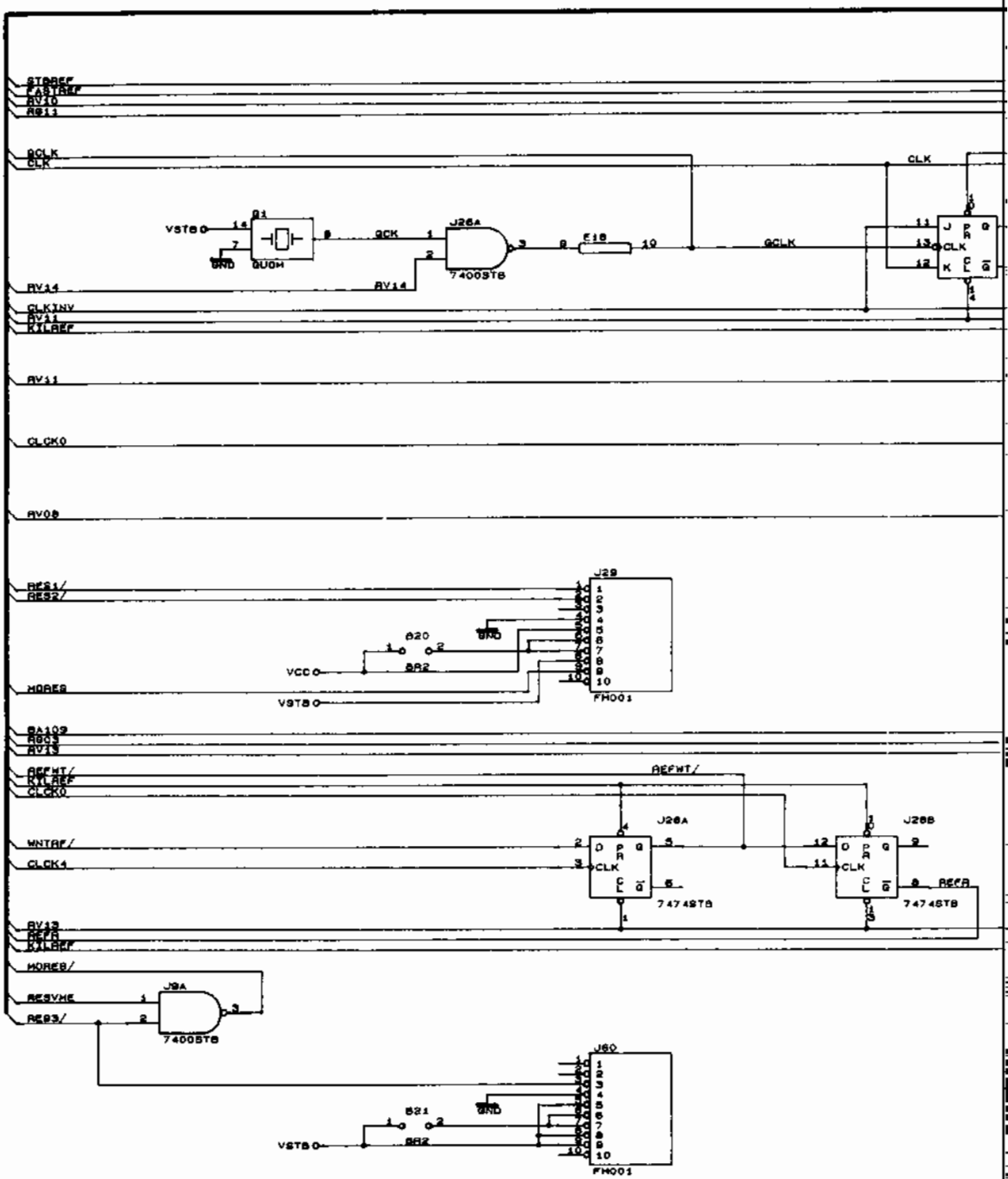
195fo30-0

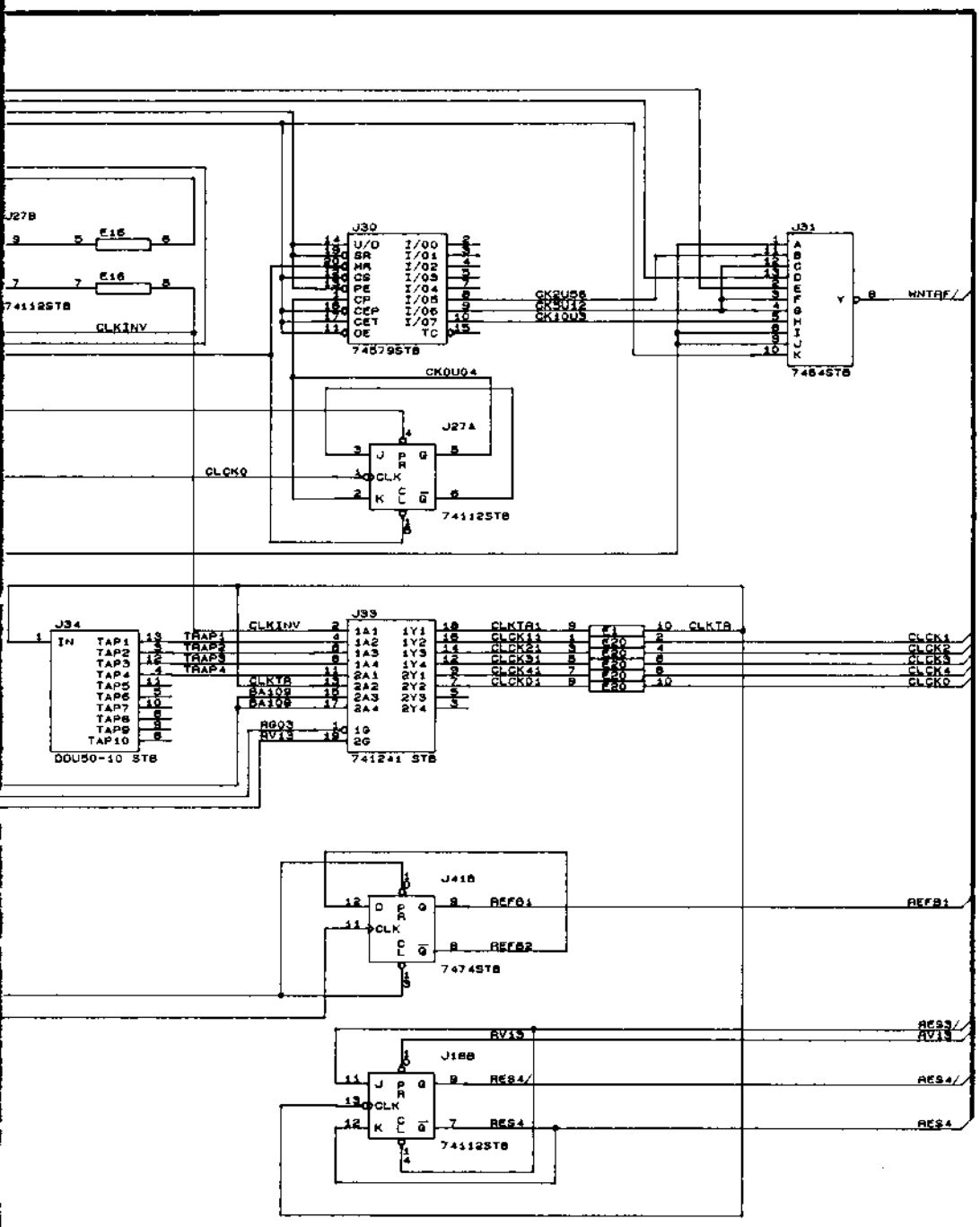
Blatt 8

v.1301

zu Gerset

zu Anlage


STOREF
FASTREF
AV10
AB11
GCLK
CLK
Q1
VSTB
14
7
8
GND
QUOH
GCK
J26A
1
2
3
7400STB
8
E18
10
GCLK
CLK
AV14
CLKINV
AV11
RILREF
AV11
CLCK0
AV08
RES1/
RES2/
J29
1
2
3
4
5
6
7
8
9
10
FH001
820
GND
1
2
VCC
RR2
MORES
VSTB
BA109
A003
AV13
REFWT/
RILREF
CLCK0
WNTRF/
CLCK4
REFWT/
J26A
J26B
D
PR
Q
CLK
CL
7474STB
REFA
AV13
REFA
RILREF
MORES/
RESVHS
RES3/
J9A
7400STB
J60
821
GND
1
2
VSTB
RR2
FH001



				Bearb	Tag 31.01.89	Name
				Gepr.		
Rev	Aender.-Nr.	Tag	Name			

FORCE COMPUTERS

Benennung

DRAM 8 A

TIMING GENERATOR

RESET LOGIC

REV.0

Stand : 07.04.89

Zeichn.-Nr.

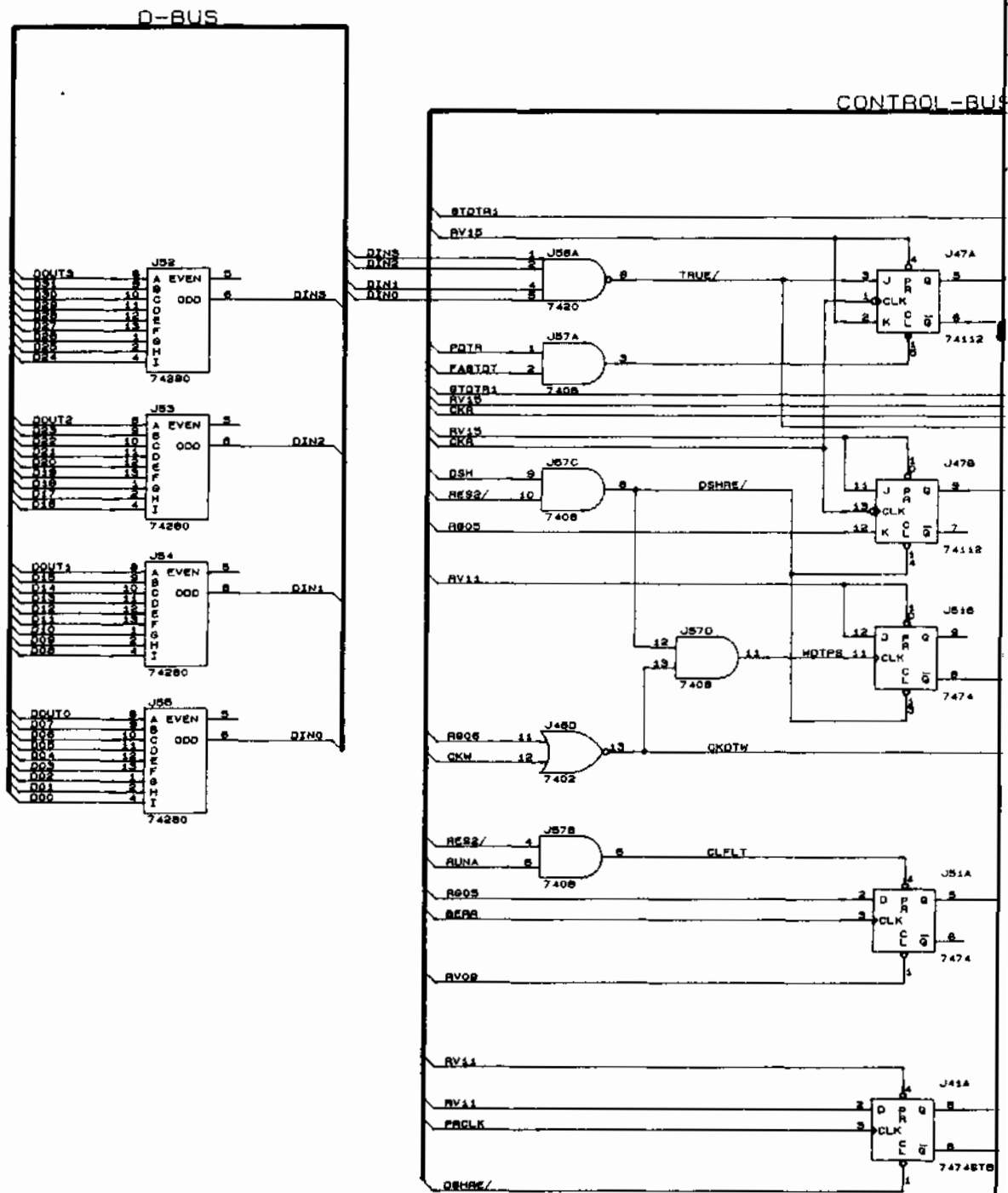
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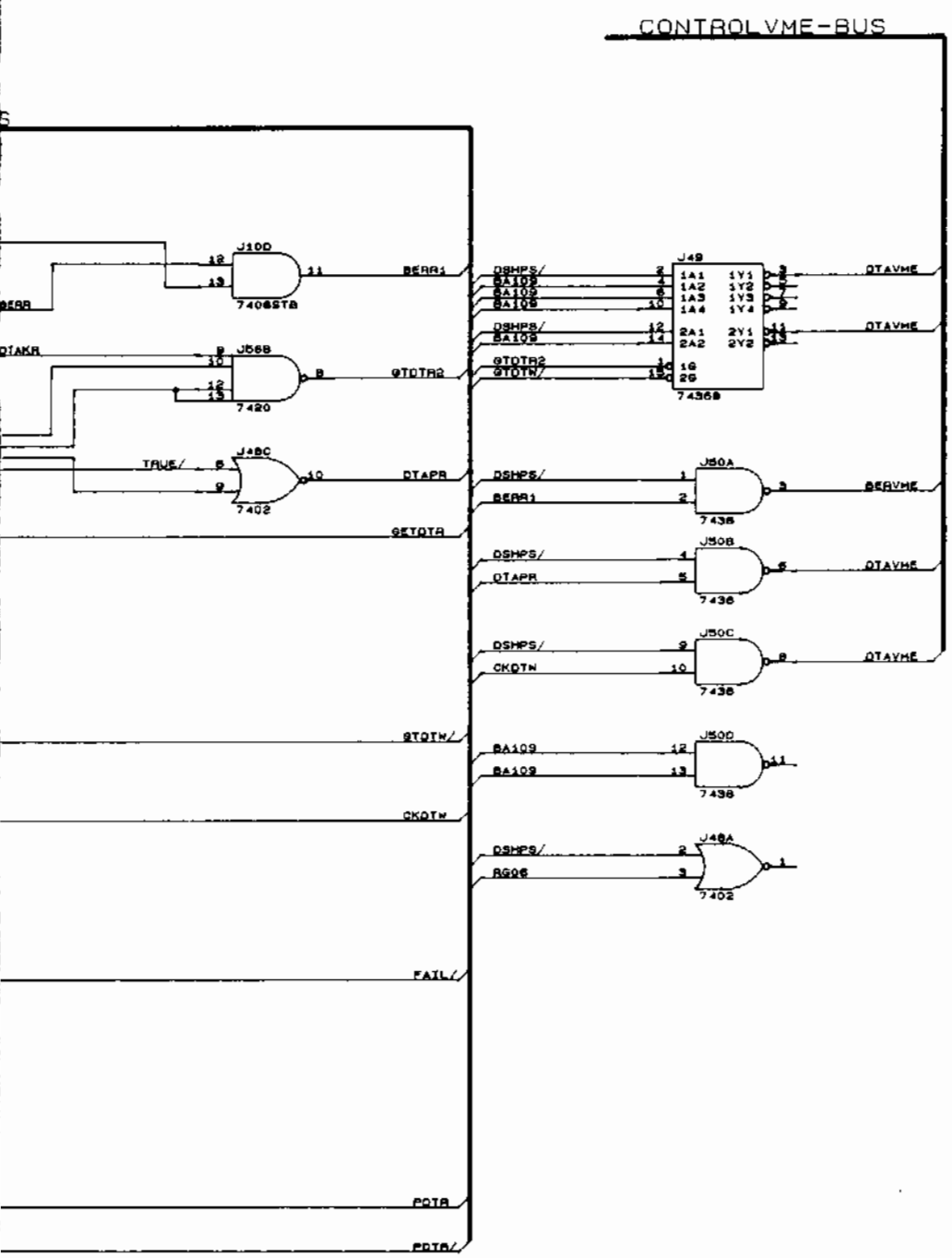
Blatt 7

V.1381

zu Gerset

zu Anlage


D-BUS
CONTROL-BUS
J52
J53
J54
J55
74280
DIN3
DIN2
DIN1
DIN0
J56A
7420
TRUE/
J47A
74112
J57A
7408
PQTR
FASTQT
J57C
DSH
RES2/
DSHRE/
J47B
R005
AV11
J57D
HQTPS
J51B
7474
J48D
7402
R006
CKW
CKQTW
J57B
RUNA
CLFLT
J51A
AV08
J41A
FACLK
DSHRE/



					Bearb	31.01.89	Name
					Gepr.		
Rev.	Aender.-Nr.	Tag	Name				

FORCE COMPUTERS

Benennung

DRAM 8 A

REV.0

PARITY GENERATOR
DTACK*/BERR*- CONTROL

Zeichn.-Nr.

195fo30-0

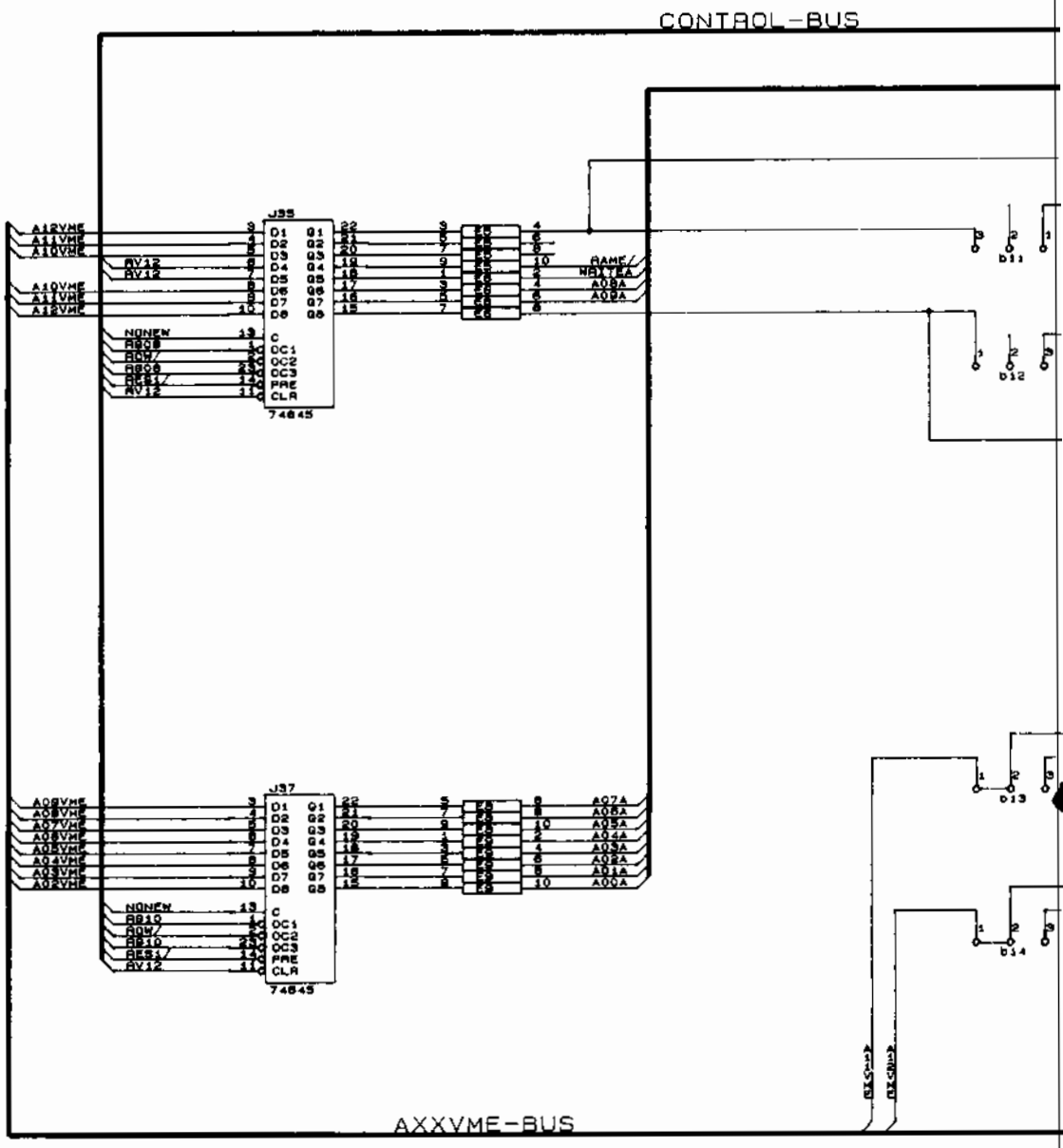
Blatt 6

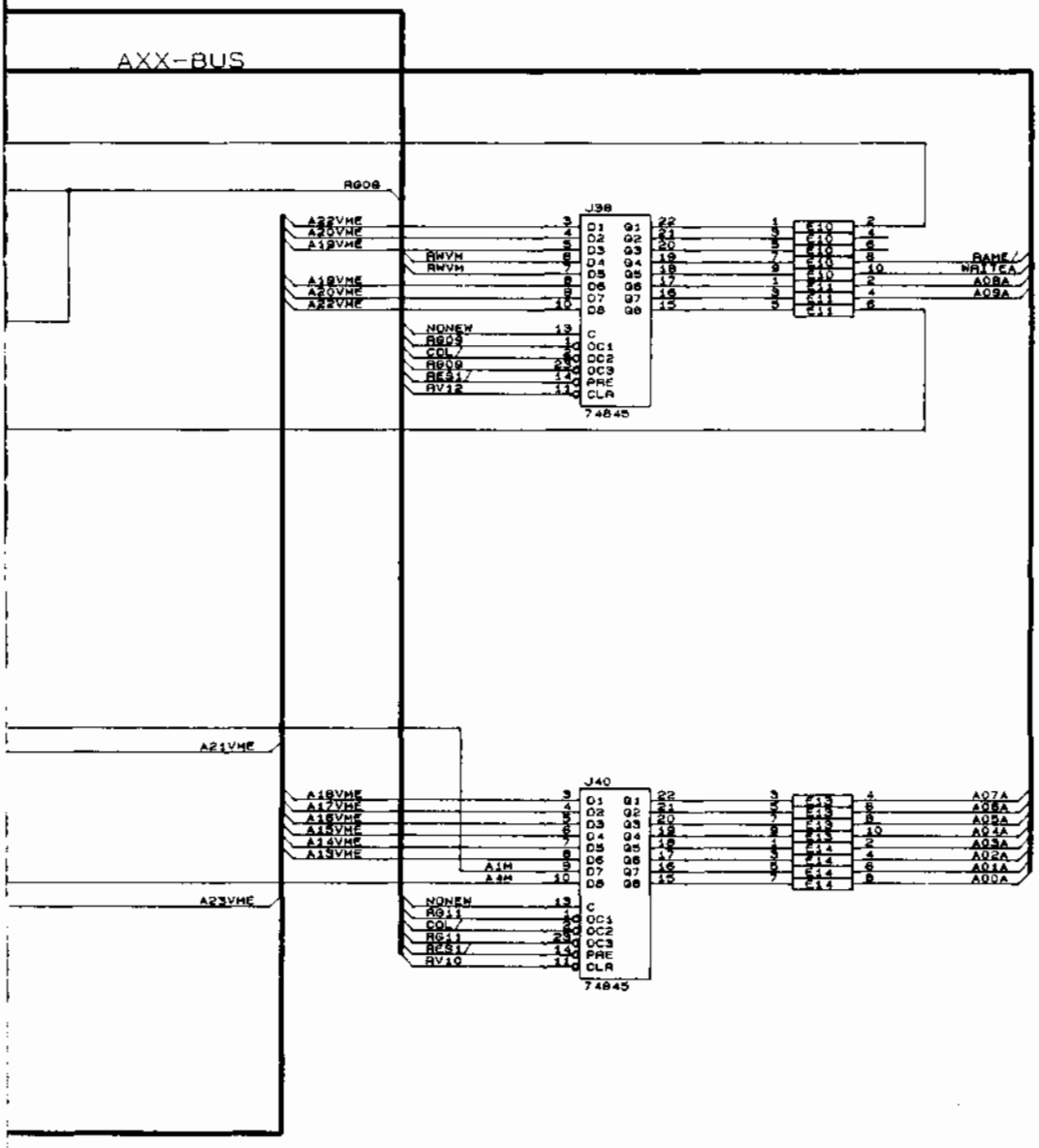
Stand : 07.04.89

V.1301

zu Gerset

zu Anlage


CONTROL-BUS
J35
A12VME
A11VME
A10VME
AV12
AV12
A10VME
A11VME
A12VME
NONEN
AB08
ADW/
AB08
AES1/
AV12
D1 D2 D3 D4 D5 D6 D7 D8
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
C
OC1
OC2
OC3
PRE
CLR
74845
RAME/
WBYTEA
A09A
A08A
J37
A09VME
A08VME
A07VME
A06VME
A05VME
A04VME
A03VME
A02VME
NONEN
AB10
ADW/
AB10
AES1/
AV12
A07A
A06A
A05A
A04A
A03A
A02A
A01A
A00A
D11
D12
D13
D14
AXXVME-BUS



Stand : 07.04.89

	Tag	Name
Bearb	31.01.89	
Gepr.		

Benennung

DRAM 8 A REV.0

ADDRESS LATCH/MUX

FORCE COMPUTERS

Zeichn.-Nr.

195fo30-0

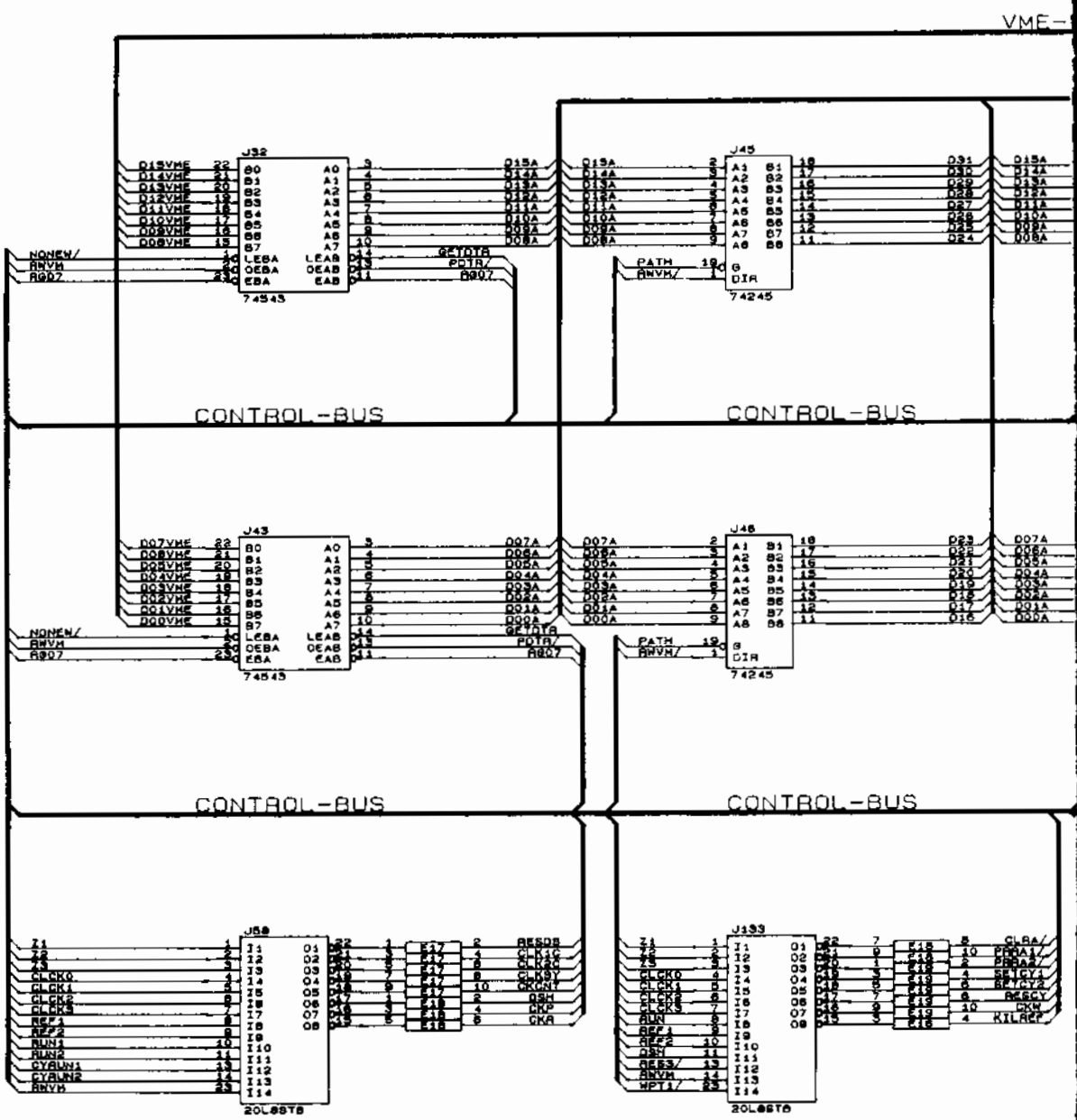
Blatt 5

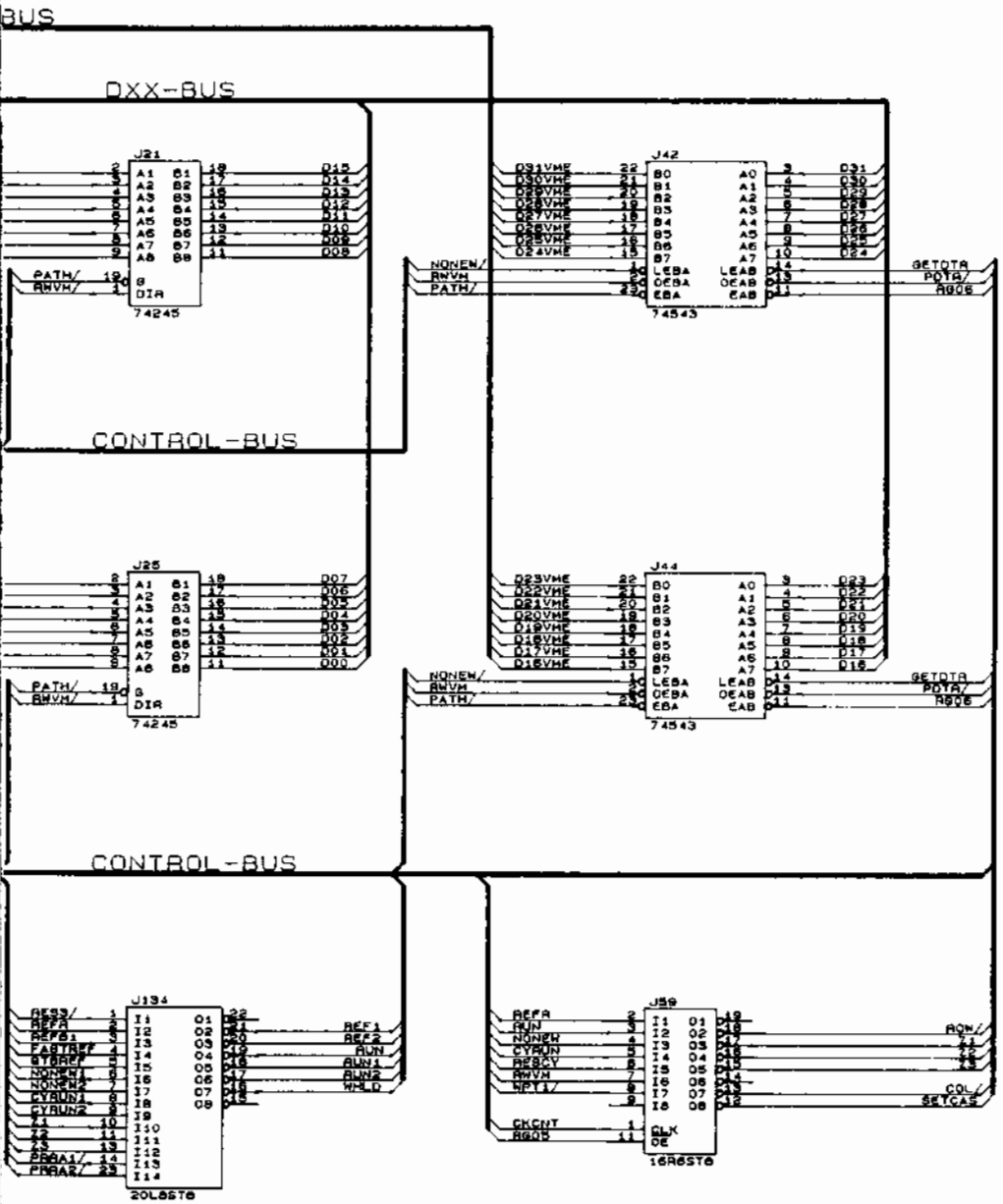
Y.1381

Rev	Aender.-Nr.	Tag	Name

zu Gerset

zu Anlage


VME-
J32
74545
CONTROL-BUS
J45
74245
CONTROL-BUS
J43
74545
CONTROL-BUS
J46
74245
CONTROL-BUS
J58
20L8ST8
J133
20L8ST8



Stand : 07.04.89

				Gesrb	31.01.89	
				Gepr.		

Benennung

DRAM 8 A REV.0

DATA-PATH/REFRESH AND CONTROL LOGIC

FORCE COMPUTERS

Zeichn.-Nr.

195fo30-0

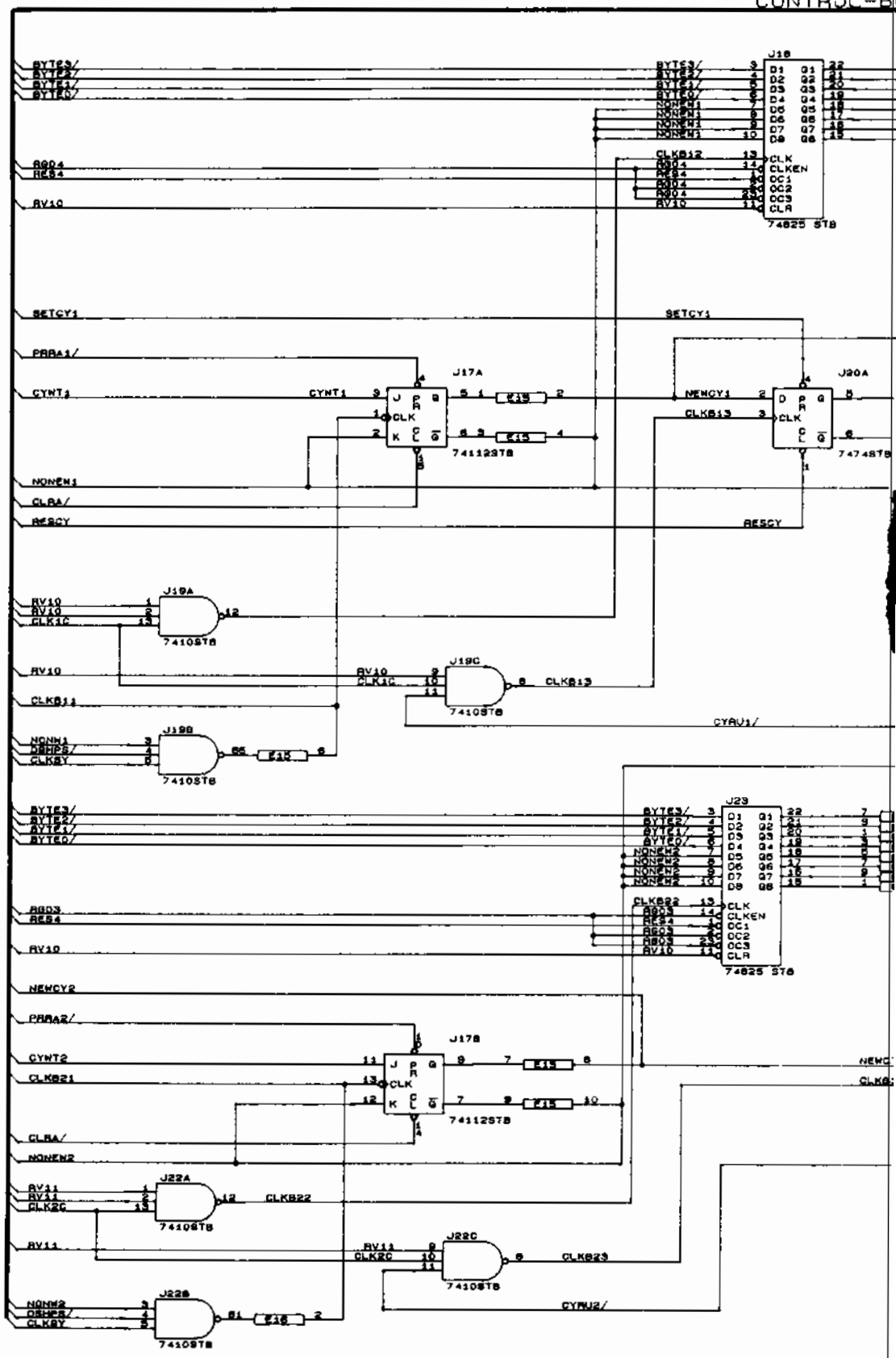
Blatt 4

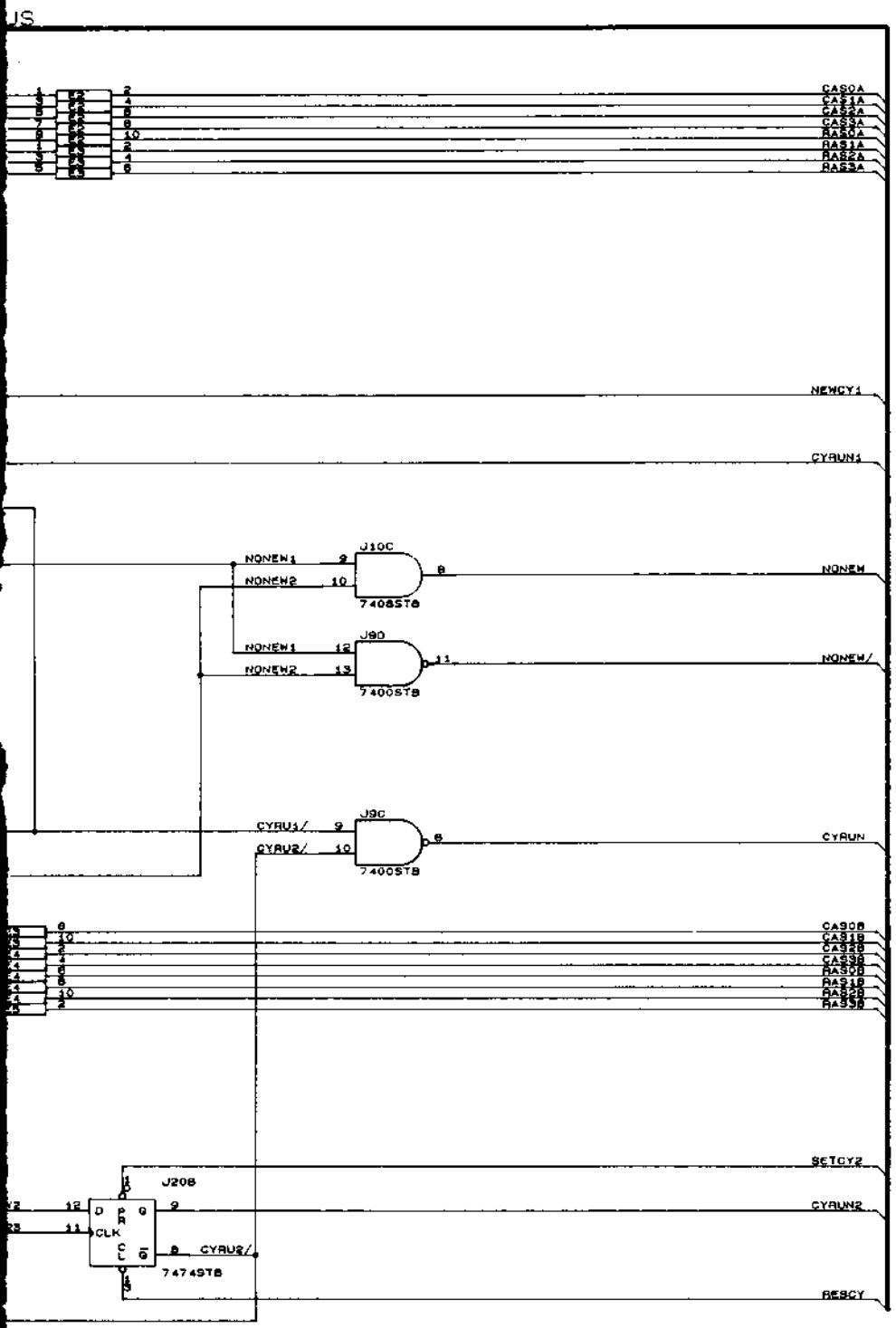
V.1381

Rev	Aender.-Nr.	Tag	Name

zu Gerset

zu Anlage


CONTROL-B
J18
74825 STB
J17A
74112STB
J20A
74748TB
J19A
7410STB
J19C
7410STB
J19B
7410STB
J23
74825 STB
J17B
74112STB
J22A
7410STB
J22C
7410STB
J22B
7410STB
BYTE3/
BYTE2/
BYTE1/
BYTE0/
A804
AE84
AV10
SETCY1
PRRA1/
CYNT1
NONEN1
CLRA/
AESCY
CLKB13
CYAV1/
A803
AE84
AV10
NEWCY2
PRRA2/
CYNT2
CLKB21
CLRA/
NONEN2
CLKB22
CLKB23
CYAV2/



				Bearb	Tag 31.01.89	Name
				Gepr.		
				FORCE COMPUTERS		
Rev	Aender.-Nr.	Tag	Name	zu Gerset		zu Anlage

Stand : 07.04.89

Bezeichnung

DRAM 8 A REV.0

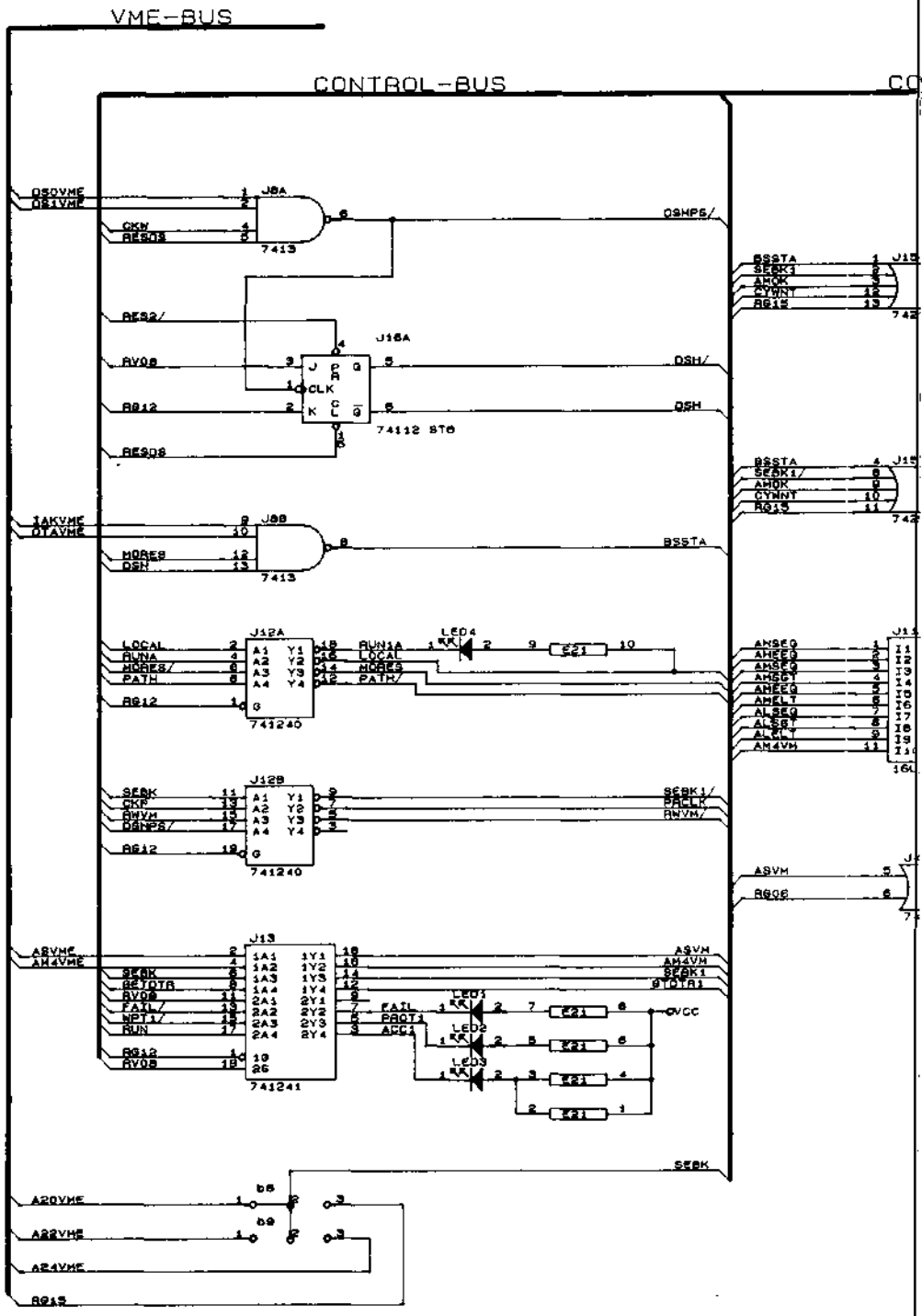
RAS/CAS-GENERATION

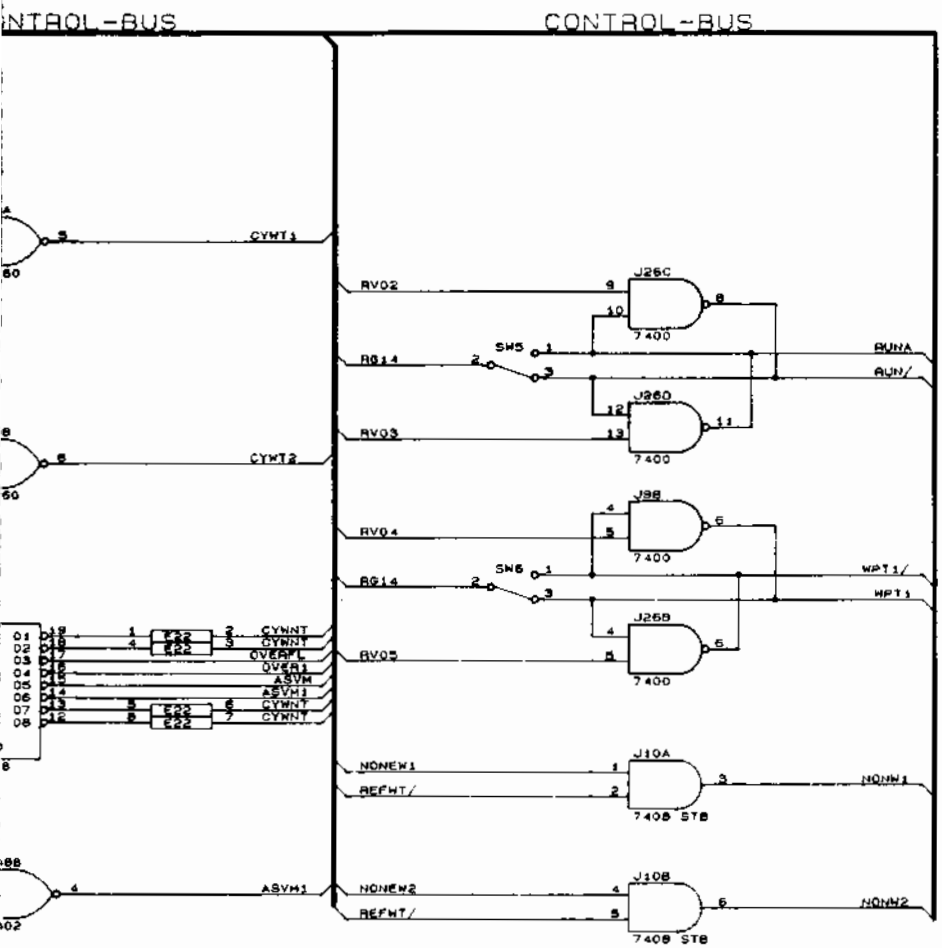
Zeichn.-Nr.

195fo30-0

Blatt 3

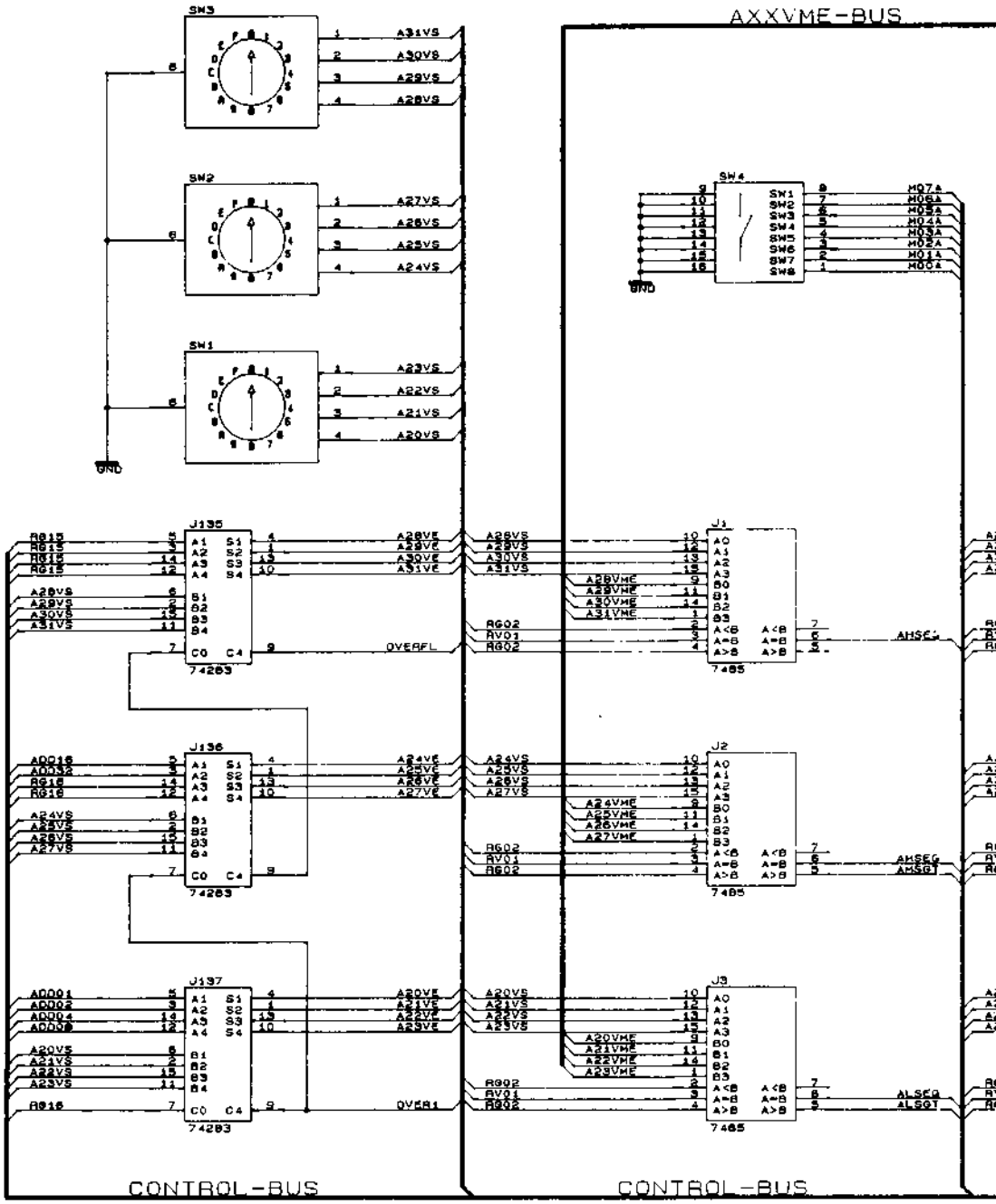
v.1301

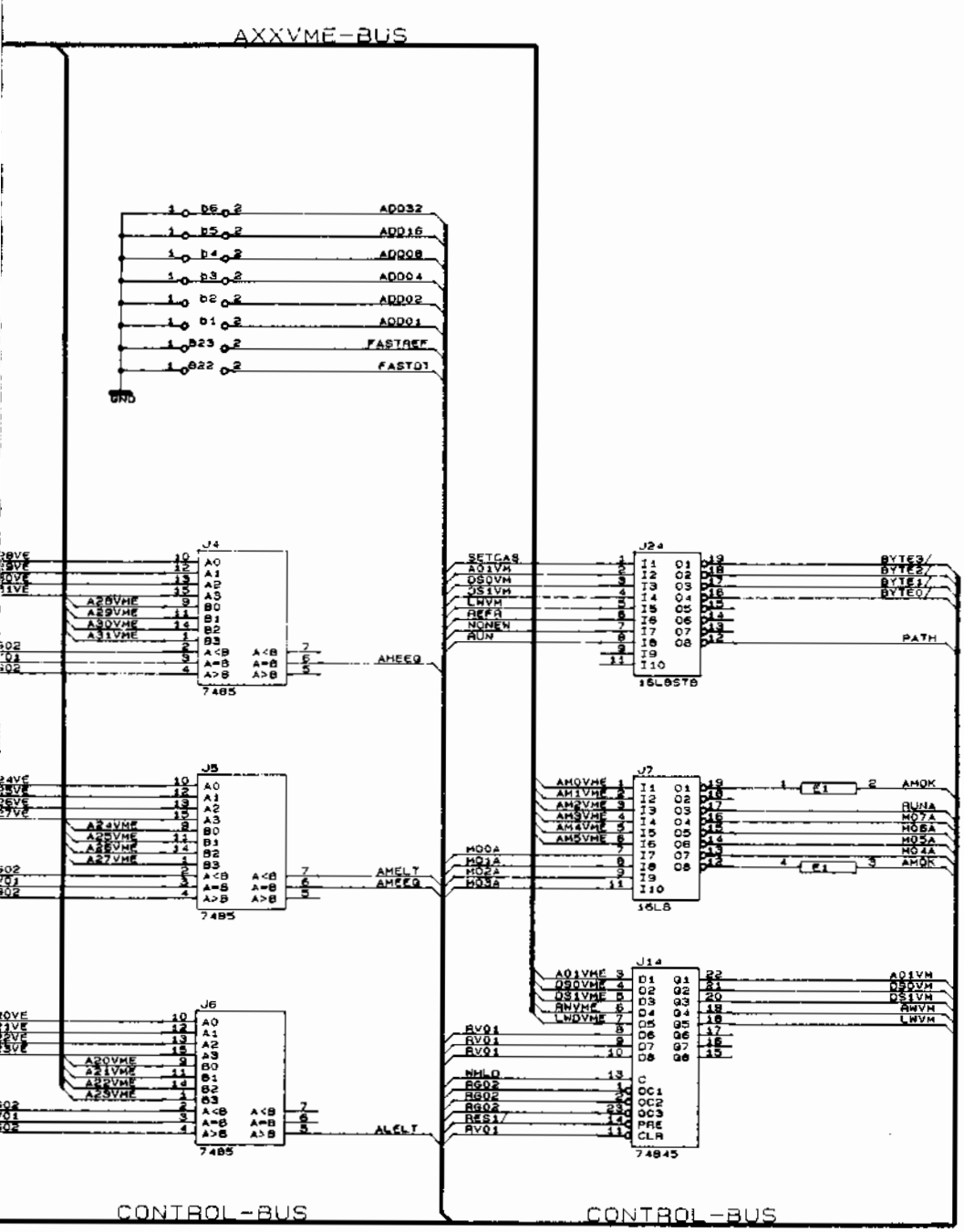

VME-BUS
CONTROL-BUS
DS0VME
DS1VME
CKN
RESDS
J8A
7413
DSHPS/
RES2/
AV08
AB12
RESDS
J16A
CLK
74112 STD
DSH/
DSH
IAKVME
DTAVME
MORES
DSH
J8B
7413
BSSTA
LOCAL
RUNA
MORES/
PATH
AB12
J12A
741240
RUN1A
LED4
R21
SEBK
CKP
AMVM
DSHPS/
AB12
J12B
741240
SEBK1/
PACLK
AMVM/
ASVME
AM4VME
SEBK
BETDTR
AV08
FAIL/
WPT1/
RUN
AB12
AV08
J13
741241
FAIL
PROT1
ACC1
LED1
LED2
LED3
+VCC
ASVM
AM4VM
SEBK1
DTA1
SEBK
A20VME
A22VME
A24VME
AB13
b6
b9



				Tag	Name	Benennung
				Bearb	31.01.89	DRAM 8 A REV.0
				Gepr.		BOARD SELECT LOGIC
				FORCE COMPUTERS		Zeichn.-Nr. 195fo30-0 Blatt 2
Rev	Aender.-Nr.	Tag	Name			Zu Gerset Zu Anlage

Stand : 07.04.89


AXXVME-BUS
SW3
SW2
SW1
SW4
GND
A31VS
A30VS
A29VS
A28VS
A27VS
A26VS
A25VS
A24VS
A23VS
A22VS
A21VS
A20VS
J135
J136
J137
J1
J2
J3
74283
7485
CONTROL-BUS
CONTROL-BUS



Rev	Aender.-Nr.	Tag	Name

	Tag	Name
Bearb	31.01.89	
Gepr.		

FORCE COMPUTERS

Stand : 07.04.89

Benennung

DRAM 8 A REV.0

ADDRESS / AM-DECODING

Zeichn.-Nr.

195fo30-0

Blatt 1

V.1301

zu Gerset

zu Anlage

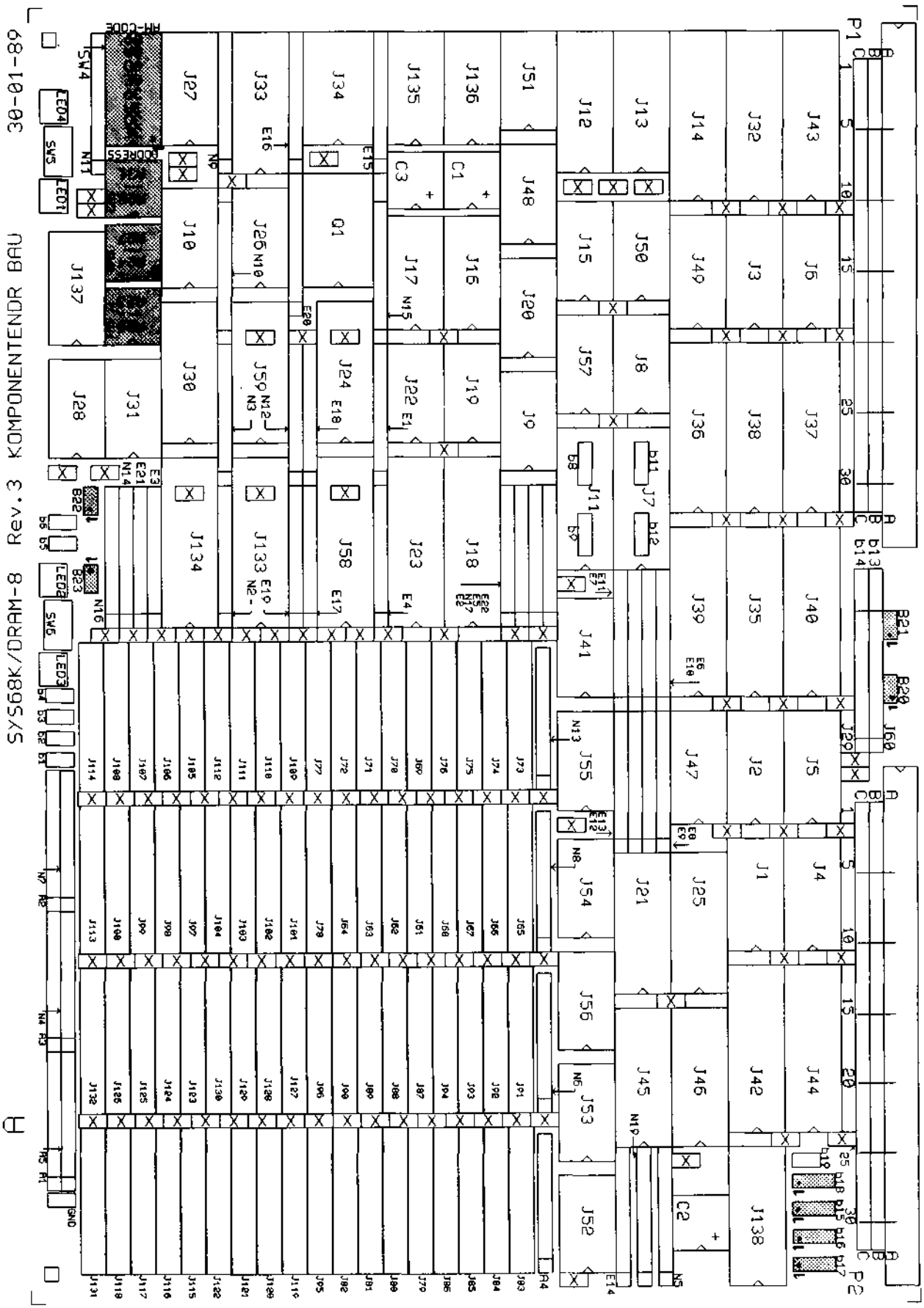
C.1. Circuit Schematics of the DRAM-8

APPENDIX C

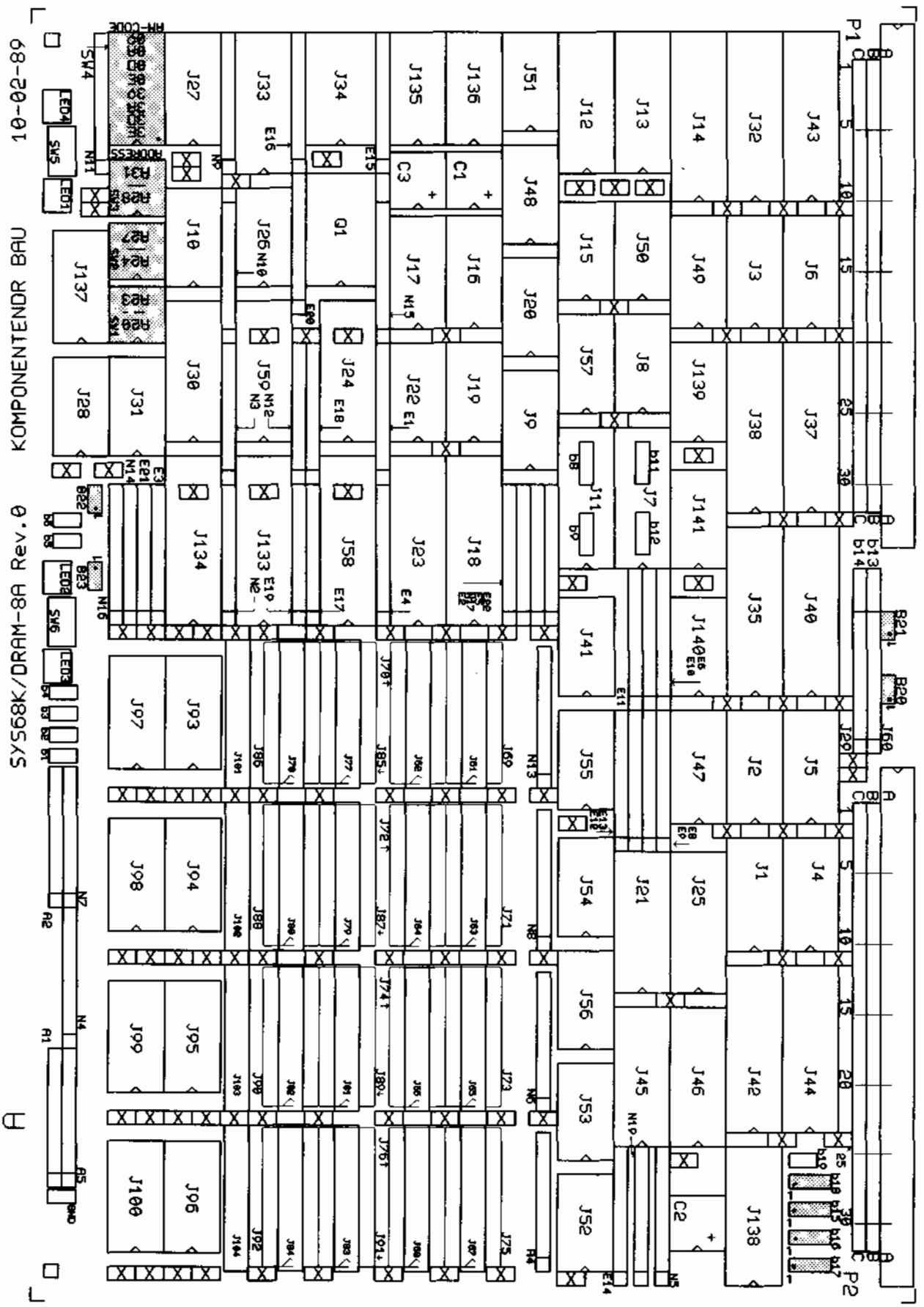
CIRCUIT SCHEMATICS OF THE DRAM BOARDS

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B.2. Location Diagram of DRAM-8B/C/D/E

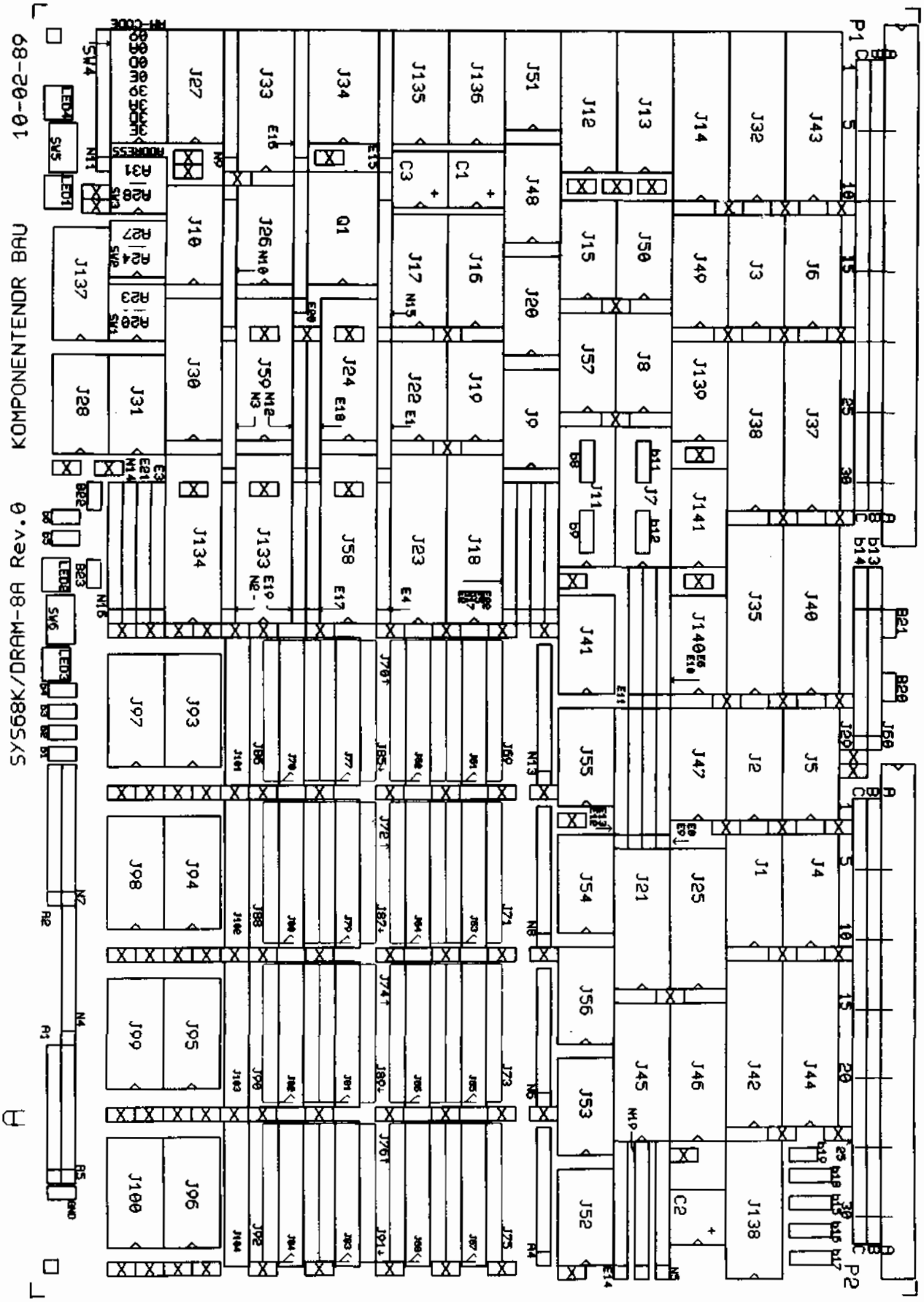


B.1. Location Diagram of DRAM-8A



APPENDIX B

LOCATION DIAGRAMS OF THE DRAM BOARDS



AM-Decoding:

Eight DIP-Switch selectable AM-Codes

Battery Backup

FRONTPANEL Switches / LEDs

VME switch
WRITE PROTECT switch
WRITE PROTECT LED
RUN/LOCAL LED
ERROR LED
ACCESS LED

Power Requirements:

+5V	7.6A (max. refresh peak)
+5V	4.5A (average max.)
+5V	3.8A (average typ.)
+5V	1.9A (battery backup typ.)

Temperatures:

0 to +50 degrees C (operating)
-55 to +85 degrees C (storage)

Relative Humidity:

0-95% (non condensing)

Dimensions:

Double Eurocard
233 * 160mm (9.2 * 6.3 in.)

APPENDIX A

SPECIFICATION OF THE SYS68K/DRAM-8X

Capacity:

DRAM-8A 2Mbytes
DRAM-8B 4Mbytes
DRAM-8C 8Mbytes
DRAM-8D 16Mbytes
DRAM-8E 32Mbytes

Organization:

36 bit internally including 4 parity bits per bank

Data Transfer Modes:

A32 : D32, D16, D8, AD0, UAT, RMW
A24 : D32, D16, D8, AD0, UAT, RMW

Access Times:

Write: 80ns (average typ.) with and without parity check

Read: 230ns (average typ.) with and without parity check

Refresh:

Common Refresh: Interleave every 15us

Shared Refresh: Interleave every 7.5us (only DRAM-8A/C/E)

Address Decoding:

HEX-Switch selectable start-address in increments of 1 Mbyte

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L I S T O F A P P E N D I C E S

A. SPECIFICATION OF THE SYS68K/DRAM-8X A-1

B. LOCATION DIAGRAMS OF THE DRAM BOARDS B-1

B.1. Location Diagram of DRAM-8A B-2

B.2. Location Diagram of DRAM-8B/C/D/E B-3

C. CIRCUIT SCHEMATICS OF THE DRAM BOARDS C-1

C.1. Circuit Schematics of the DRAM-8A C-2

C.2. Circuit Schematics of the DRAM-8B/C/D/E C-3

D. CONNECTOR PIN ASSIGNMENT OF THE SYS68K/DRAM-8 . . . D-1

D.1. P1 . . . . . D-1

D.2. P2 . . . . . D-2

E. ADDRESS MODIFIER CODES E-1

F. COMPONENT PART LISTS F-1

F.1. COMPONENT PART LISTS OF DRAM-8A F-2

F.2. COMPONENT PART LISTS OF DRAM-8B/C/D/E F-3

G. GLOSSARY OF VME/1014 TERMS G-1

H. LITERATURE REFERENCE H-1

I. PRODUCT ERROR REPORT I-1

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APPENDIX TO THE
HARDWARE USER'S MANUAL

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6. PREPARATION FOR USE

a) Please read the complete manual for correct board handling.

b) Make an optical check of the board and the components for possible damages prior to mounting the board.

c) Use adequate electrical outlets for checking.

d) Use adequate equipment for electrical checking.

e) Use a power supply with sufficient drive capacity within the IEEE1014* Standard tolerances.

f) To initialize the DRAM-8x banks, an initialization routine has to be installed before reading from the board.

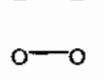
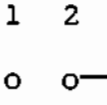
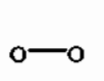
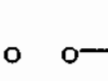
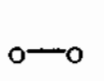
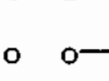
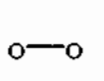
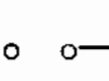
The following program example (subroutine) in 680xx assembler is useful for initialization:

```
STARTADR = first on-board bank address
ENDADR   = last on-board bank address

START LEA.L  STARTADR,A0
      LEA.L  ENDADR,A1
LOOP  MOVE.W #0,(A0)+
      CMPA.L A1,A0
      BLT.S  LOOP
      RTS
```

The next table shows the connection of the solder bridges for the different power supply possibilities.

Table 5-5: Connection of the Power Supply Solder bridges

Bridge	No battery backup	With battery backup
b15		
b16		
b17		
b18		

CAUTION:

1) If you use this option all power entries must be connected.

2) Avoid connection mismatch between the different power supplies.

3) Ensure that there is no conflict with a secondary bus (for example VSB) if you use the battery backup.

Per default (no battery backup) pins 1 and 2 of bridges b15, b16, b17, b18 are shortened by solder bridges.

5.4 Battery Backup Power Solder Bridges (b15 - b18)

All solder bridges are inserted by the factory for use of the board under standard conditions.

The solder bridges are connected by default for board usage provided that normal system power conditions exist. To install the battery backup option, the connection between pin 1 to pin 2 of the solderbridges b15, b16, b17, b18 must be opened.

In order to connect the battery backup power, close the solder bridges between pin 2 and pin 3 of b15 to b18 and ensure backup power is supplied to the VME backplane at the assigned pins (Table 5-4).

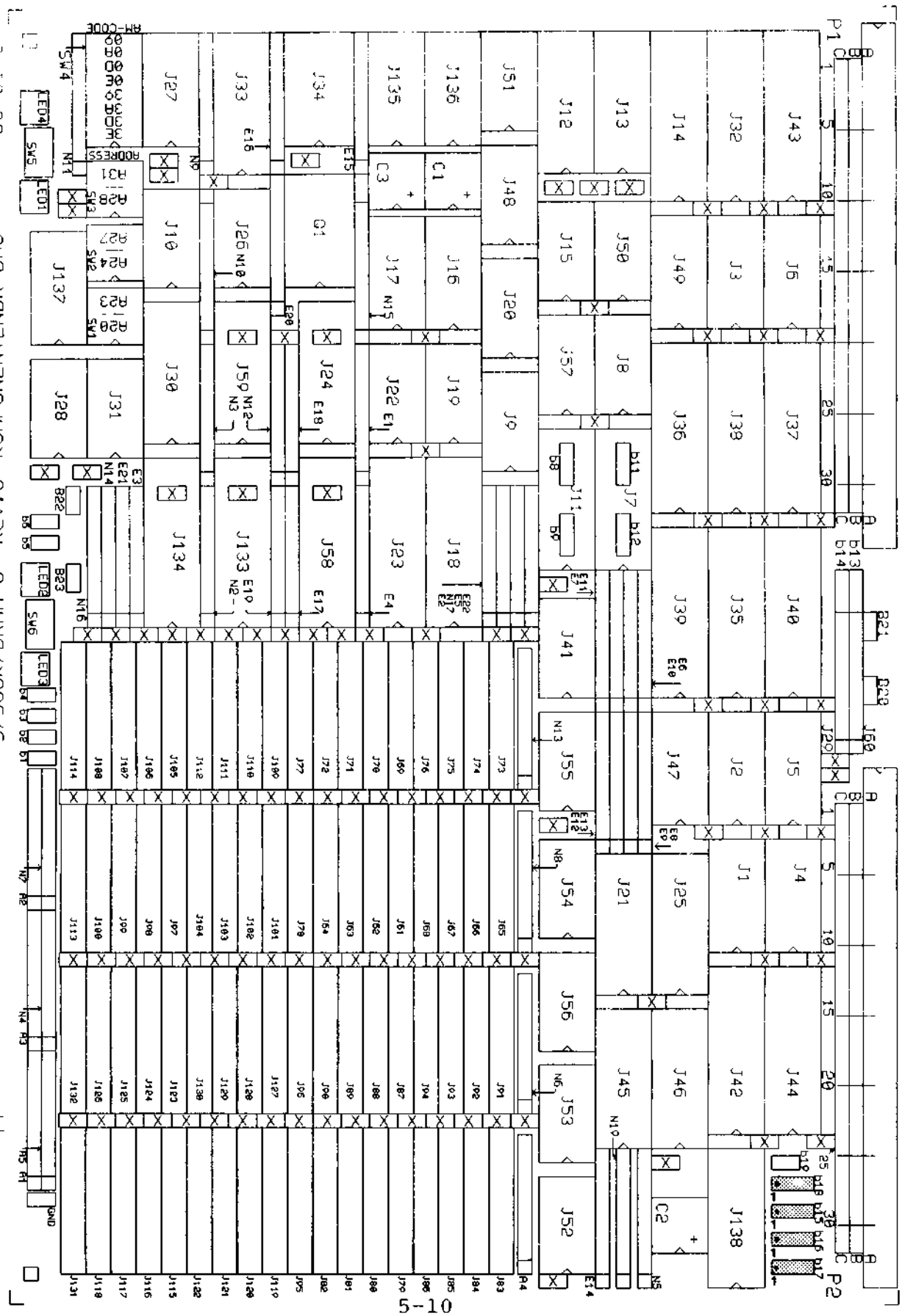
The following table shows the connection of the VMEbus lines to the pins of the bridges:

Table 5-4: Battery Backup Power Pins

VMEbus line name	located at connector/ row-pin	located bridge/pin
+5VSTDBY	P1/b31	b18/3
---	P2/a30	b15/3
---	P2/a31	b16/3
---	P2/a32	b17/3

Figure 5-5 shows the location of solder bridges b15 - b18.

Figure 5-5: Location Diagram of Solder Bridges b15 - b16



5.3 Jumper Settings

There are only three or four jumpers on the board (B20, B21, B22, B23) depending on the board type. They are used to adjust the reset voltage level of the two FORCE Reset Modules (J29, J60), to disable the byte parity error detection and to enable the shared refresh (the last function only for DRAM-8A/C/E).

5.31 Power Down Reset Jumpers (B20,B21)

These Jumpers are used to adjust the transition voltage of the reset modules. The battery backup guarding module J60 (with jumper B21) overrides the system power reset module J29 (with jumper B20). The following table shows the reset voltage of the power down modules.

Table 5-3: Reset Voltage

Jumper (B20 or B21)	Module-Transition-Voltage
IN	4.6V
OUT	4.8V

The jumpers are located between the connectors P1 and P2.

Per Default B20 and B21 are open.

Figure 5-4 shows the location of jumpers B20, and B21.

5.32 Parity Check Disable Jumper (B22)

This Jumper is used to disable the byte parity check if it is plugged in. In this case the activation of the error LED and the BERR* signal is disabled (see 3.7).

The Parity Check is enabled per default.

Figure 5-4 shows the location of jumper B22.

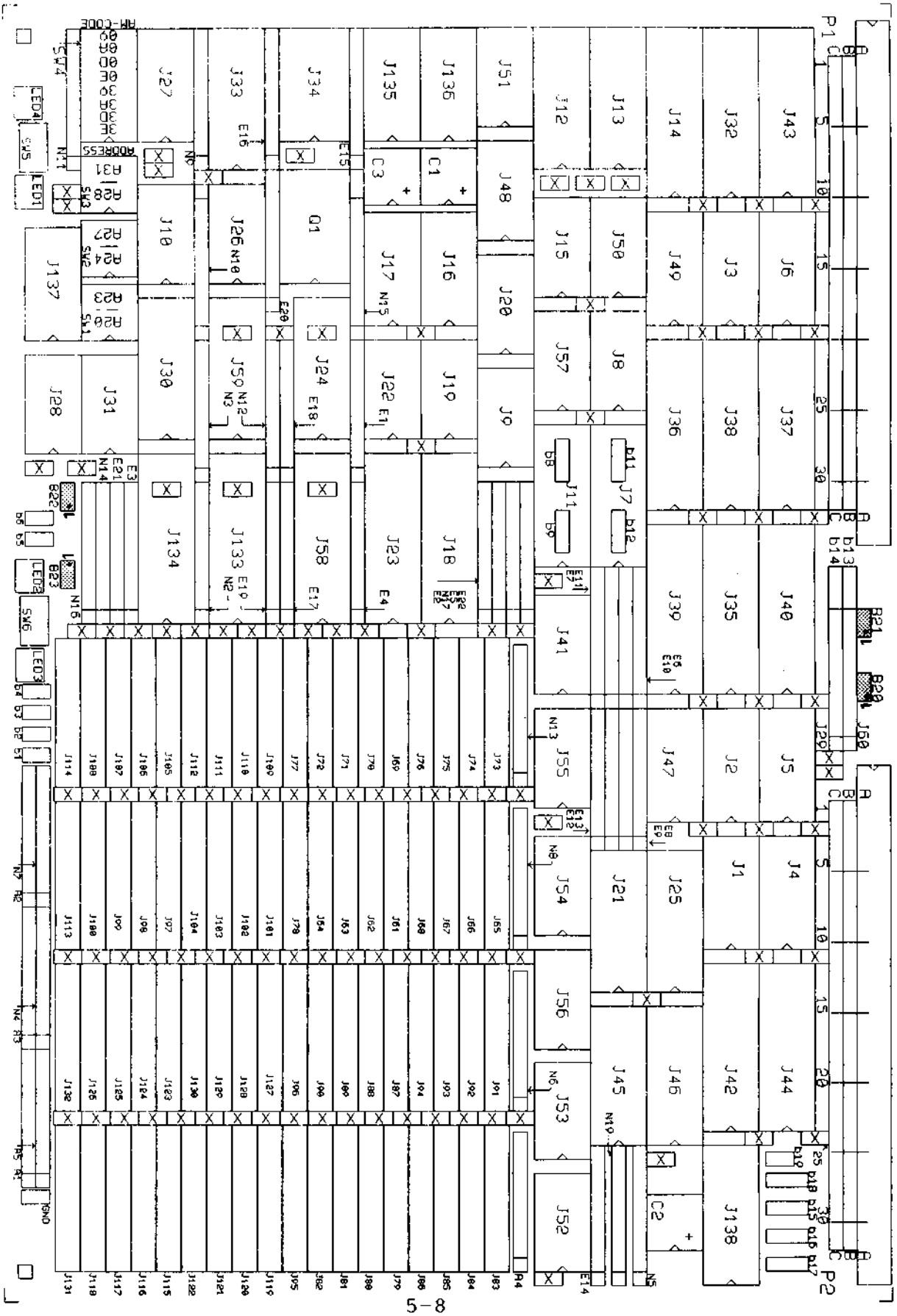
5.33 Shared Refresh Jumper (B23/Only DRAM-8A/C/E)

This Jumper exists only for DRAM-8A/C/E. It is used to double the refresh rate and share the refresh for the two physical RAM Banks, so that one Bank is refreshed after the other. This option reduces the refresh power peak and is useful for the named boards especially in combination with the battery backup option. It is activated if the jumper is open.

The shared refresh is disabled per default.

Figure 5-4 shows the location of jumper B23.

Figure 5-4: Location Diagram of Jumpers B20, B21, B22, B23



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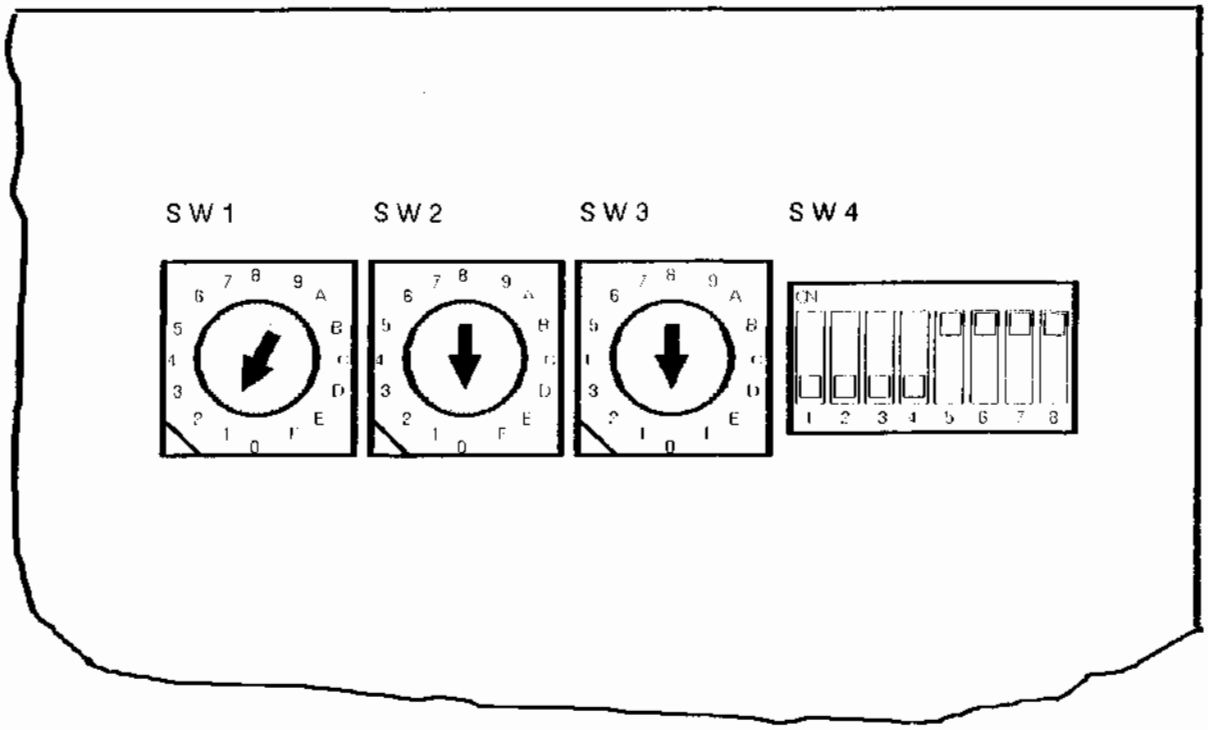
Figure 5-3: Default Settings for Rotary and DIP Switch

The Default Switch Setting consists of:

Start Address: $00100000

Enabled AM-Codes: $09, $0A, $0D, $0E

Observe the diagram below:



5.2.2 Rotary Switches (For Address Selection)

The switches S1, S2 and S3 are used to select the board start address. The switches display a HEX number. This number represents a HEX digit.

The following table shows the VMEbus address lines which are selected by the different rotary switches.

Table 5-2: Address Line Selection

SWITCH	SELECTED ADDRESS LINES	STRUCTURE OF THE HEX-ADDRESS NUMBERS
SW3	A31..A28	$sxxxxxxx
SW2	A27..A24	$xsxxxxxx
SW1	A23..A20	$xxsxxxxx

x: HEX digit, don't care
s: Defines the position of the HEX-digit in the HEX-number

The VMEbus address lines which are selected by a rotary switch are printed on the back side of the PCB at the location of the switch.

The location of the Rotary Switches are shown in Figure 5-2.

Examples:

For the switch position

```
SW3 := 0;
SW2 := 0;
SW1 := 1;
```

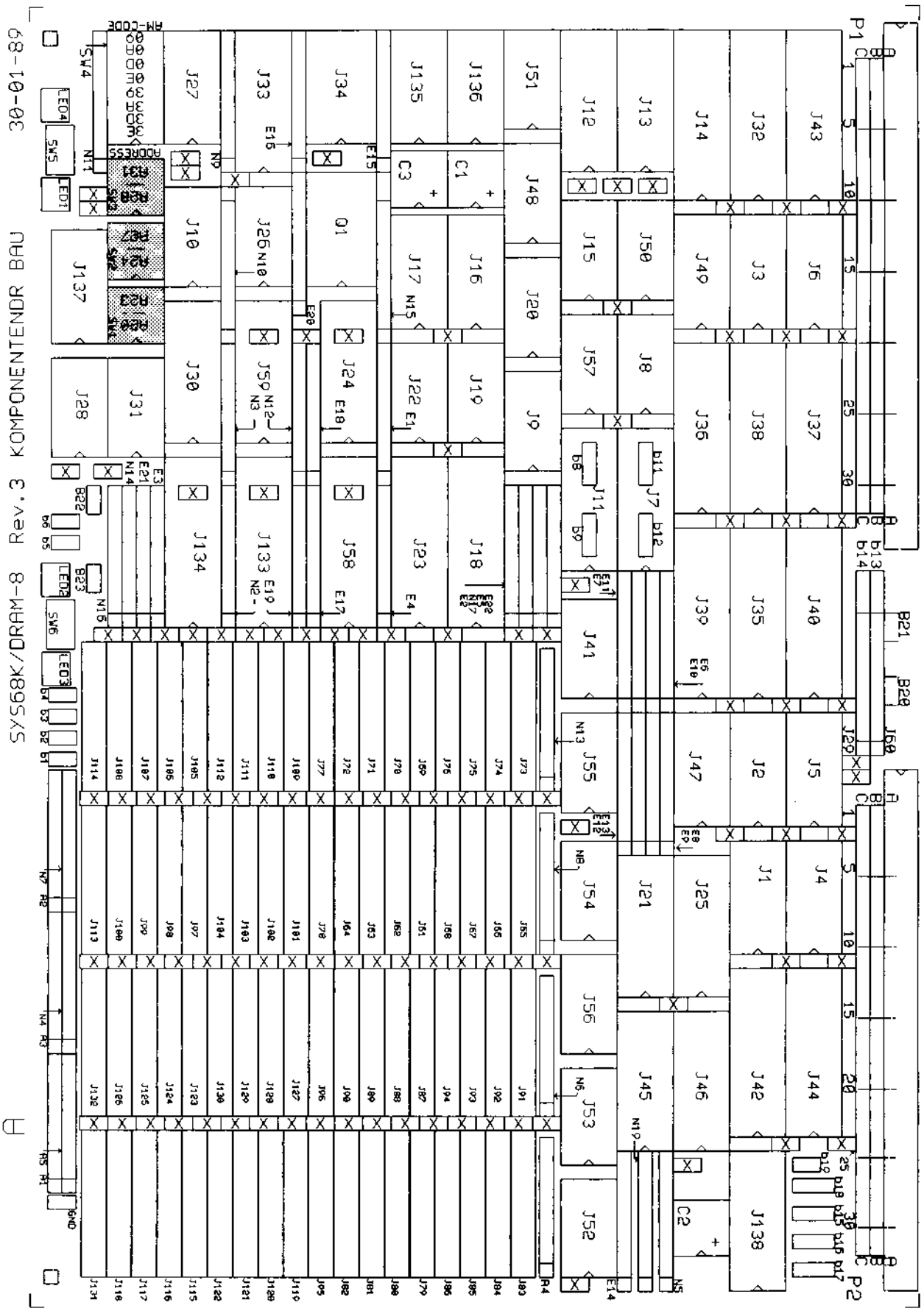
follows the
Start Address: $00100000

The switch position

```
SW3 := F;
SW2 := E;
SW1 := 0;
```

defines the
Start Address: $FE000000
(for A32 address range)

Figure 5-2: Location Diagram of the Rotary Switches



5.2 Onboard Switches

All onboard switches (S1,S2,S3,S4) are placed on the upper corner on the front panel side of the board. The figure on page 5-6 shows the default switch setting.

5.2.1 Dip Switch (For AM Code Selection)

DIP Switch S4 is used to enable the several AM-Codes of the board. More than one AM-Code at a time is possible.

The exact AM-Code function and the switch setting is shown in the following table:

Table 5-1: Supported AM-Codes

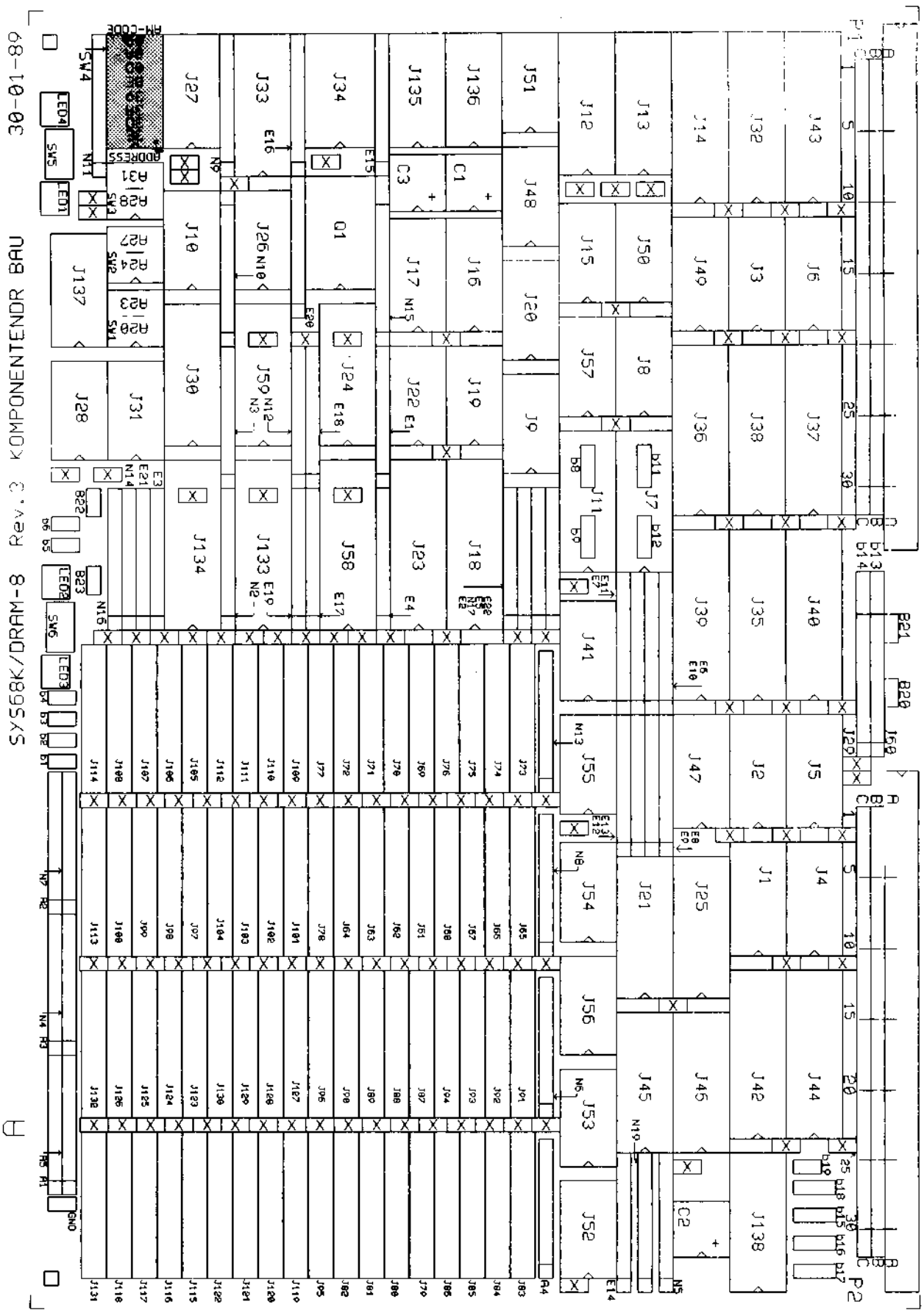
HEX-Code	AM-CODE 543210	FUNCTION	AM-CODE ENABLE SWITCH-POSITION	DEFAULT
3E	HHHHHL	Standard Supervisory Program Access	SW4-1 ON	OFF
3D	HHHHLH	Standard Supervisory Data Access	SW4-2 ON	OFF
3A	HHHLHL	Standard Non-Privileged Program Access	SW4-3 ON	OFF
39	HHHLLH	Standard Non-Privileged Data Access	SW4-4 ON	OFF
0E	LLHHHL	Extended Supervisory Program Access	SW4-5 ON	ON
0D	LLHHLH	Extended Supervisory Data Access	SW4-6 ON	ON
0A	LLHLHL	Extended Non-Privileged Program Access	SW4-7 ON	ON
09	LLHLLH	Extended Non-Privileged Data Access	SW4-8 ON	ON

(**Example**: SW4-1 ON entails that the switch marked "1" in the package SW4 is in the "ON" position).

For better handling the HEX Code of the Address Modifier is also printed on the back side of the board at location SW4.

Figure 5-1 shows the location of the DIP Switches.

Figure 5-1: Location Diagram of the DIP Switches



5. FUNCTION SWITCHES

5.1 Frontpanel Switches

5.1.1 VME Switch

The VME Switch separates the board in the "Up" position from the VMEbus (LOCAL). The "Down" position allows access from the VMEbus (RUN).

The switch is also used to clear the FAIL Indicator (see 4.1 R/L Indicator and 4.2 Fail Indicator).

5.1.2 B1 Switch

The B1 Switch disables the write access to the board. During a write access on the write disabled board, no DTACK* (VME Data Acknowledge line) is driven low and therefore it follows a BERR* low (VMEbus Error line) driven by the timeout of the accessing CPU board (see 4.3 Write Prot. Indicator).

Figure 4-1: Frontpanel of the DRAM



4. DESCRIPTION OF THE LED-INDICATORS

4.1 "R/L" Indicator

The R/L Indicator (RUN/LOCAL) is green if the board is coupled to the VMEbus and red if the board is separated from the VMEbus. (see also VME Switch). If the board is separated no access to the board is possible.

4.2 "Fail" Indicator

The FAIL Indicator displays a red light if a byte parity failure is detected (if parity check is enabled). The LED will be cleared if the VME switch is toggled from "Down" position to "Up" position and back to the "Down" position.

4.3 "Write Prot." Indicator

The board includes a Write Protect Indicator. The Write Prot. LED shines red if the write protect switch (B1) is in the "Up" position.

In this case the board never acknowledges a write cycle (see 5.1.2 B1-Switch).

4.4 "Access" Indicator

The Access Indicator is green while the board is being accessed from the VMEbus. A higher access rate is indicated by brighter light.

3.9 The Battery Backup Option

The DRAM-8 can be powered from the +5V main power of the VME motherboard only, or by Battery Backup Power and Main Power.

In the "Power Down" case, the Battery Backup protects the board against loss of data.

The Battery Backup Power drives the complete refresh logic but not the VME Interface.

The Battery Backup side of the board has it's own Power down reset module (see also chapter RESET GENERATOR and POWER DOWN RESET JUMPER).

To ensure proper function, the user is responsible for maintaining a constant Battery Backup Power in accordance with IEEE 1014* Standard. Therefore the most important data is shown in the table below:

Table 3-6: Battery Backup Voltage Conditions

Min. Voltage	Max. Voltage	Ripple/Noise below 10 Mhz (peak-to-peak)
4.875V	5.25V	50mV

For installing these options, please see 5.4, Battery Backup Power Bridges.

3.8 Reset Generator

The reset is used to initialize the board or paths of the board. The reset is driven from two FORCE FH001 (J29,J60) modules. One module (J60) drives the reset for the parts of the board which are used to drive the refresh. The other module (J29) resets the rest of the board (such as the parts of the VMEbus interface). This module is overridden by the first one. The second module also resets if a VMEbus SYSRESET* is pending.

If the battery backup is used, the first module (J60) controls the backup power and the second module (J29) controls the normal VMEbus power and the SYSRESET*.

The modules can be jumpered to different transition voltages. These are described in the following table.

Table 3-5: Approximate Power Down Transition Voltage

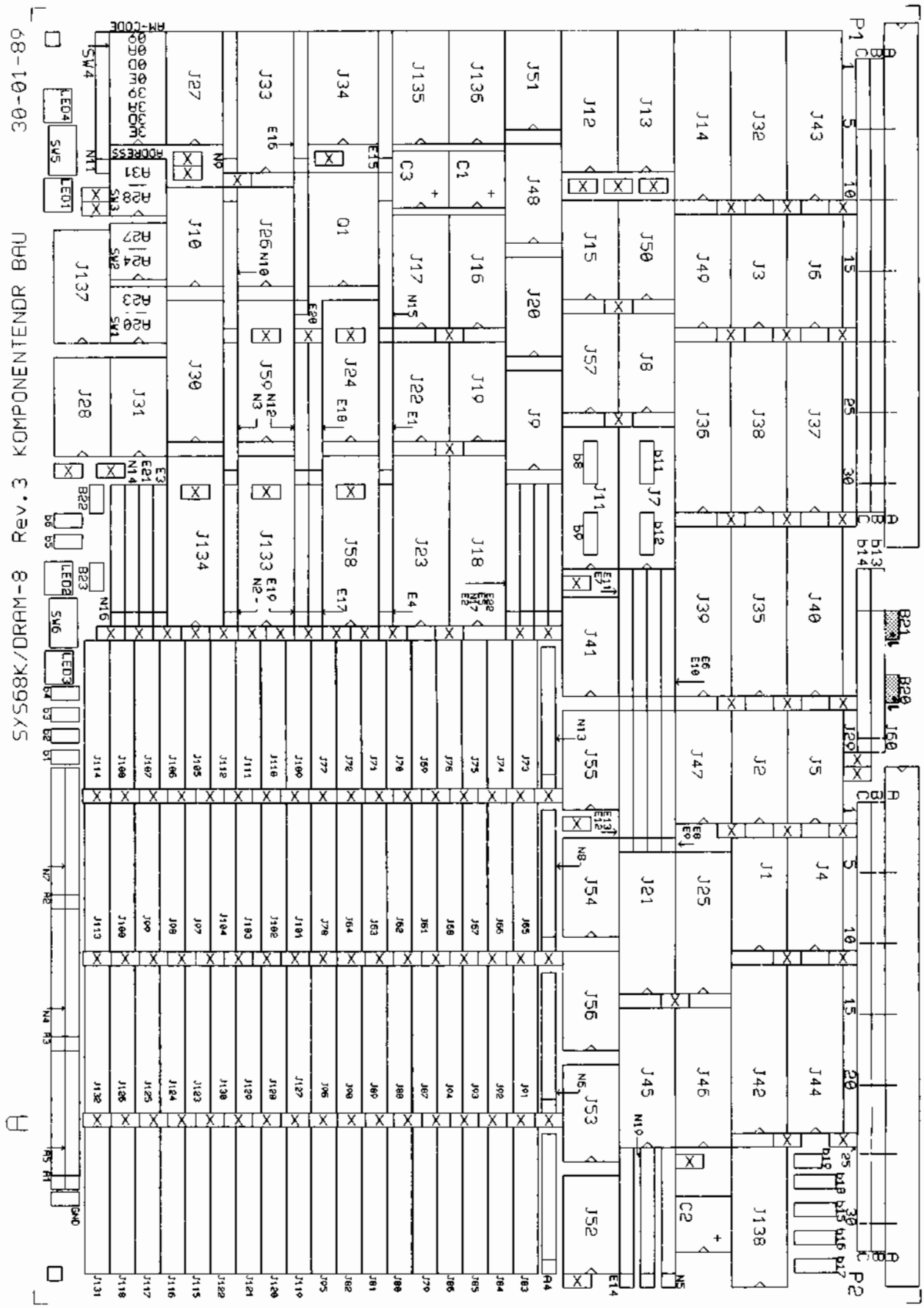
JUMPER B21 (for J60)	JUMPER B20 (for J29)	BATTERY TRANSITION VOLTAGE #	NORMAL POWER TRANSITION VOLTAGE
OUT	OUT	4.8	4.8
OUT	IN	4.8	4.8
IN	OUT	4.6	4.8
IN	IN	4.6	4.6

:= Only if Battery Backup Option is used. Otherwise the values for Normal Power are valid.

For more information see chapter 5.3.1.

The location diagram B20 and B21 is shown in Figure 3-1.

Figure 3-1: Location Diagram of Jumpers B20 and B21



3.7 The Error Detection

The DRAM-8x includes error detection circuits which allow single bit error detection for each byte.

For error detection, a byte parity bit must first be generated during a write cycle. This parity bit is stored in common with the data byte.

In conclusion to reading the parity of each byte the parity bit is tested. The result of this test is used to generate the DTACK* signal (if no single bit error is recognized) or to drive BERR* (if a single byte error is known).

This function can be disabled via the jumper setting.

For more detailed information, please refer to chapter 5.3.2, Parity Check Disable Jumper.

3.6 The RAM Area

The DRAM Area is constructed of different types of DRAM devices relevant to the type of board.

The following table shows the type and number of DRAM devices for each type of board:

Table 3-4: DRAM Devices

Type of Board	Data Devices Type/Number	Parity Devices Type/Number
DRAM-8A	256k*4/16	1M*1/4 or 256k*1/8
DRAM-8B	1M*1/32	1M*1/4
DRAM-8C	1M*1/64	1M*1/8
DRAM-8D	4M*1/32	4M*1/4
DRAM-8E	4M*1/64	4M*1/8

3.5 Refresh Cycle

Two Refresh Timings are supported. Normally a refresh is pending every 15us. This is a common time for all physical DRAM Banks (DRAM-8B/D one bank, DRAM-8A/C/E two banks). Upon a shared refresh installation (possible for DRAM-8A/C/E), only an alternate refresh may be supplied to one bank at a time. With this function a refresh is pending every 7.5us, refreshing alternately only one of the two RAM banks. This option is helpful to reduce the refresh current peak.

A refresh cycle has priority over an external access. If a VME access is running and a refresh is pending, the refresh cycle follows after the internal RAM access is terminated.

The max. refresh overhead is 320ns (with 120ns DRAMs).

3.4 Read/Write Access Cycle

The DRAM-8 is a synchronous board. If the external VMEbus access appears synchronous to the internal board clock, the access time follows the lower time border according to the table below.

If the external access is asynchronous to the internal clock, the upper border is the maximum access time for a pending access. Between these typical two time borders an access (without refresh) is possible with equal probability.

If a refresh cycle is running, a pending VMEbus access must wait until the refresh is terminated. Therefore it follows a refresh overhead time which in this case increases the access time.

The following table shows the access times (with 120ns DRAMs).

Table 3-3: Read/Write Access Times

Access	lower	average	upper
typ. WRITE	60ns	80ns	100ns
typ. READ	210ns	230ns	250ns
			maximum
WRITE with refresh			430ns
READ with refresh			580ns

These access times are defined from the low passage of the DS0* and DS1* strobes to the low passage of the DTACK* on the VMEbus.

Due to the interleaved structure of the board, a new bus access can be pending when the internal cycle is ready to function.

3.3 Address Range

The address range expands beyond the full size of the VMEbus. The start address can be switched by increments of 1 Mbyte starting at address $00000000. The memory capacity is reduced if the memory capacity is greater than the usable address range. The following examples show this condition.

Example for the DRAM-8C (8 Mbytes) with A32 address range:

Start Address	End Address	Usable Memory
$FF800000	$FFFFFFFF	8 Mbytes
$FF900000	$FFFFFFFF	7 Mbytes

Example for the DRAM-8C (8 Mbytes) with A24 address range:

Start Address	End Address	Usable Memory
$xx800000	$xxFFFFFF	8 Mbytes
$xx900000	$xxFFFFFF	7 Mbytes
x := don't care		

For address range selection see also 5.2.2 ROTARY SWITCHES.

3.2 Address Modifier Implementation

The AM-Codes are in close connection with the transfer types.

The table below shows the supported AM-Codes.

Table 3-2: Supported AM-Codes

HEX-Code	AM-CODE 543210	FUNCTION	AM-CODE ENABLE SWITCH-POSITION
3E	HHHHHL	Standard Supervisory Program Access	SW4-1 ON
3D	HHHHLH	Standard Supervisory Data Access	SW4-2 ON
3A	HHHLHL	Standard Non-Privileged Program Access	SW4-3 ON
39	HHHLLH	Standard Non-Privileged Data Access	SW4-4 ON
0E	LLHHHL	Extended Supervisory Program Access	SW4-5 ON
0D	LLHHLH	Extended Supervisory Data Access	SW4-6 ON
0A	LLHLHL	Extended Non-Privileged Program Access	SW4-7 ON
09	LLHLLH	Extended Non-Privileged Data Access	SW4-8 ON

For AM-Code selection see also 5.2.1 DIP Switches.

The AM-Codes are decoded in a PAL device.

3. FUNCTIONAL DESCRIPTION

3.1 Supported Transfer Types

The SYS68K/DRAM-8x is capable of transferring 8, 16, 24 or 32 bits of data. The VMEbus/1014* Standard defines the transfer types as well as the number of bytes to be transferred. All important predefined transfer types in the VMEbus/1014* Standard (except short and block transfers) are supported.

All transfer types supported by the DRAM-8 are listed in the table below.

Table 3-1: Supported Transfer Types of the DRAM-8x

	D24-D31	D16-D23	D8-D15	D0-D7	supported also as RMW cycle
A32:D32	x	x	x	x	x
A32:D16	-	-	x	x	x
A32:D8	-	-	x	-	x
	-	-	-	x	x
A32:UAT	x	x	x	-	x
	-	x	x	-	x
	-	x	x	x	x
A24:D32	x	x	x	x	x
A24:D16	-	-	x	x	x
A24:D8	-	-	x	-	x
	-	-	-	x	x
A24:UAT	x	x	x	-	x
	-	x	x	-	x
	-	x	x	x	x

The board access is not driven by address only cycles. Therefore there is no conflict with this type of bus access.

The selected address modifier code defines the decoding range (A24 or A32) of the memory.

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2. GENERAL OPERATION

The SYS68K/DRAM-8x contains the VMEbus interface according to IEEE 1014* (VMEbus Rev.C). Also included is a logic for timing, controlling, refresh, board selection and parity check. The DRAM area consists of up to 32 Mbytes RAM.

Easy access address selection by increments of 1 Mbyte is provided through rotary switches. Eight AM Codes are selectable via DIP switches. The front panel switches allow separation from the VMEbus and write protection of the DRAM.

If the parity error check is enabled and an error is detected, the BERR* VMEbus signal is activated.

If a write protected DRAM-8 board is in the write access mode, the DTACK* signal will not terminate the cycle. In this case the access must be terminated by the timeout Logic of the accessing master board.

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1. GENERAL INFORMATION

This high performance VMEbus based memory board combines the high RAM capacity of dynamic RAM devices with a high data throughput based on the design of the board. There are memory capacities up to 32 Mbytes and access times of 80ns for write or 230ns for read are possible.

Error detection secures against single bit failures. Write protection and board separation by front panel switches ensures high performance for program and system development.

Easy handling by the user is guaranteed by the use of rotary and DIP switches for important initializations.

The DRAM-8x has been designed for memory expansion, mass storage, backup storage, software development, as well as other design features.

The photo of the SYS68K/DRAM-8C (see Figure 1-1 in Section 1) shows the board in detail. The other members of the board family resemble the DRAM-8C with exception to the DRAM area. Section 1, Figure 1-2 shows the block diagram of the DRAM-8x.

This manual provides a general operating description of the SYS68K/DRAM-8x. Follow the installation instructions for use and troubleshooting (see "INSTALLATION", Section No. 2).

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HARDWARE USER'S MANUAL

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2.6 Power On

If the board is correctly installed, and the switches are in the correct positions, the power for the VMEbus rack can be switched on.

Initially the green R/L LED will light up.

Before reading data from an address range the board must be initialized first by writing to this address range. Otherwise a BERR* (buserror) may be driven by byte parity check, due to the fact that DRAMs contain undefined information during power up.

2.5 Installation in the Rack

The board can immediately be mounted at slot 2 or higher.

CAUTION:

1) Switch off power before installing the board to avoid electrical damages to the components.

2) The DRAM-8x has a special ejector (the handles). The board has to be plugged in and the screws on the front panel must be secured to guarantee proper installation.

3) All +5V and GND pins of the P1 and P2 connectors must be supplied with the correct power.

4) Ensure that no address range conflicts with other existing boards.

2.4 Jumper Setting

The DRAM board contains three or four jumpers depending on its type. These Jumpers influence the refresh rate (only DRAM-8A/C/E), parity error check and power down reset.

Per default the Jumper B23 is inserted on DRAM-8A/C/E. On DRAM-8B/D B23 is closed via solderbridge. The parity error check is enabled. The power down reset is driven at 4.8V. A refresh is pending every 15us.

Figure 5-4 of the Hardware User's Manual shows the location of the jumpers.

2.3 Dip Switches (For AM-Code Selection)

The board contains a DIL-package (SW4) with eight switches which are used to enable the AM-Codes.

The switch number and the "On" position are marked on the switch package.

Table 2-3: Supported AM-Codes

HEX-Code	AM-CODE 543210	FUNCTION	AM-CODE ENABLE SWITCH-POSITION
3E	HHHHHL	Standard Supervisory Program Access	SW4-1 ON
3D	HHHHLH	Standard Supervisory Data Access	SW4-2 ON
3A	HHHLHL	Standard Non-Privileged Program Access	SW4-3 ON
39	HHHLLH	Standard Non-Privileged Data Access	SW4-4 ON
0E	LLHHHL	Extended Supervisory Program Access	SW4-5 ON
0D	LLHHLH	Extended Supervisory Data Access	SW4-6 ON
0A	LLHLHL	Extended Non-Privileged Program Access	SW4-7 ON
09	LLHLLH	Extended Non-Privileged Data Access	SW4-8 ON

Per default the switches SW4-5 to SW4-8 are in the "On" position, and the switches SW4-1 to SW4-4 are "OFF". This ensures that the Extended AM-Codes are enabled.

The default setting is shown in Figure 2-1, page 2-2.

2.2 Rotary Switches (For Address Selection)

The rotary switches are installed to define the start address of the board. The end address is generated automatically. The default start address of every board is switched to $00100000. The address range is contiguous.

Table 2-1: Default Rotary Switch Setting

Switch	Hex Code
SW3	0
SW2	0
SW1	1

The default position of the rotary switches is shown in the figure on the previous page.

The default start and end addresses for the different board types are shown in the table below:

Table 2-2: Default Address Range

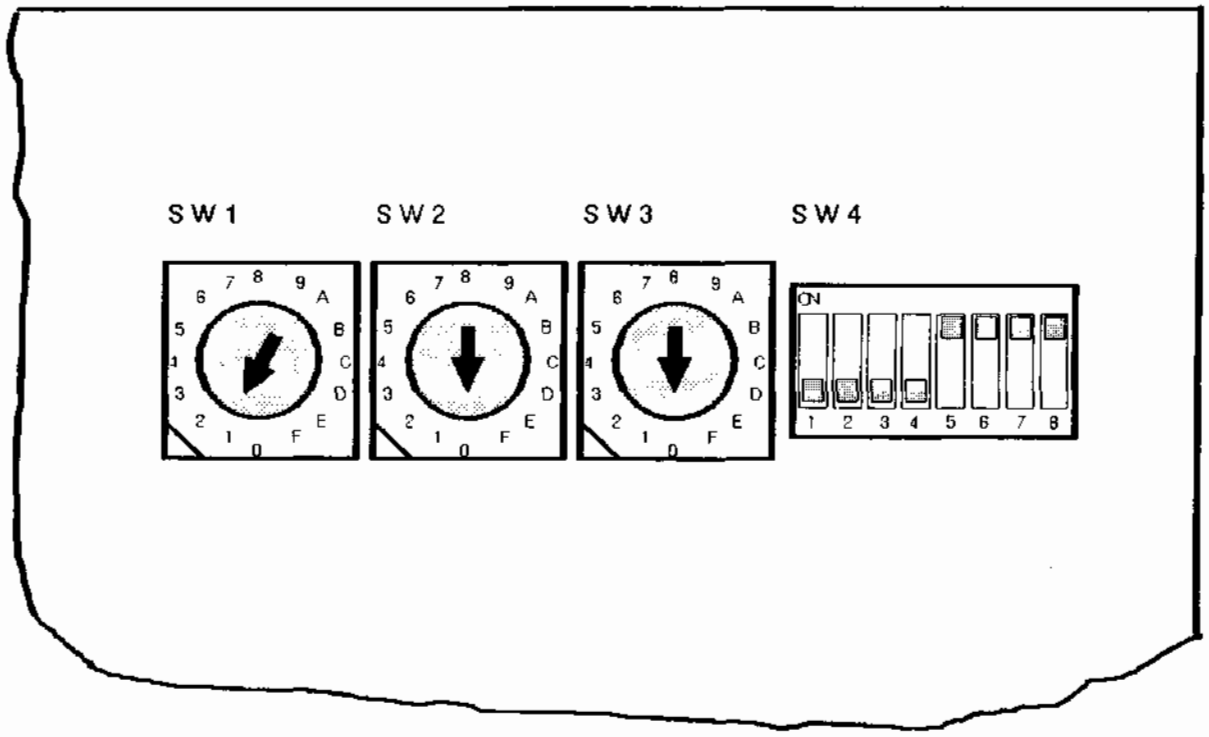
Board	Start Addr.	End Addr.
DRAM-8A	$00100000	$002FFFFF
DRAM-8B	$00100000	$004FFFFF
DRAM-8C	$00100000	$008FFFFF
DRAM-8D	$00100000	$010FFFFF
DRAM-8E	$00100000	$020FFFFF

Figure 2-1: Default Switch Setting

The Default Switch Setting consists of:

Start Address:	$00100000
Enabled AM-Codes:	$09, $0A, $0D, $0E

Observe the diagram below:



2. FUNCTION SWITCHES

2.1 Frontpanel Switches

The board contains two front panel switches listed from top to bottom:

VME

B1

The two positions of each switch are defined as "Up" and "Down".

All front panel switches must be set to the "Down" position for initial installation.

Please toggle both switches before installing the board in the rack, to detect damages to the switches during transport.

Figure 1-1: Front Panel of the DRAM-8x



1. GENERAL OVERVIEW

Easy installation of the DRAM-8 boards is provided because all switches and jumper settings are designed to access the board under standard conditions. The boards are configured to be directly accessed via the extended address range in the user and supervisor mode for program and data access starting at $00100000. The byte parity check is enabled.

Eventually changes in the setup parameters will be easily performed by switches and jumpers (in this case consult the Hardware Users Manual, Section No. 3).

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W A R N I N G

TO AVOID MALFUNCTIONS AND COMPONENT DAMAGES, PLEASE READ THE COMPLETE INSTALLATION PROCEDURE BEFORE THE BOARD IS INSTALLED IN A VMEBUS ENVIRONMENT.

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INSTALLATION

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8. HISTORY OF MANUAL REVISIONS

Revision No.	Description	Date of Last Change
0	First Print	MAR/01/1989
1	Section 3, "Hardware User's Manual", Chapter 5.3.3: Jumper description has been changed from **closed** to **open**. Section 5, "Default Jumper Settings", Chapter 4: Jumper B23 is changed from **closed** to **open**.	SEP/12/1990
2	Section 2, "Installation", Chapter 2.4: Per default the **Jumper B23** is inserted **on DRAM-8A/C/E. On DRAM-8B/D B23 is closed via solderbridge.** Section 3, "Hardware User's Manual", Chapter 3.5: **With this function a refresh is pending every 7.5 us, refreshing alternately only one of the two RAM banks.** Section 5, "Default Jumper Settings", Chapter 4: The reset voltage is set to 4.8V if the jumpers B20 and B21 are **open**. The default jumper setting for B23 is changed from **open** to **closed**.	MAR/11/1991

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7. ORDERING INFORMATION

SYS68K/DRAM-8A	2 Mbyte DRAM board for 32/24 bit address and 32 bit data including documentation
SYS68K/DRAM-8B	4 Mbyte DRAM board for 32/24 bit address and 32 bit data including documentation
SYS68K/DRAM-8C	8 Mbyte DRAM board for 32/24 bit address and 32 bit data including documentation
SYS68K/DRAM-8D	16 Mbyte DRAM board for 32/24 bit address and 32 bit data including documentation
SYS68K/DRAM-8E	32 Mbyte DRAM board for 32/24 bit address and 32 bit data including documentation
SYS68K/DRAM-8/UM	User's Manual for the SYS68K/ DRAM-8 board

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Figure 6-2: Location Diagram of DRAM-8

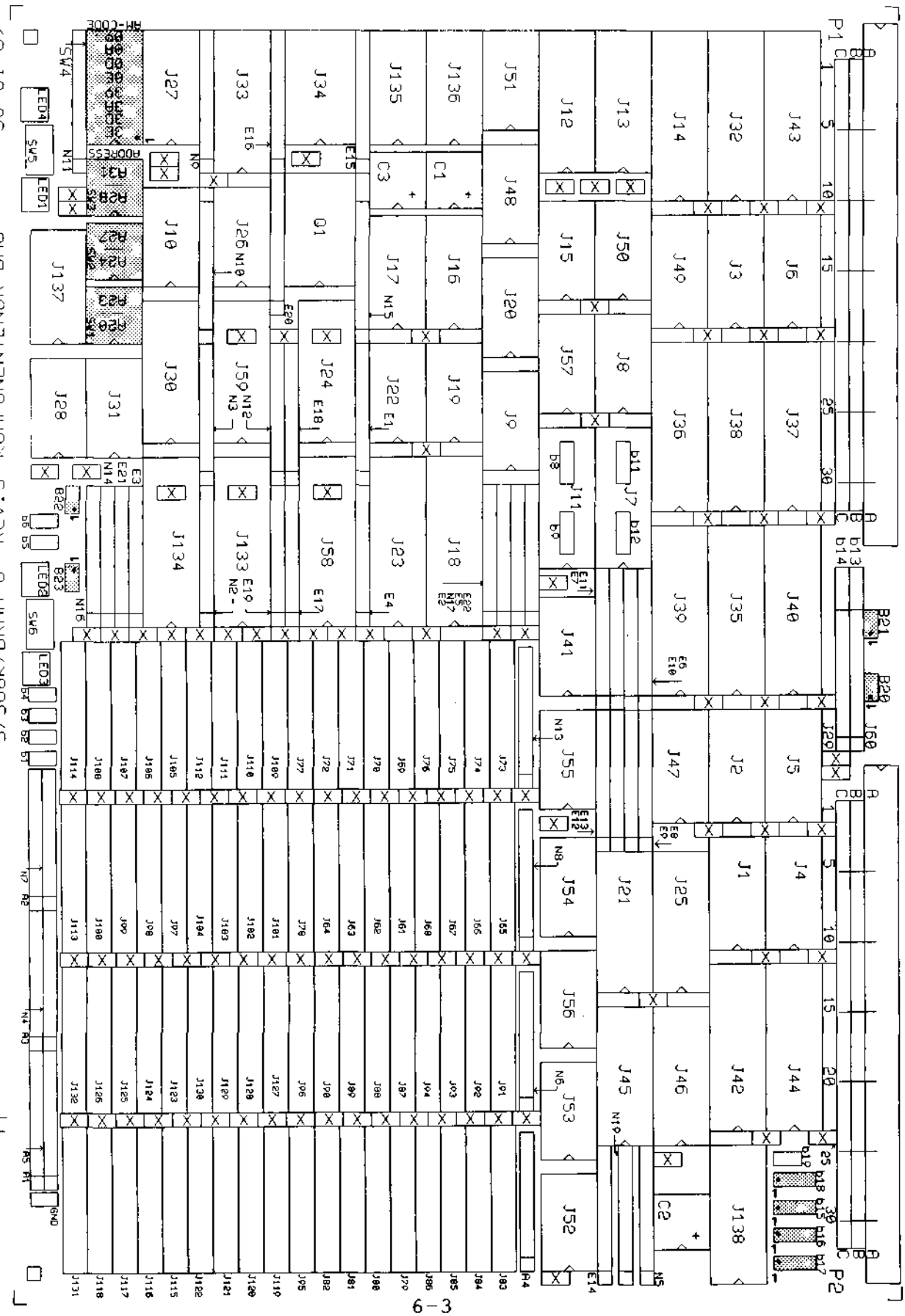


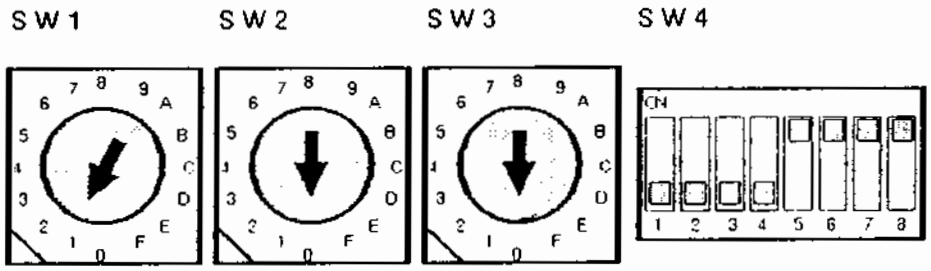
Figure 6-1: Default Settings for Rotary and DIP Switches

The Default Switch Setting consists of:

Start Address: **$00100000**

Enabled AM-Codes: **$09, $0A, $0D, $0E**

Observe the diagram below:



6. DEFAULT JUMPER SETTINGS

The following explanations refer to the factory default jumper settings.

The reset voltage is adjusted to 4.8V by the open Jumpers B20 and B21.

The byte parity check is enabled by the open Jumper B22.

A common refresh for both physical RAM banks is enabled by a closed Jumper B23 (only DRAM-8 A/C/E).

The start address is adjusted to $100000 by the rotary switches SW1, SW2 and SW3.

The Extended AM-Codes are enabled by the DIP switch SW4.

Figure 6-1 shows the Default Switch Setting.

Figure 6-2 on page 6-3 shows the location diagram of the DRAM-8.

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5. THE DRAM-8x FAMILY

The DRAM-8x family consists of five boards differing mainly in memory capacity. These boards are listed in the table below.

Table 5-1: DRAM-8x Family

TYPE	MEMORY CAPACITY
DRAM-8A	2 Mbytes
DRAM-8B	4 Mbytes
DRAM-8C	8 Mbytes
DRAM-8D	16 Mbytes
DRAM-8E	32 Mbytes

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4. AM-CODES

The following eight AM-Codes are supported :

Table 4-1: Supported AM-Codes

HEX-Code	AM-CODE 543210	FUNCTION
3E	HHHHHL	Standard Supervisory Program Access
3D	HHHHLH	Standard Supervisory Data Access
3A	HHHLHL	Standard Non-Privileged Program Access
39	HHHLLH	Standard Non-Privileged Data Access
0E	LLHHHL	Extended Supervisory Program Access
0D	LLHHLH	Extended Supervisory Data Access
0A	LLHLHL	Extended Non-Privileged Program Access
09	LLHLLH	Extended Non-Privileged Data Access

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3. TRANSFER TYPES

The DRAM-8x VMEbus interface allows the following transfers:

Table 3-1: Supported Transfer Types of the DRAM-8x

	D24-D31	D16-D23	D8-D15	D0-D7	supported also as RMW cycle
A32:D32	x	x	x	x	x
A32:D16	-	-	x	x	x
A32:D8	-	-	x	-	x
	-	-	-	x	x
A32:UAT	x	x	x	-	x
	-	x	x	-	x
	-	x	x	x	x
A24:D32	x	x	x	x	x
A24:D16	-	-	x	x	x
A24:D8	-	-	x	-	x
	-	-	-	x	x
A24:UAT	x	x	x	-	x
	-	x	x	-	x
	-	x	x	x	x

The board is not selected by address only cycles.

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2. FEATURES

- Compatible to IEEE 1014* Standard (VMEbus Rev.C)
- Up to 32 Mbytes of memory
- All 32 address and data lines of the VMEbus are supported
- VMEbus Interface:

  A32: D32, D16, D8, ADO, UAT, RMW
  A24: D32, D16, D8, ADO, UAT, RMW

- Address selectable in increments of 1 Mbyte
- 8 AM Codes
- Automatic data transfer line adjustment
- Automatic address range adjustment
- Write access time type. 80ns (with 120ns DRAMs)
- Read access time type. 230ns (with 120ns DRAMs)
- Interleaved refresh pending every 15µs
- Refresh overhead max. 320ns (with 120ns DRAMs)
- VME switch for board separation from VMEbus
- R/L (RUN/LOCAL) indicator LED
- FAIL indicator LED for parity errors
- Write protect switch for saving memory information against overwriting
- WRITE PROT. indicator LED
- ACCESS LED for indication of board access from the VMEbus
- Jumperable parity generation and check
- Memory backup possible by external power supply

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Figure 1-2: Block Diagram of the DRAM Board

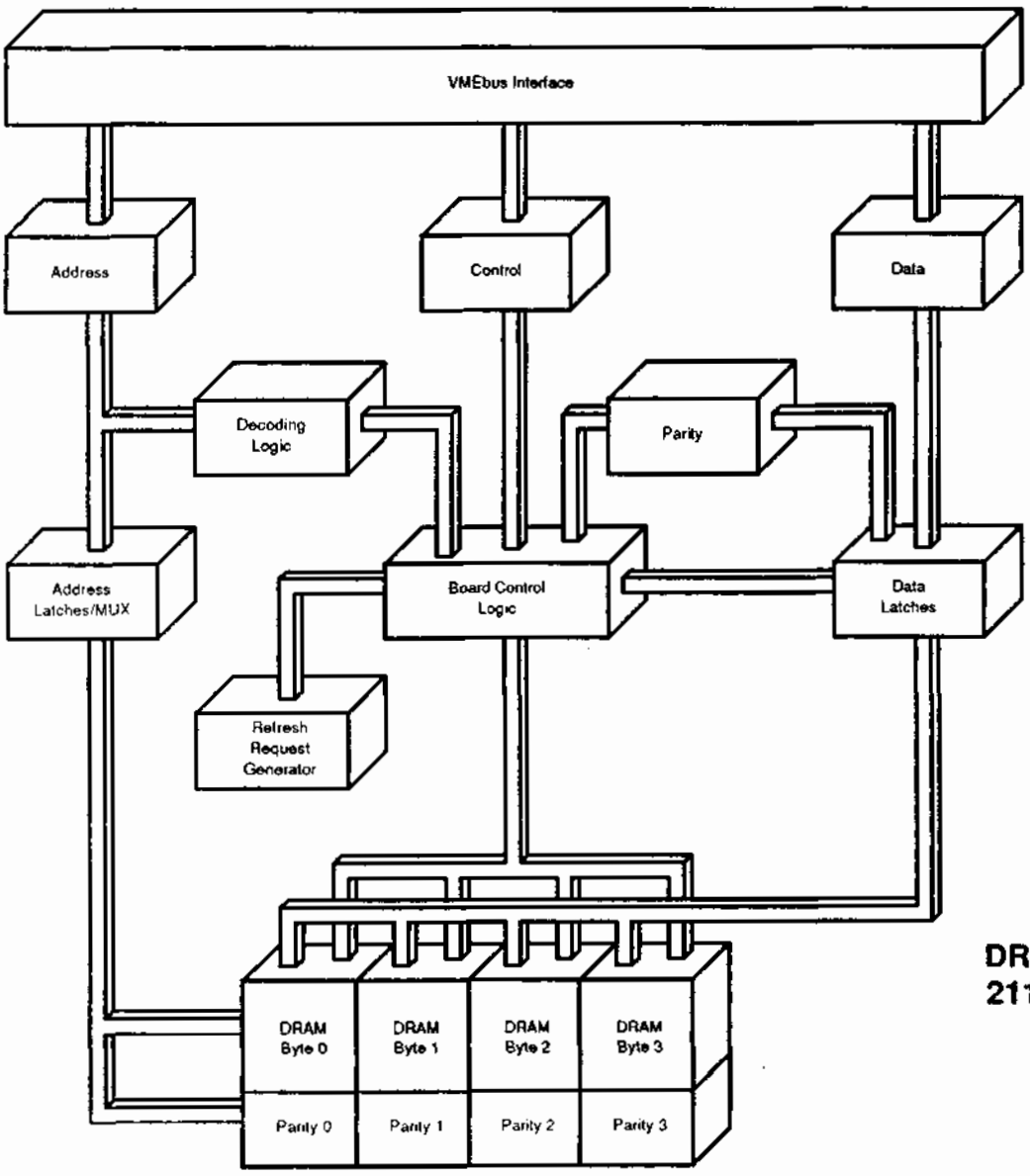
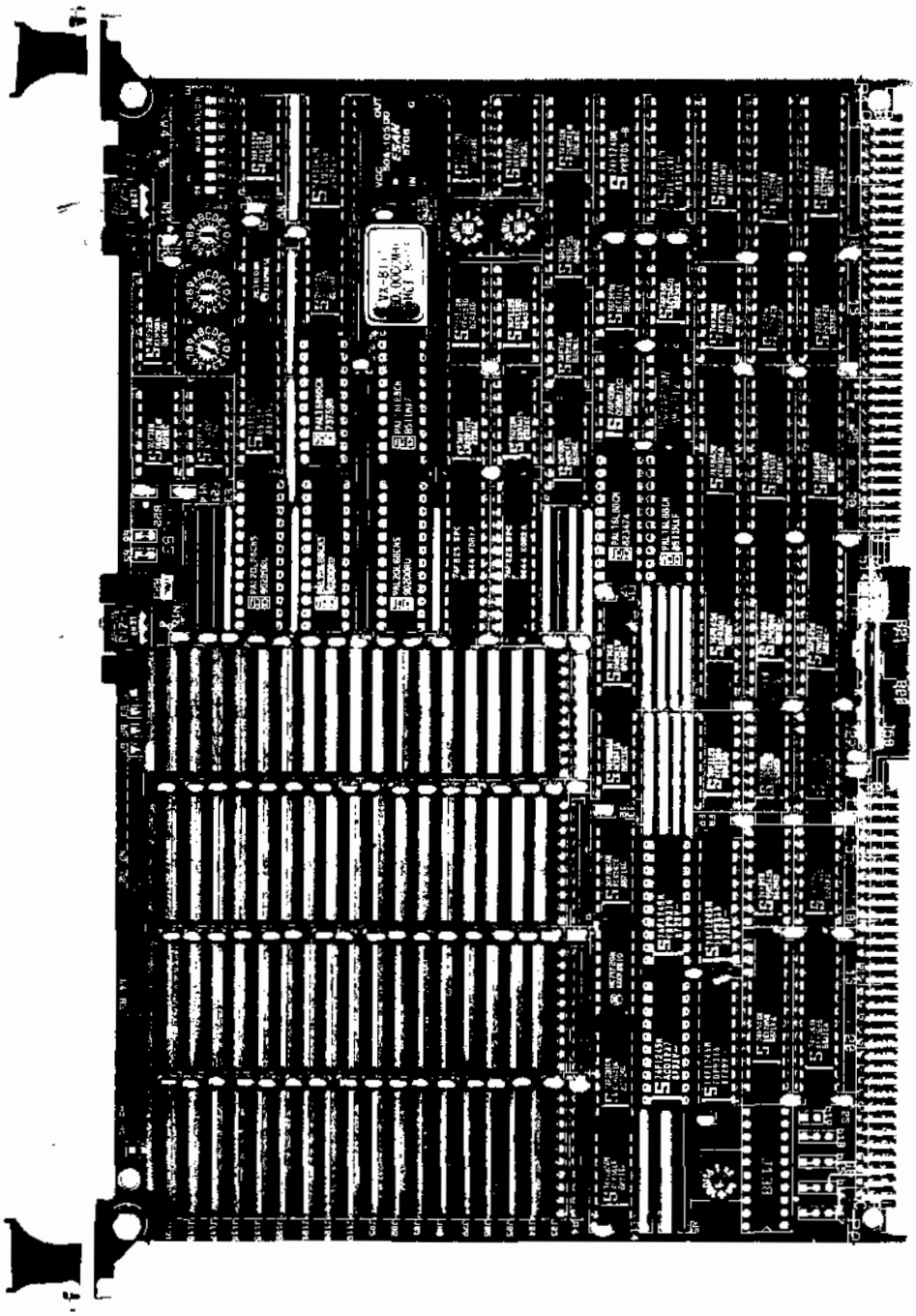


Figure 1-1: Photo of the DRAM Board



1. GENERAL INFORMATION

The SYS68K/DRAM-8x is a family of high speed, high capacity memory extensions to the VMEbus.

This board functions in accordance with the IEEE 1014* Standard (VMEbus Rev.C).

It uses dynamic RAM devices for reaching high memory capacity with low costs. The DRAM refresh is driven under control of the board with minimal refresh overhead.

The design of the board allows maximum data throughput and a high speed VMEbus read/write access.

Single bit error detection is implemented via byte parity generation and check.

The User Interface is designed for easy handling and high performance of the board.

Memory information backup is supported by external supply.

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N O T E

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INTRODUCTION

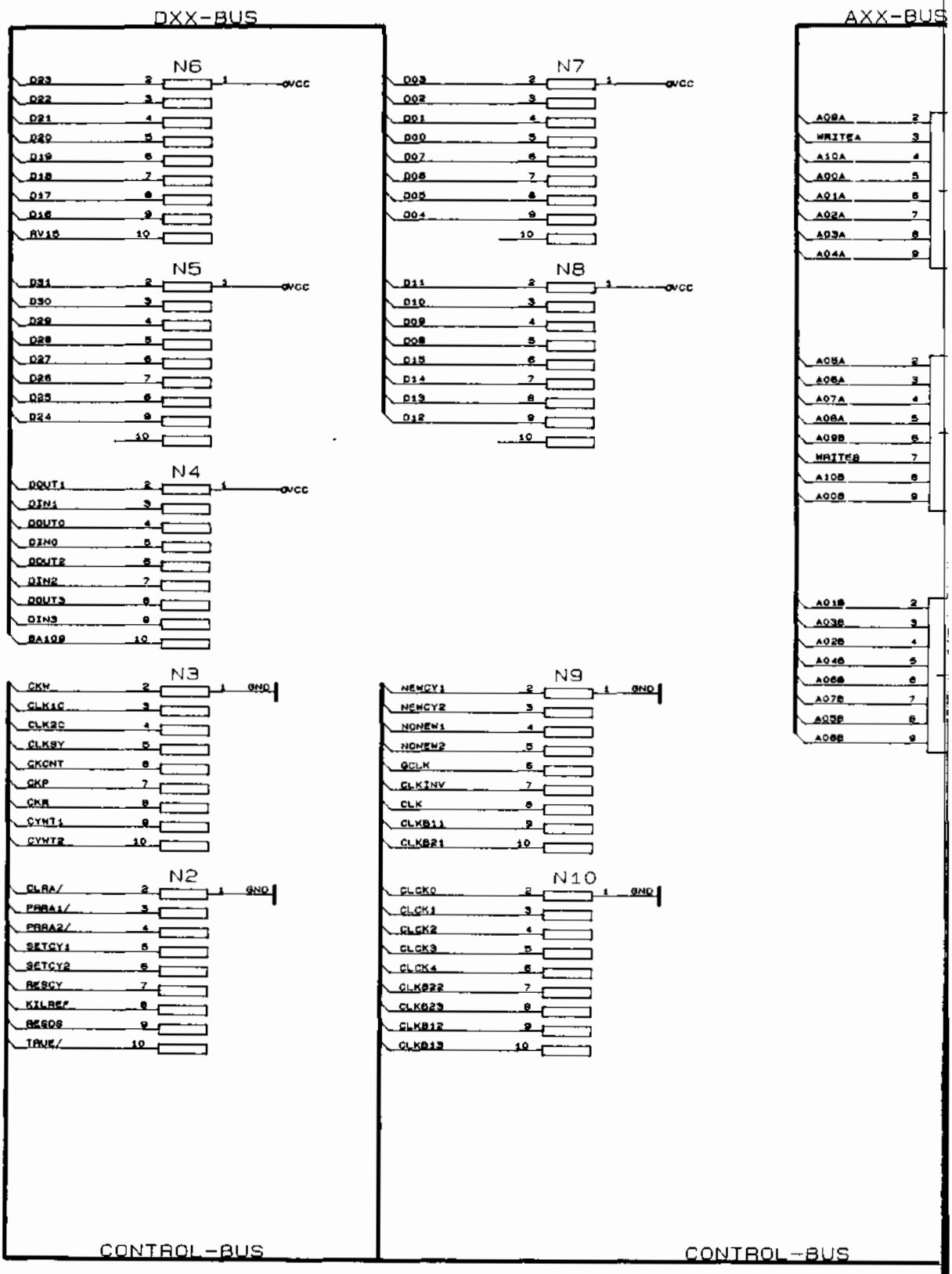
SYS68K/DRAM-8
USER'S MANUAL

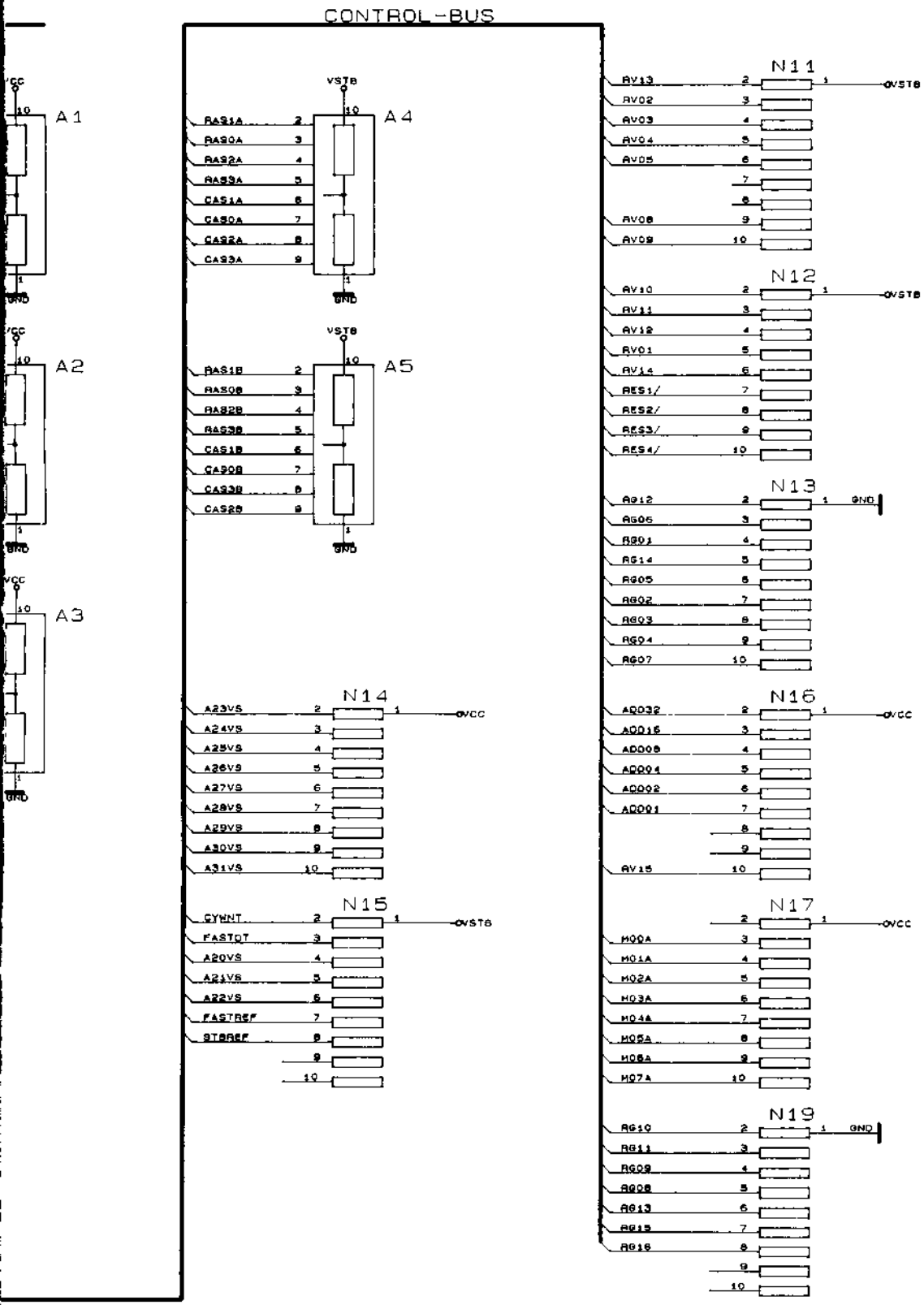
Revision No. 2
March 1992

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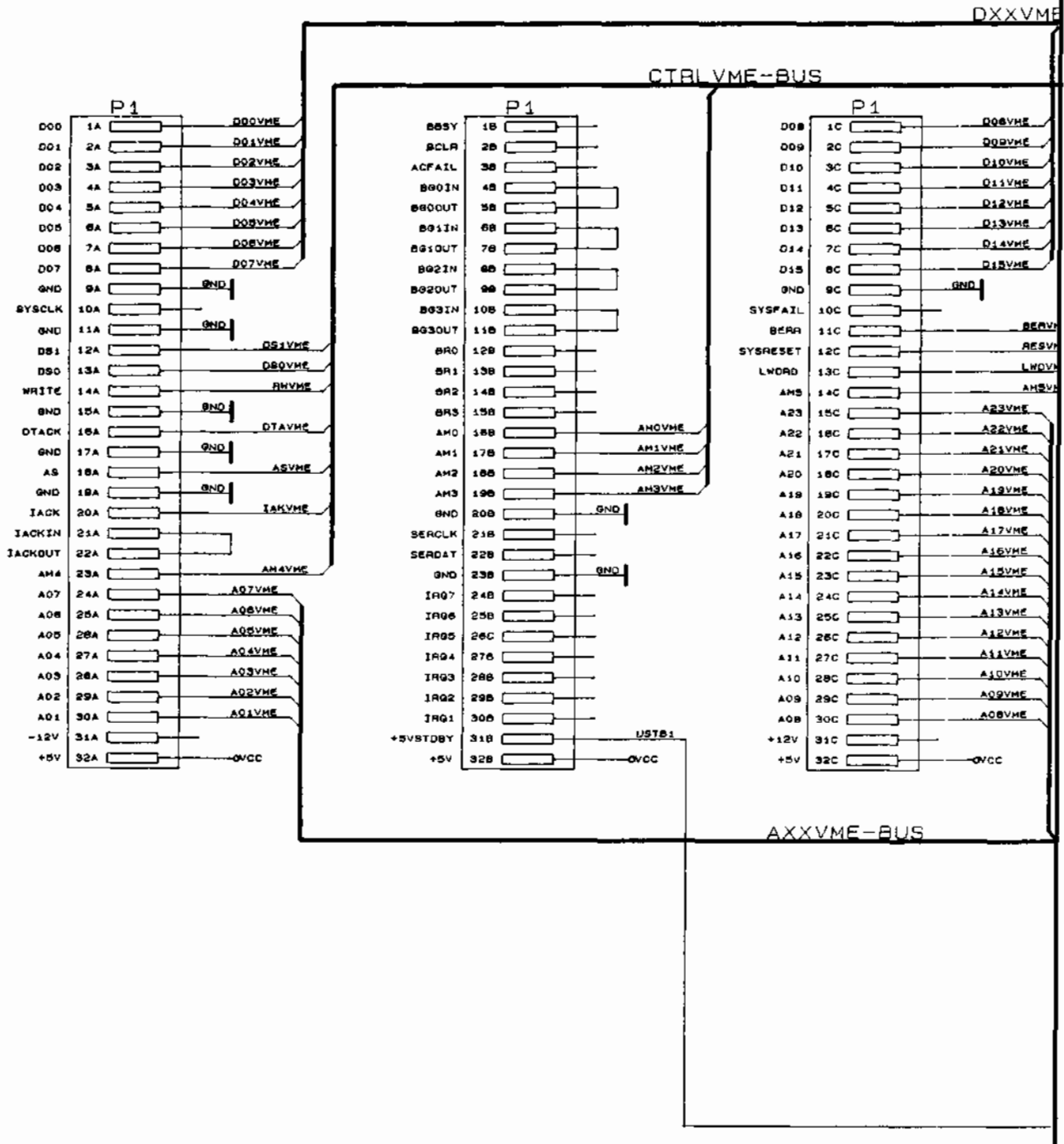
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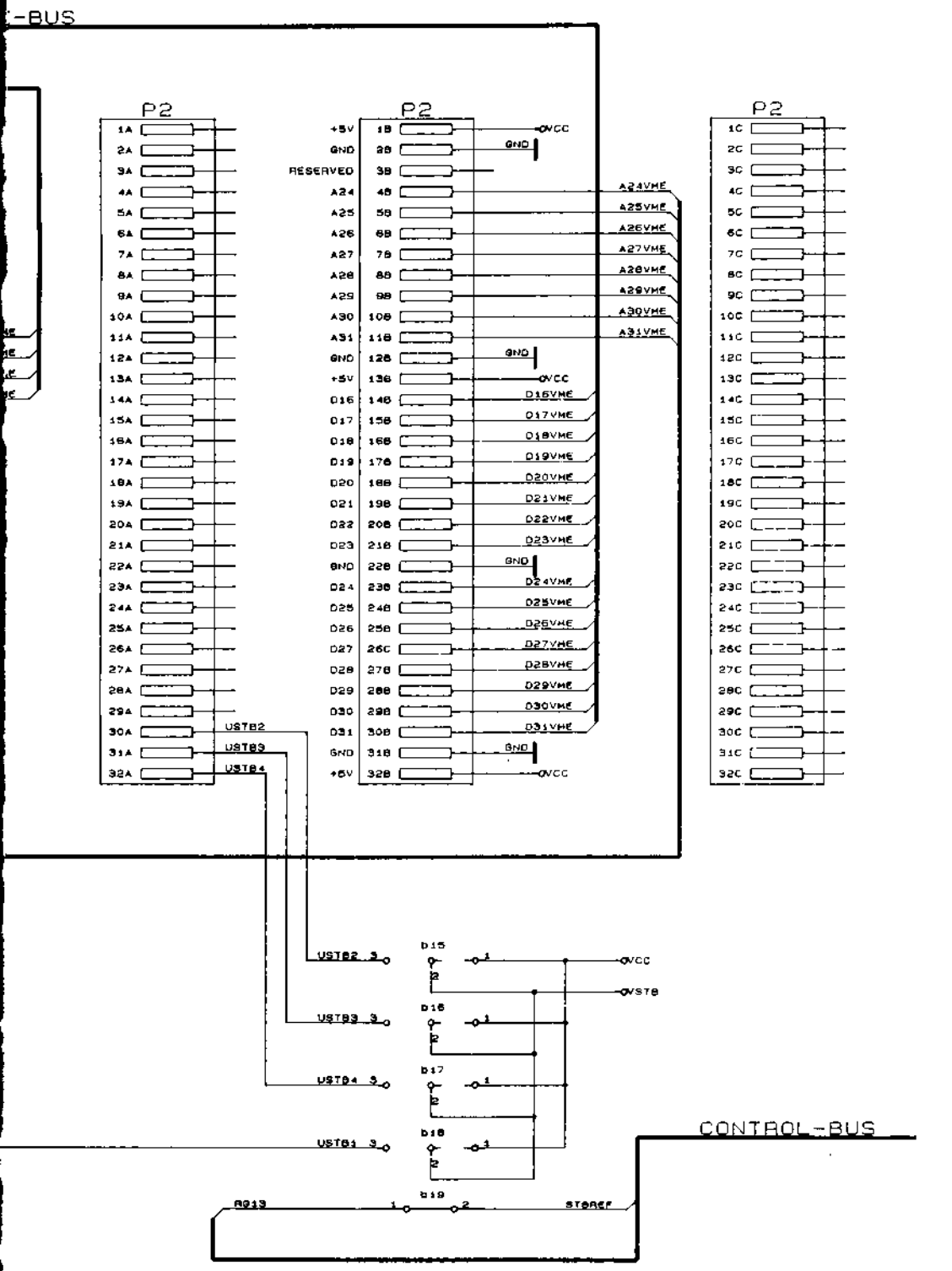

DXX-BUS
AXX-BUS
N6
D23
D22
D21
D20
D19
D18
D17
D16
AV15
@VCC
N7
D03
D02
D01
D00
D07
D06
D05
D04
@VCC
N5
D31
D30
D29
D28
D27
D26
D25
D24
@VCC
N8
D11
D10
D09
D08
D15
D14
D13
D12
@VCC
N4
DOUT1
DIN1
DOUT0
DIN0
DOUT2
DIN2
DOUT3
DIN3
BA109
@VCC
A09A
WRITEA
A10A
A00A
A01A
A02A
A03A
A04A
A05A
A06A
A07A
A08A
A09B
WRITEB
A10B
A00B
A01B
A03B
A02B
A04B
A05B
A07B
A06B
A08B
N3
CKH
CLK1C
CLK2C
CLKSY
CKCNT
CKP
CKR
CYWT1
CYWT2
GND
N9
NEWCY1
NEWCY2
NONEW1
NONEW2
QCLK
CLKINV
CLK
CLKB11
CLKB21
GND
N2
CLRA/
PRBA1/
PRBA2/
SETCY1
SETCY2
RESCY
KILREF
RESDS
TAVE/
GND
N10
CLCK0
CLCK1
CLCK2
CLCK3
CLCK4
CLKB22
CLKB23
CLKB12
CLKB13
GND
CONTROL-BUS
CONTROL-BUS



					Tag	Name	Benennung
				Bearb	31.01.89		DRAM 8 B/C/D/E REV.3
				Gepr.			RESISTORS
							Zeichn.-Nr.
				FORCE COMPUTERS			195fo30-0
Rev	Aender.-Nr.	Tag	Name				Blatt 8
				zu Geraet		zu Anlage	v.1481

Stand : 07.04.89


DXXVME
CTRLVME-BUS
AXXVME-BUS
P1
D00 1A D00VME
D01 2A D01VME
D02 3A D02VME
D03 4A D03VME
D04 5A D04VME
D05 6A D05VME
D06 7A D06VME
D07 8A D07VME
GND 9A GND
SYSCLK 10A
GND 11A GND
DS1 12A DS1VME
DS0 13A DS0VME
WRITE 14A AMVME
GND 15A GND
DTACK 16A DTAVME
GND 17A GND
AS 18A ASVME
GND 19A GND
IACK 20A IAKVME
IACKIN 21A
IACKOUT 22A
AM4 23A AM4VME
A07 24A A07VME
A06 25A A06VME
A05 26A A05VME
A04 27A A04VME
A03 28A A03VME
A02 29A A02VME
A01 30A A01VME
-12V 31A
+5V 32A +5VCC
P1
BBSY 1B
BCLR 2B
ACFAIL 3B
BG0IN 4B
BG0OUT 5B
BG1IN 6B
BG1OUT 7B
BG2IN 8B
BG2OUT 9B
BG3IN 10B
BG3OUT 11B
BR0 12B
BR1 13B
BR2 14B
BR3 15B
AM0 16B AM0VME
AM1 17B AM1VME
AM2 18B AM2VME
AM3 19B AM3VME
GND 20B GND
SERCLK 21B
SERDAT 22B
GND 23B GND
IRQ7 24B
IRQ6 25B
IRQ5 26C
IRQ4 27B
IRQ3 28B
IRQ2 29B
IRQ1 30B
+5VSTDBY 31B USTB1
+5V 32B +5VCC
P1
D08 1C D08VME
D09 2C D09VME
D10 3C D10VME
D11 4C D11VME
D12 5C D12VME
D13 6C D13VME
D14 7C D14VME
D15 8C D15VME
GND 9C GND
SYSFAIL 10C
BERR 11C BERR
SYSRESET 12C RESV
LWORD 13C LWOR
AM5 14C AM5V
A23 15C A23VME
A22 16C A22VME
A21 17C A21VME
A20 18C A20VME
A19 19C A19VME
A18 20C A18VME
A17 21C A17VME
A16 22C A16VME
A15 23C A15VME
A14 24C A14VME
A13 25C A13VME
A12 26C A12VME
A11 27C A11VME
A10 28C A10VME
A09 29C A09VME
A08 30C A08VME
+12V 31C
+5V 32C +5VCC



				Tag	Name	
				Bearb	31.01.89	
				Gepr.		
Rev.	Aender.-Nr.	Tag	Name	zu Gerast		zu Anlage

FORCE COMPUTERS

Stand : 07.04.89

Benennung

DRAM 8 B/C/D/E REV.3

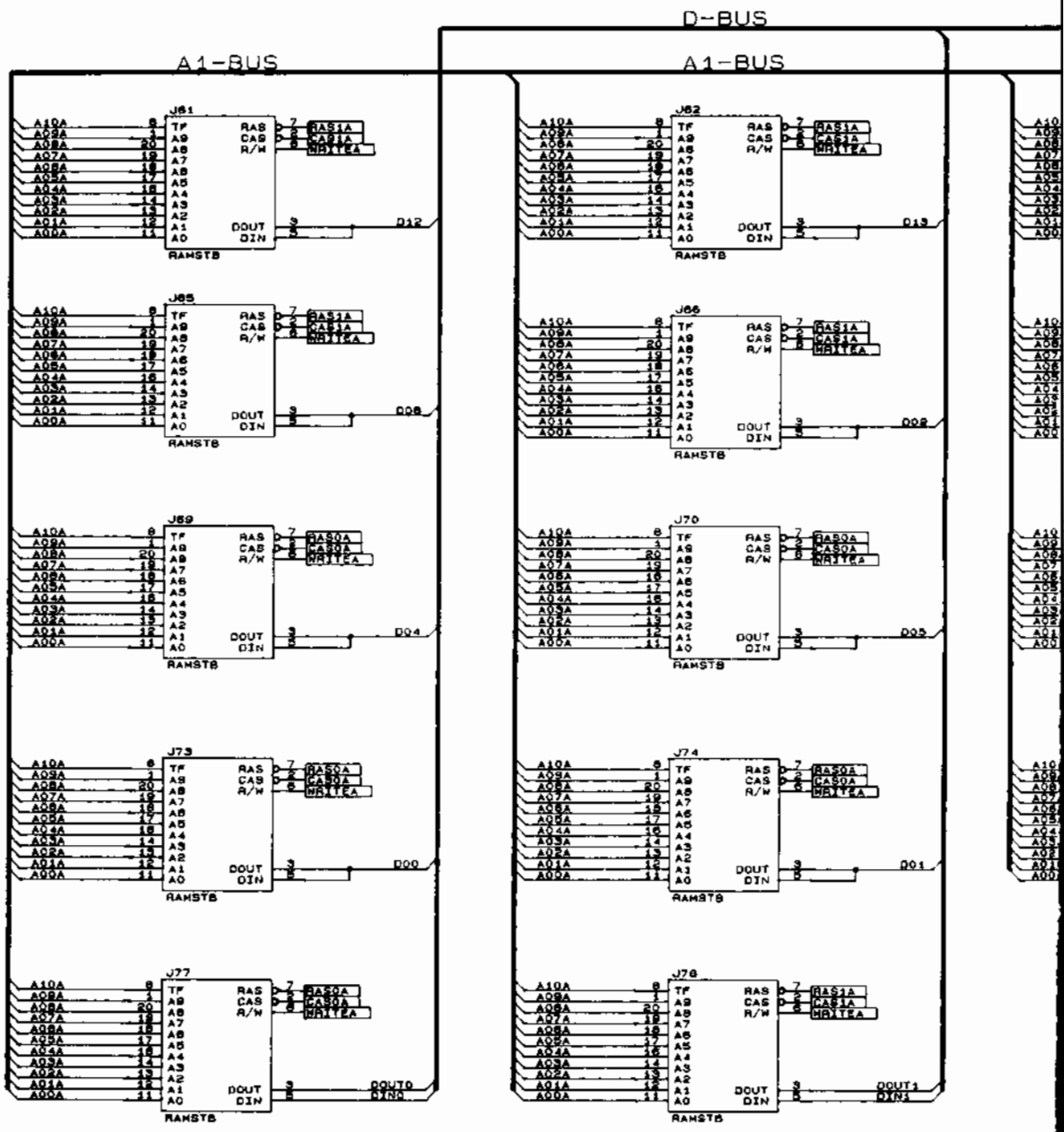
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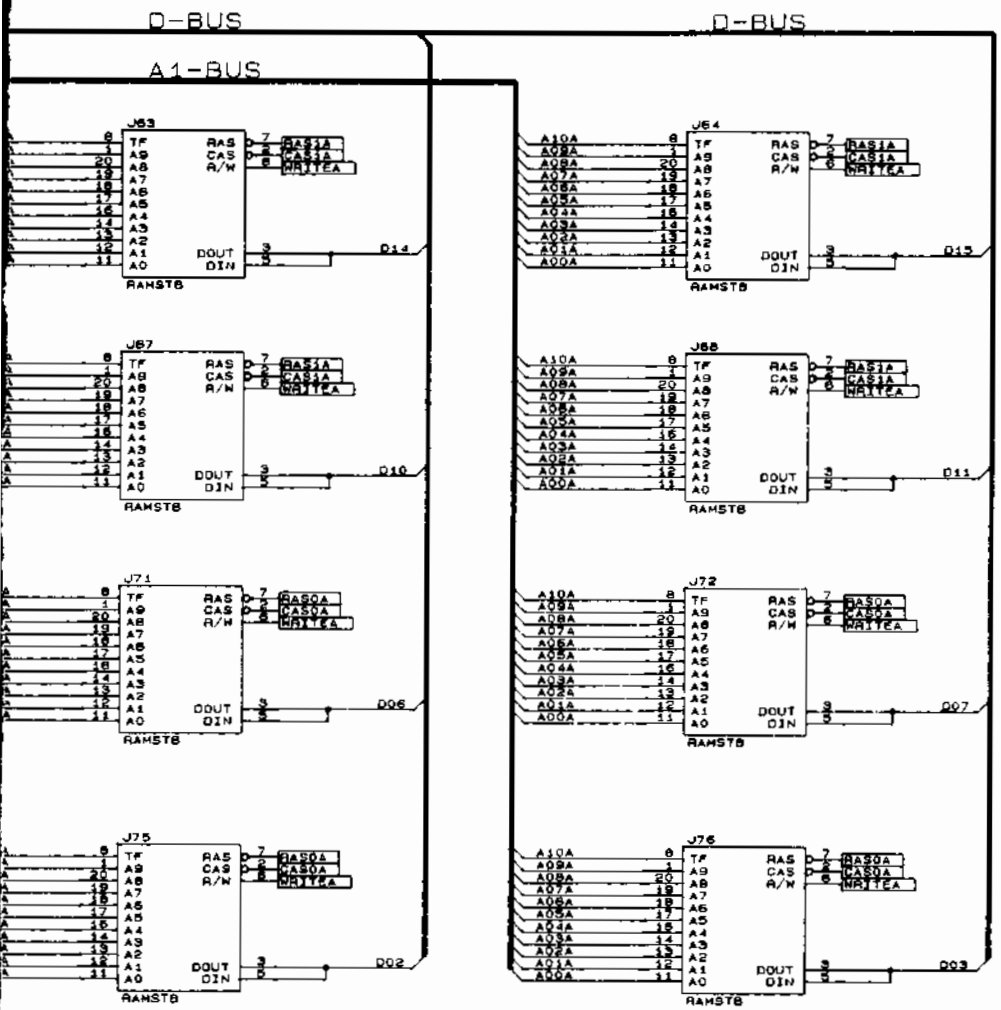
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195fo30-0

Blatt 9

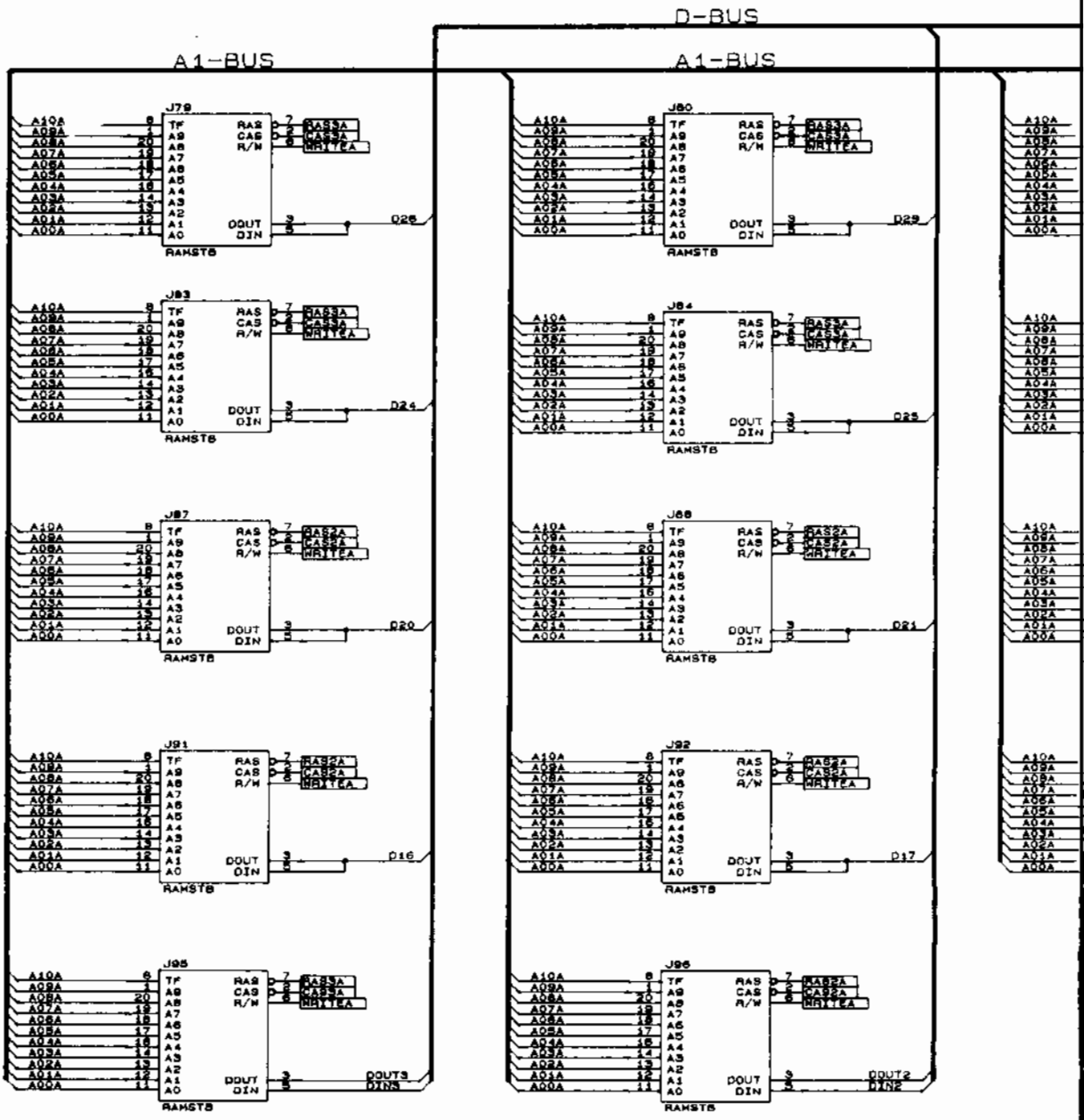
v.1481

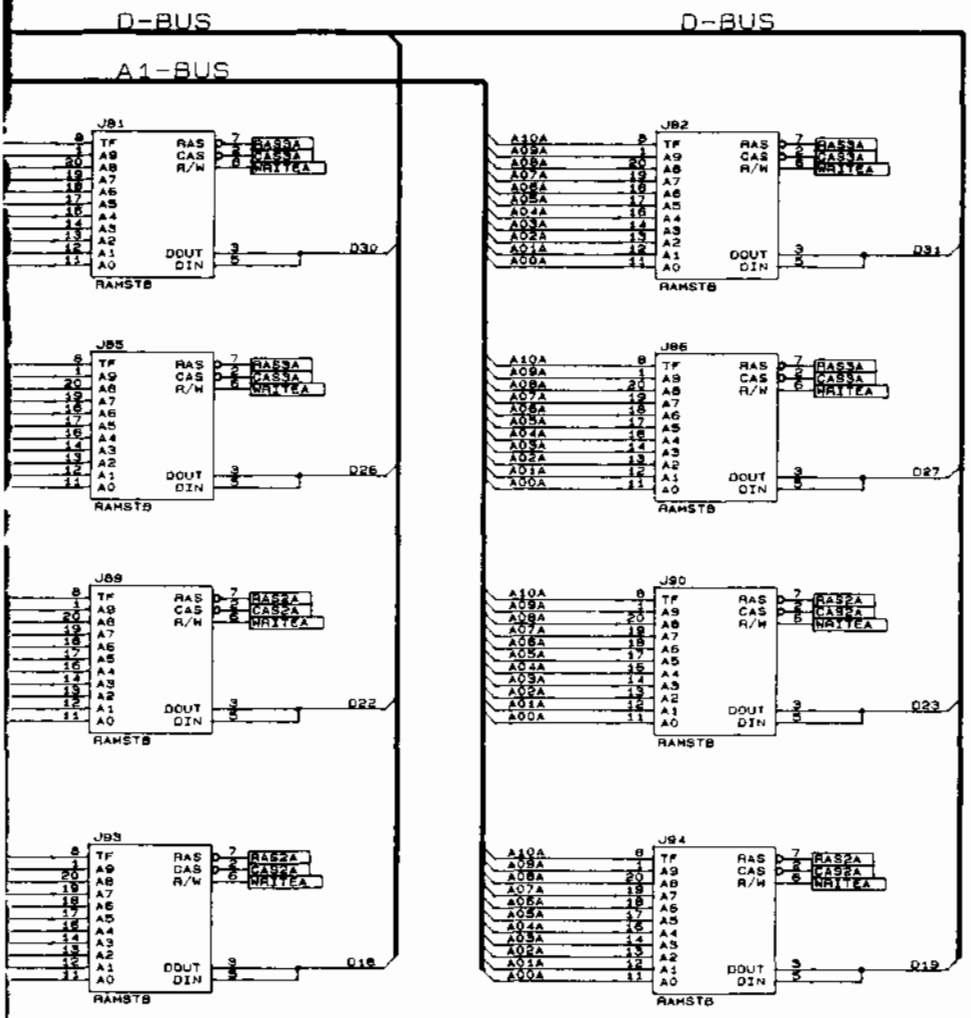

D--BUS
A1-BUS
A1-BUS
J61
J62
J65
J66
J69
J70
J73
J74
J77
J78
TF
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
R/W
DOUT
DIN
RAMSTB
RAS1A
CAS1A
RAS0A
CAS0A
WRITEA
D12
D13
D08
D09
D04
D05
D00
D01
DOUT0
DIN0
DOUT1
DIN1



			Tag	Name	Benennung: DRAM 8 B/C/D/E REV.3
			Bearb.	31.01.89	RAM AREA
			Gepr.		
					FORCE COMPUTERS
					Zeichn.-Nr.: 195fo30-0
Rev.	Aenderg.-Nr.	Tag	Name		zu Satzteil / zu Anlage

Stand: 07.04.89
Blatt 10
V.1481


D-BUS
A1-BUS
A1-BUS
J79
J80
J83
J84
J87
J88
J91
J92
J95
J96
RAMSTB
D28
D29
D24
D25
D20
D21
D16
D17
DOUT3
DIN3
DOUT2
DIN2



Rev.	Aenderg.-Nr.	T&G	Name		

	T&G	Name
Bearb.	31.01.89	
Gepr.		

FORCE COMPUTERS

Stand : 07.04.89

Benennung

DRAM 8 B/C/D/E REV.3

RAM AREA

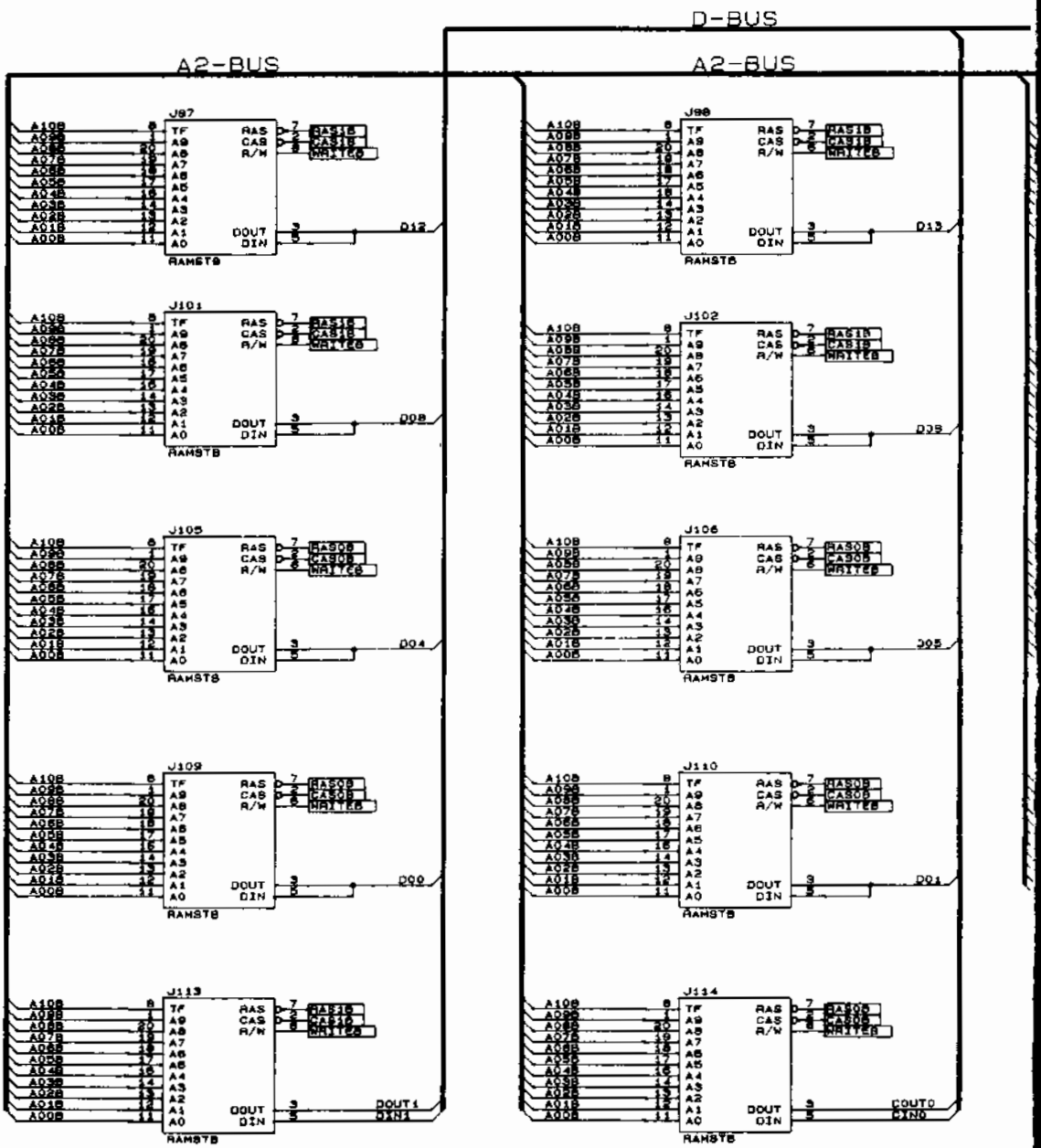
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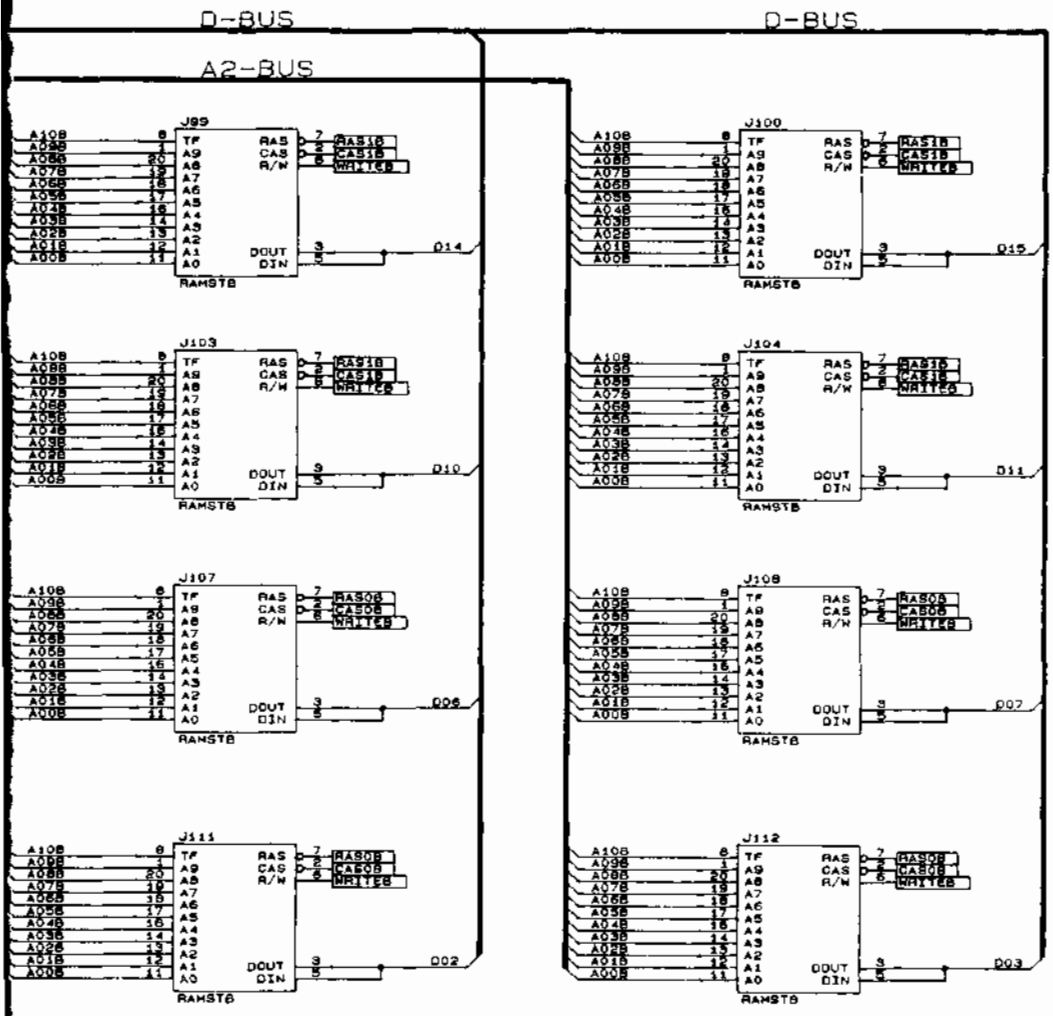
195fo30-0

Blatt 11

V.1481

TU Gerast. TU Ablage


D-BUS
A2-BUS
A2-BUS
J97
J98
J101
J102
J105
J106
J109
J110
J113
J114
RAS
CAS
R/W
DOUT
DIN
RAMSTB
D12
D13
D08
D09
D04
D05
D00
D01
DOUT1
DIN1
DOUT0
DIN0

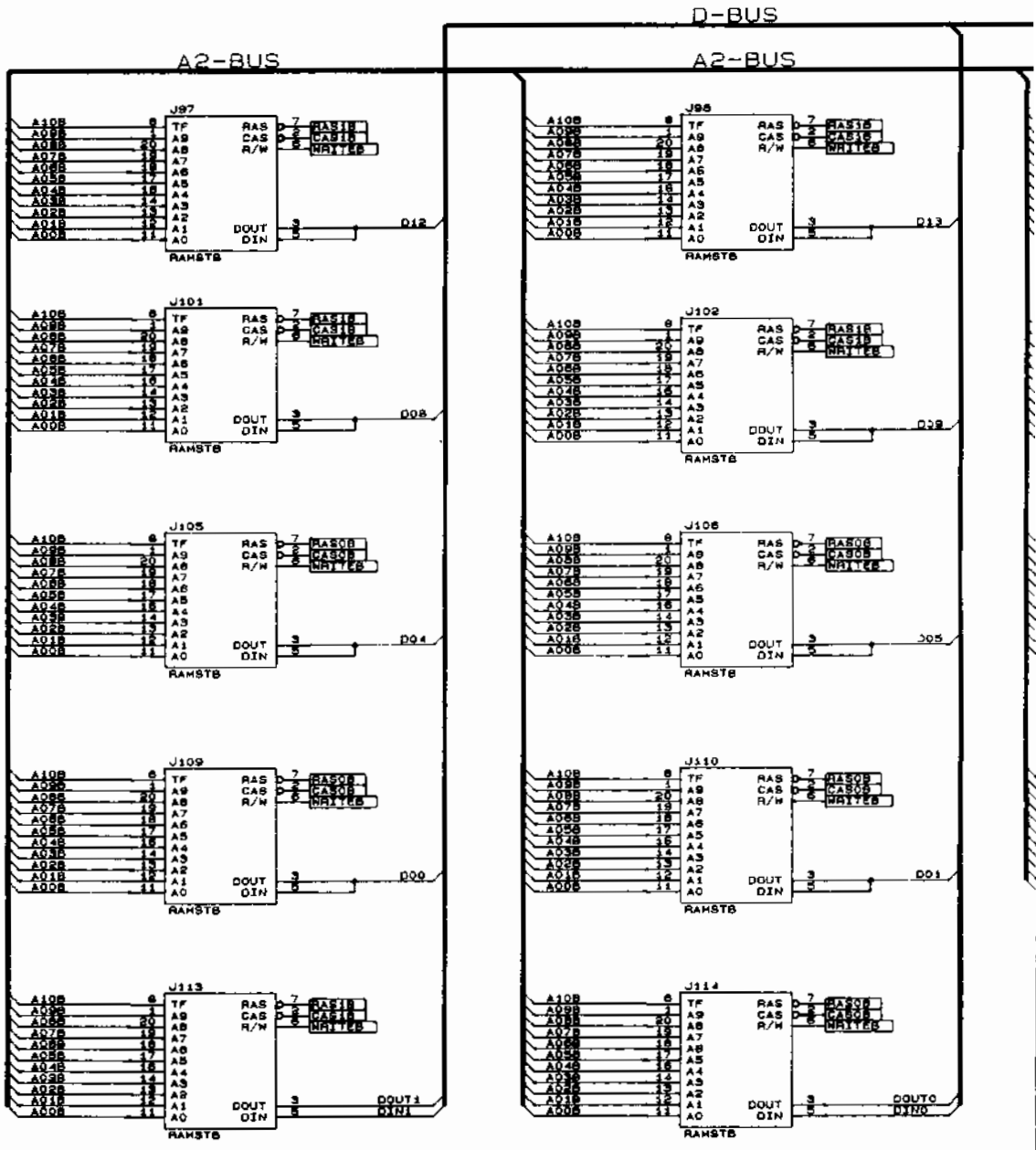


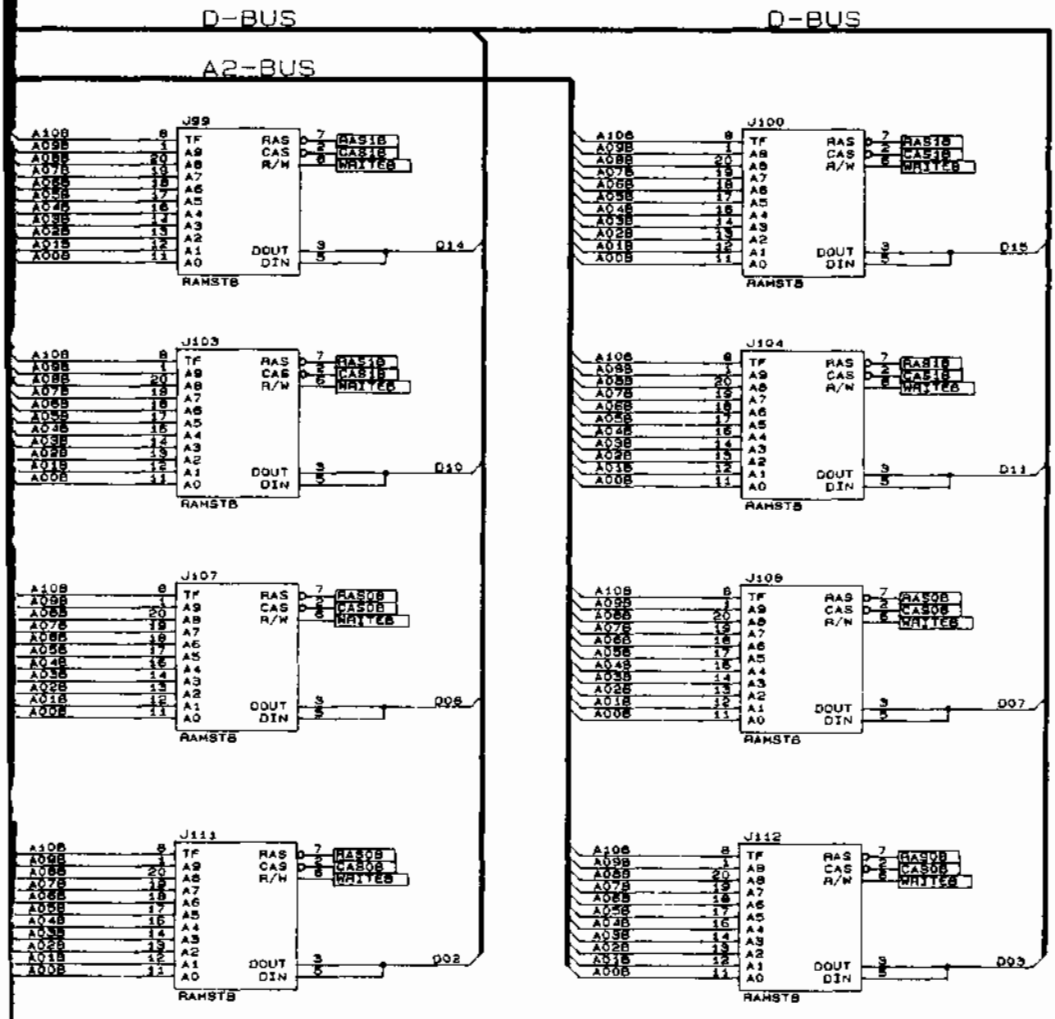
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				Gepr.		RAM AREA
				FORCE COMPUTERS		Zeichn.-Nr. 195fo30-0
Änd.	Änderung-Nr.	Tag	Name			zu Serie: zu Anlage:

Stand : 07.04.89

Blatt 12

v.1481


D-BUS
A2-BUS
A2-BUS
J97
J98
J101
J102
J105
J106
J109
J110
J113
J114
RAMSTB
D12
D13
D08
D09
D04
D05
D00
D01
DOUT1
DIN1
DOUT0
DIN0



				Tag	Name
				Bearb	31.01.89
				Gepr.	
				FORCE COMPUTERS	
Rev.	Aenderung	Tag	Name		

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Benennung

REV.3

DRAM 8 B/C/D/E

RAM AREA

Zeichn.-Nr.

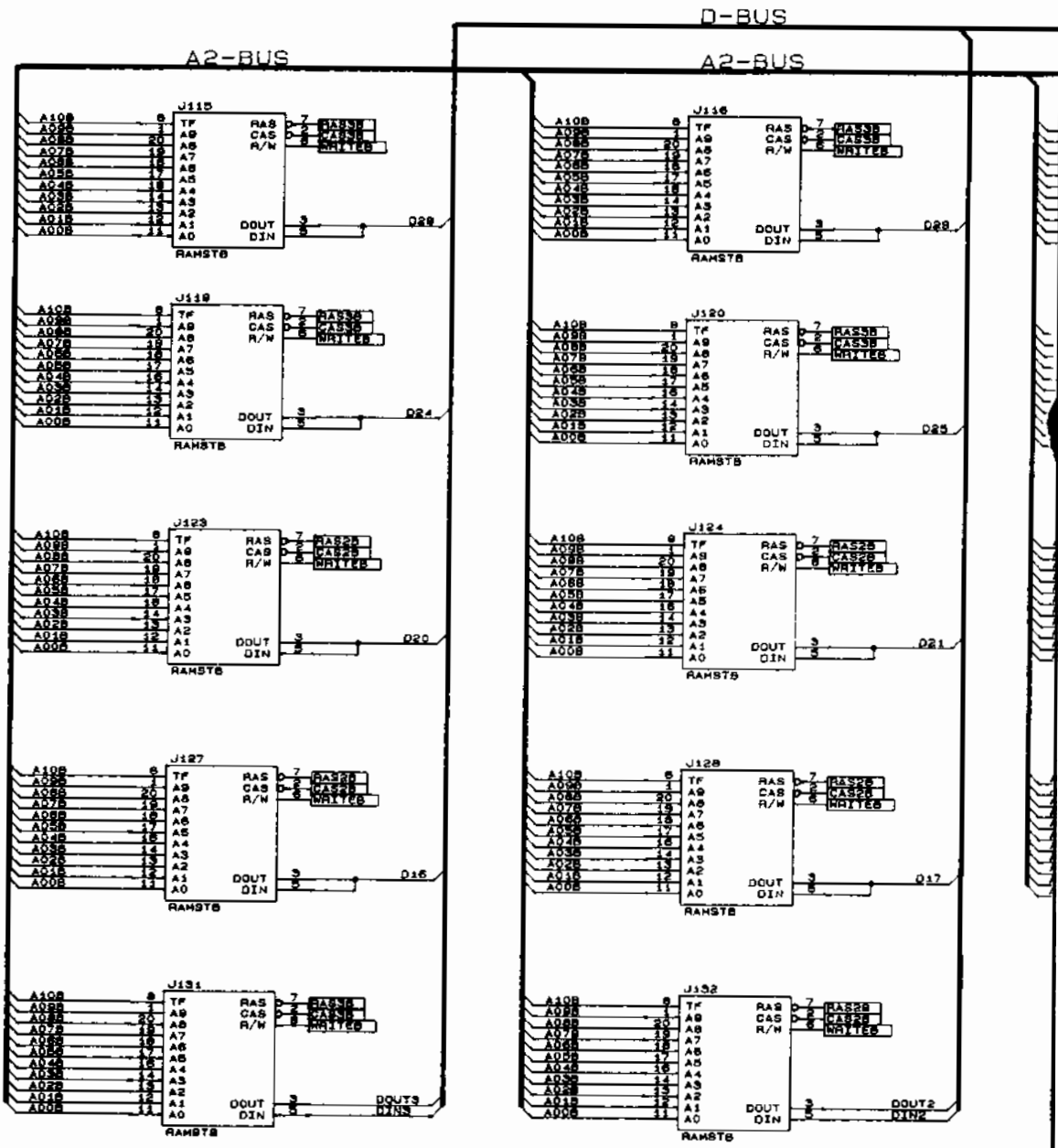
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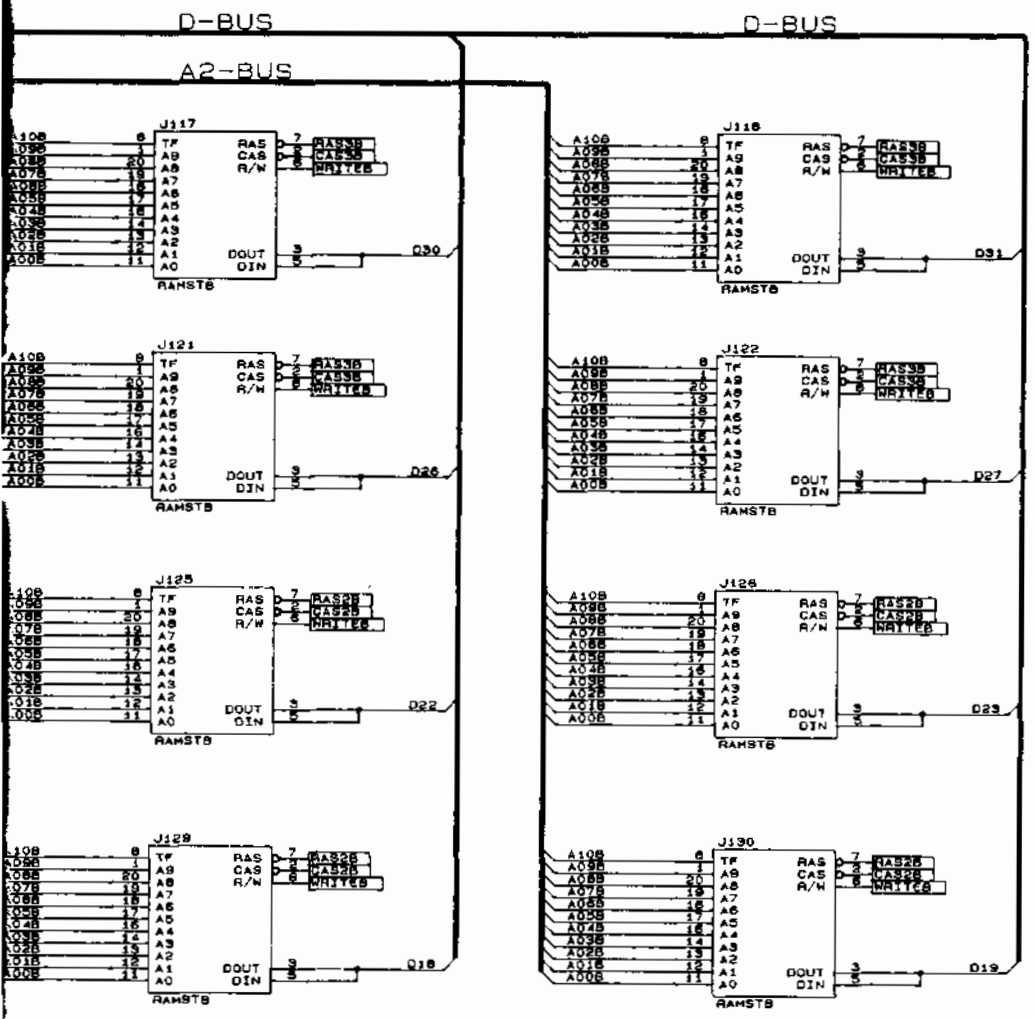
Blatt 12

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Zu Gerast

Zu Anlage


D-BUS
A2-BUS
A2-BUS
J115
J116
J119
J120
J123
J124
J127
J128
J131
J132
RAMSTB
D29
D28
D24
D25
D20
D21
D16
D17
DOUT3
DIN3
DOUT2
DIN2



Stand : 07.04.89

				Bearb	31.01.89
				Gepr.	
Dev	Aender.-Nr.	Tag	Name		

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REV.3

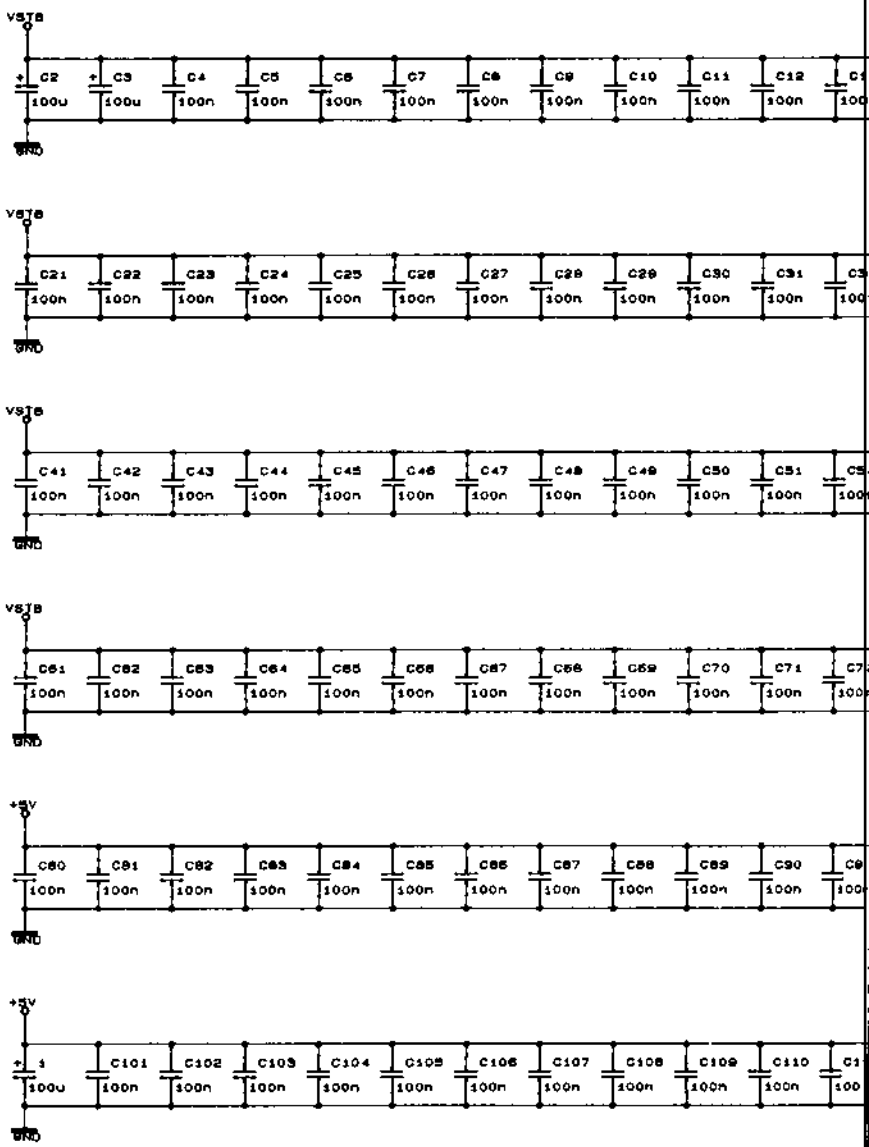
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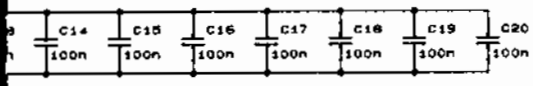
RAM AREA

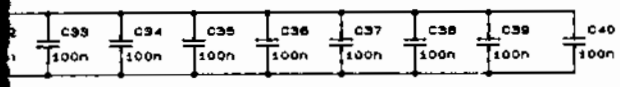
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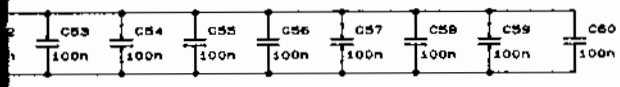
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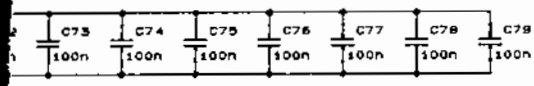
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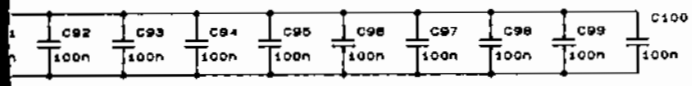

VSTB
C2 100u
C3 100u
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 100n
C11 100n
C12 100n
GND
VSTB
C21 100n
C22 100n
C23 100n
C24 100n
C25 100n
C26 100n
C27 100n
C28 100n
C29 100n
C30 100n
C31 100n
GND
VSTB
C41 100n
C42 100n
C43 100n
C44 100n
C45 100n
C46 100n
C47 100n
C48 100n
C49 100n
C50 100n
C51 100n
GND
VSTB
C61 100n
C62 100n
C63 100n
C64 100n
C65 100n
C66 100n
C67 100n
C68 100n
C69 100n
C70 100n
C71 100n
GND
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C82 100n
C83 100n
C84 100n
C85 100n
C86 100n
C87 100n
C88 100n
C89 100n
C90 100n
GND
+5V
1 100u
C101 100n
C102 100n
C103 100n
C104 100n
C105 100n
C106 100n
C107 100n
C108 100n
C109 100n
C110 100n
GND

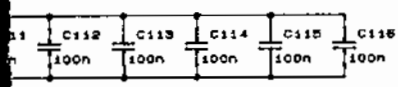












Stand : 07.04.89

					Tag	Name
				Bearb	31.01.89	
				Gepr.		
				FORCE COMPUTERS		
Rev	Aender.-Nr.	Tag	Name	zu Gerae		zu Anlage

Benennung

REV.3

DRAM 8 B/C/D/E

CAPACITORS

Zeichn.-Nr.

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Blatt 14

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