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Agilent 4396B Network/Spectrum/Impedance Analyzer

Service Manual

SERIAL NUMBERS

This manual applies directly to instruments with serial number prefix JP1KD, or firmware revision 1.00. For additional important information about serial numbers, read “Serial Number” in Appendix A.



Agilent Technologies

Agilent Part No. 04396-90121
Printed in Japan March 2001

Third Edition

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Agilent Technologies Japan, Ltd.
Component Test PGU-Kobe
1-3-2, Murotani, Nishi-ku, Kobe-shi,
Hyogo, 651-2241 Japan

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Manual Printing History

The manual's printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates that are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

May 1997 ..... First Edition (part number: 04396-90121)

June 2000 ..... Second Edition (part number: 04396-90121)

March 2001 ..... Third Edition (part number: 04396-90121)

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Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific *WARNINGS* elsewhere in this manual may impair the protection provided by the equipment. In addition it violates safety standards of design, manufacture, and intended use of the instrument.
The Agilent Technologies assumes no liability for the customer's failure to comply with these requirements.

Note 

4396B comply with INSTALLATION CATEGORY II and POLLUTION DEGREE 2 in IEC1010-1. 4396B are INDOOR USE product.

Note 

LEDs in 4396B are Class 1 in accordance with IEC825-1.
CLASS 1 LED PRODUCT

Ground The Instrument

To avoid electric shock hazard, the instrument chassis and cabinet must be connected to a safety earth ground by the supplied power cable with earth blade.

DO NOT Operate In An Explosive Atmosphere

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT Service Or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT Substitute Parts Or Modify Instrument

Because of the danger of introducing additional hazards, do not install substitute parts or perform unauthorized modifications to the instrument. Return the instrument to a Agilent Technologies Sales and Service Office for service and repair to ensure that safety features are maintained.

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Dangerous Procedure Warnings

Warnings , such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning  **Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting this instrument.**

Safety Symbols

General definitions of safety symbols used on equipment or in manuals are listed below.

 Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual.

 Alternating current.

 Direct current.

 On (Supply).

 Off (Supply).

 In position of push-button switch.

 Out position of push-button switch.

 Frame (or chassis) terminal. A connection to the frame (chassis) of the equipment which normally include all exposed metal structures.

Warning  This **Warning** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution  This **Caution** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note  This **Note** sigh denotes important information. It calls attention to a procedure, practice, condition or the like, which is essential to highlight.

 Affixed to product containing static sensitive devices use anti-static handling procedures to prevent electrostatic discharge damage to component.

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Certification

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory. Agilent Technologies further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institution's calibration facility, or to the calibration facilities of other International Standards Organization members.

Warranty

This Agilent Technologies instrument product is warranted against defects in material and workmanship for a period of one year from the date of shipment, except that in the case of certain components listed in *General Information* of this manual, the warranty shall be for the specified period. During the warranty period, Agilent Technologies will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Agilent Technologies. Buyer shall prepay shipping charges to Agilent Technologies and Agilent Technologies shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to Agilent Technologies from another country.

Agilent Technologies warrants that its software and firmware designated by Agilent Technologies for use with an instrument will execute its programming instruction when property installed on that instrument. Agilent Technologies does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

Limitation Of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. Agilent Technologies specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

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Exclusive Remedies

The remedies provided herein are buyer's sole and exclusive remedies. Agilent Technologies shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Agilent Technologies products.

For any assistance, contact your nearest Agilent Technologies Sales and Service Office. Addresses are provided at the back of this manual.

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Typeface Conventions

Bold	Boldface type is used when a term is defined. For example: **icons** are symbols.
Italics	Italic type is used for emphasis and for titles of manuals and other publications. Italic type is also used for keyboard entries when a name or a variable must be typed in place of the words in italics. For example: `copy` *filename* means to type the word `copy`, to type a space, and then to type the name of a file such as `file1`.
`Computer`	Computer font is used for on-screen prompts and messages.
HARDKEYS	Labeled keys on the instrument front panel are enclosed in ▢.
SOFTKEYS	Softkeys located to the right of the CRT are enclosed in .

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Documentation Map

The following manuals are available for the analyzer.

User's Guide

The User's Guide walks you through system setup and initial power-on, shows how to make basic measurements, explains commonly used features, and typical application measurement examples. After you receive your analyzer, begin with this manual.

Task Reference

Task Reference helps you to learn how to use the analyzer. This manual provides simple step-by-step instructions without concepts.

Function Reference

The Function Reference describes all function accessed from the front panel keys and softkeys. It also provides information on options and accessories available, specifications, system performance, and some topics about the analyzer's features.

Programming Guide

The Programming Guide shows how to write and use BASIC program to control the analyzer and describes how HP Instrument BASIC works with the analyzer..

GPIB Command Reference

The GPIB Command Reference provides a summary of all available GPIB commands. It also provides information on the status reporting structure and the trigger system (these features conform to the SCPI standard).

HP Instrument BASIC Manual Set,

The HP Instrument BASIC User's Handbook introduces you to the HP Instrument BASIC programming language, provide some helpful hints on getting the most use from it, and provide a general programming reference. It is divided into three books, *HP Instrument BASIC Programming Techniques*, *HP Instrument BASIC Interface Techniques*, and *HP Instrument BASIC Language Reference*.

Performance Test Manual

The Performance Test Manual explains how to verify conformance to published specifications.

Service Manual (Option 0BW only),

The Service Manual explains how to adjust, troubleshoot, and repair the instrument. This manual is option 0BW only.

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Contents

1. General Information

INTRODUCTION 1-1
ORGANIZATION OF SERVICE MANUAL 1-1
TABLE OF SERVICE TEST EQUIPMENT 1-3

2. Adjustments and Correction Constants

Introduction 2-1
Safety Considerations 2-1
Required Equipment 2-2
Warm-up for Adjustments and Correction Constants 2-2
Instrument Cover Removal 2-2
Order Of Adjustments 2-2
Updating Correction Constants using the Adjustments Program 2-3
Adjustments Program 2-3
Keyboard and Mouse Operation 2-3
Controller Requirement 2-4
Updating Correction Constants 2-5
40 MHz Reference Oscillator Frequency Adjustment 2-6
Required Equipment 2-6
Procedure 2-6
520 MHz Level Adjustment 2-8
Required Equipment 2-8
Procedure 2-8
CAL OUT Level Adjustment 2-10
Required Equipment 2-10
Procedure 2-10
Comb Generator Adjustment 2-12
Required Equipment 2-12
Procedure 2-12
Step Pretune Correction Constants 2-15
Required Equipment 2-15
Procedure 2-15
Second Local PLL Lock Adjustment 2-16
Required Equipment 2-16
Procedure 2-16
DC Offset and Hold Step Adjustment 2-18
Required Equipment 2-18
Procedure 2-18
0°/90° Tracking Adjustment 2-23
Required Equipment 2-23
Procedure 2-23
Band Pass Filters Adjustments 2-26
Required Equipment 2-26
Procedure 2-26
3 MHz Band Pass Filter Adjustment 2-26
1 MHz BPF Band Width Adjustment 2-27

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Final Gain Adjustment . . . 2-29
Required Equipment . . . 2-29
Procedure . . . 2-29
Source Mixer Local Leakage Adjustment . . . 2-31
Required Equipment . . . 2-31
Procedure . . . 2-31
RF OUT Level Correction Constants . . . 2-33
Required Equipment . . . 2-33
Procedure . . . 2-33
Spectrum Analyzer Absolute Magnitude Correction Constants . . . 2-34
Required Equipment . . . 2-34
Procedure . . . 2-34
Network Analyzer Absolute Magnitude Correction Constants . . . 2-35
Required Equipment . . . 2-35
Procedure . . . 2-35
Crystal Filter Correction Constants . . . 2-36
Required Equipment . . . 2-36
Procedure . . . 2-36
IF Gain Errors Correction Constants . . . 2-37
Required Equipment . . . 2-37
Procedure . . . 2-37
Network Analyzer Magnitude Ratio/Phase Correction Constants . . . 2-39
Required Equipment . . . 2-39
Procedure . . . 2-39
10 MHz Reference Oscillator Frequency Adjustment (Option 1D5 Only) . . . 2-41
Required Equipment . . . 2-41
Procedure . . . 2-41

3. Troubleshooting
INTRODUCTION . . . 3-1
TROUBLESHOOTING SUMMARY . . . 3-1
START HERE . . . 3-3
INSPECT THE POWER ON SEQUENCE . . . 3-4
Check the Fan . . . 3-4
Check the Front Panel LEDs and Displays . . . 3-4
Check Error Message . . . 3-4
OPERATOR'S CHECK . . . 3-5
Test Equipment . . . 3-5
Procedure . . . 3-5
INSPECT THE REAR PANEL FEATURE . . . 3-9
Check the GPIB Interface . . . 3-9
Check the Parallel Interface . . . 3-9
Check the mini DIN Keyboard Connector . . . 3-9

4. Isolate Faulty Group Troubleshooting
INTRODUCTION . . . 4-1
OPERATOR'S CHECK FAILURE TROUBLESHOOTING . . . 4-2
Check RF OUT Frequency . . . 4-2
Check RF OUT Power Level . . . 4-2
PERFORMANCE TESTS FAILURE TROUBLESHOOTING . . . 4-3
Perform Adjustments and Correction Constants . . . 4-3
Troubleshoot Suspicious Functional Group . . . 4-4

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5. Power Supply Troubleshooting

INTRODUCTION 5-1
START HERE 5-3
1. Check Error Messages 5-3
2. Check the Fan is Rotating 5-3
3. Check the A50 SHUTDOWN LED 5-3
A50 Shutdown LED 5-4
4. Check the A1 +5 VD LED 5-5
Measure the A1 +5 VD Voltage 5-5
5. Check the A2 Eight LEDs 5-5
6. Run the Internal Test 4: A2 POST REGULATOR 5-6
Internal Test 4: A2 POST REGULATOR 5-7
FIND OUT WHY THE FAN IS NOT ROTATING 5-8
1. Check the Line Voltage, Selector Switch Setting, and Fuse 5-8
2. Check the A50 SHUTDOWN LED 5-8
FIND OUT WHY THE A50 SHUTDOWN LED IS OFF 5-9
1. Disconnect the Cable from the A50J1 5-9
2. Disconnect the Cable from the A51J2 5-9
3. Disconnect the Cable from the A1J10 5-9
4. Remove Assemblies 5-9
FIND OUT WHY THE A1 +5 VD LED IS NOT ON STEADILY 5-10
1. Check the A40 Pre-Regulator 5-10
2. Check the A50 DC-DC Converter 5-10
3. Disconnect Cables on the A1 CPU 5-11
4. Remove Assemblies 5-12
TROUBLESHOOT THE FAN AND THE A50 DC-DC CONVERTER 5-13
1. Troubleshoot the Fan 5-13
2. Troubleshoot the A50 DC-DC Converter 5-14
TROUBLESHOOT THE A2 POST-REGULATOR 5-16
1. Check the A40 Pre-Regulator 5-16
2. Check the A50 DC-DC Converter 5-16
3. Remove Assemblies 5-16
4. Measure the A2 Post Regulator Output Voltages 5-16

6. Digital Control Troubleshooting

INTRODUCTION 6-1
A1 CPU Replacement 6-3
FIRMWARE INSTALLATION 6-4
Ordering the Firmware Diskette 6-4
Installing the Firmware 6-4
START HERE 6-6
1. Check the Power On Sequence 6-6
Check the Ch 1 and Ch 2 Operations 6-6
Check the A1 Eight LEDs 6-6
2. Check Error Messages 6-7
Check the Power On Selftest 6-7
3. Check the A1 DRAM and Flash Memory 6-10
4. Check the A1 Volatile Memory 6-11
5. Check the A30 Front Keyboard 6-11
6. Check the A53 FDD 6-11
7. Check the A32 I-BASIC Interface and the mini DIN Keyboard 6-12
TROUBLESHOOT THE A51 GSP and A52 LCD 6-13
1. Run the Internal Test 3: A51 GSP 6-13
2. Check the A52 LCD(Liquid Crystal Display) 6-13

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7. Source Group Troubleshooting

INTRODUCTION 7-1
SOURCE GROUP TROUBLESHOOTING SUMMARY 7-3
Start Here 7-3
Check A5 Synthesizer Outputs 7-3
Check A4A1 1st LO Outputs 7-3
Check an A3A1 ALC Output 7-3
Check A3A2 2nd LO Outputs 7-3
Check an A3A3 Source Output 7-4
Check A7 Output Attenuator Control Signals 7-4
Check A60 High Stability Frequency Reference (Option 1D5) 7-4
START HERE 7-5
CHECK A5 SYNTHESIZER OUTPUTS 7-7
1. Check the CAL OUT Signal 7-7
Check the CAL OUT's Spurious 7-8
2. Check the INT REF Signal 7-9
3. Check the FRAC N OSC Signal 7-11
4. Check the STEP OSC Signal 7-13
5. Check the 520 MHz Signal 7-16
6. Check the EXT REF Operation 7-18
CHECK A4A1 1ST LO OUTPUTS 7-19
1. Check the 1st LO OSC Signal at A4A1J3 7-19
2. Check the 1st LO OSC Signal at A4A1J4 7-21
CHECK AN A3A1 ALC OUTPUT 7-23
1. Check the 21.42 MHz Signal 7-23
CHECK A3A2 2ND LO OUTPUTS 7-26
1. Check the 2nd Local Oscillator Signal 7-26
2. Check the 2.05858 GHz Signal 7-27
CHECK AN A3A3 SOURCE OUTPUT 7-30
1. Check the A3A3 RF Signal 7-30
CHECK A7 OUTPUT ATTENUATOR CONTROL SIGNALS 7-32
1. Check A7 Control Signals 7-32
CHECK THE A60 HIGH STABILITY FREQUENCY REFERENCE 7-34

8. Receiver Group Troubleshooting

INTRODUCTION 8-1
RECEIVER GROUP TROUBLESHOOTING SUMMARY 8-3
Start Here 8-3
Check A8 Output Attenuator Control Signals 8-3
Check A9 Input Multiplexer Control Signals 8-3
Check Signal Inputs to A4A2 Receiver RF 8-3
START HERE 8-4
CHECK A8 INPUT ATTENUATOR CONTROL SIGNALS 8-5
CHECK A9 INPUT MULTIPLEXER CONTROL SIGNALS 8-7
CHECK SIGNAL INPUTS TO THE A4A2 RECEIVER RF 8-9
Check the Input Signal to A4A2J3 8-9
Check the Input Signal to A4A2J12 8-9

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9. Accessories Troubleshooting

INTRODUCTION 9-1
VERIFY OPERATIONS 9-2
Using 75 Ω Connectors with 50 Ω Connectors 9-2
Large Spurious Signals in the Spectrum Measurement 9-2
Odd Appearing Opens and Shorts in the Network Measurement 9-2
INSPECT THE CONNECTORS 9-3
INSPECT THE ACCESSORIES 9-4
Verify the Probe Power 9-4
Inspect the Test Set 9-5
Inspect the Calibration Kit 9-5
Verify Shorts and Opens 9-5

10. Service Key Menus

INTRODUCTION 10-1
SERVICE MENU 10-3
TESTS 10-3
SERVICE MODES (:DIAG:SERV:MODE {ON|1}) 10-3
FIRMWARE REVISION (:DIAG:FREV?) 10-3
TESTS MENU 10-4
EXECUTE TEST (:DIAG:TEST:EXET) 10-4
INTERNAL TESTS (:DIAG:TEST 0) 10-4
EXTERNAL TESTS (:DIAG:TEST 17) 10-5
ADJUSTMENT TESTS (:DIAG:TEST 41) 10-5
DISPLAY TESTS (:DIAG:TEST 48) 10-5
ALL EXT TESTS (:DIAG:TEST 53) 10-5
MISC TESTS (:DIAG:TEST 58) 10-5
Test Status 10-5
Diagnostic Tests 10-6
Test Descriptions 10-7
INTERNAL TESTS 10-7
0: ALL INT 10-7
1: A1 CPU 10-7
2: A1 VOLATILE MEMORY 10-7
3: A51 GSP 10-8
4: A2 POST REGULATOR 10-8
5: A6 A/D CONVERTER 10-8
6: A5 REFERENCE OSC 10-8
7: A5 FRACTIONAL N OSC 10-8
8: A5 STEP OSC 10-9
9: A4A1 1ST LO OSC 10-9
10: A3A2 2ND LO OSC 10-9
11: A3A1 DIVIDER 10-9
12: A6 3RD LO OSC 10-9
13: A3A1 SOURCE OSC 10-9
14: A6 3RD IF DC OFFSET 10-9
15: A6 SEQUENCER 10-9
16: A3A1 ALC 10-9
EXTERNAL TESTS 10-9
17: FRONT PANEL DIAG. 10-12
18: DSK DR FAULT ISOL'N 10-12
19: POWER SWEEP LINEARITY 10-12

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20: OUTPUT ATTENUATOR . . . 10-12
21: INPUT ATTENUATOR . . . 10-13
22: RF TO S LVL & FLTNESS . . . 10-13
23: S TO A CROSSTALK . . . 10-13
24: S INPUT COMPRESSION . . . 10-13
25: S INPUT RESIDUALS . . . 10-13
26: S INPUT NOISE LEVEL . . . 10-13
27: FRACTION SPURIOUS . . . 10-13
28: RF TO R LVL & FLTNESS . . . 10-14
29: NA CROSSTALK & NOISE . . . 10-14
30: R INPUT COMPRESSION . . . 10-14
31: RANGING . . . 10-14
32: A/R RATIO ACCURACY . . . 10-14
33: A INPUT COMPRESSION . . . 10-14
34: B/R RATIO ACCURACY . . . 10-15
35: B INPUT COMPRESSION . . . 10-15
36: RESOLUTION BANDWIDTH . . . 10-15
37: IF GAIN . . . 10-15
38: PHASE NOISE . . . 10-15
39: SPURIOUS . . . 10-15
40: X'TAL FILTER RESPONSE . . . 10-15
ADJUSTMENT TESTS . . . 10-16
41: DC OFFST/HLD STEP ADJ . . . 10-16
42: 0/90 DEG TRACKING ADJ . . . 10-16
43: FINAL GAIN ADJ . . . 10-16
44: 2nd LO PLL LOCK ADJ . . . 10-16
45: SOURCE MIXER LEAK ADJ . . . 10-16
46: 3 MHZ BPF ADJ . . . 10-16
47: 1 MHZ BPF ADJ . . . 10-16
DISPLAY TESTS . . . 10-16
48: TEST PATTERN 1 . . . 10-16
49: TEST PATTERN 2 . . . 10-17
50: TEST PATTERN 3 . . . 10-17
51: TEST PATTERN 4 . . . 10-17
52: TEST PATTERN 5 . . . 10-17
ALL EXT TESTS . . . 10-17
53: ALL EXT 1 . . . 10-17
54: ALL EXT 2 . . . 10-17
55: ALL EXT 3 . . . 10-17
56: ALL EXT 4 . . . 10-17
57: ALL EXT 5 . . . 10-17
MISC TESTS . . . 10-18
58: IMPEDANCE TEST KIT . . . 10-18
SERVICE MODES MENU . . . 10-19
BUS MEAS [OFF] . . . 10-19
CORRECTION CONSTANTS . . . 10-19
IF . . . 10-19
SYNTH . . . 10-19
SOURCE . . . 10-20
Service Modes . . . 10-20
BUS MEASUREMENT MENU . . . 10-21
BUS MEAS on OFF (:DIAG:SERV:BUS:STAT {ON|OFF}) . . . 10-21
DC BUS [OFF] (:DIAG:SERV:BUS:DC <*numeric*>) . . . 10-21

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FREQ BUS [OFF] (:DIAG:SERV:BUS:FREQ <*numeric*>) 10-21
AZ SWITCH on OFF (:DIAG:SERV:BUS:AZER {OFF|ON|0|1}) 10-22
WAIT COUNT (:DIAG:SERV:BUS:WAIT 10-22
Bus Measurement 10-22
Bus Measurement Procedure 10-22
Bus Measurement Values 10-23
DC Bus Node Descriptions 10-23
0: NONE 10-23
1: +5 V (AUX) (2.025 U) 10-23
2: −15 V (−1.92 U) 10-23
3: −12.6 V (−2.124 U) 10-23
4: −5 V (−2.025 U) 10-24
5: +5 V (2.025 U) 10-24
6: +5.3 V (2.1465 U) 10-24
7: +8.5 V (1.8955 U) 10-24
8: +15 V (AUX) (1.92 U) 10-24
9: +15 V (1.92 U) 10-24
10: +22 V (2.002 U) 10-24
11: FAN POWER 10-24
12: +65 V (2.0605 U) 10-25
13: SRC VTUNE (Source Oscillator VCO Tuning Voltage) 10-25
14: 2ND LO VTUNE (Second Local Oscillator VCO Tuning Voltage) 10-25
15: DET OUT (Detector Output) 10-25
16: LVL CONT (Level Vernier Control Voltage) 10-26
17: DAC OUT (Level DAC Output Voltage) 10-26
18: 1ST LO VTUNE (First Local Oscillator VCO Turning Voltage) 10-26
19: STEP VTUNE (Step Oscillator VCO Turning Voltage) 10-27
20: FN VTUNE (Fractional N Oscillator VCO Turning Voltage) 10-27
21: FN INTEG OUT (Fractional N Oscillator Integrator Output Voltage) . . . 10-28
22: REF VTUNE (Reference Oscillator VCO Tuning Voltage) 10-29
23: 3RD LO VTUNE (Third Local Oscillator VCO Tuning Voltage) 10-29
24: 2ND IF LVL (Second IF Signal Level) 10-29
25: AD VREF (A/D Converter Voltage Reference) 10-29
26: GND (Ground) 10-30
Frequency Bus Node Descriptions 10-30
0: OFF 10-30
1: SOURCE OSC (Source Oscillator) 10-30
2: DIVIDER OUT (Divider Output) 10-30
3: STEP OSC (Step Oscillator) 10-30
4: FN OSC (Fractional N Oscillator) 10-30
5: REF OSC (Reference Oscillator) 10-31
6: 3RD LO OSC (Third Local Oscillator) 10-31
7: SAMPLE HOLD 10-31
CORRECTION CONSTANTS MENU 10-32
FRQ RSP CC ON/off (:DIAG:SERV:CCON:FRES {OFF|ON|0|1}) 10-32
XTAL CC ON/off (:DIAG:SERV:CCON:XTAL {OFF|ON|0|1}) 10-32
IF GAIN CC ON/off (:DIAG:SERV:CCON:IFG {OFF|ON|0|1}) 10-33
SOURCE CC ON/off (:DIAG:SERV:CCON:SOUR {OFF|ON|0|1}) 10-33
Correction Constants 10-33
IF CONTROL MENU 10-35
3rd LO [ ] (:DIAG:SERV:IF:TLOC:MODE {AUTO|AC|DC}) 10-36
IF BPF [ ] (:DIAG:SERV:IF:BPF:MODE {AUTO|BW3M|BW1M|XTAL}) 10-36

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IF GAIN [ ] 10-36
IF RANGE [ ] 10-37
IF LPF [ ] (:DIAG:SERV:IF:LPF:MODE {AUTO|BW5K|BW15K|BW50K|BW150K|THR}) 10-38
S/H BW [ ] (:DIAG:SERV:IF:SHBW:MODE {AUTO|NARR|MIDD|WIDE}) 10-38
A/D MUX [ ] (:DIAG:SERV:IF:ADMX:MODE {AUTO|ALT|DEG0|DEG90}) 10-39
SYNTHESIZER CONTROL MENU 10-40
1st LO OSC [ ] (:DIAG:SYNT:FLOC:MODE {AUTO|SING|TRIP}) 10-41
FN OSC [ ] (:DIAG:SERV:STNT:FN:MODE {AUTO|NARR|WIDE}) 10-41
STEP OSC [ ] 10-41
FREQUENCY OFFSET (:DIAG:SERV:SYNT:FREQ:OFFS<*numeric*>) 10-42
SOURCE CONTROL MENU 10-43
SOURCE AUTO man (:DIAG:SERV:SOUR:MODE {AUTO|MAN}) 10-43
ALC LOOP open CLOSE (:DIAG:SERV:SOUR:ALCL: {OPEN|CLOSE}) 10-43
OUTPUT ATT [ ] (:DIAG:SERV:SOUR:ATT {AUTO|DB0|DB10|DB20|DB30|DB40|DB50|DB60}) 10-43
LVL DAC AUTO man (:DIAG:SERV:SOUR:LEV:DAC:MODE {AUTO|MAN}) 10-44
LVL DAC VALUE (:DIAG:SERV:SOUR:LEV:DAC:VAL <*numeric*>) 10-44
GAIN DAC AUTO man (:DIAG:SERV:SOUR:GAIN:DAC:MODE {AUTO|MAN}) 10-44
GAIN DAC VALUE (:DIAG:SERV:SYNT:STEP:DAC:VAL <*numeric*>) 10-44
BOOTLOADER MENU 10-45
SYSTEM UPDATE 10-45
SYSTEM BACKUP 10-45
PREVIEW DISK 10-46
REBOOT 10-46

11. Theory of Operation
ANALYZER OPERATION 11-1
Spectrum Analyzer Operation 11-2
Network Analyzer Operation 11-2
Test Sets 11-3
ANALYZER FUNCTIONAL GROUPS 11-4
POWER SUPPLY OPERATION 11-5
Line Power Module 11-7
A40 Preregulator 11-7
A50 DC-DC Converter 11-7
Switching Regulator 1 11-7
Switching Regulator 2 11-7
Regulated +5V Digital Supply (+5 VD) 11-7
A50 Shutdown LED 11-7
A2 Post-Regulator 11-8
Shutdown Circuit 11-8
Seven Status LEDs 11-8
A7 Input and A8 Output Attenuator Drive Circuit 11-9
DIGITAL CONTROL OPERATION 11-10
A1 CPU 11-12
A30 Front-Panel Keyboard 11-12
A31 I/O Connector 11-12
A32 I-BASIC Interface 11-12

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A51 GSP . . . 11-13
A54 Inverter . . . 11-13
A52 LCD (Liquid Crystal Display) . . . 11-13
A53 FDD . . . 11-13
SOURCE THEORY . . . 11-14
A5 Synthesizer . . . 11-16
REF OSC . . . 11-16
Leveler . . . 11-16
FRAC N OSC . . . 11-16
STEP OSC . . . 11-17
Multiplier (X 13) . . . 11-18
A4A1 1st LO . . . 11-18
1st Local OSC Circuit . . . 11-18
Single-Loop Operation at Frequency Spans > 45 MHz . . . 11-19
Triple-Loop Operation at Frequency Spans ≤ 45 MHz . . . 11-19
Digital Control Signals for the A4A2 Receiver RF . . . 11-19
A3A1 ALC . . . 11-19
Divider . . . 11-19
Source OSC . . . 11-19
ALC . . . 11-20
A3A2 2nd LO . . . 11-20
2nd Local OSC Circuit . . . 11-20
Source First Mixer . . . 11-21
A3A3 Source . . . 11-21
A7 Output Attenuator . . . 11-21
RECEIVER THEORY . . . 11-23
A8 Input Attenuator . . . 11-25
A9 Input Multiplexer . . . 11-25
A4A2 Receiver RF . . . 11-25
A6 Receiver IF . . . 11-26
IF BPFs and LPFs . . . 11-26
3rd Converter and 3rd LO . . . 11-27
Sample/Hold, A/D Converter, and Sequencer . . . 11-27
Gains W, X, Y, and Z and Ranges F and R . . . 11-27

12. Replaceable Parts
Introduction . . . 12-1
Ordering Information . . . 12-1
Direct Mail Order System . . . 12-1
Exchange Assemblies . . . 12-2
Replaceable Parts List . . . 12-2

13. Post Repair Procedures
INTRODUCTION . . . 13-1
POST REPAIR PROCEDURES . . . 13-1

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A. Manual Changes
Introduction A-1
Manual Changes A-1
Serial Number A-2

B. A20 Motherboard Pin Assignment

C. Power Requirement
Replacing Fuse C-1
Fuse Selection C-1
Power Requirements C-2
Power Cable C-2

Messages
Error Messages in Alphabetical Order Messages-1
Error Messages in Numerical Order Messages-9

Index

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Figures

2-1. Updating Correction Constants Setup 2-5
2-2. 40 MHz Reference Oscillator Frequency Adjustment Setup 2-6
2-3. 40 MHz Reference Oscillator Frequency Adjustment Location 2-7
2-4. 520 MHz Level Adjustment Location 2-8
2-5. 520 MHz Level Adjustment Setup 2-9
2-6. CAL OUT Level Adjustment Setup 2-10
2-7. CAL OUT Level Adjustment Location 2-11
2-8. Comb Generator Adjustment Setup 2-12
2-9. Comb Generator Adjustment Location 2-13
2-10. Comb Generator Output 2-14
2-11. Second Local PLL Adjustment Location 2-16
2-12. Second Local PLL Adjustment Setup 2-17
2-13. Plug Locations 2-18
2-14. DC Offset and Hold Step Adjustment Setup 2-19
2-15. DC Offset and Hold Step Adjustment Locations 2-19
2-16. DC Offset Adjustment Waveform 2-20
2-17. Hold Step Adjustment Waveform 2-21
2-18. Plug Locations 2-22
2-19. Plug Locations 2-23
2-20. 0°/90° Tracking Adjustment Setup 2-24
2-21. 0°/90° Tracking Adjustment Locations 2-24
2-22. Plug Locations 2-25
2-23. Band Pass Filters Adjustments Setup 2-26
2-24. Band Pass Filters Adjustment Locations 2-27
2-25. Final Gain Adjustment Setup 2-29
2-26. Final Gain Adjustment Location 2-30
2-27. Second Local Leakage Adjustment Location 2-31
2-28. Second Local Leakage Adjustment Setup 2-32
2-29. RF OUT Level Correction Constants Setup 2-33
2-30. Spectrum Analyzer Absolute Magnitude Correction Constants Setup 2-34
2-31. Network Analyzer Absolute Magnitude Correction Constants Setup 2-35
2-32. Crystal Filter Correction Constants Setup 2-36
2-33. IF Gain Errors Correction Constants Setup 1 2-37
2-34. IF Gain Errors Correction Constants Setup 2 2-38
2-35. Network Analyzer Magnitude Ratio/Phase Correction Constants Setup 1 2-39
2-36. Network Analyzer Magnitude Ratio/Phase Correction Constants Setup 2 2-40
2-37. 10 MHz Reference Oscillator Frequency Adjustment Location 2-41
2-38. 10 MHz Reference Oscillator Frequency Adjustment Setup 2-42
3-1. Troubleshooting Organization 3-2
3-2. ALL EXT 1 Test Setup 3-5
3-3. Displayed Result of ALL EXT Test 3-6
3-4. ALL EXT 2 Test Setup 3-6
3-5. ALL EXT 3 Test Setup 3-7
3-6. ALL EXT 4 Test Setup 3-7
3-7. ALL EXT 5 Test Setup 3-8
4-1. Recommended Adjustments and Correction Constants. 4-3

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5-1. Power Supply Lines Simplified Block Diagram 5-2
5-2. A50 SHUTDOWN LED Location 5-4
5-3. A1 +5 VD LED Location 5-5
5-4. A2 Eight LED Locations 5-6
5-5. Displayed Test Result 5-6
5-6. Removing Line Fuse 5-8
5-7. A40J1 Output Voltage 5-10
5-8. A1 CPU Connector Locations 5-11
5-9. Fan Troubleshooting Setup 5-13
5-10. A50 DC-DC Converter Troubleshooting Setup 5-14
5-11. A2 Output Voltage Measurement Setup 5-17
5-12. Power Supply Block Diagram 1 5-19
5-13. Power Supply Block Diagram 2 5-20
5-14. Power Supply Block Diagram 3 5-21
6-1. Digital Control Group Simplified Block Diagram 6-2
6-2. A1 EEPROM Location 6-3
6-3. Firmware Revision Label 6-4
6-4. Bootloader Menu Display 6-5
6-5. A1 Eight LEDs' Pattern 6-6
6-6. Bootloader Display 6-10
7-1. Source Group Block Diagram 7-2
7-2. External Test 20 Setup 7-6
7-3. A5 Connector Locations 7-8
7-4. CAL OUT Test Setup 7-8
7-5. Typical CAL OUT Signal 7-9
7-6. INT REF Test Setup 7-10
7-7. Typical INT REF Signal 7-11
7-8. Typical FRAC N OSC Signal in Frequency Bus Measurement 7-12
7-9. FRAC N OSC Signal Level Test Setup 7-12
7-10. FRAC N OSC Typical Signal 7-13
7-11. STEP OSC Test Setup 7-14
7-12. Typical STEP OSC Signal at Center 0 Hz 7-16
7-13. Typical 520 MHz Signal 7-17
7-14. 520 MHz Signal Test Setup 7-17
7-15. EXT REF Test Setup 7-18
7-16. 1st LO OSC Signal Test Setup 7-19
7-17. Typical 1st LO OSC Signal (Single Mode) at A4A1J3 7-20
7-18. Typical 1st LO OSC Signal (Triple Mode) at A4A1J3 7-21
7-19. 1st LO OSC Typical Signal (Single Mode) at A4J4 7-22
7-20. ALC Outputs Test Setup 7-23
7-21. Typical 21.42 MHz Signal 7-24
7-22. 2nd LO OSC Test Setup 7-26
7-23. Typical 2nd Local Oscillator Signal 7-27
7-24. Source IF Test Setup 7-28
7-25. Typical Source IF 7-29
7-26. A3A3 RF Signal Test Setup 7-30
7-27. A7 Output Attenuator Control Signals 7-32
8-1. Receiver Group, Simplified Block Diagram 8-2
8-2. A8 Input Attenuator Control Signals 8-5
8-3. A9J13 Location and Pin Assignments 8-7
9-1. Probe Power Connector Voltages 9-5
10-1. Service Key Menus 10-1
10-2. Service Menu 10-3
10-3. Tests Menu 10-4
10-4. Test Status on the Display 10-5

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10-5. Sample Program Using :DIAG:TEST:RES? 10-6
10-6. External Test Setup 1 10-10
10-7. External Test Setup 2 10-10
10-8. External Test Setup 3 10-11
10-9. External Test Setup 4 10-11
10-10. External Test Setup 5 10-12
10-11. External Test Setup 6 10-18
10-12. Service Modes Menu 10-19
10-13. Bus Measurement Menu 10-21
10-14. Fan Power Typical Trace 10-25
10-15. DET OUT, LVL CONT, and DAC OUT Typical Traces 10-26
10-16. 1st LO VTUNE Typical Trace 10-27
10-17. FN VTUNE Typical Trace 10-28
10-18. FN INTEG OUT Typical Trace 10-29
10-19. Correction Constants Menu 10-32
10-20. IF Control Menu 10-35
10-21. Synthesizer Control Menu 10-40
10-22. Source Control Menu 10-43
10-23. Bootloader Menu 10-45
11-1. Simplified Analyzer Block Diagram 11-1
11-2. 85046A/B S-Parameter Test Set Simplified Block Diagram 11-3
11-3. Power Supply Functional Group, Simplified Block Diagram 11-6
11-4. A2 Eight Status LED 11-9
11-5. Digital Control Group, Simplified Block Diagram 11-11
11-6. Source Simplified Block Diagram 11-15
11-7. Receiver Simplified Block Diagram 11-24
11-8. 4396B Source Group Block Diagram 11-29
11-9. 4396B Receiver Group Block Diagram 11-30
12-1. Top View (Major Assemblies) 12-4
12-2. Bottom View (Major Assemblies) 12-6
12-3. Angle Assembly Parts 1/3 12-7
12-4. Angle Assembly Parts 2/3 12-8
12-5. Angle Assembly Parts 3/3 12-9
12-6. ATT Assembly Parts 1/2 12-10
12-7. ATT Assembly Parts 2/2 12-11
12-8. Front Assembly Parts 1/5 12-12
12-9. Front Assembly Parts 2/5 12-13
12-10. Front Assembly Parts 3/5 12-14
12-11. Front Assembly Parts 4/5 12-15
12-12. Front Assembly Parts 5/5 12-16
12-13. Rear Assembly Parts 1/7 12-17
12-14. Rear Assembly Parts 2/7 12-18
12-15. Rear Assembly Parts 3/7 12-19
12-16. Rear Assembly Parts 4/7 12-20
12-17. Rear Assembly Parts 5/7 12-21
12-18. Rear Assembly Parts 6/7 12-22
12-19. Rear Assembly Parts 7/7 12-23
12-20. Main Frame Assembly Parts 1/19 (A3 Assemblies) 12-24
12-21. Main Frame Assembly Parts 2/19 (A3 Assemblies) 12-25
12-22. Main Frame Assembly Parts 3/19 12-26
12-23. Main Frame Assembly Parts 4/19 (A9 Input Multiplexer Assembly) 12-27
12-24. Main Frame Assembly Parts 5/19 (ATT & Angle Assemblies) 12-28
12-25. Main Frame Assembly Parts 6/19 (A53 FDD Assembly) 12-29
12-26. Main Frame Assembly Parts 7/19 (A20 Motherboard Assembly) 12-30
12-27. Main Frame Assembly Parts 8/19 (A4 First LO/Receiver RF Assembly) 12-31

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12-28. Main Frame Assembly Parts 9/19 (RF Cable Assemblies) 12-32
12-29. Main Frame Assembly Parts 10/19 (A1 CPU Assembly) 12-33
12-30. Main Frame Assembly Parts 11/19 (A40 Pre-regulator Assembly) 12-34
12-31. Main Frame Assembly Parts 12/19 (A50 DC-DC Converter Assembly) 12-35
12-32. Main Frame Assembly Parts 13/19 (A51 GSP Assembly) 12-36
12-33. Main Frame Assembly Parts 14/19 (Front Bezel Assembly) 12-37
12-34. Main Frame Assembly Parts 15/19 (A2 Post Regulator Assembly) 12-38
12-35. Main Frame Assembly Parts 16/19 (A5 and A6 Assemblies) 12-39
12-36. Main Frame Assembly Parts 17/19 12-40
12-37. Main Frame Assembly Parts 18/19 (RF Cable Assemblies) 12-41
12-38. Main Frame Assembly Parts 19/19 (Option 1D5) 12-42
12-39. A9 N Type Connector Replacement 12-43
A-1. Serial Number Plate A-2
B-1. Connector Locations On the A20 Motherboard Circuit Side B-2
B-2. Pin Assignment On the A20 Motherboard Circuit Side B-3
C-1. Power Cable Supplied C-3

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Tables

1-1. Recommended Test Equipment 1-3
2-1. Required Binaries 2-4
4-1. Functional Group to Suspect When a Performance Test Fails 4-4
5-1. A50 Power Supplies 5-15
5-2. Power Supplies on A2 Post-Regulator 5-18
6-1. Troubleshooting Information for Internal Diagnostic Test Failure 6-9
7-1. STEP OSC Frequency 7-15
7-2. A3A3 Source Test Settings 7-31
7-3. A7 Attenuation Test Settings 7-33
8-1. Suspicious Assembly When an ALL EXT Test Fails 8-4
8-2. A8 Control Signal Test Settings 8-6
8-3. A9J13 Pin Description 8-8
8-4. A9 Control Signal Test Settings 8-8
10-1. Test Status Terms 10-6
10-2. Typical STEP VTUNE Values 10-27
11-1. STEP OSC Frequency 11-17
11-2. RF OUT Power, A3A3 Output, and A7 Attenuator (Non-Power Sweep) 11-22
11-3. Stop Power, A7 Attenuation, and Allowable Start Power (Power Sweep) 11-22
11-4. Measurement Setting, Used Filter, and Sampling Mode 11-26
11-5. Gains and Ranges Settings 11-28
12-1. Manufacturers Code List 12-2
12-2. List of Abbreviations 12-3
12-3. Top View (Major Assemblies) 12-5
12-4. Bottom View (Major Assemblies) 12-6
12-5. Angle Assembly Parts 1/3 12-7
12-6. Angle Assembly Parts 2/3 12-8
12-7. Angle Assembly Parts 3/3 12-9
12-8. ATT Assembly Parts 1/2 12-10
12-9. ATT Assembly Parts 2/2 12-11
12-10. Front Assembly Parts 1/5 12-12
12-11. Front Assembly Parts 2/5 12-13
12-12. Front Assembly Parts 3/5 12-14
12-13. Front Assembly Parts 4/5 12-15
12-14. Front Assembly Parts 5/5 12-16
12-15. Rear Assembly Parts 1/7 12-17
12-16. Rear Assembly Parts 2/7 12-18
12-17. Rear Assembly Parts 3/7 12-19
12-18. Rear Assembly Parts 4/7 12-20
12-19. Rear Assembly Parts 5/7 12-21
12-20. Rear Assembly Parts 6/7 12-22
12-21. Rear Assembly Parts 7/7 12-23
12-22. Main Frame Assembly Parts 1/19 (A3 Assemblies) 12-24
12-23. Main Frame Assembly Parts 2/19 (A3 Assemblies) 12-25
12-24. Main Frame Assembly Parts 3/19 12-26
12-25. Main Frame Assembly Parts 4/19 (A9 Input Multiplexer Assembly) 12-27
12-26. Main Frame Assembly Parts 5/19 (ATT & Angle Assemblies) 12-28

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12-27. Main Frame Assembly Parts 6/19 (A53 FDD Assembly) 12-29
12-28. Main Frame Assembly Parts 7/19 (A20 Motherboard Assembly) 12-30
12-29. Main Frame Assembly Parts 8/19 (A4 First LO/RReceiver RF Assembly) 12-31
12-30. Main Frame Assembly Parts 9/19 (RF Cable Assemblies) 12-32
12-31. Main Frame Assembly Parts 10/19 (A1 CPU Assembly) 12-33
12-32. Main Frame Assembly Parts 11/19 (A40 Pre-regulator Assembly) 12-34
12-33. Main Frame Assembly Parts 12/19 (A50 DC-DC Converter Assembly) 12-35
12-34. Main Frame Assembly Parts 13/19 (A51 GSP Assembly) 12-36
12-35. Main Frame Assembly Parts 14/19 (Front Bezel Assembly) 12-37
12-36. Main Frame Assembly Parts 15/19 (A2 Post Regulator Assembly) 12-38
12-37. Main Frame Assembly Parts 16/19 (A5 and A6 Assemblies) 12-39
12-38. Main Frame Assembly Parts 18/19 (RF Cable Assemblies) 12-41
12-39. Main Frame Assembly Parts 19/19 (Option 1D5) 12-42
12-40. A9 N Type Connector Replacement 12-43
13-1. Post Repair Procedures 13-1
A-1. Manual Changes by Serial Number A-1
A-2. Manual Changes by Firmware Version A-1
B-1. Signal Name B-4
C-1. Fuse Selection C-1

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1

General Information

INTRODUCTION

This *Service Manual* is a guide to servicing the 4396B Network/Spectrum/Impedance Analyzer. There are two manuals required to service the analyzer, *Performance Test Manual* (PN 04396-90120) and this manual. The *Performance Test Manual* provides information about performance testing the analyzer. The other information required to servicing the analyzer is provided in this manual. This manual contains information about adjusting, troubleshooting, and repairing the analyzer.

ORGANIZATION OF SERVICE MANUAL

This manual consists of major chapters listed below. The chapters are divided by tabs. This section describes the names of the tabs and the content of each chapter.

- *Adjustments and Correction Constants* provides procedures for adjusting the analyzer after repair or replacement of an assembly. Some of the adjustments updates correction constants stored into the EEPROM on the A1 CPU. The correction constants is updated by using the adjustment program (PN 04396-18030).

Note The next seven, gray-tabbed chapters are the core troubleshooting chapters.



- *Troubleshooting.* The troubleshooting strategy is to systematically verify portions of the analyzer, and thus narrow down the cause of a problem to the defective assembly. This chapter is the first of a series of troubleshooting procedures. It checks the operation of the analyzer independent of system peripherals, and suggests how to remedy system problems. The *Operator's Check* is located in this chapter.
- *Isolate Faulty Group Troubleshooting* is used after a problem has been shown to be in two analyzer functional groups: Source, and Receiver. This section suggests how to isolate the fault to one of the two functional groups in the analyzer.
- *Power Supply Troubleshooting*
- *Digital Control Troubleshooting*
- *Source Troubleshooting*
- *Receiver Troubleshooting*
- *Accessories Troubleshooting*

  Each of the five functional group chapters above verifies its constituent assemblies until the faulty assembly is identified. *Accessories Troubleshooting* verifies external RF cables and calibration kit devices. *Accessories Troubleshooting* is the last of the gray-tabbed troubleshooting chapters.

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Note The following chapters are, for the most part, reference material.



- *Service Key Menus* documents the functions of the menus accessed from (System), SERVICE MENU. These menus let the operator test, verify, adjust, control, and troubleshoot the analyzer. GPIB service mnemonics are included.
- *Theory of Operation* explains the overall operation of the analyzer, the division into functional groups, and the operation of each functional group.
- *Replaceable Parts* provides part numbers and illustrations of the replaceable assemblies and miscellaneous chassis parts, together with ordering information.
- *Post-Repair Procedures* contains the table of related service procedures. It is a table of adjustments and verification procedures to be performed after repair or replacement of each assembly.
- *Appendices* contains the manual changes information (required to make this manual compatible with earlier shipment configurations of the analyzer), the motherboard pin assignment list, and the power requirement.
- *Messages* contains the service related error message list.

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TABLE OF SERVICE TEST EQUIPMENT

The first part of Table 1-1 lists all of the equipment required to verify, adjust, and troubleshoot the analyzer and perform the operator's check. The table also notes the use and critical specifications of each item, and the recommended models. Equipment other than the recommended models may be substituted if the equipment meets or exceeds the critical specifications.

In addition to test equipment listed in Table 1-1, the following tools are also required:

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Pozidriv screwdriver, pt size #2 (medium)
- IC extractor
- Open-end wrench, 1/4 inch
- Open-end wrench, 5/16 inch
- Hex socket, 7/32 inch (5.5 mm)
- Flat edge screwdriver

Table 1-1. Recommended Test Equipment

Equipment	Critical Specifications	Recommended Model/ Agilent Part Number	Qty	Use[1]
Computer	HP 9000 Series 200/300[2]		1	A
BASIC Operating System	Revision 5.0 or above		1	A
Mass Storage	3.5 inch Microfloppy Disk Drive		1	A
Program	4396B Adjustments Program (3.5 inch)	PN 04396-18030	1	A
Frequency Counter	Frequency Range: 20 MHz to 1 GHz, Time Base Error: $\leq \pm 1.9 \times 10^{-7}$/year	5343A Opt. 001[3]	1	P, A
Frequency Standard[4]	Frequency: 10 MHz, Time Base Error: $\leq \pm 1 \times 10^{-10}$/year	5061B	1	P
Spectrum Analyzer	Frequency Range: 100 kHz to 4 GHz	8566A/B	1	P, A, T
Network Analyzer	Frequency Range: 300 kHz to 1.8 GHz	8753A/B/C	1	P
Power Meter	No substitute	436A Opt. 022, 437B, or 438A	1	P, A
Power Sensor	Frequency Range: 20 MHz to 1.8 GHz, Power: +5 dBm to −20 dBm	8482A	1	P, A
Power Sensor	Frequency Range: 50 MHz to 1.8 GHz, Power: −60 dBm to −20 dBm	8481D	1	P, A
Function Genarator	Frequency Range: 10 Hz to 10 kHz, Level Accuracy: ±0.2 dB, Return loss: > 20 dB	3325A	1	P
Function Genarator	Frequency Range: 20 MHz, Level Accuracy: ±0.15 dB	3335A	1	A

1 P: Performance Tests, A: Adjustments and Correction Constants, T: Troubleshooting

2 Excluding HP 9826A

3 Option 001 (optional time base) is not required, when a frequency standard in Table 1-1 is available.

4 Required for testing an analyzer equipped with Option 1D5 (High Stability Frequency Reference).

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Table 1-1. Recommended Test Equipment (continued)

Equipment	Critical Specifications	Recommended Model/ Agilent Part Number	Qty	Use[1]
Signal Generator	Frequency Range: 100 kHz to 2.14 GHz, SSB Phase Noise at 1 kHz offset: < −110 dBc/Hz, SSB Phase Noise at 10 kHz offset: < −119 dBc/Hz, Harmonics: < −30 dBc	8663A or 8642B	1	P, A
Signal Generator	Frequency Range: 100 kHz to 1.82 GHz	8663A or 8642B	1	P, A
Oscilloscope		54600B	1	A
Oscilloscope Probe	Impedance: 1 MΩ	10431A	1	A
Step Attenuator[1]	Attenuation Range: 0 dB to 70 dB, Step: 10 dB, VSWR: ≤ 1.02	8496A/G Option 001 and H60[2]	1	P
Step Attenuator[1]	Attenuation Range: 0 dB to 10 dB, Step: 1 dB, VSWR: ≤ 1.02	8494A/G Option 001 and H60[3]	1	P
Attenuator/Switch Driver	No substitute	11713A[4]	1	P
50Ω Type-N Calibration Kit	No substitute	85032B	1	P
T/R Test Sets	Frequency Range: 300 kHz to 1.8 GHz, Directivity: ≥ 40 dB	85044A	1	P
50 MHz Low Pass Filter	Rejection at 75 MHz: ≥ 60 dB	PN 0955-0306	1	P
Termination	50Ω Termination	909C Opt 012 or part of 85032B[5]	3	P, A, T
6 dB Fixed Attenuation	50 Ω, N(m)-N(f)	8491A Opt 006	2	P
6 dB Fixed Attenuation	50 Ω, N(m)-N(f), VSWR ≤ 1.015	8491A Opt 006 & Opt H60[6]	2	P
Two-Way Power Splitter	Frequency Range: 100 kHz to 1.8 GHz, Output Tracking: ≤ 0.15 dB	11667A	1	P, A, T
Cables	Type-N cable, 50 Ω	11500B or part of 11851B[7]	4	P, A, T
	RF cable kit	11851B	1	P, A
	BNC cable, 61 cm, 50 Ω	PN 8120-1839	1	P, A, T
	BNC cable, 122 cm, 50 Ω	PN 8120-1840	2	P, A, T
	GPIB cable	10833A/B/C	3	A

1 Calibration values at 50 MHz are required in the tests. See the *Calibration Data Required for Step Attenuators* in *Performance Test Manual* .

2 An 8496A/G step attenuator with required low VSWR (≤ 1.02) can be purchased by specifying option H60.

3 An 8494A/G step attenuator with required low VSWR (≤ 1.02) can be purchased by specifying option H60.

4 Required when an 8494G or 8496G step attenuator is used in the tests.

5 The 85032B includes a type-N(m) 50 Ω termination.

6 An 8491A Opt. 006 fixed attenuator with required low VSWR (≤ 1.015) can be purchased by specifying Opt. H60.

7 The 11851B includes three N(m)-N(m) cables of 61 cm and a N(m)-N(m) cable of 88 cm.

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Table 1-1. Recommended Test Equipment (continued)

Equipment	Critical Specifications	Recommended Model/ Agilent Part Number	Qty	Use[1]
Adapters	BNC(f)-BNC(f) adapter, 50 Ω	PN 1250-0080	1	P
	BNC(f)-SMA(f) adapter, 50 Ω	PN 1250-0562	1	P, A
	Tee BNC(m)-(f)-(f) adapter, 50 Ω	PN 1250-0781	1	P, A
	SMB(m)-SMB(m) adapter, 50 Ω	PN 1250-0813	1	T
	SMC(f)-BNC(f) adapter, 50 Ω	PN 1250-0832	1	A
	SMB(f)-BNC(f) adapter, 50 Ω	PN 1250-1236	1	A
	N(f)-BNC(f) adapter, 50 Ω	PN 1250-1474	1	P
	N(m)-N(m) adapter, 50 Ω	PN 1250-1475	1	P, A, T
	N(m)-BNC(f) adapter, 50 Ω	PN 1250-1476	1	P, A, T
	N(f)-BNC(m) adapter, 50 Ω	PN 1250-1477	1	P, A, T
	SMA(m)-BNC(f) adapter, 50 Ω	PN 1250-1548	1	T
	SMA(m)-SMA(f) right angle adapter, 50 Ω	PN 1250-1741	1	A, T
	APC3.5(m)-APC3.5(f) adapter, 50 Ω	PN 1250-1866	1	P, A
	APC7.5-N(f) adapter, 50 Ω	11524A or part of 85032B[1]	1	P
	BNC(f)-SMA(m) adapter 50 Ω	PN 1250-1548	1	A

1 The 85032B includes two APC7.5-N(f) adapters.

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2

Adjustments and Correction Constants

Introduction

This chapter describes the Adjustments and Correction Constants procedures required to ensure that the 4396B Network/Spectrum/Impedance Analyzer is within its specifications. These adjustments should be performed along with periodic maintenance to keep the analyzer in optimum operating condition. The recommended calibration period is 12 months. If proper performance cannot be achieved after the Adjustments and Correction Constants procedures are performed, see Chapter 3.

Note



The correction constants are empirically derived data that is stored in memory and then recalled to refine the analyzer's measurement and to define its operation.

Safety Considerations

This manual contains NOTEs, CAUTIONs, and WARNINGs that must be followed to ensure the safety of the operator and to keep the instrument in a safe and serviceable condition. The adjustments must be performed by qualified service personnel.

Warning



Any interruption of the protective ground conductor (inside or outside the analyzer) or disconnection of the protective ground terminal can make the instrument dangerous. Intentional interruption of the protective ground system for any reason is prohibited.

The removal or opening of covers for adjustment, or removal of parts other than those that are accessible by hand will expose circuits containing dangerous voltage levels.

Remember that the capacitors in the analyzer can remain charged for several minutes, even through you have turned the analyzer OFF and unplugged it.

Warning



The adjustments described in this chapter are performed with power applied and the protective covers removed. Dangerous voltage levels exist at many points and can result in serious personal injury or death if you come into contact with them.

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Required Equipment

Table 1-1 lists the equipment required to perform the Adjustments and the Correction Constants procedures described in this chapter. Use only calibrated test equipment when adjusting the analyzer. If the recommended test equipment is not available, equipment whose specifications are equal to, or surpasses those of the recommended test equipment may be used.

Warm-up for Adjustments and Correction Constants

Warm-up the analyzer for at least 30 minute before performing any of the following Adjustments and Correction Constants procedures to ensure proper results and correct instrument operation.

Instrument Cover Removal

To gain access to the adjustment components, you need to remove the top cover and the side covers.

Order Of Adjustments

When performing more than one Adjustments or Correction Constants procedure, perform them in the order they appear in this chapter. The procedures are presented in the following order:

- 40 MHz Reference Oscillator Frequency Adjustment
- 520 MHz Level Adjustment
- CAL OUT Level Adjustment
- Comb Generator Adjustment
- Step Pretune Correction Constants
- Second Local PLL Lock Adjustment
- DC Offset and Hold Step Adjustments
- 0°/90° Tracking Adjustment
- Band Pass Filters Adjustments
- Final Gain Adjustment
- Source Mixer Local Leakage Adjustment
- RF OUT Level Correction Constants
- Spectrum Analyzer Absolute Magnitude Correction Constants
- Network Analyzer Absolute Magnitude Correction Constants
- Crystal Filter Correction Constants
- IF Gain Errors Correction Constants
- Network Analyzer Magnitude Ratio/Phase Correction Constants
- 10 MHz Reference Oscillator Frequency Adjustment (Option 1D5 Only)

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Updating Correction Constants using the Adjustments Program

This section provides general information on how to update the Correction Constants using the adjustments program.

Adjustments Program

The adjustments program is provided on one double-sided diskette. Refer to Table 1-1 for the Agilent part number of the adjustement program. The files contained on the diskette are as follows:

ADJ4396B	Adjustments Program
TE_A4396B	Equipment Configuration Program

Note



To prevent accidental deletion or destruction of the program, make working copies of the furnished master diskette (HFS or SRM system). Use the working copies for daily use. Keep the master diskettes in a safe place and use them only for making working copies.

Keyboard and Mouse Operation

The menus in "ADJ4396B" use a window format. The window format menu supports keyboard and mouse operations as follows:

- Keyboard Operation

  1. Press (▲), (▼) keys until your preference is highlighted.
  2. Choose the highlighted item by pressing (RETURN) or (SELECT) ((ENTER) or (EXECUTE), if Nimitz Keyboard).
  3. If `QUIT` or `EXIT` is displayed in a menu, select one of these to exit the menu. Otherwise, press (▼) ((CONTINUE), if Nimitz Keyboard) to exit. When you exit menus, the program displays another menu.

Note



Press (?) to access on-screen help information for the selection you have highlighted. Help information appears in a display window.

Press (RETURN) or (SELECT) ((ENTER) or (EXECUTE), if Nimitz Keyboard) to turn off the help screen.

- Mouse Operation

  1. Slide the mouse up or down until your preference is highlighted.
  2. Choose the highlighted item by pressing left-hand button on the mouse, or slide the mouse to the right.
  3. If `QUIT` or `EXIT` is displayed in a menu, select one of these to exit the menu. Otherwise, slide the mouse to the left to exit. When you exit menus, the program displays another menu.

Note



Press the right-hand mouse button to access on-screen help information for the selection you have highlighted. Help information appears in a display window.

Press the left-hand mouse button to turn off the help screen.

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Controller Requirement

The following controller system is required to run the adjustments program.

Controller	HP 9000 Series 200/300 computer
	Excluding HP 9826A computers
	Must have inverse video capability
	At least 4 M bytes of RAM
Mass Storage	At least one 3.5 inch GPIB Flexible Disk Drive
	HFS formatted hard disk system or SRM system are supported.

The controller must be equipped with HP BASIC versions between 5.1 and 5.13, and the language extension files listed in Table 2-1.

Table 2-1. Required Binaries

Name	Version	Description
GRAPH	5.2	Graphics
GRAPHX	5.2	Graphics Extensions
IO	5.1	I/O
MAT	5.1	Matrix Statements
PDEV	5.0	Program Development
KBD	5.1	Keyboard Extensions
CLOCK	5.0	Clock
MS	5.1	Mass Storage
ERR	5.1	Error Message
DISC	5.0	Small Disc Driver
CS80	5.0	CS80 Disc Driver
GPIB	5.0	GPIB Interface Driver
FGPIB	5.0	GPIB Interface Driver
CRTB	5.2	Bit-mapped CRT Driver
CRTA	5.1	Alpha CRT Driver
CRTX	5.1	CRT Extensions
EDIT	5.1	List and Edit
SRM	5.1	Shared Resource Management
DCOMM	5.0	Datacomm Interface Driver
HFS	5.3	Hierarchical File System
COMPLEX	5.1	Complex Arithmetic

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Updating Correction Constants

Correction Constants are updated using the following procedure:

1. Connect the equipment as shown in Figure 2-1

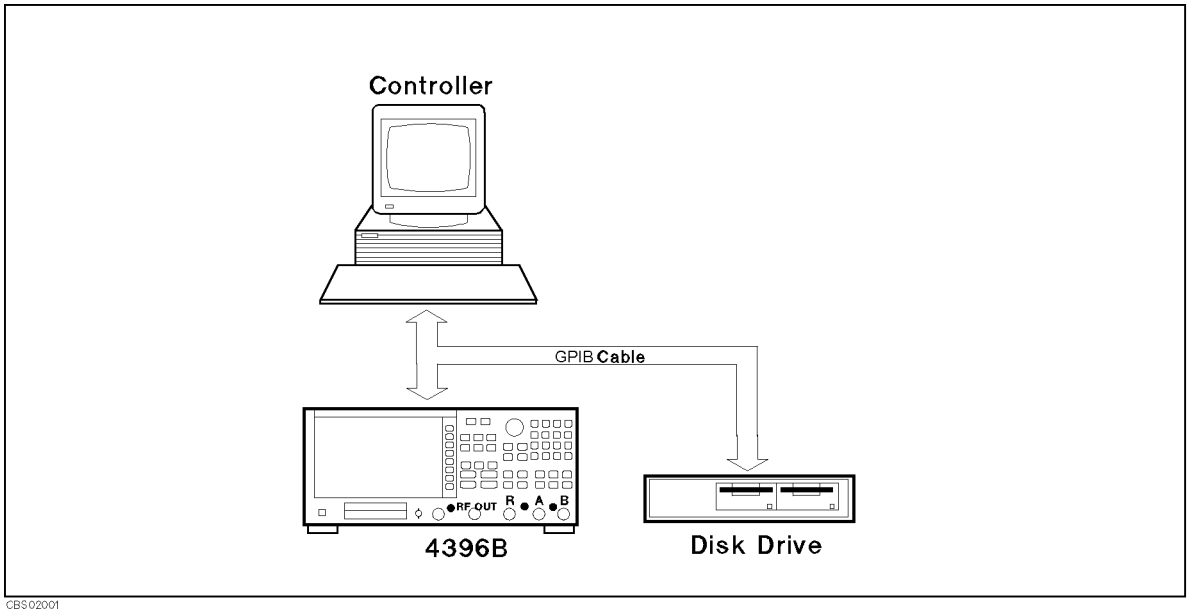


Figure 2-1. Updating Correction Constants Setup

Note

Steps 2 to 5 are used to select the equipment and to set their GPIB addresses. When you perform the Adjustments Program the first time, perform these steps to select the equipment and the GPIB address. After that, perform the "TE_A4396B" program only when you want to change the equipment or the GPIB address.

2. Locate the Equipment Configuration Program "TE_A4396B" in the address of the drive or the directly where the Adjustment Program "ADJ4396B" will be run.
3. Set the mass storage unit specifier (MSUS) to the address of the drive or the directory where "TE_A4396B" is located.
4. Load and run "TE_A4396B".
5. Follow the instructions on the controller's screen until the program ends.
6. Set the mass storage unit specifier (MSUS) to the address of the drive or the directory where the Adjustment Program "ADJ4396B" is located.
7. Load and run "ADJ4396B".
8. A window format menu is displayed.
9. Choose "INITIAL SETUP" if you want to update the Calibrated Value for the power sensor.
10. Choose the item that you want to perform.
11. Follow the instruction on the controller's screen until the program ends. The equipment connections are shown in each Correction Constants procedure in this chapter.

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40 MHz Reference Oscillator Frequency Adjustment

The purpose of this procedure is to adjust the 40 MHz reference oscillator frequency.

Required Equipment

Frequency Counter ..... 5343A Option 001
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Connect the equipment as shown in Figure 2-2.

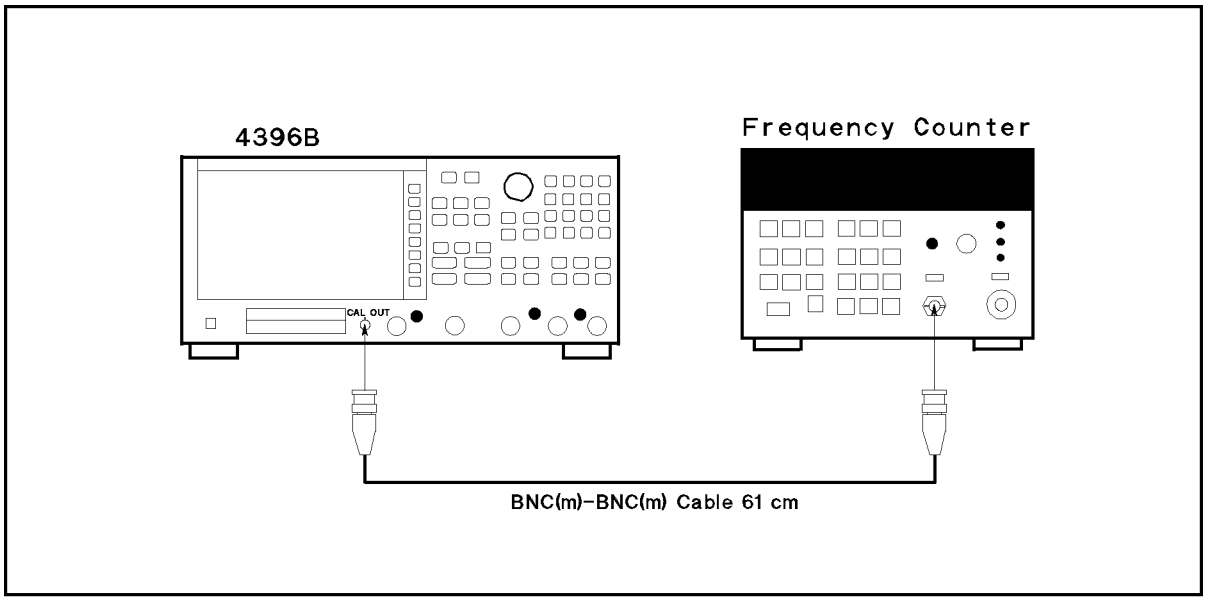


Figure 2-2. 40 MHz Reference Oscillator Frequency Adjustment Setup

2. Set the frequency counter as follows:

   Input Impedance 50 Ω
   Frequency Range 10 Hz - 500 MHz

3. Adjust A5 “40 MHz FREQ ADJ” until the frequency counter reading is within 20 MHz ± 2 Hz. The adjustment location is shown in Figure 2-4.

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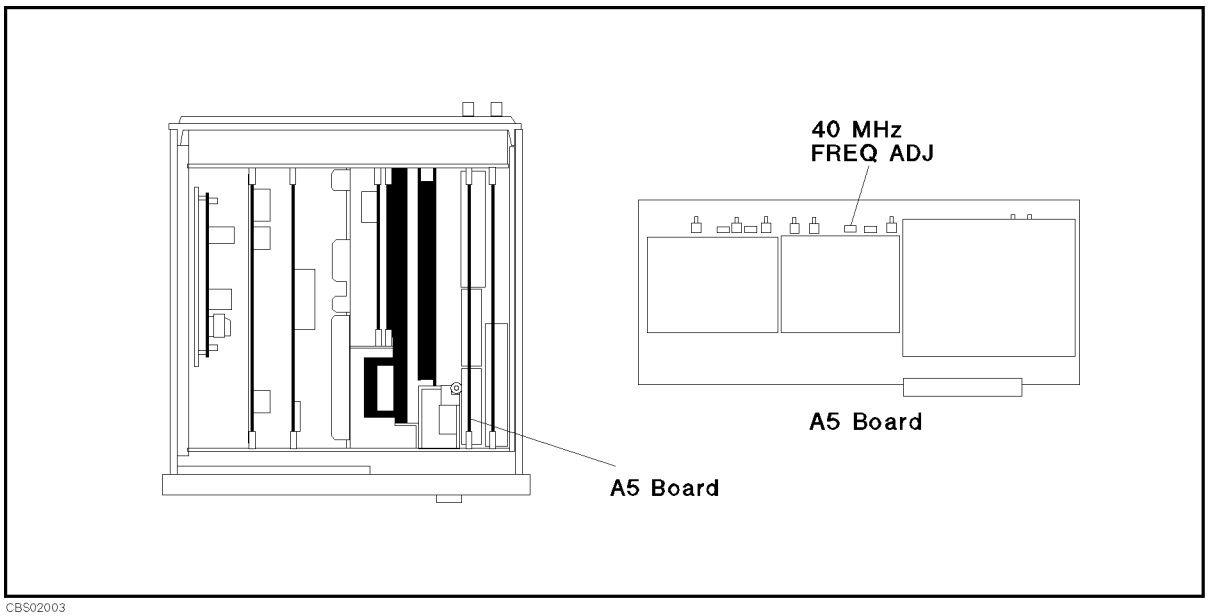


Figure 2-3. 40 MHz Reference Oscillator Frequency Adjustment Location

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520 MHz Level Adjustment

The purpose of this procedure is to adjust the 520 MHz output level.

Required Equipment

Spectrum Analyzer 8566A/B
SMC(f)-BNC(f) adapter ..... PN 1250-0832
N(m)-BNC(f) adapter ..... PN 1250-1476
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Turn the analyzer OFF.
2. Remove the "J" cable from the A5 "520 MHz OUT" connector. The connector location is shown in Figure 2-4.

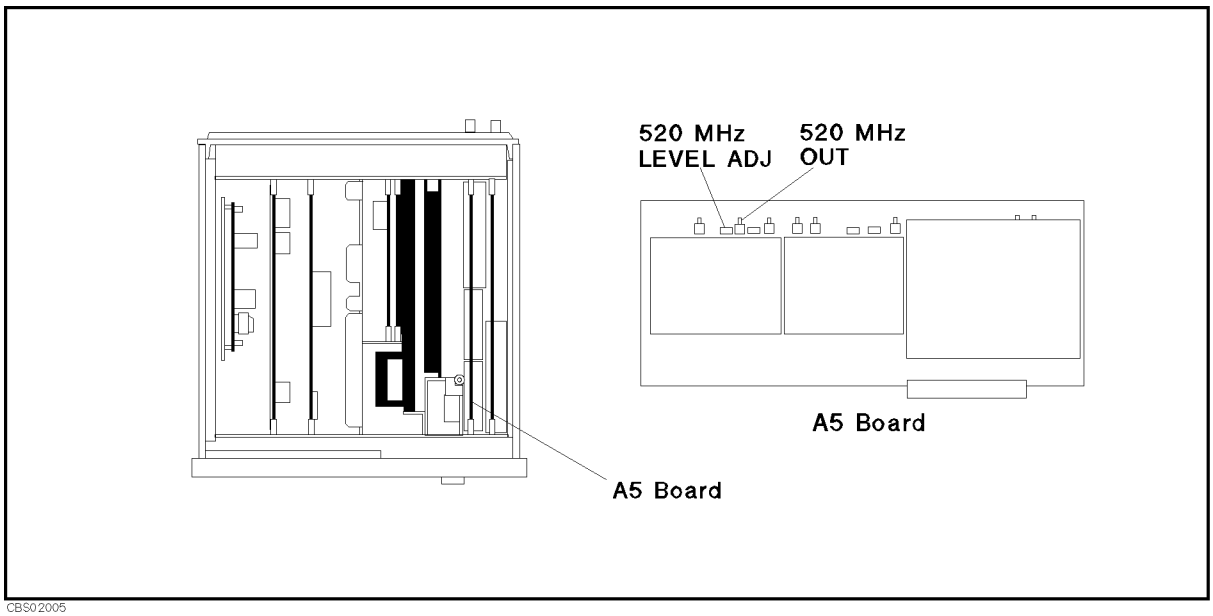


Figure 2-4. 520 MHz Level Adjustment Location

3. Connect the equipment as shown in Figure 2-5.

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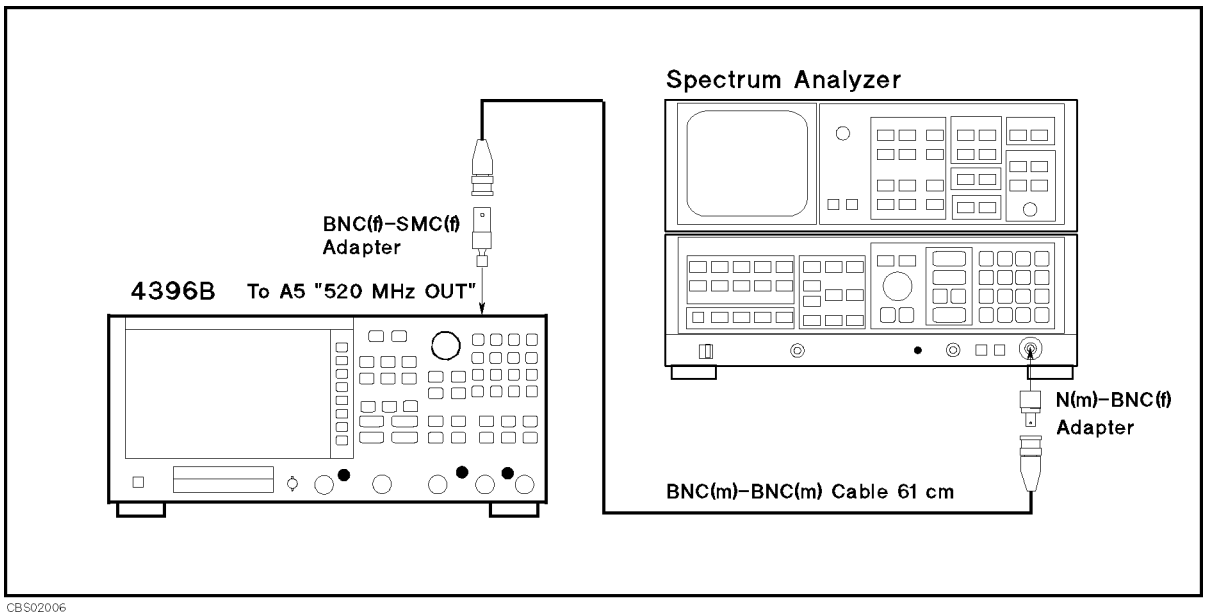


Figure 2-5. 520 MHz Level Adjustment Setup

4. Set the spectrum analyzer as follows:

CENTER Frequency	520 MHz
SPAN	1 MHz
RBW	100 kHz

5. Turn the 4396B analyzer ON.
6. Adjust A5 “520 MHz LEVEL ADJ” until the spectrum analyzer reading for 520 MHz signal level is within −15 ± 0.2 dBm. The adjustment location is shown in Figure 2-4.
7. Turn the 4396B analyzer OFF.
8. Reconnect the “J” cable to the A5 “520 MHz OUT” connector.

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CAL OUT Level Adjustment

The purpose of this procedure is to adjust the CAL OUT level.

Required Equipment

Power Meter 436A
Power Sensor 8482A
N(f)-BNC(m) adapter ..... PN 1250-1477

Procedure

1. Connect the power sensor to the power meter. Calibrate the power meter for the power sensor.
2. Connect the equipment as shown in Figure 2-6.

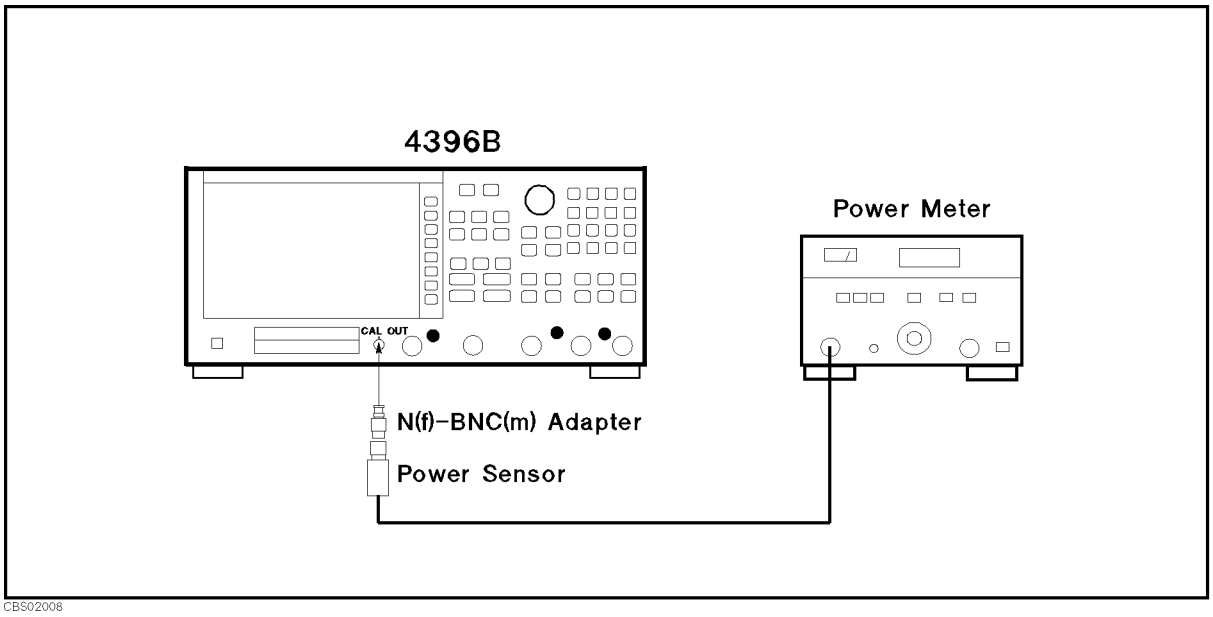
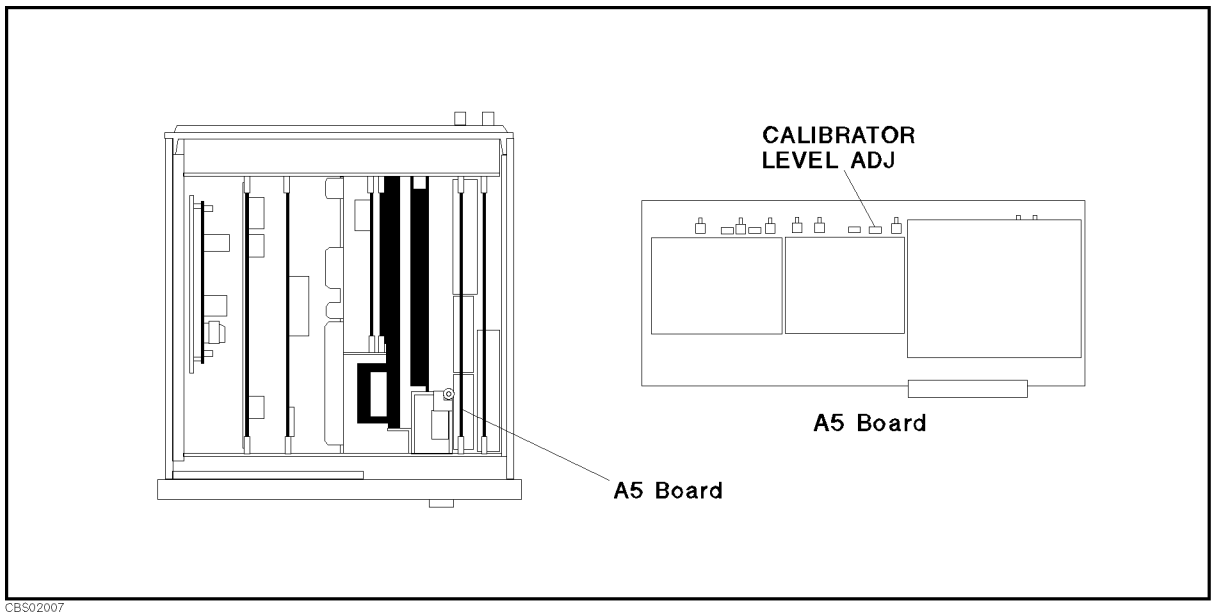


Figure 2-6. CAL OUT Level Adjustment Setup

3. Adjust A5 “CALIBRATOR LEVEL ADJ” until the power meter reading is within −20 ±0.2 dBm . The adjustment location is shown in Figure 2-7.

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Figure 2-7. CAL OUT Level Adjustment Location

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Comb Generator Adjustment

The purpose of this procedure is to adjust the comb generator output level.

Required Equipment

Spectrum Analyzer	8566A/B
SMB(f)-BNC(f) adapter	PN 1250-1236
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 122 cm	PN 8120-1840

Procedure

1. Turn the 4396B analyzer OFF.
2. Connect the equipment as shown in Figure 2-8. A5 “COMB OUT” connector location is shown in Figure 2-9

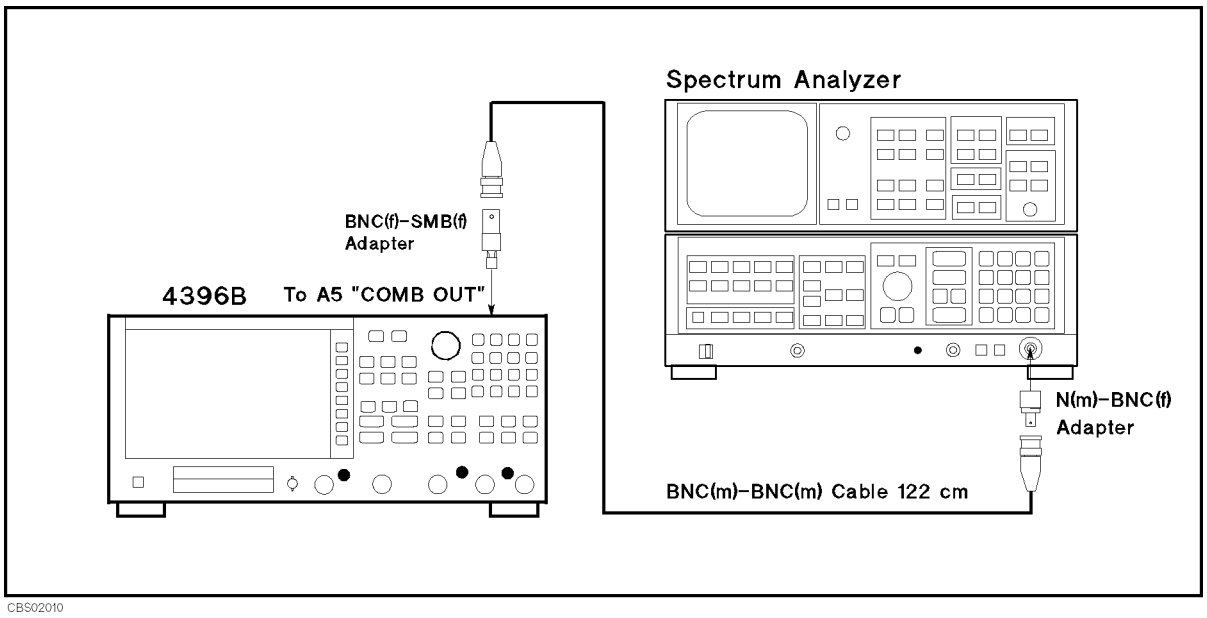


Figure 2-8. Comb Generator Adjustment Setup

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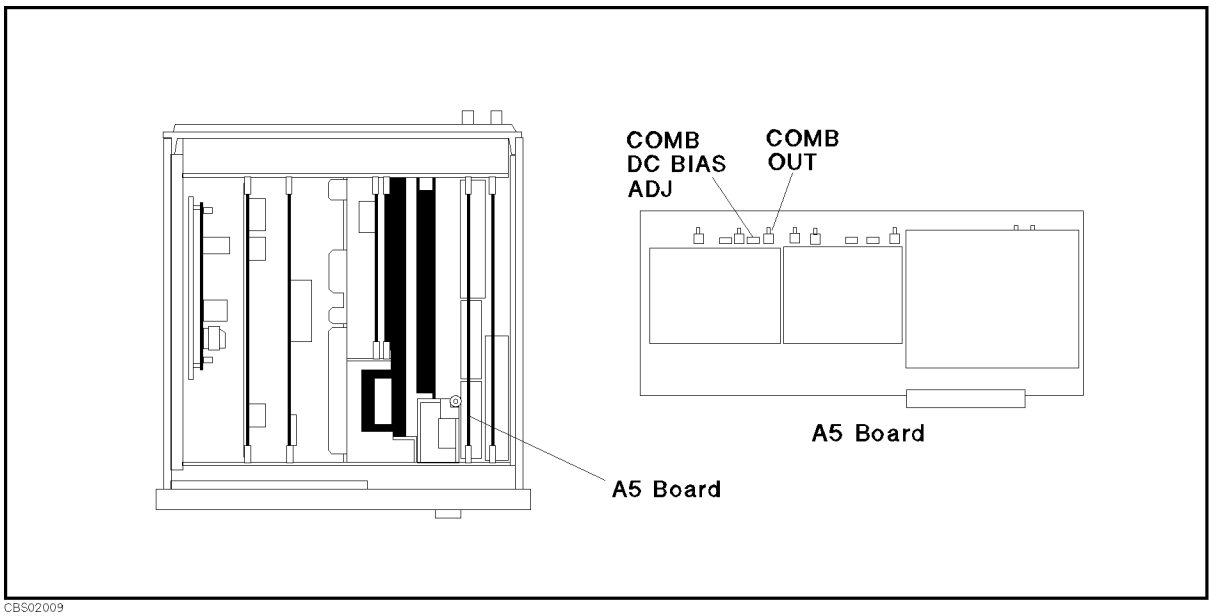


Figure 2-9. Comb Generator Adjustment Location

3. Set the spectrum analyzer as follows:

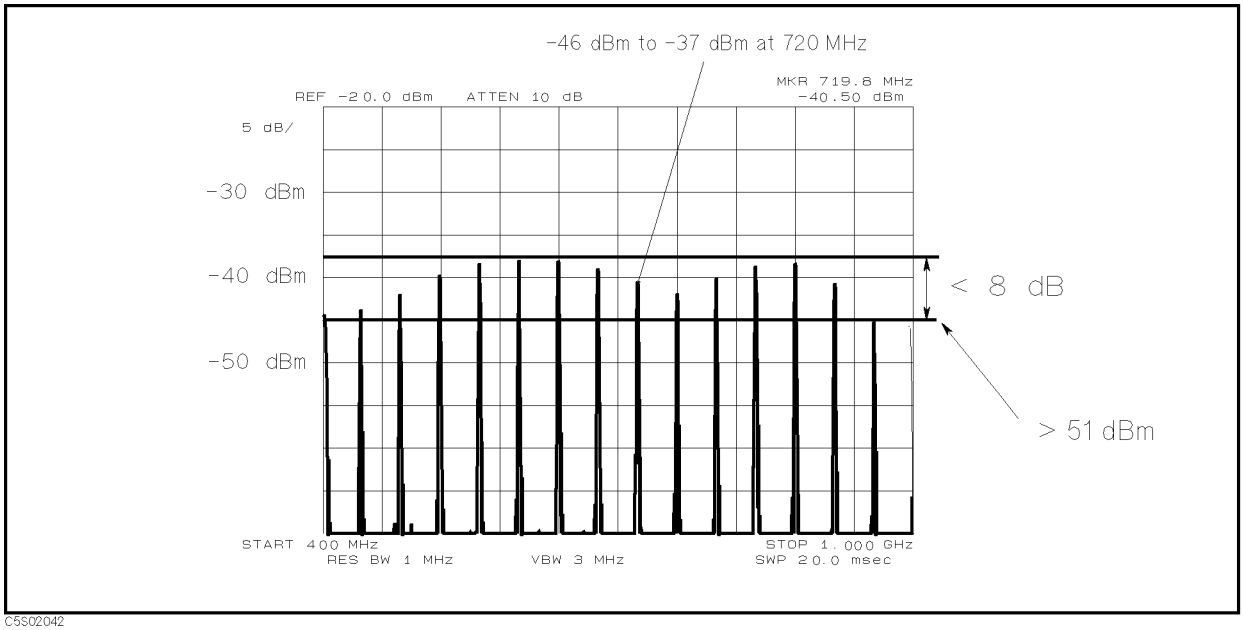
Start Frequency	400 MHz
Stop Frequency	1 GHz
RBW	1 MHz
Reference Level	– 20 dBm
Scale	5 dB/div

4. Turn the 4396B analyzer ON.
5. Adjust A5 “COMB DC BIAS ADJ” until the spectrum analyzer display meets the following requirements:

720 MHz Signal Level	between −46 and −37 dBm
480 MHz to 920 MHz Flatness	< 8 dB
480 MHz to 920 MHz Signal Level	> −51 dBm

The adjustment location is shown in Figure 2-9. The typical spectrum analyzer display is shown in Figure 2-10.

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Figure 2-10. Comb Generator Output

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Step Pretune Correction Constants

The purpose of this procedure is to generate the correction constants that are used to pretune the step loop oscillator.

Required Equipment

None

Procedure

1. Run the adjustment program and display the main menu (see “Updating Correction Constants using the Adjustments Program”).
2. Choose the Step Pretune Correction Constants.
3. Follow the adjustment program instructions to update the correction constants.

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Second Local PLL Lock Adjustment

The purpose of this procedure is to lock the second local Phase Lock Loop (PLL).

Required Equipment

Spectrum Analyzer	8566A/B
BNC(f)-SMA(m) adapter	PN 1250-1548
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 122 cm	PN 8120-1840

Procedure

1. Turn the 4396B analyzer OFF.
2. Remove the "D" cable from the A3A1 "ALC Out" connector. Remove the "I" cable from the A3A2 "Second Local Out" connector. The connector locations are shown in Figure 2-11.

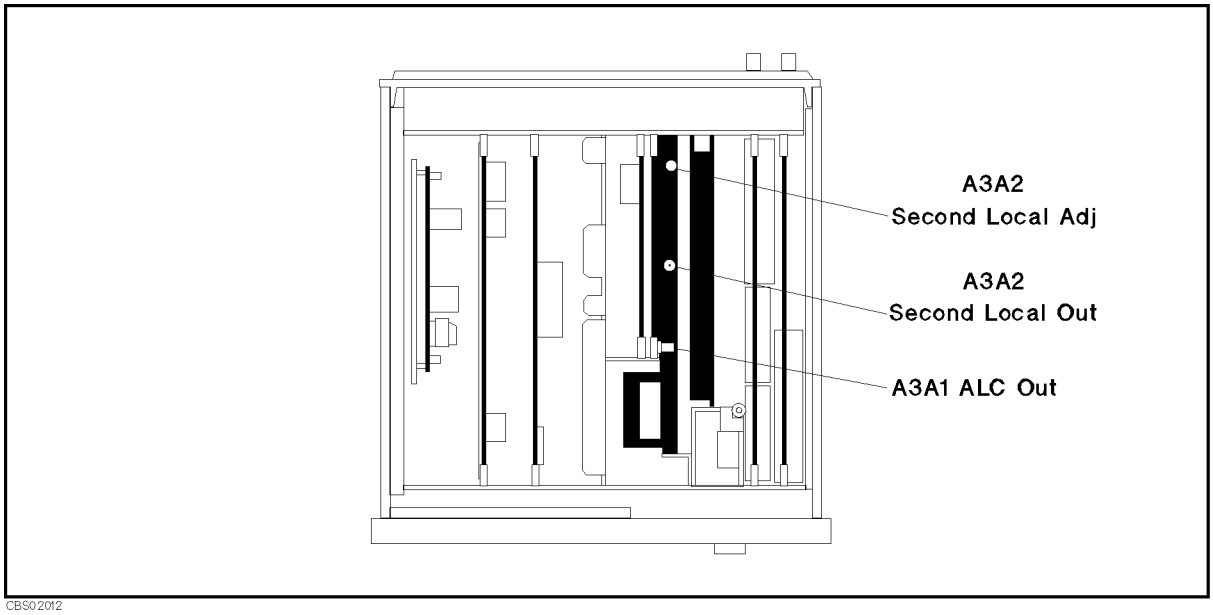


Figure 2-11. Second Local PLL Adjustment Location

3. Connect the equipment as shown in Figure 2-12.

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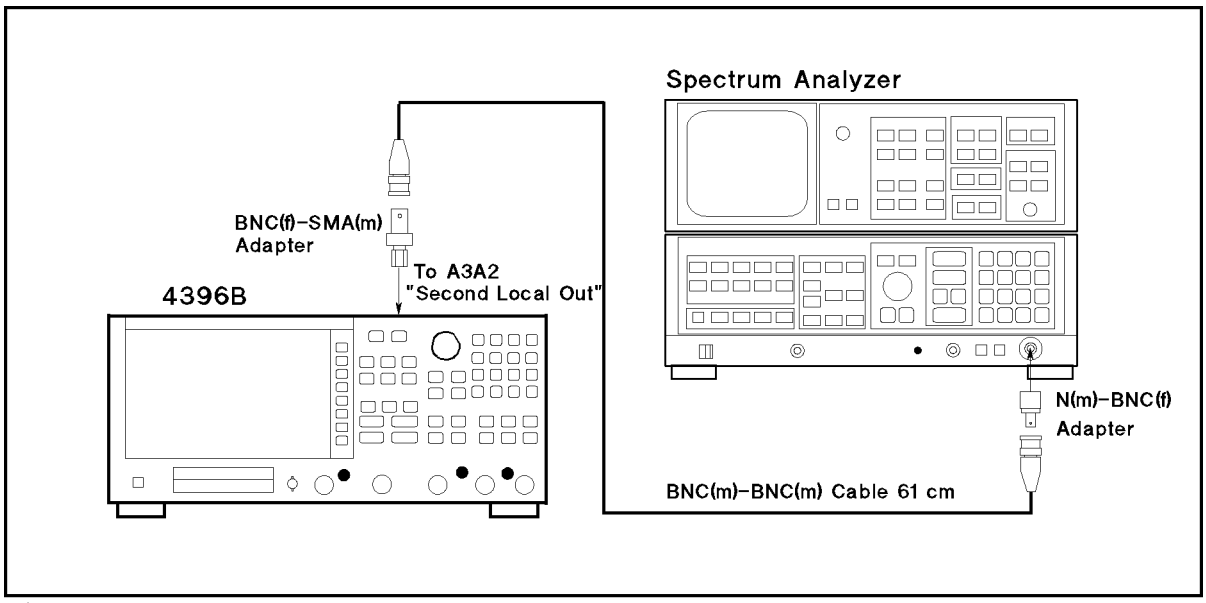


Figure 2-12. Second Local PLL Adjustment Setup

4. Set the spectrum analyzer as follows:

Center Frequency	2.08 GHz
Span	400 MHz
RBW	1 MHz

5. Turn the 4396B analyzer ON.
6. Press the following keys to execute adjust test No.44:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (4), (4), (x1), EXECUTE TEST

7. Adjust A3A2 “Second Local Adj” until 2.08 GHz appears constantly on the spectrum analyzer display and the 4396B analyzer reading is between the limit lines. If 2.24 GHz appears, rotate “Second Local Adj” clockwise. If 1.92 GHz appears, rotate “Second Local Adj” counterclockwise. The adjustment location is shown in Figure 2-11.
8. Turn the analyzer OFF.
9. Reconnect the “I” cable to the A3A2 “Second Local Out” connector. Reconnect the “D” cable to the A3A1 “ALC Out” connector.

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DC Offset and Hold Step Adjustment

The purpose of this procedure is to minimize the hold step and DC offset of the sample hold output.

Required Equipment

Oscilloscope 54600B
10:1 Divider Probe, 1 MΩ 10431A

Procedure

1. Turn the analyzer OFF.
2. To gain access to the adjustment components, remove the side panel on the control keys side.
3. Pull the A6 board out. Place the board on the analyzer with the component side facing upward.
4. Remove the shield case from the board.
5. Pull the plugs that block the "DC OFFSET ADJ" holes out (see Figure 2-13). If you are also going to do the 0°/90° tracking adjustment, pull the other two plugs out.

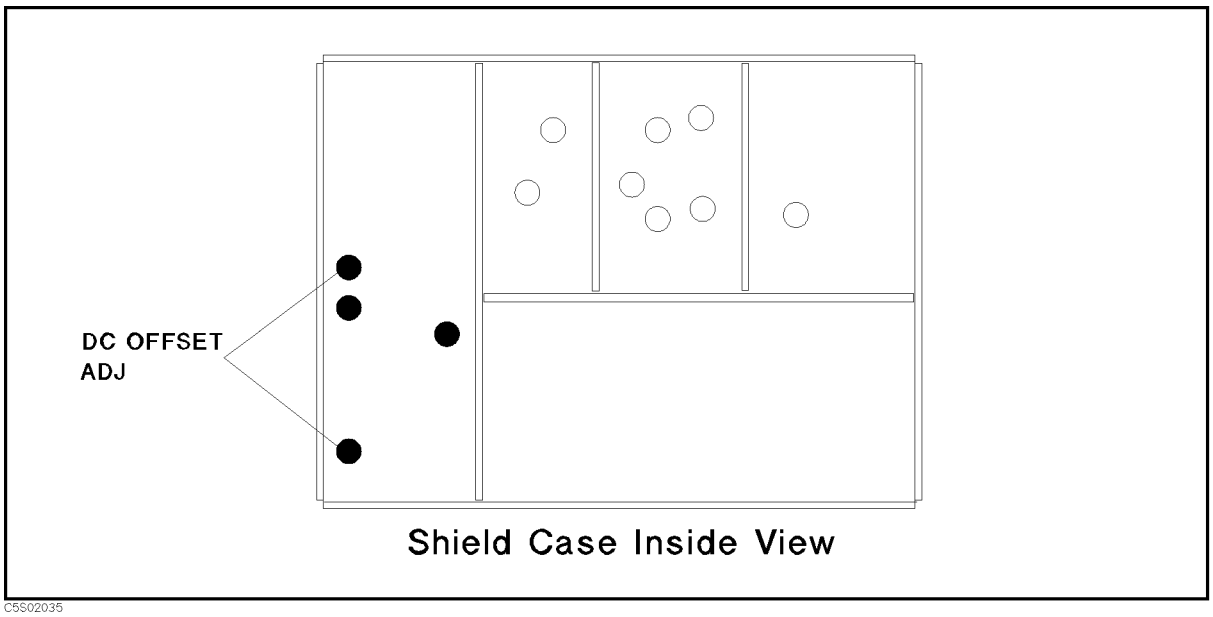


Figure 2-13. Plug Locations

6. Replace the shield case on the A6 board. Replace the A6 board into the slot.
7. Connect the equipment as shown in Figure 2-14 to monitor the sample hold output signal. Test pins locations are shown in Figure 2-15.

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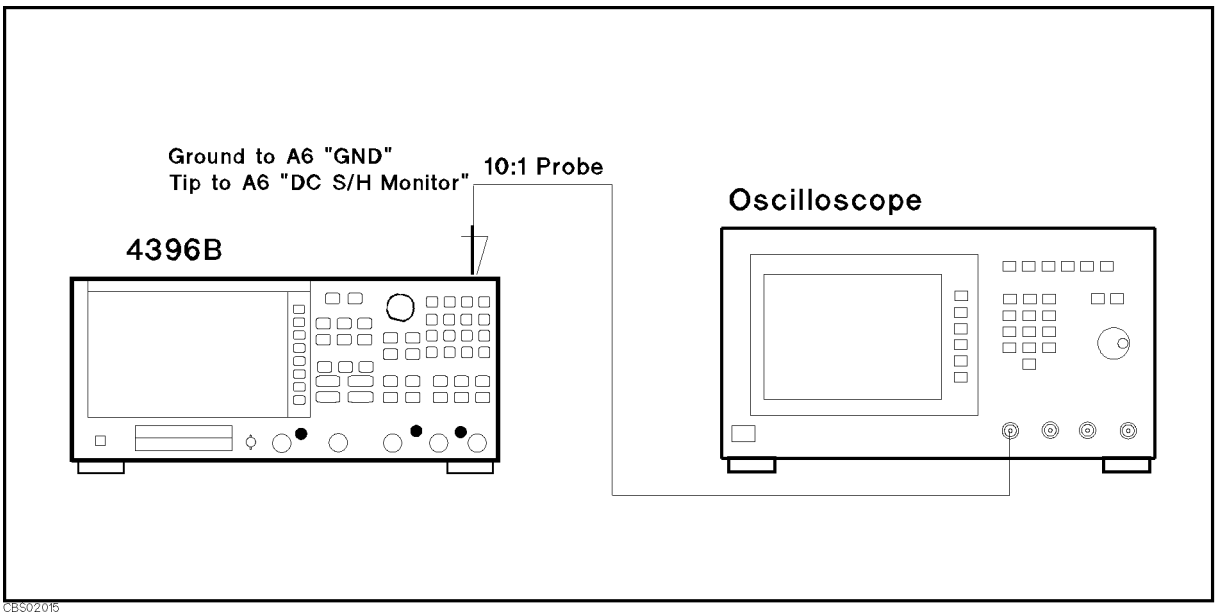


Figure 2-14. DC Offset and Hold Step Adjustment Setup

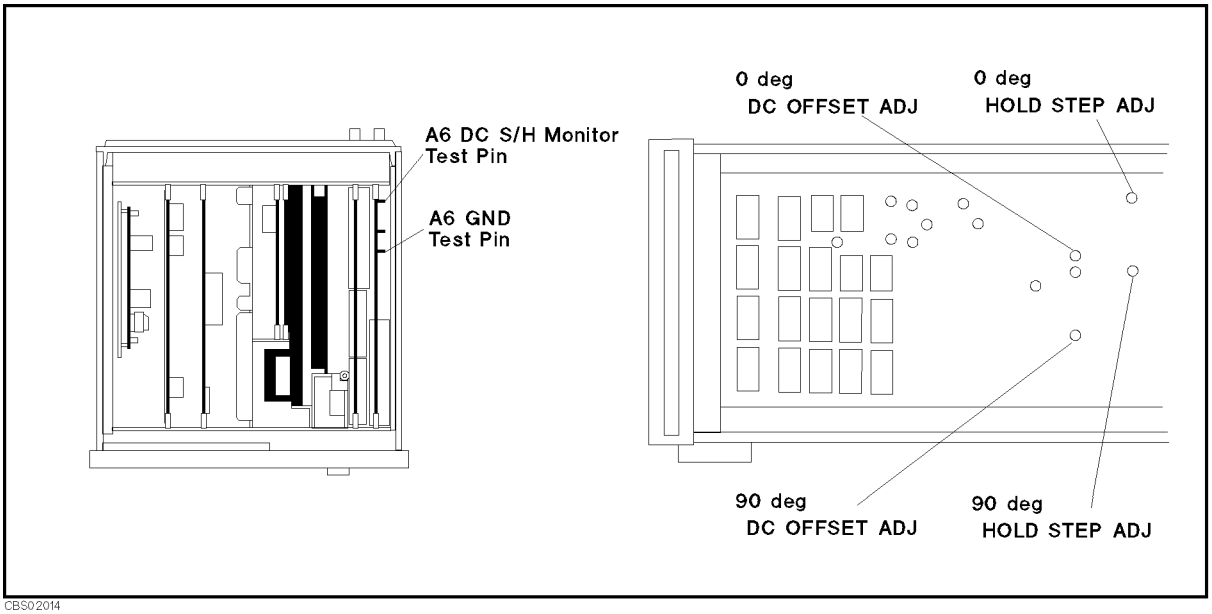


Figure 2-15. DC Offset and Hold Step Adjustment Locations

8. Set the oscilloscope as follows:

INPUT	Range:	400 mV
	Coupling:	DC, 1 MΩ
TIMBASE	Range:	50 μS

9. Turn the analyzer ON.
10. Press the following keys to execute adjust test No.41:

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(PRESET), (SYSTEM), SERVICE MENU, TESTS, (4), (1), (x1), EXECUTE TEST

11. Adjust "0 deg DC OFFSET ADJ" until the oscilloscope waveform's longer step voltage is within 0 ± 25 mV as shown in Figure 2-16. The adjustment location is shown in Figure 2-15.

Note If the waveform doesn't appear on the oscilloscope display, change the oscilloscope range setting to 4 V to adjust coarsely.

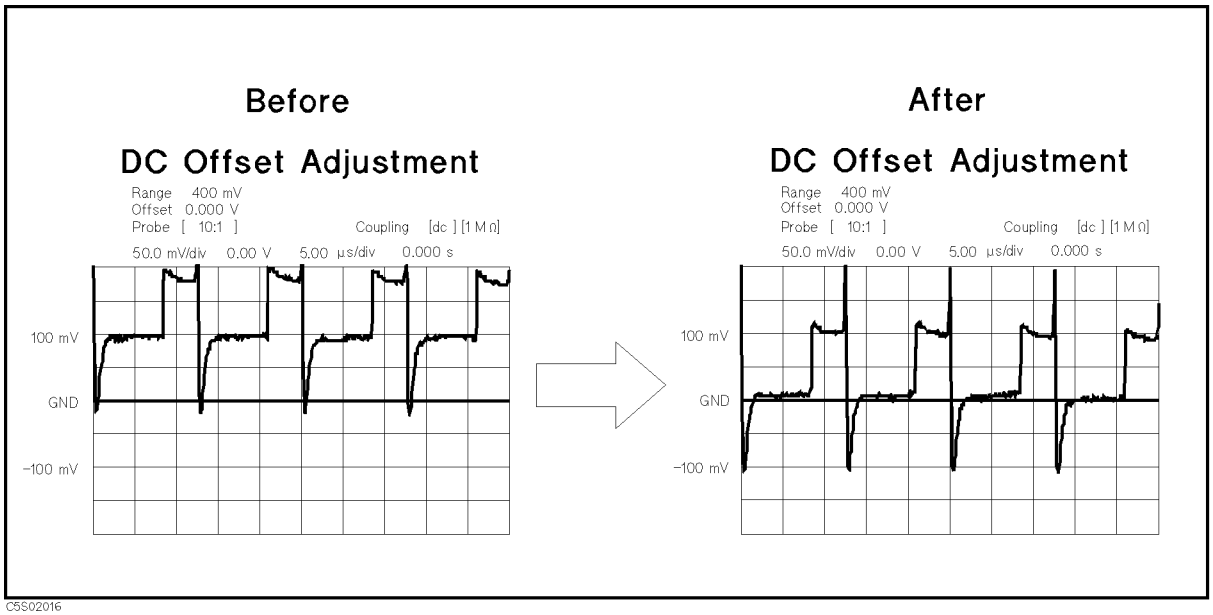


Figure 2-16. DC Offset Adjustment Waveform

12. Adjust "0 deg HOLD STEP ADJ" until the voltage difference between the longer step and shorter step is smaller than 50 mV, as shown in Figure 2-17. The adjustment location is shown in Figure 2-15.

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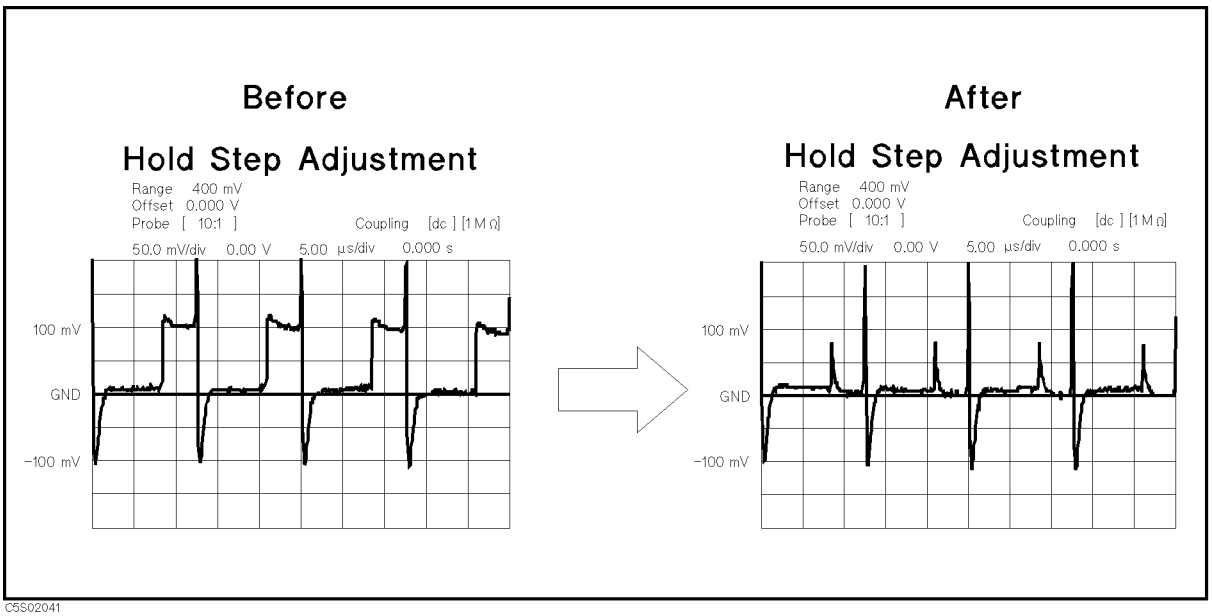


Figure 2-17. Hold Step Adjustment Waveform

13. Press CONT to proceed to the adjustments for 90 °.
14. Adjust "90 deg HOLD STEP ADJ" and "90 deg DC OFFSET ADJ" the same as the 0 deg adjustments.
15. Press CONT to finish the adjustment.

Note

Steps 16 to 19 replace the plugs into the "DC OFFSET ADJ" holes. If you are going to do the 0°/90° tracking adjustment, skip these steps.

16. Turn the analyzer OFF.
17. Pull the A6 board out. Place the board on the analyzer with the component side facing upward.
18. Replace the plugs into the "DC OFFSET ADJ" holes see Figure 2-18.

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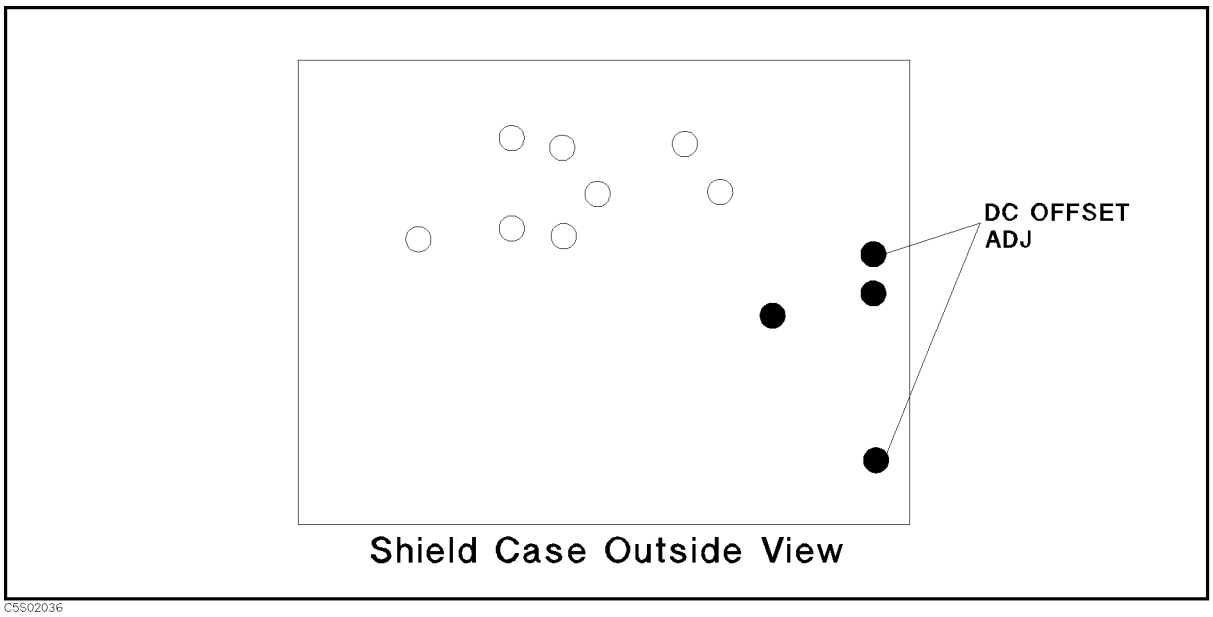


Figure 2-18. Plug Locations

19. Replace the A6 board into the slot.

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0°/90° Tracking Adjustment

The purpose of this procedure is to minimize the difference between the third IF 0° measurement circuit and 90° measurement circuit.

Required Equipment

N(m)-BNC(f) adapter ..... PN 1250-1476
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Turn the analyzer OFF.
2. To gain access to the adjustment components, remove the side panel on the control keys side.

Note



Steps 3 to 6 pull the plugs that block the "TRACKING ADJ" holes out. If these plugs are already out, skip these steps.

3. Pull the A6 board out. Place the board on the analyzer with the component side facing upward.
4. Remove the shield case from the board.
5. Pull the plugs that block the "TRACKING ADJ" holes (see Figure 2-19).

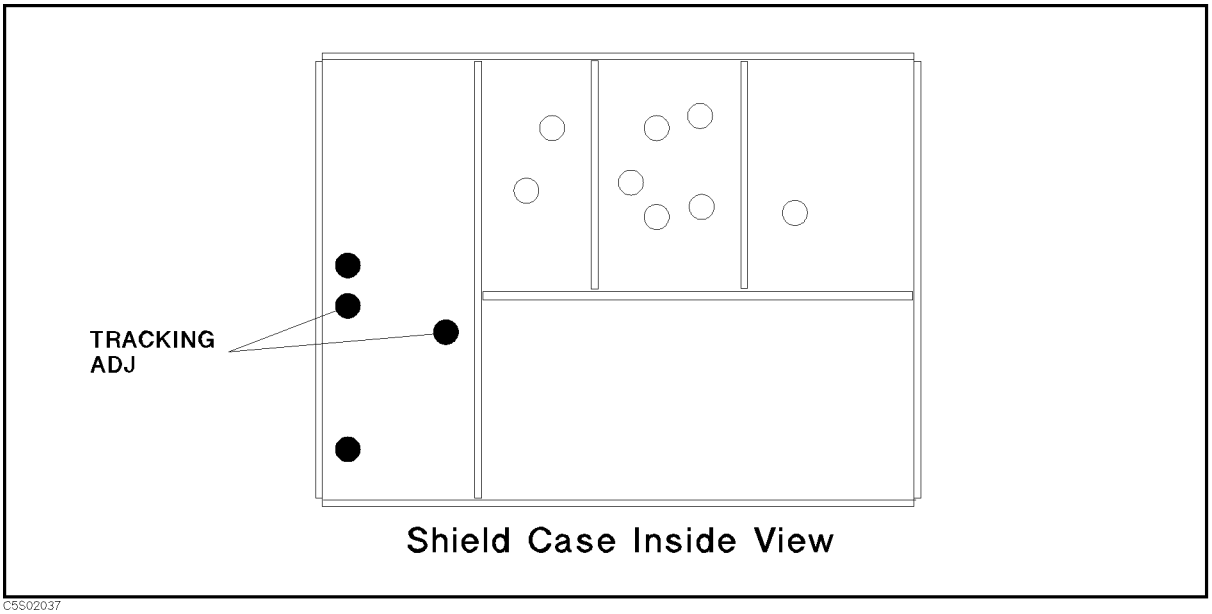


Figure 2-19. Plug Locations

6. Replace the shield case on the A6 board. Replace the A6 board into the slot.
7. Turn the analyzer ON.
8. Connect the equipment as shown in Figure 2-20

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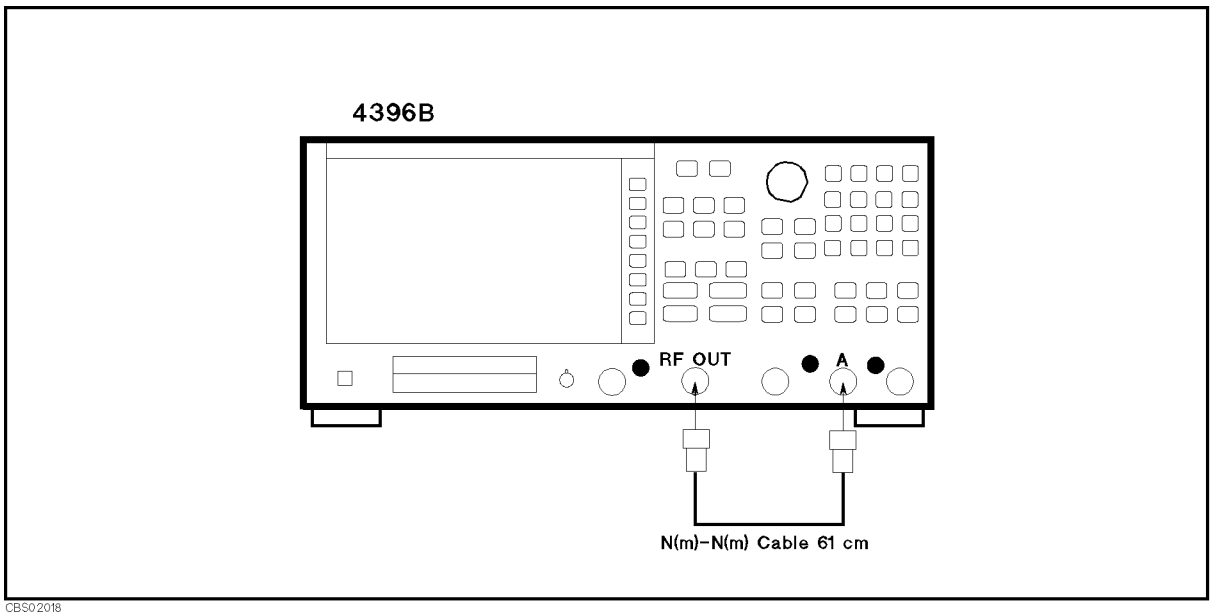


Figure 2-20. 0°/90° Tracking Adjustment Setup

9. Press the following keys to execute adjust test No.42:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (4), (2), (x1), EXECUTE TEST

10. Adjust "PHASE" and "GAIN" of "0/90 deg TRACKING ADJ" until the analyzer's marker reading of magnitude is smaller than 0.1 U. (The smallest circle of the analyzer display shows the adjustments limit.) Adjustment locations are shown in Figure 2-21.

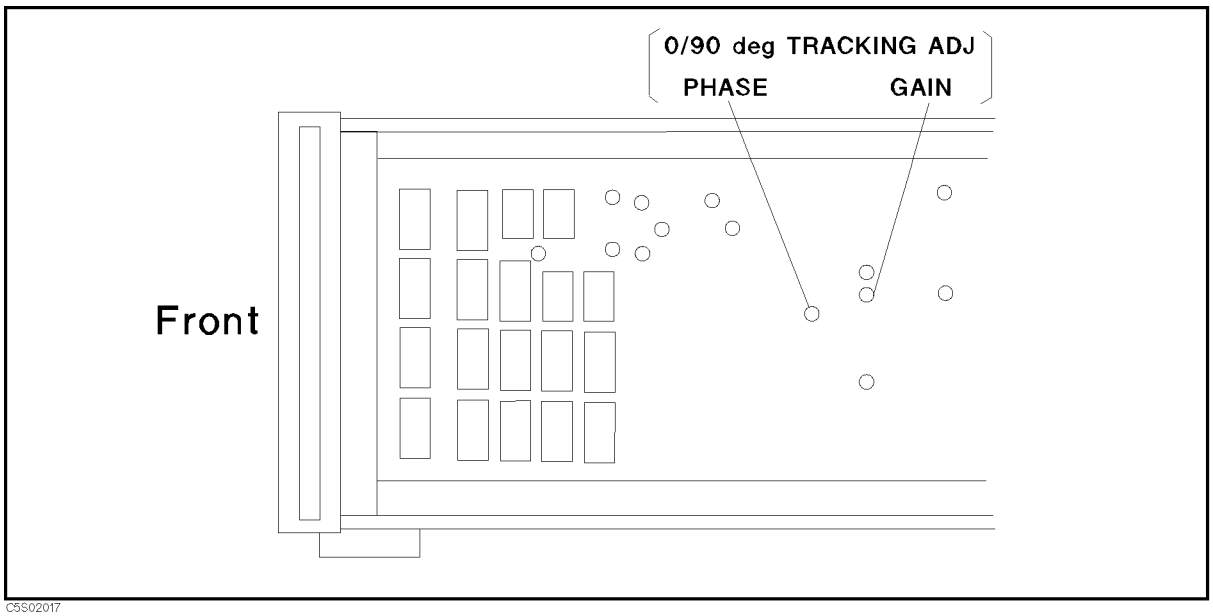


Figure 2-21. 0°/90° Tracking Adjustment Locations

11. Press CONT to finish the adjustment.

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12. Turn the analyzer OFF.
13. Pull the A6 board out. Place the board on the analyzer with the component side facing upward.
14. Replace the plugs into the “TRACKING ADJ” holes (see Figure 2-22). If the plugs for the “DC OFFSET ADJ” are out, replace the plugs.

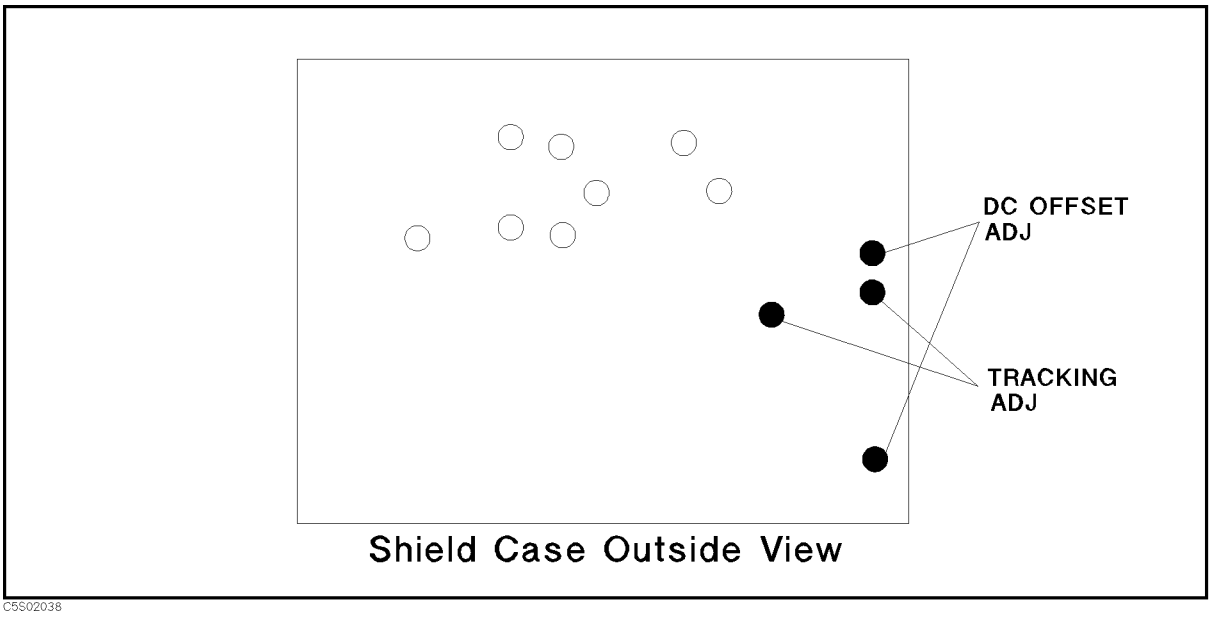


Figure 2-22. Plug Locations

15. Replace the A6 board into the slot.

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Band Pass Filters Adjustments

The purpose of this procedure is to optimize the 1 MHz and 3 MHz Band Pass Filters.

Required Equipment

N(m)-BNC(f) adapter ..... PN 1250-1476
BNC cable, 61 cm ..... PN 8120-1839

Procedure

3 MHz Band Pass Filter Adjustment

1. Turn the analyzer OFF.
2. To gain access to the adjustment components, remove the side panel on the control keys side.
3. Connect the equipment as shown in Figure 2-23

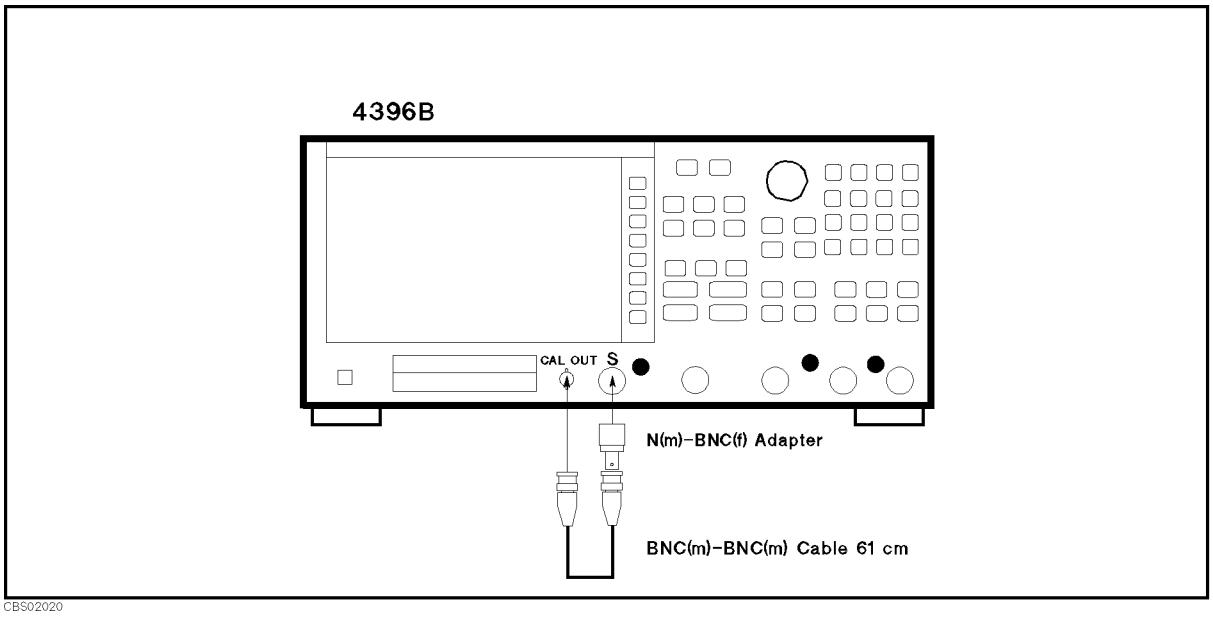


Figure 2-23. Band Pass Filters Adjustments Setup

4. Turn the analyzer ON.
5. Press the following keys to execute adjust test No.46:

   [PRESET], [SYSTEM], SERVICE MENU, TESTS, [4], [6], [x1], EXECUTE TEST

6. Adjust "BW"s of "3 MHz BPF ADJ" until the analyzer measurement trace is within the limits and "PASS" is displayed. The adjustment locations are shown in Figure 2-24.

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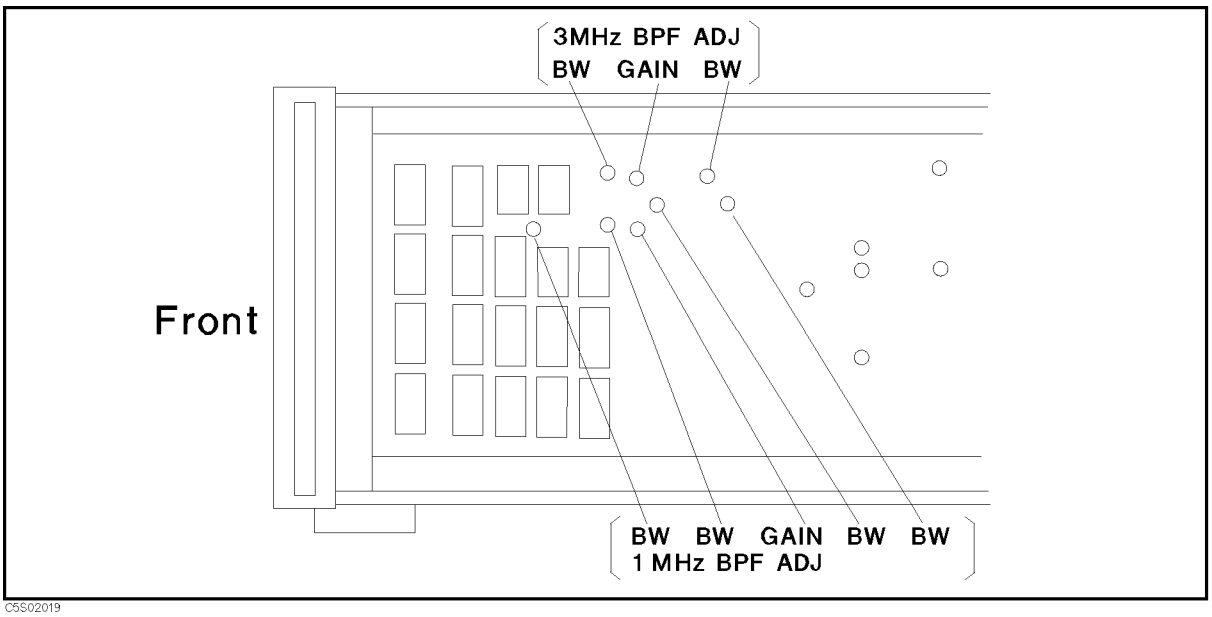


Figure 2-24. Band Pass Filters Adjustment Locations

7. Press CONT to continue the 3 MHz band pass filter adjustment.
8. Adjust "BW"s of the "3 MHz BPF ADJ" until the analyzer readings of "BW" (– 3 dB band width) and marker frequency meet the following requirements and "PASS" is displayed.

   BW 3 MHz ± 0.27 MHz
   Marker Frequency 20 MHz ± 0.18 MHz

9. Press CONT to continue the 3 MHz band pass filter adjustment.
10. Adjust "GAIN" of "3 MHz BPF ADJ" until the analyzer reading of marker magnitude is between −1 ± 0.1 dBm and "PASS" is displayed. The adjustment location is shown in Figure 2-24.
11. Press CONT to finish the 3 MHz band pass filter adjustment.

1 MHz BPF Band Width Adjustment

12. Press the following keys to execute adjust test No.47:

    PRESET, SYSTEM, SERVICE MENU, TESTS, 4, 7, x1, EXECUTE TEST

13. Adjust "BW"s of "1 MHz BPF ADJ" until the analyzer measurement trace is within the limits and "PASS" is displayed. The adjustment locations are shown in Figure 2-24.
14. Press CONT to continue the 1 MHz band pass filter adjustment.
15. Adjust "BW"s of the "1 MHz BPF ADJ" until the analyzer readings of "BW" (– 3 dB band width) and marker frequency meet the following requirements and "PASS" is displayed.

    BW 1 MHz ± 0.12 MHz
    Marker Frequency 20 MHz ± 0.06 MHz

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16. Press CONT to continue the 1 MHz band pass filter adjustment.
17. Adjust “GAIN” of “1 MHz BPF ADJ” until the analyzer reading of marker magnitude is between -1 ± 0.1 dBm and “PASS” is displayed. The adjustment location is shown in Figure 2-24.
18. Press CONT to finish the 1 MHz band pass filter adjustment.

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Final Gain Adjustment

The purpose of this procedure is to adjust the total gain of the receiver.

Required Equipment

Signal Generator	3335A
BNC cable, 61 cm (2 required)	PN 8120-1839
N(m)-BNC(f) adapter	PN 1250-1476

Procedure

1. Connect the equipment as shown in Figure 2-25.

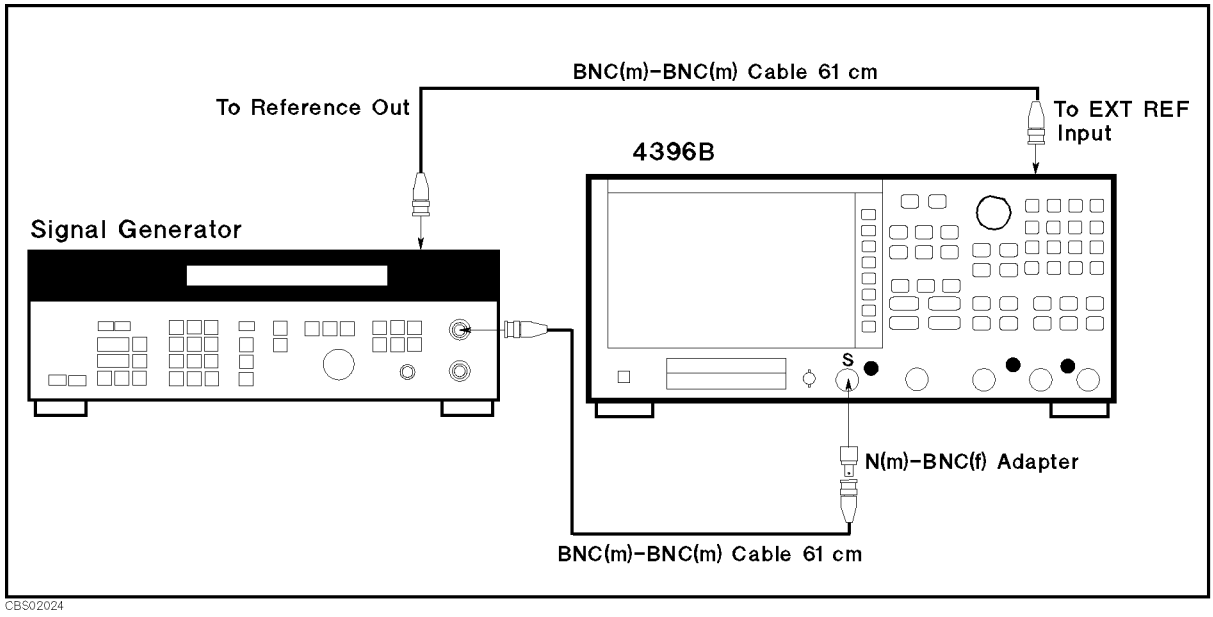


Figure 2-25. Final Gain Adjustment Setup

2. Press the following keys to execute adjust test No.43:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (4), (3), (x1), EXECUTE TEST

3. Set the signal generator as follows:

   Frequency 20 MHz
   Amplitude 0 dBm

4. Adjust "FINAL GAIN ADJ" until the analyzer reading is between the limit lines and PASS is displayed. The adjustment location is shown in Figure 2-26.

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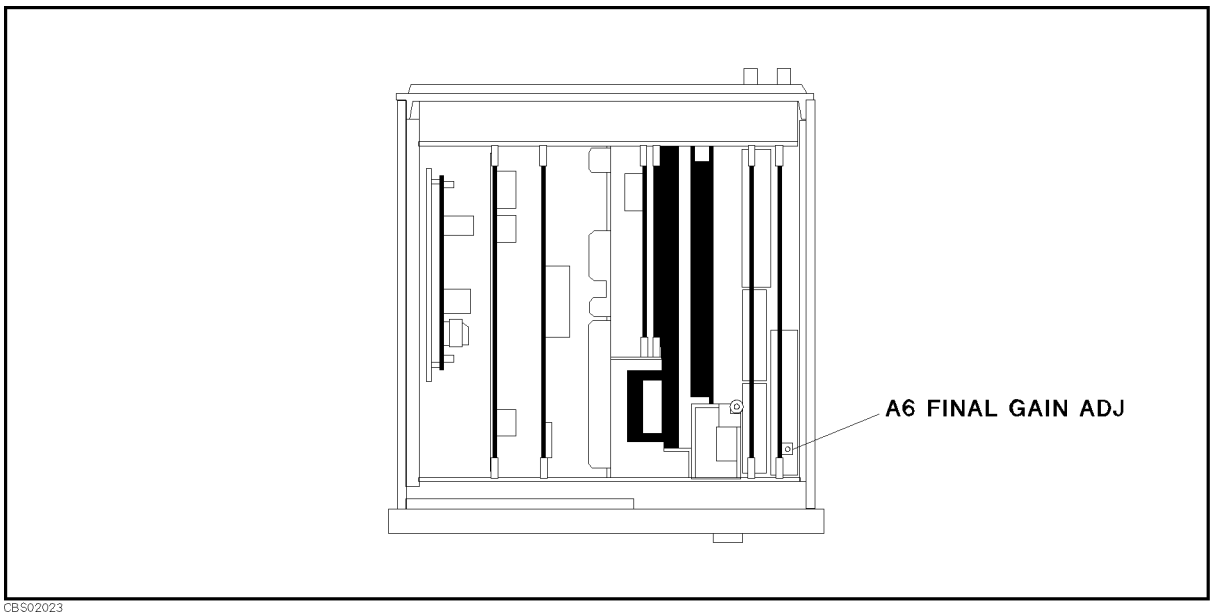


Figure 2-26. Final Gain Adjustment Location

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Source Mixer Local Leakage Adjustment

The purpose of this procedure is to minimize the source mixer local leakage.

Required Equipment

Signal Generator 1	8642B
Signal Generator 2	8663A
N(m)-BNC(f) adapter	PN 1250-1476
BNC(f)-SMA(m) adapter	PN 1250-1548
Tee BNC(m)-(f)-(f) adapter	PN 1250-0781
SMA(m)-SMA(f) right angle adapter	PN 1250-1741
BNC cable, 61 cm	PN 8120-1839
BNC cable, 122 cm (2 required)	PN 8120-1840
Type-N Cable, 61 cm (2 required)	11500B or part of 11851B

Procedure

1. Turn the analyzer OFF.
2. Remove the "C" cable from the A3A3 first local input connector. The connector location is shown in Figure 2-27.

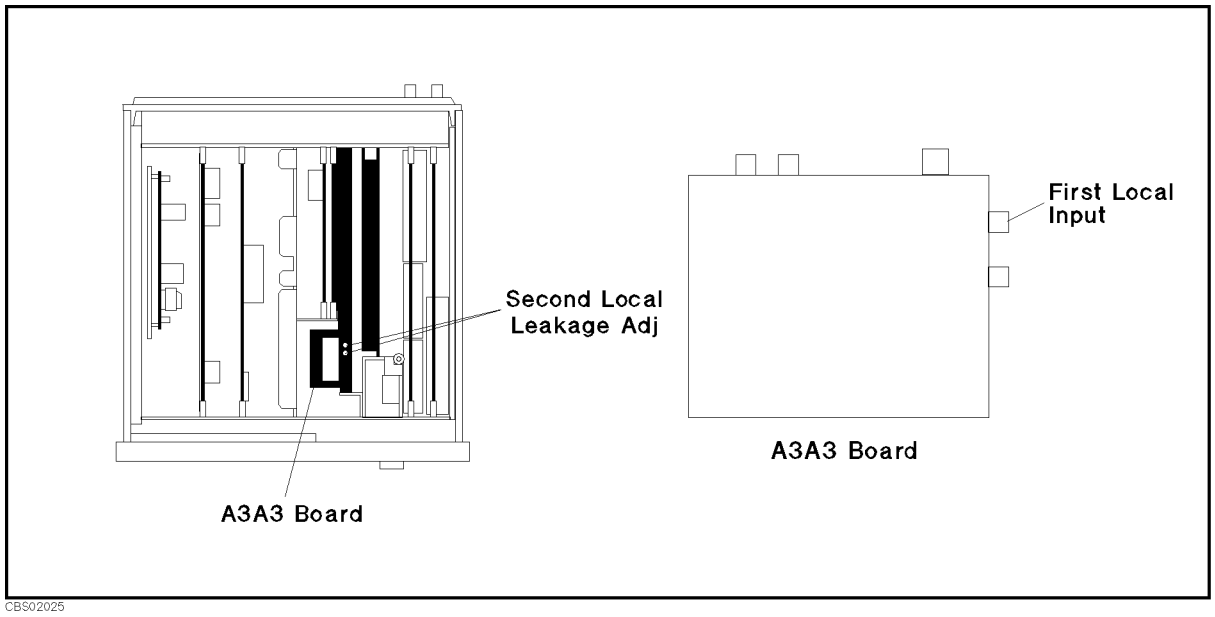


Figure 2-27. Second Local Leakage Adjustment Location

3. Connect the equipment as shown in Figure 2-28.

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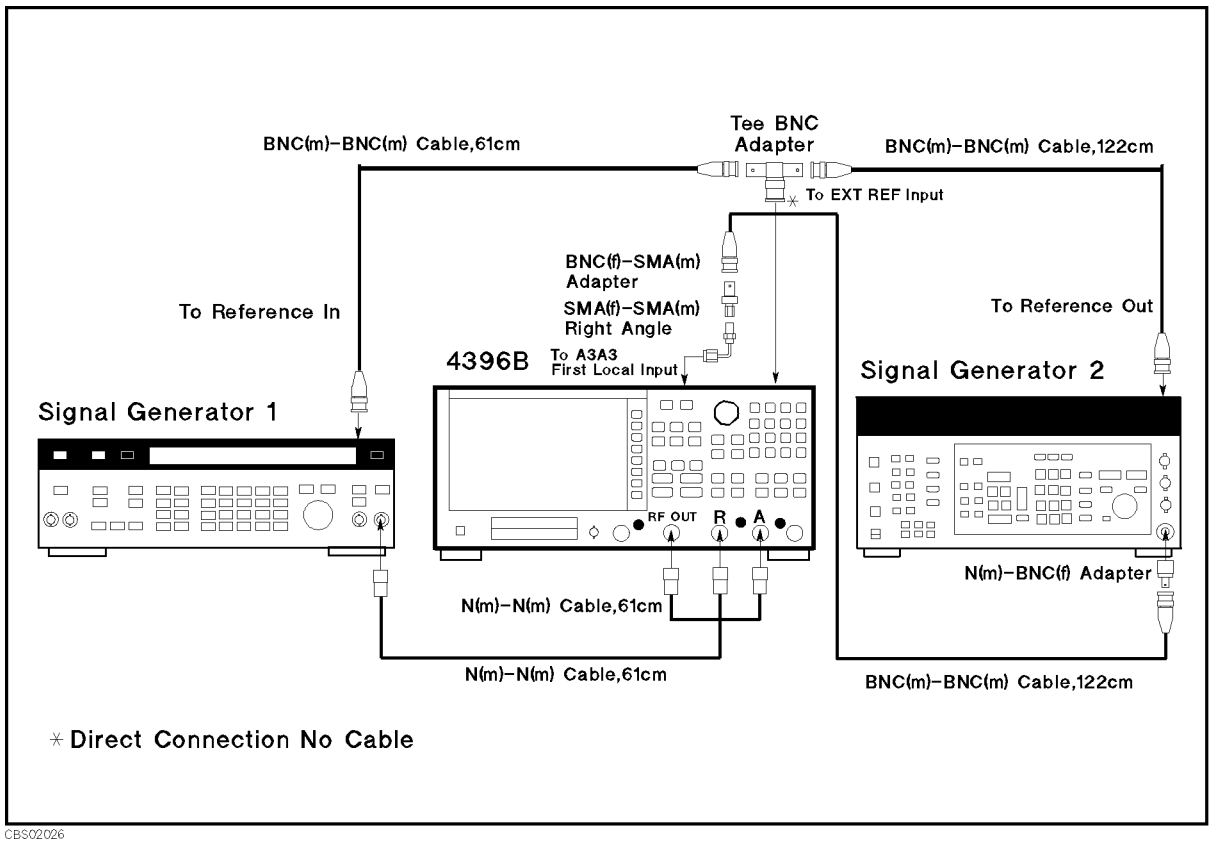


Figure 2-28. Second Local Leakage Adjustment Setup

4. Turn the analyzer ON.
5. Press the following keys to execute adjust test No.45:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (4), (5), (x1), EXECUTE TEST

6. Set the signal generators as follows:

	Signal Generator 1 Setting	Signal Generator 2 Setting
Frequency	100 MHz	2.18 GHz
Amplitude	0 dBm	–4 dBm

7. Adjust second local leakage adjustments until the analyzer's marker reading of magnitude is smaller than 5 mU and "PASS" is displayed. (The smallest circle of the analyzer display shows the adjustments limit.) The adjustment locations are shown in Figure 2-27.
8. Reconnect the "C" cable to the A3A3 first local input connector.

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RF OUT Level Correction Constants

The purpose of this procedure is to obtain the correction constants that correct the RF OUT signal linearity and flatness.

Required Equipment

Power Meter 436A
Power Sensor 8482A

Procedure

1. Run the adjustment program and display the main menu (see "Updating Correction Constants using the Adjustments Program").
2. Choose the RF OUT Level Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 2-29 shows the equipment setup for the Correction Constants.

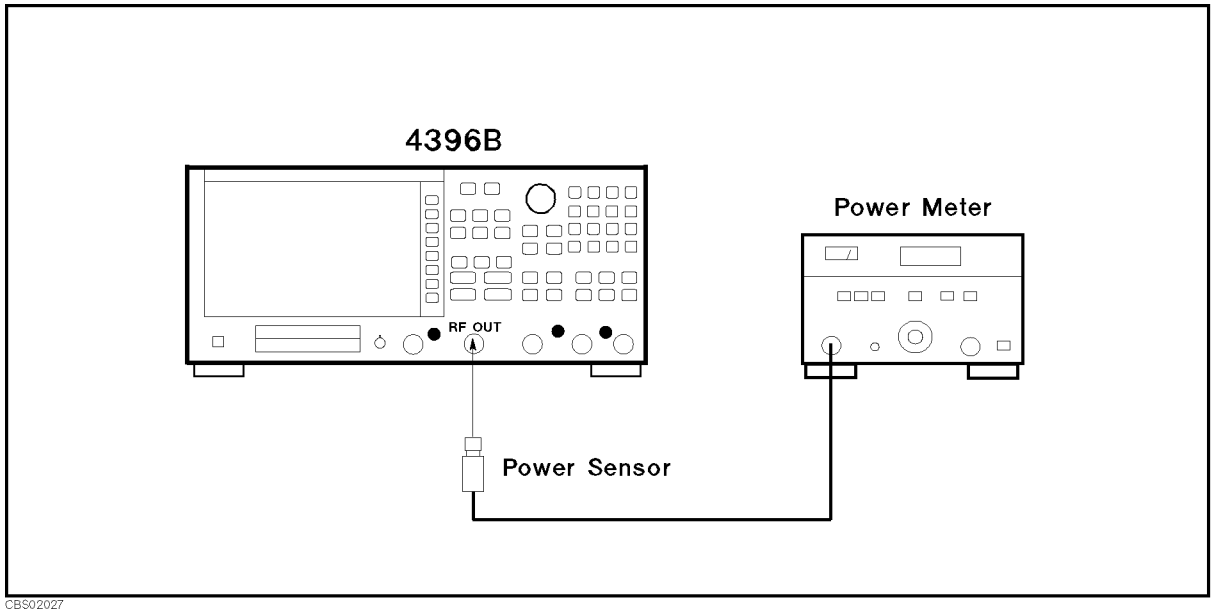


Figure 2-29. RF OUT Level Correction Constants Setup

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Spectrum Analyzer Absolute Magnitude Correction Constants

The purpose of this procedure is to obtain the correction constants that correct the spectrum analyzer absolute magnitude measurement.

Required Equipment

Signal Generator	8663A
Power Meter	436A
Power Sensor	8482A
Two-Way Power Splitter	11667A
N(m)-N(m) adapter	PN 1250-1475
Type-N Cable, 61 cm	11500B or part of 11851B

Procedure

1. Run the adjustment program and display the main menu (see "Updating Correction Constants using the Adjustments Program").
2. Choose the SA Absolute Magnitude Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 2-30 shows the equipment setup for the Correction Constants.

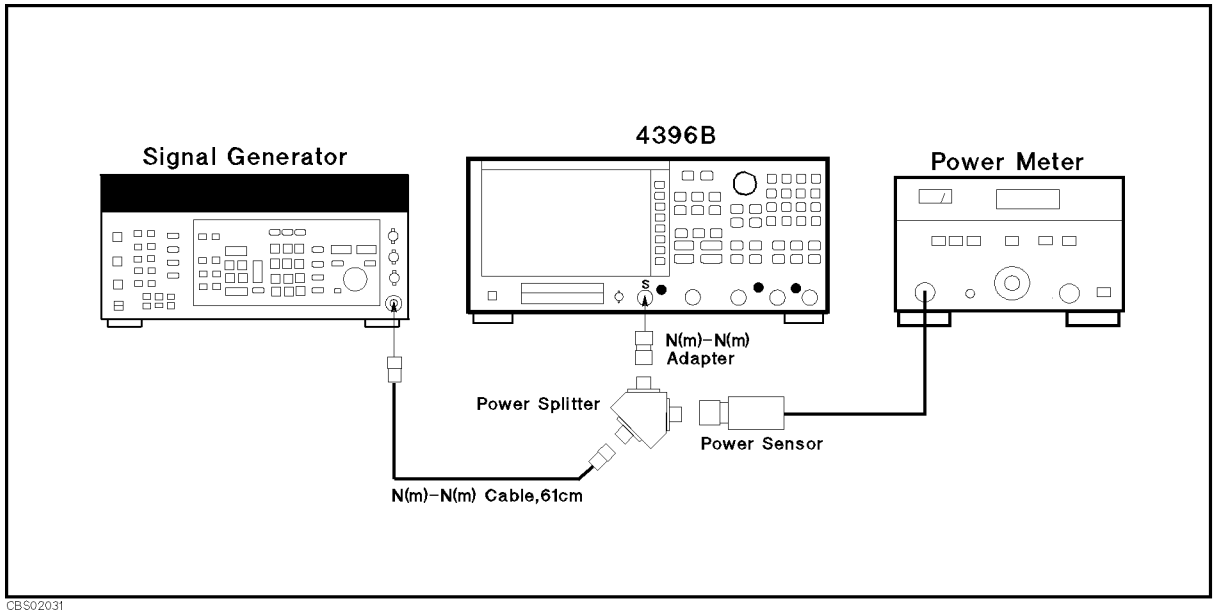


Figure 2-30. Spectrum Analyzer Absolute Magnitude Correction Constants Setup

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Network Analyzer Absolute Magnitude Correction Constants

The purpose of this procedure is to obtain the correction constants that correct the network analyzer absolute magnitude measurement.

Required Equipment

Signal Generator	8663A
Power Meter	436A
Power Sensor	8482A
Two-Way Power Splitter	11667A
N(m)-N(m) adapter	PN 1250-1475
Type-N Cable, 61 cm	11500B or part of 11851B

Procedure

1. Run the adjustment program and display the main menu (see "Updating Correction Constants using the Adjustments Program").
2. Choose the NA Absolute Magnitude Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 2-31 shows the equipment setup for the Correction Constants.

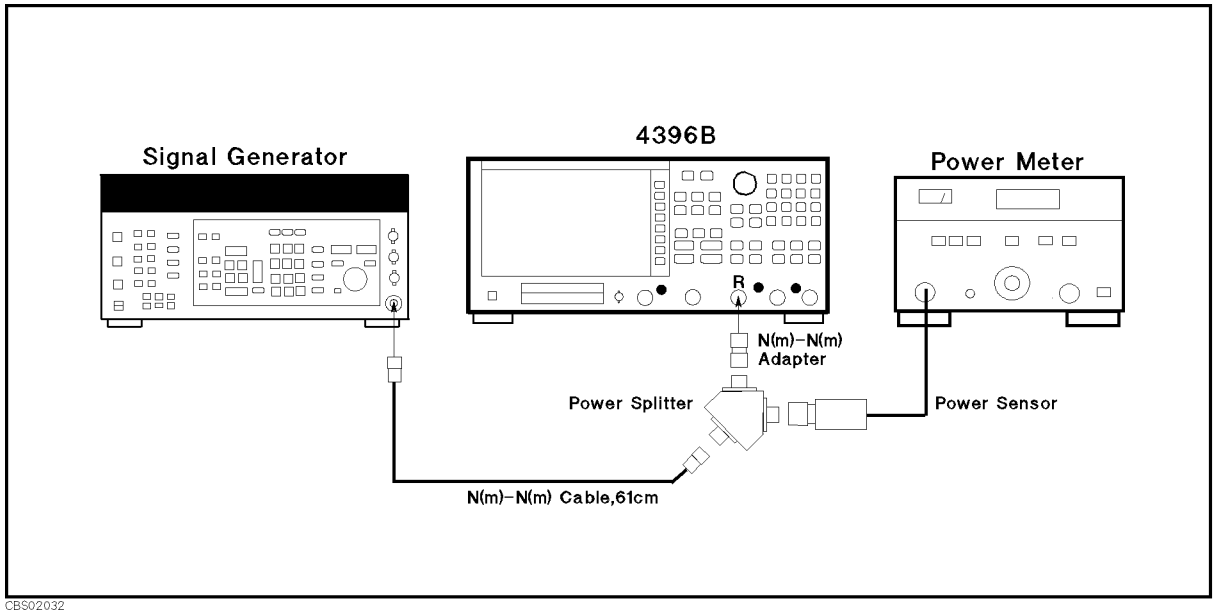


Figure 2-31. Network Analyzer Absolute Magnitude Correction Constants Setup

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Crystal Filter Correction Constants

The purpose of this procedure is to obtain the correction constants that correct the crystal filter frequency response.

Required Equipment

Signal Generator 8663A
Type-N Cable, 61 cm ..... 11500B or part of 11851B

Procedure

1. Run the adjustment program and display the main menu (see "Updating Correction Constants using the Adjustments Program").
2. Choose the Crystal Filter Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 2-32 shows the equipment setup for the Correction Constants.

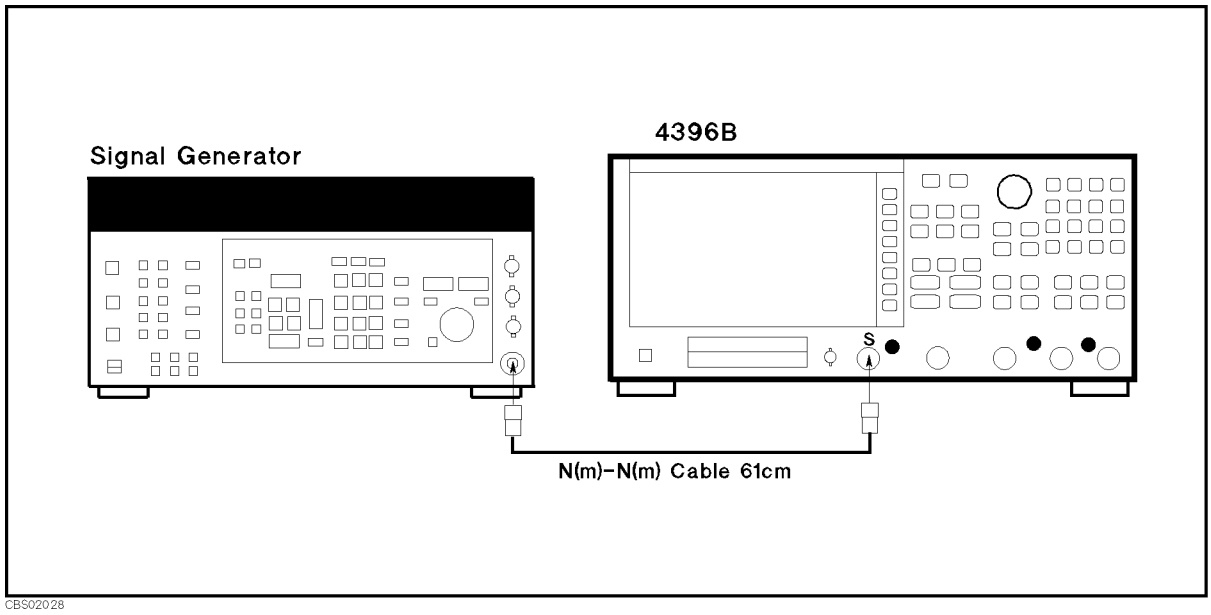


Figure 2-32. Crystal Filter Correction Constants Setup

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IF Gain Errors Correction Constants

The purpose of this procedure is to obtain the correction constants that correct the IF gain changing errors for network analysis and spectrum analysis.

Required Equipment

Signal Generator 8663A
Type-N Cable, 61 cm ..... 11500B or part of 11851B

Procedure

1. Run the adjustment program and display the main menu (see "Updating Correction Constants using the Adjustments Program").
2. Choose the IF Gain Errors Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 2-33 and Figure 2-34 show the equipment setups for the Correction Constants.

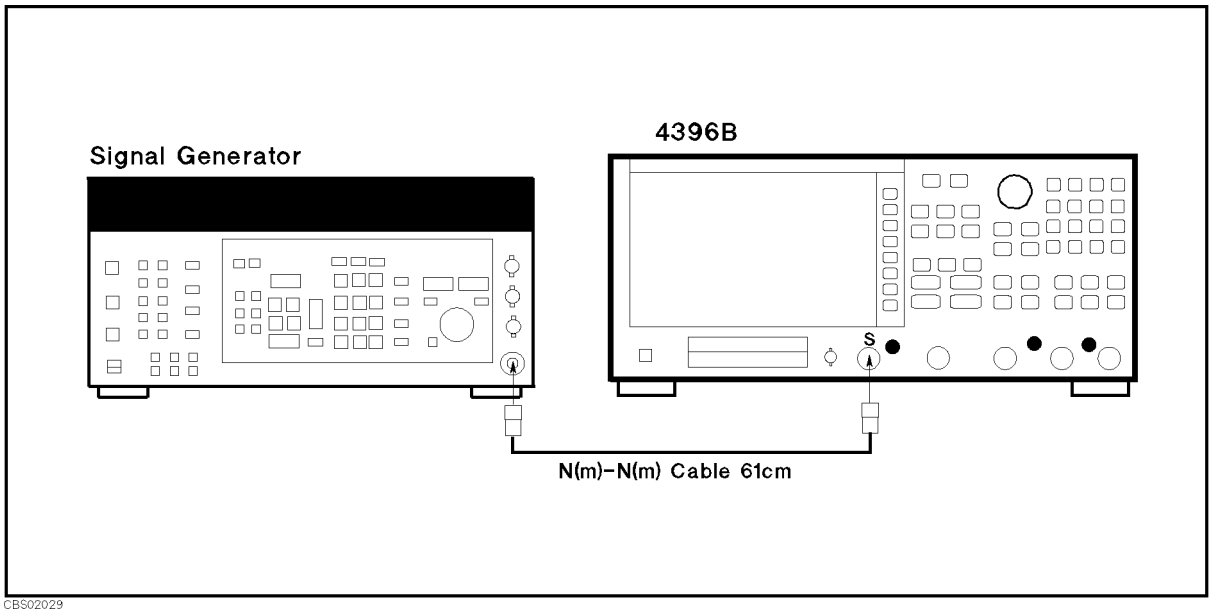


Figure 2-33. IF Gain Errors Correction Constants Setup 1

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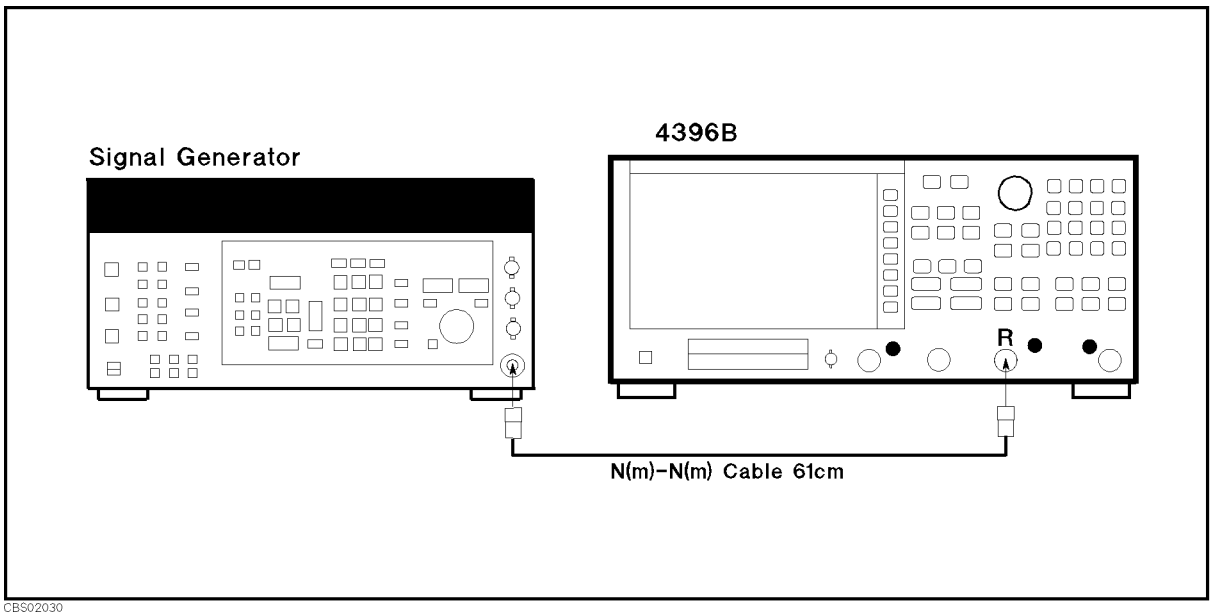


Figure 2-34. IF Gain Errors Correction Constants Setup 2

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Network Analyzer Magnitude Ratio/Phase Correction Constants

The purpose of this procedure is to obtain the correction constants that correct the network analyzer magnitude ratio and phase measurement for A/R and B/R.

Required Equipment

Two-Way Power Splitter 11667A
N(m)-N(m) adapter ..... PN 1250-1475
Type-N Cable, 61 cm (2 required) ..... 11500B or part of 11851B

Procedure

1. Run the adjustment program and display the main menu (see "Updating Correction Constants using the Adjustments Program").
2. Choose the NA Magnitude Ratio/Phase Correction Constants.
3. Follow the adjustment program instructions to update the correction constants. Figure 2-35 and Figure 2-36 show the equipment setups for the Correction Constants. Two measurements are done for each of A/R and B/R, changing the power splitter connection, to correct the difference between the power splitter arms.

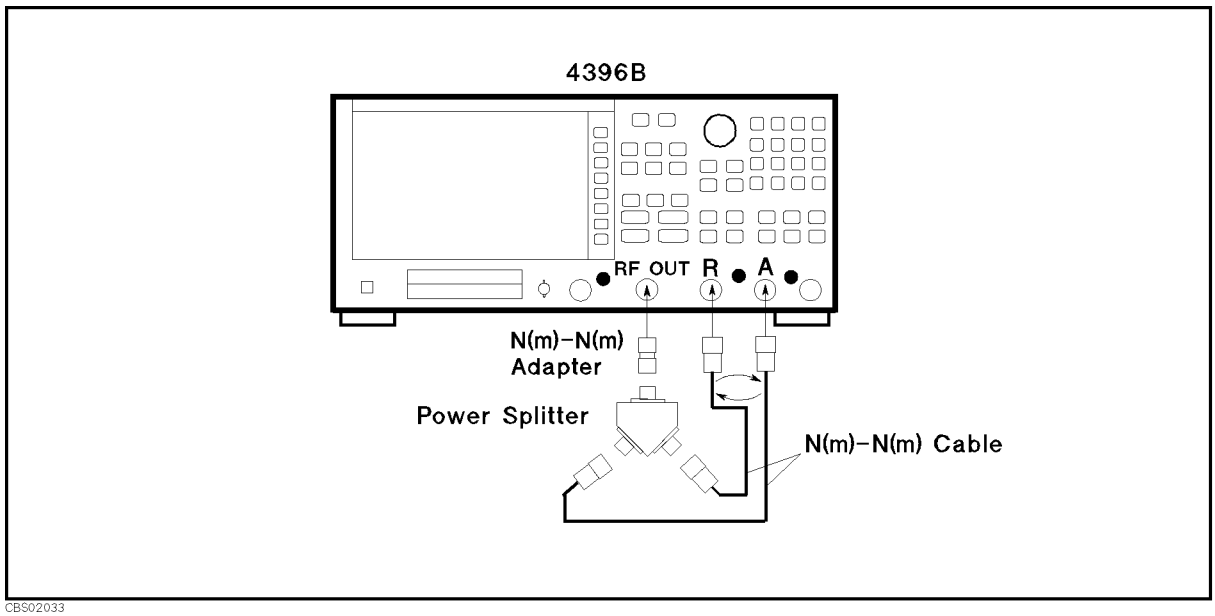


Figure 2-35. Network Analyzer Magnitude Ratio/Phase Correction Constants Setup 1

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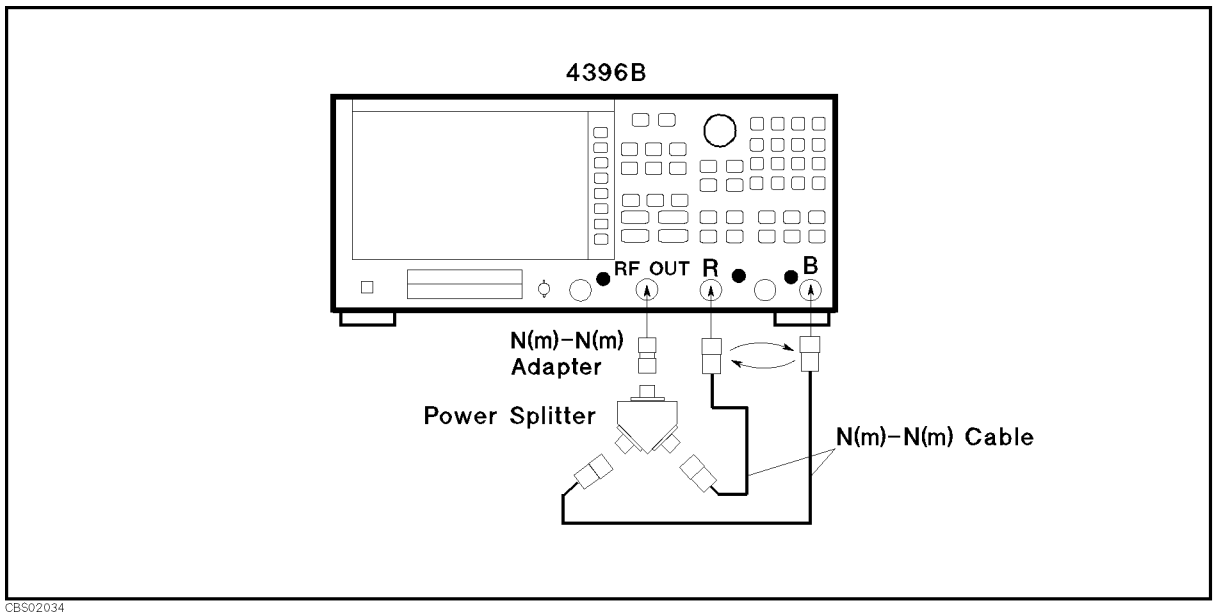


Figure 2-36. Network Analyzer Magnitude Ratio/Phase Correction Constants Setup 2

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10 MHz Reference Oscillator Frequency Adjustment (Option 1D5 Only)

The purpose of this procedure is to adjust the 10 MHz high stability reference oscillator (Option 1D5) frequency.

Required Equipment

Frequency Counter	5343A
Frequency Standard	5061B
APC3.5(m)-APC3.5(f) adapter	PN 1250-1866
BNC(f)-SMA(f) adapter	PN 1250-0562
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 61 cm (3 required)	PN 8120-1839

Procedure

1. Turn the analyzer OFF.
2. Pull the A60 assembly out. Place it on the analyzer with the bracket facing upward. The A60 location is shown in Figure 2-37.

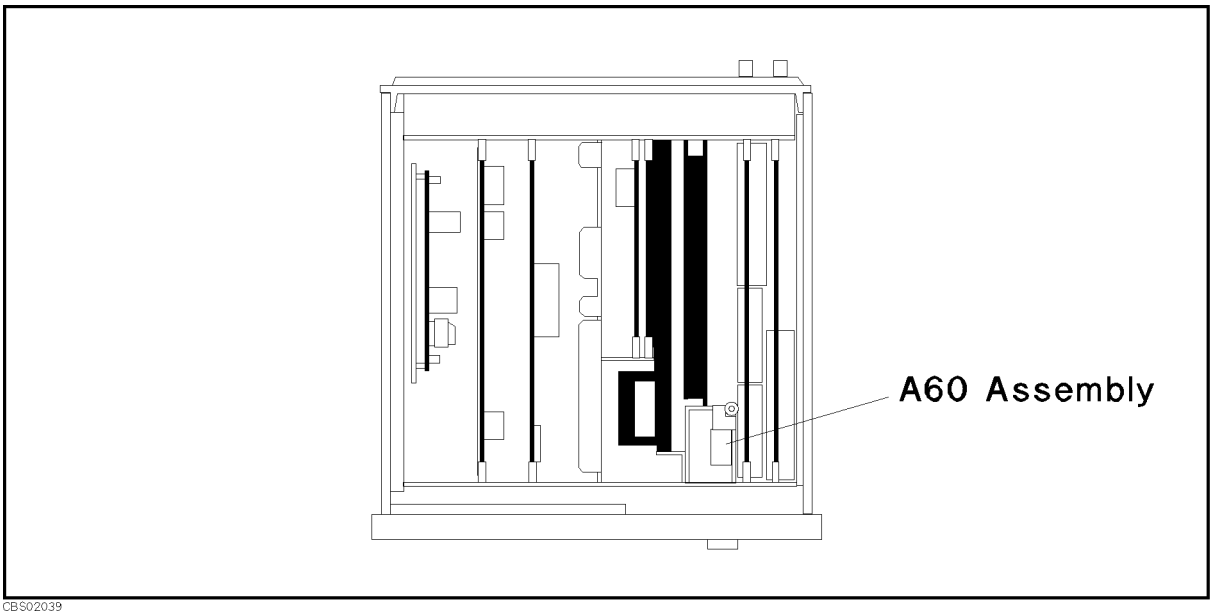


Figure 2-37. 10 MHz Reference Oscillator Frequency Adjustment Location

Note

The analyzer must be ON continuously for at least 24 hours immediately prior to the oscillator adjustment. This warm-up time allows both the temperature and frequency of the oscillator to stabilize. Failure to allow sufficient stabilization time could result in oscillator misadjustment.

3. Allow the analyzer to remain ON continuously for at least 24 hours to ensure that both the temperature and frequency of A60 can stabilize.
4. Connect the equipment as shown in Figure 2-38.

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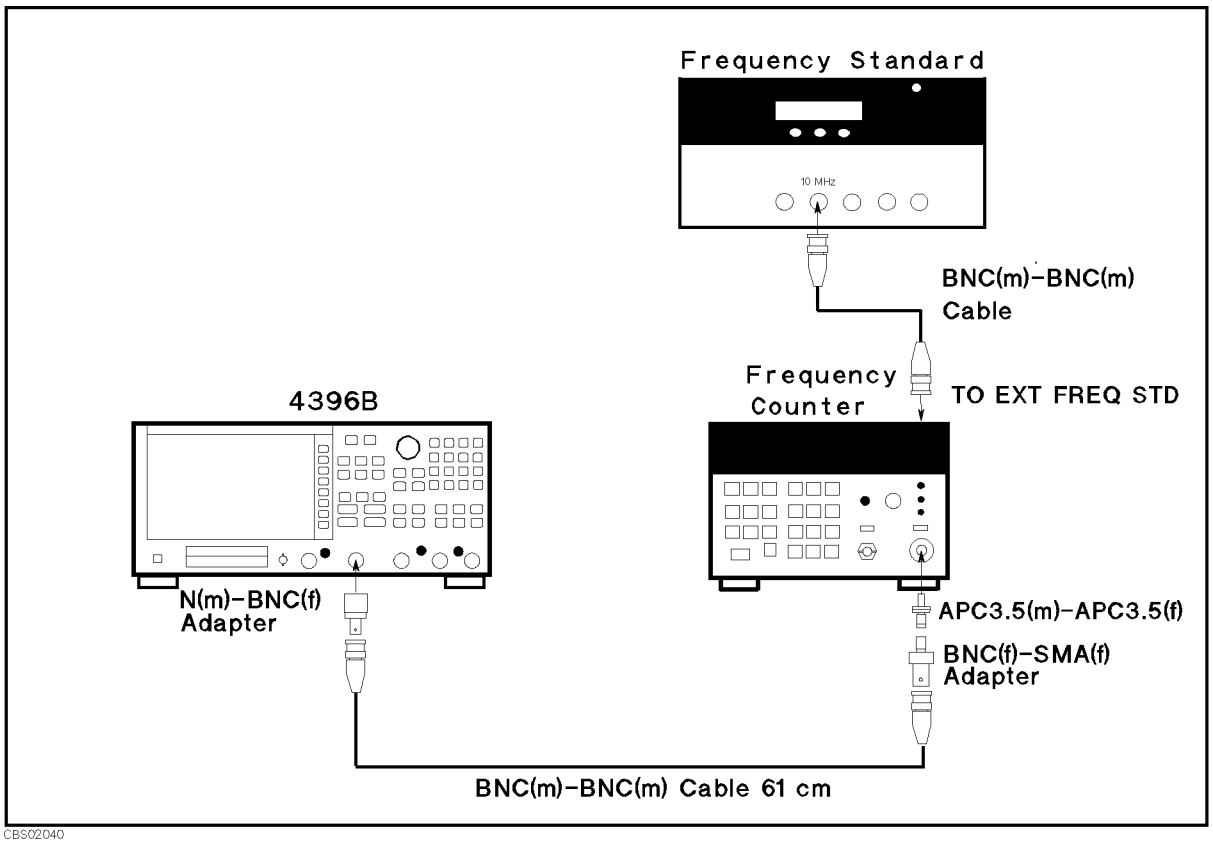


Figure 2-38. 10 MHz Reference Oscillator Frequency Adjustment Setup

5. Press (Preset) to initialize the analyzer. Then set the analyzer controls as follows:

Control Settings	Key Strokes
Analyzer Type: Network	(Meas), ANALYZER TYPE, NETWORK ANALYZER
Center Frequency: 1.8 GHz	(Center), (1), (.), (8), (G/n)
Frequency Span: 0 Hz	(Span), ZERO SPAN
Source Power: −20 dBm	(Source), POWER, (−), (2), (0), (x1)

6. Set the frequency counter as follows:

   Input Impedance 50 Ω
   Frequency Range 500 MHz - 26.5 GHz

7. Remove the dust cap screw on the A60 assembly to gain access to the adjustment screw.
8. Adjust the A60 adjustment screw until the frequency counter reading is within 1.8 GHz ± 1 Hz.
9. Turn the analyzer OFF.
10. Replace the dust cap screw into the A60 assembly, and replace the A60 assembly into the slot.

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3

Troubleshooting

INTRODUCTION

This chapter describes overall troubleshooting summary and provides the procedure to determine whether the analyzer is faulty, or not. The procedure is performed first in the troubleshooting of this manual.

TROUBLESHOOTING SUMMARY

The troubleshooting strategy of this manual is based on a verification (rather than symptomatic) approach. This chapter's first step is to verify the operation of the analyzer alone, independent of accessories or system peripherals. Accessories are devices like test sets, power probes, power splitters, cables, and calibration kits. Peripherals are devices like computers, printers, and keyboards, for instance, and which typically use an GPIB connection and a line connection. This chapter also suggests remedies for system problems external to the analyzer.

This chapter identifies one or some faulty groups in the analyzer's five functional groups. Then refers the technician to the appropriate chapter. The five functional groups are power supply, digital control, source, receiver, and accessories. Descriptions of these groups are provided in the *Theory of Operation* chapter.

Isolate Faulty Group Troubleshooting , the next chapter, assumes that the fault is within one of two functional groups: source, receiver. *Isolate Faulty Group Troubleshooting* identifies the faulty group and refers the technician to the appropriate chapter. These first chapters, *Troubleshooting* and *Isolate Faulty Group Troubleshooting*, stress simple, straight forward procedures.

Figure 3-1 diagrams the troubleshooting organization.

Each of the five chapters following *Isolate Faulty Group Troubleshooting* verifies, one at a time, the assemblies within a group until the faulty assembly is identified. These five chapters employ more lengthy, complicated procedures.

Post-Repair Procedures, is the last chapter of the troubleshooting portion of the manual. *Post-Repair Procedures* is organized by assembly and notes what adjustment to perform and how to verify proper instrument operation following the replacement of an assembly.

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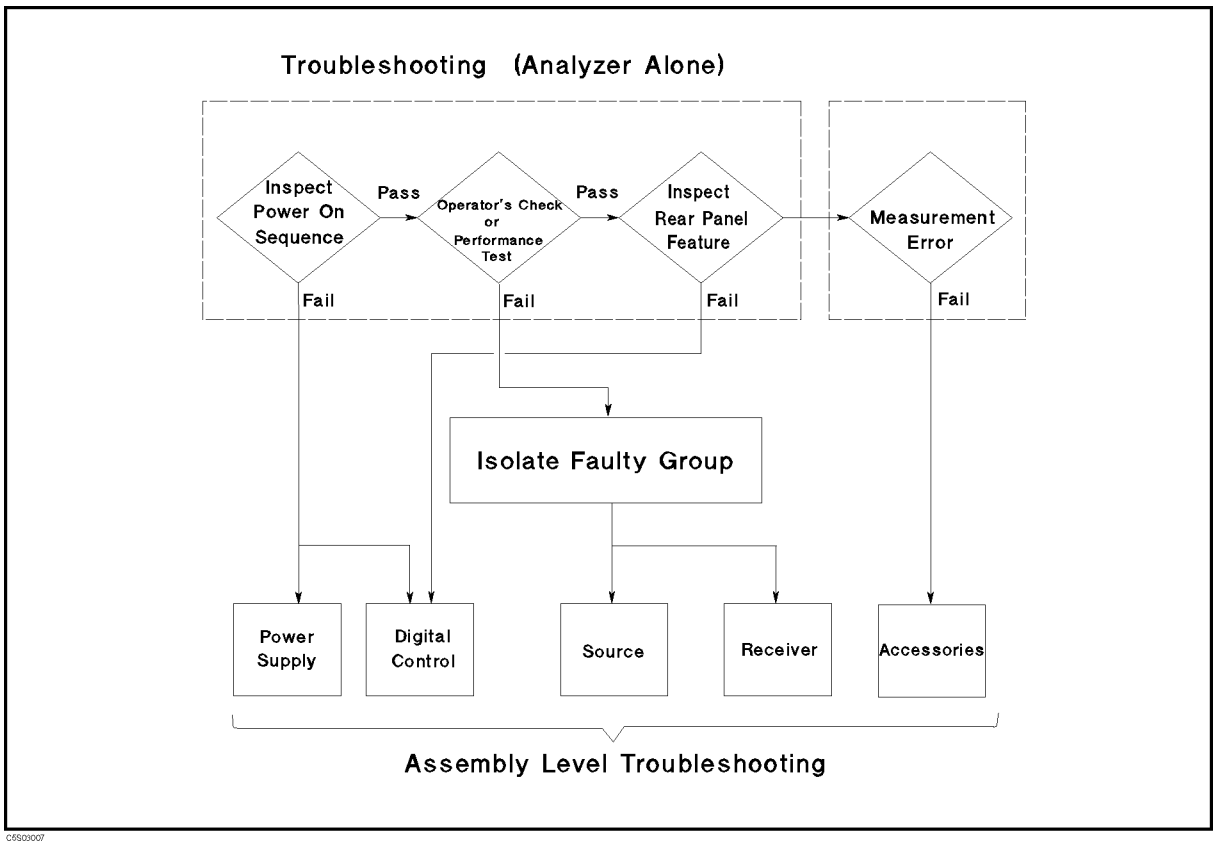


Figure 3-1. Troubleshooting Organization

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START HERE

A system failure can be caused by a problem in the analyzer and its accessories or out of the analyzer (in a peripheral or programming). To verify the operation of the analyzer alone, perform the following procedure.

1. Disconnect everything from the analyzer: All test set interconnect, GPIB cable, probe power, and RF cables.
2. Perform the *INSPECT THE POWER ON SEQUENCE* in this chapter.
3. Perform the *OPERATOR's CHECK* in this chapter.
4. Perform the *INSPECT THE REAR PANEL FEATURE* in this chapter.

If the analyzer has passed all of the checks in steps 2 through 4 but it still making incorrect measurements or unexpected operations, suspect the accessories. Accessories such as RF or interconnect cables, calibration and verification kit devices, test set can all induce system problems.

Configure the system as it is normally used and reconfirm the problem. Continue with the *Accessories Troubleshooting* chapter.

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INSPECT THE POWER ON SEQUENCE

Check the Fan

Turn the analyzer power on. Inspect the fan on the rear panel.

- The fan should be rotating and audible.

If case of unexpected results, check AC line power to the analyzer. Check the fuse (rating listed on the rear panel). Check the line voltage setting. For setting the line voltage, see the *Power Requirements* in Appendix C.

If the problem persists, continue with the *Power Supply Troubleshooting* chapter.

Check the Front Panel LEDs and Displays

Turn on the analyzer and watch for the following events in this order:

1. Beep is sounding.
2. The Ch 1 LED turns on and the analyzer displays Internal Test In Progress for several seconds.
3. The analyzer displays the graticule.

If case of unexpected results, continue with *Digital Control Troubleshooting* chapter.

Check Error Message

Turn the analyzer power on. Inspect the LCD. No error message should be displayed.

If one of the error message or a status annotation listed below appears on the LCD, continue with the *Digital Control Troubleshooting* chapter.

- `POWER ON TEST FAILED`
- `Svc` (Status annotation)

These error messages indicate that one of power-on self tests fails. If an other error message appears, refer to the *Error Messages* in Messages.

If the response of front panel, GPIB commands, or built-in FDD is unexpected, continue with the *Digital Control Troubleshooting* chapter.

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OPERATOR'S CHECK

The *Operator's Check* verifies with 80% confidence that the analyzer is functioning properly. This is an excellent test to begin troubleshooting measurement problems.

When you want to test the individual analyzer specifications, perform the performance test in accordance with the *Performance Test Manual*. If one or some of the performance tests fail, continue with the *Isolate Faulty Group Troubleshooting* chapter.

Test Equipment

Two-Way Power Splitter	11667A
50Ω Termination (two required)	909C Opt 012 or part of 85032B
Type-N Cable, 61 cm (two required)	11500B or part of 11851B
BNC cable, 30 cm	PN 8120-1838
N(m)-N(m) adapter	PN 1250-1475
N(m)-BNC(f) adapter	PN 1250-1476

Procedure

1. Turn the analyzer power on.
2. Press (PRESET) to initialize the analyzer.
3. Press (SYSTEM), SERVICE MENU, TESTS, (5), (3), (x1) to access the ALL EXT 1 test. When "TEST 53 ALL EXT 1" appears on the LCD, press EXECUTE TEST.
4. The connection instruction is displayed on the LCD. Connect the equipment as shown in Figure 3-2. Then press CONT.

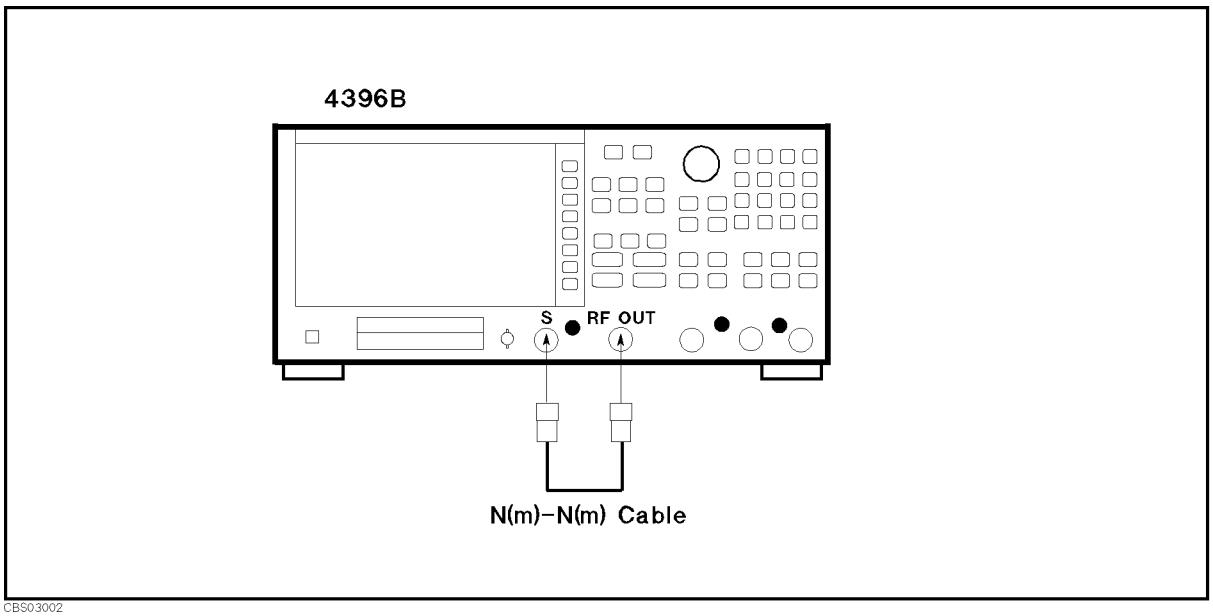


Figure 3-2. ALL EXT 1 Test Setup

5. Wait until the analyzer displays the test result. The analyzer displays the test results, PASS or FAIL, as shown in Figure 3-3.

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■ If the ALL EXT 1 test fails, continue with step 18.

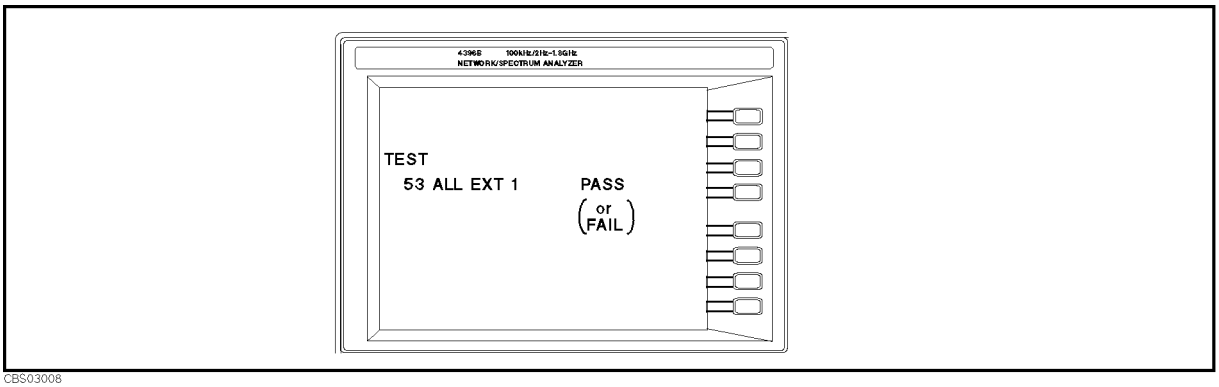


Figure 3-3. Displayed Result of ALL EXT Test

6. Press (↑) to access the ALL EXT 2 test. Then press `EXECUTE TEST` to execute the test.
7. At the prompt, connect the equipment as shown in Figure 3-4. Then press `CONT`.

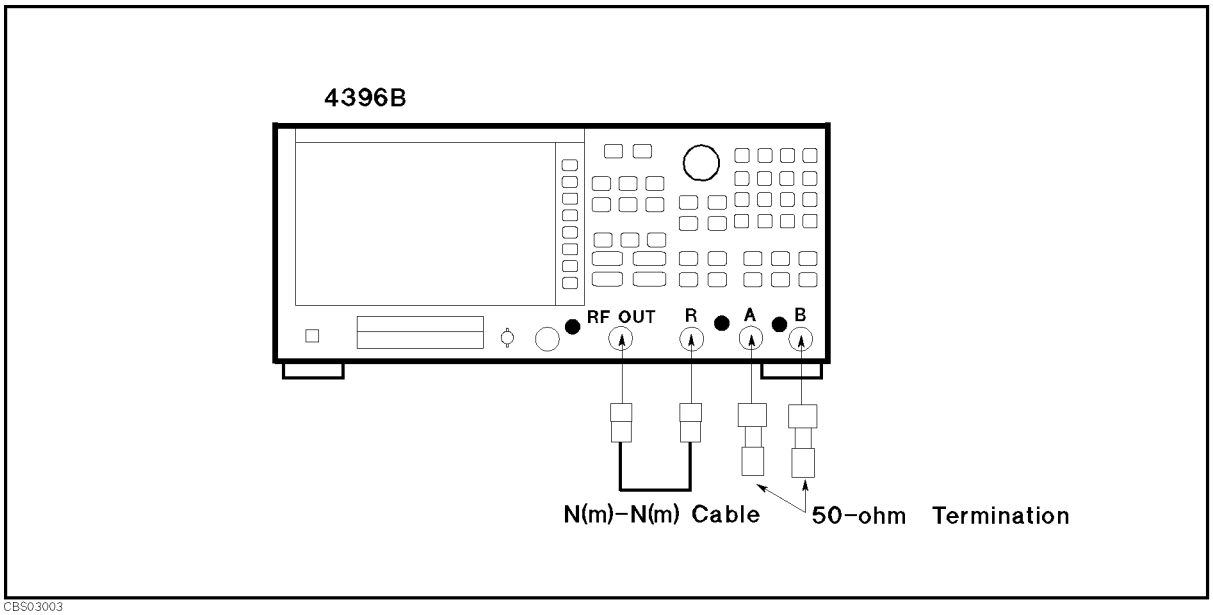


Figure 3-4. ALL EXT 2 Test Setup

8. Wait until the analyzer displays PASS or FAIL.
   ■ If the ALL EXT 2 test fails, continue with step 18.
9. Press (↑) to access the ALL EXT 3 test. Then press `EXECUTE TEST` to execute the test.
10. At the prompt, connect the equipment as shown in Figure 3-5. Then press `CONT`.

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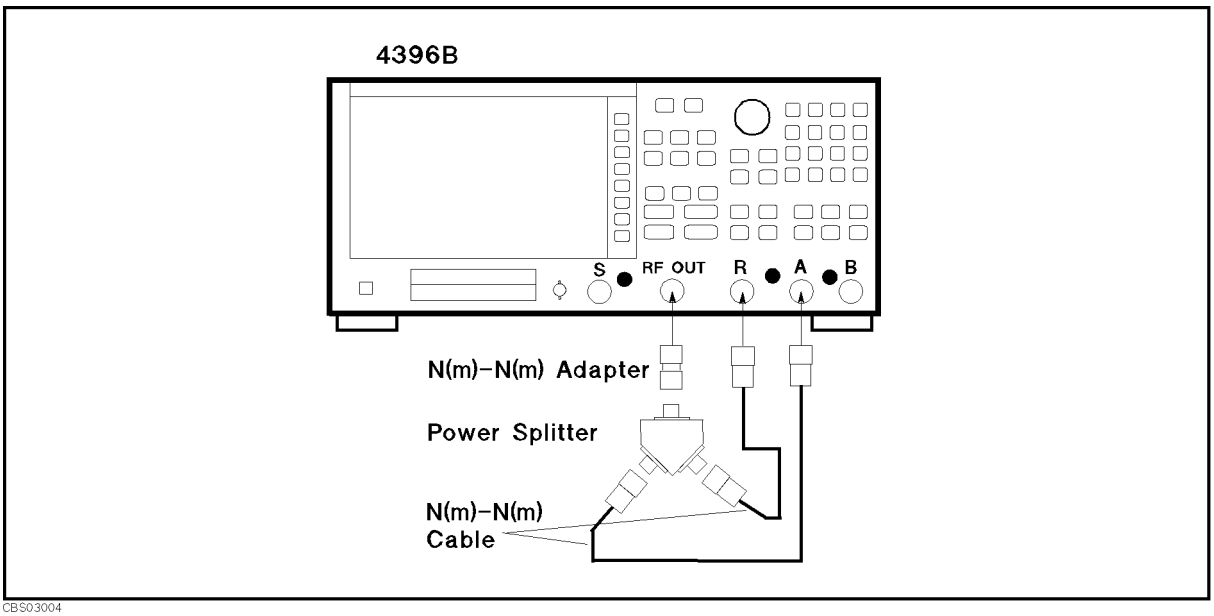


Figure 3-5. ALL EXT 3 Test Setup

11. Wait until the analyzer displays PASS or FAIL.
    - If the ALL EXT 3 test fails, continue with step 18.
12. Press ⇧ to access the ALL EXT 4 test. Then press `EXECUTE TEST`.
13. At the prompt, connect the equipment as shown in Figure 3-6. Then press `CONT`.

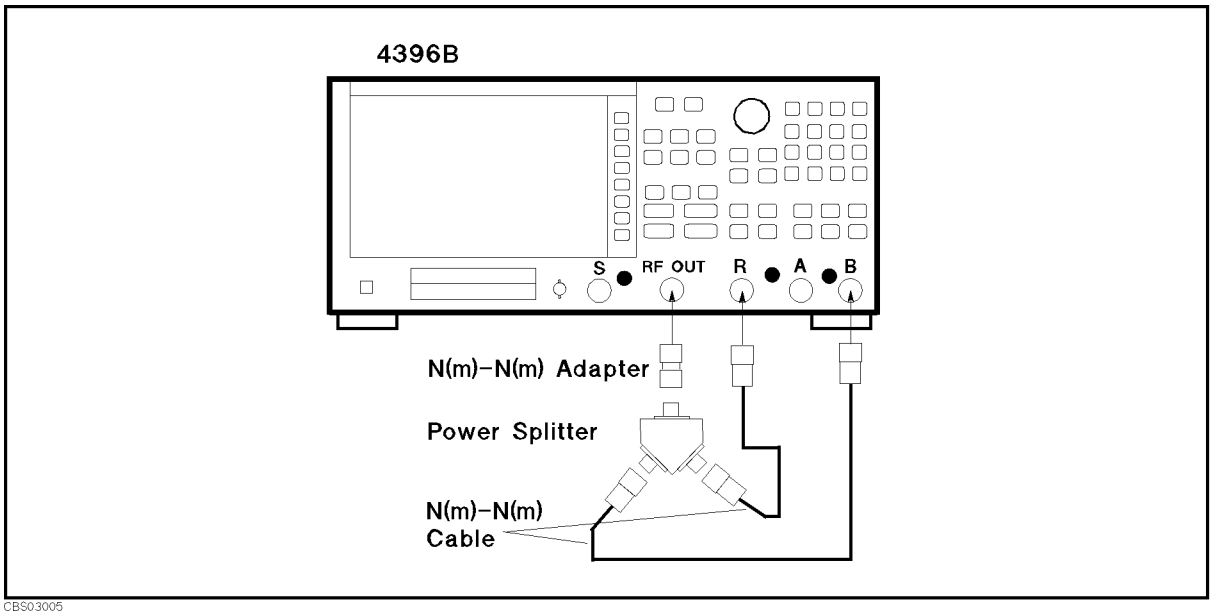


Figure 3-6. ALL EXT 4 Test Setup

14. Wait until the analyzer displays PASS or FAIL.

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- If the ALL EXT 4 test fails, continue with step 18.

15. Press (⇧) to access the ALL EXT 5 test. Then press `EXECUTE TEST`.

16. At the prompt, connect the equipment as shown in Figure 3-7. Then press `CONT`.

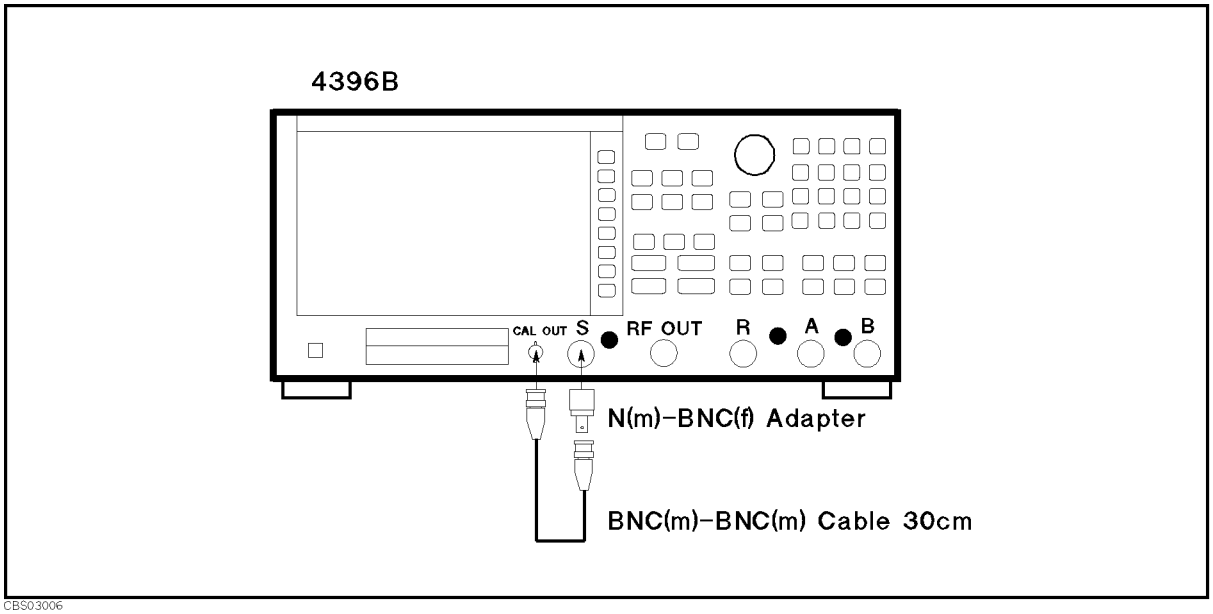


Figure 3-7. ALL EXT 5 Test Setup

17. Wait until the analyzer displays PASS or FAIL.

18. If one or some of the ALL EXT tests fail:

- Recheck the equipment configuration and connections; if necessary, retest.
- Confirm that the power splitter, terminations, and cables meet their published specifications. Visually inspect the connectors. If necessary, retest.
- If the tests still fail, continue with the *Isolate Faulty Group Troubleshooting* chapter.

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INSPECT THE REAR PANEL FEATURE

If the analyzer is operating unexpectedly after these checks are verified, continue with *Digital Control Troubleshooting* chapter.

Check the GPIB Interface

If the unexpected operations appear when controlling the analyzer with an external controller, perform the following checks to verify the problem is not with the controller.

- Compatibility, must be HP 9000 series 200/300, see the manuals of the controller and the BASIC system.
- GPIB interface hardware must be installed in the controller, see the manuals of the controller and the BASIC system.
- I/O and GPIB binaries loaded, see the manuals of the BASIC system.
- Select code, see the manuals of the BASIC system.
- GPIB cables, see the manuals of the BASIC system.
- Programming syntax, see the manuals of the BASIC system.

Check the Parallel Interface

See the Printing Out The Measurement Result at the Chapter 3, Network Analyzer Tour of the 4396B User's Guide, and make a hardcopy of the display.

Check the mini DIN Keyboard Connector

See the Connecting a Keyboard at the Chapter 1, Installation and Setup guide of 4396B User's Guide and Using HP Instrument BASIC with the 4396B.

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4

Isolate Faulty Group Troubleshooting

INTRODUCTION

Use these procedures after you have read the *Troubleshooting* chapter. This chapter provides two procedures:

- *OPERATOR'S CHECK FAILURE TROUBLESHOOTING*
- *PERFORMANCE TEST FAILURE TROUBLESHOOTING*

These are procedures to determine which group is faulty in the two functional groups: source, and receiver. Descriptions of these groups are provided in the *Theory of Operation* chapter.

Use the *OPERATOR'S CHECK FAILURE TROUBLESHOOTING* when the *Operator's Check* in *Troubleshooting* chapter fails. Use the *PERFORMANCE TEST FAILURE TROUBLESHOOTING* when any of the performance tests fail. These procedures isolates the most probable faulty group.

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OPERATOR'S CHECK FAILURE TROUBLESHOOTING

Perform the following procedures sequentially when the *Operator's Check* in *Troubleshooting* chapter fails.

Check RF OUT Frequency

This uses a frequency counter to measure the actual frequency of the analyzer RF OUT signal when it tuned to 1 GHz or a particular frequency of the measurement problem. This purposes to verify the A5 synthesizer operation. If the frequency accuracy meets its specification, the A5 synthesizer is probably working.

1. Perform the *FREQUENCY ACCURACY TEST* in accordance with the *Performance Test Manual (pn 04396-90120).*

If the measurement problem troubleshooted appears at a particular frequency or other controls, set the analyzer to the controls of the measurement problem. Then verify the frequency accuracy meets the specification.

If this test fails, continue with the *Source Troubleshooting* chapter. If this test passes, go to the next *Check RF OUT Power Level* section.

Check RF OUT Power Level

This uses a power meter and a power sensor to measure the actual power level of the RF OUT signal. This verifies the operation of the A3 source module that consists of A3A1 ALC, A3A2 2nd LO, and A3A3 source. If the level accuracy meets its specification, the A3 source module is probably working.

1. Perform the *SOURCE LEVEL ACCURACY/FLATNESS TEST* in accordance with the *Performance Test Manual (pn 04396-90120).*
2. Perform the *POWER SWEEP LINEARITY TEST* in accordance with the *Performance Test Manual.*

If the measurement problem troubleshooted appears at a particular power level or other controls, set the analyzer to the particular controls. And measure the RF OUT power level. Then verify the RF OUT power level meets the specification.

If this test fails, continue with the *Source Troubleshooting* chapter.

If this test passes but still making the operator's check failure, the probable faulty group is receiver. Continue with the *Receiver Troubleshooting* chapter.

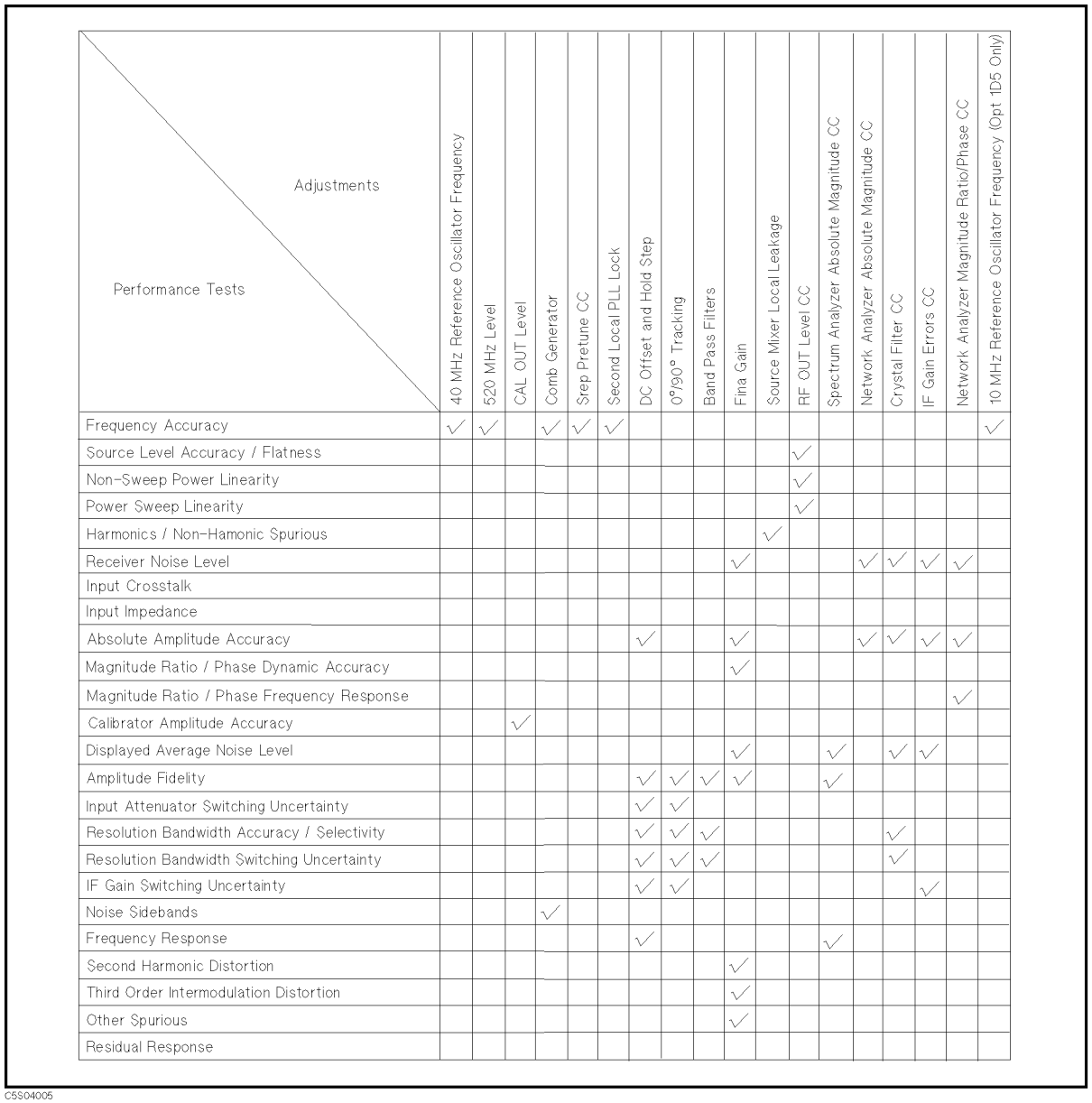
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PERFORMANCE TESTS FAILURE TROUBLESHOOTING

Perform the following procedure sequentially when any of performance tests fail.

Perform Adjustments and Correction Constants

Figure 4-1 gives the recommended adjustments and correction constants when a performance test fails. If a performance test fails, you should perform the corresponding adjustments or correction constants function as shown in Figure 4-1. If the tests still fail, see Table 4-1. In a few cases, other adjustments and correction constants may bring the tests into specification. The following table lists some typical cases.



Performance Tests \ Adjustments	40 MHz Reference Oscillator Frequency	520 MHz Level	CAL OUT Level	Comb Generator	Srep Preture CC	Second Local PLL Lock	DC Offset and Hold Step	0°/90° Tracking	Band Pass Filters	Fina Gain	Source Mixer Local Leakage	RF OUT Level CC	Spectrum Analyzer Absolute Magnitude CC	Network Analyzer Absolute Magnitude CC	Crystal Filter CC	IF Gain Errors CC	Network Analyzer Magnitude Ratio/Phase CC	10 MHz Reference Oscillator Frequency (Opt 1D5 Only)
Frequency Accuracy	✓	✓		✓	✓	✓												✓
Source Level Accuracy / Flatness												✓						
Non-Sweep Power Linearity												✓						
Power Sweep Linearity												✓						
Harmonics / Non-Hamonic Spurious											✓							
Receiver Noise Level										✓				✓	✓	✓	✓	
Input Crosstalk																		
Input Impedance																		
Absolute Amplitude Accuracy							✓			✓				✓	✓	✓	✓	
Magnitude Ratio / Phase Dynamic Accuracy										✓								
Magnitude Ratio / Phase Frequency Response																	✓	
Calibrator Amplitude Accuracy			✓															
Displayed Average Noise Level										✓			✓		✓	✓		
Amplitude Fidelity							✓	✓	✓	✓			✓					
Input Attenuator Switching Uncertainty							✓	✓										
Resolution Bandwidth Accuracy / Selectivity							✓	✓	✓						✓			
Resolution Bandwidth Switching Uncertainty							✓	✓	✓						✓			
IF Gain Switching Uncertainty							✓	✓								✓		
Noise Sidebands				✓														
Frequency Response							✓						✓					
Second Harmonic Distortion										✓								
Third Order Intermodulation Distortion										✓								
Other Spurious										✓								
Residual Response																		

C5S04005

Figure 4-1. Recommended Adjustments and Correction Constants.

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Troubleshoot Suspicious Functional Group

Table 4-1 lists the functional groups to suspect first when a performance test fails. If a performance test fails, you should check the function groups as shown in the table. The following table lists some typical cases. In a few cases, other groups may actually be faulty.

Table 4-1. Functional Group to Suspect When a Performance Test Fails

Test	Source	Receiver	Most Suspicious Assembly
Frequency Accuracy	√		
Source Level Accuracy/Flatness.	√		
Non-Sweep Power Linearity	√		
Power Sweep Linearity	√		
Harmonics and Non-Harmonics	√		
Receiver Noise Level	√	√	
Input Crosstalk	√	√	A9
Input Impedance		√	A9
Absolute Amplitude Accuracy		√	
Magnitude Ratio/Phase Dynamic Accuracy		√	
Magnitude Ratio/Phase Frequency Response		√	
Calibrator Amplitude Accuracy	√		A5
Displayed Average Noise Level	√	√	
Amplitude Fidelity		√	
Input Attenuator Switching Uncertainty		√	A8
Resolution Bandwidth Accuracy/Selectivity		√	A6
Resolution Bandwidth Switching Uncertainty		√	A6
IF Gain Switching Uncertainty		√	A6
Noise Sideband	√	√	
Frequency Response		√	
Second Harmonics Distortion		√	
Third Order Intermodulation Distortion		√	
Other Spurious		√	
Residual Response		√	

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5

Power Supply Troubleshooting

INTRODUCTION

Use this procedure only if you have read *Troubleshooting*, and you believe the problem is in the power supply. The procedure is designed to let you identify the bad assembly within the power supply functional group in the shortest possible time.

The power supply functional group consists of:

- A40 Pre-Regulator
- A50 DC-DC Converter
- A2 Post-Regulator

All assemblies, however, are related to the power supply functional group because power is supplied to each assembly. Figure 5-1 shows all power lines in simplified block diagram form. For more information about the signal paths and specific connector pin numbers, see Figure 5-12, Figure 5-13, and Figure 5-14 at the end of this chapter.

If an assembly is replaced, see Table 13-1 *Post Repair Procedures* in the *Post Repair Procedures* chapter in this manual. It tells what additional tests or adjustments need to be done after replacing any assembly.

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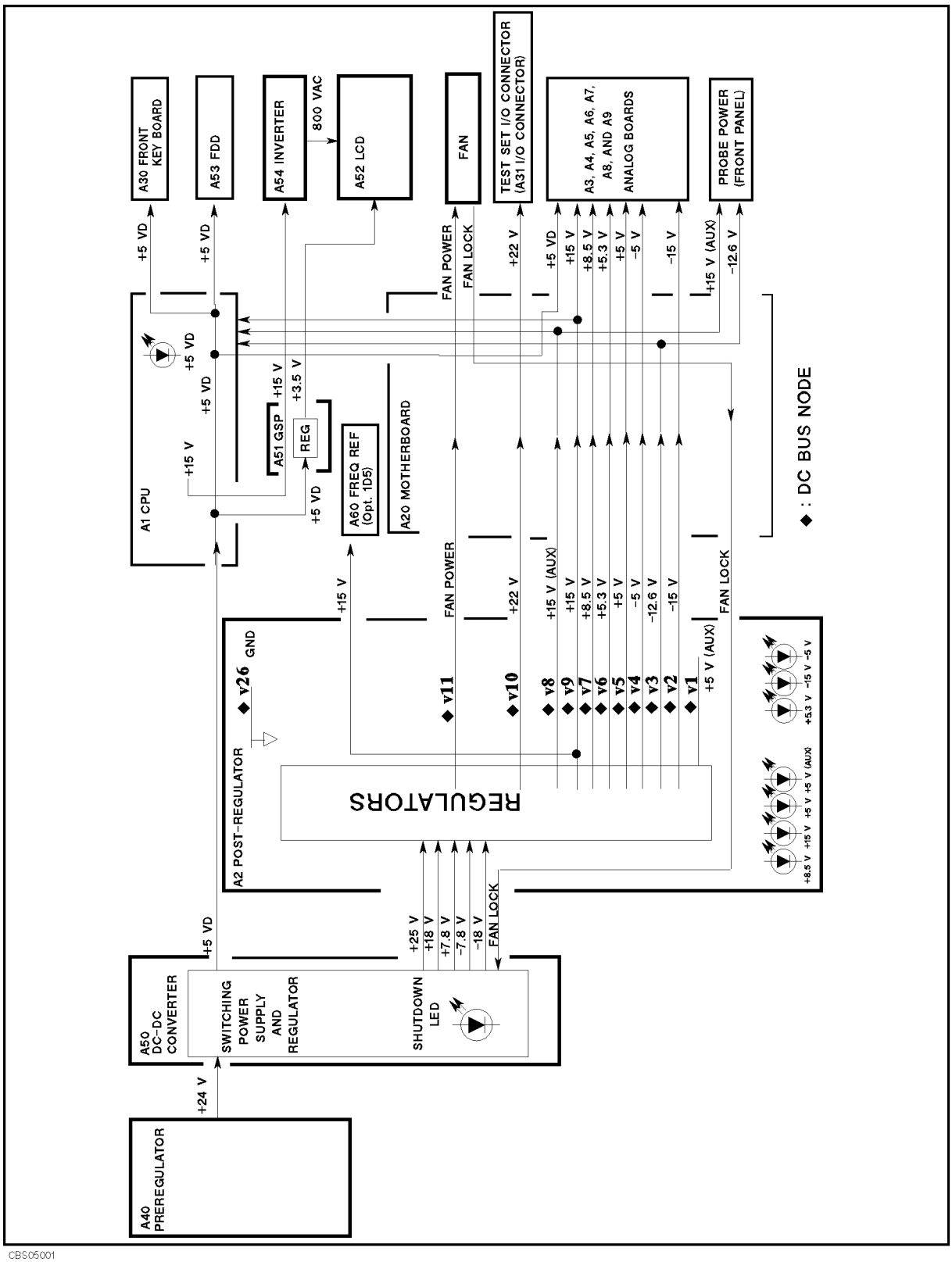


Figure 5-1. Power Supply Lines Simplified Block Diagram

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START HERE

1. Check Error Messages

Turn the analyzer power on. If one of error messages listed below appears on the display, follow the instruction of the displayed error message. If no error message is displayed, continue with the next *Check the Fan is Rotating*.

Error Messages	Instruction
`POWER FAILED ON - - -`	One or some of A2 power supplies, +15 V, +8.5V, +5.3 V, +5 V, -5 V, -15 V are displayed in - - - of the message. The displayed power supplies are shut down due to the trouble on the A2 post-regulator. Continue with the *CHECK THE A2 EIGHT LEDs* in this *START HERE*.
`POWER FAILED ON PostRegHot`	This indicates A2 power supplies, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V, are shut down due to too hot heat sink on A2 post-regulator. Cool down the analyzer for about 30 minutes. Then turn the analyzer power on. If this message is still displayed, replace A2 post-regulator.

These messages are associated with the power supplies functional group. These messages indicate the A2 protective shutdown circuit is shutting down some of A2 power supplies to protect them from over current, over voltage, under voltage, and too hot conditions. For more information about the A2 shutdown circuit, see the Figure 5-13 Power Supply Block Diagram 2.

Note



These messages are displayed only after the power on sequence. When one of these message is displayed, the analyzer's front keys are disabled. In the power on sequence, the analyzer checks the shutdown status of the A2 power supplies, +15 V, +5 V, -5 V, -15 V. If a power supply is shut down, the analyzer displays an error message and stops its operation. Once the analyzer stops the operation, any front key operations are disabled. The only way to reset the analyzer is turning the analyzer power off.

2. Check the Fan is Rotating

Look at the fan on the rear panel. Check the fan is rotating.

- If the fan is not rotating, continue with the *FIND OUT WHY THE FAN IS NOT ROTATING* in this chapter.
- If the fan is rotating, continue with the next *Check the A50 SHUTDOWN LED.*

3. Check the A50 SHUTDOWN LED

There is a LED, SHUTDOWN LED, on the A50 DC-DC Converter. Perform the following procedure to check it. The SHUTDOWN LED is described in the next *A50 SHUTDOWN LED* .

a. Turn the analyzer power off.

b. Remove the analyzer's top cover and shield plate.

c. Turn the analyzer power on.

d. Look at the A50 SHUTDOWN LED. The LED is normally on. The SHUTDOWN LED location on A50 DC-DC Converter is shown in Figure 5-2.

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- If the A50 SHUTDOWN LED is off, check the cable connection between A50J2 and A2J4. If the connection is good, continue with the *FIND OUT WHY THE A50 SHUTDOWN LED IS OFF* in this chapter.
- If the A50 SHUTDOWN LED is on, continue with the *Check the A1 +5 VD LED* in this procedure.

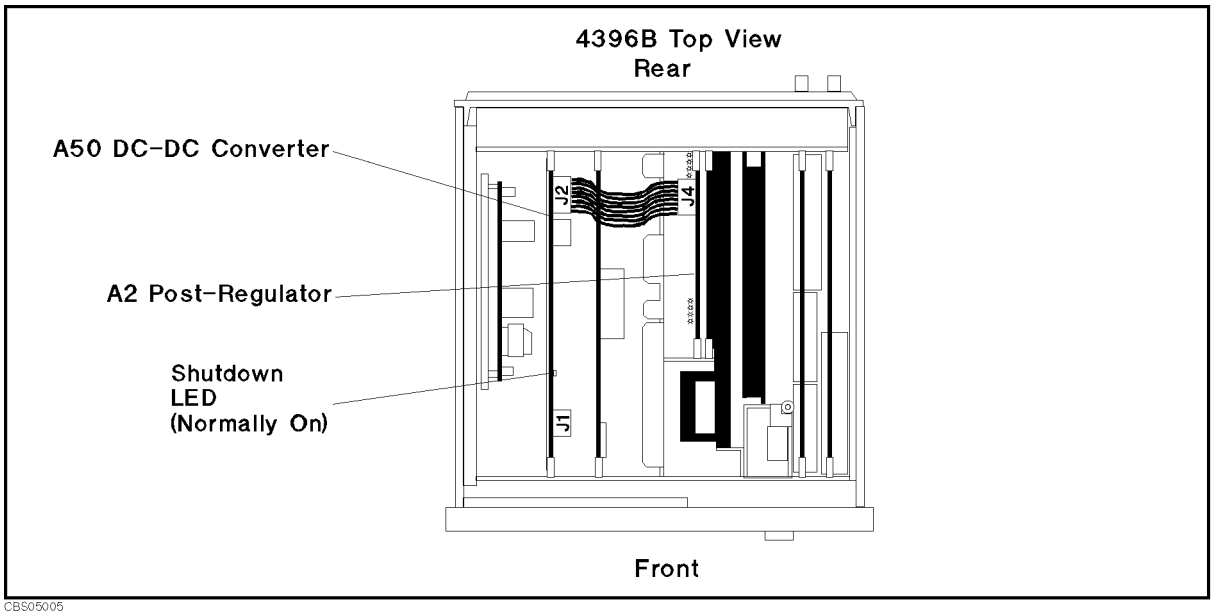


Figure 5-2. A50 SHUTDOWN LED Location

A50 Shutdown LED

The A50 SHUTDOWN LED turning off indicates some of A50 power supply is shut down by the A50 shutdown circuitry.

There are two FAN conditions, rotating and not rotating when the SHUTDOWN LED turns off. When the fan is rotating, the shutdown circuit is probably activated by the over current condition on the power lines in the A50 DC-DC Convereter or the A2 Post Regulator. In this condition, though the A50 power supplies, +24 V, +5 VD, +18 V, +7.8 V, -7.8 V, and -18 V are shut down, the Fan Power +24 V is still supplied to the fan. When the fan is not rotating, the shutdown circuit is probably activated by the FAN LOCK signal missing.

For more information about the A50 shutdown circuit operation, see the Figure 5-12 Power Supply Block Diagram 1.

Note

Once the A50 shutdown circuit is activated, the only way to reset the circuit is turning the analyzer power off. Wait a minute after turning the analyzer off. Then turn it on.

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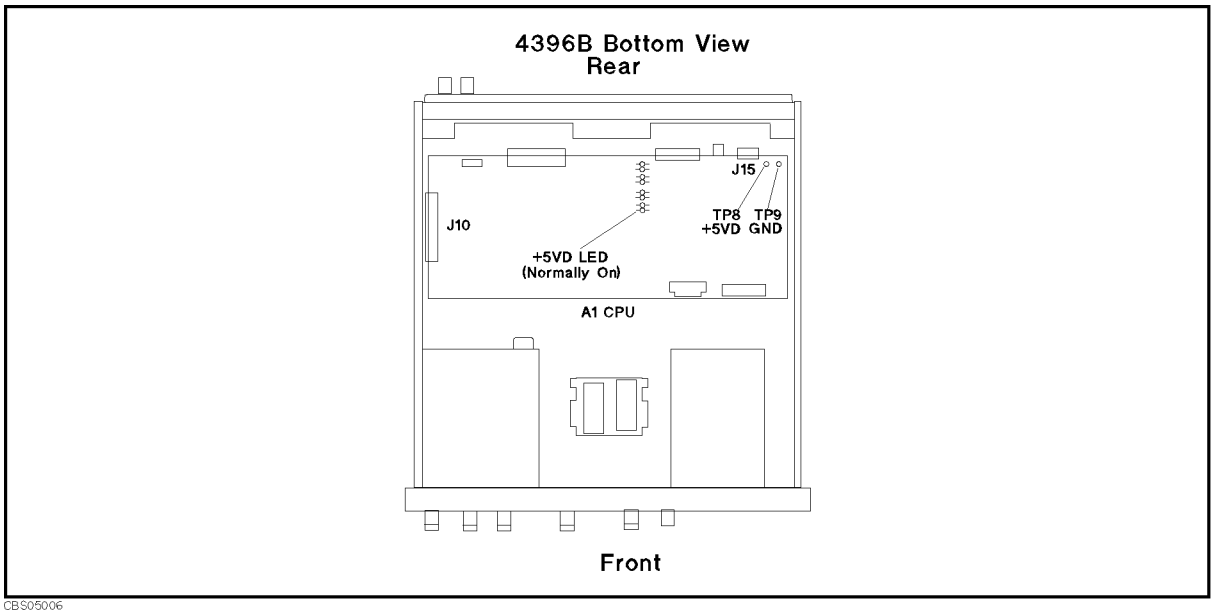
4. Check the A1 +5 VD LED

a. Remove the analyzer's bottom cover.

b. Turn the analyzer power on.

c. Look at the +5 VD LED. The +5 VD LED location on A1 CPU is shown in Figure 5-3. The LED is normally on.

- If the +5 VD LED is off, continue with the *FIND OUT WHY THE A1 +5 VD LED IS NOT ON STEADILY* in this chapter.
- If the +5 VD LED is on, the +5 VD power supply is verified with 95% confidence level. Continue with the *Check A2 Eight LEDs* in this procedure. If you want to confirm the last 5% uncertainty, perform steps in the next *Measure the A1 +5 VD Voltage*.



CBS05006

Figure 5-3. A1 +5 VD LED Location

Measure the A1 +5 VD Voltage

Measure the DC voltage on a test point A1TP8 (+5 VD) using a voltmeter. Check the voltmeter reading is within 4.59 V to 5.61 V.

- If the voltmeter reading is out of the limits, continue with the *FIND OUT WHY THE A1 LED IS NOT ON STEADILY*.
- If the voltmeter reading is within the limits, continue with the next step.

5. Check the A2 Eight LEDs

a. Remove the analyzer's top cover and shield.

b. Turn the analyzer power on.

c. Look at the A2 eight LEDs. The A2 eight LED locations are shown in Figure 5-4. Check the LEDs are correctly on.

- If two or more LEDs are off, continue with the *TROUBLESHOOT A2 POST-REGULATOR* in this chapter.

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- If the LEDs are correctly on, continue with the next *Run the Internal Test 4: A2 POST REGULATOR*.

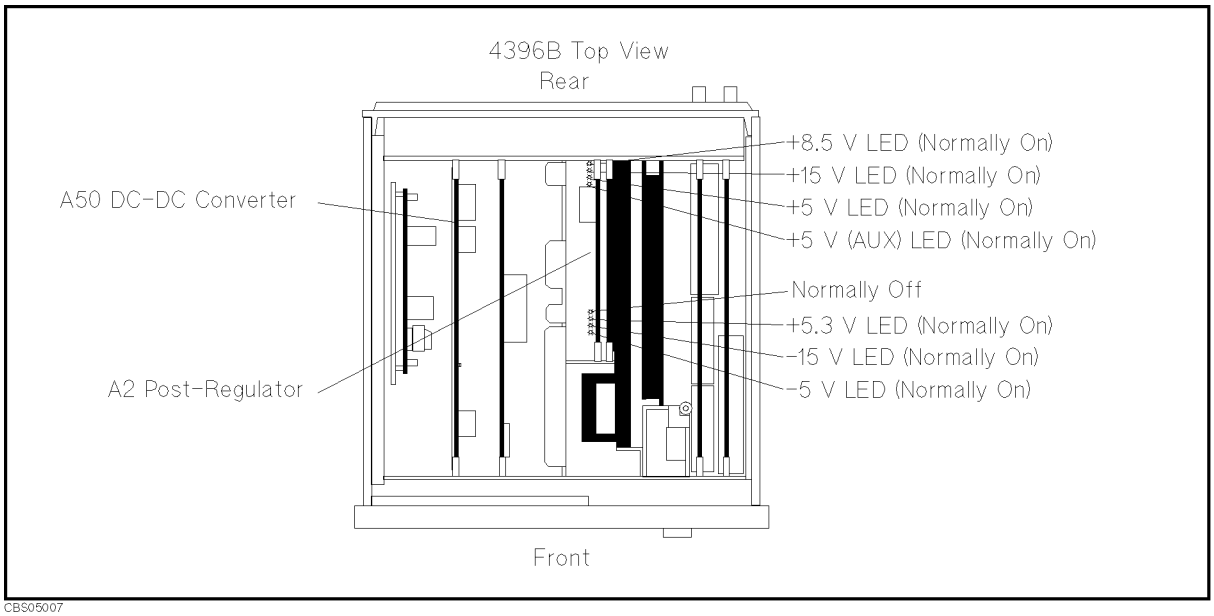


Figure 5-4. A2 Eight LED Locations

6. Run the Internal Test 4: A2 POST REGULATOR

The internal test 4: A2 POST REGULATOR verifies the A2 post-regulator. Perform the following procedure to check the A2 post-regulator. The internal test 4 is described in the next *Internal Test 4: A2 POST REGULATOR*.

Press (System), SERVICE MENU, TESTS, (4), (x1), EXECUTE TEST to execute the internal test 4: A2 POST REGULATOR. After the test completed, the test result is displayed as shown in Figure 5-5.

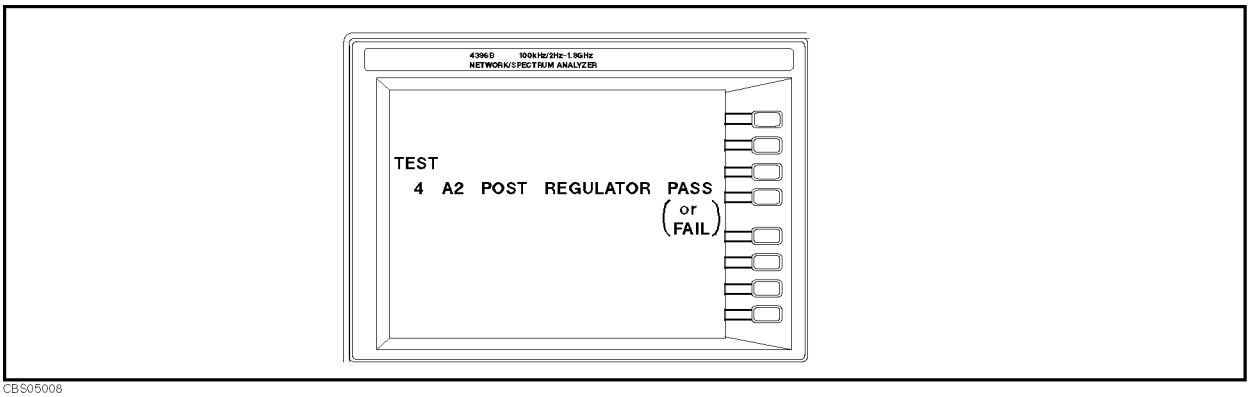


Figure 5-5. Displayed Test Result

- If "PASS" is displayed, the power supply function group are working properly with a 95% confidence level. To confirm the last 5% uncertainty of the A2 power supplies, measure the all A2 power supply voltages. See the *MEASURE A2 POST-REGULATOR OUTPUT VOLTAGE* at the end of this chapter.

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- If “FAIL” is displayed, perform the following steps.
  a. Press `RETURN`, `SERVICE MODES`, `BUS MEAS [ON]`, `DC BUS`. Then the abbreviated faulty power supply is displayed on the LCD.
  b. Continue with the *TROUBLESHOOT A2 POST-REGULATOR* in this chapter. In particular, check the faulty power supply.

Internal Test 4: A2 POST REGULATOR

The internal test 4: A2 POST REGULATOR is a built-in diagnostics test. The test checks all A2 power supply voltages within the limits using the DC BUS and the A/D converter on the A6 receiver IF. If a power supply failure is found, the analyzer stops the test process and displays the test result as shown in Figure 5-5. For more information about the internal test and the DC BUS, see the *Service Key Menu* chapter in this manual.

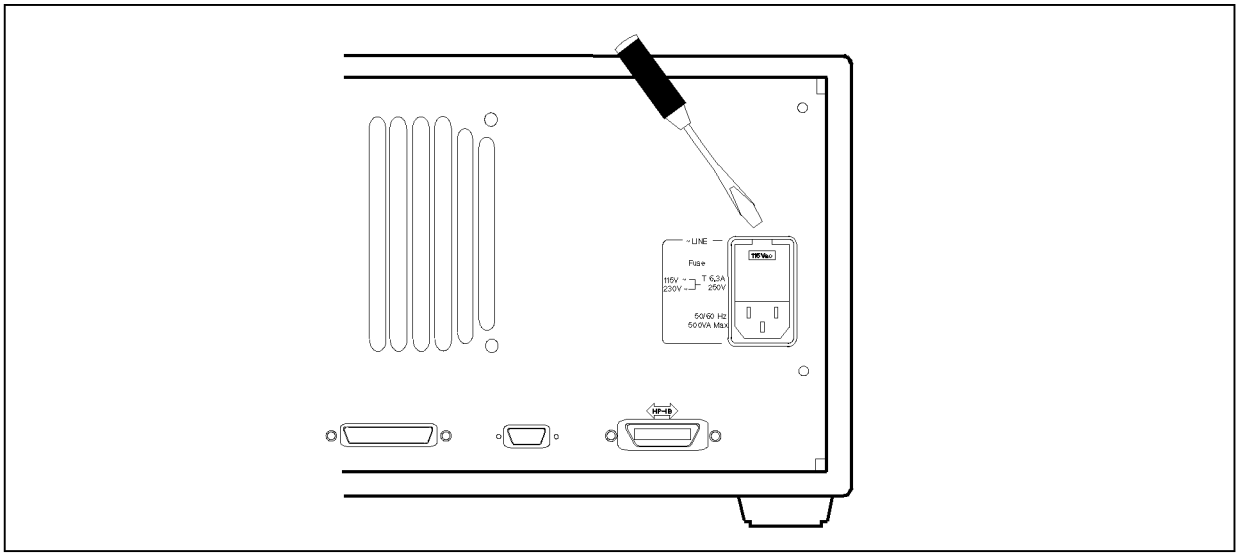
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FIND OUT WHY THE FAN IS NOT ROTATING

If the fan is not rotating, the problem may be in the A40 pre-regulator, the A50 DC-DC Converter, the A2 post-regulator, or the fan.

1. Check the Line Voltage, Selector Switch Setting, and Fuse

Check the main power line cord, line fuse, and actual line voltage to see that they are all correct. Figure 5-6 shows how to remove the line fuse, using a small flat-bladed screwdriver to pry off the fuse holder. For more information about the line cord and line fuse, see the *Power Requirements* in Appendix C.



CBS05010

Figure 5-6. Removing Line Fuse

2. Check the A50 SHUTDOWN LED

When the fan stops, the A50 SHUTDOWN LED is off. See the Figure 5-12 Power Supply Block Diagram 1. The fan generates a FAN LOCK signal. The signal is fed into the FAN LOCK SENSE circuit in the A50 DC-DC converter. If the FAN stops, the FAN LOCK signal is missing. Then the FAN LOCK SENSE circuit activates the A50 shutdown circuitry, resulting the SHUTDOWN LED turned off.

Perform the following procedure to check the A50 SHUTDOWN LED on.

a. Remove the analyzer's top cover and shield plate.

b. Make sure the A2 post-regulator is firmly seated and the cables are connected properly.

c. Turn the analyzer power on.

d. Look at the A50 SHUTDOWN LED. The LED location is shown in Figure 5-2.

- If the SHUTDOWN LED is on, replace the A50 DC-DC Converter.
- If the SHUTDOWN LED is off, check the cable connection between A50J2 and A2J4. If the connection is good, continue with the *TROUBLESHOOT THE FAN AND THE A50 DC-DC Converter* in this chapter.

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FIND OUT WHY THE A50 SHUTDOWN LED IS OFF

Use this procedure when the fan is rotating. If the fan is not rotating, see the *FIND OUT WHY THE FAN IS NOT ROTATING*.

If the fan is rotating, the A50 SHUTDOWN LED turning off indicates the A50 shutdown circuit is protecting the +5 VD power supply from the over voltage condition. The +5 VD power line may be shorted with one of power lines higher than +5 V. The problem may be in the A50 DC-DC Converter, the A2 post-regulator, and any of assemblies obtaining the power from +5 VD supply and the higher power supplies.

1. Disconnect the Cable from the A50J1

Turn the analyzer power off. Disconnect the cable from the A50J1. Turn the analyzer power on.

- If the A50 SHUTDOWN LED is still off, replace the A50 DC-DC Converter.
- If the A50 SHUTDOWN LED goes on, the A50 DC-DC Converter is verified. Turn the analyzer power off and reconnect the cable to the A50J1. Continue with the next *Disconnect the Cable from the A51J2*.

2. Disconnect the Cable from the A51J2

Turn the analyzer power off. Disconnect the cable from the A51J2. Turn the analyzer power on.

- If the A50 SHUTDOWN LED goes on, replace the A51 GSP.
- If the A50 SHUTDOWN LED is still off, the A51 GSP is verified. Turn the analyzer power off and reconnect the cable to the A51J2. Continue with the next *Disconnect the Cable from the A1J10*.

3. Disconnect the Cable from the A1J10

Turn the analyzer power off. Disconnect the cable from A1J10. Turn the analyzer power on.

- If the A50 SHUTDOWN LED goes on, replace the A1 CPU.
- If the A50 SHUTDOWN LED is still off, the A1 CPU is verified. Turn the analyzer power off and reconnect the cable to the A1J10. Continue with the next *Remove Assemblies*.

4. Remove Assemblies

a. Turn the analyzer power off.

b. Remove the assemblies, A3, A4, A5, and A6. Don't remove the A2 post-regulator.

c. Turn the analyzer power on.

- If the A50 SHUTDOWN LED is still off, the A2 post-regulator is probably faulty. Replace the A2 post-regulator. If the SHUTDOWN LED is still off after replacing the A2 post-regulator, inspect the A20 motherboard for soldering bridges and shorted traces on the FAN POWER and the FAN LOCK signal paths.
- If the A50 SHUTDOWN LED goes on, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

d. Reinstall each assembly one at a time. Turn the analyzer power on after each is installed. The assembly that causes the A50 SHUTDOWN LED to go on is the most probable faulty assembly. Replace the assembly.

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FIND OUT WHY THE A1 +5 VD LED IS NOT ON STEADILY

If the +5 VD LED is not on steadily, the +5 VD line voltage is missing or is not enough to power the analyzer. The problem may be in the A40 pre-regulator, the A50 DC-DC Converter, the A1 CPU, and any of assemblies obtaining the power from +5 VD supply.

1. Check the A40 Pre-Regulator

a. Turn the analyzer power off.

b. Disconnect a cable form the A50J1. The A50J1 location is shown in Figure 5-7.

c. Turn the analyzer power on.

d. Check the voltage between the pin 1 and pin 6(GND) of the cable within +22.0 V to +27.0 V using a voltmeter with a small probe.

- If the voltmeter reading is out of the limits, replace the A40 pre-regulator.
- If the voltmeter reading is within the limits, the A40 pre-regulator is verified. Turn the analyzer power off and reconnect the cable to the A50J1. Then continue with the next *Check the A50 DC-DC Converter* section.

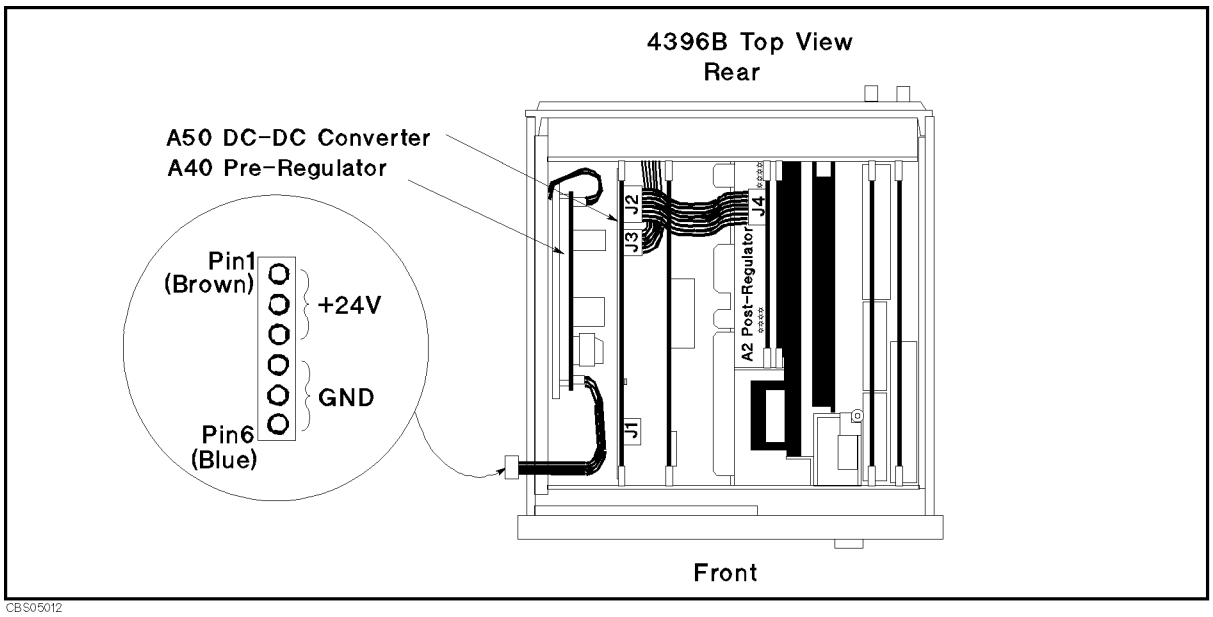


Figure 5-7. A40J1 Output Voltage

2. Check the A50 DC-DC Converter

a. Turn the analyzer power off.

b. Disconnect a cable form the A50J3. The A50J3 location is shown in Figure 5-7.

c. Turn the analyzer power on.

d. Check the voltage between the A50J3 pin 1 and pin 6(GND) within +4.59 V to +5.61 V using a voltmeter with a small probe.

- If the voltmeter reading is out of the limits, replace the A50 DC-DC Converter.

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- If the voltmeter reading is within the limits, the A50 +5 VD power supply is verified. Turn the analyzer power off and reconnect the cable to the A50J3. Then continue with the next *Disconnect Cables on the A1 CPU* section.

3. Disconnect Cables on the A1 CPU

a. Turn the analyzer power off.

b. Disconnect cables from the A1 CPU's connectors, J10, J11, J12, J13, J14, J15, and J17. The connector locations are shown in Figure 5-8

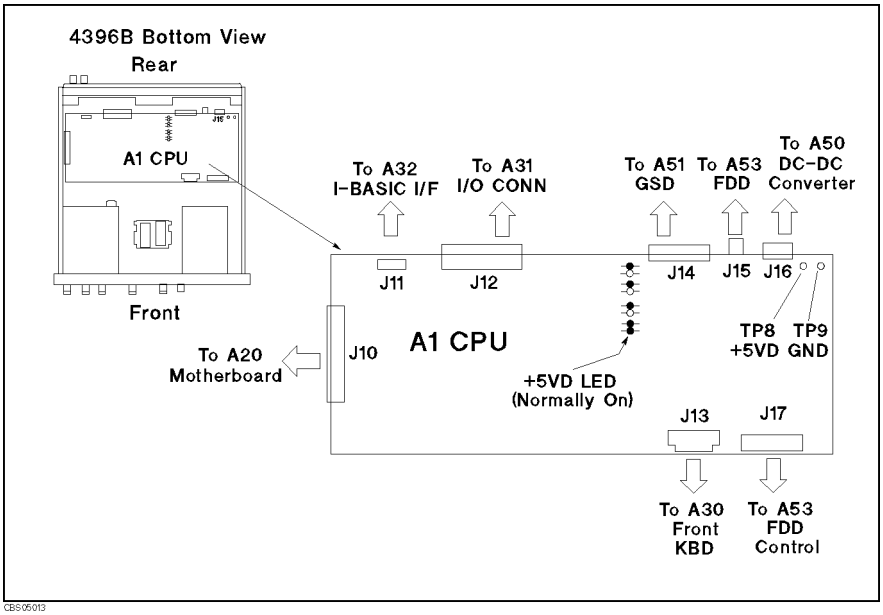


Figure 5-8. A1 CPU Connector Locations

c. Turn the analyzer power on. Look at the A1 +5 VD LED.

- If the LED is still off, the A1 CPU is probably faulty. Replace the A1 CPU.
- If the LED goes on, the A1 CPU is verified. Continue with the next step.

d. Turn the analyzer power off. Reconnect the cable to the A1J10. Turn the analyzer power on. Look at the A1 +5 VD LED.

- If the +5 VD LED goes out, the problem may be in the analog assemblies. Continue with the next *Remove Assemblies*.
- If the + 5 VD LED is still on, continue with the next step.

e. Reconnect one of the disconnected cables to its connector at a time. Turn the analyzer power on after each cable is connected. The assembly related with the cable turning the +5 VD LED off is probably faulty. Replace the assembly.

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4. Remove Assemblies

a. Turn the analyzer power off. Remove the assemblies, A3, A4, A5, A6 and A60. Do not remove the A2 post-regulator.

b. Turn the analyzer power on. Look at the A1 +5 VD LED.

- If the LED is still off, replace the A2 post-regulator. If the +5 VD LED is still off after replacing the A2 post-regulator, inspect the A20 motherboard.
- If the LED goes on, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

c. Reinstall one of the removed assemblies at a time. Turn the analyzer power on after each is installed. The assembly that turns the A1 +5 VD LED on is the most probable faulty assembly. Replace the assembly.

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TROUBLESHOOT THE FAN AND THE A50 DC-DC CONVERTER

Perform the following procedure to troubleshoot the fan and the A50 DC-DC Converter.

1. Troubleshoot the Fan

a. Turn the analyzer power off.

b. Disassemble the rear panel.

c. Remove the fan power cable from the Motherboard A20J18.

d. Connect a DC power supply, a 10 kΩ resistance, and a oscilloscope to the fan power cable using appropriate wires as shown in Figure 5-9.

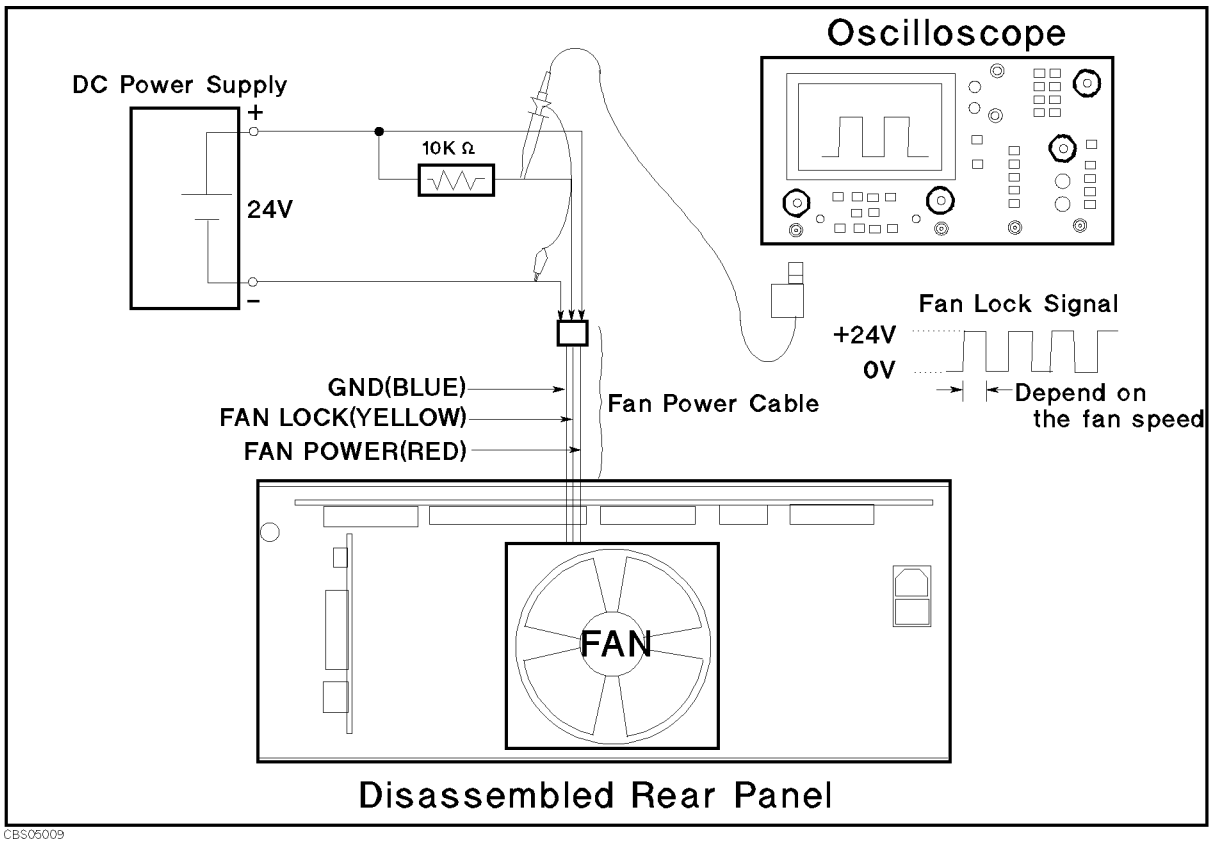


Figure 5-9. Fan Troubleshooting Setup

e. Turn the DC power supply on. Adjust the output voltage to +24 V.

f. Check the fan is rotating. Check the FAN LOCK signal is as shown in Figure 5-9.

- If the fan is not rotating or the FAN LOCK signal is unexpected, replace the fan.
- If these are good, the fan is verified.
- Reconnect the fan power cable to the Motherboard A20J18.

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2. Troubleshoot the A50 DC-DC Converter

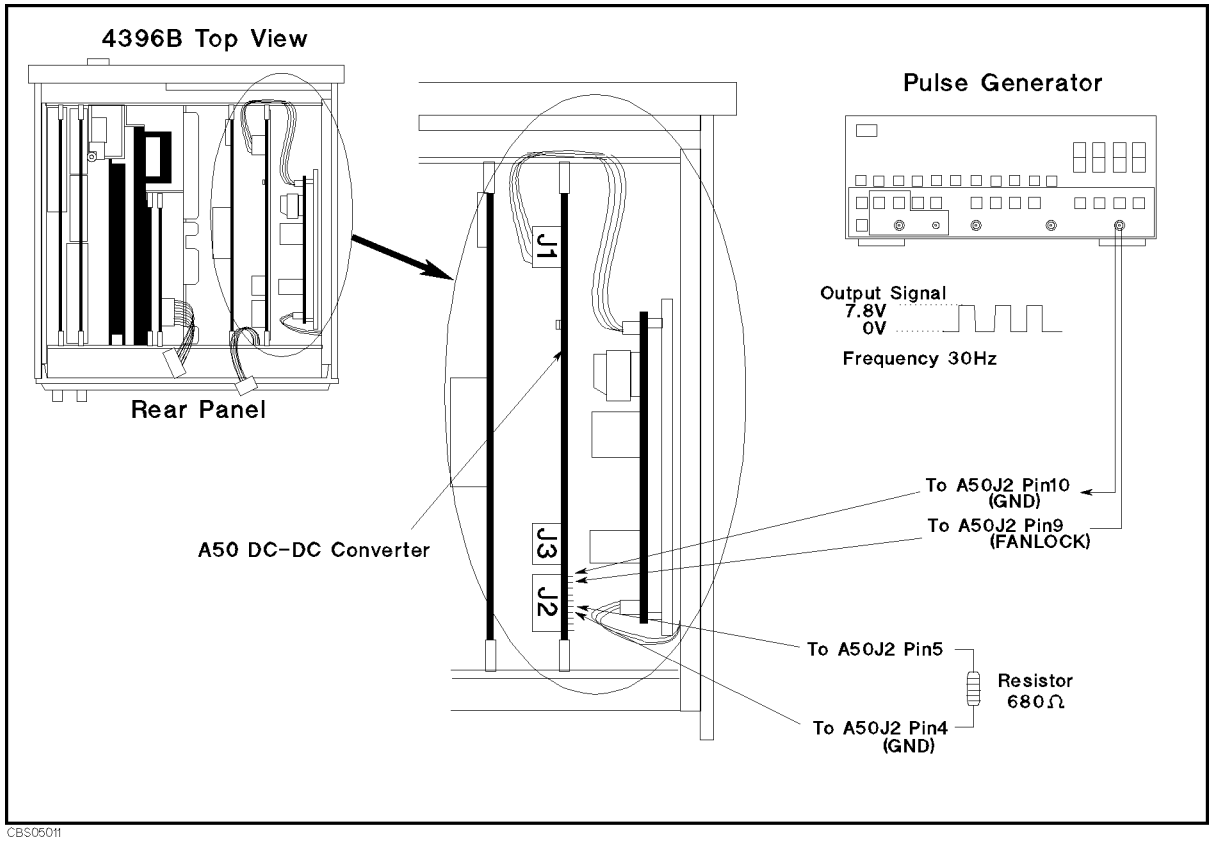


Figure 5-10. A50 DC-DC Converter Troubleshooting Setup

a. Turn the analyzer power off.

b. Disconnect cables from the A50J2 and A50J3. The connector locations are shown in Figure 5-10

c. Connect the pulse generator to the A50J2 as shown in Figure 5-10. The pulse generator is used to feed the substitute of the FAN LOCK signal to the A50 DC-DC converter. This purposes not to shut down the A50 DC-DC converter.

d. Turn the pulse generator power on. Set the controls as follows:

Wave Form	Square
Frequency	Approximately 30 Hz
Amplitude	+7.8 V

e. Connect a resister (appoximately 680ohms, 125mW) between the A50J2 pin 5 (+7.8 V) and pin 4(GND) as shown in Figure 5-10.

f. Turn the analyzer power on.

g. Measure all power supply voltages on A50J2 and A50J3 using a voltmeter with a small probe. See the Table 5-1 for power lines, connector pins, and limits.

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Table 5-1. A50 Power Supplies

Supply	Connector Pin	GND Connector Pin	Range
+5 VD	A50J3 Pin 1, 2, and 3	A50J3 Pin 4, 5, and 6	+4.6 V to +5.7 V
-18 V	A50J2 Pin 1	A50J2 Pin 3 and 4	-14.0 V to -27.0 V
+18 V	A50J2 Pin 2	A50J2 Pin 3 and 4	14.0 V to 27.0 V
+7.8 V	A50J2 Pin 5	A50J2 Pin 3 and 4	7.0 V to 9.0 V
-7.8 V	A50J2 Pin 6	A50J2 Pin 3 and 4	-6.0 V to -12.0 V
+24 V	A50J2 Pin 8	A50J2 Pin 10	22.0 V to 27.0 V

- If any of the power supply voltages are out of the limits, replace the A50 DC-DC Converter.
- If all A50 power supply voltages are good, the A50 pre-regulator is verified.

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TROUBLESHOOT THE A2 POST-REGULATOR

Use this procedure when the fan is rotating and the A50 SHUTDOWN LED turns on.

If one or some of the A2 eight LEDs are not on steadily, the corresponding A2 power supply voltages, -15 V, -5 V, +5 V, +5.3 V, +15 VD, are missing or are not enough to power the analyzer. The problem may be in the A40 pre-regulator, the A50 DC-DC Converter, the A2 post-regulator, and any of assemblies obtaining the A2 post-regulator.

1. Check the A40 Pre-Regulator

See *FIND OUT WHY THE A1 +5VD LED IS NOT ON STEADILY* section to verify the A40 Pre-Regulator.

2. Check the A50 DC-DC Converter

See *TROUBLESHOOT THE FAN AND THE A50 DC-DC CONVERTER* section to verify the A50 DC-DC Converter.

3. Remove Assemblies

See *FIND OUT WHY THE A1 +5VD LED IS NOT ON STEADILY* section to verify the A3, A4, A5, A6 and A60.

4. Measure the A2 Post Regulator Output Voltages

Use this procedure to measure all A2 post-regulator voltages. If all A2 output voltages are within the limits, the A2 post-regulator is verified with 100% confidence.

This procedure put out the A2 post-regulator from the analyzer and measure the voltages on the A2J3 pins. A pulse generator is used to feed the substitute of the FAN LOCK signal to the A2 post regulator. This purposes not to shut down the A50 DC-DC converter.

a. Turn the analyzer power off.

b. Remove the cable from A2J4.

c. Remove A2 post-regulator from the analyzer.

d. Reconnect the cable between the A2J4 and the A50J2 as shown in Figure 5-11.

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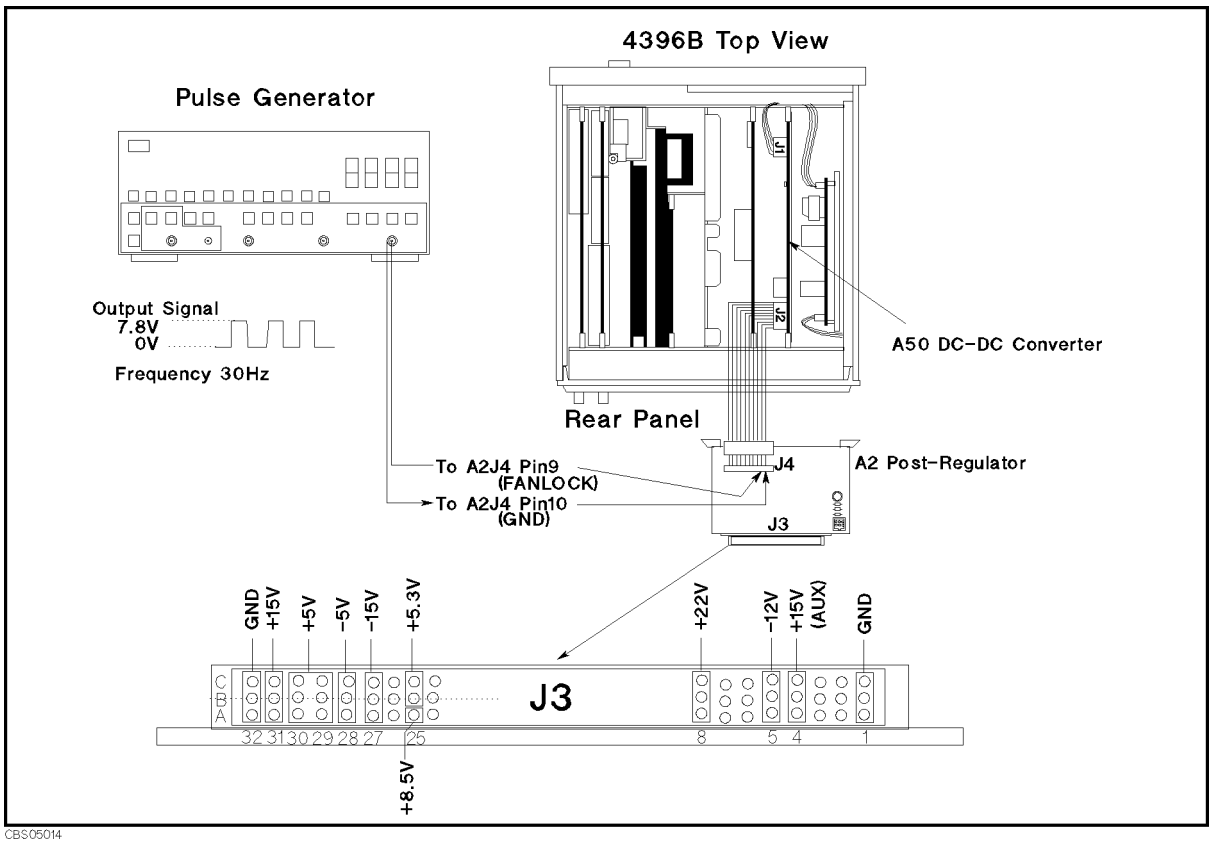


Figure 5-11. A2 Output Voltage Measurement Setup

e. Connect the pulse generator to the A2J4 as shown in Figure 5-11.

f. Turn the pulse generator power on. Set the controls as follows:

Wave Form	Square
Frequency	Approximately 30 Hz
Amplitude	+7.8 V

g. Turn the analyzer power on.

h. Measure the A2 output voltages at the A2J3 pins using a voltmeter with a small probe. See Figure 5-11 and Table 5-2 for the power supplies, A2J3, and the limits.

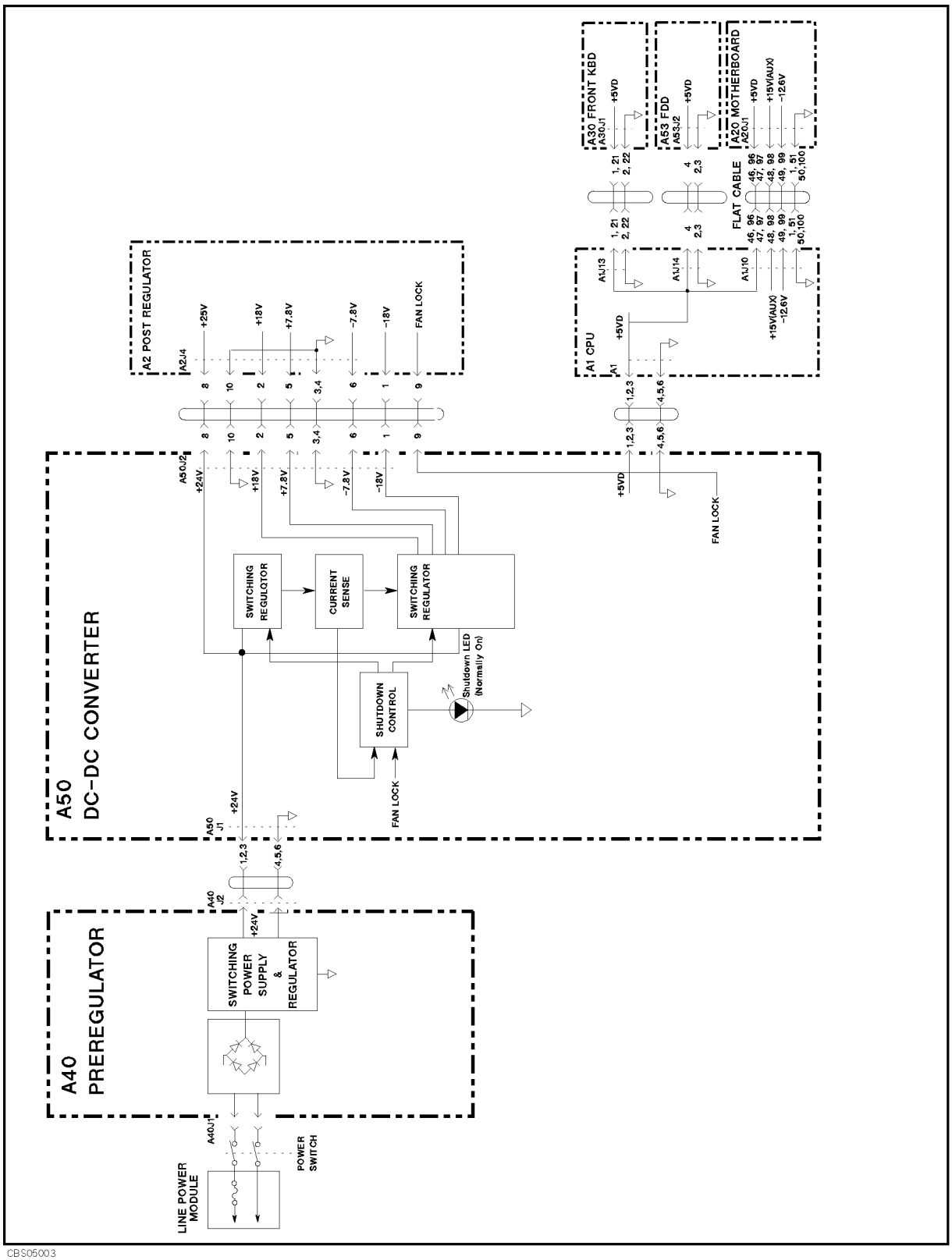
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Table 5-2. Power Supplies on A2 Post-Regulator

Supply	Connector Pin	Range
+22 V	J3 Pin 8	19.8 V to 24.2 V
+15 V(AUX)	J3 Pin 4	13.5 V to 16.5 V
+15 V	J3 Pin 31	13.5 V to 16.5 V
+8.5 V	J3 Pin 25C	7.65 V to 9.35 V
+5.3 V	J3 Pin 25A 25B	4.77 V to 5.83 V
+5 V	J3 Pin 30 29	4.5 V to 5.5 V
-5 V	J3 Pin 28	-4.5 V to -5.5 V
-12 V	J3 Pin 5	-10.8 V to -13.2 V
-15 V	J3 Pin 27	-13.5 V to -16.5 V
FAN POWER	J3 Pin 8	19.2 V to 28.8 V
GND	J3 Pin 3,4,10	
	J5 Pin 4	

- If any of the line voltages are out of the limits, replace the A2 post-regulator.
- If all line voltages are within the limits, the A2 post-regulator is verified.

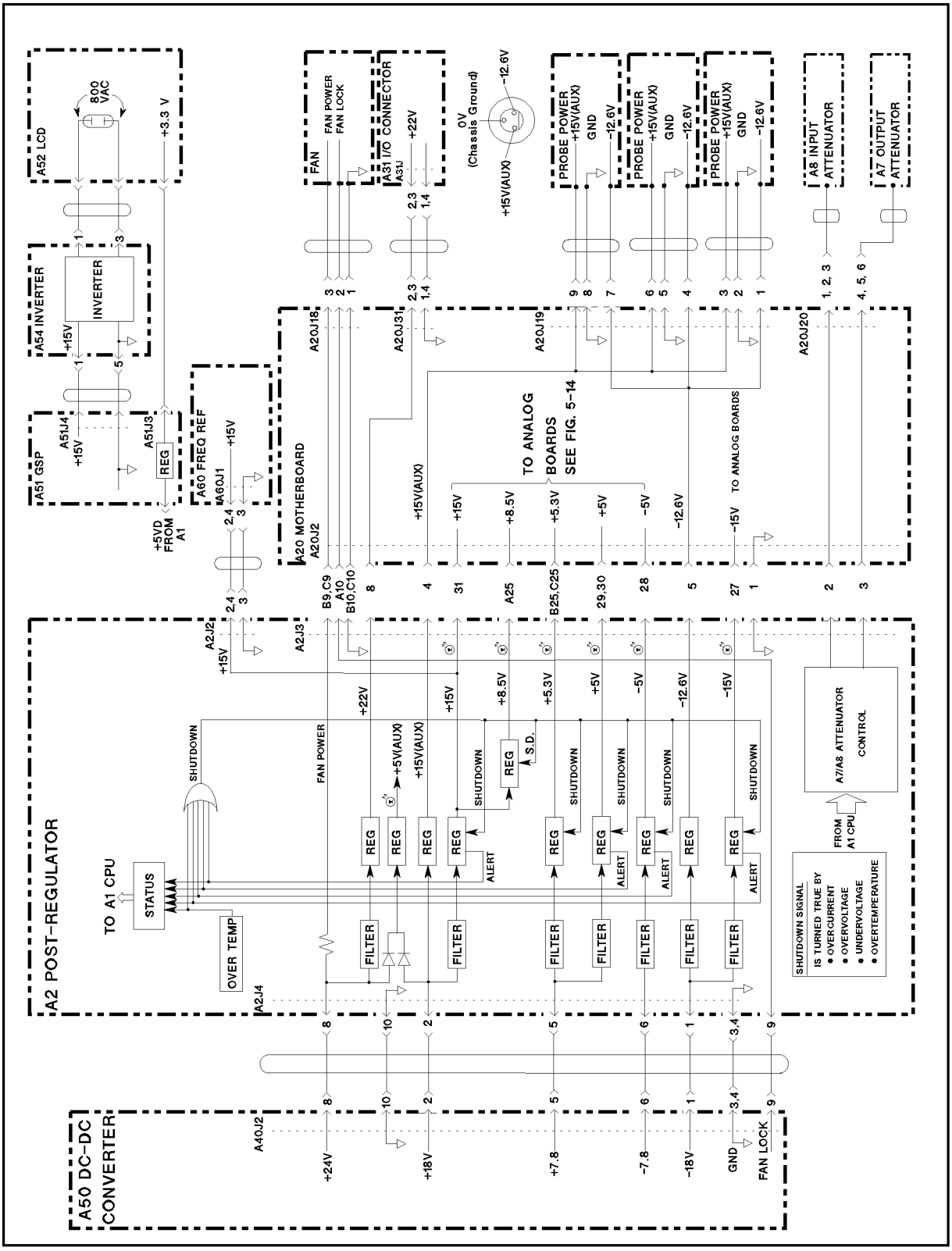
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CBS05003

Figure 5-12. Power Supply Block Diagram 1

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CBS05002

Figure 5-13. Power Supply Block Diagram 2

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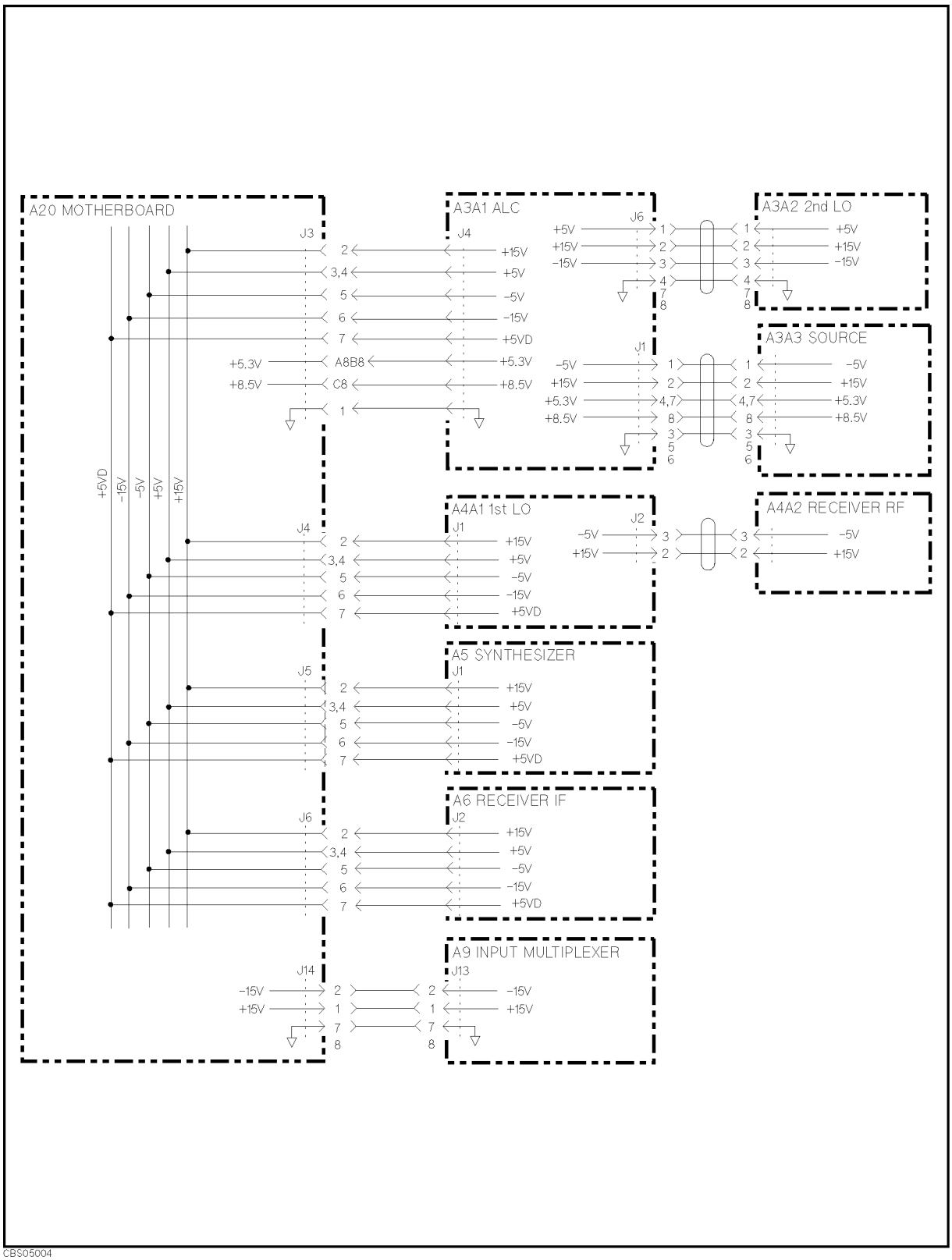


Figure 5-14. Power Supply Block Diagram 3

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6

Digital Control Troubleshooting

INTRODUCTION

Use this procedure only if you have followed the procedures in the *Troubleshooting* chapter, and believe the problem to be in the digital control group. This procedure is designed to let you identify the bad assembly within the digital control group in the shortest possible time. Whenever an assembly is replaced in this procedure, refer to the *Table of Related Service Procedures* in the *Post-Repair Procedures* chapter in this manual.

Figure 6-1 shows the digital control group in simplified block diagram form. The following assemblies make up the digital control group:

- A1 CPU
- A30 Front Keyboard
- A31 I/O Connector
- A32 I-BASIC Interface
- A51 GSP
- A52 LCD(Liquid Crystal Display)
- A53 FDD

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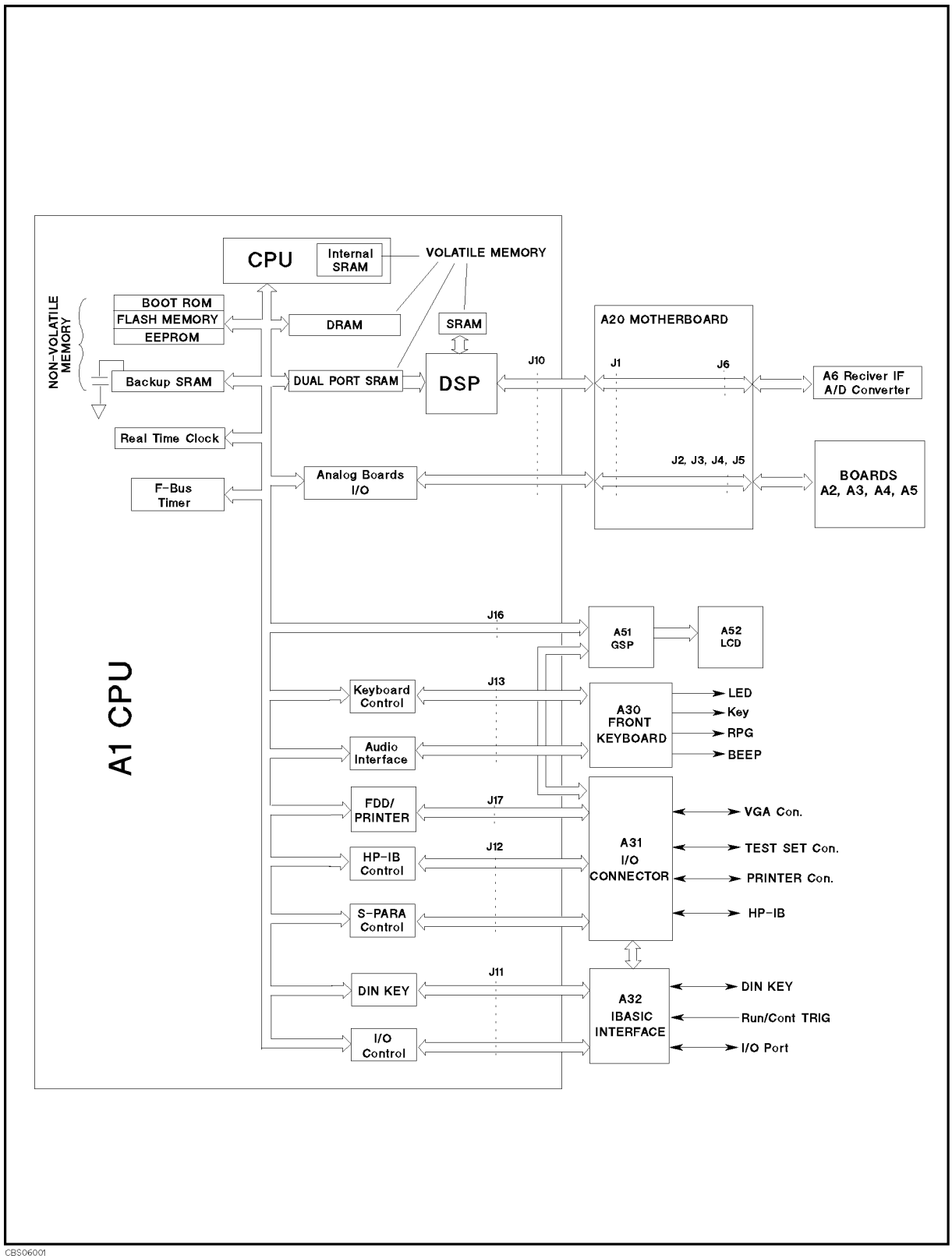


Figure 6-1. Digital Control Group Simplified Block Diagram

6-2 Digital Control Troubleshooting

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A1 CPU Replacement

When you replave a faulty A1 CPU with a new one, remove the EEPROM from the faulty A1 and mount the EEPROM on the replacement A1.

In the EEPROM, the correction constants data is stored after performing the Adjustment and Correction Constants procedures described in the chapter 2. The data may be valid for the new A1 CPU.

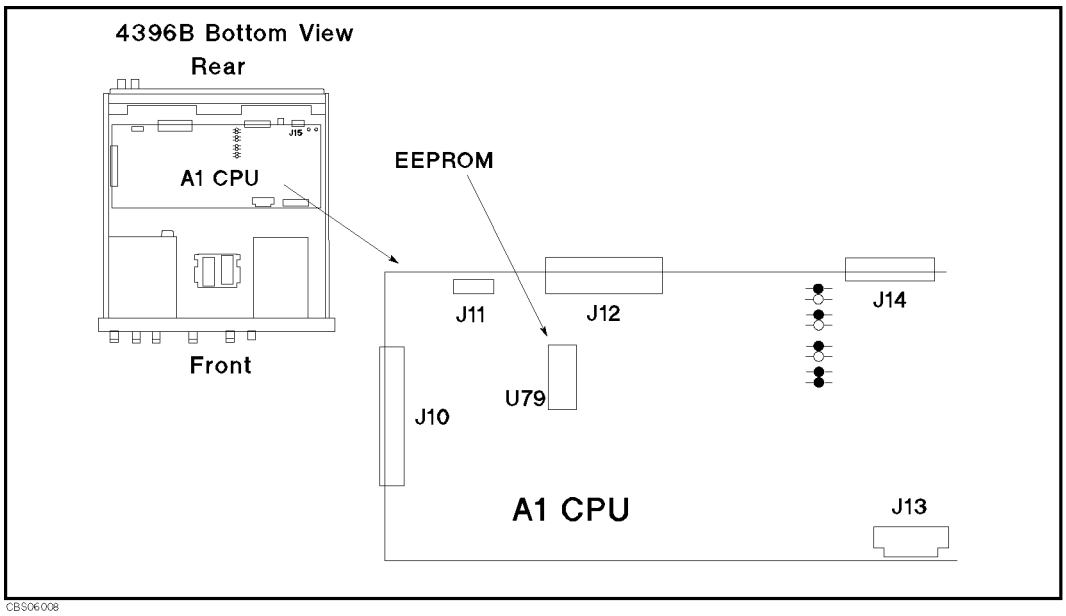


Figure 6-2. A1 EEPROM Location

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FIRMWARE INSTALLATION

No firmware is installed in new A1 CPU assembly. When you replace a faulty A1 CPU with a new one, perform the following steps to install the firmware into the A1 CPU.

Ordering the Firmware Diskette

A firmware diskette (3.5 inch) that contains the analyzer's firmware is required for the firmware installation. If you do not have a firmware diskette, you must order one. For ordering information, contact your nearest Agilent Technologies service center and provide the revision of the analyzer's firmware. The part number of the firmware diskette depends on the firmware revision. The firmware revision of the analyzer is indicated on the revision label attached on the rear panel as shown in Figure 6-3.

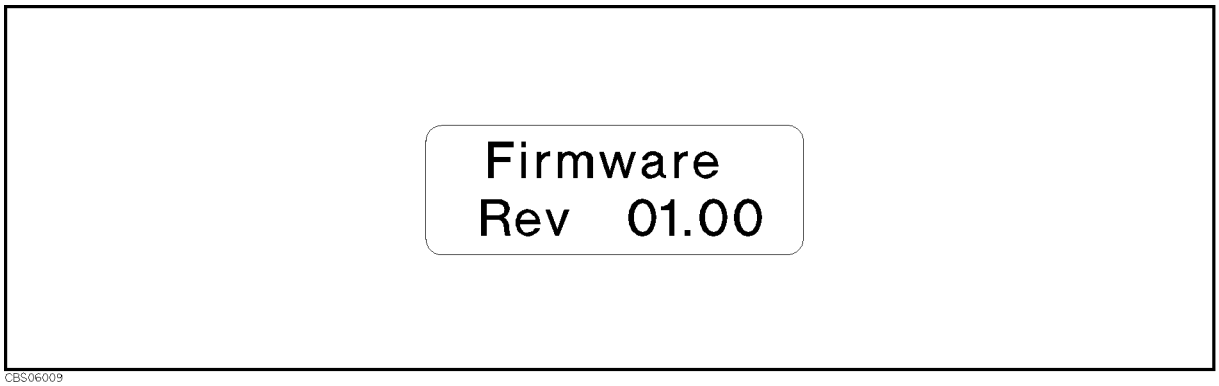


Figure 6-3. Firmware Revision Label

Installing the Firmware

Perform the following procedure to install the firmware into the analyzer.

1. Turn the analyzer power off.
2. Press both the (Start) and (Preset) keys. While pressing both keys, turn the analyzer power on.
3. Wait until the bootloader menu appears on the LCD as shown in Figure 6-4.

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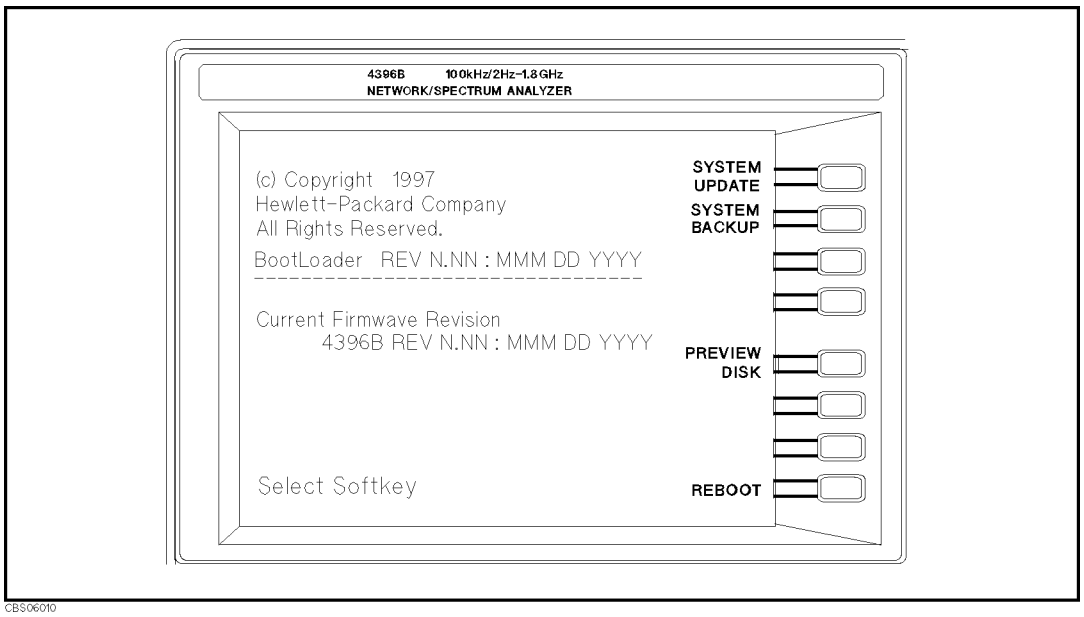


Figure 6-4. Bootloader Menu Display

4. Insert the firmware diskette into the floppy disk drive on the front panel.
5. Press `SYSTEM UPDATE` and `CONTINUE`. The analyzer displays "Loading From Disk" and starts the firmware installation.
6. Wait until the analyzer displays "Update Complete."
7. Press `REBOOT` or turn the analyzer power off and on. The analyzer starts the operation using the installed firmware.
8. Verify that no error message is displayed and that the revision displayed is that of the revision label.
   - In case of unexpected results, inspect the firmware diskette for any damage. Clean the built-in FDD and retry the procedure.

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START HERE

1. Check the Power On Sequence

See the INSPECT THE POWER ON SEQUENCE in the chapter 3 for checking the Power On Sequence.

Check the [Ch 1] and [Ch 2] Operations

a. Press [Ch 1] and [Ch 2] alternately.

b. Check that the two LEDs alternately light each time you press the keys.

- If both LEDs would not light, continue with the next *Check the A1 Eight LEDs*.
- If the two LEDs do not alternately light (the [Ch 1] LED is still lit even if pressing the [Ch 2]), the A1 CPU is probably faulty. Replace the A1 CPU.
- If the two LEDs alternately light each time you press the keys, the A1 CPU is probably working properly. Continue with the *TROUBLESHOOT THE A51 GSP AND A52 LCD* in this chapter.

Check the A1 Eight LEDs

There are eight LEDs on the A1 CPU. These LEDs should be in the pattern shown in Figure 6-5 at the end of the power on sequence. Perform the following procedure to check the A1 eight LEDs.

a. Turn the analyzer turn off.

b. Remove the bottom cover of the analyzer.

c. Turn the analyzer power on.

d. Look at the A1 eight LEDs. Some of the LEDs light during the power on sequence. At the end of the power on sequence, the LEDs should stay in the pattern shown in Figure 6-5. If the LEDs stay in the other pattern, the A1 CPU is probably faulty. Replace the A1 CPU.

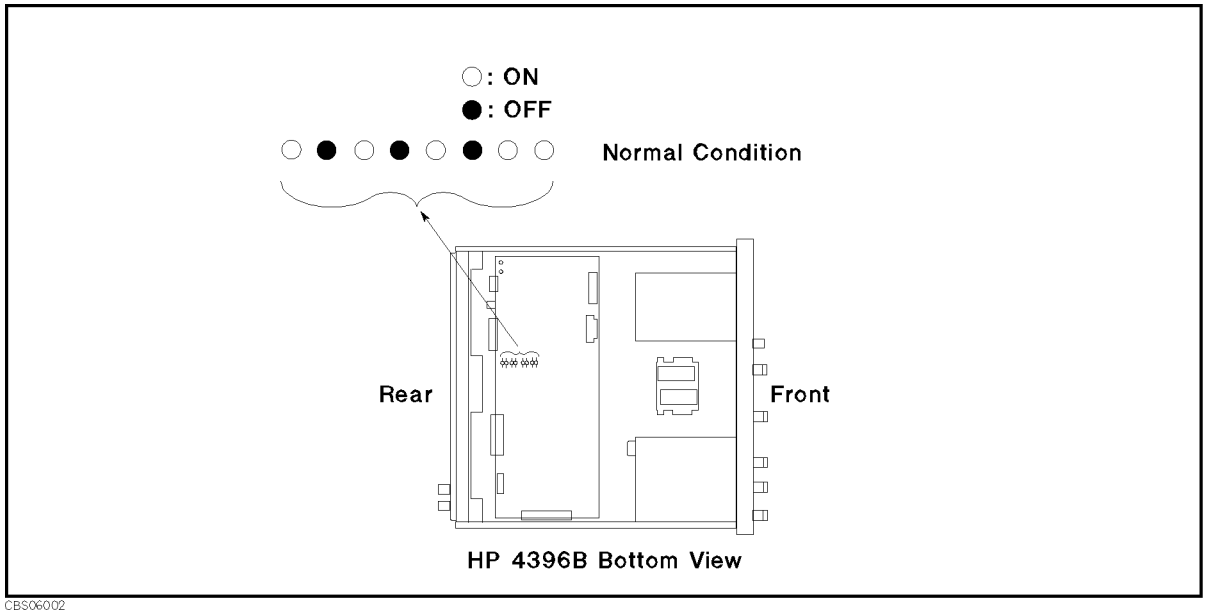


Figure 6-5. A1 Eight LEDs' Pattern

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2. Check Error Messages

Turn the analyzer power on. Check no error message appears on the LCD.

- If no error message is displayed, continue with the *Check A1 DRAM and Flash Memory* in this *START HERE*.
- If one of error messages listed below is displayed, follow the instruction described below. For the other message, see the *Error Messages* in Messages.

Error Messages	Instruction
POWER ON TEST FAILED	This indicates the power on selftest failed. Continue with the next *Check Power On Selftest*.
EEPROM CHECK SUM ERROR	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Rewrite all correction constants into the EEPROM. For the detailed procedure, See the *Adjustments and Correction Constants* chapter in this manual. If the rewriting is not successfully performed, replace the EEPROM and then rewrite the all correction constants into the new EEPROM.
Svc (Status Annotation)	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. See the instruction of the EEPROM CHECK SUM ERROR message.
POWER FAILED ON - - -	One or some of A2 power supplies, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V are displayed in - - - of the message. The displayed power supplies are shut down due to the trouble on the A2 post-regulator. Continue with the *Power Supply Troubleshooting* chapter.
POWER FAILED ON PostRegHot	This indicates A2 power supplies, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V, are shut down due to too hot heat sink on A2 post-regulator. Cool down the analyzer for about 30 minutes. Then turn the analyzer power on. If this message is still displayed, replace A2 post-regulator.
PHASE LOCK LOOP UNLOCKED	This indicates one or some of PLLs (phase lock loops) in the oscillators listed below is not working properly. These oscillators are checked in the internal test 0: ALL INT. Continue with the next *Check the Power On Selftest* in where the ALL INT test is executed.

Assembly	Oscillator
In the A5 Synthesizer	Reference Oscillator
	Step Oscillator
In the A3A2 2nd LO	2nd LO Oscillator
In the A4A1 1st LO	1st LO Oscillator
In the A6 Receiver IF	3rd LO Oscillator

Check the Power On Selftest

The analyzer performs the power on selftest every time when the analyzer is turned on. In the power on selftest, internal diagnostic tests 1, 4, 5, 6, 7, and 9 through 16 are executed sequentially. The first failed test indicates the most probable faulty assembly. For more information about the internal tests, see the *Service Menu Keys* chapter in this manual.

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If the power on selftest fails and "POWER ON TEST FAILED" message is displayed, execute the ALL INT test to identify the first failed test. Then refer to the Table 6-1 for further troubleshooting information.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (0), and (x1) to access the internal test 0: ALL INT.

b. Press EXECUTE TEST to execute the ALL INT test.

c. Wait until the test result, PASS or FAIL, is displayed.

d. Press the (⇧), (⇩) keys to find the first occurrence of a FAIL message for tests 1 and 4 through 16.

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Table 6-1.
Troubleshooting Information for Internal Diagnostic Test Failure

Test No.	First Failed Test	Troubleshooting Information
1	A1 CPU	Replace A1 CPU.
4	A2 POST REGULATOR	The power supply functional group is the most probable faulty group. See the *Power Supply Troubleshooting* chapter.
5	A6 A/D CONVERTER	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF. See the *Receiver Troubleshooting* chapter.
6	A5 REFERENCE OSC	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer. See the *Source Troubleshooting* chapter.
7	A5 FRACTIONAL N	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer. See the *Source Troubleshooting* chapter.
8	A5 STEP OSC	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer. See the *Source Troubleshooting* chapter.
9	A4A1 1ST LO OSC	The A4A1 1st LO OSC is the most probable faulty board. Replace the A4A1 1st LO. See to the *Source Group Troubleshooting* chapter.
10	A3A2 2ND LO OSC	The A3A2 2nd LO OSC is the most probable faulty board. Replace the A3A2 2nd LO. See the *Source Group Troubleshooting* chapter.
11	A3A1 DIVIDER	The A3A1 ALC is the most probable faulty board. Replace the A3A1 ALC. See the *Source Group Troubleshooting* chapter.
12	A6 3RD LO OSC	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF. See the *Receiver Group Troubleshooting* chapter.
13	A3A1 SOURCE OSC	The A3A1 ALC is the most probable faulty board. Replace the A3A1 ALC. See the *Source Group Troubleshooting* chapter.
14	A6 3rd IF DC OFFSET	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF. See the *Receiver Troubleshooting* chapter.
15	A6 SEQUENCER	The A6 receiver IF is the most probable board. Replace the A6 receiver IF. See the *Receiver Troubleshooting* chapter.
16	A3A1 ALC	The A3A1 ALC is the most probable faulty board. Replace the A3A1 ALC. See the *Source Group Troubleshooting* chapter.

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3. Check the A1 DRAM and Flash Memory

The A1 DRAM and flash memory are tested on the sequence to access the bootloader menu. For the bootloader menu, see the *Service Key Menus* chapter.

Perform the following procedure to verify the A1 DRAM and flash memory.

a. Turn the analyzer power off.

b. Push two keys (Start) and (Preset). With keeping the two keys pushed down, turn the analyzer power on.

c. Wait for the display shown in Figure 6-6 appears on the LCD.

d. Check no error message displayed on the LCD.

- If no error message is displayed, the A1 DRAM and flash memories are verified. Continue with the next *Check the A1 Volatile Memory* .
- If an error message is displayed or the display shown in Figure 6-6 does not appear, the A1 CPU is probably faulty. Replace the A1 CPU.

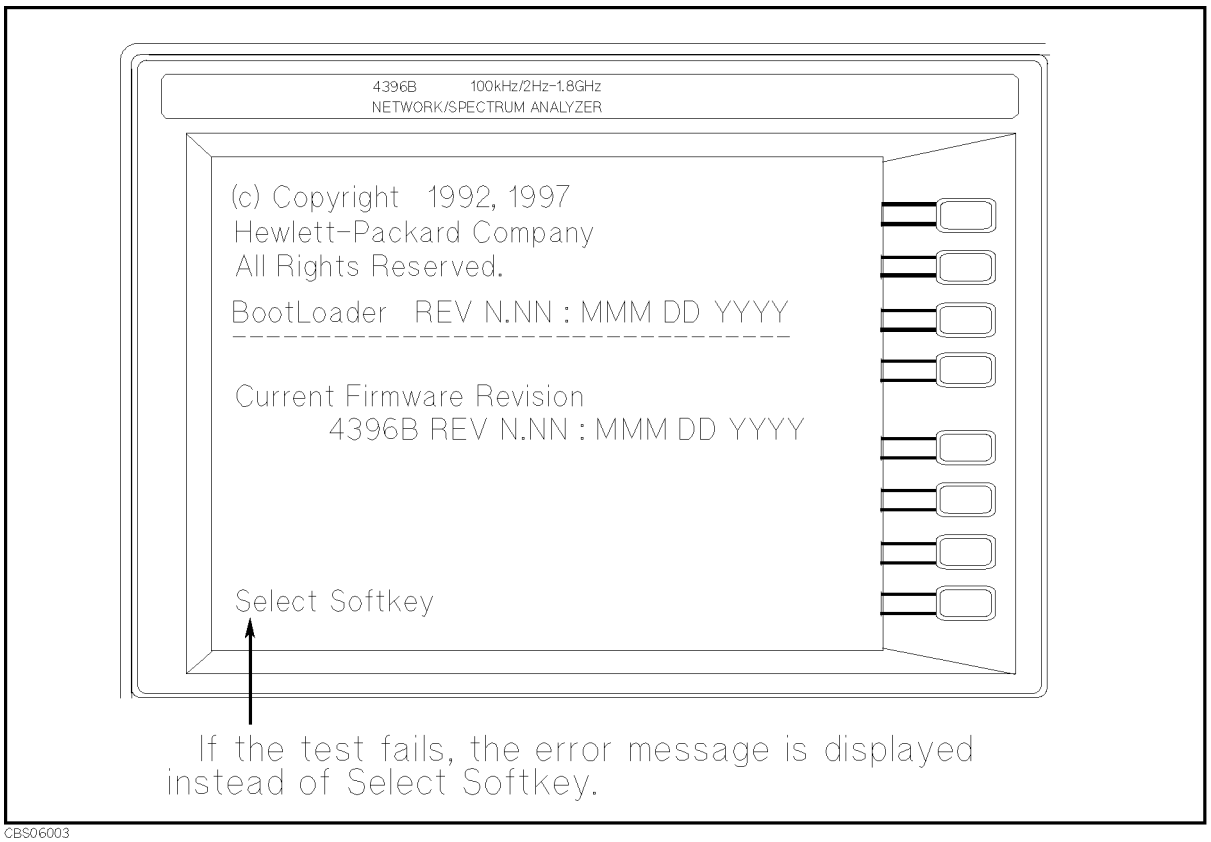


Figure 6-6. Bootloader Display

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4. Check the A1 Volatile Memory

a. Turn the analyzer power on.

b. Press (System), SERVICE MENU, TESTS, (2), (x1), EXECUTE TEST to run the internal test 2: A1 VOLATILE MEMORY.

c. Check no error message displayed. At the end of this test, the analyzer returns the control settings to the default values (power on reset). If the test fails, the analyzer displays an error messages for a few second before returning to the defaults.

- If no error message is displayed, the A1 volatile memories are verified. Continue with the next *Check the A30 Front Keyboard*.
- If one of error messages listed below is displayed, the A1 CPU is faulty. Replace the A1 CPU.

  CPU INTERNAL SRAM R/W ERROR
  DSP SRAM R/W ERROR
  DUAL PORT SRAM R/W ERROR
  CPU BACKUP SRAM R/W ERROR

5. Check the A30 Front Keyboard

The A30 front keyboard can be checked using the external test 17: FRONT PANEL DIAG.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (7), (x1), EXECUTE TEST to run the external test 17.

b. Press all of the front panel keys. The pressed abbreviated key name should be displayed at a key pressed. When you rotate the RPG knob, the RPG tuned direction (CW or CCW) and its response speed (SLOW, MID, FAST) should be displayed. So you can check every key on the A30 Keyboard except for (PRESET). (If you want to exit this test, press (PRESET).)

- If one or more keys seems to be defective, replace the A30 front keyboard.
- If all keys seem to be good, the A30 front keyboard is verified. Continue with the next *Check the A53 FDD*.

6. Check the A53 FDD

The A53 FDD (Flexible Disk Drive) can be checked using the external test 18: DISK DR FALUT ISOL'N.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (8), (x1), EXECUTE TEST to run the external test 18.

b. As the analyzer instructs, insert a flexible disk into FDD. Use a formatted but blank flexible disk, otherwise the data on the disk will be overwritten by this test. Then press CONT.

c. Check the test result, PASS or FAIL, that is displayed at the end of the test.

- If this test fails, replace the A53 FDD.

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7. Check the A32 I-BASIC Interface and the mini DIN Keyboard

The mini DIN external keyboard is connected to the A32 I-BASIC I/O connector, and is used to develop programs.

If the external keyboard of the I-Basic is not working, perform the following procedure to verify the keyboard.

Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (x1), EXECUTE TEST to run the internal test 1: A1 CPU.

- If the internal test 1 passes, the HP HIL driver circuit on the A1 CPU is probably working. Inspect cables between the external keyboard and the A1 CPU through the A32 I-BASIC interface. If the cable is good, replace the external keyboard.
- If the internal test 1 fails, replace the A1 CPU.

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TROUBLESHOOT THE A51 GSP and A52 LCD

Use this procedure when the LCD(Liquid Crystal Display) is unacceptable, or not being bright.

1. Run the Internal Test 3: A51 GSP

The A51 GSP can be checked using the internal test 3: A51 GSP. If the test fails, the [Ch 1] and [Ch 2] LEDs blink several time and a few beeps sound at the end of the test. Then the analyzer returns the control settings to the power-on default setting values.

a. Press [PRESET], [SYSTEM], SERVICE MENU, TESTS, [3], [x1], EXECUTE TEST to run the internal test 3. When this test starts, [Ch 1] LED and [Ch 2] LED are turned off.

b. Check the [Ch 1] and [Ch 2] LEDs and the beeps at the end of the test.

- If no beep sound and the LEDs don't blink, the A51 GSP is probably working. Continue with the next *Check the Two LEDs on A51 GSP.*
- If a beep sounds and the LEDs blink one time, the A51 GSP chip is faulty. Replace the A51 GSP.
- If two beep sound and the LED blinks two time, the A51 GSP's DRAM is faulty. Replace the A51 GSP.
- If three beep sound and the LED blinks three time, the A51 GSP's VRAM is faulty. Replace the A51 GSP.

2. Check the A52 LCD(Liquid Crystal Display)

The A52 LCD can be tested using the internal test 48 to 52.

a. Press [PRESET], [SYSTEM], SERVICE MENU, TESTS, [4], [8], [x1], EXECUTE TEST CONTINUE to run the internal test 48, and run the other tests with the same manner.

b. If any defects on the LCD, replace the LCD.

c. If no correct patterns are displayed, check the A54 Inverter.

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7

Source Group Troubleshooting

INTRODUCTION

Use these procedures only if you have read the *Isolate Faulty Group Troubleshooting* chapter and you believe the problem is in the source group.

This procedure is designed to let you identify the bad assembly within the source group in the shortest possible time. Whenever an assembly is replaced in this procedure, refer to Table 13-1 *Post Repair Procedures* in the *Post-Repair Procedures* chapter.

Figure 7-1 shows a simplified block diagram of the source group. The source group consists of the following assemblies:

- A5 Synthesizer
- A4A1 1st LO
- A3A1 ALC
- A3A2 2nd LO
- A3A3 Source
- A7 Output Attenuator
- A60 High Stability Frequency Reference (Option 1D5)

Note



Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the analyzer to warm up for at least 30 minutes before you perform any procedure in this chapter.

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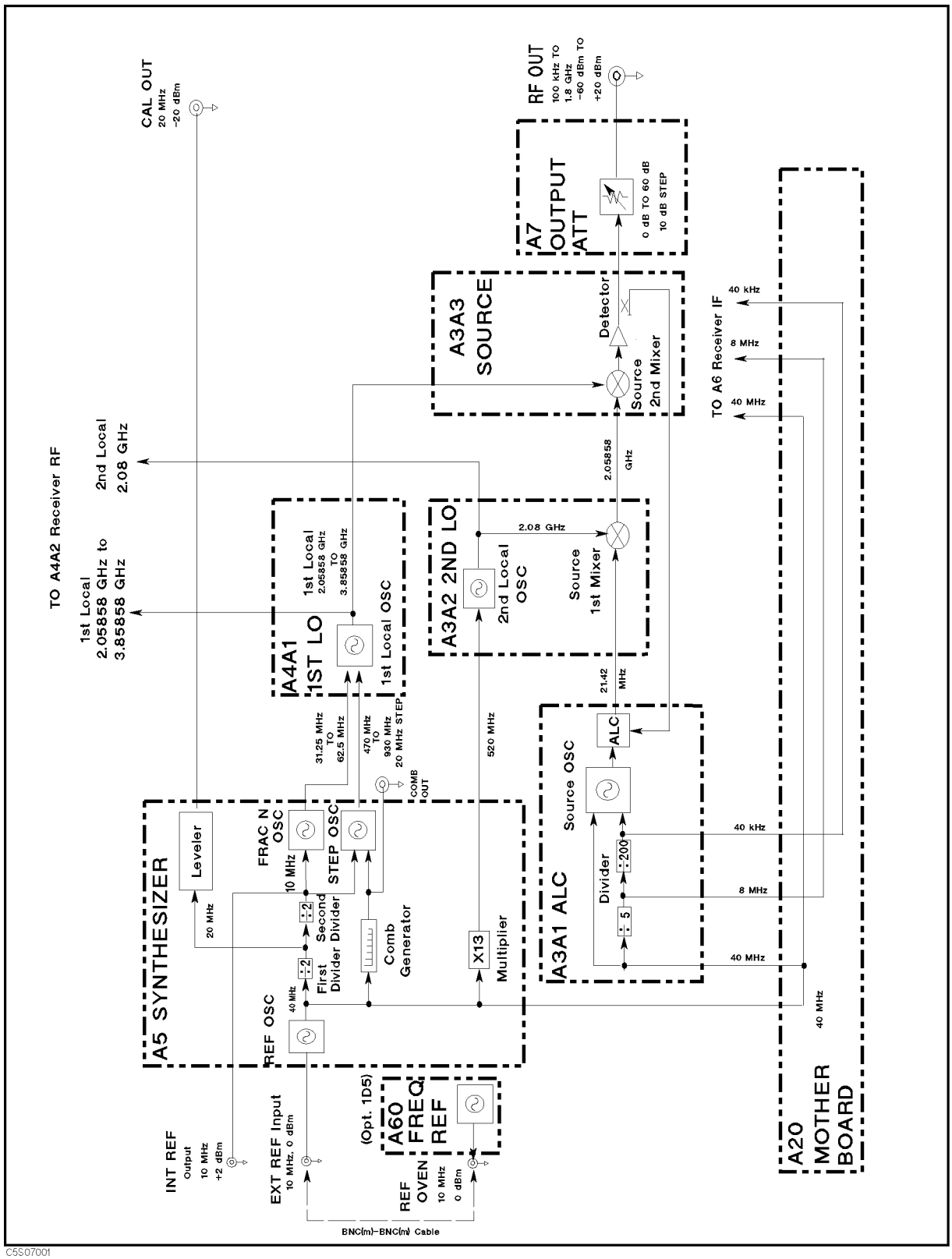


Figure 7-1. Source Group Block Diagram

7-2 Source Group Troubleshooting

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SOURCE GROUP TROUBLESHOOTING SUMMARY

This overview summarizes the sequence of checks included in this chapter. Experienced technicians may save time by following this summary instead of reading the entire procedure. Headings in this summary match the headings in the procedure.

Start Here

1. Run internal test 11. If the test fails, check the CAL OUT signal. If the CAL OUT signal is good, replace the A3A1 ALC. If the CAL OUT signal is bad, replace the A5 Synthesizer.
2. Run internal test 5. If the test fails, replace the A6 Receiver IF in the receiver group.
3. Run internal test 6. If the test fails, replace A5.
4. Run internal test 7. If the test fails, replace A5.
5. Run internal test 8. If the test fails, replace A5.
6. Run internal test 9. If the test fails, replace the A4 1st LO/Receiver RF.
7. Run internal test 13. If the test fails, replace the A3A1 ALC.
8. Run internal test 16. If the test fails, replace A3A1.
9. Run internal test 10. If this test fails, replace the A3A2 2nd LO.
10. Run external test 20. If this test fails, check the A7 Output Attenuator control signals in accordance with the *Check A7 Output Attenuator Control Signals* section in this chapter. If the control signals are good, replace A7. If they are bad, replace the A2 post-regulator.

Check A5 Synthesizer Outputs

1. Check the CAL OUT signal. If it is bad, replace A5.
2. Check the INT REF signal. If it is bad, replace A5.
3. Check the FRAC N OSC signal. If it is bad, replace A5.
4. Check the STEP OSC signal. If it is bad, replace A5.
5. Check the 520 MHz signal. If it is bad, replace A5.
6. Check the EXT REF operation. If it is bad, replace A5.

Check A4A1 1st LO Outputs

1. Check the 1st local oscillator signal at A4A1J3. If it is bad, replace A4.
2. Check the 1st local oscillator signal at A4A1J4. If it is bad, replace A4.

Check an A3A1 ALC Output

1. Check the 21.42 MHz signal. If it is bad, replace A3A1.

Check A3A2 2nd LO Outputs

1. Check the 2nd local oscillator signal. If it is bad, replace A3A2.
2. Check the 2.05858 GHz signal. If it is bad, replace A3A2.

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Check an A3A3 Source Output

1. Check the A3A3 RF signal. If it is bad, replace A3A3.

Check A7 Output Attenuator Control Signals

1. Check the A7 control signals If the control signals are good, replace A7. If the control signals are bad, replace A2.

Check A60 High Stability Frequency Reference (Option 1D5)

1. Check the REF OVEN signal. If it is bad, replace A60.
2. Perform the *10 MHz Reference Oscillator Frequency Adjustment*. If the adjustment fails, replace A60.

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START HERE

The following procedure verifies the operation of each assembly in the source group by using the 4396B's self-test functions (internal and external tests). For detailed information about the self-test functions, see the *Service Key Menus*.

In this procedure, the A3A1's divider and the A6's A/D converter (receiver group) are verified first. This is done because the internal tests use the A/D converter to measure voltages at DC bus nodes within the source group. Also, the A3A1's divider output is used to generate the A/D converter's control signals.

Perform the following steps to troubleshoot the source group:

1. Press (Preset), (System), SERVICE MENUS, TESTS, (1), (1), (x1), EXECUTE TEST to run internal test 11: A3A1 DIVIDER.
   - If the test fails, there is a possibility that the A5 synthesizer is faulty. This possibility exists because the A3A1 divider obtains the 40 MHz reference signal from A5. Perform the *1. Check the CAL OUT Signal* procedure in the *Check A5 Synthesizer Outputs* section. This procedure verifies the 40 MHz reference signal. If the CAL OUT signal is good, A3A1 is probably faulty. Replace A3A1. If the CAL OUT signal is bad, replace A5.
2. Press (5), (x1), EXECUTE TEST to run internal test 5: A6 A/D CONVERTER. If the test fails, replace A6 in the receiver group.
3. Press (6), (x1), EXECUTE TEST to run internal test 6: A5 REFERENCE OSC. If the test fails, replace A5.
4. Press (7), (x1), EXECUTE TEST to run internal test 7: A5 FRACTIONAL N OSC. If the test fails, replace A5.
5. Press (8), (x1), EXECUTE TEST to run internal test 8: A5 STEP OSC. If the test fails, replace A5.
6. Press (9), (x1), EXECUTE TEST to run internal test 9: A4A1 1st LO OSC. If the test fails, replace A4.
7. Press (1), (3), (x1), EXECUTE TEST to run internal test 13: A3A1 SOURCE OSC. If the test fails, replace A3A1.
8. Press (1), (6), (x1), EXECUTE TEST to run internal test 16: A3A1 ALC. If the test fails, A3A1, A3A2, or A3A3 is probably faulty. Verify A3A1, A3A2, and A3A3 in accordance with the *Check an A3A1 ALC Output*, *Check A3A2 2nd LO Outputs*, and *Check an A3A3 Source Output* sections in this chapter.
9. Press (1), (0), (x1), EXECUTE TEST to run internal test 10: A3A2 2ND LO OSC. If the test fails, replace A3A2.
10. Press (2), (0), (x1), EXECUTE TEST to run internal test 20: OUTPUT ATTENUATOR. Then connect the equipment as shown in Figure 7-2 and press CONTINUE to start the test. If the test fails, the A7 Output Attenuator is probably faulty. Perform the procedure provided in the *A7 Output Attenuator Control Signals* section to confirm that A7 is faulty.

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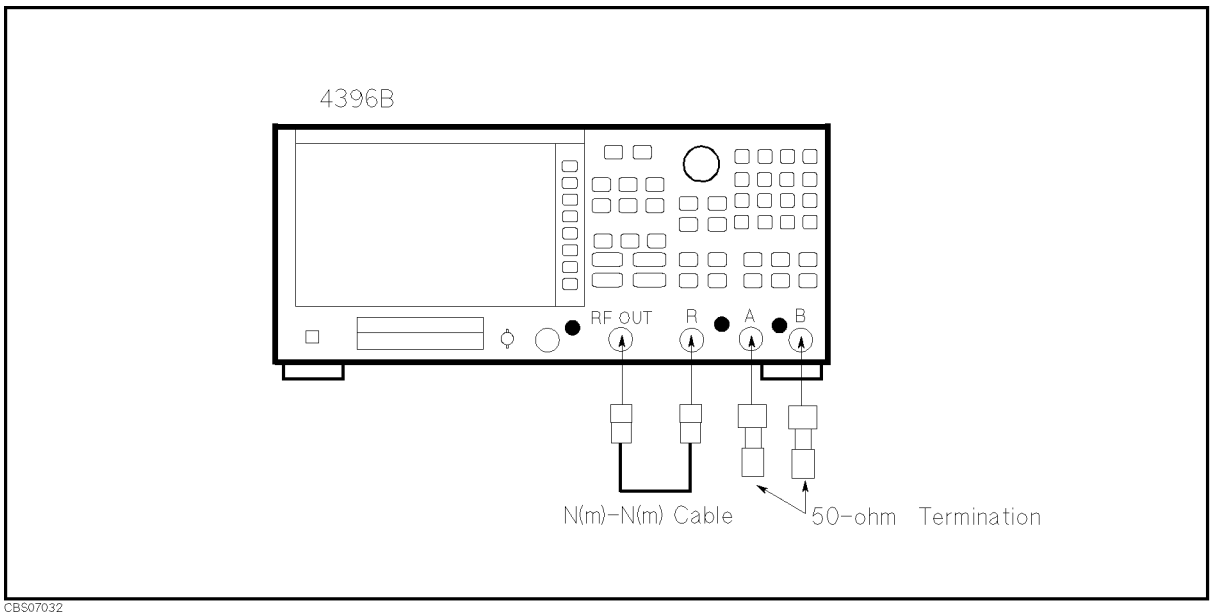


Figure 7-2. External Test 20 Setup

If all the tests listed above pass and you still believe that the problem is in the source group, verify all the outputs of each assembly in the source group. The procedures to do this are provided in the following sections.

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CHECK A5 SYNTHESIZER OUTPUTS

The output signals from the A5 Synthesizer are listed below. The input signal to A5 is the external reference signal from the EXT REF connector. See Figure 7-1. If all the output signals and the 4396B operation using the EXT REF input signal are good, A5 is probably good.

- CAL OUT signal on the front panel
- INT REF signal on the rear panel
- FRAC N OSC signal going to A4A1
- STEP OSC signal going to A4A1
- 520 MHz signal going to A3A2
- 40 MHz signal going to A3A1 and A6

Perform the following procedures sequentially to verify all the signals listed above and to verify the 4396B operation when the EXT REF signal is used.

In these procedures, the 40 MHz signal is not verified because it is indirectly verified if the CAL OUT signal is good. The signals are observed using test equipment and the 4396B self-test functions. For detailed information about the self-test functions, see the *Service Key Menus*.

1. Check the CAL OUT Signal

The front-panel CAL OUT signal (20 MHz, −20 dBm ± 0.4 dB) is derived from the 40 MHz reference signal through the first 1/2 divider and the leveler. See the A5 Synthesizer block in Figure 7-1.

Perform the two adjustments listed below to verify the CAL OUT signal's frequency and level (see the *Adjustments and Correction Constants* chapter).

a. 40 MHz Reference Oscillator Frequency Adjustment
b. CAL OUT Level Adjustment

- If both adjustments are successfully completed, the CAL OUT signal is verified. Therefore, the reference oscillator, the first 1/2 divider, and the leveler are verified. Continue with *2. Check the INT REF Signal.*
- If one or both of the adjustments are difficult or cannot be completed due to unstable frequency or level conditions, continue with the *Check the CAL OUT's Spurious* procedure that follows this procedure.
- If both adjustments fail, inspect the cable and connections between the CAL OUT connector and A5J5. See Figure 7-3 for the location of A5J5. If the cable and connections are good, replace A5.

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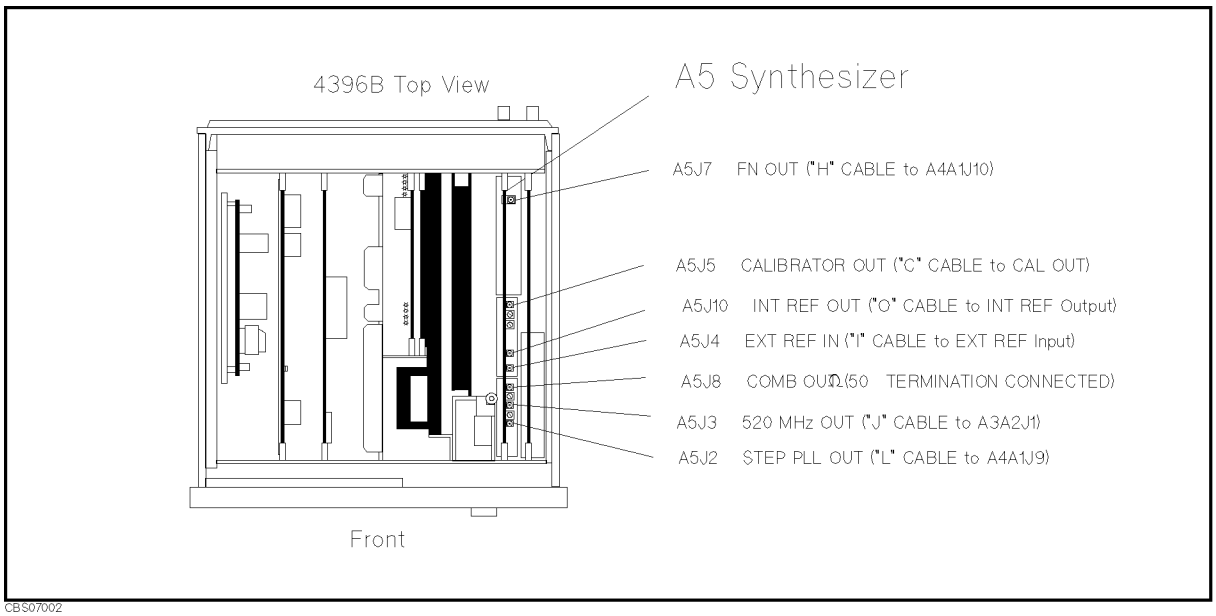


Figure 7-3. A5 Connector Locations

Check the CAL OUT's Spurious

Only perform the CAL OUT's spurious level check if the adjustments in the previous procedure were difficult or could not be completed.

a. Connect the equipment as shown in Figure 7-4.

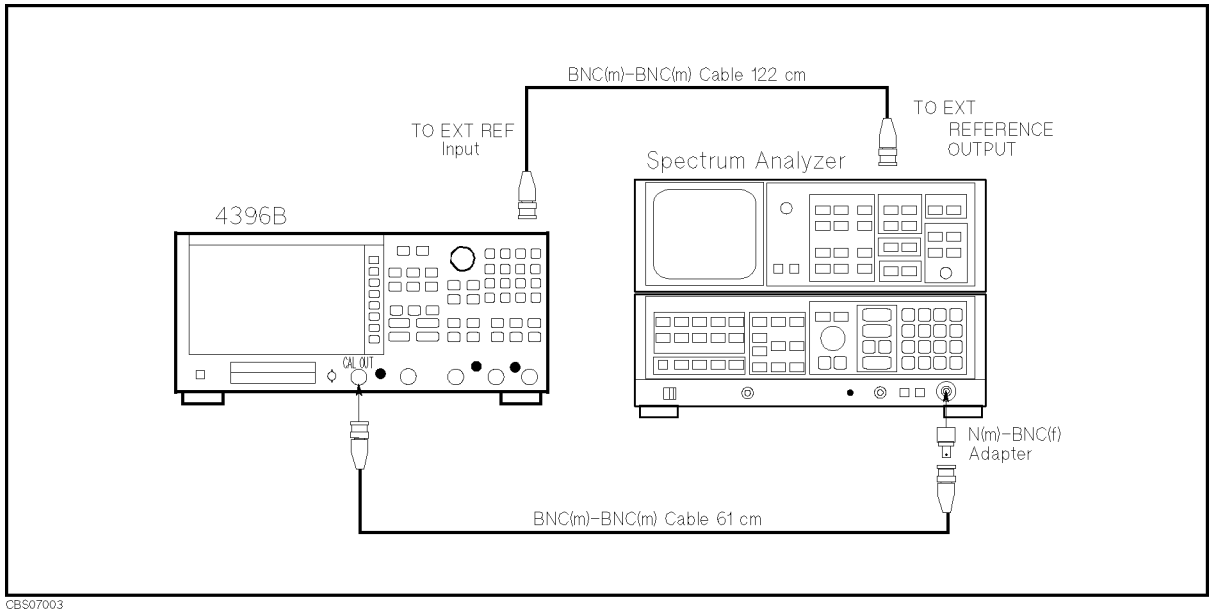


Figure 7-4. CAL OUT Test Setup

b. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Start Frequency	1 MHz

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Stop Frequency 80 MHz

c. Check that the spurious levels are lower than −45 dBc. The CAL OUT signal should be as shown in Figure 7-5.

- If the signal is good, continue with *2. Check the INT REF Signal.*
- If the signal is bad, replace the A5 Synthesizer.

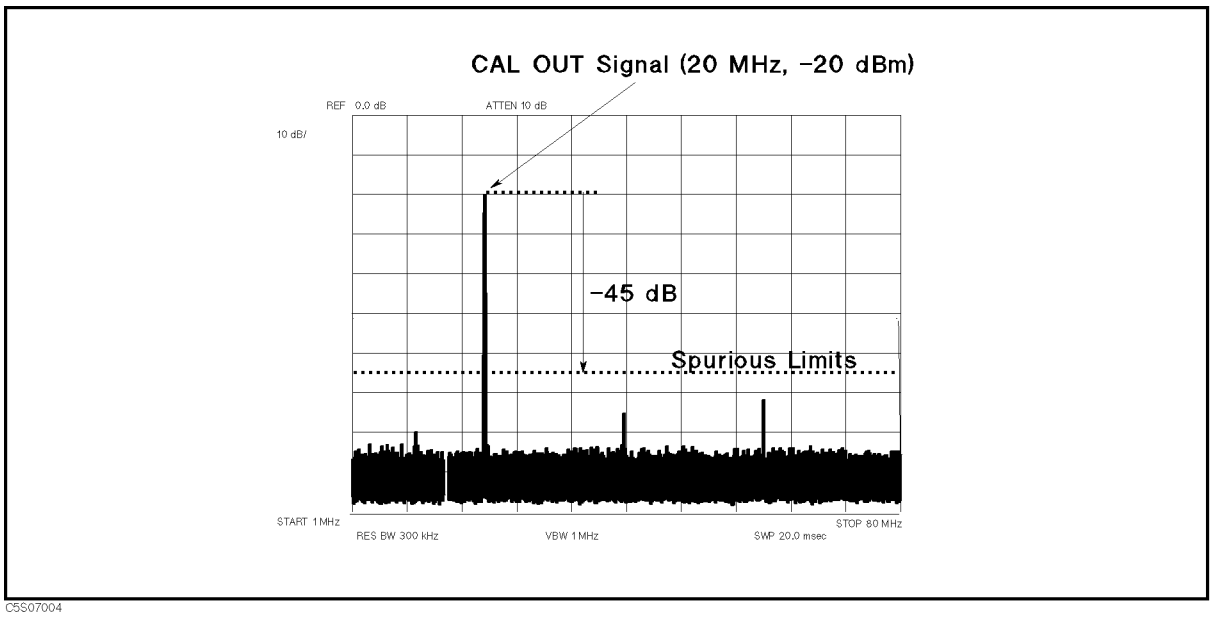


Figure 7-5. Typical CAL OUT Signal

2. Check the INT REF Signal

The INT REF signal (10 MHz, +2 dBm typical) on the rear panel is derived from the 40 MHz reference signal through the first and second 1/2 dividers. See the A5 Synthesizer block in Figure 7-1. Perform the following steps to verify the INT REF signal's frequency and level:

a. On the 4396B, press the following keys to measure the INT REF frequency by using the bus measurement function:

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER OF POINTS, (2), (x1), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (5), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

The frequency bus measures the INT REF frequency (10 MHz) through a 1/4 divider. Therefore, the measured value is 2.5 U (10 MHz divided by 4). The unit "U" in the frequency bus measurement is equivalent to MHz.

b. Check that the marker reading is 2.5 U ± 0.01 U.

- If the marker reading is good, continue with the next step.
- If the marker reading is bad, the second 1/2 divider in A5 is probably faulty. Replace A5.

c. Connect the equipment as shown in Figure 7-6.

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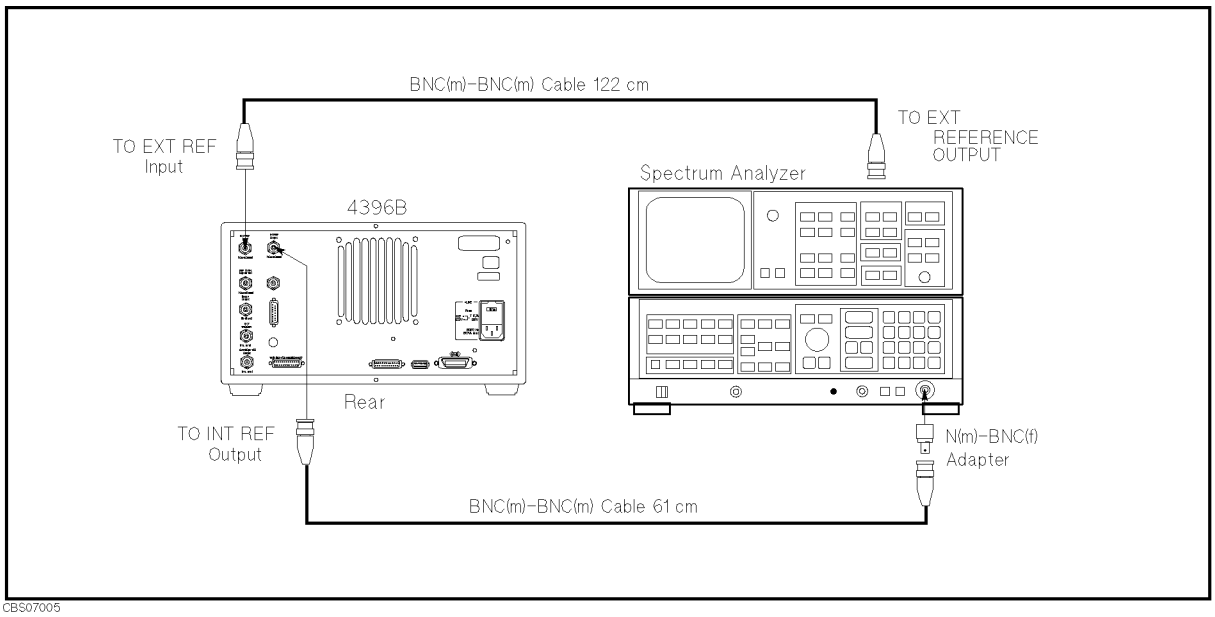


Figure 7-6. INT REF Test Setup

d. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	10 MHz
Span	15 MHz
Reference Level	10 dBm

e. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the INT REF signal.

f. Check that the frequency is approximately 10 MHz and the level is +2 dBm ± 4 dB. The INT REF signal should be as shown in Figure 7-7.

- If the INT REF signal is good, continue with *3. Check the FRAC N OSC Signal.*
- If the INT REF signal is bad, inspect the cable and connections between the INT REF connector and A5J10. See Figure 7-3 for the location of A5J10. If the cable and connections are good, replace A5.

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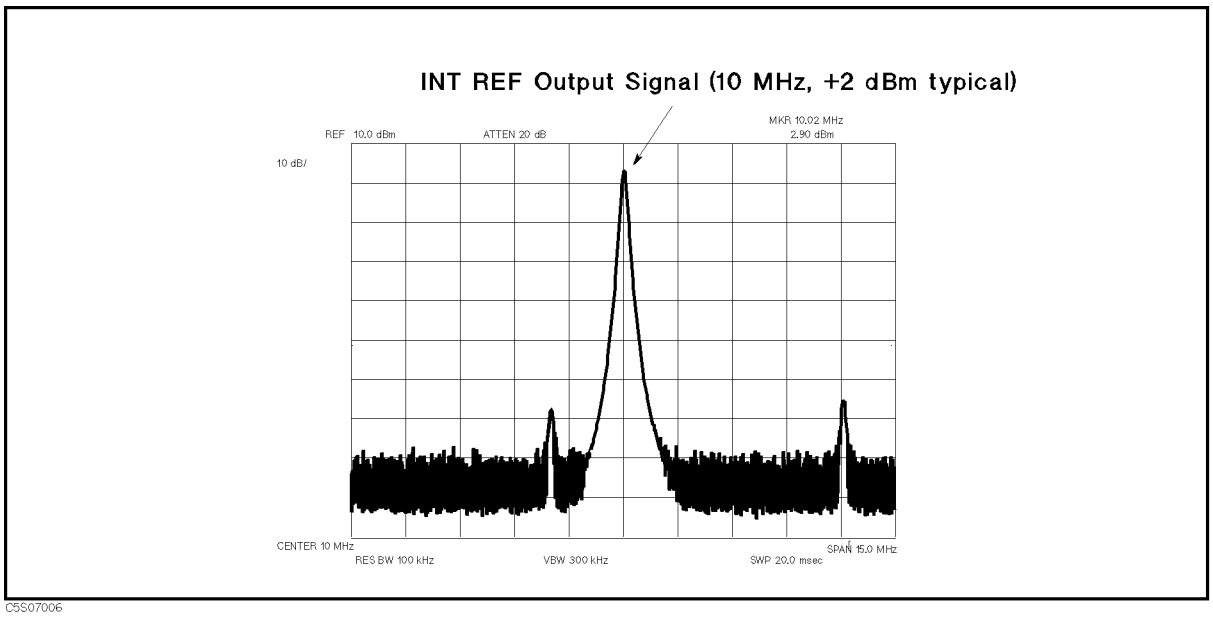


Figure 7-7. Typical INT REF Signal

3. Check the FRAC N OSC Signal

The fractional N oscillator (FRAC N OSC) generates the signal for frequencies from 31.25 MHz to 62.5 MHz. The signal level must be +4.25 dBm ± 5 dB over the frequency range. Perform the following steps to verify the frequency and level of the FRAC N OSC signal:

a. Press (Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset).

During this procedure, the start and stop frequencies are set to 0 Hz and 1.8 GHz, respectively. These start and stop settings sweep the FRAC N OSC frequency from 32.1653125 MHz (at the start frequency 0 Hz) to 60.2903125 MHz (at the stop frequency 1.8 GHz).

b. Press the following keys to measure the FRAC N OSC frequency by using the bus measurement function:

(System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (4), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

The frequency bus measures the FRAC N OSC frequency through a 1/16 divider. Therefore, the measured value is 1/16 of the actual frequency. For example, the measured value at the start frequency 0 Hz is 2.0103 U (32.1653125 MHz divided by 16). The unit "U" in the frequency bus measurement is equivalent to MHz.

c. Wait for the completion of the sweep.

d. Perform the following steps to verify the frequencies of the FRAC N OSC signal:

i. Press (Marker), (0), (x1) to move the marker to the start frequency 0 Hz. Then check that the marker reading is 2.0103 U ± 0.01 U.
ii. Press (Marker), (1), (.), (8), (G/n) to move the marker to the stop frequency 1.8 GHz. Then check that the marker reading is 2.8892 U ± 0.01 U.
iii. Check that the displayed trace is straight (see Figure 7-8).

■ If the marker readings and the trace are good, continue with the next step.

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■ If one (or more) of the marker readings or the trace is bad, the FRAC N OSC is probably faulty. Replace A5.

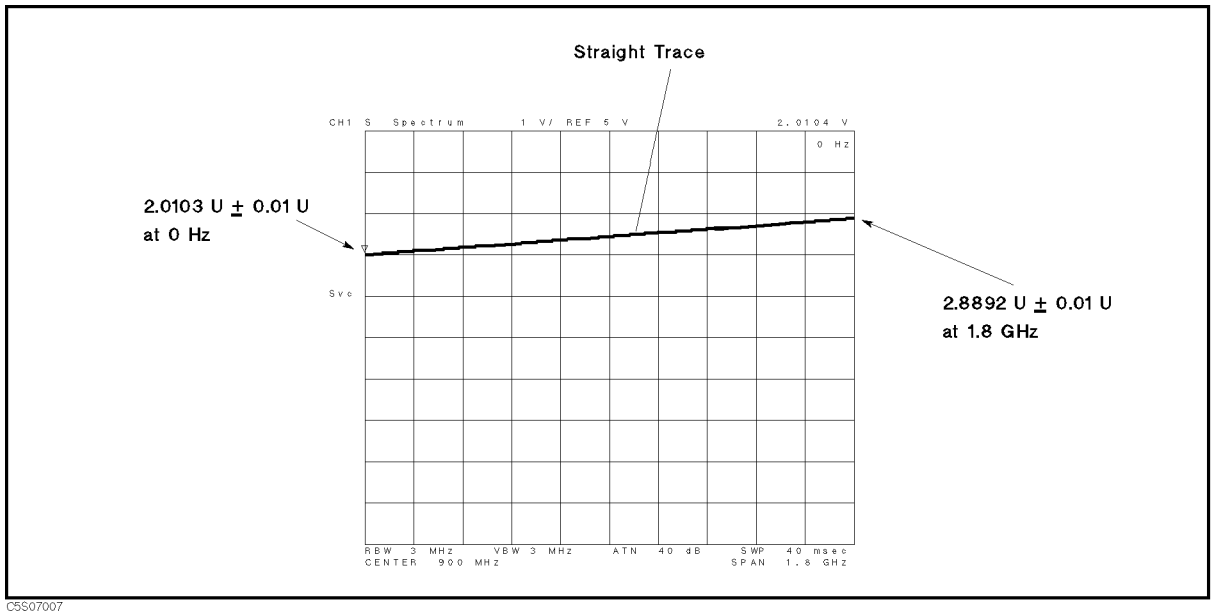


Figure 7-8. Typical FRAC N OSC Signal in Frequency Bus Measurement

e. Remove the "H" cable from the A5J7 "FN OUT" connector. Then connect the equipment as shown in Figure 7-9.

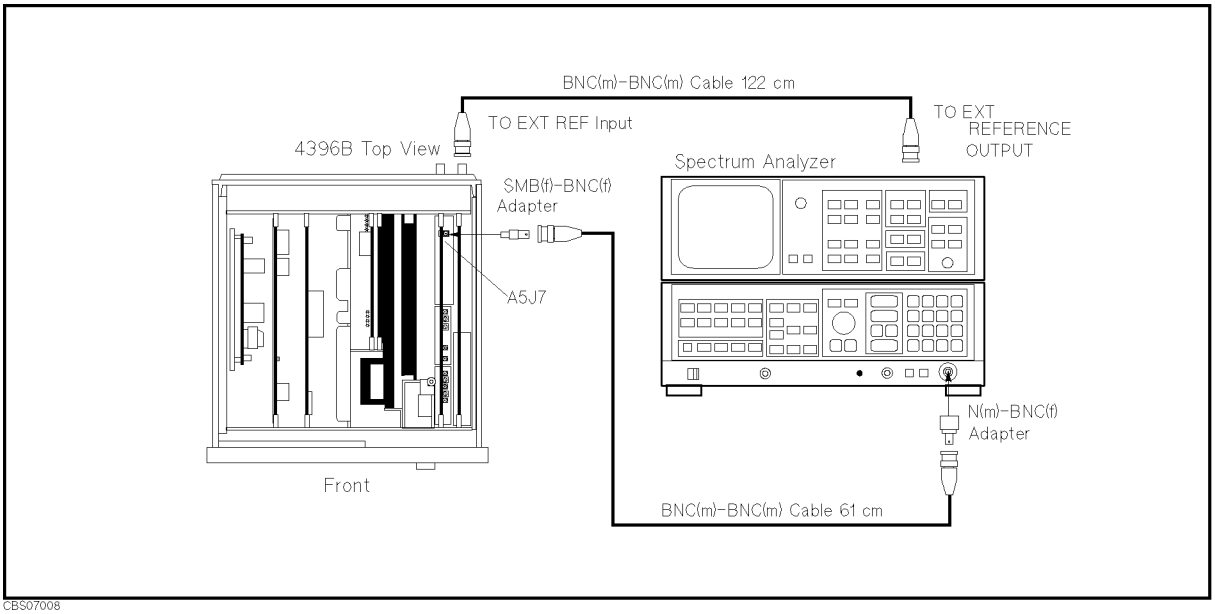


Figure 7-9. FRAC N OSC Signal Level Test Setup

f. On the 4396B, press Preset, Sweep, SWEEP TIME, 2, 0, x1.

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g. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	Settings
Start Frequency	30 MHz
Stop Frequency	70 MHz
Reference Level	10 dBm
Max Hold	ON

h. On the 4396B, press (Trigger), MEASURE RESTART. Wait for the completion of the sweep.

i. Check that the signal level is +4.5 dBm ± 5 dB over the frequency range of 32.165 MHz to 60.290 MHz. The displayed trace should be as shown in Figure 7-10.

- If the signal is good, the FRAC N OSC is working. Continue with the next step.
- If the signal is bad, the FRAC N OSC is faulty. Replace A5.

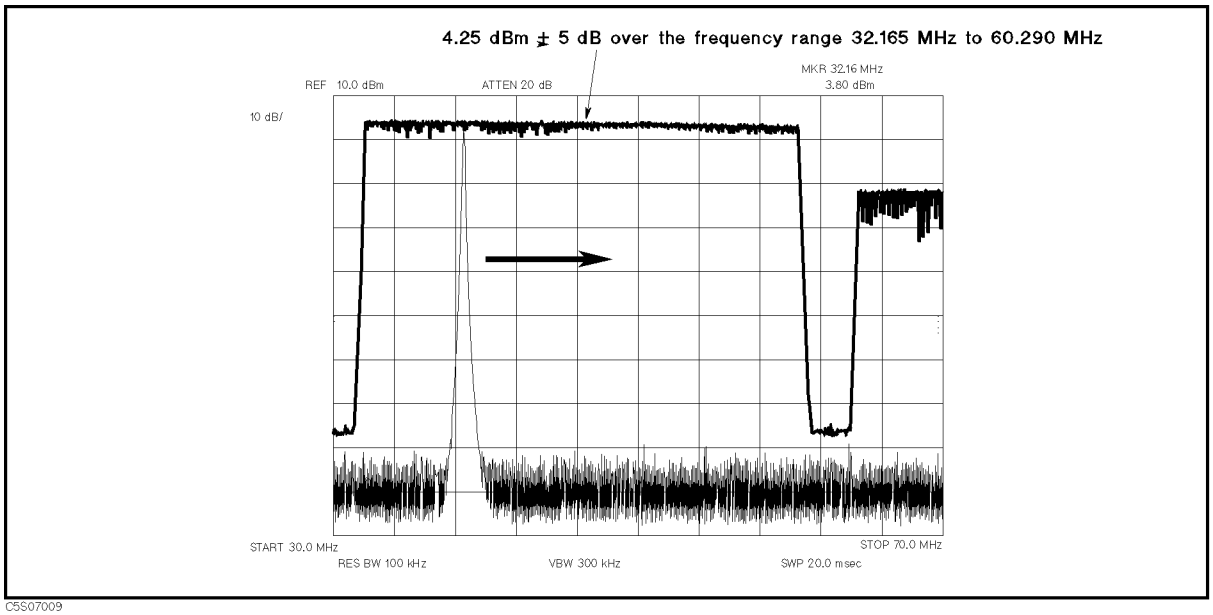


Figure 7-10. FRAC N OSC Typical Signal

j. Reconnect the "H" cable to the A5J7 "FN OUT" connector. Continue with *4. Check the STEP OSC Signal.*

4. Check the STEP OSC Signal

The step oscillator (STEP OSC) generates the signal for frequencies from 470 MHz to 930 MHz with a 20 MHz step. The signal level is typically between −3 dBm and +5 dBm over the frequency range. Perform the following steps to verify the STEP OSC signal:

a. Remove the "L" cable from the A5J2 "STEP PLL OUT" connector. Then connect the equipment as shown in Figure 7-11.

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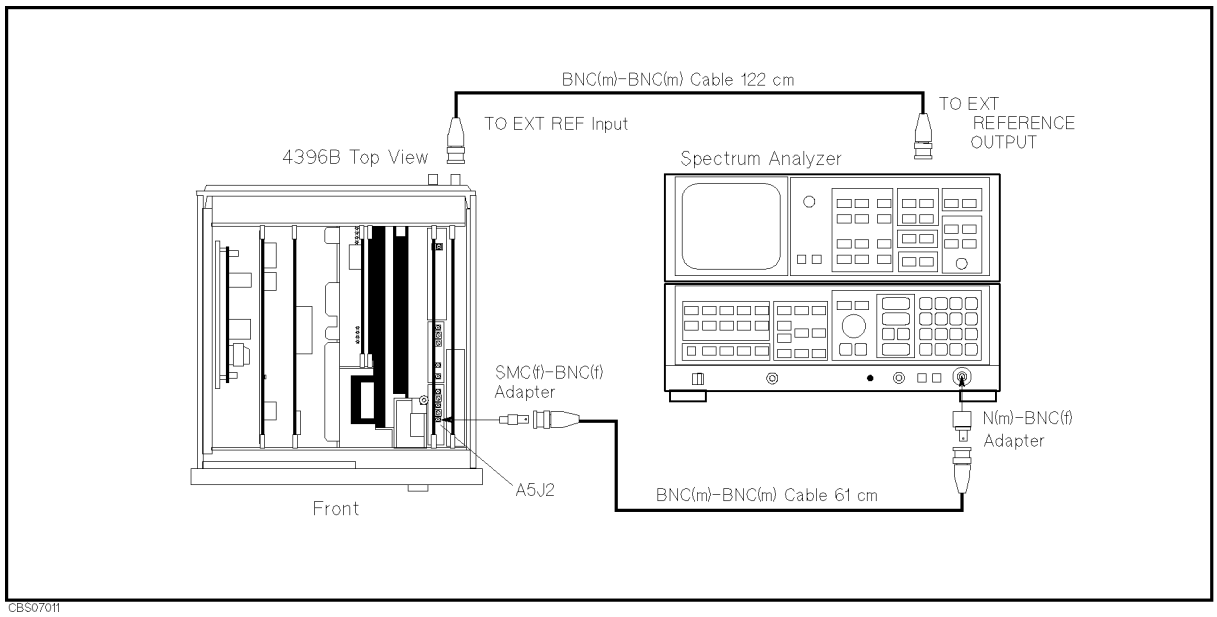


Figure 7-11. STEP OSC Test Setup

b. On the 4396B, press the following keys to measure the STEP OSC frequency by using the bus measurement function:

   (Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset), (Center), CENTER STEP SIZE, (8), (0), (M/μ), (Span), (1), (x1) (then **PHASE LOCK LOOP UNLOCKED** message appears on the display), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (3), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Start Frequency	400 MHz
Stop Frequency	1 GHz
Reference Level	10 dBm

d. On the 4396B, press (Center), (1), (x1), to set the center frequency to the first setting of 1 Hz in of Table 7-1.

   During this procedure, the center frequency and span are set to 1 Hz and 1 Hz, respectively. These center and span settings set the STEP OSC frequency to 470 MHz. By changing the center frequency from 1 Hz to 1.82 GHz in 80 MHz steps, the STEP OSC frequency changes from 470 MHz to 930 MHz in 20 MHz steps.

   The frequency bus measures the STEP OSC frequency through a 1/256 divider. Therefore, the measured value is 1/256 of the actual frequency. For example, the measured value at a center frequency of 0 Hz is 1.8359 U (470 MHz divided by 256). The unit "U" in the frequency bus measurement is equivalent to MHz.

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Table 7-1. STEP OSC Frequency

4396B Center Frequency	STEP OSC Frequency	Bus Measurement Limits
1 Hz	470 MHz	1.8359 U ± 0.01 U
80.000001 MHz	490 MHz	1.9140 U ± 0.01 U
160.000001 MHz	510 MHz	1.9921 U ± 0.01 U
240.000001 MHz	530 MHz	2.0703 U ± 0.01 U
320.000001 MHz	550 MHz	2.1484 U ± 0.01 U
400.000001 MHz	570 MHz	2.2265 U ± 0.01 U
480.000001 MHz	590 MHz	2.3046 U ± 0.01 U
560.000001 MHz	610 MHz	2.3828 U ± 0.01 U
640.000001 MHz	630 MHz	2.4609 U ± 0.01 U
720.000001 MHz	650 MHz	2.5390 U ± 0.01 U
800.000001 MHz	670 MHz	2.6171 U ± 0.01 U
880.000001 MHz	690 MHz	2.6953 U ± 0.01 U
960.000001 MHz	710 MHz	2.7734 U ± 0.01 U
1.040000001 GHz	730 MHz	2.8515 U ± 0.01 U
1.120000001 GHz	750 MHz	2.9296 U ± 0.01 U
1.200000001 GHz	770 MHz	3.0078 U ± 0.01 U
1.280000001 GHz	790 MHz	3.0859 U ± 0.01 U
1.360000001 GHz	810 MHz	3.1640 U ± 0.01 U
1.440000001 GHz	830 MHz	3.2421 U ± 0.01 U
1.520000001 GHz	850 MHz	3.3203 U ± 0.01 U
1.600000001 GHz	870 MHz	3.3984 U ± 0.01 U
1.680000001 GHz	890 MHz	3.4765 U ± 0.01 U
1.760000001 GHz	910 MHz	3.5546 U ± 0.01 U
1.819999999902 GHz	930 MHz	3.6328 U ± 0.01 U

e. On the spectrum analyzer, press PEAK SEARCH to move the marker to the peak of the STEP OSC signal.

f. Perform the following checks to verify the STEP OSC signal at a center frequency of 0 Hz:

i. Check that the 4396B marker reading (STEP OSC signal frequency) is 1.8359 U ± 0.01 U. The limits are listed in the third column of Table 7-1.

ii. Check that the spectrum analyzer's marker reading (STEP OSC signal level) is between −3 dBm to +5 dBm.

iii. Check that the trace displayed on the spectrum analyzer is as shown in Figure 7-12.

- If the signal is good, continue with the next step.
- If the signal is bad, perform the *Comb Generator Adjustment* and *Step Pretune Correction Constants* procedures (see the *Adjustments and Correction Constants* chapter). If the signal is still bad after the adjustments are performed, the STEP OSC is probably faulty. Replace A5.

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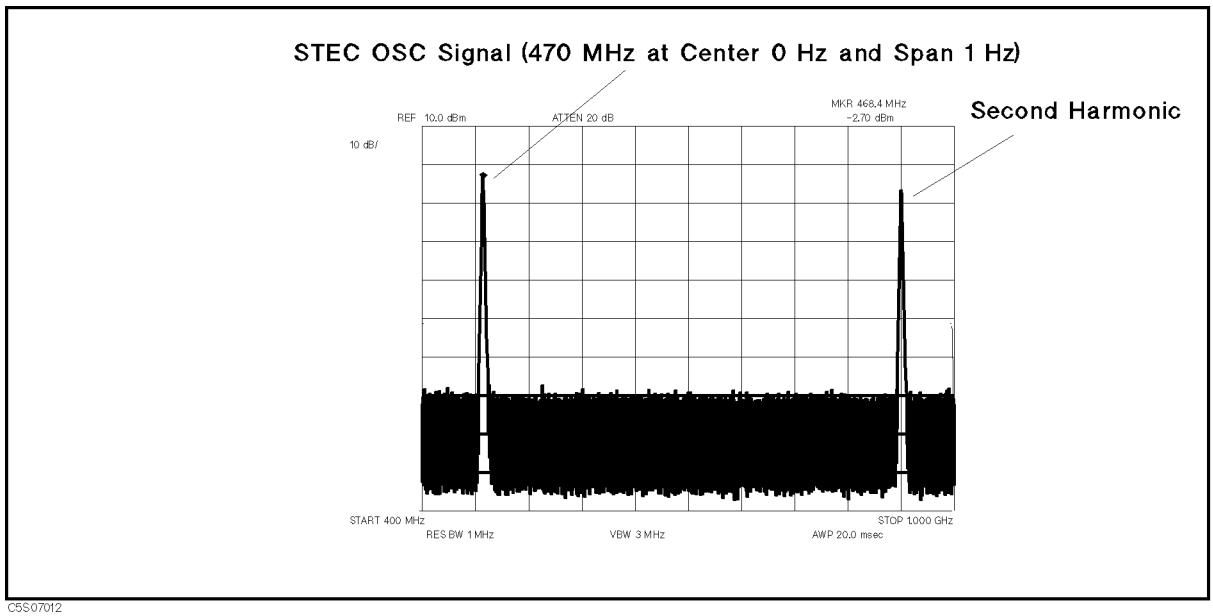


Figure 7-12. Typical STEP OSC Signal at Center 0 Hz

g. On the 4396B, press (Center), (⇧) to change the center frequency in accordance with Table 7-1. Repeat steps e and f for each setting.

h. Reconnect the "L" cable to the A5J2 "STEP PLL OUT" connector. Continue with *5. Check the 520 MHz Signal.*

5. Check the 520 MHz Signal

The 520 MHz signal (520 MHz, −15 dBm ± 0.2 dB) is derived from the 40 MHz reference signal through the X 13 Multiplier. See the A5 Synthesizer block in Figure 7-1. Therefore, the signal contains 40 MHz harmonics as shown in Figure 7-13. Perform the following steps to verify the 520 MHz signal:

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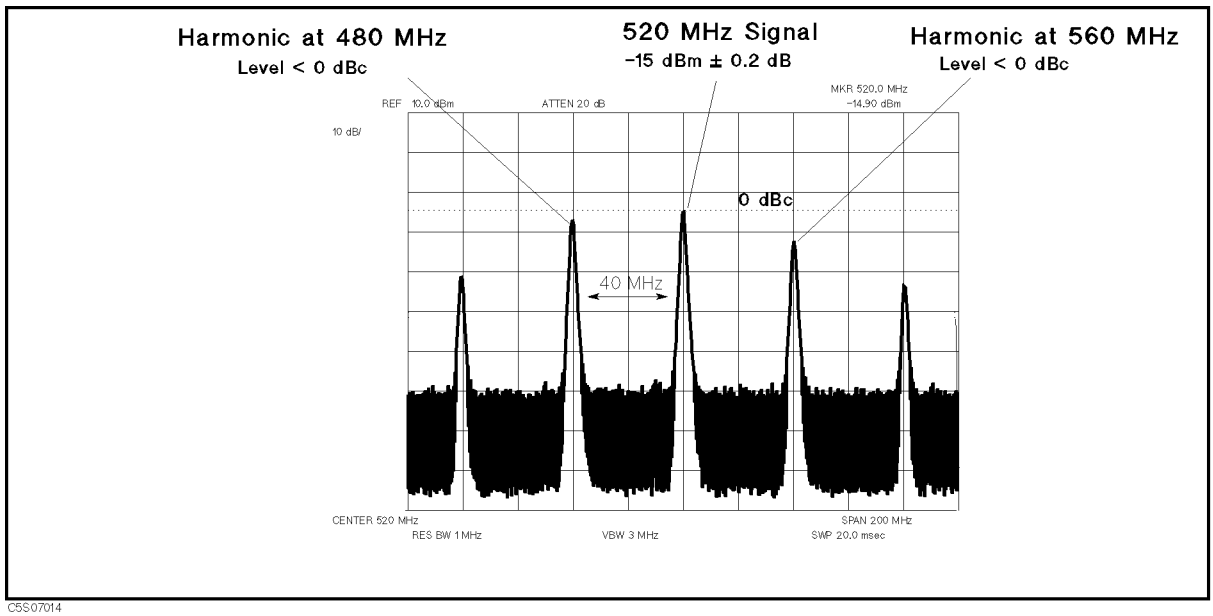


Figure 7-13. Typical 520 MHz Signal

a. Press (Preset) to initialize the 4396B.

b. Remove the "J" cable from the A5J3 "520 MHz OUT" connector. After the "PHASE LOCK LOOP UNLOCKED" message appears, connect the equipment as shown in Figure 7-14.

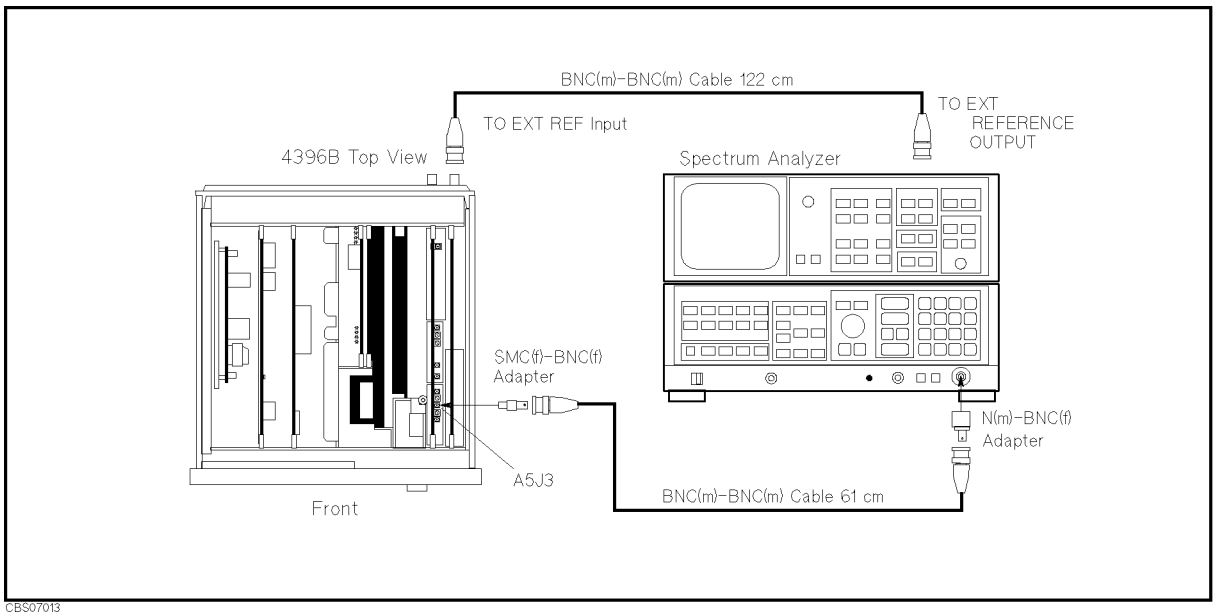


Figure 7-14. 520 MHz Signal Test Setup

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	520 MHz
Span	200 MHz

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d. On the spectrum analyzer, press PEAK SEARCH to move the marker to the peak of the 520 MHz signal.

e. Check that the frequency is 520 MHz, the level is −15 dBm ± 0.2 dB, and the harmonic levels at 480 MHz and 560 MHz are lower than 0 dBc (lower than the 520 MHz signal level). The trace displayed on the spectrum analyzer should be as shown in Figure 7-13.

- If the signal is good, continue with *6. Check the EXT REF Operation.*
- If the signal level is out of the limits, perform the *520 MHz Level Adjustment* (see the *Adjustments and Correction Constants* chapter).
  - If the adjustment is successfully completed, continue with *6. Check the EXT REF Operation.*
  - If the adjustment fails, the X13 multiplier is faulty. Replace A5.
- If the signal is bad, the X13 multiplier is faulty. Replace A5.

6. Check the EXT REF Operation

When an external reference signal (10 MHz, 0 dBm) is applied to the EXT REF input connector on the rear panel, the message "`ExtRef`" appears on the display. When the external reference signal is removed, the "`ExtRef`" message disappears.

Perform the following steps to verify the operation of the EXT REF input:

a. Connect the equipment as shown in Figure 7-15. Then check that the "`ExtRef`" message appears on the display. If Option 1D5 is installed in the 4396B, connect the cable between the EXT REF Input connector and REF OVEN (Opt 1D5) connector.

b. Disconnect the cable from the EXT REF input. Then check that the "`ExtRef`" message disappears.

- If the "`ExtRef`" message appears and disappears correctly, the EXT REF circuit probably working. At this point, the A5 synthesizer is verified.
- If the "`ExtRef`" message does not appear, inspect the cable and connections between the EXT REF input connector and A5J4. See Figure 7-3 for the location of A5J4. If the cable and connections are good, the most probable faulty assembly is A5. Replace A5.

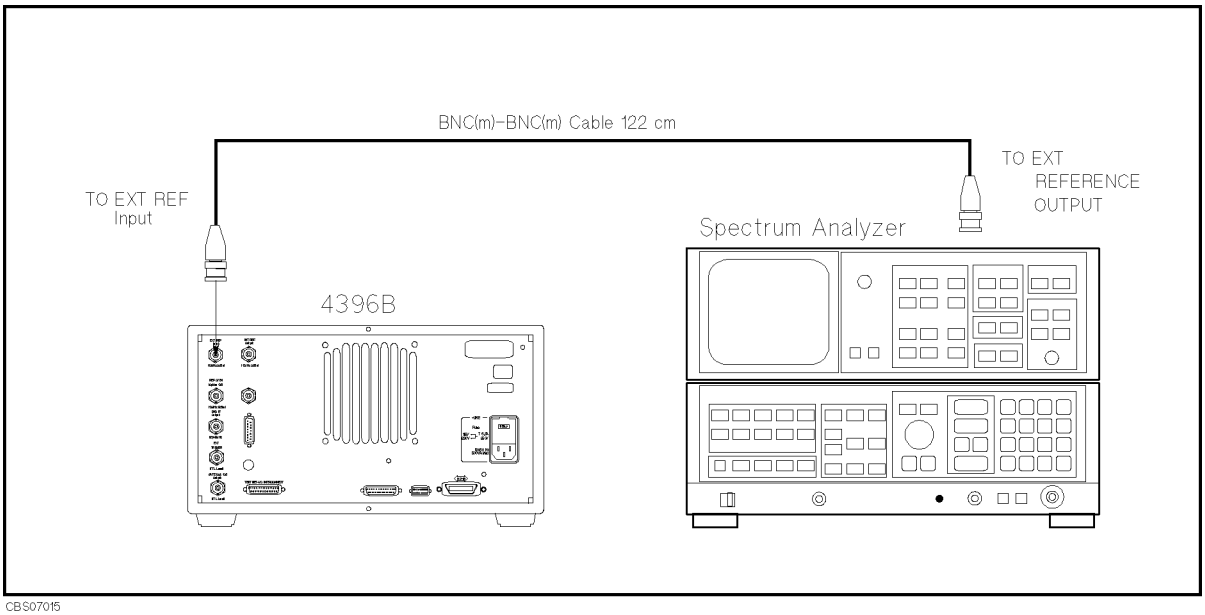


Figure 7-15. EXT REF Test Setup

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CHECK A4A1 1ST LO OUTPUTS

The input signals to A4A1 are the FRAC N OSC signal and the STEP OSC signal (see Figure 7-1). Before performing the procedures in this section, verify the FRAC N OSC signal and STEP OSC signal in accordance with the previous section.

The output signals from A4A1 are two 1st local oscillator signals (2.05858 GHz to 3.85858 GHz). One goes from the A4A1J3 connector to the A3A3 source. The other goes from the A4A1J4 connector to the A4A2 Receiver RF. If the two signals are good, the A4A1 1st LO is verified.

Perform the following procedures sequentially to verify the two A4A1 output signals at A4A1J3 and A4A1J4.

Note If one or both of the signals are bad, the A4A1 1st LO is faulty. Replace the A4 1st LO/Receiver RF (which consists of the A4A1 1st LO and the A4A2 Receiver RF).

In these procedures, the two A4A1 outputs are observed using test equipment and the 4396B self-test functions. For detailed information about the 4396B self-test functions, see the *Service Key Menus*. Also, the signals are verified in two A4A1 operation modes, single-loop mode and triple-loop mode. For a description of these operation modes, see the *Theory of Operation* chapter.

1. Check the 1st LO OSC Signal at A4A1J3

The 1st local oscillator signal at A4A1J3 is a swept 2.05858 GHz to 3.85858 GHz signal with the power level between −5 dBm to +5 dBm over the frequency range. Perform the following steps to verify the 1st local oscillator signal at A4A1J3:

a. Remove the “C” semi-rigid cable from A4A1J3. See Figure 7-16 for the location of A4A1J4. Then connect the equipment as shown in Figure 7-16. Connect the BNC(m)-BNC(m) cable to A4A1J3.

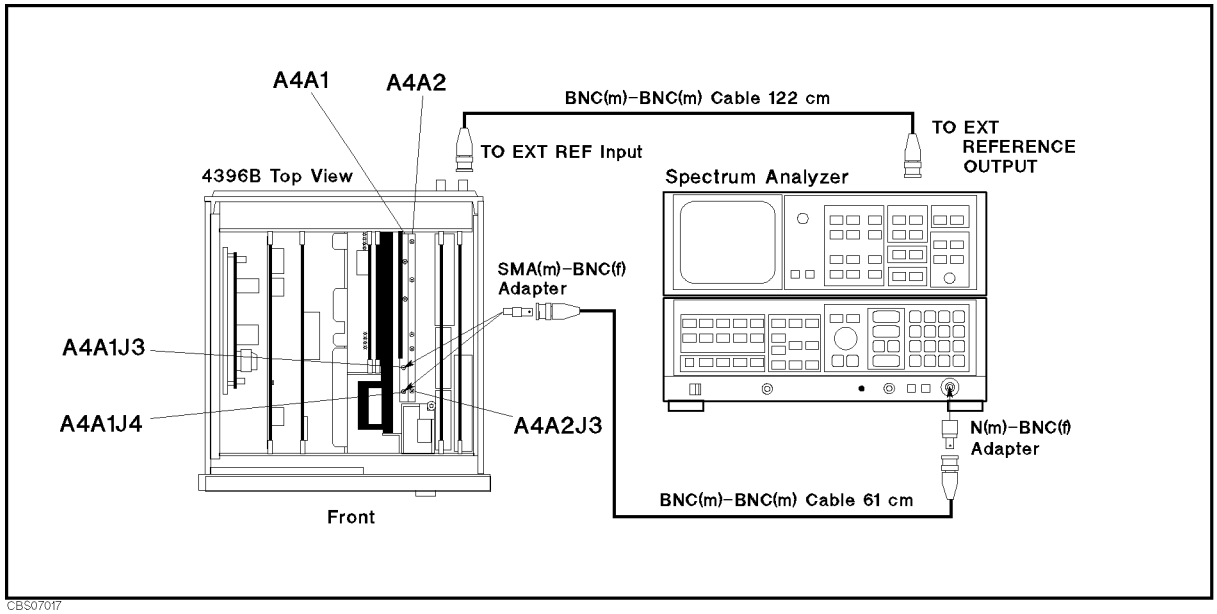


Figure 7-16. 1st LO OSC Signal Test Setup

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b. Press (Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset), (Sweep), SWEEP TIME, (2), (0), (x1).

During this procedure, the start and stop frequencies are set to 0 MHz and 1.8 GHz, respectively. These start and stop settings set the 1st LO OSC to the single-loop mode and sweep the frequency from 2.05858 GHz (at the start frequency 0 Hz) to 3.85858 GHz (at the stop frequency 1.8 GHz).

c. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	**Settings**
Start Frequency	2 GHz
Stop Frequency	4 GHz
Reference Level	10 dBm
Max Hold	ON

d. On the 4396B, press (Trigger), MEASURE RESTART. Wait for the completion of the sweep

e. Check that the signal level is −5 dBm to +5 dBm over the frequency range of 2.058 G MHz to 3.858 GHz. The displayed trace should be as shown in Figure 7-17.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss at high frequencies. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

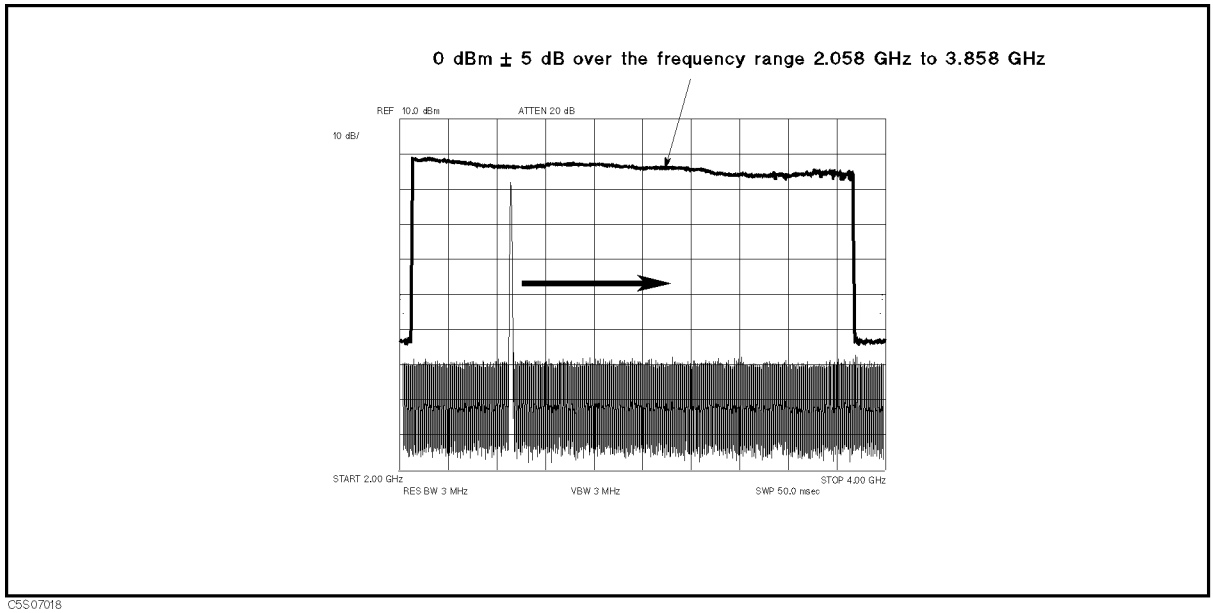


Figure 7-17. Typical 1st LO OSC Signal (Single Mode) at A4A1J3

f. On the 4396B, press (Span), (4), (5), (M/μ).

During this procedure, the start and stop frequencies are set to 877.5 MHz and 922.5 MHz, respectively. These start and stop settings set the 1st LO OSC to the triple-loop mode and sweep the 1st LO OSC frequency from 2.93608 GHz (at the start frequency 877.5 MHz) to 2.98108 GHz (at the stop frequency 922.5 GHz).

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g. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	Settings
Start Frequency	2.9 GHz
Stop Frequency	3 GHz
Reference Level	10 dBm
Max Hold	ON

h. On the 4396B, press (Trigger), MEASURE RESTART. Wait for the completion of the sweep

i. Check that the signal level is −5 dBm to +5 dBm over the frequency range of 2.936 G MHz to 2.981 GHz. The displayed trace should be as shown in Figure 7-18.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss in the high frequency range. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

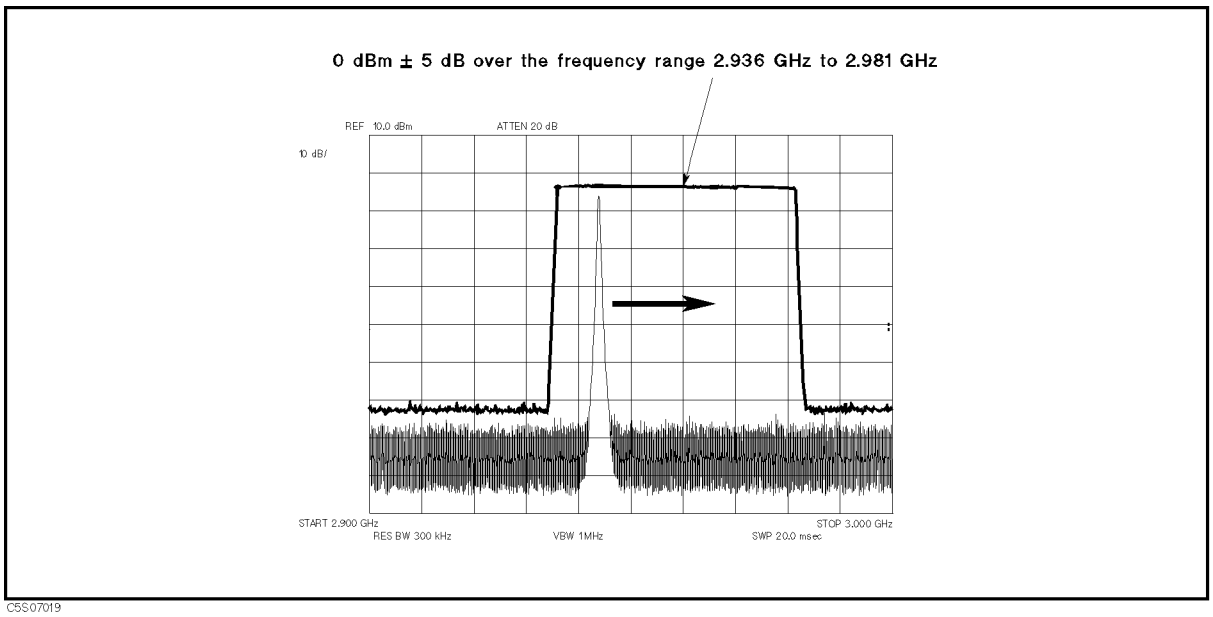


Figure 7-18. Typical 1st LO OSC Signal (Triple Mode) at A4A1J3

j. Reconnect the "C" semi-rigid cable to A4A1J3. Then continue with *2. Check the 1st LO OSC Signal at A4A1J4.*

2. Check the 1st LO OSC Signal at A4A1J4

The 1st local oscillator signal at A4A1J4 is a swept 2.05858 GHz to 3.85858 GHz signal with the power level > +16 dBm over the frequency range. Perform the following steps to verify the 1st local signal at A4A1J3:

a. Remove the "F" semi-rigid cable from A4A1J4 and A4A2J3. See Figure 7-16 for the location of A4A1J4 and A4A2J3. Then connect the equipment as shown in Figure 7-16. Connect the BNC(m)-BNC(m) cable to A4A1J3.

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b. On the 4396B, press (Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset), (Sweep), SWEEP TIME, (2), (0), (x1). During this procedure, the start and stop frequencies are set to 0 MHz and 1.8 GHz, respectively.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Start Frequency	2 GHz
Stop Frequency	4 GHz
Reference Level	20 dBm
Max Hold	ON

d. On the 4396B, press (Trigger), MEASURE RESTART. Wait for the completion of the sweep

e. Check that the signal level is higher than +16 dBm over the frequency range of 2.058 G MHz to 3.858 GHz. The displayed trace should be as shown in Figure 7-19.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss in the high frequency range. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

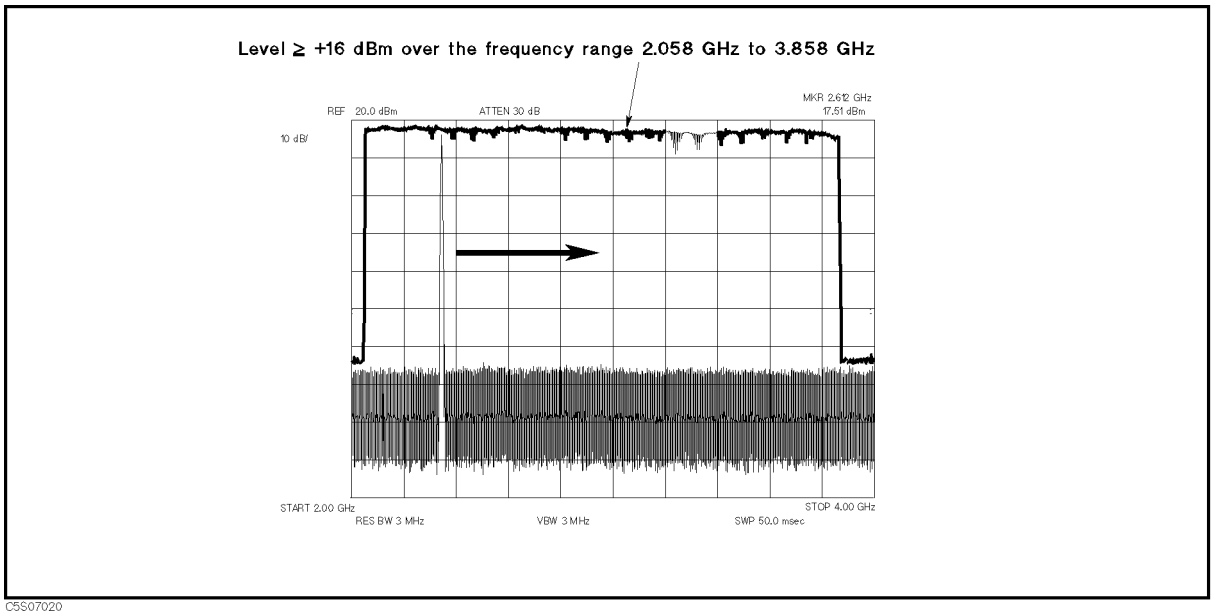


Figure 7-19. 1st LO OSC Typical Signal (Single Mode) at A4J4

f. Reconnect the "F" semi-rigid cable to A4A1J4 and A4A2J3. At here, the A4A1 1st LO is verified.

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CHECK AN A3A1 ALC OUTPUT

The input signal to the A3A1 ALC is the 40 MHz reference signal coming from A5 (see Figure 7-1). Before performing the procedures in this section, verify the CAL OUT signal in accordance with the *Check A5 Synthesizer Outputs* section. This ensures that the 40 MHz reference signal is good. In addition, perform the *RF OUT Level Correction Constants* (see the *Adjustments and Correction Constants* chapter) to verify that the ALC circuit is working correctly.

The three output signals from A3A1 are the 21.42 MHz signal with the level controlled by the automatic leveling control (ALC) circuit, the 8 MHz reference signal, and the 40 kHz reference signal.

Perform the following procedures sequentially to verify the 21.42 MHz signal. If the signal is bad, replace A3A1.

In this procedure, only the 21.42 MHz signal is verified. This is because the 8 MHz and 40 kHz reference signals are verified by running internal test 11 in the *Start Here*. The 21.42 MHz signal is observed using test equipment and its level is controlled by the 4396B self-test functions. For detailed information about the 4396B self-test functions, see the *Service Key Menus*.

1. Check the 21.42 MHz Signal

Perform the following steps to verify the 21.42 MHz signal:

a. Remove the "D" cable from A3A2J22. See Figure 7-20 for the location of A3A2J22. Then connect the equipment to the "D" cable as shown in Figure 7-20.

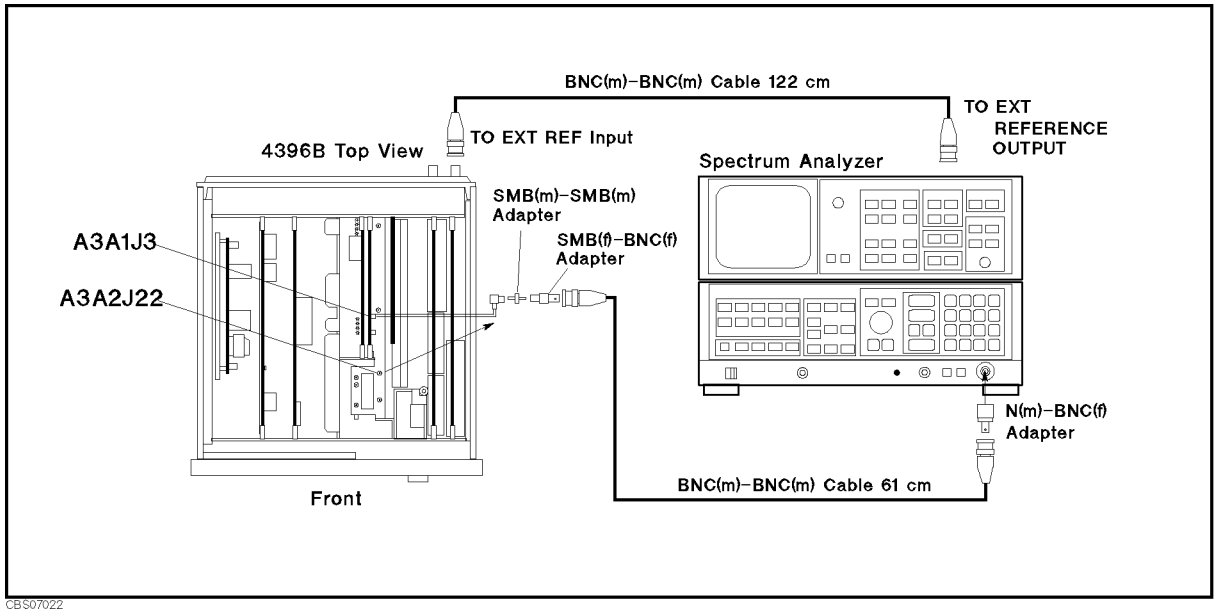


Figure 7-20. ALC Outputs Test Setup

b. Press (Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset) to initialize the 4396B.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	21.42 MHz

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Span	1 MHz
Reference Level	10 dBm

d. On the 4396B, press the following keys.

(System), SERVICE MENU, SERVICE MODES, SOURCE, SOURCE AUTO man (then the label changes to SOURCE auto MAN), LVL DAC AUTO man (then the label changes to LVL DAC auto MAN), LVL DAC VALUE, (4), (0), (0), (x1), GAIN DAC AUTO man (then the label changes to GAIN DAC auto MAN), GAIN DAC VALUE, (4), (x1)

e. On the spectrum analyzer, press (PEAK SEARC) to move the marker to the peak of the 21.42 MHz signal.

f. Check that the frequency is 21.42 MHz and the level is higher than 0 dBm. The displayed trace should be as shown in Figure 7-21.

- If the signal is good, continue with the next step.
- If the signal is bad, the ALC is not working properly. Replace A3A1.

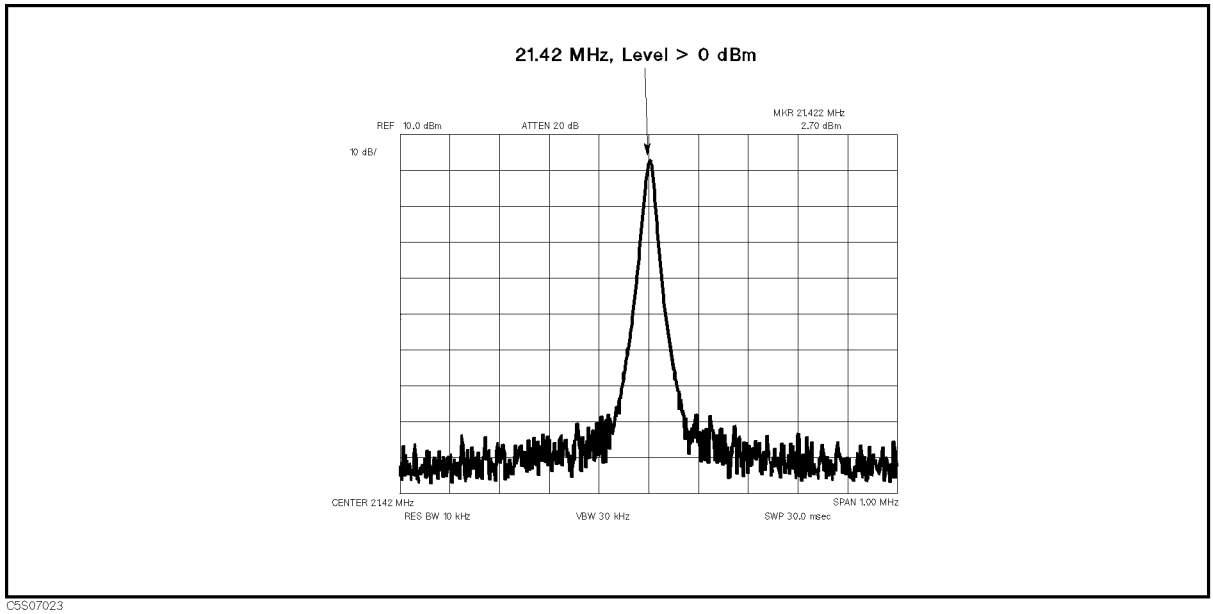


Figure 7-21. Typical 21.42 MHz Signal

g. On the 4396B, press ALC LOOP open CLOSE (then the label changes to ALC LOOP OPEN close), LVL DAC VALUE.

h. Press (⇧) and (⇩) as required to change the level DAC value. Then check that the signal level changes on the spectrum analyzer's display.

- If the level changes, continue with the next step.
- If the level does not change, the ALC is faulty. Replace A3A1.

i. On the 4396B, press ALC LOOP OPEN close (then the label changes to ALC LOOP open CLOSE), (Source), RF OUT ON off (then the label changes to RF OUT on OFF).

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j. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the 21.42 MHz signal.

k. Check that the signal level is lower than −70 dBm.

- If the signal is good, continue with the next step.
- If the signal is bad, the ALC is faulty. Replace A3A1.

l. Reconnect the “D” cable to A3A2J22. At this point, the A3A1 ALC is probably verified.

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CHECK A3A2 2ND LO OUTPUTS

The two input signals to A3A2 are the 520 MHz signal coming from A5 and the 21.42 MHz signal coming from A3A1. See Figure 7-1. Before performing the procedures in this section, verify the 520 MHz signal in accordance with the *Check A5 Synthesizer Outputs* section and verify the 21.42 MHz signal in accordance with the *Check an A3A1 ALC Output* section. In addition, perform the *RF OUT Level Correction Constants* procedure (see the *Adjustments and Correction Constants* chapter) to verify that the ALC circuit is working correctly.

The two output signals from A3A2 are the 2.08 GHz 2nd local oscillator signal going to the A4A2 Receiver IF and the 2.05858 GHz signal going to the A3A3 source. Perform the following procedures sequentially to verify these signals. If one of the signals is bad, replace A3A2.

In this procedure, the 2.05858 GHz signal level is controlled by the 4396B self-test functions. For detailed information about the 4396B self-test functions, see the *Service Key Menus*.

1. Check the 2nd Local Oscillator Signal

The 2nd local oscillator signal is the 2.08 GHz CW signal a with signal level > +7 dBm (typical). Perform the following steps to verify the frequency and level of the 2nd local oscillator signal:

a. Remove the "I" semi-rigid cable from A3A2J19 and remove the "D" cable from A3A1J3. See Figure 7-22 for the locations of A3A2J19 and A3A1J3. Then connect the equipment as shown in Figure 7-22.

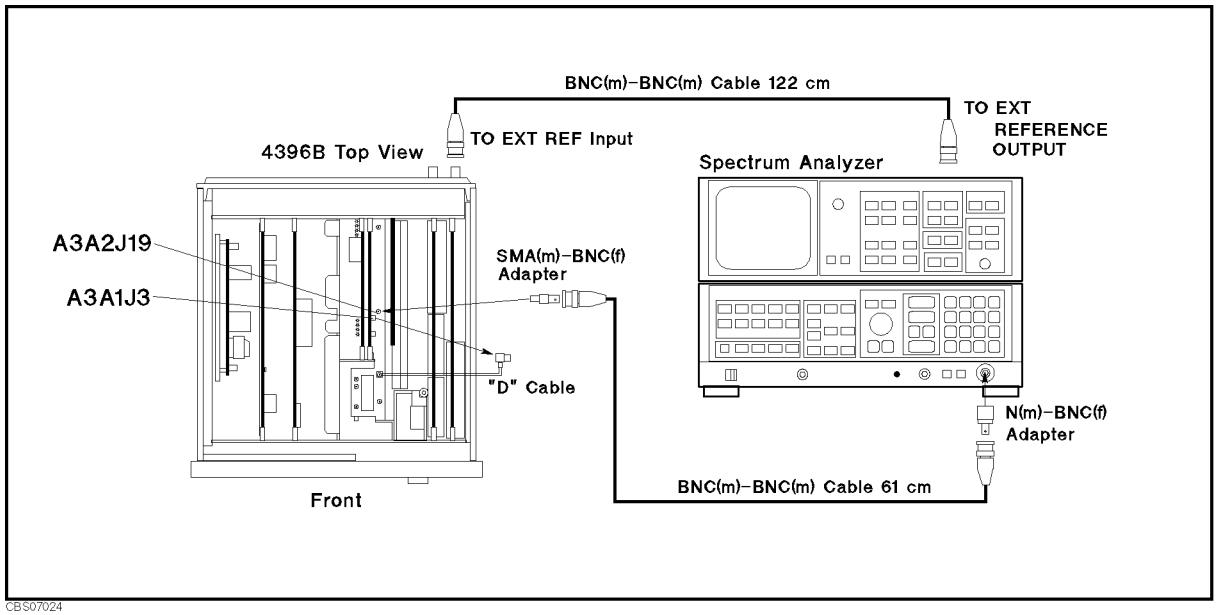


Figure 7-22. 2nd LO OSC Test Setup

b. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	2.08 GHz
Span	1 MHz
Reference Level	20 dBm

c. On the spectrum analyzer, press PEAK SEARCH to move the marker to the peak of the 2nd Local.

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d. Check that the frequency is 2.08 GHz and the level is higher than +7 dBm. The 2nd local oscillator signal should be as shown in Figure 7-23.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss at high frequency. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal is good, continue with the next step.
- If it is bad, perform the *Second Local PLL Lock Adjustment* (see the *Adjustments and Correction Constants* chapter). If the problem persists after the adjustment, the A3A2 2nd LO OSC is faulty. Replace A3A2.

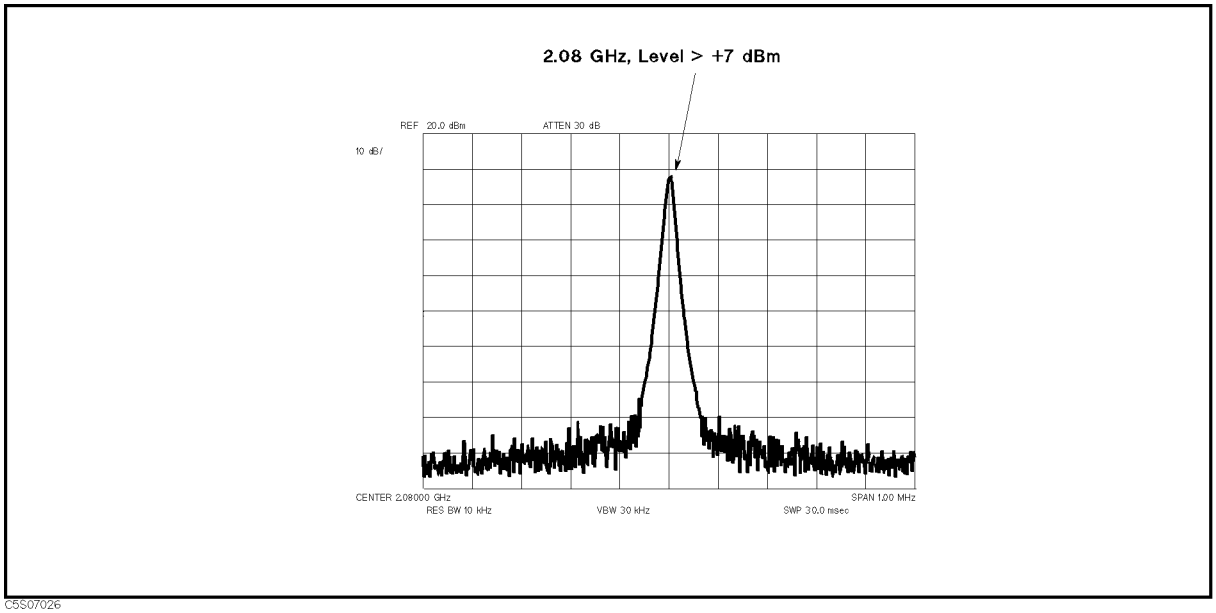


Figure 7-23. Typical 2nd Local Oscillator Signal

e. Reconnect the "I" semi-rigid cable to A3A2J19 and reconnect the B"D" cable to A3A1J3. Then continue with *2. Check the 2.05858 GHz Signal.*

2. Check the 2.05858 GHz Signal

The 2.05858 GHz signal level is controlled by the ALC loop. See the A3A2 2nd LO block in Figure 7-1. Perform the following steps to verify the frequency and level of the 2.05858 GHz signal:

a. Remove the "E" cable from A3A2J23. See Figure 7-22 for the location of A3A2J23. Then connect the equipment as shown in Figure 7-24.

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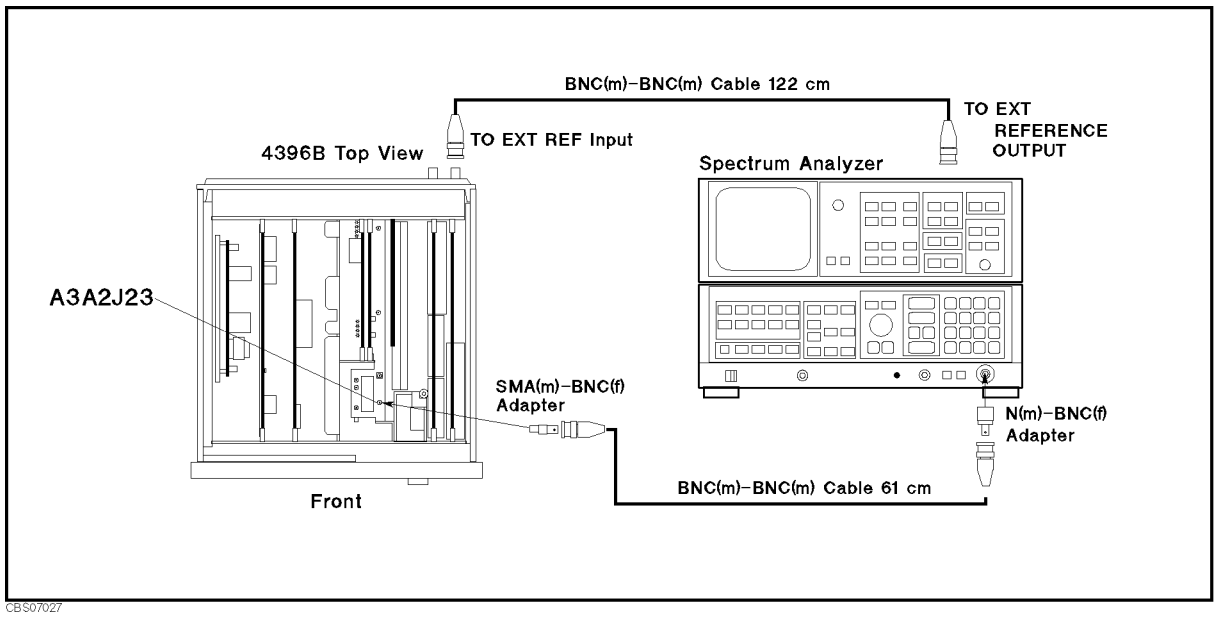


Figure 7-24. Source IF Test Setup

b. Press (Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset) to initialize the 4396B.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	2.05858 GHz
Span	1 MHz
Reference Level	20 dBm

d. On the 4396B, press the following keys.

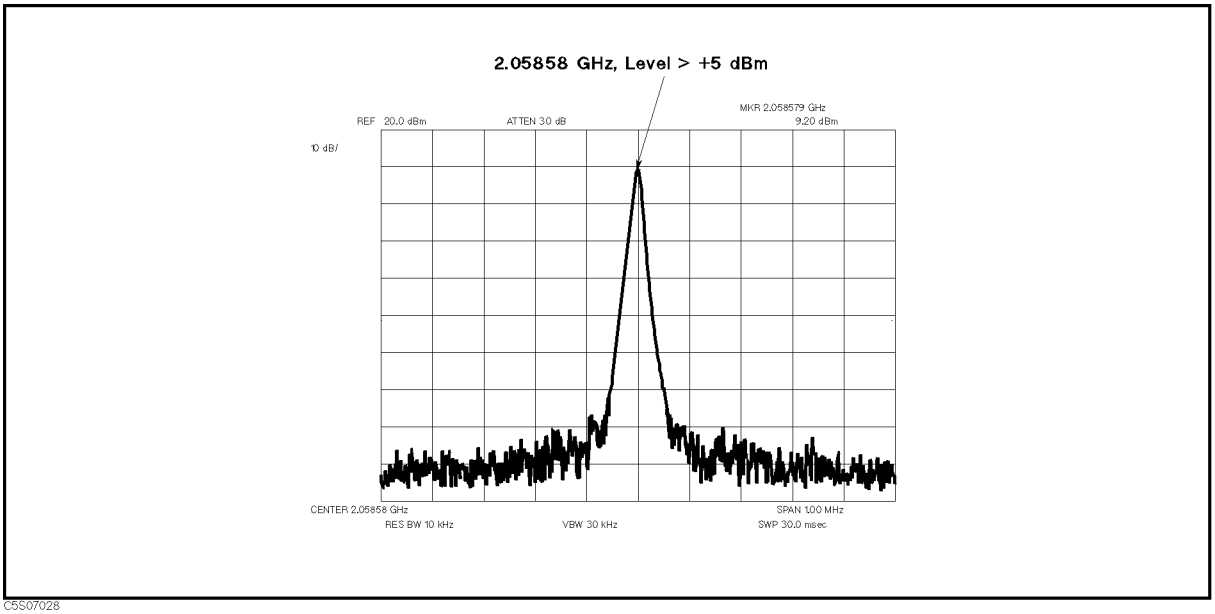
(System), SERVICE MONU, SERVICE MODES, SOURCE, SOURCE AUTO man (then the label changes to SOURCE auto MAN), LVL DAC AUTO man (then the label changes to LVL DAC auto MAN), LVL DAC VALUE, (4), (0), (0), (x1), GAIN DAC AUTO man (then the label changes to GAIN DAC auto MAN), GAIN DAC VALUE, (4), (x1)

e. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the ALC output signal.

f. Check that the frequency is 2.05858 GHz and the level is higher than +5 dBm. The displayed trace should be as shown in Figure 7-25.

- If the signal is good, continue with the next step.
- If the signal is bad, the Source First Mixer is faulty. Replace A3A2.

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C5S07028

Figure 7-25. Typical Source IF

g. On the 4396B, press `ALC LOOP open CLOSE` (then the label changes to `ALC LOOP OPEN close`), `LVL DAC VALUE`.

h. Press ⇧ and ⇩ as required to change the level DAC value. Then check the signal level changes on the spectrum analyzer's display.

- If the level changes, continue with the next step.
- If the level does not change, the Source First Mixer is faulty. Replace A3A2.

i. Reconnect the "E" semi-rigid cable to A3A2J23. At this point, the A3A2 2nd LO is verified.

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CHECK AN A3A3 SOURCE OUTPUT

The two input signals to A3A3 are the 1st local oscillator signal coming from A4A1 and the 2.05858 GHz signal coming from A3A2. See Figure 7-1. Before performing the procedures in this section, verify the 1st local oscillator signal at A4A1J3 in accordance with the *Check A4A1 1st LO Outputs* section and verify the 2.05858 GHz signal in accordance with the *Check A1A2 2nd LO Outputs*. In addition, perform the *RF OUT Level Correction Constants* in accordance with the *Adjustments and Correction Constants* chapter in this manual to have the ALC circuit to work correctly.

The two output signals from A3A3 are the RF signal (100 kHz to 1.8 GHz, −10 dBm to +20 dBm) going to the A7 output attenuator and the level detector's signal going to the A3A1 ALC. If the RF signal is good, the ALC circuit and the level detector's signal are verified. Therefore, only the RF signal is checked in the following procedure.

Perform the following procedure to verify the RF signal. If the signal is bad, replace A3A3.

1. Check the A3A3 RF Signal

The A3A3 source generates the RF signal (100 kHz to 1.8 GHz, −10 dBm to +20 dBm). Perform the following steps to verify the frequency and level of the RF signal:

a. Remove the "D" semi-rigid cable from A3A3 Source. See Figure 7-26 for the locations of the "D" cable. Then connect the equipment as shown in the setup 1 of Figure 7-26.

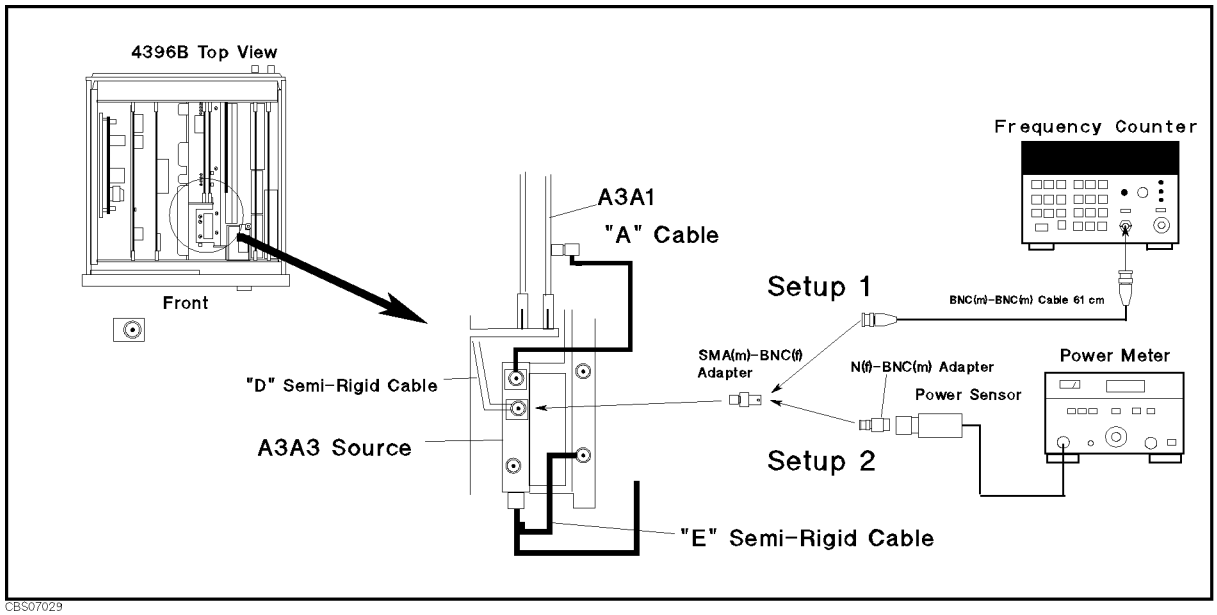


Figure 7-26. A3A3 RF Signal Test Setup

b. Press (Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Center), (5), (0), (M/μ), (Span), ZERO SPAN.

c. Check that the frequency counter reading is 50 MHz ± 275 Hz.

- If the frequency is good, continue with the next step.
- If the frequency is bad, inspect the "E" semi-rigid cable and the connections between A3A2 and A3A3. If the cable and the connections are good, A3A3 is the most probable faulty assembly. Replace A3A3.

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d. Connect the power sensor to the power meter and calibrate the power meter for the power sensor. Then connect the equipment as shown in the setup 2 of Figure 7-26.

e. Wait for the power meter reading to settle. Then check the power meter reading (RF signal level) is 10 dBm ± 0.5 dB.

- If the RF signal level is good, continue with the next step.
- If the RF signal level is bad, inspect the "A" cable and the connections between A3A3 and A3A1. For the location of the "A" cable, see Figure 7-26. If the cable and the connections are good, A3A3 is the most probable faulty assembly. Replace A3A3.

f. Press the following keys.

(Preset), (Sweep), SWEEP TYPE MENU, POWER SWEEP, RETURN, NUMBER OF POINTS, (7), (x1), (Source), CW FREQ, (5), (0), (M/μ), (Start), (-), (1), (0), (x1), (Stop), (2), (0), (x1), (Trigger), TRIGGER:[FREE RUN], MANUAL, TRIG EVENT [ON SWEEP] (then the label changes to TRIG EVENT [ON POINT])

g. Press (Trigger), SINGLE, TRIGGER:[MANUAL] to start a power sweep and to set the 4396B power to the 1st sweep point of −10 dBm. Table 7-2 lists test settings.

Table 7-2. A3A3 Source Test Settings

4396B Source Power	A3A3 RF Signal Level [a]	Power Sweep Linearity[1]	Limits
−10 dBm	**a1 =** _____ dBm	**a5−a1−20 =** _____ dB	± 0.5 dB
−5 dBm	**a2 =** _____ dBm	**a6−a2−20 =** _____ dB	± 0.5 dB
0 dBm	**a3 =** _____ dBm	**a7−a3−20 =** _____ dB	± 0.5 dB
+5 dBm	**a4 =** _____ dBm	**a7−a4−15 =** _____ dB	± 0.5 dB
+10 dBm	**a5 =** _____ dBm	**a7−a5−10 =** _____ dB	± 0.5 dB
+15 dBm	**a6 =** _____ dBm	**a7−a6−5 =** _____ dB	± 0.5 dB
+20 dBm	**a7 =** _____ dBm		

1 Calculate the linearity using the equations provided below.

h. Wait for the power meter reading to settle. Then record the power meter reading in the second column of Table 7-2.

i. Press MANUAL to set the source power to the next measurement point listed in Table 7-2. Then repeat step h until a power sweep is completed.

The sweep indicator moves to the last measurement point on the sweep. (The sweep indicator indicates the last measurement point on the sweep, not the current point.)

j. Calculate the power sweep linearity using the equations given in Table 7-2. Then check that the power sweep linearity is within the limits.

- If the power linearity is good, continue with the next step.
- If the power linearity is bad, inspect the "A" cable and the connections between A3A3 and A3A1. If the cable and the connections are good, A3A3 is the most probable faulty assembly. Replace A3A3.

k. Reconnect the "D" cable to A3A3. At this point, the A3A3 Source is verified.

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CHECK A7 OUTPUT ATTENUATOR CONTROL SIGNALS

Use this procedure when the A7 Output Attenuator is the most suspicious assembly (for example, if external test 20 fails).

A7 is controlled by the three signals at A7J1, A7J2, and A7J3 that come from the A2 post-regulator. The location of A7J1, A7J2, and A7J3 are shown in Figure 7-3.

Perform the following procedure to verify the A7 control signals. If the signals are good, replace A7. If the signals are bad, replace A2.

In this procedure, the control signal is set using the 4396B self-test functions. For detailed information about the 4396B self-test functions, see the *Service Key Menus*.

1. Check A7 Control Signals

The A7 Output Attenuator is controlled by the three lines at A7J1, A7J2, and A7J3 as shown in Figure 7-27. Perform the following steps to verify the A7 control signals:

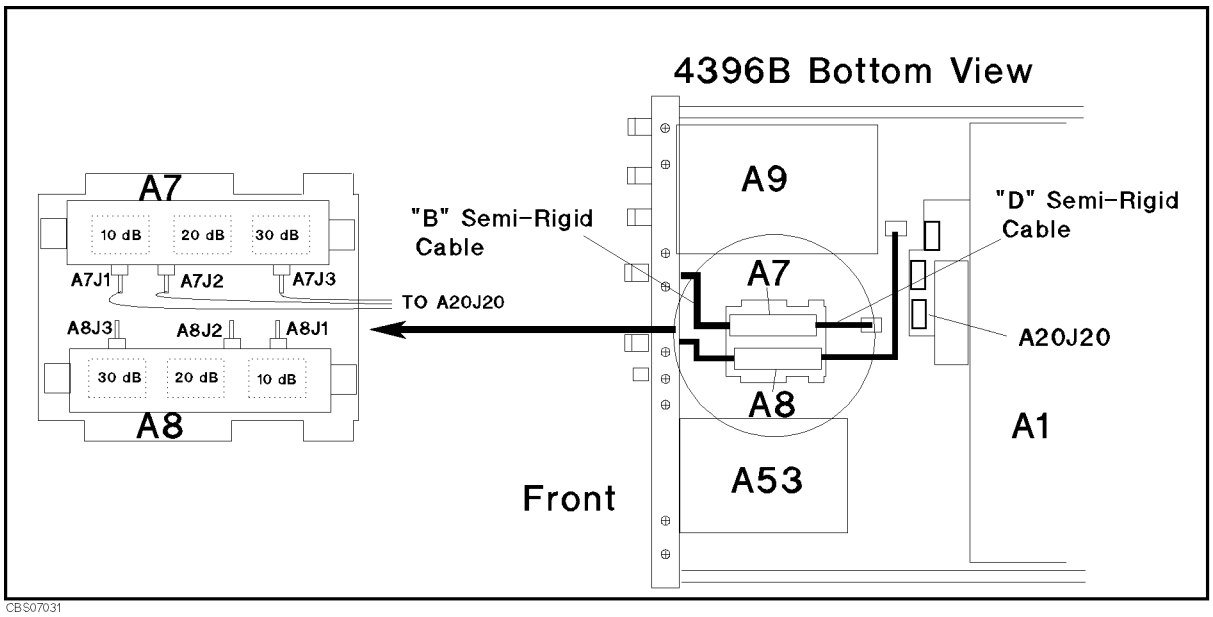


Figure 7-27. A7 Output Attenuator Control Signals

a. Press the following keys.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Center), (5), (0), (M/μ), (Span), ZERO SPAN, (Source), SOURCE POWER, (0 dBm), (System), SERVICE MENU, SERVICE MODES, SOURCE, SOURCE AUTO man then the label changes to SOURCE auto MAN

b. On the 4396B, press OUTPUT ATT [AUTO], 0 dB to set A7 to the first setting of 0 dB in Table 7-3.

c. Measure voltage at A7J1, A7J2, and A7J3 using a voltmeter. Then check the measured values are within limits. The typical voltages are listed in Table 7-3.

- If the control voltages are good, continue with the next step.

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- If the control voltages are bad, inspect the cable between A7 and A20J20. If the cable is good, the attenuator control circuit in the A2 post-regulator is probably faulty. Replace A2.

Table 7-3. A7 Attenuation Test Settings

A7 Attenuation	A7J1 Voltage	A7J2 Voltage	A7J3 Voltage
0 dB	High[1]	Low[2]	Low
−10 dB	Low	Low	Low
−20 dB	High	High	Low
−30 dB	Low	High	Low
−40 dB	Low	Low	High
−50 dB	High	High	High
−60 dB	Low	High	High

1 Is within +8.4 V to +16 V (+12 V typical).

2 Is 0 V typical.

d. Repeat steps b and c to set A7 in accordance with Table 7-3.

At this point, the A7 attenuator control signals are verified.

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CHECK THE A60 HIGH STABILITY FREQUENCY REFERENCE

Perform the following procedures to verify the A60 High Stability Frequency Reference:

1. Observe the REF OVEN signal on the rear panel using a spectrum analyzer. Check that the frequency is 10 MHz and the level is approximately 0 dBm.
   - If the signal is good, continue with the next step.
   - If the signal is bad, inspect the cable and connections between A60 and REF OVEN. If the cable and connections are good, replace the A60 High Stability Frequency Reference.
2. Perform the *10 MHz Reference Oscillator Frequency Adjustment (Option 1D5 Only).* For the procedure, see the *Adjustments and Correction Constants* chapter.
   - If the adjustment is successfully completed, the A60 High Stability Frequency Reference is verified.
   - If the adjustment fails, check the CAL OUT Signal and the EXT REF operation in accordance with the procedures provided in the *Check A5 Synthesizer Outputs* section of this chapter. If both are good, the A60 High Stability Frequency Reference is probably faulty. Replace A60.

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8

Receiver Group Troubleshooting

INTRODUCTION

Use these procedures only if you have read the *Isolate Faulty Group Troubleshooting* chapter, and you believe the problem is in the receiver group.

These procedures are designed to let you identify the bad assembly within the receiver group in the shortest possible time. Whenever an assembly is replaced in this procedure, refer to Table 13-1 *Post Repair Procedures* in the *Post-Repair Procedures* chapter in this manual.

The procedures isolate the faulty assembly by using the 4396B self-test functions (internal and external tests). In the external tests, the RF OUT signal (which is the output of the source group) is used to test the receiver group. Therefore, before performing these procedures, verify the source group. See the *Operator's Check Troubleshooting* in the *Isolate Faulty Group* chapter.

Figure 8-1 shows a simplified block diagram of the receiver group. The receiver group consists of the following assemblies:

- A8 Input Attenuator
- A9 Input Multiplexer
- A4A2 Receiver RF
- A6 Receiver IF

Note



Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the analyzer to warm up for at least 30 minutes before you perform any procedure in this chapter.

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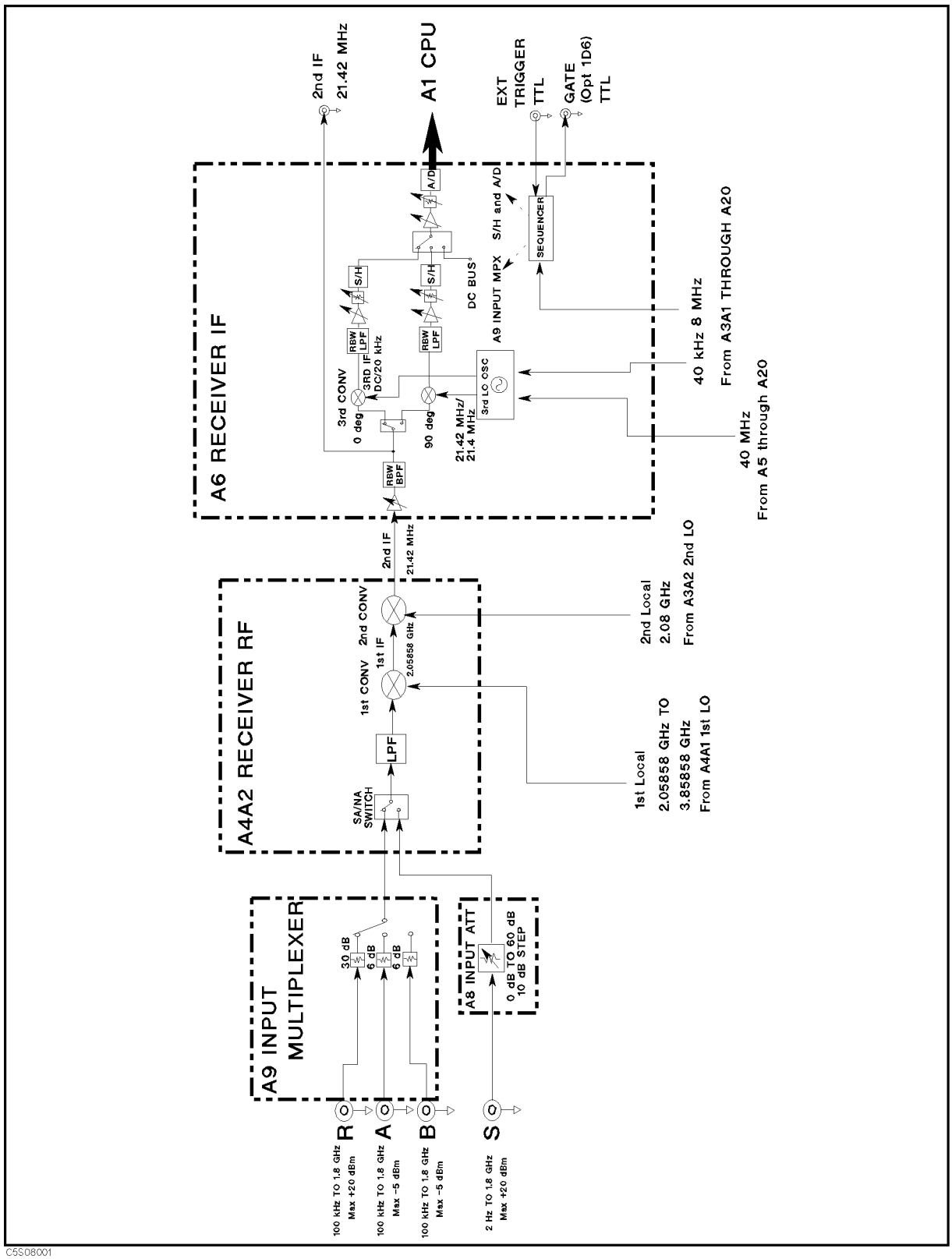


Figure 8-1. Receiver Group, Simplified Block Diagram

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RECEIVER GROUP TROUBLESHOOTING SUMMARY

This overview summarizes the sequence of checks included in this chapter. Experienced technicians may save time by following the summary instead of reading the entire procedure. Headings in this summary match the headings in the procedure.

Start Here

1. Run internal test 15. If the test fails, check if the internal test 11 passes. If internal test 11 passes, replace A6. If it fails, troubleshoot the source group.
2. Run internal test 5. If the test fails, replace A6.
3. Run internal test 12. If the test fails, replace A6.
4. Run internal test 14. If the test fails, replace A6.
5. Run external tests 53 through 57. If one (or more) of the tests fails, identify the most questionable assembly in accordance with Table 8-1. Then verify the control signals or signal inputs to the questionable assembly. The procedures to do this are provided in this chapter.

Check A8 Output Attenuator Control Signals

Check the A8 attenuation control signals. If the control signals are good, replace A8. If any control signal is bad, replace the A2 post-regulator.

Check A9 Input Multiplexer Control Signals

Check the A9 control signals. If the control signals are good, replace A9. If any control signal is bad, replace A6.

Check Signal Inputs to A4A2 Receiver RF

1. Check the input signals to A4A2J3. If the signals are good, continue with the next step. If the signals are bad, troubleshoot the source group.
2. Check the input signal to A4A2J12. If the signals are good, replace A4A2. If the signals are bad, troubleshoot the source group.

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START HERE

The following procedures verify the operation of each assembly in the receiver group by using the 4396B self-test functions (internal and external tests). For detailed information about the self-test functions, see the *Service Key Menus*.

Perform the following procedures sequentially to troubleshoot the receiver.

1. Press (Preset), (System), SERVICE MENUS, TESTS, (1), (5), (x1). EXECUTE TEST to run internal test 15: A6 SEQUENCER.
   - If the test fails, there is a possibility that he A3A1 ALC is faulty. Check if internal test 11: A3A1 DIVIDER passes. If the internal test 11 passes, replace A6. If it fails, troubleshoot the source in accordance with the *Source Group Troubleshooting* chapter.
2. Press (5) (x1), EXECUTE TEST to run internal test 5: A6 A/D CONVERTER. If the test fails, replace A6.
3. Press (1), (2), (x1), EXECUTE TEST to run internal test 12: A6 3RD LO OSC. If the test fails, replace A6.
4. Press (1), (4), (x1), EXECUTE TEST to run internal test 14: A6 3RD IF DC OFFSET. If the test fails, replace A6.
5. Run all of the ALL EXT tests (external tests 53 through 57). For the procedures, see the *Operator's Check* in the *Troubleshooting* chapter.

   If one (or more) of the ALL EXT tests fails, identify the questionable assemblies in accordance with Table 8-1. Table 8-1 lists the assembly to suspect first when an ALL EXT test fails. For example, if only the ALL EXT 5 test fails, suspect A6. If ALL EXT 1 and 5 pass but ALL EXT 2 through 4 fail, suspect A9. Table 8-1 lists some typical cases. In a few cases, another assembly may be faulty.

   If A6 is the most questionable assembly, replace A6. If another assembly is questionable, verify the input signals to the questionable assembly. The procedures to do this are provided in the following sections.

Table 8-1. Suspicious Assembly When an ALL EXT Test Fails

External Test	A8	A9	A4A2	A6
53: ALL EXT 1	√[1]		√	√
54: ALL EXT 2			√[2]	√[2]
55: ALL EXT 3		√[3]		
56: ALL EXT 4		√[3]		
57: ALL EXT 5				√[4]

1 If only external test 21 in the ALL EXT 1 fails, A8 is faulty.

2 There is a possibility that A9 is faulty.

3 There is a possibility that A4A2 or A6 is faulty.

4 There is a possibility that A8 or A4A2 is faulty.

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CHECK A8 INPUT ATTENUATOR CONTROL SIGNALS

Use this procedure when the A8 input attenuator is the most questionable assembly.

The A8 input attenuator (0 dB to 60 dB, 10 dB step) is used in the spectrum analyzer mode. A8 attenuates the RF signal coming from the S input. The attenuated signal goes to the A4A2 receiver RF. See the A8 block in Figure 8-1.

A8 is controlled by the three signals at A8J1, A8J2, and A8J3 (coming from the A2 post-regulator). The locations of A8J1, A8J2, and A8J3 are shown in Figure 8-2. Perform the following steps to verify the A8 control signals. If the control signals are good, replace A8. If any control signal is bad, replace A2.

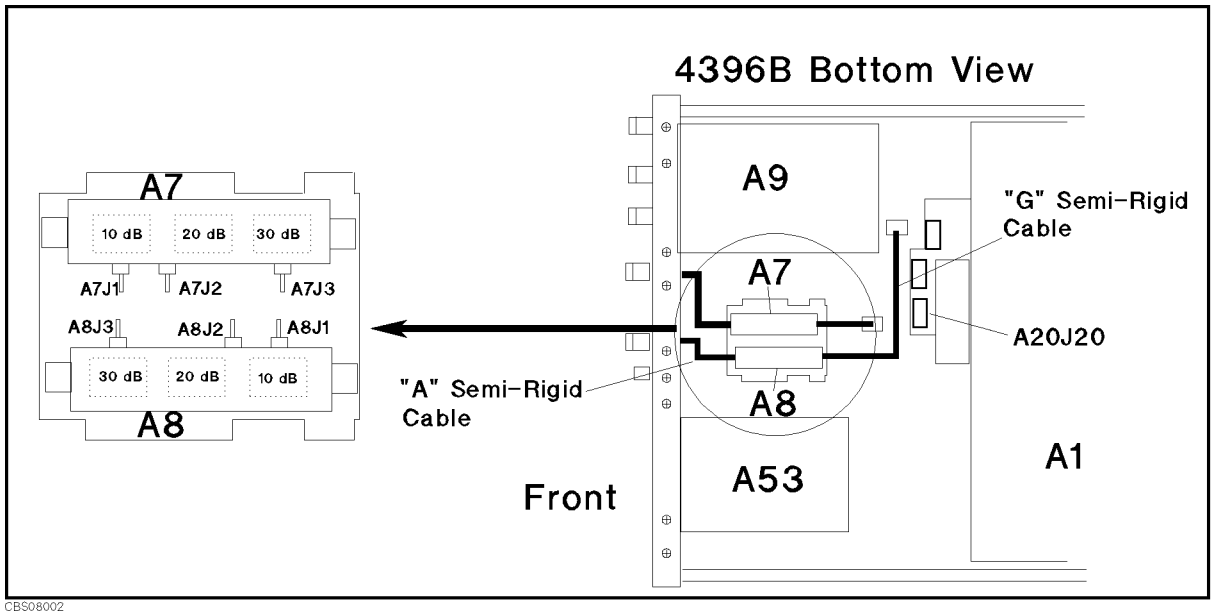


Figure 8-2. A8 Input Attenuator Control Signals

a. Press the following keys.

(Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset), (Scale Ref), ATTEN AUTO man (then the label changes to ATTEN auto MAN)

During this procedure, A8 is set to 10 dB.

b. On the 4396B, press ATTEN, 0, (x1) to set A8 to the first setting of 0 dB in Table 8-2.

c. Measure the voltage at A8J1, A8J2, and A8J3 using a voltmeter. Then check that the measured values are within the limits. The typical voltages are listed in Table 8-2.

- If the control voltages are good, continue with the next step.
- If the control voltages are bad, inspect the cable between A8 and A20J20. If the cable is good, the attenuator control circuit in the A2 post-regulator is probably faulty. Replace A2.

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Table 8-2. A8 Control Signal Test Settings

A8 Attenuation	A8J1 Voltage	A8J2 Voltage	A8J3 Voltage
0 dB	High[1]	Low[2]	Low
−10 dB	Low	Low	Low
−20 dB	High	High	Low
−30 dB	Low	High	Low
−40 dB	Low	Low	High
−50 dB	High	High	High
−60 dB	Low	High	High

1 Is within +8.4 V to +16 V (+12 V typically).

2 Is 0 V typically.

d. Repeat steps b and c to set A8 in accordance with Table 8-2.

At this point, the A8 attenuator control signals are verified.

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CHECK A9 INPUT MULTIPLEXER CONTROL SIGNALS

Use this procedure when the A9 Input Multiplexer is the most questionable assembly.

A9 consists of the multiplexer and three fixed attenuators. See the A9 block in Figure 8-1. The multiplexer connects one of the R, A, or B inputs to the A4A2 receiver RF and is controlled by three signals at A9J13 coming from the A6 Receiver IF.

Perform the following procedures to verify the multiplexer control signals at A9J13. If the control signals are good, replace A9. If the control signals are bad, replace A6.

The location of A9J13 and its pin assignments are shown in Figure 8-3 and Table 8-3. Perform the following steps to verify the A9 control signals:

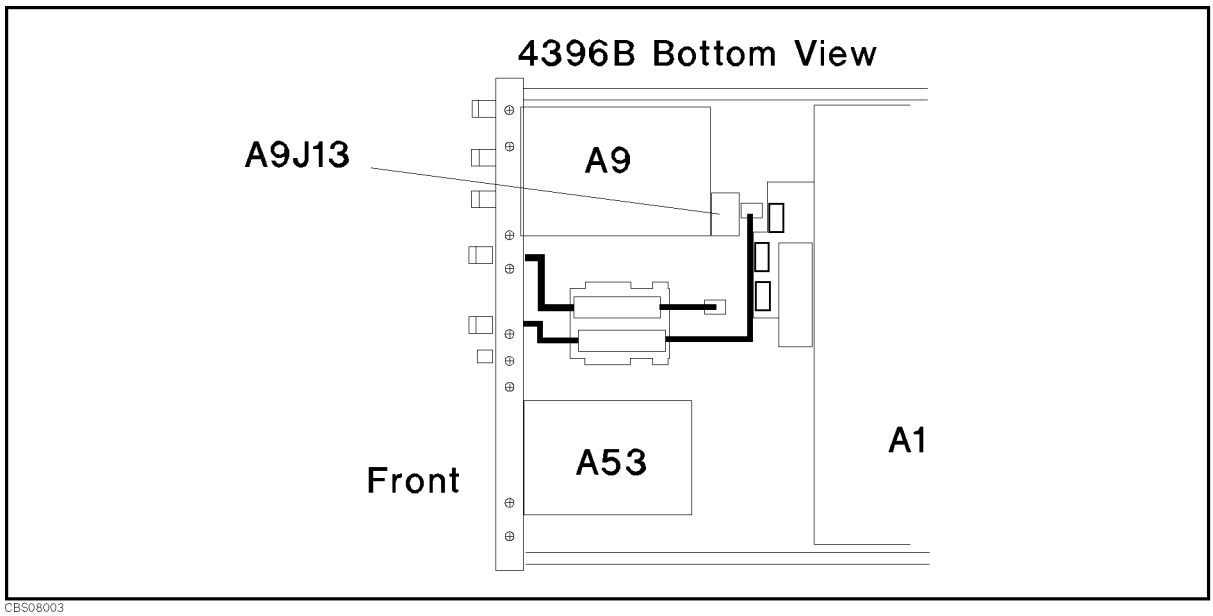


Figure 8-3. A9J13 Location and Pin Assignments

a. Press the following keys:

(Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset), (Sweep), SWEEP TIME, (1), (0), (0), (x1)

b. Measure the power supply voltages at pins 1, 2, and 6 through 8 of A9J13 using an oscilloscope. Then check that the measured values are within the limits. The typical voltages are listed in Table 8-3.

- If the voltages are good, continue with the next step.
- If the voltages are bad, inspect the cable between A9J13 and A20J14. If the cable is good, the A2 post-regulator is probably faulty. Replace A2.

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Table 8-3. A9J13 Pin Description

Pin	Description
1	+15 V Power Supply
2	−15 V Power Supply
3	R Input Select (TTL Level)
4	A Input Select (TTL Level)
5	B Input Select (TTL Level)
6 through 8	GND (0 V)

c. Press (Meas), R to select the R input. Then measure the voltages at pins 3, 4, and 5 of A9J13 using an oscilloscope. Check that the measured values are within the limits. The typical voltages are listed in Table 8-4.

- If the voltages are good, continue with the next step.
- If the voltages are bad, inspect the cable between A9J13 and A20J14. If the cable is good, the A6 receiver IF is probably faulty. Replace A6.

Table 8-4. A9 Control Signal Test Settings

Input	A9J13 Pin 3	A9J13 Pin 4	A9J13 Pin 5
R	High[1]	Low[2]	Low
A	Low	High	Low
B	Low	Low	High

1 is typically +5 V (TTL level).

2 is typically 0 V (TTL Level).

d. Change the input in accordance with Table 8-4. Repeat step c for each setting.

If all of checks above are good, the A9 control signals are verified.

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CHECK SIGNAL INPUTS TO THE A4A2 RECEIVER RF

Use this procedure when the A4A2 receiver IF is the most questionable assembly.

A4A2 consists of the NA/SA Switch, the first converter, and the second converter. See the A4A2 block in Figure 8-1. Perform the following procedures to verify the input signals to A4A2. If the signals are good, replace A4A2.

Check the Input Signal to A4A2J3

The input signal to A4A2J3 is the first local oscillator signal (2.05858 GHz to 3.85858 GHz) coming from the A4A1 1st LO. Verify the signal in accordance with the *Check the 1st LO OSC Signal at A4A1J4.* in the *Source Group Troubleshooting* chapter.

- If the input signal to A4A2J3 is good, continue with the *Check the 2nd LO OSC Signal at A4A2J12.*
- If the input signal to A4A2J3 is bad, inspect the "F" semi- rigid cable between A4A2J3 and A4A1J4. If the cable is good, continue with the *Check A4A1 1st LO Outputs* in the *Source Group Troubleshooting* chapter.

Check the Input Signal to A4A2J12

The input signal to A4A2J12 is the 2.08 GHz second local oscillator signal from the A3A2 2nd LO. Verify the signal in accordance with the *Check the 2nd LO Signal* in the *Source Troubleshooting* chapter.

- If the input signal to A4A2J3 is good, all input signals to A4A2 are verified.
- If the input signal to A4A2J3 is bad, inspect the "I" semi- rigid cable between A4A2J12 and A3A2J3. If the cable is good, continue with the *Check A3A2 2nd LO Outputs* in the *Source Group Troubleshooting* chapter.

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9

Accessories Troubleshooting

INTRODUCTION

Use these procedures only if you have followed the troubleshooting procedures and believe the problem is one of the accessories. Reconfigure the system as it is normally used and reconfirm the measurement problem. The measurement problem must be caused by a failure outside of the analyzer (that is, by one of the accessories).

Suspect the following typical problems:

- Operation Errors (for example, too high an input level in the spectrum measurement or improper calibration techniques in the network measurement.
- Faulty Accessories (for example, damaged adapters and RF cables in the spectrum and network measurements, a faulty power splitter, T/R test set, or S-Parameter Test Set in the network measurement).

This chapter consists of the following procedures. Perform these procedures sequentially.

VERIFY OPERATIONS
INSPECT CONNECTORS
INSPECT ACCESSORIES

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VERIFY OPERATIONS

The measurement problem can be caused by improper operation. Confirm that all operations, connections and control settings, etc., are properly made during the measurement. For detailed information about proper operations, see the following manuals:

Task Reference (p/n 04396-90020)
User's Guide (p/n 04396-90021)
Function Reference (p/n 04396-90022)
Programming Guide (p/n 04396-90023)
GPIB Command Reference (p/n 04396-90024)

Some examples of the typical operation errors are shown in the following paragraph.

Using 75 Ω Connectors with 50 Ω Connectors

Do not use 50 Ω connectors with 75 Ω connectors; their center conductors are different diameters. Using a 50 Ω male connector with a 75 Ω female connector will destroy the female connector.

Large Spurious Signals in the Spectrum Measurement

Large spurious signals around the fundamental signal can be caused by an input signal level that is higher than the reference level. Reducing the input signal level or setting the reference level higher can solve the spurious signal problem.

Odd Appearing Opens and Shorts in the Network Measurement

Opens and shorts can appear as short lines (rather than the expected points) on a Smith Chart. This is a result of some shorts and opens being offset. See the calibration kit manual to determine the offset. To verify the opens and shorts, see *Verify Shorts and Opens* in the *Inspect the Calibration Kit* procedure later in this chapter.

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INSPECT THE CONNECTORS

Check the physical condition of the analyzer front-panel connectors, the calibration kit devices, and the test set connectors.

1. Inspect the front panel connectors on the analyzer. Check for bent or broken center pins and loose connector bulkheads.

   Gage the connectors. (Gage kit is Agilent part number 85054-80011.) The specified front-panel type-N connector center pin **protrusion** is 0.201 to 0.207 inch.

   If the center pin protrusion is incorrect, replace the entire connector assembly, S input assembly, or A9 input multiplexer. See the *Replaceable Parts* chapter.

2. Inspect the calibration kit devices for bent or broken center conductors and other physical damage. Gage each device. The mechanical specifications for each device are given in the calibration kit manual.

   If any calibration device is out of mechanical tolerance, replace the device.

3. Inspect and the gage test set and the power splitter connectors as described in steps 1 and 2.

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INSPECT THE ACCESSORIES

Measurement problems can be caused by faulty accessories or faulty devices between the accessories and the analyzer. For example, the RF cables, the probe power connector, the TEST SET-I/O INTERCONNECT connector, and the interconnect cable can cause problems.

Some recommended accessories used with the analyzer are listed below. For more information about the accessories, see Chapter 9 in the *Function Reference* (p/n 04396-90022).

- Test Sets (for example, the 85046A/B S Parameter Test Set).
- Active Probes (for example, the 41800A Active Probe).
- Preamplifier (for example, the 19855A Broadband Preamplifier).
- Power Splitter and Directional Bridges (for example, the 11850C/D Three-way Power Splitter).
- Calibration Kits (for example, the 85032B 50 Ω Type-N Calibration Kit).

Inspect the cables for any damage. Verify the probe power connector and the TEST SET-I/O INTERCONNECT connector (if they are used). Then inspect and verify the accessories that are used in the measurement.

This inspection consists of the following procedures:

Verify the Probe Power
Inspect the Test Set
Inspect the Calibration Kit

Verify the Probe Power

Perform the following procedure to verify the front-panel probe power connector:

1. Turn the analyzer power off.
2. Remove the power cable of the accessory from the probe power connector.
3. Turn the analyzer power on.
4. Measure the power voltages (+15 V and -12.6 V) at the probe power connector using a voltmeter with a small probe. See Figure 9-1 for the voltages and pins on the probe power connector.
   - If the voltages are within the limits, the analyzer's probe power is verified. Suspect a faulty accessory. Verify the accessory used in the measurement problem in accordance with its manual.
   - If the voltages are out of the limits, see the *Power Supply Troubleshooting* chapter in this manual to troubleshoot the power lines (+15 V(AUX) and -12.6 V) of the probe power.

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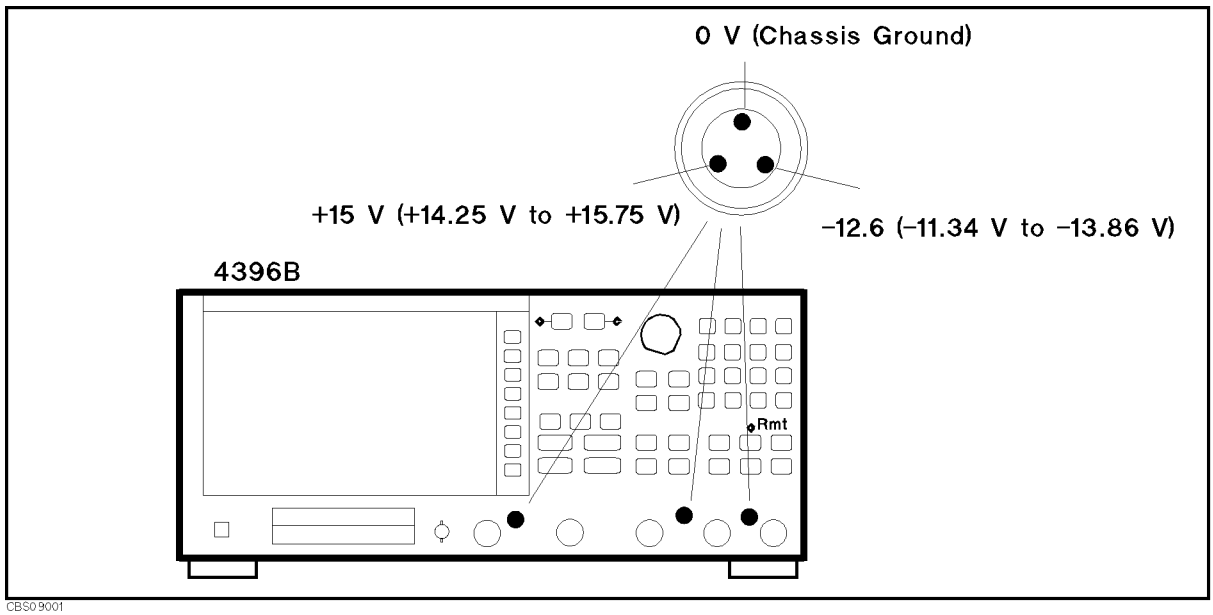


Figure 9-1. Probe Power Connector Voltages

Inspect the Test Set

This procedure checks the operation of the RF transfer switch in the 85046A/B test set.

1. Turn the analyzer power off.
2. Connect the test set to the analyzer.
3. Turn the analyzer power on.
4. Press (PRESET), (Meas), `ANALYZER TYPE`, `NETWORK ANALYZER`, `Refl: REV S22(B/R)`. Then check that the S22 S12 indicator LED lits.
5. Press `Refl: FWD S11 (A/R)`. Check that the S11 S21 indicator LED lits.

   - If the LED operations are not expected, inspect the cable between the analyzer and the test set. If the cable seems good, verify the test set in accordance with its manual.
   - If the LED operations are correct, continue with this chapter unless a test set failure is suspected. To troubleshoot test set failures, see the test set manual.

Inspect the Calibration Kit

Inspect all of the terminations (load, open, and short) for any damage. If no damage is found, perform the following procedure to verify the short and open. If any damage is found, replace the termination with a good one.

Verify Shorts and Opens

Substitute a known good short and open of the same connector type as the terminations in question. If the devices are not from a standard calibration kit, see *Modifying Calibration Kits* in the *Function Reference* to use the `MODIFY [CAL KIT]` function. Set aside the short and open that could be causing the problem.

1. Perform an S11 1-port calibration on a port using the good short and open. Then press (Format), `SMITH CHART` to view the devices in Smith chart format.

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2. Connect the good short to the calibrated port. Press Scale Ref, ELEC DELAY MENU, ELECTRICAL DELAY and turn the RPG to enter enough electrical delay so that the trace appears as a dot at the left side of the circle.

   Replace the good short with the questionable short at the port. The trace of the questionable short should appear very similar to the known good short.

3. Connect the good open to the calibrated port. Press Scale Ref, ELEC DELAY MENU, ELECTRICAL DELAY and turn the RPG to enter enough electrical delay so that the trace appears as a dot at the right side of the circle.

   Replace the good open with the questionable open at the port. The trace of the questionable open should appear very similar to the known good open.

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10

Service Key Menus

INTRODUCTION

The service key menus are used to test, verify, adjust, and troubleshoot the analyzer. They are also used to install and update the firmware in the analyzer.

The service key menus consist of several menus that are accessed through the service menu and the Bootloader menu as shown in Figure 10-1. The service menu is displayed by pressing (System), SERVICE MENU. The Bootloader menu is displayed by turning the analyzer power on while pressing (Start) and (Preset).

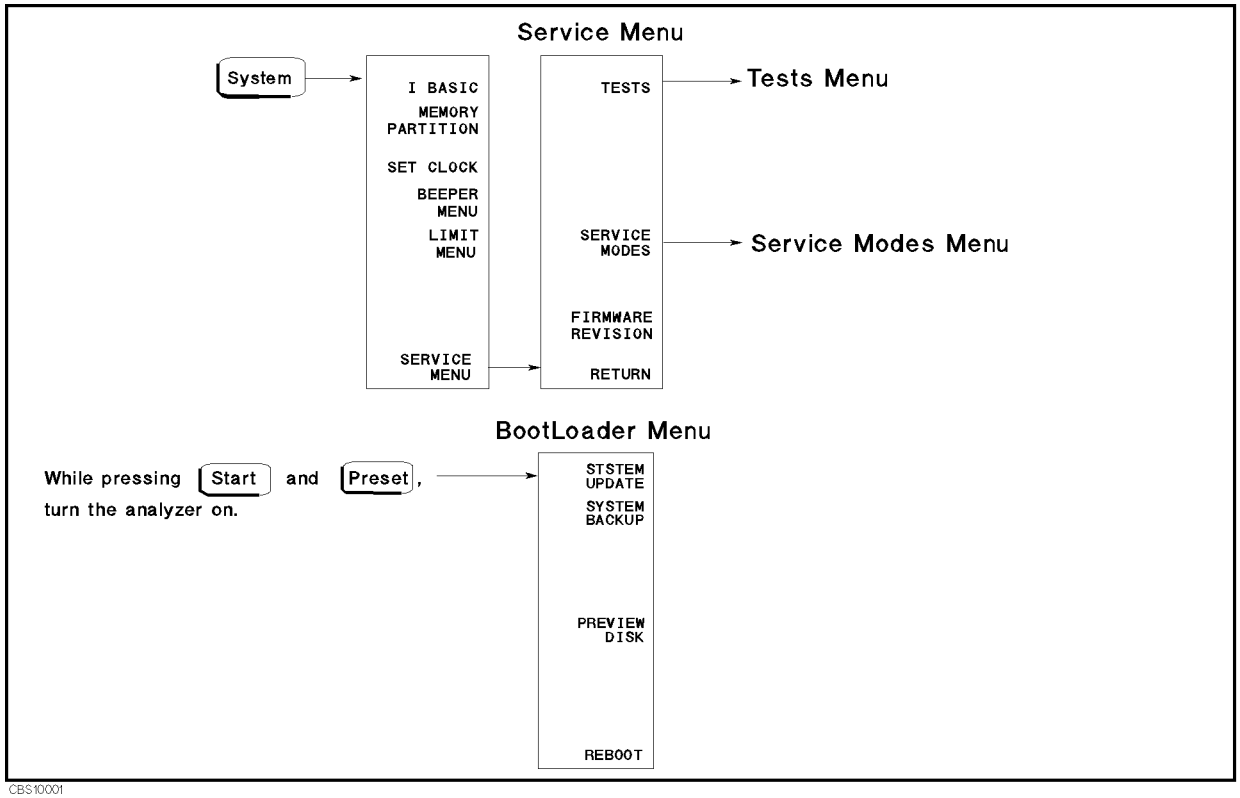


Figure 10-1. Service Key Menus

The service key menus allow you to perform the following functions:

- Select and execute a built-in diagnostic test. The analyzer has 59 built-in diagnostic tests. For detailed information, see the *Tests Menu* in this chapter.
- Control and monitor various circuits for troubleshooting. For detailed information, see the *Service Modes Menu* in this chapter.
- Display the firmware revision. See the *Service Menu* in this chapter.

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- Install and update the firmware in the analyzer. For detailed information, see the *Bootloader Menu* in this chapter.

When applicable, the GPIB mnemonic is written in parentheses following the softkey using the following symbol conventions:

{ }	A necessary appendage
<*numeric*>	A necessary numerical appendage
|	A delimiter for applicable appendages. For example, {OFF|ON|0,1|} means OFF, ON, 0, or 1.

For more information about the GPIB commands, see the *4396B GPIB Command Reference*.

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SERVICE MENU

Figure 10-2 shows the service menu. This menu is used to display the tests menu, the service modes menu, and the firmware revision information. To display the service menu, press (System), SERVICE MENU. Each softkey in the service menu is described below.

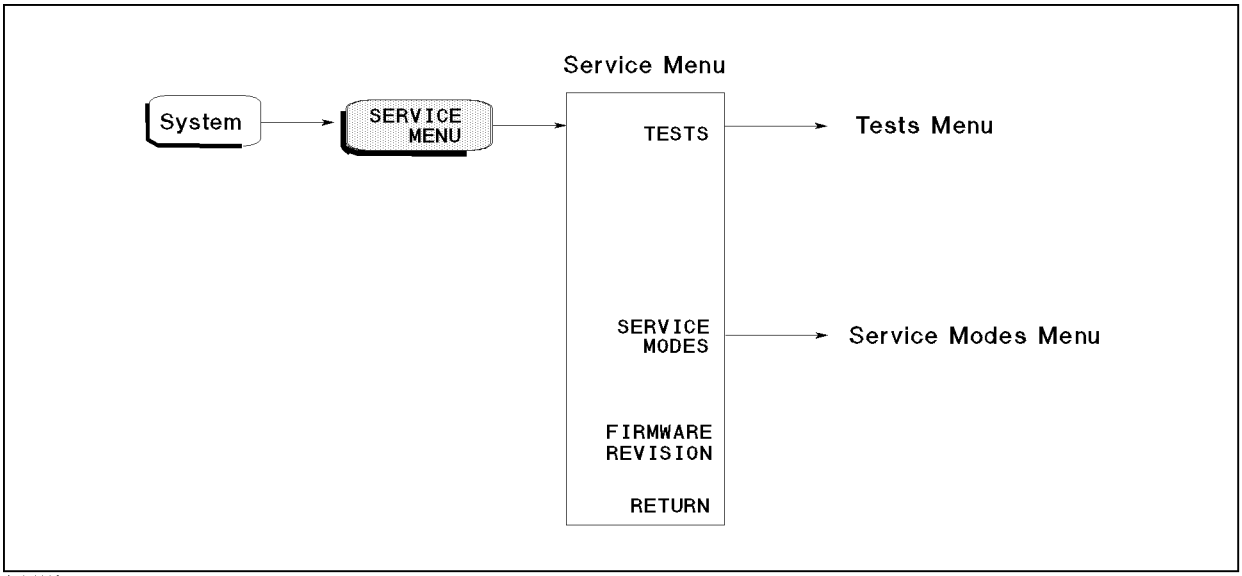


Figure 10-2. Service Menu

TESTS

Displays the tests menu. For more information about the tests menu, see the *Tests Menu* later in this chapter.

SERVICE MODES (:DIAG:SERV:MODE {ON|1})

Activates the service modes and displays the service modes menu. For more information about the service modes menu, see the *Service Modes Menu* later in this chapter.

FIRMWARE REVISION (:DIAG:FREV?)

Displays the current firmware revision information. The number and implementation date appear in the active entry area of the display as shown below. Another way to display the firmware information is to cycle the analyzer power (off then on).

```
4396B REVN.NN MON DD YEAR HH:MM:SS
```

where	N.NN:	Revision Number
	MON DD YEAR	Implementation Date (Month Day Year)
	HH:MM:SS	Implementation Time (Hour:Minute:Second)

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TESTS MENU

Figure 10-3 shows the tests menu. The tests menu is used to select and execute one of the 59 built-in diagnostic tests. More information about the diagnostic tests is provided in the *Diagnostic Tests* later in this section. To display the tests menu, press System, SERVICE MENU, and TESTS.

When entering the tests menu, internal test 0: ALL INT is selected as the default test. The test number, name, and status abbreviation is displayed in the active entry area of the display. For the test status, see Figure 10-4.

The diagnostic tests are numbered from 0 to 58. To select a test, enter the desired test number using the numeric keypad, ↑, ↓, RPG knob or GPIB command (:DIAG:TEST <*numeric*>).

Each softkey in the tests menu is described below.

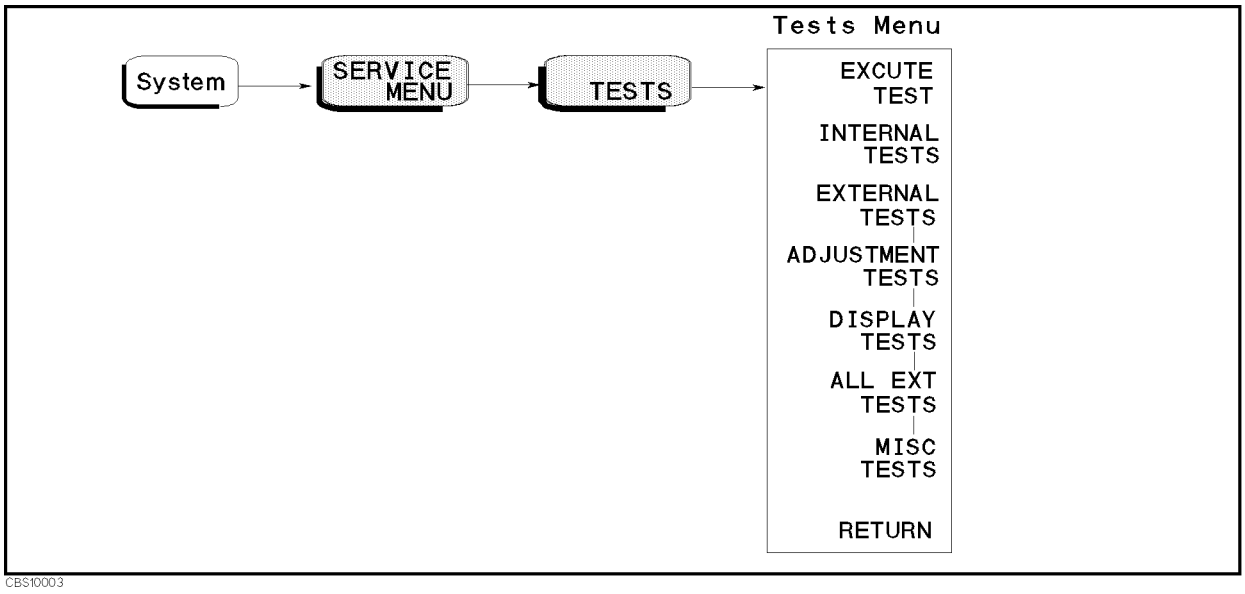


Figure 10-3. Tests Menu

EXECUTE TEST (:DIAG:TEST:EXET)

Runs the selected test. When the executed test requires user interaction, CONT (:DIAG:TEST:CONT) and the instruction appear on the display. Follow the displayed instruction and press CONT to continue the test.

INTERNAL TESTS (:DIAG:TEST 0)

Selects the first internal test 0: ALL INT.

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EXTERNAL TESTS (:DIAG:TEST 17)

Selects the first external test 17: FRONT PANEL DIAG.

ADJUSTMENT TESTS (:DIAG:TEST 41)

Selects the first adjustment test 41: DC OFFST/HLD STEP ADJ.

DISPLAY TESTS (:DIAG:TEST 48)

Selects the first display test 48: TEST PATTERN 1.

ALL EXT TESTS (:DIAG:TEST 53)

Selects the first ALL EXT test 53: ALL EXT 1.

MISC TESTS (:DIAG:TEST 58)

Selects the first MISC tests 58: IMPEDANCE TEST KIT.

Note

After executing a test by pressing EXECUTE TEST, an annotation (Svc) is displayed to indicate any tests executed and the analyzer settings changed to the test settings. To return the analyzer to normal operation, cycle the analyzer power (off then on), or press (PRESET).

Note

While any test is being executed, do not change the analyzer setting using the front-panel keys, the GPIB, or the I-BASIC program . If the setting is changed during test execution, the test result and the analyzer operation are undefined.

Test Status

When selecting a test, the test status abbreviation is displayed as shown in Figure 10-4.

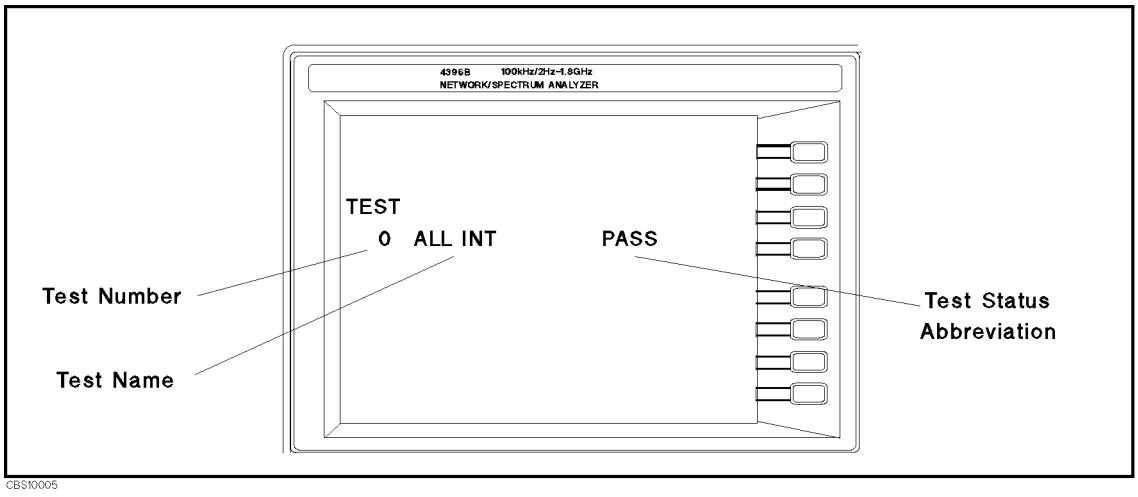


Figure 10-4. Test Status on the Display

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To see the test status of the desired test, enter the desired test number using the numeric keypad, ⇧, ⇩, or RPG knob. Also, the three GPIB commands listed below are available to get the test status using GPIB.

`:DIAG:TEST:RES?` <*numeric*>	returns the test status. The <*numeric*> specifies the test number and is an integer from 0 to 58.
`*TST?`	executes internal test 0: ALL INT and returns the test result.
`:DIAG:INIT:RES?`	returns the power on self-test result.

A sample program using the command `:DIAG:TEST:RES?` is shown in Figure 10-5. This program displays the test status of internal test 1. See the *4396B GPIB Command Reference* for more information.

```
10    !
20    ASSIGN @Hp4396 TO 717 ! When iBASIC is used, replace "717" to "800."
30    !
40    OUTPUT @Hp4396;"DIAG:TEST:RES? 1"
50    ENTER @Hp4396;Test_status$
60    PRINT Test_status$
70    !
```

Figure 10-5. Sample Program Using `:DIAG:TEST:RES?`

Table 10-1 shows the test status abbreviation, its definition, and the GPIB test status code.

Table 10-1. Test Status Terms

Status Abbreviation	Definition	GPIB Code
PASS	Pass	"PASS"
FAIL	Fail	"FAIL"
-IP-	In progress	"BUSY"
-ND-	Not done	"NDON"
DONE	Done	"DONE"

The test status is stored in nonvolatile memory (battery backup memory). If the power to the nonvolatile memory is lost, the analyzer will set all test status abbreviations to "-ND-" (not done). If a test is aborted by pressing any key during its execution, the test status is undefined.

Diagnostic Tests

The analyzer has 59 built-in diagnostic tests. The analyzer performs the power on self-test every time the power on sequence occurs (when the analyzer is turned on). These tests are used to test, verify, adjust, and troubleshoot the analyzer.

The 59 built-in diagnostic tests are divided by function into six categories: internal tests, external tests, adjustment tests, display tests, ALL EXT tests and MISC tests. Each group is described below. Descriptions of the tests in each category are given in the *Test Descriptions* section. To access the first test in each category, the category softkey is available in the tests menu.

The power on self-test consists of internal tests 1, 4, 5, 6, 7, and 9 through 16. They are executed in the listed order. If any of the tests fail, that test displays a "`POWER ON TEST`

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FAILED" message at the end of the power on sequence. The first failed test indicates the most probable faulty assembly.

Internal Test	These tests are completely internal and self-evaluating. They do not require external connections or user interaction. The analyzer has 16 internal tests.
External Tests	These are additional self-evaluating tests. However, these tests require some user interaction (such as key entries). The analyzer has 24 external tests.
Adjustment Tests	These tests are used to adjust the analyzer. See the *Adjustments and Correction Constants* chapter. The analyzer has 7 adjustment tests.
Display Tests	These tests are used to adjust and check for proper operation of the display circuits. See the *Adjustments and Correction Constants* chapter. The analyzer has 5 display tests.
ALL EXT Tests	These tests are used to perform the Operator's Check. See the *Troubleshooting* chapter. The analyzer has 5 ALL EXT tests.
MISC Tests	The tests are used to evaluate 43961A RF Impedance Test Kit.

Test Descriptions

This section describes all 59 diagnostic tests.

INTERNAL TESTS

This group of tests run without external connections or operator interaction. All return a "PASS" or "FAIL" indication on the display. Except as noted, all are run during the power on self-test and when Preset pressed.

0: ALL INT

Runs only when selected. It consists of internal tests 1 and 4 through 16. If any of these tests fail, this test displays the "FAIL" status indication. Use the RPG knob to scroll through the tests to see which test failed. If all pass, the test displays the "PASS" status indication. Each test in the subset retains its own test status.

1: A1 CPU

Verifies the following circuit blocks on the A1 CPU:

- Digital Signal Processor (DSP)
- System Timer
- Real Time Clock
- Front Key Controller
- Flexible Disk Drive Controller
- GPIB Controller
- EEPROM

2: A1 VOLATILE MEMORY

Runs only when selected. It verifies the A1 volatile memories:

CPU internal SRAM
DSP SRAM
Dual Port SRAM
Backup SRAM

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At the end of the test, the analyzer is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

If the test fails, the test displays an error message for a few seconds and then sets the analyzer to the default state. The error message indicates the faulty memory.

3: A51 GSP

Runs only when selected. It verifies the following circuit blocks on the A51 GSP:

GSP Chip
DRAM
VRAM

When this test starts, Ch 1 LED and Ch 2 LED are turned off. At the end of this test, the analyzer is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

If the test fails, the test indicates the faulty circuit using the Ch 1 LED, the Ch 2 LED, and beeps. It then sets the analyzer to the default state. If the GSP chip is faulty, a beep sounds and the LEDs blink once. If the DRAM is faulty, two beeps sound and the LEDs blink twice. If the VRAM is faulty, three beeps sound and the LEDs blink three times.

4: A2 POST REGULATOR

Verifies all A2 post regulator output voltages:

+5 V(AUX), +15 V(AUX)
−15 V, −12.6 V, −5 V, +5 V, +5.3 V, +8.5 V, +15 V,
+22 V, FAN POWER, GND

This test measures the A2 output voltages at DC bus nodes 1 through 12, and 26. It checks that each measured value is within limits.

5: A6 A/D CONVERTER

Verifies the following circuit blocks on the A6 Receiver IF:

A/D Converter
Gain Y
Gain Z
Range R

This test measures the A/D converter's reference voltage (VREF) at DC bus node 25 through the gain Y, the gain Z, and the range R. These circuits are set to several settings in the test. For each setting, this test checks that the measured value is within limits.

6: A5 REFERENCE OSC

Verifies the reference oscillator in the A5 synthesizer. This test measures the VCO tuning voltage at DC bus node 22 and the frequency (2.5 MHz) at frequency bus node 6. It then checks that each measured value is within limits.

7: A5 FRACTIONAL N OSC

Verifies the fractional N oscillator in the A5 synthesizer. This sets the oscillator frequency to several frequencies over the entire range. For each setting, this test measures the VCO tuning voltage at DC bus node 20 and the frequency at frequency bus node 4. It then checks that each measured value is within limits.

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8: A5 STEP OSC

Runs only when selected. It verifies the step oscillator in the A5 synthesizer. This test sets the oscillator frequency to several frequencies over the entire range. For each frequency, the test measures the VCO tuning voltage at DC bus node 19 and the frequency at frequency bus node 3. It then checks that each measured value is within limits.

9: A4A1 1ST LO OSC

Verifies the 1st LO oscillator in the A4A1 1st LO. This test sets the oscillator frequency to several frequencies over the entire range. For each frequency, the test measures the VCO tuning voltage at DC bus node 18 and checks that each measured value is within limits.

10: A3A2 2ND LO OSC

Verifies the 2nd LO oscillator in the A3A2 2nd LO. This test measures the VCO tuning voltage at DC bus node 14 and checks that the measured value is within limits.

11: A3A1 DIVIDER

Verifies the divider circuit in the A3A1 ALC. This test measures the frequency (40 kHz) at frequency bus node 2 and checks that the measured value is within limits.

12: A6 3RD LO OSC

Verifies the 3rd LO oscillator on the A6 receiver IF. This test measures the VCO tuning voltage at DC bus node 23 and the frequency (40 kHz) at frequency bus node 6. It then checks that each measured value is within limits.

13: A3A1 SOURCE OSC

Verifies the source oscillator in the A3A1 ALC. This test measures the VCO tuning voltage at DC bus node 13 and the frequency (40 kHz) at frequency bus node 1. It then checks that each measured value is within limits.

14: A6 3RD IF DC OFFSET

This test measures the DC offset voltages on the 0° and 90° paths in the A6 receiver IF and checks that each measured value is within limits.

15: A6 SEQUENCER

Verifies the A/D sequencer circuit in the A6 receiver IF. This test measures the frequency (80 kHz) of the A/D sequence output at frequency bus node 7 and checks that the measured value is within limits.

16: A3A1 ALC

Verifies the ALC (automatic leveling control) circuit in the A3A1 ALC. This test varies the power level and frequency of the RF OUT signal. For each setting, the test measures the voltage at DC bus nodes 15 and 17 and checks that each measured value is within limits.

EXTERNAL TESTS

This group of tests require either external equipment and connections or operator interaction to run. These tests are used in the *Troubleshooting* chapter.

There are five test setups (1 through 5) for the external tests as shown in Figure 10-6 through Figure 10-10. If required, the external test description indicates the test setup used in that external test.

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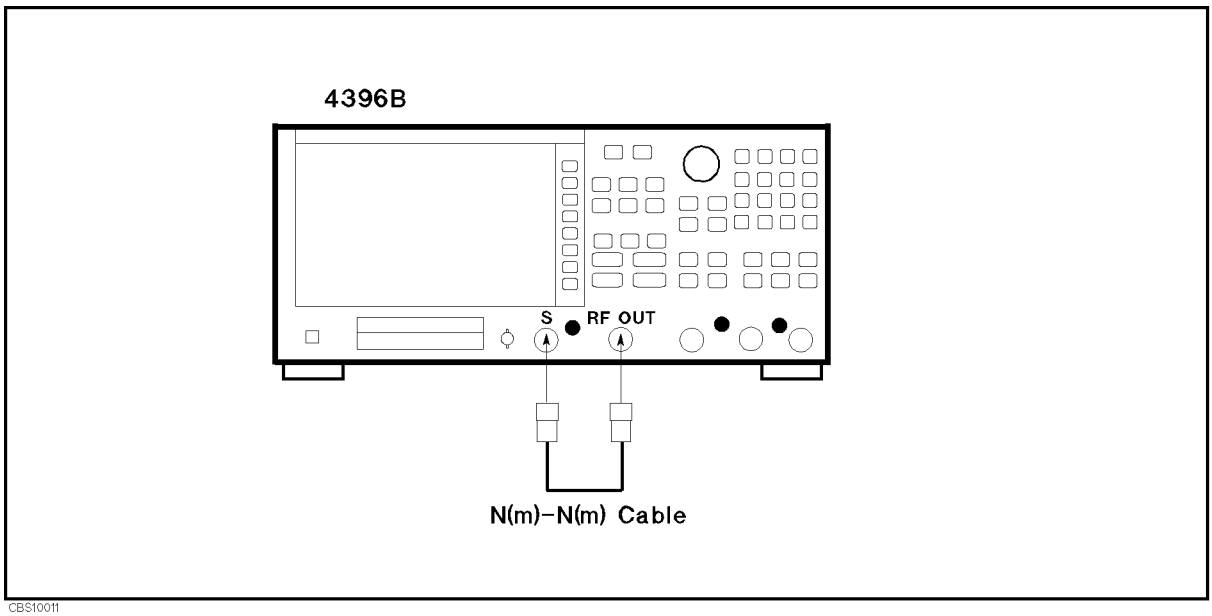


Figure 10-6. External Test Setup 1

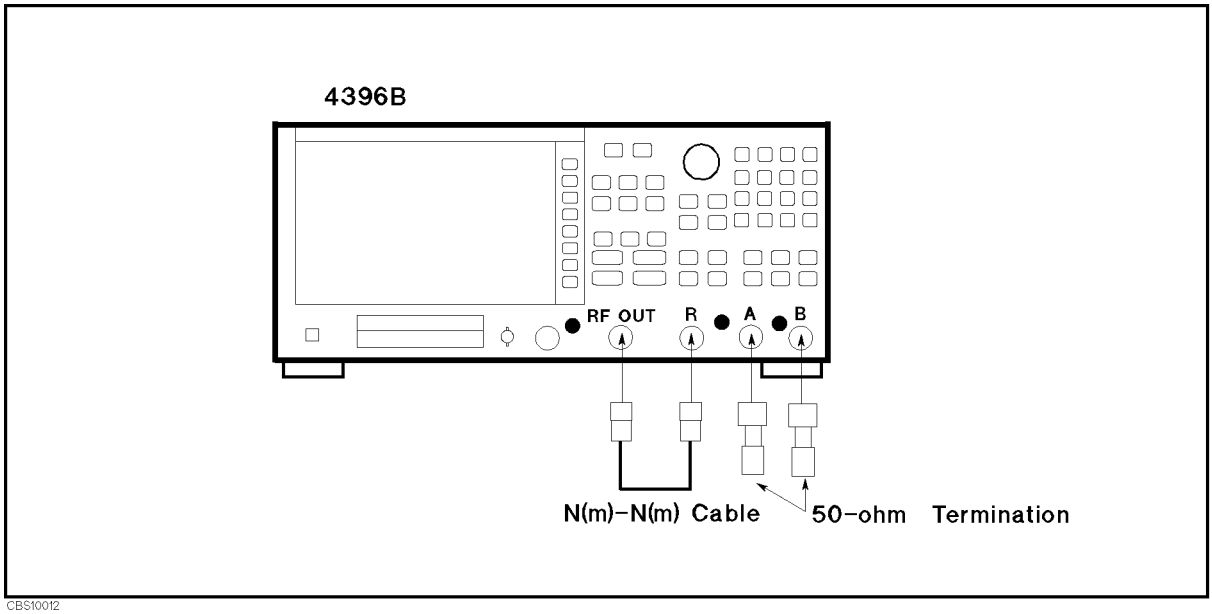


Figure 10-7. External Test Setup 2

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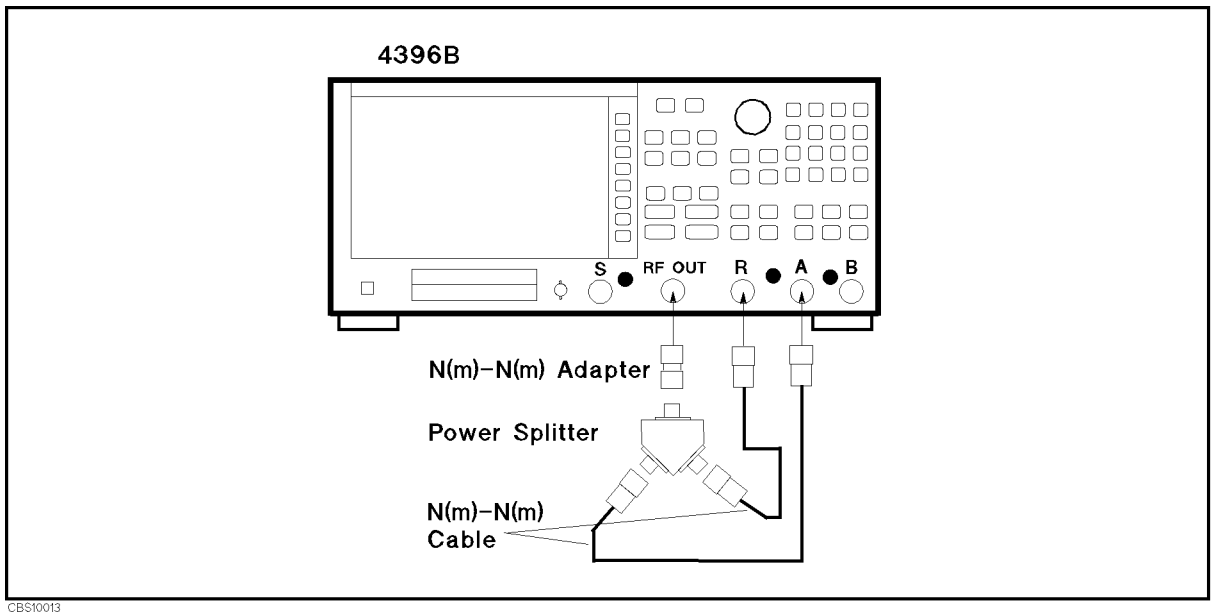


Figure 10-8. External Test Setup 3

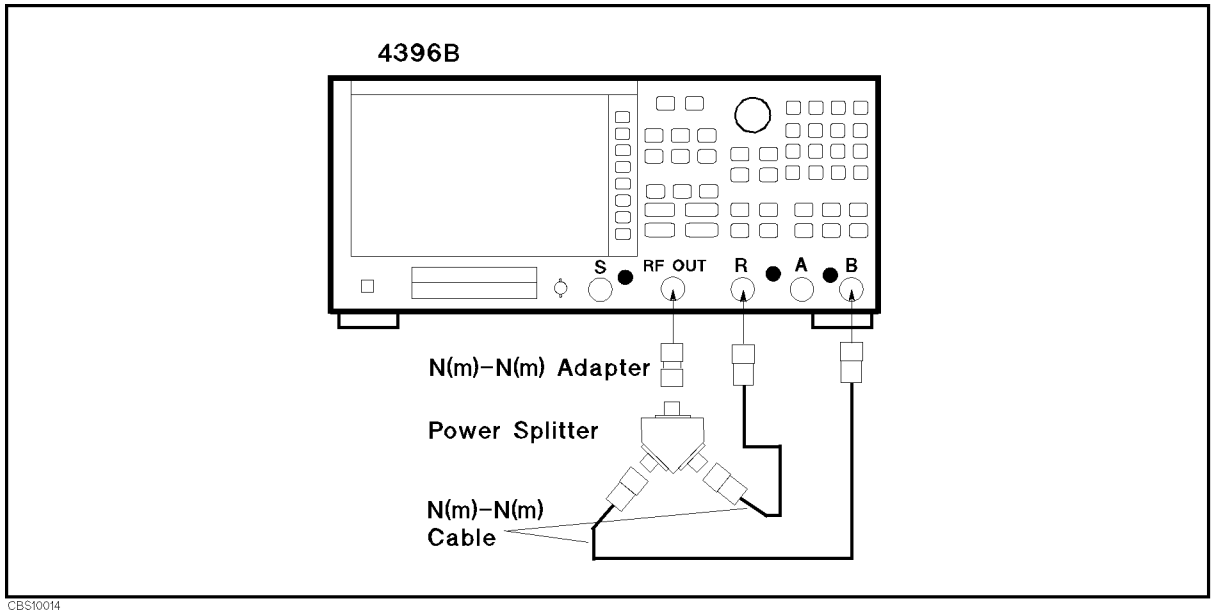


Figure 10-9. External Test Setup 4

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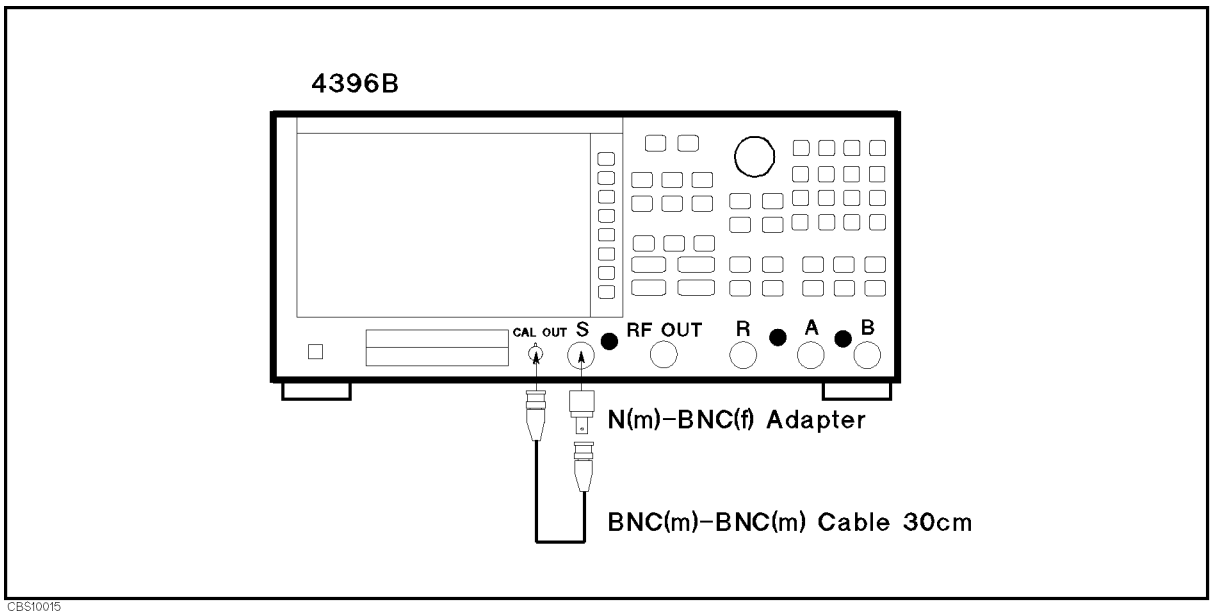


Figure 10-10. External Test Setup 5

17: FRONT PANEL DIAG.

Checks the RPG and all front-panel keys on the A30 keyboard. The abbreviated name is displayed when pressing one of the keys or rotating the RPG.

18: DSK DR FAULT ISOL'N

Checks the FDD (Flexible Disk Drive). When this test is started, a bit pattern is written to the flexible disk. Then the pattern is read back and checked. This write pattern check is repeated from the low to high addresses.

Note After this test is performed, the data stored on the floppy disk is lost.

19: POWER SWEEP LINEARITY

Checks that the power sweep linearity is within limits. As a result, the A3A1 ALC, A3A2 2nd LO, and A3A3 are verified.

External test setup 2 (shown in Figure 10-7) is used in this test. This test measures the RF OUT levels in the power sweep mode over its entire span. The R input is used to measure the RF OUT level.

20: OUTPUT ATTENUATOR

Checks that the A7 attenuation accuracy relative to the 10 dB setting and the frequency response of the attenuation are within limits. As a result, the A7 output attenuator is verified.

External test setup 2 (shown in Figure 10-7) is used in this test. This test sets the output attenuator over its entire setting range by changing the RF OUT level. For each setting, the RF OUT signal level is measured using the R input over the appropriate frequency range.

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21: INPUT ATTENUATOR

Checks that the A8 attenuation accuracy relative to the 10 dB setting and the frequency response of the attenuation are within limits. As a result, the A8 input attenuator is verified.

External test setup 1 (shown in Figure 10-6) is used in this test. The test sets the RF OUT level to a constant level and varies the input attenuator setting at the S input over its entire range of settings. For each setting, the RF OUT signal level is measured using the S input over the appropriate frequency range.

22: RF TO S LVL & FLTNESS

Checks that the level accuracy and flatness of the RF OUT signal are within limits. As a result, the A3A1 ALC, A3A2 2nd LO, A3A3 source, A4A2 receiver RF, and A6 receiver IF are verified.

External test setup 1 (shown in Figure 10-6) is used in this test. The test sets the RF OUT level to a constant level and measures the RF OUT level using the S input over the appropriate frequency range.

23: S TO A CROSSTALK

Checks that the input crosstalk from the S input to the A input and source crosstalk into the A input are within limits. As a result, the NA/SA switch circuit in A4A2 receiver RF is verified.

External test setup 1 (shown in Figure 10-6) is used in this test. The test sets the RF OUT level to a constant level and measures the level using the S input over the appropriate frequency range.

24: S INPUT COMPRESSION

Checks that the input compression at the S input is within limits. As a result, the A4A2 receiver RF and A6 receiver IF are verified.

External test setup 1 (shown in Figure 10-6) is used in this test. The test sets the RF OUT level to several levels and measures the levels using the S input over the appropriate frequency range.

25: S INPUT RESIDUALS

Checks that the residual response at the S input is lower than the limit. As a result, the A4A1 1st LO, A4A2 receiver RF, A5 synthesizer, and A6 receiver IF are verified.

External test setup 1 (shown in Figure 10-6) is used in this test. The test sets the RF OUT level to a low level and measures the levels of the S input residuals at the frequency points where the residuals are most likely to appear.

26: S INPUT NOISE LEVEL

Checks that the noise level at the S input is lower than the limit. As a result, the A4A2 receiver RF and A6 receiver IF are verified.

External test setup 1 (shown in Figure 10-6 is used in this test. The test sets the RF OUT level to a low level and measures the noise levels of the S input at the appropriate frequency range.

27: FRACTION SPURIOUS

The fraction spurious is caused by the fractional N oscillator in the A5 synthesizer. This test checks that the spurious level is lower than the limit. As a result, the A5 synthesizer is verified.

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External test setup 1 (shown in Figure 10-6) is used in this test. The test sets the RF OUT level to a constant level and measures the noise levels of the S input at the appropriate frequency range.

28: RF TO R LVL & FLTNESS

Checks that the level accuracy and flatness of the RF OUT signal are within limits. As a result, the A3A1 ALC, A3A2 2nd LO, A3A3 source, A4A2 receiver RF, A6 receiver IF, and A9 input multiplexer are verified.

External test setup 2 (shown in Figure 10-7) is used in this test. This sets the RF OUT level to a constant level and measures the RF OUT level using the R input over the appropriate frequency range.

29: NA CROSSTALK & NOISE

Checks that the input crosstalk from the R input to the A and B inputs, and the source crosstalk and noise level at the R, A and B inputs are within limits. As a result, the A4A2 receiver RF and A9 input multiplexer are verified.

External test setup 2 (shown in Figure 10-7) is used in this test. For the input crosstalk test, the test sets the RF OUT level to a constant level and measures the crosstalk levels at the A and B inputs over the appropriate frequency range. For the source crosstalk and noise level test, the test sets the RF OUT level to a low level and measures the crosstalk and noise levels at the R, A and B inputs over the appropriate frequency range.

30: R INPUT COMPRESSION

Checks that the input compression at the R input is within limits. As a result, the A4A2 receiver RF, A6 receiver IF, and A9 input multiplexer are verified.

External test setup 2 (shown in Figure 10-7) is used in this test. The test sets the RF OUT level to several levels and measures the levels using the R input over the appropriate frequency range.

31: RANGING

Checks operation of the RANGE R and F circuits in the A6 receiver IF.

External test setup 2 (shown in Figure 10-7) is used in this test. The test sets the RF OUT level to a constant level and varies the range F and R settings. For each setting, the RF OUT level is measured using the R input.

32: A/R RATIO ACCURACY

Checks that the A/R magnitude ratio/phase accuracy is within limits. As a result, the A9 input multiplexer is verified.

External test setup 3 (shown in Figure 10-8) is used in this test. The test measures the A/R magnitude ratio and phase at the test setup over the entire frequency range.

33: A INPUT COMPRESSION

Checks that the input compression at the A input is within limits. As a result, the A4A2 receiver RF, A6 receiver IF, and A9 input multiplexer are verified.

External test setup 3 (shown in Figure 10-8) is used in this test. The test sets the RF OUT level to several levels and measures the levels using the A input over the entire frequency range.

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34: B/R RATIO ACCURACY

Checks that the B/R magnitude ratio/phase accuracy is within limits. As a result, the A9 input multiplexer is verified.

External test setup 4 (shown in Figure 10-9) is used in this test. The test measures the B/R magnitude ratio and phase at the test setup over the entire frequency range.

35: B INPUT COMPRESSION

Checks that the input compression at B input is within limits. As a result, the A4A2 receiver RF, A6 receiver IF, and A9 input multiplexer are verified.

External test setup 4 (shown in Figure 10-9) is used in this test. The test sets the RF OUT level to several levels and measures the levels using the B input over the entire frequency range.

36: RESOLUTION BANDWIDTH

Checks that the following performance specifications for resolution bandwidth (RBW) settings $\leq$ 10 kHz are within limits:

- RBW Accuracy (3 dB bandwidth)/Selectivity (60 dB bandwidth/3 dB bandwidth).
- Trace Noise (Peak to Peak).
- RBW Switching Uncertainty.

As a result, the A6 receiver IF is verified.

External test setup 5 (shown in Figure 10-10) is used in this test. The test varies the RBW setting. For each setting, the CAL OUT signal (20 MHz) spectrum is measured using the S input. In the test, the frequency span is set appropriately for each measurement of the bandwidth, trace noise, and switching uncertainty.

37: IF GAIN

Checks operation of the IF GAIN W, X, Y, and Z circuits in the A6 receiver IF.

External test setup 5 (shown in Figure 10-10) is used in this test. The test varies the reference level setting to change the GAIN W, X, Y, and Z settings. For each setting, the CAL OUT level is measured using the S input.

38: PHASE NOISE

Checks that the phase noise of the CAL OUT signal (20 MHz) is lower than the limits. As a result, the A3A2 2nd LO, A4A1 1st LO, A5 synthesizer, and A6 receiver IF are verified.

External test setup 5 (shown in Figure 10-10) is used in this test. The test measures the phase noise of the CAL OUT signal at several offsets from the fundamental using the S input.

39: SPURIOUS

Checks that the spurious response of the receiver is lower than the limits. As a result, the A3A2 2nd LO, A4A1 1st LO, A5 synthesizer, and A6 receiver IF are verified.

External test setup 5 (shown in Figure 10-10) is used in this test. The test measures the CAL OUT signal using the S input and checks the spurious level at several frequency points where spurious signals are most likely to appear.

40: X'TAL FILTER RESPONSE

Checks 10 kHz crystal bandpass filter in the A6 receiver IF. As a result, the A3A2 2nd LO, A4A1 1st LO, A5 synthesizer, and A6 receiver IF are verified.

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External test setup 5 (shown in Figure 10-10) is used in this test. The test measures the CAL OUT signal using the S input to evaluate the frequency response over the 3 dB passband of the crystal bandpass filter.

`ADJUSTMENT TESTS`

This group of tests is used when adjusting the analyzer. These tests make the adjustment procedure easier. For more detailed operating information, see the *Adjustments and Correction Constants* chapter.

41: DC OFFST/HLD STEP ADJ

Used when the *DC Offset/Hold Step Adjustment* on the A6 receiver IF is performed.

42: 0/90 DEG TRACKING ADJ

Used when the *0°/90° Tracking Adjustment* on the A6 receiver IF is performed.

43: FINAL GAIN ADJ

Used when the *Final Gain Adjustment* on the A6 receiver IF is performed.

44: 2nd LO PLL LOCK ADJ

Used when the *Second Local PLL Lock Adjustment* on the A3A2 2nd LO is performed.

45: SOURCE MIXER LEAK ADJ

Used when the *Source Mixer Local Leakage Adjustment* on the A3A2 2nd LO is performed.

46: 3 MHZ BPF ADJ

Used when the *Band Pass Filters Adjustment* on the A6 receiver IF is performed.

47: 1 MHZ BPF ADJ

Used when the *Band Pass Filters Adjustment* on the A6 receiver IF is performed.

`DISPLAY TESTS`

These tests are test patterns that are used in the factory for display adjustments, diagnostics, and troubleshooting. They are not used for field service. Test patterns are executed by entering the test number (48 through 62), then pressing `EXECUTE TEST`, `CONTINUE`. The test pattern is displayed and the softkey labels are blanked. To exit the test pattern and return to the softkey labels, press softkey 8 (on the bottom). The following is a description of the test patterns.

Note Do NOT press any keys except softkey 8 (on the bottom) while the test pattern is being executed. If you do, you CANNOT quit the test pattern (that is, you can quit the test pattern only when the analyzer is turned OFF).

48: TEST PATTERN 1

All Black. This pattern is used to verify the color purity of the LCD Display.

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49: TEST PATTERN 2

All White. This pattern is used to verify the light output and to check the color purity of the LCD display.

50: TEST PATTERN 3

All Red. This pattern has the same use as TEST PATTERN 2.

51: TEST PATTERN 4

All Green. This pattern has the same use as TEST PATTERN 2.

52: TEST PATTERN 5

All Blue. This pattern has the same use as TEST PATTERN 2.

`ALL EXT TESTS`

The ALL EXT tests execute a group of external tests. External tests 19 through 40 are divided by the test setup into five groups. When an ALL EXT test is executed, external tests included in a group are sequentially executed. The ALL EXT tests are used in the *Operator's Check* in the *Troubleshooting* chapter.

53: ALL EXT 1

This test executes all external tests that require external test setup 1 (shown in Figure 10-6). This consists of external tests 21 through 27. If any of the tests fail, the test displays a "FAIL" status indication. Use the RPG knob to scroll through tests 21 to 27 to see what test failed. If all tests pass, the test displays a "PASS" status indication. Each test retains its own test status.

54: ALL EXT 2

This test executes all external tests that require external test setup 2 (shown in Figure 10-7). This test consists of external tests 19, 20, and 28 through 31. If any of the tests fail, this test displays a "FAIL" status indication. Use the RPG knob to scroll through tests 19, 20, and 28 to 31 to see what test failed. If all tests pass, the test displays a "PASS" status indication. Each test retains its own test status.

55: ALL EXT 3

This test executes all external tests that require external test setup 3 (shown in Figure 10-8). This test consists of external tests 32 and 33. If any of the tests fail, this test displays a "FAIL" status indication. Use the RPG knob to scroll through tests 32 to 33 to see what test failed. If all tests pass, the test displays a "PASS" status indication. Each test retains its own test status.

56: ALL EXT 4

This test executes all external tests that require external test setup 4 (shown in Figure 10-9). This test consists of external tests 34 and 35. If any of the tests fail, this test displays a "FAIL" status indication. Use the RPG knob to scroll through tests 34 to 35 to see what test failed. If all tests pass, the test displays a "PASS" status indication. Each test retains its own test status.

57: ALL EXT 5

This test executes all external tests that require external test setup 5 (shown in Figure 10-10). This test consists of external tests 36 through 40. If any of the tests fail, the test displays a "FAIL" status indication. Use the RPG knob to scroll through tests 35 to 40 to see what test failed. If all tests pass, the test displays a "PASS" status indication. Each test retains its own test status.

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MISC TESTS

58: IMPEDANCE TEST KIT

This test verify 43961A RF Impedance Test Kit, that require external test setup 6 (shown in Figure 10-11). Press EXECUTE TEST and follow the displyed instructions. If any of the tests fail, the test displays a “FAIL” status indication.

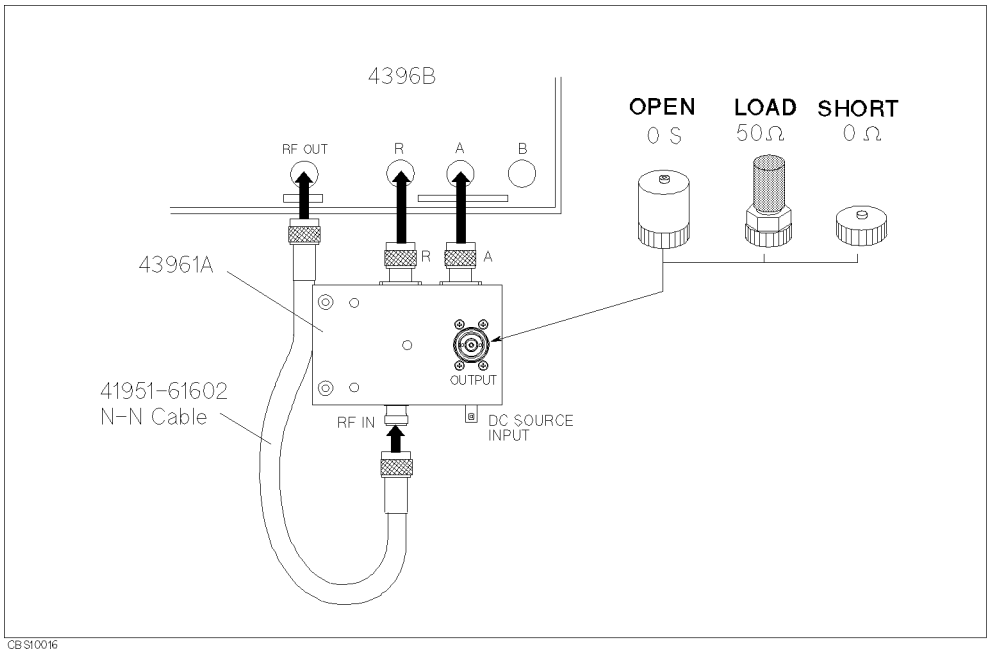


Figure 10-11. External Test Setup 6

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SERVICE MODES MENU

Figure 10-12 shows the service modes menu. The service modes menu leads to one of the menus used to control the analyzer service modes. For the analyzer's service modes, see the *Service Modes* . To display the service modes menu, press System, SERVICE MENU, and SERVICE MODES. Each softkey in the service modes menu is described below.

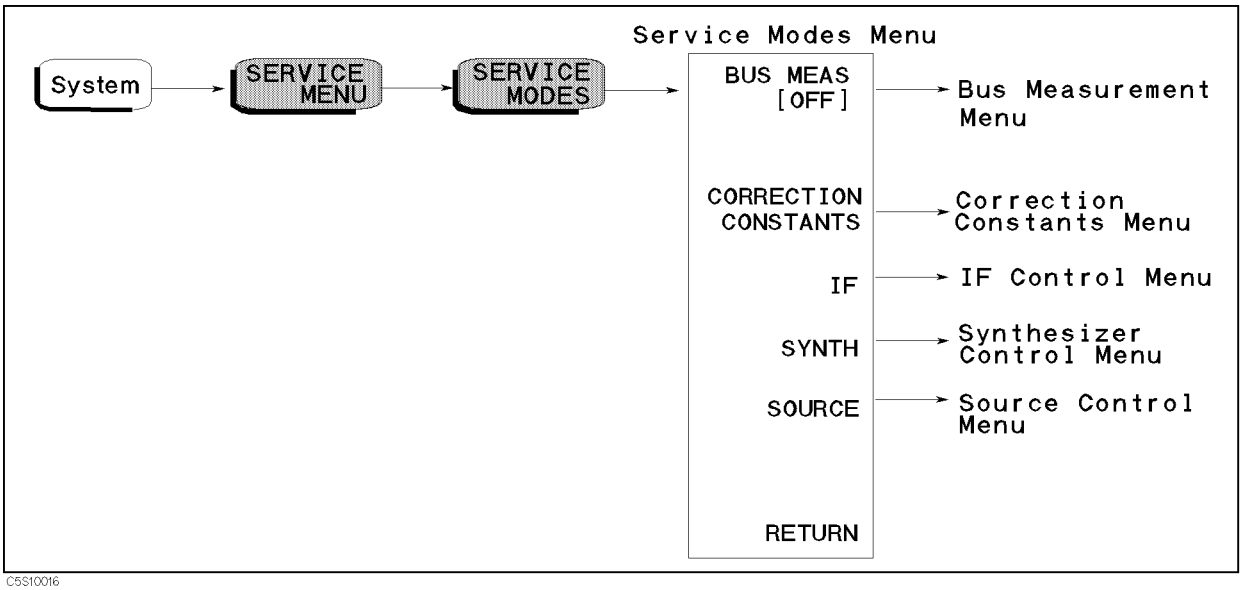


Figure 10-12. Service Modes Menu

BUS MEAS [OFF]

Displays the Bus Measurement Menu. See the *Bus Measurement Menu* in this chapter.

CORRECTION CONSTANTS

Displays the Correction Constant Menu. See the *Correction Constant Menu* in this chapter.

IF

Displays the IF Control Menu. See the *IF Control Menu* in this chapter.

SYNTH

Displays the Synthesizer Control Menu. See the *Synthesizer Control Menu* in this chapter.

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SOURCE

Displays the Source Control Menu. See the *Source Control Menu* in this chapter.

Service Modes

The analyzer has various service modes. These service modes are powerful tools to test, verify, adjust, and troubleshoot the analyzer. The service modes are divided by function into the five groups listed below:

Bus Measurement	measures and displays the signal voltage or frequency at the selected bus node of the analyzer. This service mode allows you to check the circuit operation by monitoring the circuit signal without accessing the inside of the analyzer.
Correction Constants On/Off	allows you to turn one (or more) of the corrections on/off.
IF Control	allows you to control the internal circuit settings in the A6 receiver IF.
Synthesizer Control	allows you to control the internal circuit settings in the A5 synthesizer.
Source Control	allows you to control the internal circuit settings in the A3A1 ALC.

Note



After pressing SERVICE MODES, an annotation (Svc) is displayed to indicate that the service modes are activated. The settings made in the service modes are kept until the analyzer is turned off or (PRESET) is pressed.

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BUS MEASUREMENT MENU

Figure 10-13 shows the bus measurement menu. This menu is used to control the bus measurements. For more information about the bus measurements, see the *Bus Measurement*. For the bus measurement procedure, see the *Bus Measurement Procedure* .

To display the bus measurement menu, press System, SERVICE MENU, SERVICE MODES, and BUS MEAS [ ]. Each softkey in the bus measurement menu is described below.

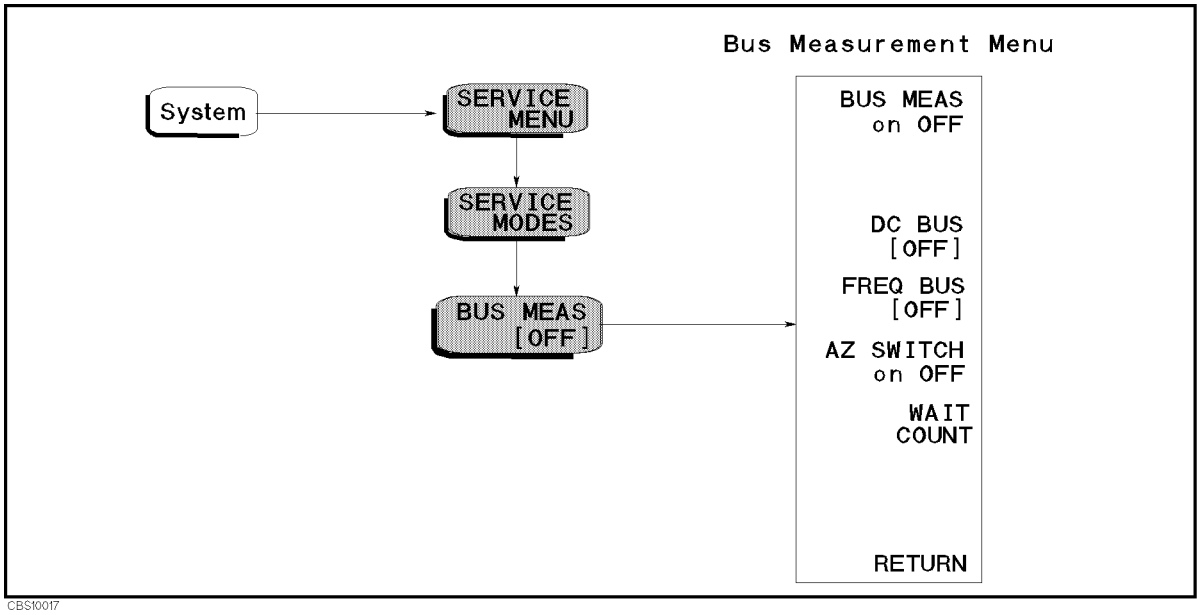


Figure 10-13. Bus Measurement Menu

BUS MEAS on OFF (:DIAG:SERV:BUS:STAT {ON|OFF})

Toggles the bus measurement on and off. After pressing this softkey, the menu changes to BUS MEAS ON off and the measured value of the bus measurement is displayed.

DC BUS [OFF] (:DIAG:SERV:BUS:DC <*numeric*>)

Allows you to select one of the DC bus nodes. The DC bus nodes are numbered from 0 to 26. To select the desired DC bus node, press this softkey and then enter the node number by using the numeric keypad, ↑, ↓, or RPG knob. The node number and name are displayed in the active entry area of the display and the node abbreviation is displayed in the brackets of the menu.

FREQ BUS [OFF] (:DIAG:SERV:BUS:FREQ <*numeric*>)

Allows you to select one of the frequency bus nodes. The frequency bus nodes are numbered from 0 to 7. To select the desired frequency bus node, press this softkey and then enter the frequency node number by using the numeric keypad, ↑, ↓, or RPG knob The node number and name are displayed in the active entry area of the display and the node abbreviation is displayed in the brackets of the menu.

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`AZ SWITCH on OFF` (:DIAG:SERV:BUS:AZER {OFF|ON|0|1})

Toggles the auto zero switch on and off.

`WAIT COUNT` (:DIAG:SERV:BUS:WAIT

<*numeric*>)

Sets the wait count to specify the wait time in the DC bus measurement. The wait count is an integer from 2 to 32767. When the wait count is N, the analyzer waits N * 12.5 μsec before each DC bus measurement.

Bus Measurement

In this service mode, the analyzer measures and displays the signal voltage or frequency at the selected bus node. This service mode allows you to check the circuit operation by monitoring the circuit signal without accessing the inside of the analyzer.

The analyzer has 33 bus nodes for this service mode. Of these, 26 bus nodes are for DC voltage measurement. These nodes are connected to the A/D converter in the A6 receiver IF through the DC Bus, a single multiplexer line with twenty-six channels. The other 7 bus nodes are for frequency measurement. These nodes are connected to the frequency bus timer in the A1 CPU through the frequency bus, a single multiplexer line with 7 channel.

Each of the DC bus nodes and the frequency bus nodes is described in the *DC Bus Nodes* and *Frequency Bus Nodes* in this section.

Bus Measurement Procedure

Use this procedure to perform the bus measurement.

1. Press (Preset) to initialize the analyzer.
2. Set the analyzer controls to the settings that you desire to observe in the bus measurement.
3. Press (System), `SERVICE MENU`, `SERVICE MODES`, `BUS MEAS` to display the bus measurement menu.
4. Select the desired bus node as follows:
   - If a DC bus measurement is desired, press `DC BUS [OFF]`. Then enter a node number between 1 and 26.
   - If a frequency bus measurement is desired, press `FREQ BUS`. Then enter a node number between 1 and 7.
5. Press `BUS MEAS on OFF` to activate the bus measurement. The menu changes to `BUS MEAS ON off`. The DC or frequency bus measurement value is displayed in the marker value. See the *Bus Measurement Values* section.
6. Observe the bus measurement trace and marker value.
7. Press (Preset) to exit the bus measurement.

To change the bus node to another node, repeat the steps above.

Both the DC bus and the frequency bus can be monitored simultaneously. This helps when observing the relationship between the VCO tuning voltage and the VCO output frequency of the fractional N oscillator. See the *Bus Measurement Values* section.

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Bus Measurement Values

The bus measurement value is displayed with a unit "U."

- The DC bus measurement's "1 U" is equivalent to "1 V." The displayed value in the DC bus measurement does not corresponding to the measured voltage because the voltage detected at the DC bus node is scaled appropriately and measured. The scaling factor depends on each DC node. For example, the scaling factor at the DC bus node 1 of +5 V (AUX) is approximately 0.405. Therefore the displayed value is nominally 2.025 U (5 U x 0.405). A typical value for each DC bus node measurement is provided in the *DC Bus Node Descriptions*.
- The frequency bus measurement's "1 U" is equivalent to "1 MHz." For example, a measured value of 1 kHz is displayed as 1 mU. A typical value for each frequency bus measurement is provided in the *Frequency Bus Node Descriptions*.

The DC bus measurement values are displayed using real format. The frequency bus measurement values are displayed using imaginary format. When a DC or Frequency bus node is measured, the **Re** or **Im** notation appears on the display and indicates the used format. When both a DC bus node and a frequency bus node are measured simultaneously, the DC bus versus frequency bus measurement values are displayed using a polar chart format. This is helpful to observe the relationship between the VCO tuning voltage and the VCO output frequency of the fractional N oscillator.

DC Bus Node Descriptions

The following paragraphs describe the 26 DC bus nodes. They are listed in numerical order.

0: NONE

The DC bus is off. This is the default setting.

1: +5 V (AUX) (2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V (AUX) power supplied to the A2 post- regulator. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.025 U (±10%).

2: −15 V (−1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V (AUX) power supplied to the analog boards. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately −1.92 U (±10%).

3: −12.6 V (−2.124 U)

This node is located on the A2 post-regulator and detects the voltage of the −12.6 V power supplied to the probe power connectors on the front panel. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately −2.124 U (±10%).

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4: −5 V (−2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the −5 V power supplied to the analog boards. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately −2.025 U (±10%).

5: + 5 V (2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V power supplied to the analog boards. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.025 U (±10%).

6: + 5.3 V (2.1465 U)

This node is located on the A2 post-regulator and detects the voltage of the +5.3 V power supplied to the A3A3 source. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.1465 U (±10%).

7: + 8.5 V (1.8955 U)

This node is located on the A2 post-regulator and detects the voltage of the +8.5 V power supplied to the A3A3 source. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +1.8955 U (±10%).

8: + 15 V (AUX) (1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +15 V (AUX) power supplied to the probe power connectors on the front panel. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +1.8955 U (±5%).

9: + 15 V (1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +15 V power supplied to the analog boards. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +1.92 U (±10%).

10: + 22 V (2.002 U)

This node is located on the A2 post-regulator and detects the voltage of the +22 V power supplied to the S-parameter test set through the TEST SET-I/O INTERCONNECT connector on the rear panel. See Figure 5-1.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat at approximately +2.002 U (±10%).

11: FAN POWER

This node is located on the A2 post-regulator and detects the voltage of the FAN POWER (nominal 24 V) supplied to the fan on the rear panel. See Figure 5-1.

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To observe this node, perform the steps in the *Bus Measurement Procedure* . The typical trace is shown in Figure 10-14.

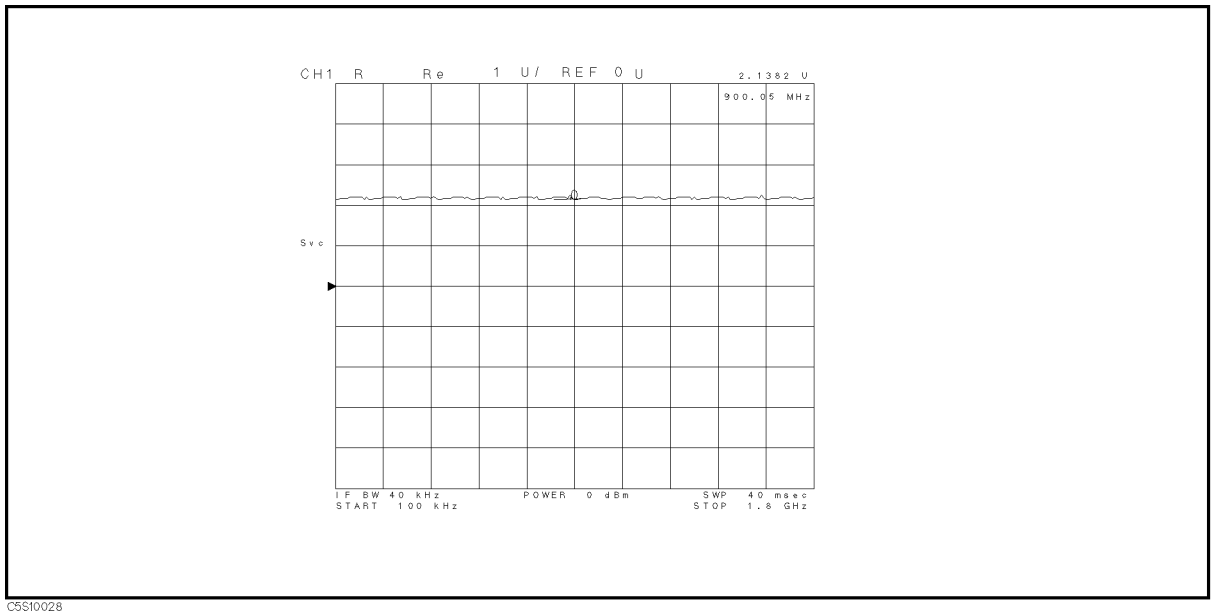


Figure 10-14. Fan Power Typical Trace

12: +65 V (2.0605 U)

(This node is not connected to the DC Bus.)

13: SRC VTUNE (Source Oscillator VCO Tuning Voltage)

This node is located in the source oscillator on the A3A1 ALC and detects the 85.68 MHz VCO tuning voltage. See Figure 11-6.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within +0.1 U to +3.0 U.

14: 2ND LO VTUNE (Second Local Oscillator VCO Tuning Voltage)

This node is located in the second local oscillator on the A3A2 2nd LO and detects the 1.04 GHz VCO tuning voltage. See Figure 11-6.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within −130 mU to +130 mU.

15: DET OUT (Detector Output)

This node is located in the ALC circuit on the A3A1 ALC and detects the level detector voltage that loops back from A3A3 source. See Figure 11-6.

The typical trace for the following keystrokes' setting is displayed as the DET OUT trace in Figure 10-15. The absolute value of the typical marker reading is within +1 mU to +70 mU at a power of −20 dBm and within −1.5 U to −3.8 U at a power of +10 dBm.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER of POINTS, (7), (x1), (Sweep), SWEEP TYPE MENU, POWER SWEEP, (Start), (-), (2), (0), (x1), (Stop), (1), (0), (x1)

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

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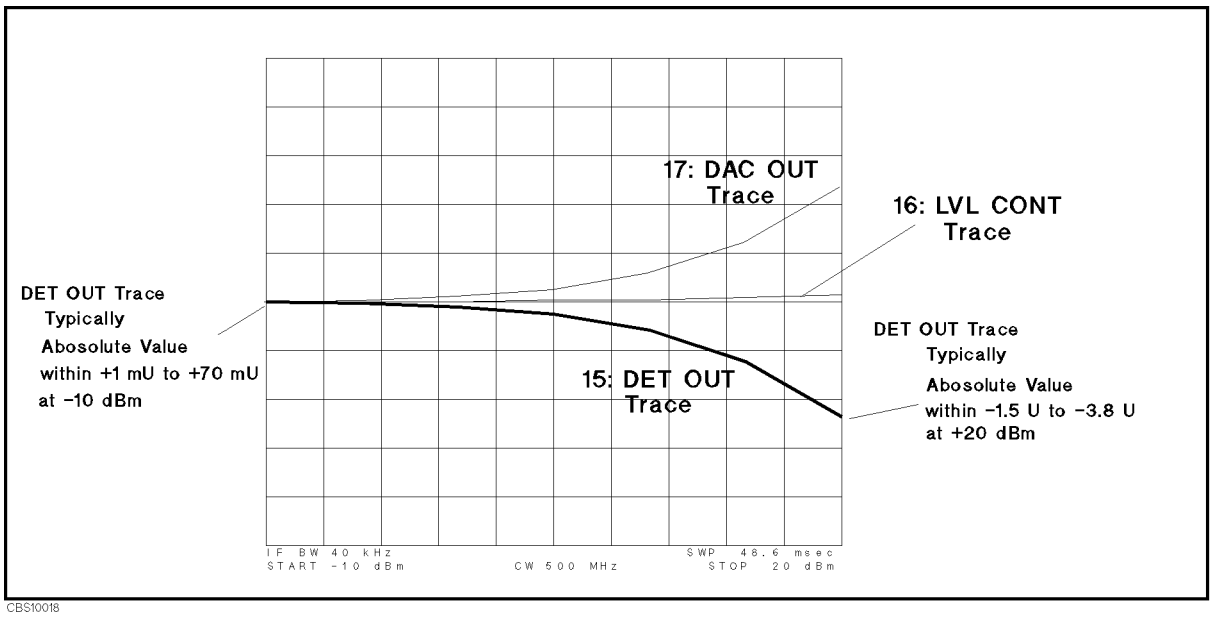


Figure 10-15. DET OUT, LVL CONT, and DAC OUT Typical Traces

16: LVL CONT (Level Vernier Control Voltage)

This node is located in the ALC circuit on the A3A1 ALC and detects the level vernier control voltage. See Figure 11-6.

The typical trace for the following keystrokes' setting is displayed as the LVL CONT trace in Figure 10-15.

Meas, ANALYZER TYPE, NETWORK ANALYZER, Preset, Sweep, NUMBER of POINTS, 7, x1, Sweep, SWEEP TYPE MENU, POWER SWEEP, Start, -, 2, 0, x1, Stop, 1, 0, x1

To observe the trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

17: DAC OUT (Level DAC Output Voltage)

This node is located in the ALC circuit on the A3A1 ALC and detects the level DAC output voltage. See Figure 10-15.

The typical trace for the following keystrokes' setting is displayed as the DAC OUT trace in Figure 10-15.

Meas, ANALYZER TYPE, NETWORK ANALYZER, Preset, Sweep, NUMBER of POINTS, 7, x1, Sweep, SWEEP TYPE MENU, POWER SWEEP, Start, -, 2, 0, x1, Stop, 1, 0, x1

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

18: 1ST LO VTUNE (First Local Oscillator VCO Turning Voltage)

This node is located in the 1st local oscillator on the A4A1 1st LO and detects the 2.05858 GHz to 3.85858 GHz VCO tuning voltage. See Figure 11-6.

The typical trace for the following keystrokes' setting is displayed in Figure 10-16. The displayed trace is typically straight. The typical marker value is within −2.3 U to −1.2 U at a frequency of 100 kHz and within +0.1 U to +1.9 U at a frequency 1.8 GHz.

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(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER of POINTS, (5), (x1), (Bw/Avg), IF BW, (1), (0), (k/m)

To observe this trace, perform the steps in the *Bus Measurement Procedure*. At step 2 in the procedure, press the keys listed above.

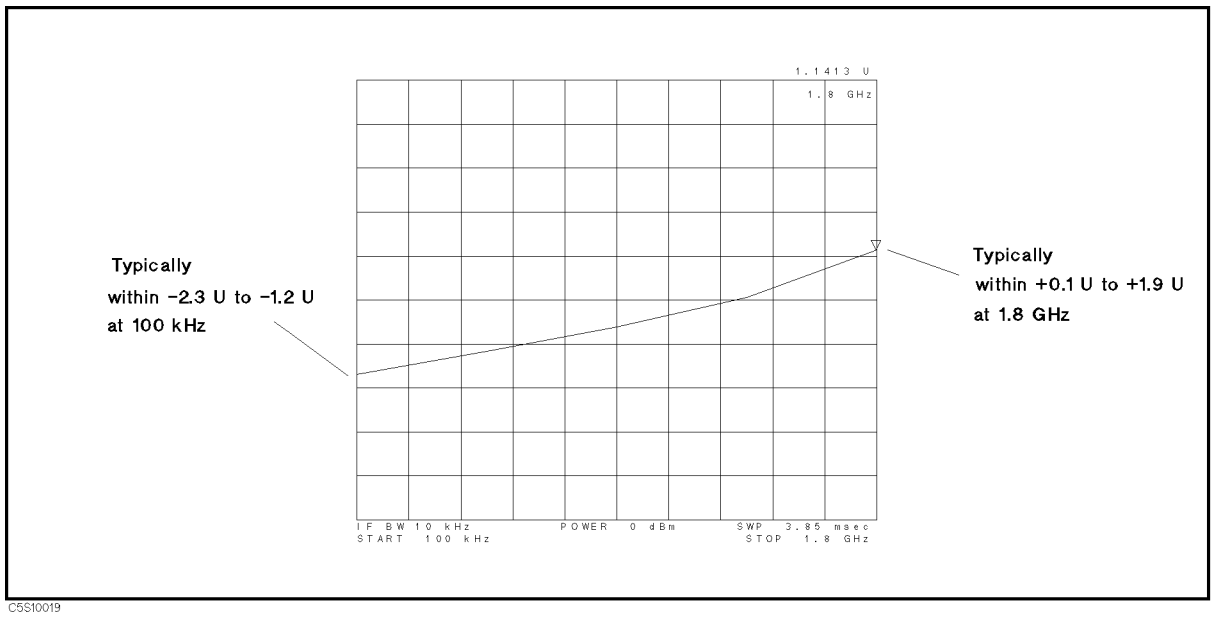


Figure 10-16. 1st LO VTUNE Typical Trace

19: STEP VTUNE (Step Oscillator VCO Turning Voltage)

This node is located in the step oscillator on the A5 synthesizer and detects the 470 MHz to 930 MHz VCO tuning voltage. See Figure 11-6.

The typical trace for the following keystrokes' setting is flat and within 0 U to +2 U. The typical values for the three center frequency ranges are provided in Table 10-2.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Span), ZERO SPAN, (Center), (1) (M/μ)

To observe this trace, perform the steps in the *Bus Measurement Procedure*. At step 2 in the procedure, press the keys listed above.

Table 10-2. Typical STEP VTUNE Values

Center Frequency	Typical STEP VTUNE Value
1 MHz Hz to 400 MHz	0 U to +2 U
400 Hz to 1 GHz	0 U to +3 U
1 GHz Hz to 1.8 GHz	+0.5 U to +4 U

20: FN VTUNE (Fractional N Oscillator VCO Turning Voltage)

This node is located in the fractional N oscillator on the A5 synthesizer and detects the 31.25 MHz to 62.5 MHz VCO tuning voltage. See Figure 11-6.

The typical trace for the following keystrokes' setting is displayed in Figure 10-17. The displayed trace is typically straight and higher than −2 U.

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Meas, ANALYZER TYPE, NETWORK ANALYZER, Preset, Sweep, NUMBER of POINTS, 5, x1, Bw/Avg, IF BW, 1, 0, k/m

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

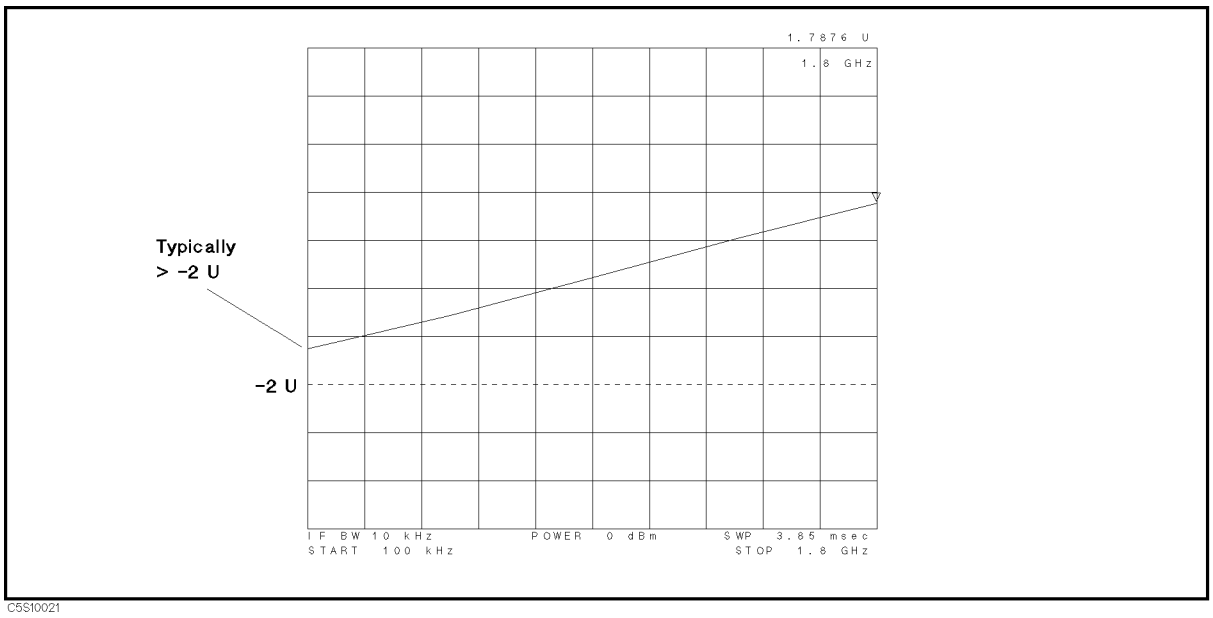


Figure 10-17. FN VTUNE Typical Trace

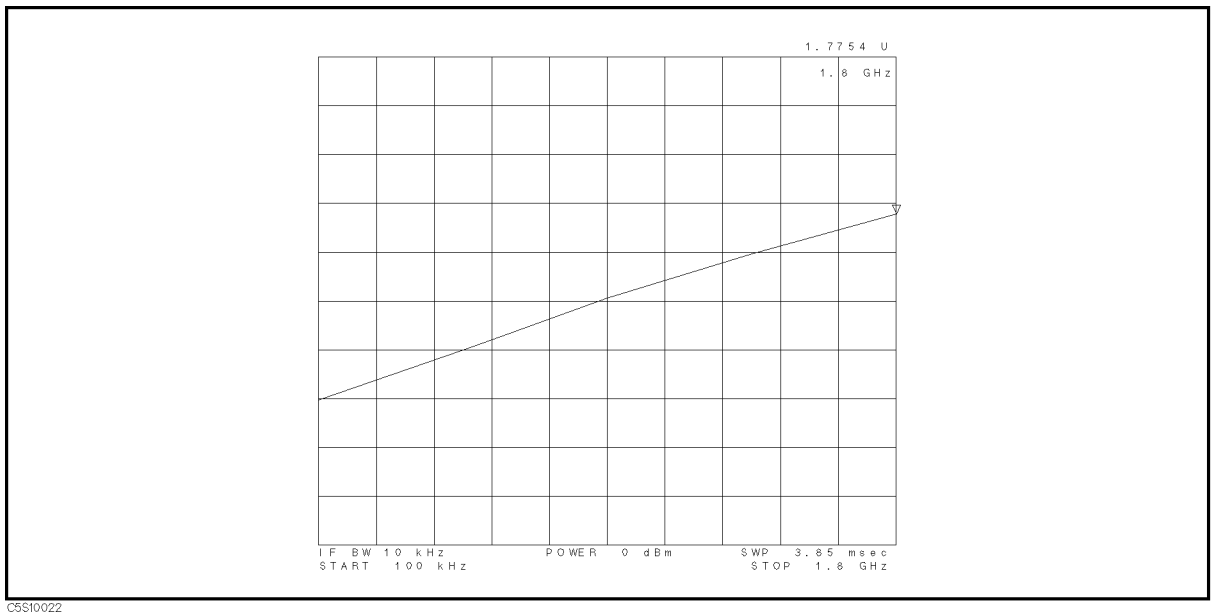
21: FN INTEG OUT (Fractional N Oscillator Integrator Output Voltage)

This node is located in the fractional N oscillator on the A5 synthesizer and detects the integrator output voltage. See Figure 11-6.

The typical trace for the following keystrokes' setting is displayed in Figure 10-18. The displayed trace is typically straight.

Meas, ANALYZER TYPE, NETWORK ANALYZER, Preset, Sweep, NUMBER of POINTS, 5, x1, Bw/Avg, IF BW, 1, 0, k/m

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C5S10022

Figure 10-18. FN INTEG OUT Typical Trace

To observe this trace, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

22: REF VTUNE (Reference Oscillator VCO Tuning Voltage)

This node is located in the reference oscillator on the A5 synthesizer and detects the 40 MHz VCXO tuning voltage. See Figure 11-6.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within 0 U to +3.0 U.

23: 3RD LO VTUNE (Third Local Oscillator VCO Tuning Voltage)

This node is located in the third local oscillator on the A6 receiver IF and detects the 85.6 MHz/85.68 MHz VCXO tuning voltage. See Figure 11-7.

To observe this node, perform the steps in the *Bus Measurement Procedure* . When this node is selected, the trace is typically flat and within +0.1 U to +3.0 U.

24: 2ND IF LVL (Second IF Signal Level)

This node is located in the A6 receiver IF and detects the second local oscillator signal level. See Figure 11-7. To observe this node, perform the steps in the *Bus Measurement Procedure* .

25: AD VREF (A/D Converter Voltage Reference)

This node is located in the A6 receiver IF and detects the reference voltage of the A/D converter. See Figure 11-7.

The typical trace for the following keystrokes' setting is flat and within +0.16 U to +0.24.

(Meas), ANALYZER TYPE, SPECTRUM ANALYZER, (Preset)

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

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26: GND (Ground)

This node is located on the A2 post-regulator and detects the ground voltage. See Figure 5-1. To observe this node, perform the steps in the *Bus Measurement Procedure*. When this node is selected, the trace is typically flat and within −0.1 to +0.1.

Frequency Bus Node Descriptions

The following paragraphs describe the 6 frequency bus nodes. They are listed in numerical order.

0: OFF

The frequency bus is off. This is the default setting.

1: SOURCE OSC (Source Oscillator)

This node is located in the source oscillator on the A3A1 ALC and measures the loop back frequency of 40 kHz from the 85.68 MHz VCO. See Figure 11-6.

The typical trace for the following keystrokes' setting is flat and within +39.992 mU to +40.008 mU.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER OF POINTS, (2), (x1)

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed above.

2: DIVIDER OUT (Divider Output)

This node is located in the divider on the A3A1 ALC and measures the 1/200 divider output frequency 40 kHz. See Figure 11-6.

The typical trace is flat and within +39.992 mU to +40.008 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed below to make a fast sweep.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

3: STEP OSC (Step Oscillator)

This node is located in the step oscillator on the A5 synthesizer and measures the step oscillator frequency through the 1/256 divider. See Figure 11-6.

The typical trace is flat and the trace value depends on the measurement settings (center and span settings). The typical values for several settings are provided in Table 7-1 STEP OSC Frequency in chapter 7.

4: FN OSC (Fractional N Oscillator)

This node is located in the fractional N oscillator on the A5 synthesizer and measures the fractional N oscillator frequency through the 1/16 divider. See Figure 11-6.

The typical trace is flat and the trace value depends on the measurement settings (center and span settings). The typical values for several settings are provided in the *Check the FRAC N OSC Signal* in chapter 7.

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5: REF OSC (Reference Oscillator)

This node is located in the INT REF output circuit on the A5 synthesizer and measures the INT REF output frequency 10 MHz through the 1/4 divider. See Figure 11-6.

The typical trace is flat and within +2.4996 U to +2.5004 U.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed below to make a fast sweep.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

6: 3RD LO OSC (Third Local Oscillator)

This node is located in the third local oscillator on the A6 receiver IF and measures the loop back frequency of 40 kHz from the 85.6 MHz/85.68 MHz VCO. See Figure 11-7.

The typical trace is flat and within +39.992 mU to +40.008 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed below to make a fast sweep.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

7: SAMPLE HOLD

This node is located in the sequencer on the A6 receiver IF and measures the 80 kHz sampling signal in the sequencer. See Figure 11-7.

The typical trace is flat and within +79.984 mU to +80.016 mU.

To observe this node, perform the steps in the *Bus Measurement Procedure* . At step 2 in the procedure, press the keys listed below to make a fast sweep.

(Meas), ANALYZER TYPE, NETWORK ANALYZER, (Preset), (Sweep), NUMBER OF POINTS, (1), (0), (x1)

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CORRECTION CONSTANTS MENU

Figure 10-19 shows the correction constants menu. This menu allows you to turn off one (or more) of the corrections. When one (or more) corrections are turned off, the analyzer displays the raw measured data. You can check the raw characteristics of the source and receiver circuit. For the corrections, see the *Correction Constants*.

To display the menu, press System, SERVICE MENU, SERVICE MODES, and CORRECTION CONSTANTS. Each softkey in the correction constants menu is described below.

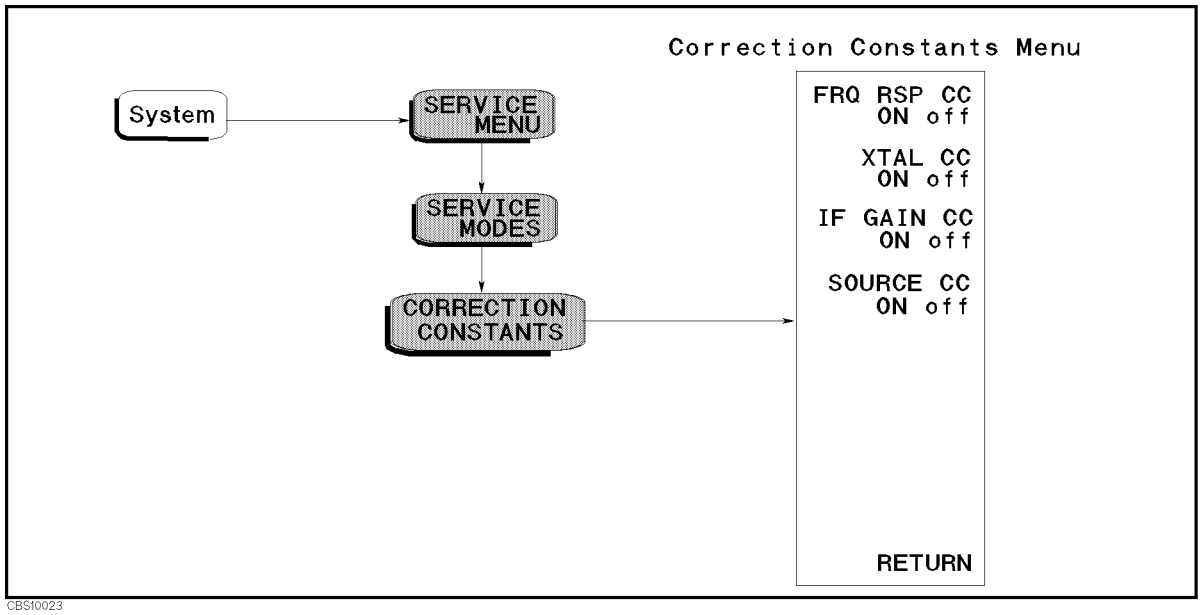


Figure 10-19. Correction Constants Menu

FRQ RSP CC ON/off (:DIAG:SERV:CCON:FRES {OFF|ON|0|1})

Toggles the receiver frequency response correction on and off. When the correction is turned off, the corrections using the following constants are turned off.

Spectrum analyzer absolute magnitude correction constants.
Network analyzer absolute magnitude correction constants.
Network analyzer magnitude ratio/phase correction constants.

XTAL CC ON/off (:DIAG:SERV:CCON:XTAL {OFF|ON|0|1})

Toggles the crystal filter frequency response correction on and off. When this correction is turned off, the analyzer does not perform the compensation using the crystal filter correction constants.

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`IF GAIN CC ON/off` (:DIAG:SERV:CCON:IFG {OFF|ON|0|1})

Toggles the IF gain error correction on and off.

`SOURCE CC ON/off` (:DIAG:SERV:CCON:SOUR {OFF|ON|0|1})

Toggles the RF OUT level correction on and off.

Note All corrections must be turned to on except when checking the analog circuits.



Correction Constants

The analyzer has the following seven correction constants in the EEPROM on the A1 CPU. It uses them to control the internal circuits and to achieve optimum performance by compensating for errors due to circuit characteristics. Each of the correction constants is described below. For the circuits that appear in the following description, see the *Theory of Operation* chapter.

- **Step Pretune Correction Constants** are control values for the pretune DAC in the STEP oscillator on the A5 synthesizer. They are used to control the STEP oscillator frequency. If these values are not correct, the following performance specification is severely degraded:

  Frequency accuracy at span frequency $\leq$ 45 MHz in the network and the spectrum analyzer modes.

- **RF OUT Level Correction Constants** are control values for the level DAC and the Gain ALC in the ALC on the A3A1 ALC. These affect the following performance specifications:

  Source Level Accuracy/Flatness in the network analyzer mode.
  Non-Sweep Power Linearity in the network analyzer mode.
  Power Sweep Linearity in the network analyzer mode.

- **Spectrum Analyzer Absolute Magnitude Correction Constants** are equivalent to the frequency response of the signal path used in the spectrum analyzer mode. These corrections are used to compensate for errors due to the frequency response in the spectrum analyzer mode. These are used for the following performance specification:

  Frequency response in the spectrum analyzer mode.

  If these are not correct, the following performance specifications in the spectrum analyzer mode are severely degraded:

  Displayed average noise level in the spectrum analyzer mode.
  Amplitude fidelity in the spectrum analyzer mode.

- **Network Analyzer Absolute Magnitude Correction Constants** are equivalent to the amplitude frequency response of the signal path used in the network analyzer mode. These corrections are used to compensate errors due to the receiver frequency response in the network analyzer mode. They are also used in the spectrum analyzer mode using one of inputs R, A, and B. They are for the following performance specification:

  Absolute amplitude accuracy in the network analyzer mode.

  If these correction constants are not correct, the performance specification listed below is severely degraded:

  Receiver noise level in the network analyzer mode.

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- **Crystal Filter Correction Constants** are equivalent to the frequency response of the 10 kHz passband of the crystal BPF. These corrections are used in the spectrum measurement using RBW $\leq$ 3 kHz. In this measurement, the IF signal through the crystal filter (10 kHz passband) is digitized in the time domain. The analyzer performs the FFT (fast fourier transform) for the digitized signal and calculates the required spectrum amplitudes over 10 kHz bandwidth. The calculated data contains errors due to the frequency response of the crystal filter (10 kHz passband). The analyzer compensates the errors using the crystal filter correction constants. These corrections are for the following performance specification:

  Frequency response at RBW $\leq$ 3 kHz in the spectrum. analyzer mode

  If these are not correct, the following performance specifications are severely degraded:

  Receiver noise level in the network analyzer mode.
  RBW accuracy/selectivity in the spectrum analyzer mode.
  RBW switching uncertainty in the spectrum analyzer mode.

- **IF Gain Errors Correction Constants** are equivalent to the actual IF gains for every used settings of the IF BPFs, the gains (W, X, Y and Z), and the ranges (F and R) on the A6 receiver IF. These corrections are for the following performance specifications:

  Absolute amplitude accuracy in the network analyzer mode.
  IF gain switching uncertainty in the spectrum analyzer mode.

  If these correction constants are not correct, the following performance specifications are severely degraded:

  Receiver noise level in the network analyzer mode.
  Displayed average noise level in the spectrum analyzer mode.

- **Network Analyzer Magnitude Ratio/Phase Correction Constants** are equivalent to the receiver's magnitude ration/phase frequency response in the network analyzer mode. These corrections are for the following performance specifications:

  Absolute amplitude accuracy in the network analyzer mode.
  Magnitude ratio/phase frequency response in the network analyzer mode.

  If these correction constants are not correct, the performance specification listed below is severely degraded:

  Receiver noise level in the network analyzer mode.

Each of the correction constants is predefined and stored in the EEPROM on the A1 CPU. Each procedure for predefining the constants is provided under the heading corresponding to the constant's name in the *Adjustment and Correction Constants* chapter.

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IF CONTROL MENU

Figure 10-20 shows the IF control menu hierarchy. To display the IF control menu, press System, SERVICE MENU, SERVICE MODES, and IF. A softkey in the IF control menu displays one of menus used to control one of the A6 receiver IF circuits. Each softkey in the IF control menu is described below.

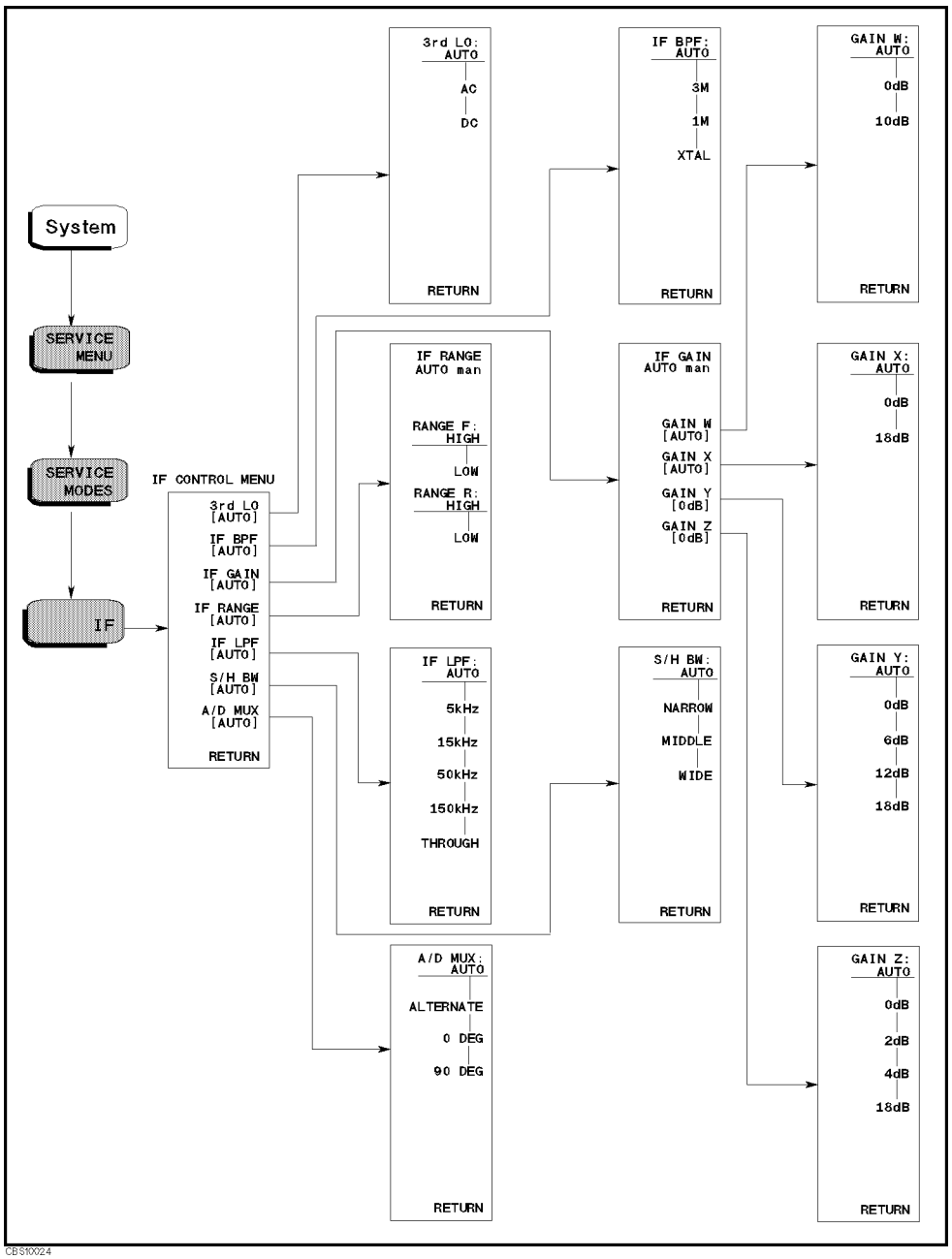


Figure 10-20. IF Control Menu

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3rd LO [ ] (:DIAG:SERV:IF:TLOC:MODE {AUTO|AC|DC})

Displays the control menu that allows you to control the 3rd LO (third local oscillator) in the A6 receiver IF. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

3rd LO: AUTO sets the 3rd LO control to the automatic mode (normal operation). In this mode, the analyzer controls the 3rd LO automatically according to the measurement settings.

AC sets the 3rd LO to the AC sampling mode. In this mode, the 3rd LO generates 85.6 MHz.

DC sets the 3rd LO to the DC sampling mode. In this mode, the 3rd LO generates 85.68 MHz.

IF BPF [ ] (:DIAG:SERV:IF:BPF:MODE {AUTO|BW3M|BW1M|XTAL})

Displays the control menu that allows you to select one of the IF BPFs (IF band pass filters) in the A6 receiver IF. The 2nd IF goes through the selected BPF to the 3rd IF converter. The softkeys in this control menu are described below. The abbreviation of the selected BPF is displayed in the brackets of the menu.

IF BPF: AUTO sets the IF BPF control to automatic mode (normal operation). In this mode, the analyzer sets the IF BPF setting to the 3 MHz, 1 MHz, or crystal IF BPFs automatically according to the measurement setting.

3M selects the 3 MHz BPF in the IF BPFs.

1M selects the 1 MHz BPF in the IF BPFs.

XTAL selects the 10 kHz crystal BPF in the IF BPFs.

IF GAIN [ ]

Displays the control menus that allow you to control the IF gains W, X, Y and Z in the A6 receiver IF. The softkeys in these control menus are described below. The abbreviation of the current setting (AUTO or MANUAL) is displayed in the brackets of the menu.

IF GAIN AUTO man (:DIAG:SERV:IF:GAIN:MODE {AUTO|MAN})

Toggles the IF gain control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the analyzer controls the IF gain W, X, Y, and Z settings automatically according to the measurement setting. In the manual mode, the IF gains are controlled by the following softkeys.

GAIN W [ ] (:DIAG:SERV:IF:GAIN:W {AUTO|DB0|DB10})

Displays the control menu for the IF GAIN W. The softkeys in this control menu are described below. The abbreviation of the current setting (AUTO, 0 dB, or 10 dB) is displayed in the brackets of the menu.

GAIN W: AUTO sets the IF GAIN W setting to automatic mode.

0 dB sets the IF GAIN W to 0 dB.

10 dB sets the IF GAIN W to 10 dB.

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`GAIN X [ ]` (:DIAG:SERV:IF:GAIN:X {AUTO|DB0|DB18})

Displays the control menu for the IF GAIN X. The softkeys in this control menu are described below. The abbreviation of the current setting (AUTO, 0 dB, or 18 dB) is displayed in the brackets of the menu.

`GAIN X: AUTO` sets the IF GAIN X to automatic mode.

`0 dB` sets the IF GAIN X to 0 dB.

`18 dB` sets the IF GAIN X to 18 dB.

`GAIN Y [ ]` (:DIAG:SERV:IF:GAIN:Y {AUTO|DB0|DB6|DB12|DB18})

Displays the control menu for the IF gain Y. The softkeys in this control menu are described below. The abbreviation of the current setting (AUTO, 0 dB, 6 dB, 12 dB, or 18 dB) is displayed in the brackets of the menu.

`GAIN Y: AUTO` sets the IF gain Y setting to automatic mode.

`0 dB` sets the IF gain Y to 0 dB.

`6 dB` sets the IF gain Y to 6 dB.

`12 dB` sets the IF gain Y to 12 dB.

`18 dB` sets the IF gain Y to 18 dB.

`GAIN Z [ ]` (:DIAG:SERV:IF:GAIN:Z {AUTO|DB0|DB2|DB4|DB18})

Displays the control menu for the IF gain Z. The softkeys in this control menu are described below. The abbreviation of the current setting (AUTO, 0 dB, 2 dB, 4 dB, or 18 dB) is displayed in the brackets of the menu.

`GAIN Z: AUTO` sets the IF GAIN Z setting to automatic mode.

`0 dB` sets the IF GAIN Z to 0 dB.

`2 dB` sets the IF GAIN Z to 2 dB.

`4 dB` sets the IF GAIN Z to 4 dB.

`18 dB` sets the IF GAIN Z to 18 dB.

IF RANGE [ ]

Displays the control menus that allow you to control the IF ranges F and R in the A6 receiver IF. The softkeys in these control menus are described below. The abbreviation of the current setting (AUTO or MANUAL) is displayed in the brackets of the menu.

`IF RANGE AUTO man` (:DIAG:SERV:IF:RANG:MODE {AUTO|MAN})

Toggles the IF range control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the analyzer controls the IF range F and R settings automatically according to the measurement setting. In the manual mode, the IF ranges are controlled by the following softkeys.

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`RANGE F: HIGH` (:DIAG:SERV:IF:RANG:F HIGH)

Sets the IF range F to high (1/1).

`LOW` (:DIAG:SERV:IF:RANG:F LOW)

Sets the IF range F to low (1/8).

`RANGE R: HIGH` (:DIAG:SERV:IF:RANG:R HIGH)

Sets the IF range R to high (1/1).

`LOW` (:DIAG:SERV:IF:RANG:R LOW)

Sets the IF range R to low (1/8).

`IF LPF [ ]` (:DIAG:SERV:IF:LPF:MODE {AUTO|BW5K|BW15K|BW50K|BW150K|THR})

Displays the control menu that allows you to select one of the IF LPFs (IF low pass filters) in the A6 receiver IF. The 3rd IF goes through the selected LPF to the A/D converter. The softkeys in the control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

`IF LPF: AUTO` sets the IF LPF control to automatic mode (normal operation). In this mode, the analyzer controls the IF BPF setting automatically according to the measurement setting.

`5kHz` selects the 5 kHz LPF in the IF LPFs.

`15kHz` selects the 15 kHz LPF in the IF LPFs.

`50kHz` selects the 50 kHz LPF in the IF LPFs.

`150Hz` selects the 150 kHz LPF to the IF LPFs.

`THROUGH` selects the through in the IF LPFs.

`S/H BW [ ]` (:DIAG:SERV:IF:SHBW:MODE {AUTO|NARR|MIDD|WIDE})

Displays the control menu that allows you to control the S/H's BW (sample and hold circuit's bandwidth) in the A6 receiver IF. The softkeys in this control menu are described below. The abbreviation of the current setting (narrow, middle, or wide) is displayed in the brackets of the menu.

`S/H BW: AUTO` sets the S/H BW control to automatic mode (normal operation). In this mode, the analyzer controls the S/H BW setting automatically according to the measurement setting.

`NARROW` sets the S/H BW setting to narrow (bandwidth 1 MHz).

`MIDDLE` sets the IF BPF setting to middle (bandwidth 2 MHz).

`WIDE` sets the IF BPF setting to wide (bandwidth 6 MHz).

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A/D MUX [ ] (:DIAG:SERV:IF:ADMX:MODE {AUTO|ALT|DEG0|DEG90})

Displays the control menu that allows you to control the A/D MUX (A/D converter multiplexer) in the A6 receiver IF. The A/D MUX connects one of the 0° and 90° paths to the A/D converter. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

A/D MUX: AUTO	sets the A/D MUX control to automatic mode (normal operation). In this mode, the analyzer controls the A/D MUX setting automatically according to the measurement setting.
ALTERNATE	connects the 0° and 90° paths to the A/D converter alternatively.
0 DEG	connects the 0° path to the A/D converter.
90 DEG	connects the 90° path to the A/D converter.

Note All settings must be turned to auto except when checking the analog circuits.



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SYNTHESIZER CONTROL MENU

Figure 10-21 shows the synthesizer control menus. To display the synthesizer control menu, press System, SERVICE MENU, SERVICE MODES, and SYNTH. Each softkey in the synthesizer control menu is described below.

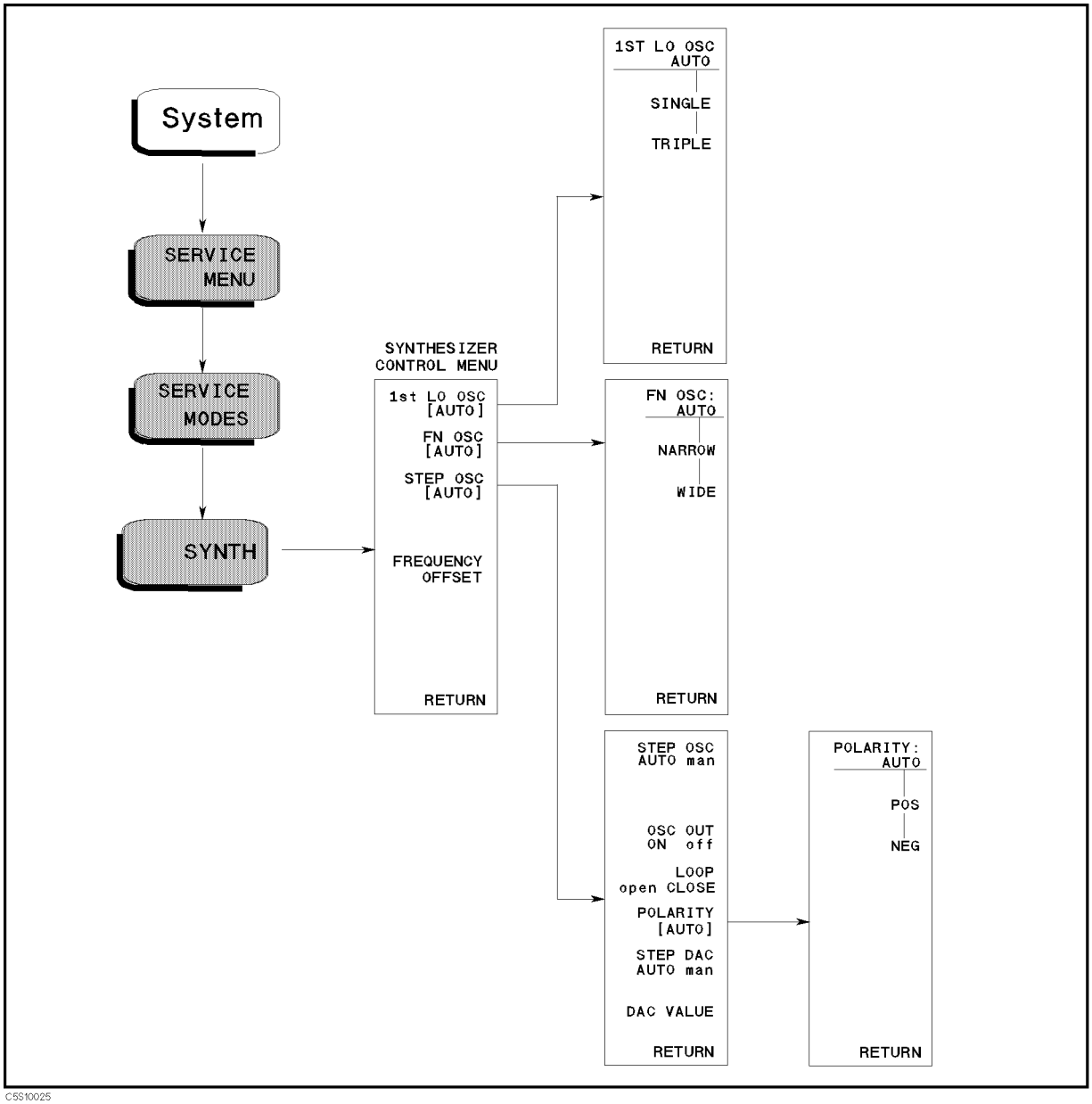


Figure 10-21. Synthesizer Control Menu

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1st LO OSC [ ] (:DIAG:SYNT:FLOC:MODE {AUTO|SING|TRIP})

Displays the control menu that allows you to control the 1st LO (first local oscillator) in the A4A1 1st LO. The softkeys in this control menu are described below. The abbreviation of the current setting (auto, single, or triple) is displayed in the brackets of the menu.

1ST LO OSC: AUTO	sets the 1st LO control to the automatic mode (normal operation). In this mode, the analyzer controls the 1st LO automatically according to the measurement settings.
SINGLE	sets the 1st LO to single mode.
TRIPLE	sets the 1st LO to triple mode.

FN OSC [ ] (:DIAG:SERV:STNT:FN:MODE {AUTO|NARR|WIDE})

Displays the control menu that allows you to control the FN OSC (fractional N oscillator) in the A5 synthesizer. The softkeys in this control menu are described below. The abbreviation of the current setting (auto, narrow, or wide) is displayed in the brackets of the menu.

IF BPF: AUTO	sets the IF BPF control to automatic mode (normal operation). In this mode, the analyzer set the IF BPF setting to the 3 MHz, 1 MHz, or crystal IF BPFs automatically according to the measurement setting.
NARROW	sets the FN OSC to narrow mode.
WIDE	sets the FN OSC to wide mode.

STEP OSC [ ]

Displays the control menus that allow you to control the STEP OSC (step oscillator) in the A5 synthesizer. The softkeys in these control menus are described below. The abbreviation of the current setting (AUTO or MANUAL) is displayed in the brackets of the menu.

STEP OSC AUTO man (:DIAG:SERV:SYNT:STEP:MODE {AUTO|MAN})

Toggles the STEP OSC control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the analyzer controls the STEP OSC automatically according to the measurement setting. In the manual mode, the STEP OSC is controlled by the following softkeys.

OSC OUT ON off (:DIAG:SERV:SYNT:STEP:OUTP {OFF|ON|0|1})

Toggles the STEP OSC output to on or off.

LOOP open CLOSE (:DIAG:SERV:SYNT:STEP:LOOP {OPEN|CLOSE})

Toggles the phase locked loop of the STEP OSC to open or close.

POLARITY [ ] (:DIAG:SERV:SYNT:STEP:POL {AUTO|POS|NEG})

Displays the control menu for ±1 converter in the STEP OSC. The softkeys in this control menu are described below. The abbreviation of the current setting (AUTO, POS, or NEG) is displayed in the brackets of the menu.

POLARITY: AUTO sets the ±1 converter control to automatic mode. In this mode, the analyzer selects one of the

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±1 converter automatically according to the measurement setting.

`POS` selects the +1 converter.

`NEG` selects the −1 converter.

`STEP DAC AUTO man` (:DIAG:SERV:SYNT:STEP:DAC:MODE {AUTO|MAN})

Toggles the STEP DAC mode in the STEP LO to automatic mode or manual mode. In the automatic mode, the analyzer sets the STEP DAC control value according to the measurement settings. In the manual mode, the STEP DAC control value is set by using the `DAC VALUE` softkey.

`DAC VALUE` (:DIAG:SERV:SYNT:STEP:DAC:VAL <*numeric*>)

Allows you to enter the STEP DAC control value (0 to 4095). This value is used when the STEP DAC is set to manual mode.

`FREQUENCY OFFSET` (:DIAG:SERV:SYNT:FREQ:OFFS<*numeric*>)

Allows you to enter the frequency offset value. Factory use only.

Note All settings must be turned to auto except when checking the analog circuits.



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SOURCE CONTROL MENU

Figure 10-22 shows the cbc hierarchy. To display the source control menu, press System, SERVICE MENU, SERVICE MODES, and SOURCE. Each softkey in the source control menus is described below.

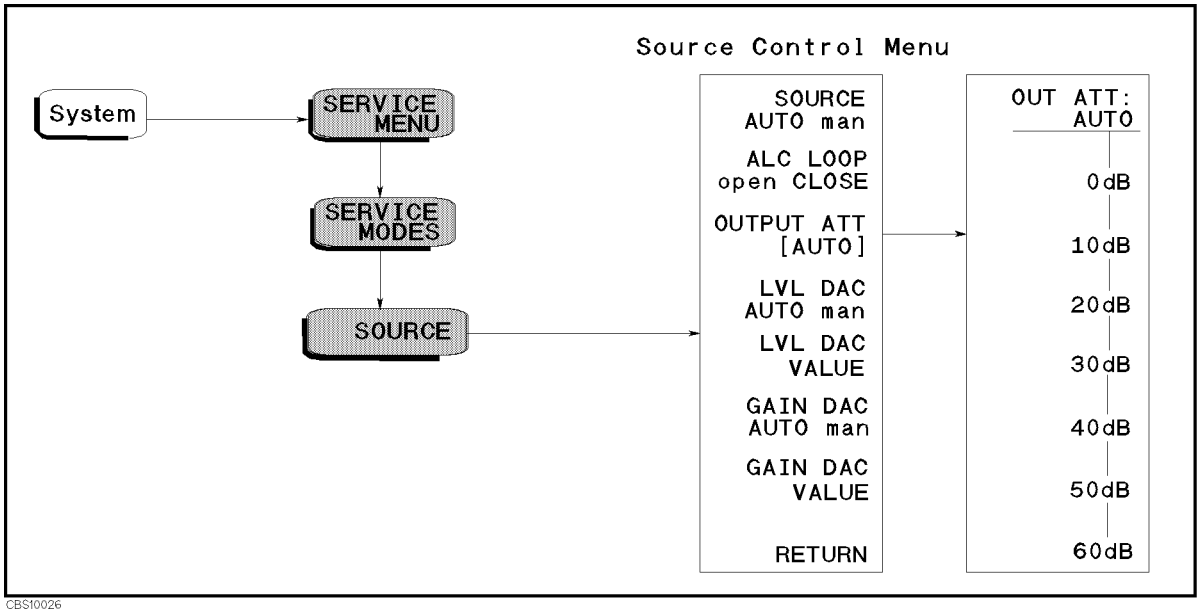


Figure 10-22. Source Control Menu

SOURCE AUTO man (:DIAG:SERV:SOUR:MODE {AUTO|MAN})

Toggles the source control mode to automatic mode and manual mode. In the automatic mode, the analyzer sets the source automatically according to the measurement settings. In the manual mode, the source are controlled by the following softkeys.

ALC LOOP open CLOSE (:DIAG:SERV:SOUR:ALCL: {OPEN|CLOSE})

Toggles the ALC (automatic leveling control) loop to open and close.

OUTPUT ATT [ ] (:DIAG:SERV:SOUR:ATT {AUTO|DB0|DB10|DB20|DB30|DB40|DB50|DB60})

Displays the control menu that allows you to control the A8 output attenuator. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

OUT ATT: AUTO	sets the A8 control to automatic mode. In this mode, the analyzer controls the A8 automatically according to the measurement setting.
0 dB	sets the A8 output attenuator to 0 dB.
10 dB	sets the A8 output attenuator to 10 dB.
20 dB	sets the A8 output attenuator to 20 dB.
30 dB	sets the A8 output attenuator to 30 dB.

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`40 dB` sets the A8 output attenuator to 40 dB.

`50 dB` sets the A8 output attenuator to 50 dB.

`60 dB` sets the A8 output attenuator to 60 dB.

`LVL DAC AUTO man` (:DIAG:SERV:SOUR:LEV:DAC:MODE {AUTO|MAN})

Toggles the level DAC control mode in the ALC to automatic mode and manual mode. In the automatic mode, the analyzer sets the level DAC according the measurement settings. In the manual mode, the level DAC output is controlled by the `DAC VALUE` softkey.

`LVL DAC VALUE` (:DIAG:SERV:SOUR:LEV:DAC:VAL <*numeric*>)

Allows you to enter the level DAC control value (0 to 4095). This value is used when the level DAC control mode is set to manual.

`GAIN DAC AUTO man` (:DIAG:SERV:SOUR:GAIN:DAC:MODE {AUTO|MAN})

Toggles the ALC gain control to automatic mode and manual mode. In the automatic mode, the analyzer sets the ALC gain according the measurement settings. In the manual mode, the ALC gain is controlled by the softkey `GAIN DAC VALUE`.

`GAIN DAC VALUE` (:DIAG:SERV:SYNT:STEP:DAC:VAL <*numeric*>)

Allows you to enter the ALC gain control value (0 to 15). This value is used when the ALC gain is set to manual mode (`GAIN DAC auto MAN`).

Note All settings must be turned to auto except when checking the analog circuits.



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BOOTLOADER MENU

Figure 10-23 shows the Bootloader menus and the associated menus. To display the menu, turning the analyzer on with pressing (Start) and (Preset). The Bootloader menu is used to install the firmware into the analyzer using a firmware diskette and the built-in FDD. Also these menus are used to make a system backup diskette. Each softkey in the Bootloader menus is described below.

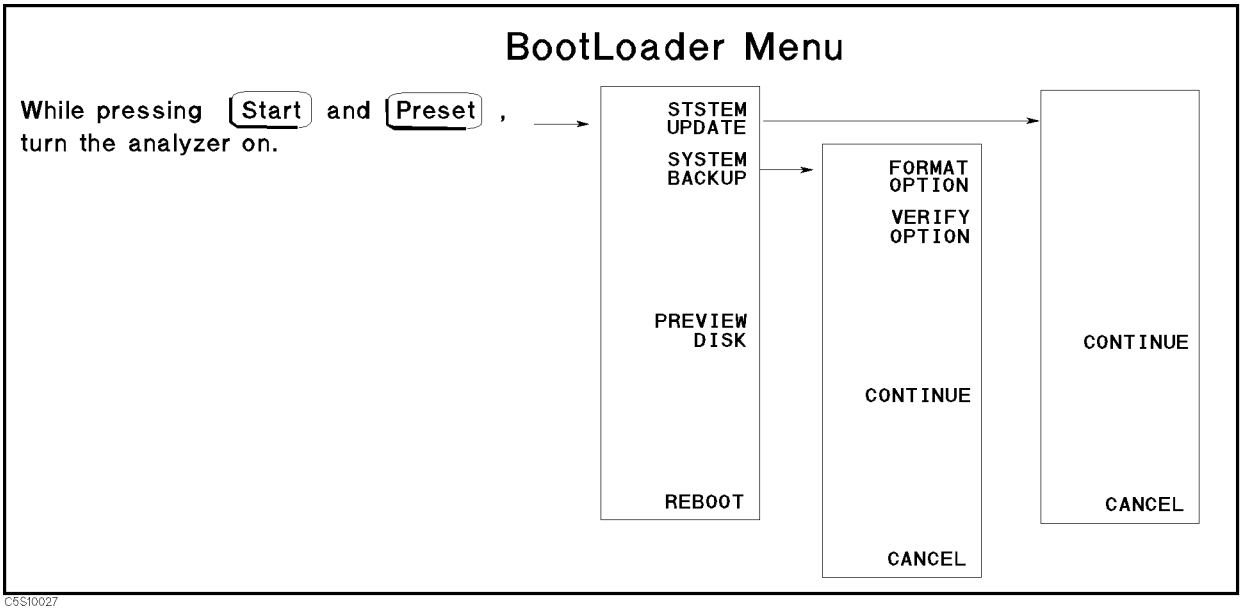


Figure 10-23. Bootloader Menu

SYSTEM UPDATE

Allows you to install and update the firmware in the analyzer. Before pressing this softkey, insert the firmware diskette into the FDD on the front panel. Then press this softkey to install the firmware from the diskette to the analyzer. The detailed procedure is provided in the *Firmware Installation* in chapter 14.

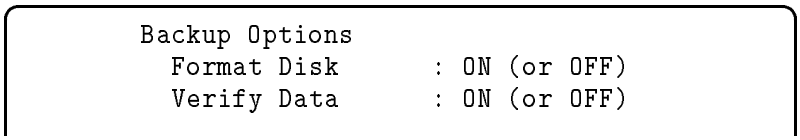
After pressing this softkey, CONTINUE and CANCEL softkeys appear on the display. Press CONTINUE to continue the firmware installation. Press CANCEL to cancel the firmware installation.

SYSTEM BACKUP

Displays the control menu that allows you to make a system backup diskette in which the current firmware is stored. The applicable diskette is a 3.5 inch 1.44 MByte flexible disk. The softkeys in the control menu are described below.

FORMAT OPTION toggles format option on and off. When the format option is set to on, the flexible diskette is initialized before storing the firmware. When the format option is set to off, the diskette is not initialized. The default setting is on. The format option setting is displayed as shown below.

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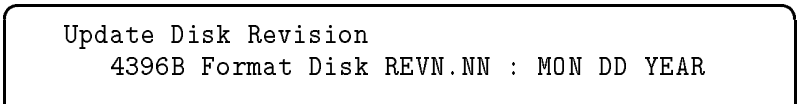
`VERIFY OPTION` toggles verify option on and off. When the verify option is set to on, the system stored in the flexible diskette is verified to be the same as the current firmware in the analyzer after storing the firmware. When the verify option is set to off, the verification is not performed. The default setting is on. The verify option setting is displayed as shown above.

`CONTINUE` continues making the system backup. Before pressing this softkey, insert a diskette into the FDD on the front panel.

`CANCEL` stops making the system backup and return to the Bootloader menu.

PREVIEW DISK

Displays the revision information of the firmware stored in the firmware diskette as shown below. Before pressing this softkey, insert a firmware diskette into the FDD on the front panel.



where N.NN: Revision Number
MON DD YEAR: Implementation Date (Month Day Year)

REBOOT

Reboots the analyzer. If the new firmware is installed, the analyzer boots up using the new firmware. After pressing the softkey, the analyzer performs the normal power on sequence.

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11

Theory of Operation

The theory of operation begins with a general description of the operation of a network and spectrum analyzer system (including the test sets). This description is followed by the detailed operating theory for the functional groups of the analyzer.

Each functional group consists of several assemblies that combine to perform basic instrument functions. These groups are the power supplies, the digital control, the source, and the receiver. The operation of each group is described to the assembly level only. Detailed component-level circuit theory is not provided in this manual.

Simplified block diagrams illustrate the operation of each functional group. The detailed analog section block diagram is provided at the end of this chapter.

ANALYZER OPERATION

The 4396B has two modes of operation: a network analyzer mode and a spectrum analyzer mode. To perform these operations, the analyzer uses four functional groups: a source, a receiver, a digital control, and a power supply. See Figure 11-1.

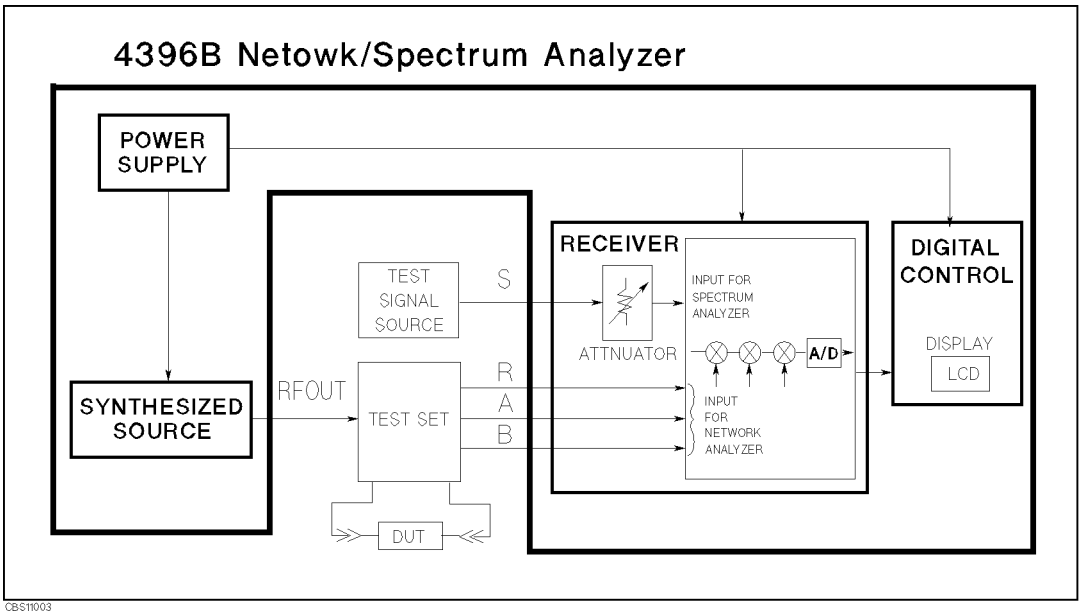


Figure 11-1. Simplified Analyzer Block Diagram

The source includes a synthesizer. The synthesizer generates reference signals and two local oscillator signals. These signals are used in the source and the receiver.

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The receiver has four inputs (R, A, B, and S). The receiver is used in both the network analyzer mode and the spectrum analyzer mode. To operate in both the network and spectrum analyzer modes using one receiver, the receiver has two switches, an Input Multiplexer and a NA/SA switch at the front end. One of the signals from the four inputs (R, A, B, or S) is switched to the circuit following these switches.

Spectrum Analyzer Operation

A spectrum analyzer measures the amplitude and frequency of a signal spectral line by sweeping the tuning frequency of the receiver.

A typical spectrum analyzer consists of four main groups: a synthesizer, a receiver, a digital control, and a power supply. In the 4396B, the synthesizer is included in the source.

The RF signal to be tested is applied to the receiver. The receiver converts the signal frequency to a 20 kHz or DC 3rd IF (third intermediate frequency) for signal processing. It then converts the signal to a digital value using the A/D (analog to digital) converter. The digitized raw data is then transferred to the digital control group.

The raw data is processed in the digital control group. The formatted data is finally routed to the LCD for display, and to the GPIB for remote operation. For details of the data processing signal flow, see the *Analyzer Feature* chapter of the *4396B Function Reference Manual*.

In the 4396B, the receiver requires three local oscillator signals to convert the RF signal to the 1st/2nd/3rd IF signals. The synthesizer in the analyzer's source generates the 1st and 2nd local oscillator signals and supplies these signals to the receiver. The third local oscillator signal is generated in the receiver.

The power supply regulates all the required voltages from the AC power and supplies power to all the assemblies in the analyzer.

Network Analyzer Operation

A network analyzer measures the reflection and transmission characteristics of devices by applying a known swept signal and measuring the response of the DUT (device under test).

A typical network analyzer system consists of a network analyzer and signal separation devices (a test set or power splitter). Furthermore, the network analyzer consists of four main groups: a source, a receiver, a digital control, and a power supply.

The 4396B's built-in synthesized source generates a known CW (continuous wave) or swept RF signal in the range of 100 kHz to 1.8 GHz. The RF signal power is leveled using the ALC (automatic leveling control), to a maximum level of +20 dBm. In addition, the source supplies the local oscillator signals to the receiver.

The source's RF signal is applied to the DUT through the signal separation device. The signal transmitted through the device or reflected from its input goes to the B and/or A inputs of the receiver and is compared with the incident signal at the R input. The signal separation device in the network analyzer system is an 85046A/B S-Parameter test set, an 87512A/B transmission/reflection test set, or an 11850C/D or 11667A power splitter. The test sets are described below.

The receiver converts the RF input frequency to a 20 kHz or DC 3rd IF for signal processing. It then converts the signal to a digital signal using the A/D converter. The digitized raw data is transferred to the digital control group.

The raw data is then processed in the digital control. The formatted data is finally routed to the LCD for display, and to the GPIB for remote operation. For details of the data processing signal flow, see the *Analyzer Feature* chapter of the *4396B Function Reference Manual*.

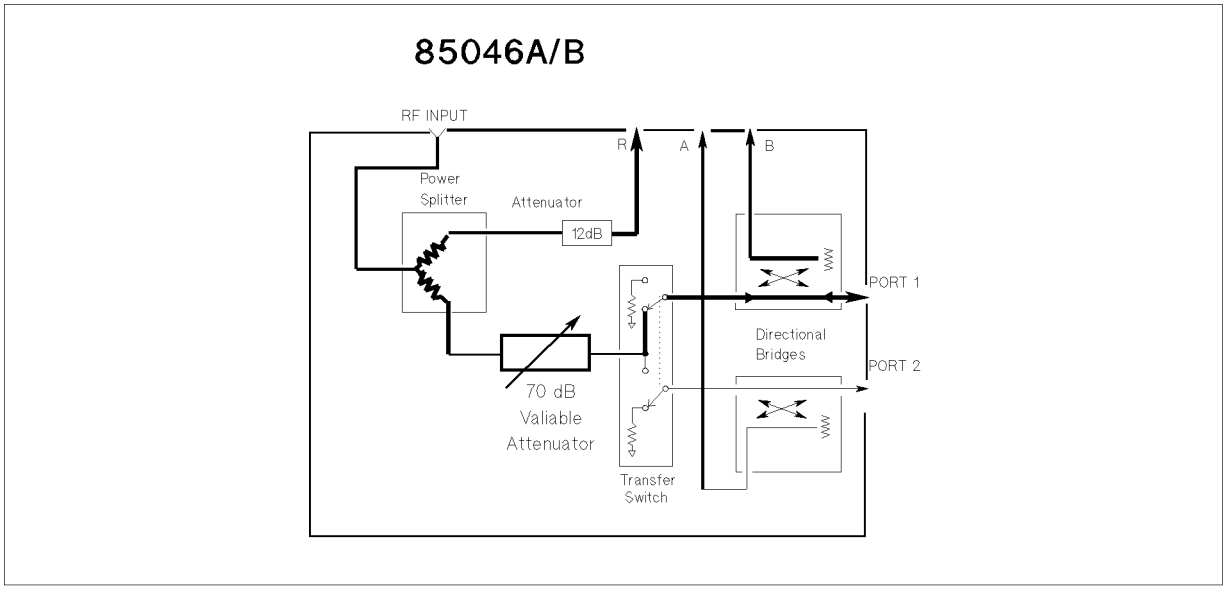
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The power supply regulates all the required voltages from the AC power and supplies power to all the assemblies in the analyzer.

Test Sets

The test sets are described briefly. For more information about the test sets, see the applicable test set manual.

The 85046A/B S-Parameter test set contains a power splitter to divert a portion of the incident signal to the R input of the analyzer for reference. The remainder of the incident signal is routed through a switch to one of two directional bridges at the measurement ports. The RF path switch is controlled by the analyzer to enable switching between forward and reverse measurements. A 70 dB step attenuator in the test set, also controlled from the analyzer, adjusts the power level to the DUT without changing the level of the incident power in the reference path. Two bias tees are included, for external biasing of active devices connected to the test ports. Figure 11-2 shows a simplified block diagram of the 85046A/B.



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Figure 11-2. 85046A/B S-Parameter Test Set Simplified Block Diagram

The 87512A/B transmission/reflection test set contains a power splitter to divert a portion of the incident signal to the R input of the analyzer. The remainder of the incident signal is routed through a directional bridge to the measurement port.

In addition to the analyzer and signal separation devices, a network measurement system includes cables for interconnections, and a calibration standard for accuracy enhanced measurement.

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ANALYZER FUNCTIONAL GROUPS

The analyzer consists of four main functional groups: a source, a receiver, a digital control, and a power supply. Each group consists of several major assemblies, and performs a distinct function in the analyzer. However, all the groups are interrelated to some extent and affect each other's performance.

Power Supply: The power supply functional group consists of the A40 preregulator, the A50 DC-DC converter and the A2 post-regulator. It supplies power to the other assemblies in the analyzer.

Digital Control: The digital control group consists of the A1 CPU, the A30 keyboard, the A31 I/O connector, the A32 Instrument BASIC interface, the A51 GSP (Graphics System Processor), the A52 LCD (Liquid Crystal Display), and the A53 FDD (Flexible Disk Drive). These assemblies combine to provide digital control for the analyzer and an S-Parameter Test set (if used).

Source: The source group consists of the A5 synthesizer, the A4A1 1st LO (1st local oscillator), the A3A1 ALC (automatic leveling control), the A3A2 2nd LO (second local oscillator), the A3A3 source, the A7 output attenuator, and the A60 high stability frequency reference (option 1D5 only). The source supplies a phase-locked RF signal to the device under test and supplies the 1st and 2nd local oscillator signals to the receiver.

Receiver: The receiver group consists of the A9 input multiplexer, the A8 input attenuator, A4A2 receiver RF, and the A6 receiver IF. The receiver measures and processes RF signal inputs for display.

The following pages describe the operation of the functional groups.

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POWER SUPPLY OPERATION

The power supply functional group consists of the following assemblies:

- A40 Preregulator
- A50 DC-DC Converter
- A2 Post-Regulator

These three assemblies comprise a switching power supply that provides regulated DC voltages to power all assemblies in the analyzer. See Figure 11-3.

The A40 preregulator steps down and rectifies the line voltage, and provide +24 V to the A50 DC-DC converter.

The A50 DC-DC converter contains two switching regulators, and provides the follwing six power supply voltages.

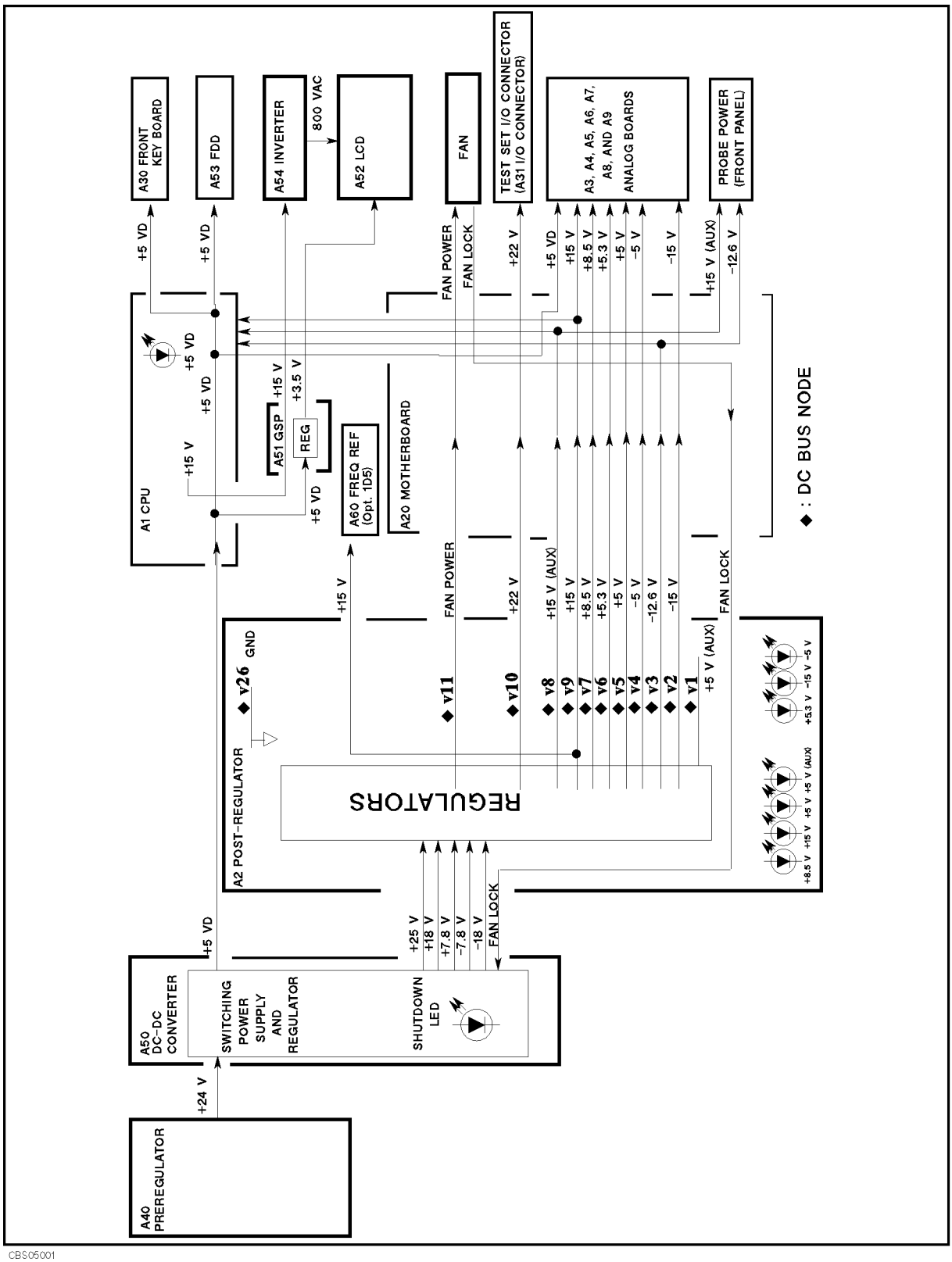
+5 VD, +7.8 V, -7.8 V, +18 V, -18 V and +24 V

The +5 VD (+5 V digital supply) is fully regulated in A50 and is directly supplied to the A1 CPU. The other five power supplies are preregulated in A50 and go to the A2 post-regulator for final regulation. A50 receives the FAN LOCK signal from the fan through the A20 motherboard and the A2 post-regulator.

The A2 post-regulator filters and regulates the five power supply voltages from A50. It distributes the following eleven regulated voltages to individual assemblies throughout the analyzer:

FAN POWER (+24 V), +22 V, +15 V, +15 V (AUX), +8.5, +5.3 V, +5 V, +5 V (AUX), −5 V, −12.6 V, −15 V

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Figure 11-3. Power Supply Functional Group, Simplified Block Diagram

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Line Power Module

The line power module includes the main fuse. The main fuse, which protects the input side of the preregulator from drawing too much line current, is also accessible at the rear panel. See *Power Requirements* in appendix C for the fuse replacement and other power considerations.

A40 Preregulator

The A40 preregulator contains a rectifier and a switching regulator, converts the line voltage to +24 V and provides it to the A50 DC-DC converter.

A50 DC-DC Converter

The A50 DC-DC Converter consists of the two switching regulators (1 and 2). The DC-DC convereter provides an LED (visible at the top) to indicate circuit status. See Figure 5-12 in chapter 5. The shutdown LED is turned off when the overcurrent protection circuit activates. The circuit activates when an overcurrent is sensed on the +5 VD power line, when an overcurrent is sensed on the four power supplies (±18 V and ±7.8 V), or when the FAN LOCK signal is sensed. It shuts down the five power supplies of the switching regulators (1 and 2). For A50 to work properly, the +7.8 V must be loaded (approximately 680 ohms, more than 125mW). If it is not, the other preregulated voltages in the A50 DC-DC converter will not be correct.

Switching Regulator 1

Switching regulator 1 converts the +24 V to the regulated +5 VD (digital supply). The +5 VD goes directly to the A1 CPU.

Switching Regulator 2

Switching preregulator 2 converts the +24 V to four DC voltages, +7.8 V, −7.8 V, +18 V, −18 V. The voltages are routed to the A2 post-regulator for final regulation.

Regulated + 5V Digital Supply (+ 5 VD)

The +5VD power supply is fully regulated in the A50 DC-DC converter. It goes directly to the A1 CPU and is supplied to all assemblies requiring a digital +5 V supply through A1, and the A20 motherboard. See Figure 11-3.

A50 Shutdown LED

The A50 shutdown LED is on during normal operation. It turns off when the A50 protective circuits are activated and shut down some power lines. The shutdown LED turns off when one of the following conditions is sensed:

- Overcurrent on +5 VD Power Line.
- Overcurrent on the four power supplies (±18 V and ±7.8 V)
- Fan is not rotating (FAN LOCK signal is sensed).

The fan obtains its power +24 V from A40 preregulator through the A50 DC-DC converter and the A2 post-regulator. When the power is missing, the FAN LOCK signal shuts the switching regulators down and turns the A50 shutdown LED off.

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A2 Post-Regulator

The A2 post-regulator consists of seven filters, nine regulators, and the drive circuits for the A7 output attenuator and the A8 input attenuator. See Figure 5-13 in chapter 5.

The A2 post-regulator distributes the following eleven power supply voltages to individual assemblies throughout the analyzer. Each of the nine regulators receives the DC voltage pre-regulated in A50 through a filter and converts it to one of the fully regulated constant DC voltages listed below:

FAN POWER	is derived from the +24 V supply from A40. It powers the fan.
+22 V	is derived from the +24 V supply from A50. It goes to the TEST SET I/O INTERCONNECT connector and powers the Test Set connected to the 4396B rear panel.
+15 V	is derived from the +18 V supply from A50. It powers analog assemblies A3 through A9.
+15 V (AUX)	is derived from the +18 V supply from A50. It powers the three probe power outputs on the front panel.
+8.5 V	is derived from the +15 V supply regulated in the A2 post-regulator. It powers the A3A3 source.
+5.3 V	is derived from the +7.8 V supply from A50. It powers the A3A3 source.
+5 V	is derived from the +7.8 V supply from A50. It powers analog assemblies A3 through A9.
+5 V (AUX)	is derived from the +24 V or +18 V supplies from A50. It powers A2.
−5 V	is derived from the −7.8 V supply from A50. It powers analog assemblies A3 through A9.
−12.6 V	is derived from the −18 V supply from A50. It powers the probe power connector.
−15 V	is derived from the −18 V supply from A50. It powers analog assemblies A3 through A9.

The A2 post-regulator is equipped with a protective shutdown circuit.

The A2 post-regulator provides two LED arrays, visible at the top edge of the A2 post-regulator. Each LED array consists of four LEDs and indicates the status of the seven power supplies.

Shutdown Circuit

Four regulators for power supplies, +15 V, +5 V, −5 V, and −15 V are equipped with the capability of sensing overcurrent, and overvoltage, undervoltage on their output lines. When a regulator senses one of these conditions, it triggers the protective shutdown circuit. The circuit is also triggered by an over temperature condition in A2.

The following power supplies are not shutdown:

FAN POWER, +22 V, +12.6 V, +15 V (AUX), +5 V (AUX)

The shutdown circuit also provides the shutdown status to the A1 CPU. When the circuit is activated, it triggers the A1 CPU. The A1 CPU checks the shutdown status on the A2 post-regulator and displays a warning message. Then the analyzer stops its operation. Once the analyzer stops the operation, the front-panel keys are disabled. The only way to reset the analyzer is to turn the analyzer power off then on.

Seven Status LEDs

The seven status LEDs on the A2 post-regulator are on during normal operation. They indicate that the correct voltage is present in each supply. See Figure 11-4. If one (or more) of them is off or flashing, there is a problem in the corresponding power supply.

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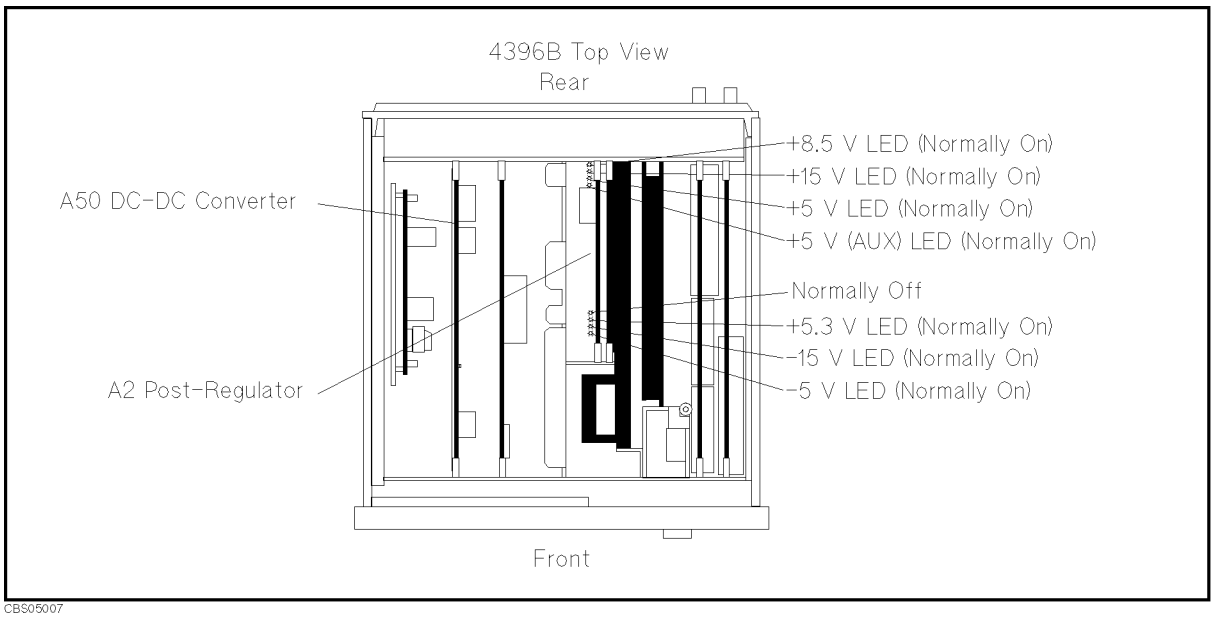


Figure 11-4. A2 Eight Status LED

A7 Input and A8 Output Attenuator Drive Circuit

The A2 post-regulator has the drive circuit for the A7 input attenuator and the A8 output attenuator. The circuit decodes the control signal from the A1 CPU and generates the following TTL signals:

- A7 output attenuator drive signals (10 dB ON/OFF, 20 dB ON/OFF, 30 dB ON/OFF).
- A8 input attenuator drive signals (10 dB ON/OFF, 20 dB ON/OFF, 30 dB ON/OFF).

These signals are supplied to A7 and A8 through the A20 motherboard.

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DIGITAL CONTROL OPERATION

The digital control functional group consists of the following assemblies:

- A1 CPU
- A30 Front Keyboard
- A31 I/O Connector
- A32 I-BASIC Interface
- A51 GSP
- A52 LCD (Liquid Crystal Display)
- A53 FDD (Flexible Disk Drive)

These assemblies combine to provide digital control for the analyzer and the 85046A/B S-Parameter test set. They provide math processing functions, as well as communications between the analyzer and an external controller and/or peripherals. Figure 11-5 is a simplified block diagram of the digital control functional group.

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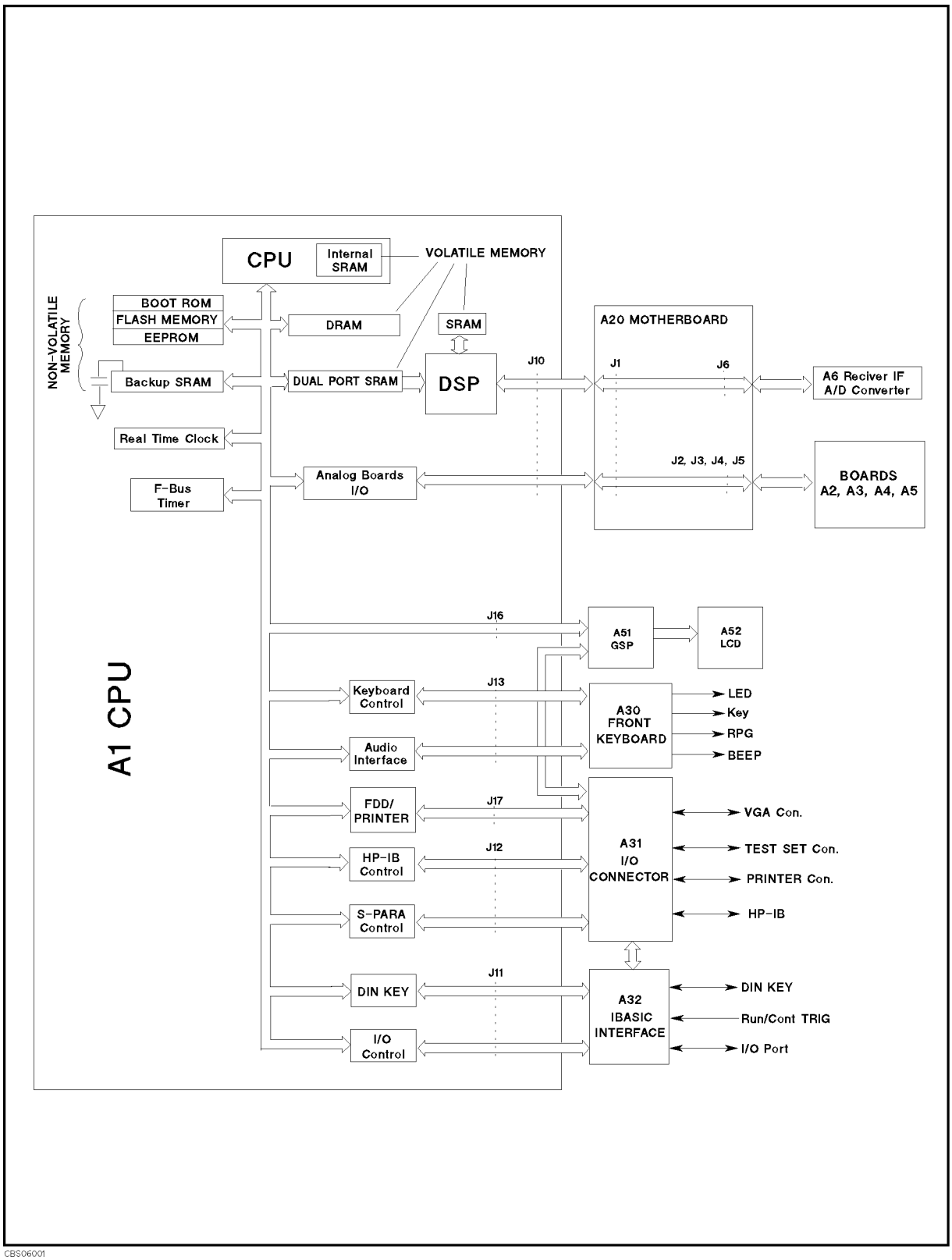


Figure 11-5. Digital Control Group, Simplified Block Diagram

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A1 CPU

The A1 CPU consists of the following circuits and parts (See Figure 11-5):

CPU	central processing unit that controls the analyzer.
DSP	digital signal processor that is used for fast data processing.
Memory storages	consists of BOOT ROMs, Flash Memory, EEPROM, Backup SRAM, DRAM, and Dual Port SRAM. The backup SRAM is powered from a large capacitor that is charged when the analyzer is turned on. Therefore, the SRAM keeps its data at least 72 hours after the analyzer is turned off. The Dual Port SRAM is used for communication between the CPU and DSP.
F-Bus Timer	is used in the frequency bus measurement that is a diagnostic function of the analyzer. For a description of the frequency bus measurement, see the *Service Key Menus* chapter.
Analog Board Interface	interfaces between the CPU and analog assemblies A3 through A9
Keyboard Controller	controls the A30 front-panel keyboard.
Audio Interface	controls the beeper on the A30 front-panel keyboard.
FDD Control	controls the A53 FDD.
GPIB Control	communicates with the external GPIB devices through the GPIB connector on the A31 I/O connector.
S-Para Control	controls a test set through the TEST SET I/O INTERCONNECT connector on the A31 I/O connector.
External Keyboard Control	interfaces between the CPU and the external keyboard through the mini DIN connector on the A32 I-BASIC Interface.
I/O Control	controls the external devices through the I/O PORT connector on the A32 IBASIC interface. It also interfaces between the CPU and the external inputs through the EXT PROG RUN/CONT connector.

A30 Front-Panel Keyboard

The A30 front-panel keyboard assembly detects your inputs (key inputs and RPG inputs) from the front panel of the analyzer, and transmits them to the keyboard controller on A1.

A31 I/O Connector

The two A31 I/O connectors are the GPIB connector and the TEST SET I/O INTERCONNECT connector. These connectors are connected to the GPIB controller and the S-parameter control circuit on A1 through the A20 motherboard.

A32 I-BASIC Interface

The three A32 I/O connectors are the EXT PROG RUN/CONT connector, the I/O Port connector, and the mini DIN Keyboard connector. These connectors are connected to the I/O control and mini DIN control circuit on A1 through the A20 motherboard.

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A51 GSP

The A51 GSP (graphics system processor) provides an interface between the A1 CPU and the A52 LCD. The A1 CPU converts the formatted data to GSP commands and writes them to the A51 GSP. The A51 GSP processes the data to obtain the necessary signals and sends these signals to the A52 LCD

The A51 GSP receives two power supply voltages: +5 VD, which is used for data processing and converted to +3.3 V, and +15 V, which is passed on the A54 Inverter. The +3.3 V goes to the A52 LCD. See Figure 5-1 for more details.

A54 Inverter

The A54 Inverter is located in the LCD module on the front panel assembly. The A54 receives +15 V from A1 CPU and provides a high voltage (800 to 1000 VAC) to the backlight of the LCD. See Figure 5-1 for more details.

A52 LCD (Liquid Crystal Display)

The A52 LCD is a 8.4 TFT Color LCD, receives a high voltage (800 to 1000 VAC) from the A54 Inverter as backlight power and the digital horizontal and the vertical signals from the A51 GSP.

A53 FDD

The analyzer has a built-in, 3-1/2 inch FDD (Flexible Disk Drive) on the front panel. It uses 2 high density or 2 double density 3-1/2 inch flexible disks. The A53 FDD stores and retrieves data to and from the disk.

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SOURCE THEORY

The two functional subgroups of the source group are the synthesizer and the ALC (automatic leveling control).

The synthesizer subgroup generates the 40 MHz reference frequency, the 1st local oscillator signal (2.05858 GHz to 3.85858 GHz), and the second local oscillator signal (2.08 GHz). These signals are used in both the ALC subgroup in the source functional group and in the receiver functional group.

There are two synthesizer operation modes used in generating the first local oscillator signal, the single-loop mode and the triple-loop mode. The single- loop mode is used to generate the 1st local oscillator signal when the frequency span setting of the analyzer is wider than 45 MHz. At frequency span settings $\leq$ 45 MHz, the triple-loop mode is used to generate the 1st local oscillator signal with low phase noise.

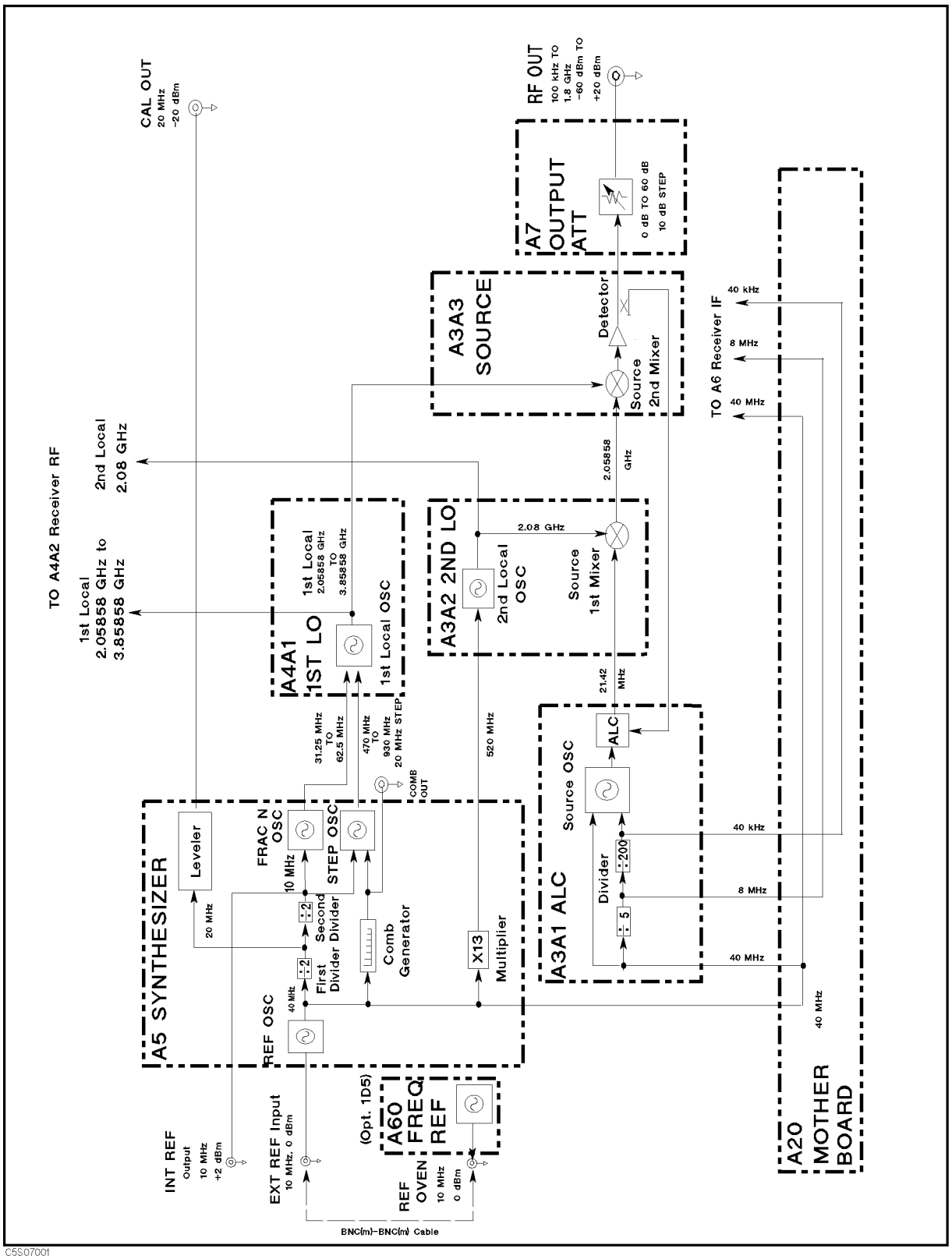
The ALC subgroup generates a stable and accurate RF OUT signal. This signal is a CW or swept signal between 100 kHz to 1.8 GHz with a power level from −60 dBm to +20 dBm.

Figure 11-6 shows the simplified block diagram of the source functional group. The source group consists of the following assemblies:

- A5 Synthesizer
- A4A1 1st LO
- A60 High Stability Frequency Reference (Option 1D5)
- A3A1 ALC
- A3A2 2nd LO
- A3A3 Source
- A7 Output Attenuator

The first three assemblies and part of the A3A2 2nd LO belong to the synthesizer subgroup. The remaining four assemblies belong to the ALC subgroup. A3A2 contains the second local oscillator and the source first mixer. The second local oscillator is part of the synthesizer subgroup. The source first mixer is part of the ALC subgroup.

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Figure 11-6. Source Simplified Block Diagram

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A5 Synthesizer

The A5 synthesizer provides a 40 MHz reference frequency, a 20 MHz CAL OUT signal, an INT REF signal, a FRAC N OSC signal, a STEP OSC signal, and a 520 MHz signal.

The 40 MHz reference signal is supplied to the A3A1 ALC and the A6 receiver IF and is used as the reference signal. The FRAC N OSC and the STEP OSC signals are supplied to the A4A1 1st LO and are used to generate the 1st local oscillator signal. The 520 MHz signal is supplied to the A3A2 2nd LO and is used to generate the second local oscillator signal.

The A5 Synthesizer consists of the following circuits:

- REF OSC (Reference Oscillator)
- Leveler
- FRAC N OSC (Fractional N Oscillator)
- STEP OSC (Step Oscillator)
- X 13 Multiplier

REF OSC

The REF OSC generates three stable reference frequencies of 40 MHz, 20 MHz, and 10 MHz. It does this by dividing the output of a 40 MHz VCXO (voltage control crystal oscillator) as required. The 40 MHz reference signal is supplied to the A3A1 ALC. The 20 MHz reference frequency goes to the CAL OUT connector on the front panel (through the leveler). The 10 MHz reference frequency is routed to the INT REF Output connector on the rear panel.

When a 10 MHz external reference signal is applied to the EXT REF Input connector on the rear panel, the REF OSC output signals are phase locked to the external reference signal.

The REF OSC is a phase locked oscillator and contains a 40 MHz VCXO, a phase detector, and three 1/2 dividers. See Figure 11-8. When the 10 MHz external reference signal is applied to the EXT REF Input connector on the rear panel, the reference frequency is divided by two. It is then compared with the VCXO frequency ($\mathbf{F_{vcxo}}$) divided by eight in the phase detector. Phase locking imposes the condition of 10 MHz/2 = $\mathbf{F_{vcxo}}$/8. Therefore, the output frequency ($\mathbf{F_{vcxo}}$) is locked to 40 MHz.

A detector circuit detects the external reference input signal and sends the status to the A1 CPU. Then the A1 CPU displays a message (**ExtRef**) on the CRT. In addition, an unlock detector monitors the control voltage to the VCXO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. Then the A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The *40 MHz Reference Oscillator Frequency Adjustment* adjusts the VCXO to lock to the 40 MHz when the external reference signal is not applied.

Leveler

The leveler is a power amplifier that produces a power level of 20 dBm ± 0.4 dB. The front-panel CAL OUT signal is derived from the 20 MHz reference signal from the REF OSC through the leveler. The *CAL OUT Level Adjustment* adjusts the leveler to output a CAL OUT signal at the specified power level.

FRAC N OSC

The FRAC N OSC (Fractional N Oscillator) generates a swept signal of 31.25 MHz to 62.5 MHz with a high frequency resolution. The signal is supplied to the A4A1 1st LO and is used to generate the swept 1st local oscillator signal.

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The FRAC N OSC is a phase locked oscillator. The output signal is phase locked to the 10 MHz reference signal of the REF OSC. The oscillator contains a 31.25 MHz to 62.5 MHz VCO, a phase detector, and a fractional N divider (N.F. divider: 1/integer.fraction). See Figure 11-8.

The 10 MHz reference signal from the REF OSC is applied to the phase detector through the 1/10 divider. The reference signal is then compared with the VCO frequency ($\mathbf{F_{vco}}$) divided by the fractional N divider in the phase detector. Phase locking imposes the condition of 10 MHz/10 = $\mathbf{F_{vco}}$/N.F. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 1 MHz x N.F.

The fractional N divider is a dedicated divider used to generate the high frequency resolution signal. It divides the signal frequency by a real value (N.F.). The resolution of the fractional part F is 3.55 x 10^{-15} (= $1/2^{48}$). Therefore, the FRAC N OSC generates a swept signal with 3.55 nHz (1 MHz x 3.55 x 10^{-15}) frequency resolution. The fractional N divider is controlled by the A1 CPU and the A6 Receiver IF.

STEP OSC

The STEP OSC (Step Oscillator) generates a CW signal between 470 MHz and 930 MHz in 20 MHz steps. The signal is supplied to the A4A1 1st LO and is used to generate the 1st local oscillator signal (only in the triple-loop mode). The output signal frequency depends on the frequency center setting as shown in Table 11-1.

Table 11-1. STEP OSC Frequency

4396B Center Frequency	STEP OSC Frequency
0 Hz ≤ Center < 48.92 MHz	470 MHz
48.92 MHz ≤ Center < 128.92 MHz	490 MHz
128.92 MHz ≤ Center < 208.92 MHz	510 MHz
208.92 MHz ≤ Center < 288.92 MHz	530 MHz
288.92 MHz ≤ Center < 368.92 MHz	550 MHz
368.92 MHz ≤ Center < 448.92 MHz	570 MHz
448.92 MHz ≤ Center < 528.92 MHz	590 MHz
528.92 MHz ≤ Center < 608.92 MHz	610 MHz
608.92 MHz ≤ Center < 688.92 MHz	630 MHz
688.92 MHz ≤ Center < 768.92 MHz	650 MHz
768.92 MHz ≤ Center < 848.92 MHz	670 MHz
848.92 MHz ≤ Center < 928.92 MHz	690 MHz
928.92 MHz ≤ Center < 1008.92 MHz	710 MHz
1008.92 MHz ≤ Center < 1088.92 MHz	730 MHz
1088.92 MHz ≤ Center < 1168.92 MHz	750 MHz
1168.92 MHz ≤ Center < 1248.92 MHz	770 MHz
1248.92 MHz ≤ Center < 1328.92 MHz	790 MHz
1328.92 MHz ≤ Center < 1408.92 MHz	810 MHz
1408.92 MHz ≤ Center < 1488.92 MHz	830 MHz
1488.92 MHz ≤ Center < 1568.92 MHz	850 MHz
1568.92 MHz ≤ Center < 1648.92 MHz	870 MHz
1648.92 MHz ≤ Center < 1728.92 MHz	890 MHz
1728.92 MHz ≤ Center < 1808.92 MHz	910 MHz
1808.92 MHz ≤ Center < 1820.00 MHz	930 MHz

The STEP OSC consists of a comb generator and a phase locked oscillator that is phase locked to the 10 MHz reference signal of the REF OSC.

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The comb generator receives the 40 MHz reference signal from the REF OSC and multiples the fundamental signal into a comb of harmonic frequencies (40 MHz x N). The level of the harmonics is adjusted in the *Comb Generator Adjustment*.

The phase locked oscillator consists of a 470 MHz to 930 MHz VCO, a phase detector, a mixer, a pretune DAC and ±1 converters. See Figure 11-6. The VCO frequency ($\mathbf{F_{vco}}$) is mixed with the comb generator output in the mixer. The mixer produces multiple harmonics ($\mathbf{F_{vco}} \pm$ 40 MHz x N) through the LPF (low pass filter). The mixer output is compared with the 10 MHz reference signal in the phase detector. Phase locking imposes the condition of 10 MHz = $\mathbf{F_{vco}} \pm$ 40 MHz x N, and the loop locks to the nearest 40 MHz harmonic satisfying that condition. The initial frequency ($\mathbf{F_{vco}}$) is set to the desired harmonic frequency of **40 MHz x N** (N = 12 to 23) using the pretune DAC. This locks the output frequency ($\mathbf{F_{vco}}$) to the desired **40 MHz x N ± 10 MHz** selection of the frequencies listed in Table 11-1. The polarity of the 10 MHz offset is controlled by the ±1 converters in the loop.

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The pretune DAC values are predefined by performing the *Step Pretune Correction Constants* and are stored in the EEPROM in the A1 CPU.

Multiplier (X 13)

The multiplier receives the 40 MHz reference signal and generates a 520 MHz signal. This signal is supplied to A3A2 2nd LO and is used to generate the second local oscillator signal. See Figure 11-6. The 520 MHz signal level is adjusted in the *520 MHz Level Adjustment*.

A4A1 1st LO

The A4A1 1st LO generates the swept 1st local oscillator signal 2.05858 GHz to 3.85858 GHz with 1 mHz resolution. The sweep range depends on the start and stop (or center and span) settings of the analyzer. The signal frequency sweeps between the start frequency + 2.05858 GHz to the stop frequency + 3.85858 GHz.

The 1st local oscillator signal is supplied to the A3A3 source and the A4A2 receiver RF. In A3A3, the local oscillator signal is used to convert the 2.05858 GHz IF (intermediate frequency) signal to the 100 kHz to 1.8 GHz RF signal. A4A2 also uses the first local to convert the RF input signal to the IF signal.

In addition, the A4A1 1st LO decodes two digital control signals for the A4A2 Receiver RF, and the decoded signals are supplied to A4A2.

1st Local OSC Circuit

The 1st local oscillator circuit is a phase locked oscillator. The output signal is phase locked to the FRAC N OSC output signal. The oscillator contains a 2.05858 GHz to 3.85858 GHz VCO, a phase detector, a 1/4 divider, a mixer, a 1/16 divider, and a single/triple switch. See Figure 11-8.

The single/triple switch is for the single/triple mode and switches the VCO signal to one of the mixers and the 1/16 divider.

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of the limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

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Single-Loop Operation at Frequency Spans > 45 MHz. In the single-loop mode, the VCO signal loops back to the phase detector through the 1/4 divider and the 1/16 divider. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 64 and then compared with the FRAC N OSC signal frequency ($\mathbf{F_{frac}}$) (31.25 MHz to 62.5 MHz) in the phase detector. Phase locking imposes the condition of $\mathbf{F_{frac}} = \mathbf{F_{vco}}$ /64. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to $\mathbf{F_{frac}}$ x 64. The $\mathbf{F_{vco}}$ sweeps from 2 GHz (31.25 MHz x 64) to 4 GHz (62.5 MHz x 64) according to the FRAC N OSC; swept signal. The frequency range actually used in the analyzer is 2.05858 GHz (at a measurement frequency 0 Hz) to 3.85858 GHz (at a measurement frequency 1.82 GHz).

Triple-Loop Operation at Frequency Spans ≤ 45 MHz. In the triple-loop mode, the VCO signal loops back to the phase detector through the 1/4 divider and the mixer. The VCO frequency ($\mathbf{F_{vco}}$) is mixed with the STEP OSC output ($\mathbf{F_{step}}$) in the mixer. The mixer then produces the shifted frequency of $\mathbf{F_{vco}}/4 - \mathbf{F_{step}}$. The mixer output is compared with the FRAC N OSC output signal in the phase detector. Phase locking imposes the condition of $\mathbf{F_{frac}} = \mathbf{F_{vco}}/4 - \mathbf{F_{step}}$. Therefore, the output frequency $\mathbf{F_{vco}}$ is locked to $\mathbf{F_{frac}}$ x 4 + $\mathbf{F_{step}}$ x 4. The $\mathbf{F_{vco}}$ sweeps over the appropriate range determined by the start and stop setting according to the $\mathbf{F_{frac}}$.

The $\mathbf{F_{step}}$ is determined by the center frequency of the analyzer as shown in Table 11-1. The $\mathbf{F_{frac}}$ sweeps between {(start frequency + 2.05858 GHz)/4 - $\mathbf{F_{step}}$}/4 to {(stop frequency + 2.05858 GHz)/4 - $\mathbf{F_{step}}$}/4.

Digital Control Signals for the A4A2 Receiver RF

The A4A2 1st LO has the decoder circuitry for the following digital control signals. These signals come from the A1 CPU. The decoded signals are supplied to the A4A2 Receiver RF through the cable at A4A1J2.

- NA/SA Switch Control Signal
- AZ (Auto Zero) Control Signal

A3A1 ALC

The A3A1 ALC generates the level-controlled 21.42 MHz IF signal, an 8 MHz reference signal, and a 40 kHz reference signals.

The 21.42 MHz signal is supplied to the A3A2 2nd LO and converted to a 2.05858 GHz IF signal through the source first converter. The 8 MHz and 40 kHz signals are supplied to the A6 receiver IF and used as reference signals.

The A3A1 ALC consists of the following circuits:

- Divider
- Source OSC (Source Oscillator)
- ALC (Automatic Leveling Control)

Divider

The divider contains a 1/5 divider and a 1/200 divider. The 40 MHz reference frequency from the A5 synthesizer is down converted to 8 MHz and 40 kHz through the two dividers. The two signals are then supplied to the A6 receiver IF through the A20 motherboard.

Source OSC

The source OSC (source oscillator) is a phase locked oscillator. The output signal is phase locked to the 40 kHz frequency of the divider output. The oscillator generates the 85.68 MHz signal. The signal divided by the 1/4 divider. The resulting 21.42 MHz signal is supplied to the ALC circuit.

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The oscillator contains an 85.68 MHz VCO, a phase detector, a 1/2 divider, a mixer, and a 1/71 divider. See Figure 11-6. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 2 and mixed with the 40 MHz reference frequency in the mixer. The mixer then produces a shifted frequency ($\mathbf{F_{vco}}/2 - 40$ MHz). The mixer output is divided by 71 and then compared with the 40 kHz reference signal in the phase detector. Phase locking imposes the condition of 40 kHz = ($\mathbf{F_{vco}}/2 - 40$ MHz)/71. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 85.68 MHz (= (40 kHz x 71 + 40 MHz) x 2).

ALC

The ALC controls the level of the 21.42 MHz CW signal from the source OSC. The signal is routed to the RF OUT connector through the A3A2 2nd LO, the A3A3 source, and the A7 Output Attenuator. The A3A3 output level is detected and loops back to the ALC for automatic leveling control.

The ALC consists of a level DAC, an error detector, an integrator, a Gain ALC, and a level vernier. See Figure 11-6. In addition, a switch that follows the level vernier is used to turn the RF OUT signal on and off.

The loop-backed A3A3 output level is compared with the level DAC output in the error detector. The error detector produces a DC voltage proportional to the error between the A3A3 output level and the level DAC output. The error detector output controls the 21.42 MHz signal level through the integrator and the level vernier. ALC loop locking imposes the condition of Level DAC Output = A3A3 Output Level. Therefore, the A3A3 output level is determined by the level DAC setting.

The A3A3 output level for each level DAC setting is predefined by performing the *RF OUT Level Correction Constants*. The predefined data is stored in the EEPROM of the A1 CPU.

The Gain ALC is a variable amplifier from 0 dB to 6 dB. It is used to shorten the time required for the ALC loop to be locked after the frequency is changed. It does this by compensating the frequency response of the source amplifier's gain in the A3A3 source. Therefore, the Gain ALC setting depends on the RF signal frequency. The Gain ALC settings are predefined over the entire frequency range by performing the *RF OUT Level Correction Constants*. The predefined setting data is stored in the EEPROM of the A1 CPU.

A3A2 2nd LO

The A3A2 2nd LO generates the second local oscillator signal (a 2.08 GHz CW signal) and converts the 21.42 MHz signal from the A3A1 ALC to a 2.05858 GHz IF signal by mixing the 21.42 MHz and the second local oscillator signal.

The 2.05858 GHz IF signal is supplied to the A3A3 source and then converter to a swept RF signal. The second local oscillator signal is supplied to the A4A2 receiver RF.

The A3A1 ALC consists of the following circuits:

- 2nd LO
- Source First Mixer

2nd Local OSC Circuit

The 2nd Local oscillator circuit is a phase locked oscillator. The output signal is phase locked to the 520 MHz frequency from the A5 synthesizer. The oscillator generates a 2.08 GHz signal. The signal is supplied to the source first mixer and the A4A1 receiver RF.

The oscillator contains a 1.04 GHz VCO, a phase detector, and a 1/2 divider. See Figure 11-6. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 2 and then compared with the 520 MHz reference signal in the phase detector. Phase locking imposes the condition of 520 MHz = $\mathbf{F_{vco}}/2$. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 1.04 GHz (= 520 MHz x 2). Then the signal frequency is converted to 2.08 GHz by the doubler.

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The 520 MHz reference signal contains 40 MHz harmonics because it is generated by multiplying the 40 MHz reference signal in the A5 synthesizer. The *Second Local PLL Adjustment* adjusts the 2nd LO to lock to the 520 MHz harmonic, rather than the neighboring harmonics (480 MHz or 560 MHz).

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of the limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

Source First Mixer

The 21.42 MHz CW signal from the A3A1 ALC is mixed with the 2.08 GHz second local oscillator signal through the first source mixer. Then the signal is converted to a 2.05858 GHz CW signal through the BPF (band pass filter). The 2.05858 GHz signal is supplied to the A3A3 source.

A3A3 Source

The A3A3 source generates a stable and accurate RF signal. This signal is a CW or swept signal between 100 kHz to 1.8 GHz, with a power level from −10 dBm to +20 dBm. The RF signal is supplied to the A7 output attenuator. The A3A3 source consists of the following circuits (see Figure 11-6):

- Source Second Mixer
- Source Amplifier
- Level Detector

The 2.05858 GHz IF signal from the A3A2 2nd LO is applied to the source second mixer. It is then converted to the CW or swept RF signal (100 kHz to 1.8 GHz) by mixing with the CW or swept 1st local oscillator signal (2.05859 GHz to 3.85858 GHz) from the A4A1 1st LO. The RF signal is amplified with a constant gain through the source amplifier. It is then supplied to the A7 output attenuator through the level detector. The level detector loops the RF signal level back to the A3A1 ALC.

A7 Output Attenuator

The A7 output attenuator is a 10 dB step attenuator from 0 dB to 60 dB. A7 consists of three segments (10 dB, 20 dB, and 30 dB). Attenuation from 0 dB to 60 dB is obtained by combining one (or more) of the three segments. Each segment is activated by the TTL signals from the A2 post-regulator. The TTL signals are controlled by the A1 CPU.

The RF signal from the A3A3 source is routed to the front-panel RF OUT connector through A7. A7 is used to produce the RF OUT power range of −60 dBm to 20 dBm using the A3A3 RF signal of −10 dBm to +20 dBm.

Table 11-2 shows the relationship between the RF OUT power setting, the A3A3 output level, and the A7 setting in the non-power sweep (frequency sweep) measurement. The RF OUT power from −60 dBm to +10 dBm is obtained by attenuating the A3A3 RF signal of 0 dBm to +10 dBm. This reduces errors in the non power sweep linearity performance due to the ALC loop's linearity error.

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Table 11-2.
RF OUT Power, A3A3 Output, and A7 Attenuator (Non-Power Sweep)

RF OUT Power	A3A3 Output	A7 Attenuation
0 dBm < Setting ≤ +20 dBm	0 dBm < Setting ≤ +20 dBm	0 dB
−10 dBm < Power ≤ 0 dBm	0 dBm < Setting ≤ +20 dBm	10 dB
−20 dBm < Power ≤ −10 dBm	0 dBm < Setting ≤ +10 dBm	20 dB
−30 dBm < Power ≤ −20 dBm	0 dBm < Setting ≤ +10 dBm	30 dB
−40 dBm < Power ≤ −30 dBm	0 dBm < Setting ≤ +10 dBm	40 dB
−50 dBm < Power ≤ −40 dBm	0 dBm < Setting ≤ +10 dBm	50 dB
−60 dBm ≤ Power ≤ −50 dBm	0 dBm ≤ Setting ≤ +10 dBm	60 dB

When making a power sweep measurement, the A7 output attenuator cannot be changed during a power sweep. Therefore, the applicable power sweep range is the maximum 30 dB that is the A3A3's RF signal power range. The A7 setting is determined by the stop power setting in the power sweep measurement. Also, the allowable start power depends on the stop power setting. Table 11-3 shows the relationship among the stop power setting, the A7 setting, and the allowable start power in the power sweep measurement.

Table 11-3.
Stop Power, A7 Attenuation, and Allowable Start Power (Power Sweep)

Stop Power	A7 Attenuator	Allowable Start Power
+10 dB < Power ≤ +20 dBm	0 dB	−10 dBm ≤ Power < Stop Power
0 dB < Power ≤ +10 dBm	10 dB	−20 dBm ≤ Power < Stop Power
−10 dB < Power ≤ 0 dBm	20 dB	−30 dBm ≤ Power < Stop Power
−20 dB < Power ≤ −10 dBm	30 dB	−40 dBm ≤ Power < Stop Power
−30 dB < Power ≤ −20 dBm	40 dB	−50 dBm ≤ Power < Stop Power
−40 dB < Power ≤ −30 dBm	50 dB	−60 dBm ≤ Power < Stop Power
−60 dB < Power ≤ −40 dBm	60 dB	−60 dBm ≤ Power < Stop Power

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RECEIVER THEORY

The RF input signals to be tested can be connected to the R, A, B, or S inputs. The input signals are multiplexed at the front end of the receiver and one of signals is routed to the following receiver circuit. The signal is converted to the 1st IF (intermediate frequency), then to 2nd IF, and finally to the 3rd IF. The 3rd IF is converted to a digital signal using A/D converter.

Figure 11-7 shows the simplified block diagram of the receiver functional group. The receiver group consists of the following assemblies:

- A8 Input Attenuator
- A9 Input Multiplexer
- A4A2 Receiver RF
- A6 Receiver IF

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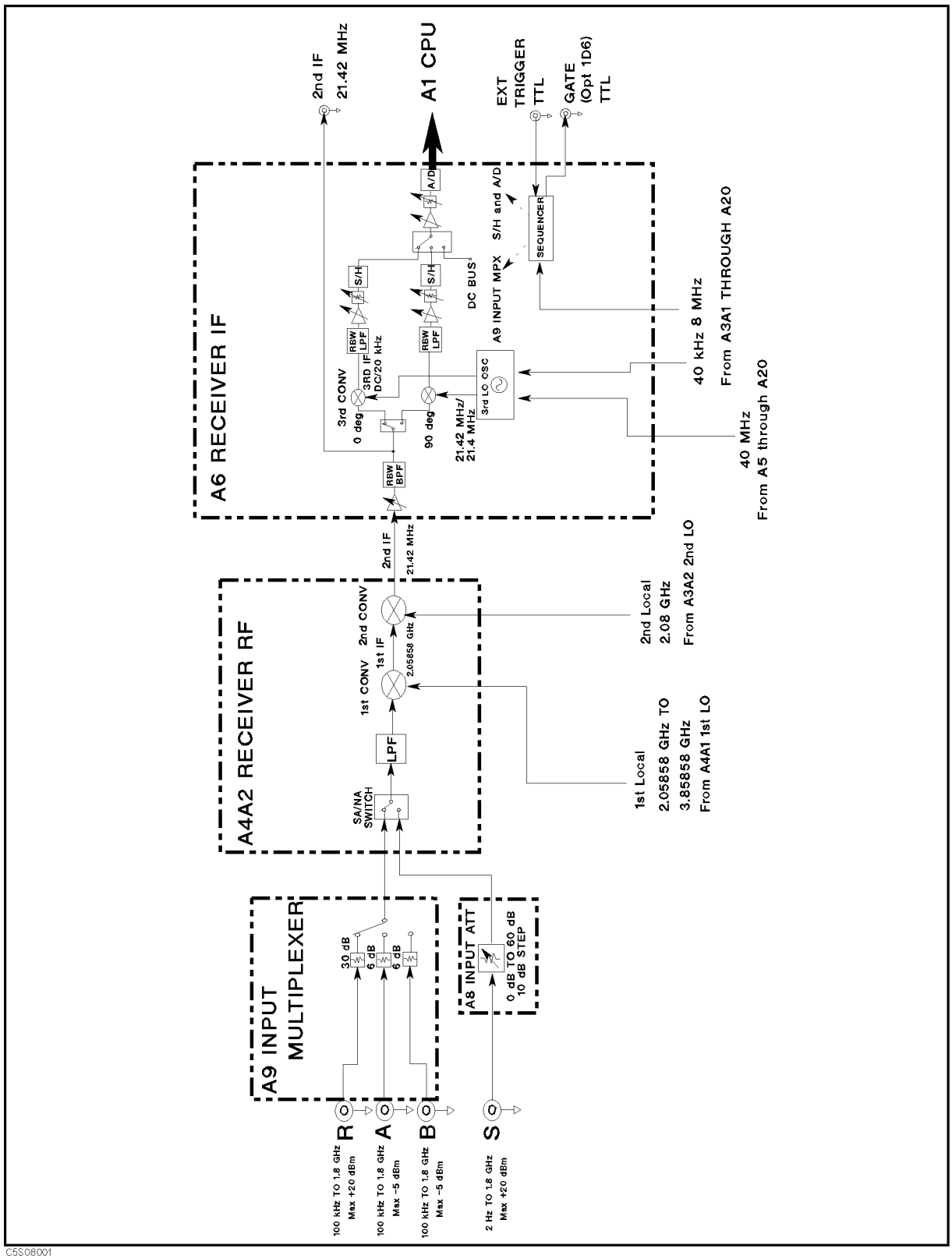


Figure 11-7. Receiver Simplified Block Diagram

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A8 Input Attenuator

The A8 input attenuator is a 10 dB step attenuator (0 dB to 60 dB) with a maximum input level of +30 dBm. It is used only in the spectrum analyzer mode.

The RF input signal from the S input is routed to the A4A2 Receiver RF through A8. A8 is used to control the input signal level to the fist mixer in A4A2. The A8 setting can be controlled from the front panel by changing the attenuation setting directly or by changing the reference level in the auto attenuation mode.

A8 consists of three segments (10 dB, 20 dB, and 30 dB). Attenuation from 0 dB to 60 dB is obtained by combining one (or more) of the three segments. Each segment is activated by a TTL signal from the A2 post-regulator. The TTL signals are controlled by the A1 CPU.

A9 Input Multiplexer

The A9 multiplexer multiplexes the RF signals from inputs R, A, and B to the A4A2 receiver RF. A9 is primarily used in the network analyzer mode. However, it can be used in the spectrum analyzer mode when the spectrum monitoring function of the R, A, or B input is used.

A9 consists of three fixed attenuators and a multiplexer. See Figure 11-7. The R input signal is attenuated by 30 dB and then routed to A4A2 through the multiplexer. The A and B input signals are attenuated by 6 dB and then routed to A4A2 through the multiplexer.

A9 has very low signal leakage between any two of the three inputs. The input crosstalk performance of the analyzer is mainly determined by A9. In addition, the input impedance performance for the R, A, and B inputs is determined by A9 because each input connector is in A9.

A4A2 Receiver RF

The A4A2 receiver RF converts the RF input signal from A8 or A9 to the 21.42 MHz 2nd IF. The 2nd IF is routed to the A6 receiver IF.

The A4A2 receiver RF consists of the following circuits (See Figure 11-7):

- NA/SA Switch
- 1st Converter
- 2nd Converter
- Auto Zero Switch

The RF signals from A8 or A9 go to the NA/SA switch. In the switch, one of the signals is routed to the 1st converter and then to the second converter.

In the first converter, the RF signal (2 Hz to 1.8 GHz in the spectrum analyzer mode and 100 kHz to 1.8 GHz in the network analyzer mode) is mixed with the 1st local oscillator signal (2.058580002 GHz to 3.85858 GHz in the spectrum analyzer mode and 2.05868 GHz to 3.85858 GHz in the network analyzer mode) from A4A1 and then converted to the 2.05858 GHz 1st IF through the band pass and low pass filters.

In the second converter, the 1st IF is mixed with the 2.08 GHz second local oscillator signal from A3A2. This converts it to the 21.42 MHz second IF through the low pass filters.

The 21.42 MHz second IF is routed to A6 through the auto-zero switch. The auto-zero switch is used for an auto-zero detection. The analyzer performs auto-zero detection automatically to measure the offset error on the signal path in the A6 receiver IF. It then compensates the measured value with the detected offset error. In auto-zero detection, the input signal to the A6 receiver IF is grounded in the auto-zero switch.

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A6 Receiver IF

The A6 Receiver IF converts the 21.42 MHz 2nd IF from A4A2 to the final 3rd IF. The 3rd IF is then converted to a digital value in the A/D converter. The digital signal is routed to the DSP on the A1 CPU.

The A6 receiver IF consists of the following circuits (See Figure 11-7):

- IF BPFs and IF LPFs
- 3rd Converter (third converter) and 3rd LO (third local oscillator)
- Sample/Hold, A/D Converter, and Sequencer
- Gains W, X, Y, Z and Ranges F and R
- Sequence

There are two signal paths (0° and 90°) between the IF BPFs and the A/D converter. These paths are the same and are used for a DC sampling mode that is described below. The 3rd local oscillator input signals to the respective 3rd converters are phase shifted by 90° from each other.

The A6 Receiver IF has two operation modes, AC sampling mode and DC sampling mode. The sampling mode is automatically selected according to the analyzer mode and IFBW/RBW setting. See the Table 11-4.

In the AC sampling mode, the 2nd IF is converted to 20 kHz in the 3rd converter. Only the 0° path signal is converted to a digital value and used for data processing.

In the DC sampling mode, the 2nd IF is converted to DC in the third converter. The 0° and 90° DC 3rd IF are converted to digital values ($\mathbf{e}_{0°}$ and $\mathbf{e}_{90°}$). Then the spectrum amplitude is calculated by taking the square root of $\mathbf{e}_{0°}{}^2 + \mathbf{e}_{90°}{}^2$. This mode is used to take advantage of the fast spectrum measurement with RBWs $\geq$ 10 kHz.

IF BPFs and LPFs

The IF BPFs consist of three bandpass filter with a enter frequency 21.42 MHz. The pass bandwidths are 10 kHz, 1 MHz, and 3 MHz, respectively. The 10 kHz BPF is a crystal BPF.

The IF LPFs consist of a through and four LPFs. The LPFs' cutoff frequencies are 5 kHz, 15 kHz, 50 kHz, and 150 kHz, respectively.

These BPFs and LPFs are used to shape the bandwidth of the IF signals going to the A/D converter. See Table 11-4 for the selection requirements.

Table 11-4. Measurement Setting, Used Filter, and Sampling Mode

Analyzer Mode	IF BW/RBW	Used IF BPF	Used IF LPF	Sampling Mode
Network Analyzer	10 kHz, 40 kHz	1 MHz	50 kHz	AC Sampling
	10 Hz to 3 kHz	10 kHz (X'tal)	50 kHz	AC Sampling
Spectrum Analyzer	3 MHz	3 MHz	Through	DC Sampling
	1 MHz	1 MHz	Through	DC Sampling
	300 kHz	1 MHz	150 kHz	DC Sampling
	100 kHz	1 MHz	50 kHz	DC Sampling
	30 kHz	1 MHz	15 kHz	DC Sampling
	10 kHz	1 MHz	5 kHz	DC Sampling
	1 Hz to 3 kHz	10 kHz (X'tal)	50 kHz	AC Sampling

In the spectrum measurement, the 3 MHz and 1 MHz RBWs are shaped by the IF BPFs at the 2nd IF stage (before the 3rd converter) and the IF LPFs are by-passed. This is done so that

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the shape is not disturbed. Because of the inphase-quadrature detection characteristics, the LPF cutoff frequencies used for RBWs 10 kHz to 300 kHz are half of the RBWs respectively. RBWs $\leq$ 3 kHz are realized by the FFT technique. For RBWs $\leq$ 3 kHz using the FFT, the 10 kHz crystal BPF in the 2nd IF stage and the 50 kHz LPF are selected to reject the unwanted image/aliasing signals.

3rd Converter and 3rd LO

In the 3rd converter, the 21.42 MHz 2nd IF is converted to the final 20 kHz or DC 3rd IF. The 3rd LO provides the third local oscillator signal (21.4 MHz/21.42 MHz) to the third converter.

In the AC sampling mode, the 3rd LO provides the 21.4 MHz local oscillator signal to the 3rd converter. In the third converter, the 21.42 MHz 2nd IF is mixed with the 21.4 MHz 3rd local oscillator signal and then converted to 20 kHz.

In the DC sampling mode, the 3rd LO provides the 21.42 MHz local oscillator signal to the 3rd converter. In the third converter, the 21.42 MHz 2nd IF is mixed with the 21.42 MHz 3rd local oscillator signal and then converted to DC.

An unlock detector monitors the control voltage to the VCO within the 3rd LO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. Then the A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

Sample/Hold, A/D Converter, and Sequencer

The 3rd IF is sampled and held in the Sample/Hold on the 0° path and the 90° path. One of the 0° and 90° hold signals is connected to the A/D converter through the A/D multiplexer and then converted to a digital value.

The A/D multiplexer is a 3-channel multiplexer that multiplexes the 0° path, the 90° path, and the DC bus to the A/D converter. The DC bus is a single multiplexed line that networks 26 nodes within the analyzer. When the DC bus is connected to the A/D converter, the A/D converter is used to measure the voltage at a selected node within the analyzer. For more information about the DC bus measurement, see the *Service Key Menus* chapter.

The analyzer uses a 16 bit A/D converter with 100 ks/sec. It is used at the rate of 80 ks/sec. The sequencer consists of four GALs (gate array logic) ICs that are used as follows:

- Timing generator for the sample/hold the A/D converter.
- Timing generator/Gate shaper for the real time gated analysis.
- Timer driver/Input multiplexer driver/Frequency increment driver (controlling A5 FRAC N OSC).
- Decoder for control signal from the A1 CPU.

Gains W, X, Y, and Z and Ranges F and R

The gains W (0 dB/10 dB), X (0 dB/18 dB), Y (0 dB/6 dB/12 dB/18 dB), and Z (0 dB/2 dB/4 dB/18 dB) are variable amplifiers, respectively. The ranges F and R are ranging amplifiers that consist of a 0 dB/18 dB switchable attenuator and a 18 dB amplifier, respectively.

These amplifiers are used to optimize the IF gain (total gain through the 1st/2nd/3rd IF signal path) in order to use the A/D converter's widest possible dynamic range. The analyzer automatically controls these gains according to the maximum first mixer level that is determined by the reference level and input attenuator settings. See Table 11-5. Therefore, when an RF signal with a full scale level is applied to an input on the front panel, the 3rd IF input level applied to the A/D converter corresponds to the full scale of the A/D converter.

The gain value at each IF gain setting is measured relative to the reference setting shown in Table 11-5 is obtained by performing the *IF Gain Correction Constants*. These values are stored in the EEPROM of the A1 CPU.

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Table 11-5. Gains and Ranges Settings

Analyzer Mode	IF BW/ RBW	1st Mixer Level[1]	Gain W	Gain X	Gain Y	Gain Z	Range F	Range R
Network Analyzer	10 Hz to 40 kHz	Measured[1]	0 dB	18 dB	0 dB	18 dB	Auto[2]	Auto[2]
Spectrum Analyzer	1 MHz, 3 MHz,	−10 dBm	0 dB	0 dB	0 dB	0 dB	0 dB[3]	0 dB
	and RBWs ≤ 3 kHz	−12 dBm	0 dB	0 dB	0 dB	2 dB	0 dB	0 dB
		−14 dBm	0 dB	0 dB	0 dB	4 dB	0 dB	0 dB
		−16 dBm	0 dB	0 dB	6 dB	0 dB	0 dB	0 dB
		−18 dBm	0 dB	0 dB	6 dB	2 dB	0 dB	0 dB
		−20 dBm	0 dB	0 dB	6 dB	4 dB	0 dB	0 dB
		−22 dBm	0 dB	0 dB	12 dB	0 dB	0 dB	0 dB
		−24 dBm	0 dB	0 dB	12 dB	2 dB	0 dB	0 dB
		−26 dBm	0 dB	0 dB	12 dB	4 dB	0 dB	0 dB
		−28 dBm	0 dB	18 dB	0 dB	0 dB	0 dB	0 dB
		−30 dBm	0 dB	18 dB	0 dB	2 dB	0 dB	0 dB
		−32 dBm	0 dB	18 dB	0 dB	4 dB	0 dB	0 dB
		−34 dBm	0 dB	18 dB	6 dB	0 dB	0 dB	0 dB
		−36 dBm	0 dB	18 dB	6 dB	2 dB	0 dB	0 dB
		−38 dBm	0 dB	18 dB	6 dB	4 dB	0 dB	0 dB
		−40 dBm	10 dB	18 dB	0 dB	2 dB	0 dB	0 dB
		−42 dBm	10 dB	18 dB	0 dB	4 dB	0 dB	0 dB
		−44 dBm	10 dB	18 dB	6 dB	0 dB	0 dB	0 dB
		−46 dBm	10 dB	18 dB	6 dB	2 dB	0 dB	0 dB
		−48 dBm	10 dB	18 dB	6 dB	4 dB	0 dB	0 dB
		−50 dBm	10 dB	18 dB	12 dB	0 dB	0 dB	0 dB
Spectrum Analyzer	10 kHz to 300 kHz	−10 dBm[4]	0 dB	18 dB	0 dB	0 dB	Auto[2]	0 dB
		−12 dBm	0 dB	18 dB	0 dB	2 dB	Auto	0 dB
		−14 dBm	0 dB	18 dB	0 dB	4 dB	Auto	0 dB
		−16 dBm	0 dB	18 dB	6 dB	0 dB	Auto	0 dB
		−18 dBm	0 dB	18 dB	6 dB	2 dB	Auto	0 dB
		−20 dBm	0 dB	18 dB	6 dB	4 dB	Auto	0 dB
		−22 dBm	0 dB	18 dB	12 dB	0 dB	Auto	0 dB
		−24 dBm	0 dB	18 dB	12 dB	2 dB	Auto	0 dB
		−26 dBm	0 dB	18 dB	12 dB	4 dB	Auto	0 dB
		−28 dBm	0 dB	18 dB	18 dB	0 dB	Auto	0 dB
		−30 dBm	0 dB	18 dB	18 dB	2 dB	Auto	0 dB
		−32 dBm	0 dB	18 dB	18 dB	4 dB	Auto	0 dB
		−34 dBm	0 dB	18 dB	6 dB	18 dB	Auto	0 dB
		−36 dBm	0 dB	18 dB	6 dB	18 dB	Auto	0 dB
		−38 dBm	0 dB	18 dB	6 dB	18 dB	Auto	0 dB
		−40 dBm	10 dB	18 dB	18 dB	2 dB	Auto	0 dB
		−42 dBm	10 dB	18 dB	18 dB	4 dB	Auto	0 dB
		−44 dBm	10 dB	18 dB	6 dB	18 dB	Auto	0 dB
		−46 dBm	10 dB	18 dB	6 dB	18 dB	Auto	0 dB
		−48 dBm	10 dB	18 dB	6 dB	18 dB	Auto	0 dB
		−50 dBm	10 dB	18 dB	12 dB	18 dB	Auto	0 dB

1 = Reference Level [dBm] − Input Attenuator [dB] in the spectrum analyzer mode. In the network analyzer mode, the analyzer measures the input signal level at each measurement point.

2 The analyzer optimizes the setting according to the signal level at each measurement point.

3 Not used for RBW 3 MHz and 1 MHz.

4 Reference setting for the IF gain correction constants.

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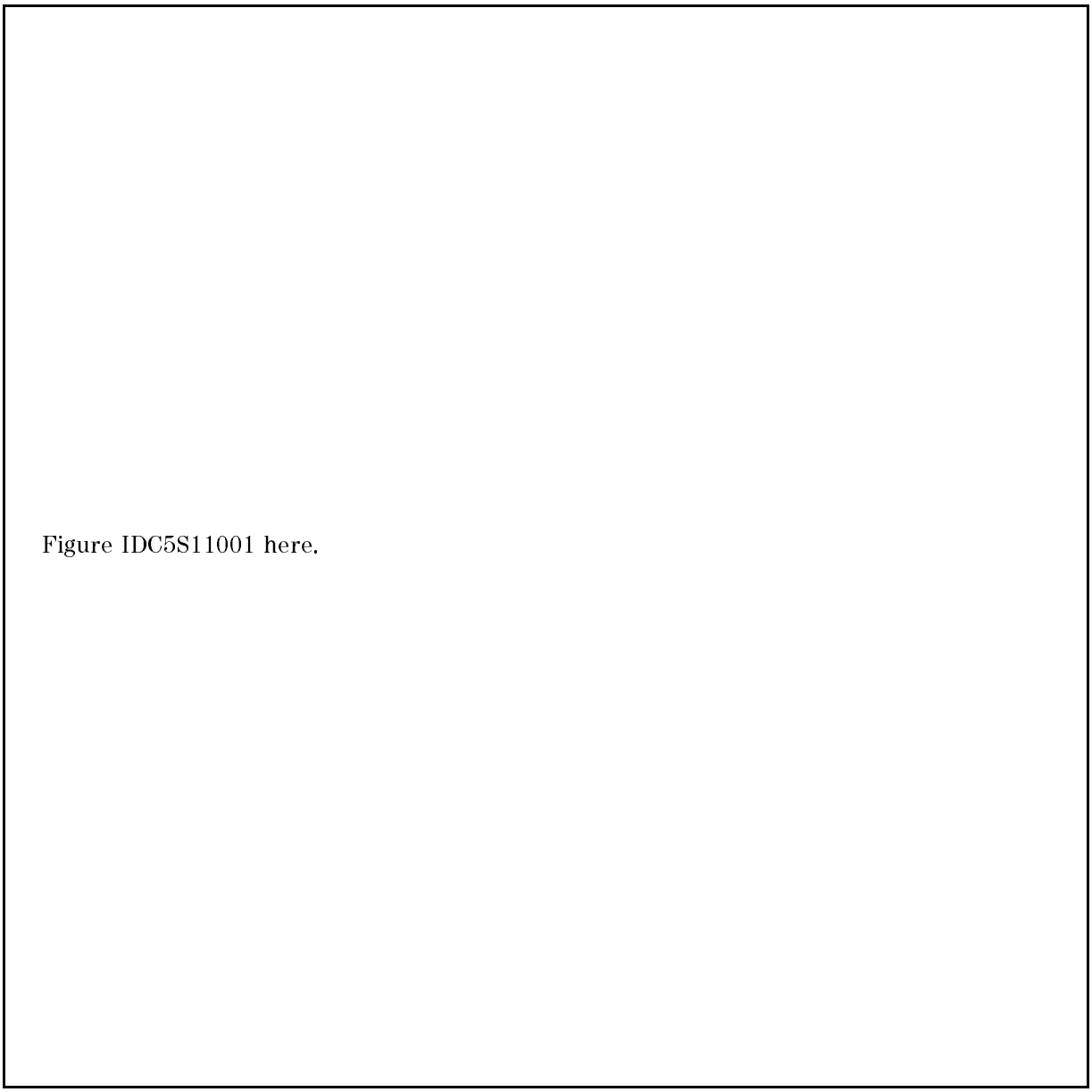


Figure 11-8. 4396B Source Group Block Diagram

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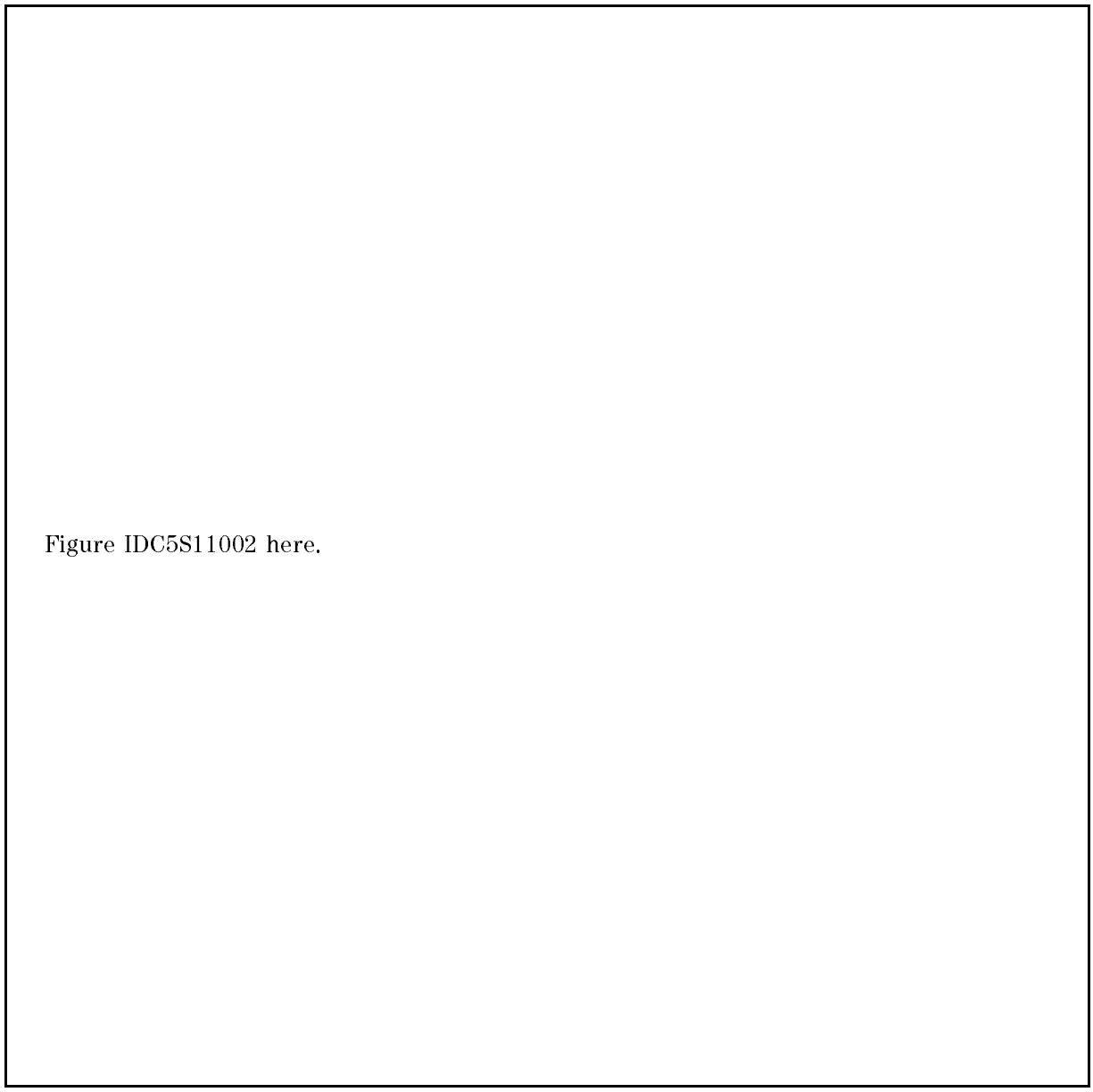


Figure 11-9. 4396B Receiver Group Block Diagram

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12

Replaceable Parts

Introduction

This chapter lists the analyzer's replaceable parts. How to order the parts is also described.

Ordering Information

To order a part listed in the replaceable parts table, quote the Agilent Technologies part number (with a check digit), indicate the quantity required, and address the order to the nearest Agilent Technologies office. The check digit will ensure accurate and timely processing of the order.

To order a part not listed in the replaceable parts table, include the instrument model number, the description and function of the part, and the quantity of parts required. Address the order to the nearest Agilent Technologies office.

Direct Mail Order System

Within the USA, Agilent Technologies can supply parts through a direct mail order system. Advantages of using this system are:

1. Direct ordering and shipment from the Agilent Technologies Parts Center in Mountain View, California.
2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local Agilent Technologies office when the orders require billing and invoicing).
3. Prepaid transportation (there is a small handling charge for each order).
4. No invoices.

To provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Agilent Technologies office, addresses and phone numbers are located at the back of this manual.

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Exchange Assemblies

Under the rebuilt-exchange assembly program, certain factory-repaired and tested assemblies are available on a trade-in basis. These assemblies are offered at lower cost than a new assembly while meeting all of the factory specifications required of a new assembly.

Replaceable Parts List

Replaceable parts tables list the following information for each part.

1 Agilent Technologies part number.
2 Part number check digit (CD).
3 Part quantity as shown in the corresponding figure. There may or may not be more of the same part located elsewhere in the instrument.
4 Part description, using abbreviations (see Table 12-2).
5 A typical manufacturer of the part in a five-digit code (see Table 12-1).
6 The manufacturer's part number.

Table 12-1. Manufacturers Code List

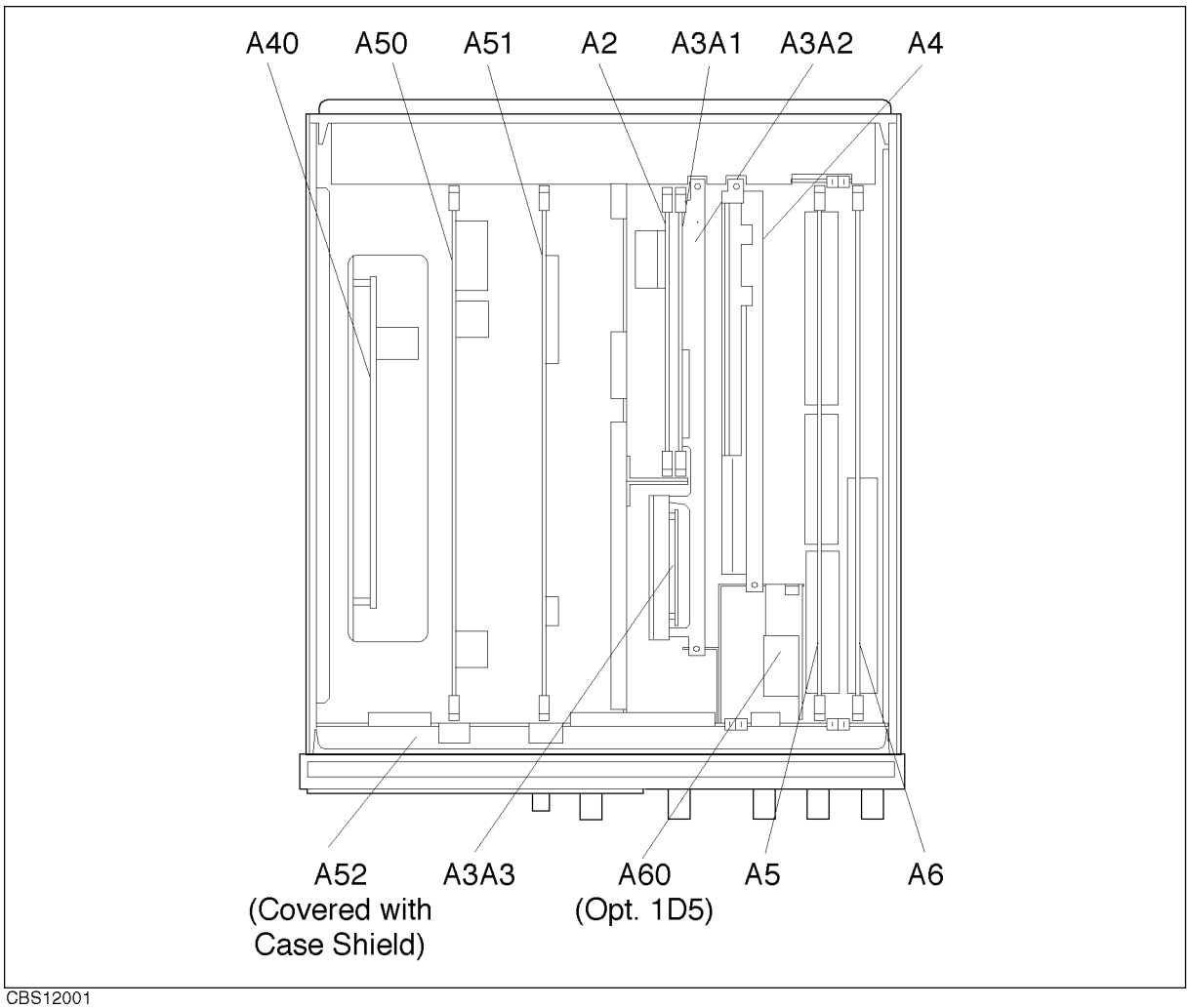
Mfr #	Name	Location	Zipcode
00779	AMP INC	HARRISBURG PA US	17111
06369	HIROSE ELECTRIC CO	JP	
06691	HOUSE OF METRICS LTD	SPRING VALLEY NY US	10977
08747	KITAGAWA KOGYO	TOKYO JP	
09635	TAJIMI MUSEN	TOKYO JP	
10572	XICOR INC	MILPITAS CA	
12085	SCHLEGEL CORP	ROCHESTER NY US	14692
13160	TEAC OF AMERICA INC	MONTEBELLO CA US	90640
28480	AGILENT TECHNOLOGIES CO CORPORATE HQ	PALO ALTO CA US	94304
28520	HEYCO MOLDED PRODUCTS	KENTWORTH NJ US	07033
73734	FEDERAL SCREW PRODUCTS CO	CHICAGO IL US	60618
76381	3M CO	ST PAUL MN US	55144
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN IL US	60126

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Table 12-2. List of Abbreviations

A	: amperes	N/C	: normally closed
A.F.C.	: automatic frequency control	NE	: neon
AMPL	: amplifier	NI PL	: nickel plate
B.F.O	: beat frequency oscillator	N/O	: normally open
BE CU	: beryllium copper	NPO	: negative positive zero (zero temperature coefficient)
BH	: binder head	NPN	: negative-positive-negative
BP	: bandpass	NRFR	: not recommended for field replacement
BRS	: brass	NSR	: not separately replaceable
BWO	: backward wave oscillator	OBD	: order by description
CCW	: counter-clockwise	OH	: oval head
CER	: ceramic	OX	: oxide
CMO	: cabinet mount only	P	: peak
COEF	: coefficient	PC	: printed circuit
COM	: common	p	: pico
COMP	: composition	PH BRZ	: phosphor bronze
COMPL	: complete	PHL	: Philips
CONN	: connector	PIV	: peak inverse voltage
CP	: cadmium plate	PNP	: positive-negative-positive
CRT	: cathode-ray tube	P/O	: part of
CW	: clockwise	POLY	: polystyrene
DE PC	: deposited carbon	PORC	: porcelain
DR	: drive	POS	: position(s)
ELECT	: electrolytic	POT	: potentiometer
ENCAP	: encapsulated	PP	: peak to peak
EXT	: external	PT	: point
F	: farads	PWV	: peak working voltage
f	: femto	RECT	: rectifier
FH	: flat head	RF	: radio frequency
FIL H	: fillister head	RH	: round head or right hand
FXD	: fixed	RMO	: rack mount only
G	: giga	RMS	: root-mean square
GE	: germanium	RWV	: reverse working voltage
GL	: glass	S-B	: slow-blow
GRD	: ground(ed)	SCR	: screw
H	: henries	SE	: selenium
HEX	: hexagonal	SECT	: section(s)
HG	: mercury	SEMICON	: semiconductor
HR	: hour(s)	SI	: silicon
Hz	: hertz	SIL	: silver
IF	: intermediate freq.	SL	: slide
IMPG	: impregnated	SPG	: spring
INCD	: incandescent	SPL	: special
INCL	: include(s)	SST	: stainless steel
INS	: insulation(ed)	SR	: split ring
INT	: internal	STL	: steel
k	: kilo	TA	: tantalum
LH	: left hand	TD	: time delay
LIN	: linear taper	TGL	: toggle
LK WASH	: lock washer	THD	: thread
LOG	: logarithmic taper	TI	: titanium
LPF	: low pass filter	TOL	: tolerance
m	: milli	TRIM	: trimmer
M	: meg	TWT	: traveling wave tube
MET FLM	: metal film	μ	: micro
MET OX	: metallic oxide	VAR	: variable
MFR	: manufacturer	VDCW	: dc working volts
MINAT	: miniature	W/	: with
MOM	: momentary	W	: watts
MTG	: mounting	WIV	: working inverse voltage
MY	: “mylar”	WW	: wirewound
n	: nano	W/O	: without

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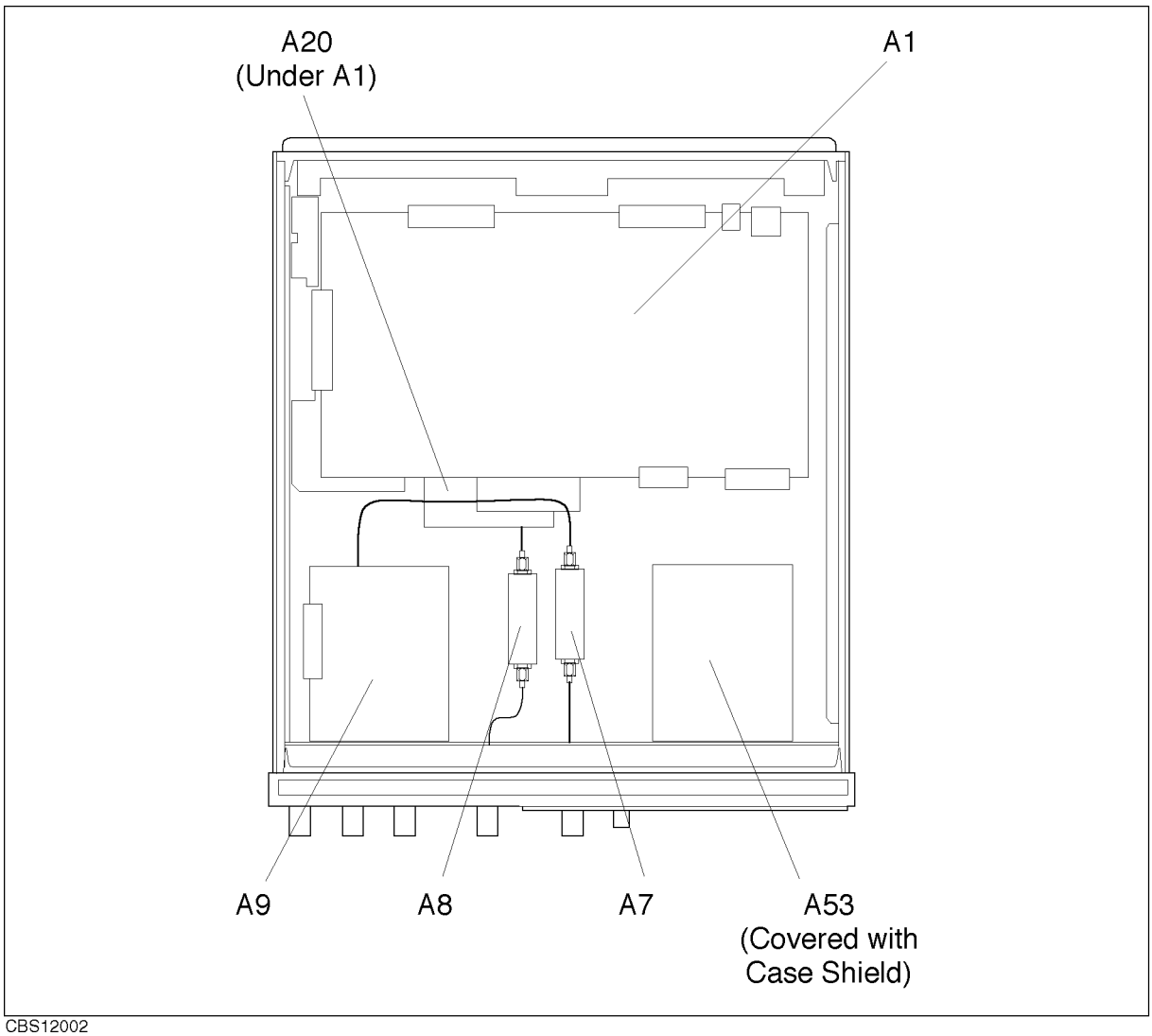
Figure 12-1. Top View (Major Assemblies)

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Table 12-3. Top View (Major Assemblies)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A2	04396-66522	0	1	Post Regulator	28480	04396-66522
A3A1	04396-66503	7	1	ALC	28480	04396-66503
A3A2	04396-66513	9	1	Second LO	28480	04396-66513
A3A2	04396-69513			Second LO (rebuilt-exchange)	28480	04396-69513
A3A3	5086-7620	1	1	Source	28480	5086-7620
A3A3	5086-6620			Source (rebuilt-exchange)	28480	5086-6620
A4	04396-61004	3	1	First LO/Receiver RF	28480	04396-61004
A4	04396-69004			First LO/Receiver RF (rebuilt-exchange)	28480	04396-69004
A5	04396-66505	9	1	Synthesizer	28480	04396-66505
A5	04396-69505			Synthesizer (rebuilt-exchange)	28480	04396-69505
A6	04396-66506	0	1	Receiver IF	28480	04396-66506
A6	04396-69506			Receiver IF (rebuilt-exchange)	28480	04396-69506
A40	0950-3246	7	1	Preregulator	28480	0950-3246
A50	E4970-66550	7	1	DC-DC Converter	28480	E4970-66550
A51	E4970-66552	9	1	GSP	28480	E4970-66552
A60	04396-61060	1	1	Freq Ref (opt. 1D5)	28480	04396-61060

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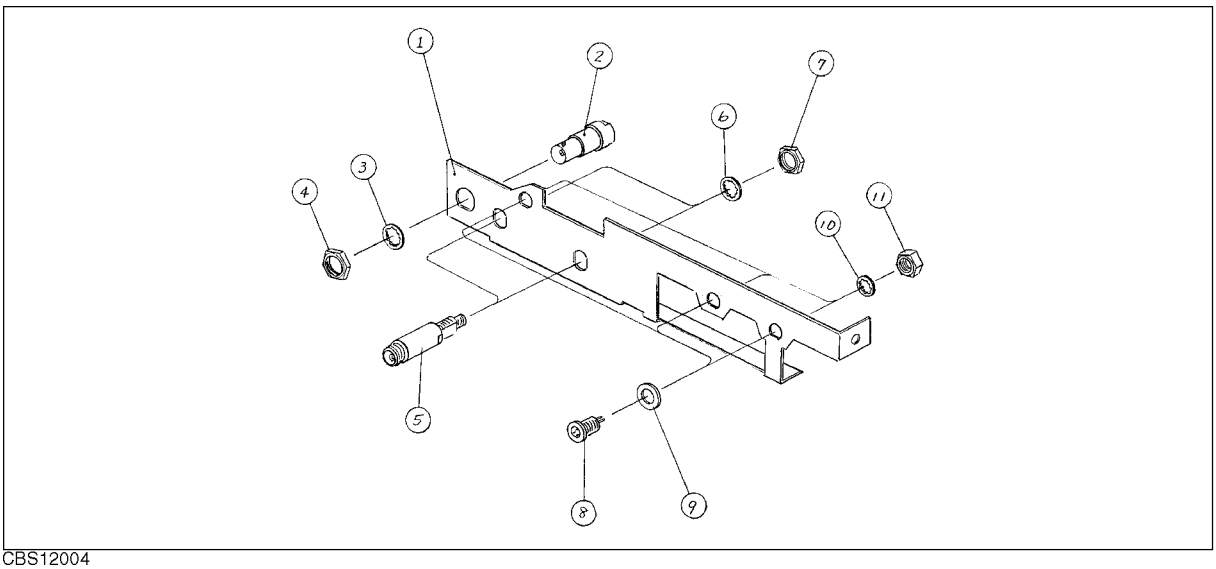
CBS12002

Figure 12-2. Bottom View (Major Assemblies)

Table 12-4. Bottom View (Major Assemblies)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A1	E4970-66501	8	1	CPU ASSY	28480	E4970-66501
A7	0955-0664	7	1	Input ATT	28480	0955-0664
A8	0955-0664		1	Output ATT	28480	0955-0664
A9	04396-66509	3	1	Input Multiplexer	28480	04396-66509
A9	04396-69509			Input Multiplexer (rebuilt-exchange)	28480	04396-69509
A20	04396-66520	8	1	Motherboard	28480	04396-66520
A53	0950-3208	1	1	FDD	13160	0950-3208

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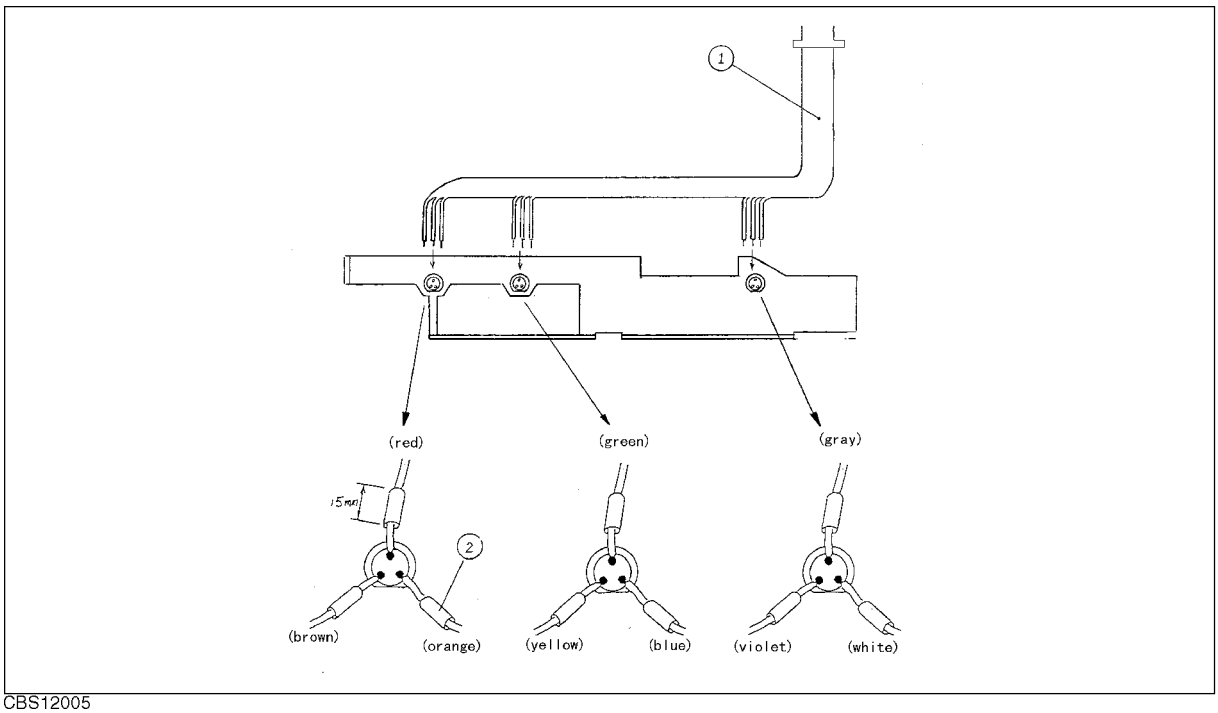
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Figure 12-3. Angle Assembly Parts 1/3

Table 12-5. Angle Assembly Parts 1/3

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-01201	6	1	BRACKET	28480	04396-01201
2	1250-0252	6	1	CONN-RF BNC	28480	1250-0252
3	2190-0102	8	1	WSHR-LK INTL T	28480	2190-0102
4	2950-0035	8	1	NUT-HEX-DBL-CHAM	28480	2950-0035
5	1250-2312	3	2	ADPT-RF N-SMA	28480	1250-2312
6	2190-0104	0	2	WSHR-LK INTL T	28480	2190-0104
7	2950-0132	6	2	NUT-HEX-DUB-CHAM	28480	2950-0132
8	1252-4294	8	3	CONN CIR 3M GRY	28480	1252-4294
9	04396-25003	6	3	SPACER	28480	04396-25003
10	2190-0016	3	3	WSHR-LK INTL T	28480	2190-0016
11	2950-0144	0	3	NUT-HEX-DBL-CHAM	28480	2950-0144

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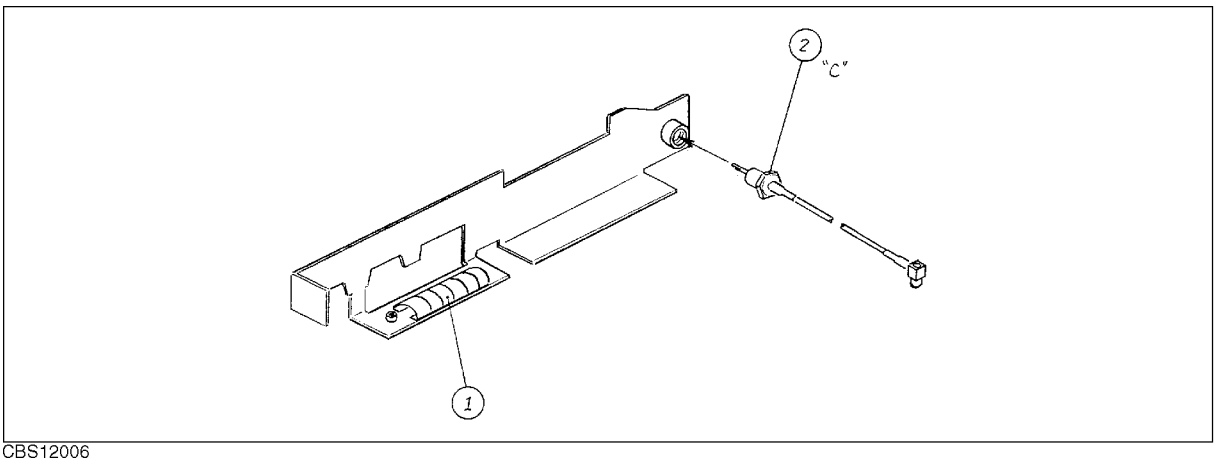
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Figure 12-4. Angle Assembly Parts 2/3

Table 12-6. Angle Assembly Parts 2/3

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61681	2	1	WIRE ASSY	28480	04396-61681
2	0890-1480	9	13	TUB-HEAT SHRK	28480	0890-1480

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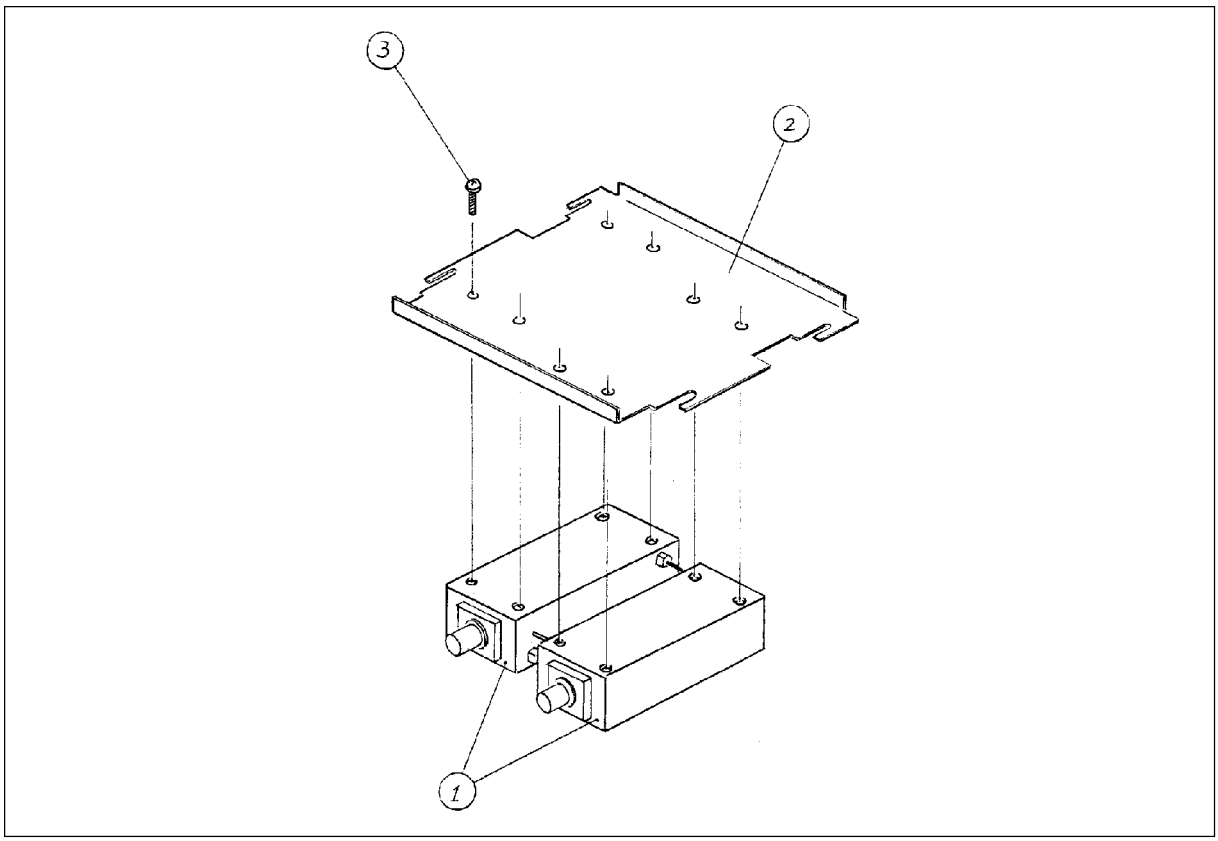
CBS12006

Figure 12-5. Angle Assembly Parts 3/3

Table 12-7. Angle Assembly Parts 3/3

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	8160-0619	5	0	SHIELD GASKET	28480	8160-0619
2	04396-61631	2	1	RF CBL ASSY	28480	04396-61631

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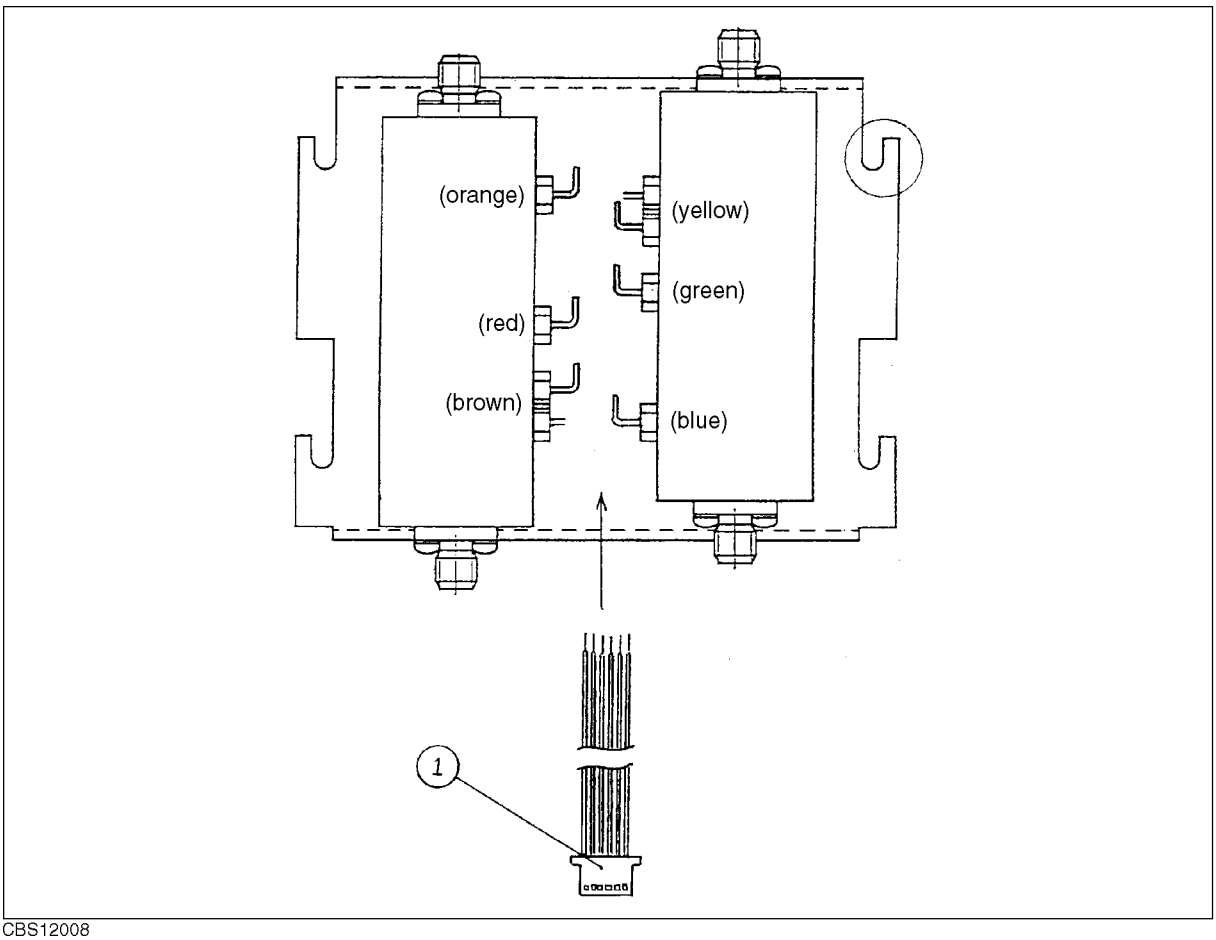
CBS12007

Figure 12-6. ATT Assembly Parts 1/2

Table 12-8. ATT Assembly Parts 1/2

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0955-0664	7	1	A7 Input ATT	28480	0955-0664
	0955-0664	7	1	A8 Output ATT	28480	0955-0644
2	04396-01206	1	1	HOLDER	28480	04396-01206
3	0515-1550	0	8	SCR M3-L 8 P-H	28480	0515-1550

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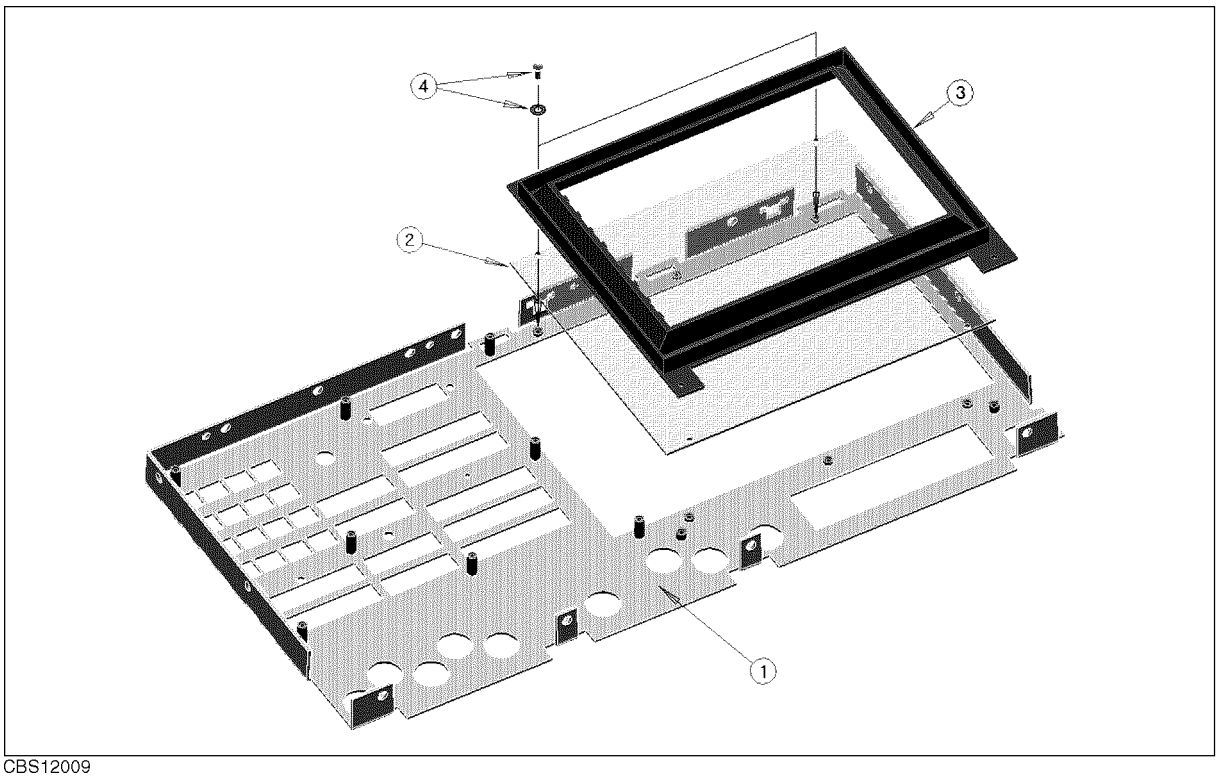
CBS12008

Figure 12-7. ATT Assembly Parts 2/2

Table 12-9. ATT Assembly Parts 2/2

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61679	8	1	WIRE ASSY	28480	04396-61679

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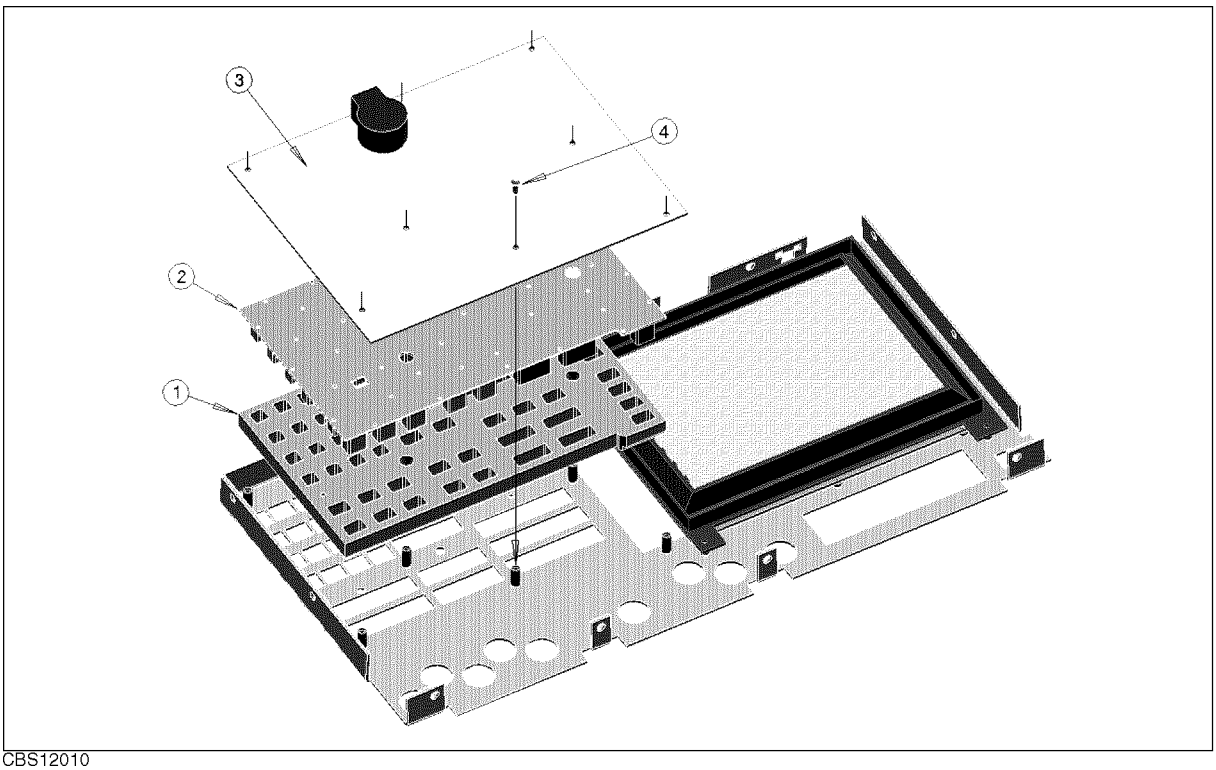
CBS12009

Figure 12-8. Front Assembly Parts 1/5

Table 12-10. Front Assembly Parts 1/5

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-00272	9	1	PANEL SUB	28480	04396-00272
2	E4970-25001	7	1	FILTER	28480	E4970-25001
3	04396-40071	0	1	BEZEL BACK	28480	04396-40071
4	0515-1550	0	2	SCR M3-L 8 P-H	28480	0515-1550
	3050-0891	7	2	WASHER M3	28480	3050-0891

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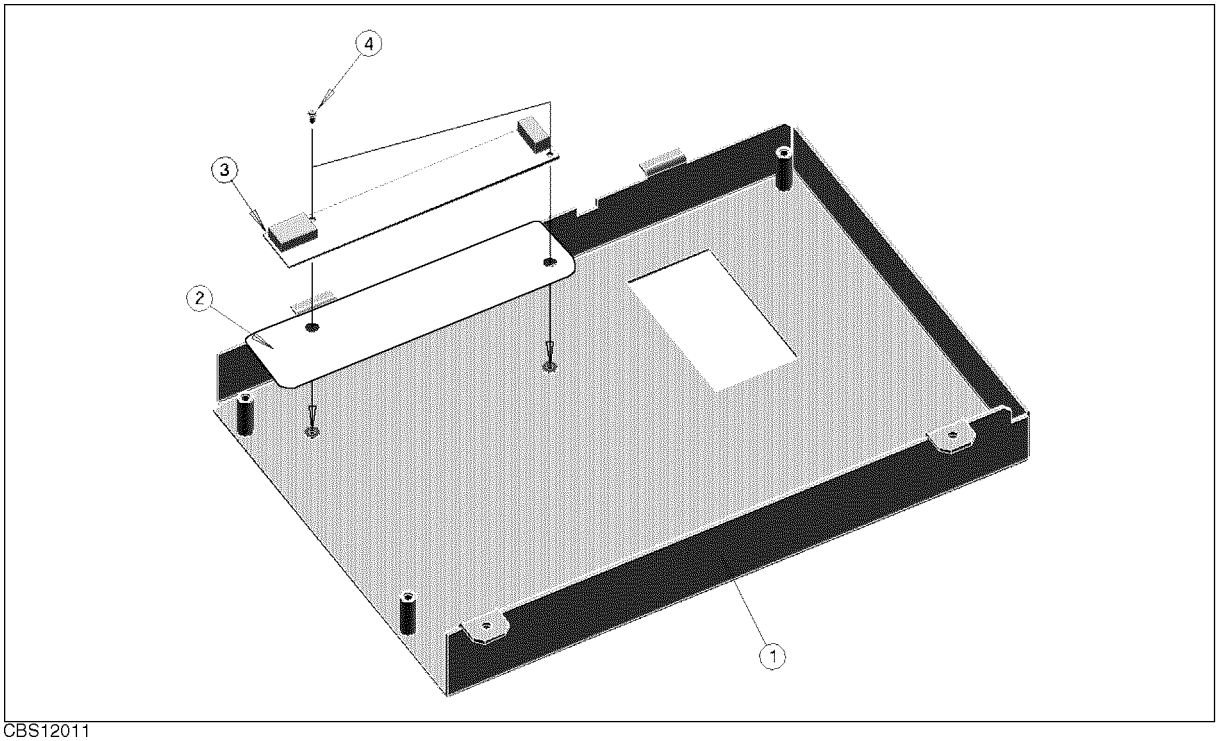
CBS12010

Figure 12-9. Front Assembly Parts 2/5

Table 12-11. Front Assembly Parts 2/5

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-40003	8	1	GUIDE	28480	04396-40003
2	04396-25051	4	1	KEYPAD RUBBER	28480	04396-25051
3	04396-66530	0	1	A30 Front Keyboard	28480	04396-66530
4	0515-1550	0	8	SCR M3-L 8 P-H	28480	0515-1550

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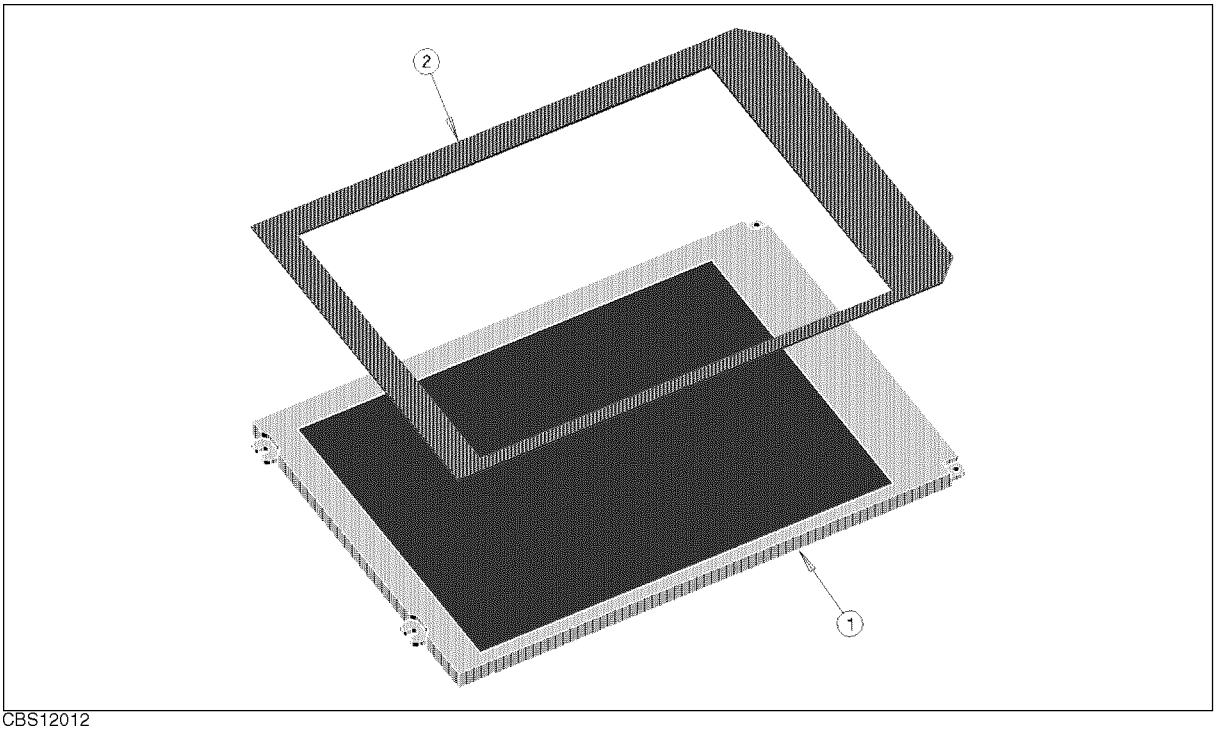
CBS12011

Figure 12-10. Front Assembly Parts 3/5

Table 12-12. Front Assembly Parts 3/5

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-04001	3	1	COVER	28480	E4970-04001
2	E4970-25001	7	1	FILTER	28480	E4970-25001
3	0950-2924	6	1	A54 Inverter	28480	0950-2924
4	0515-0977	3	2	SCR-MACH M2X0.4	28480	0515-0977

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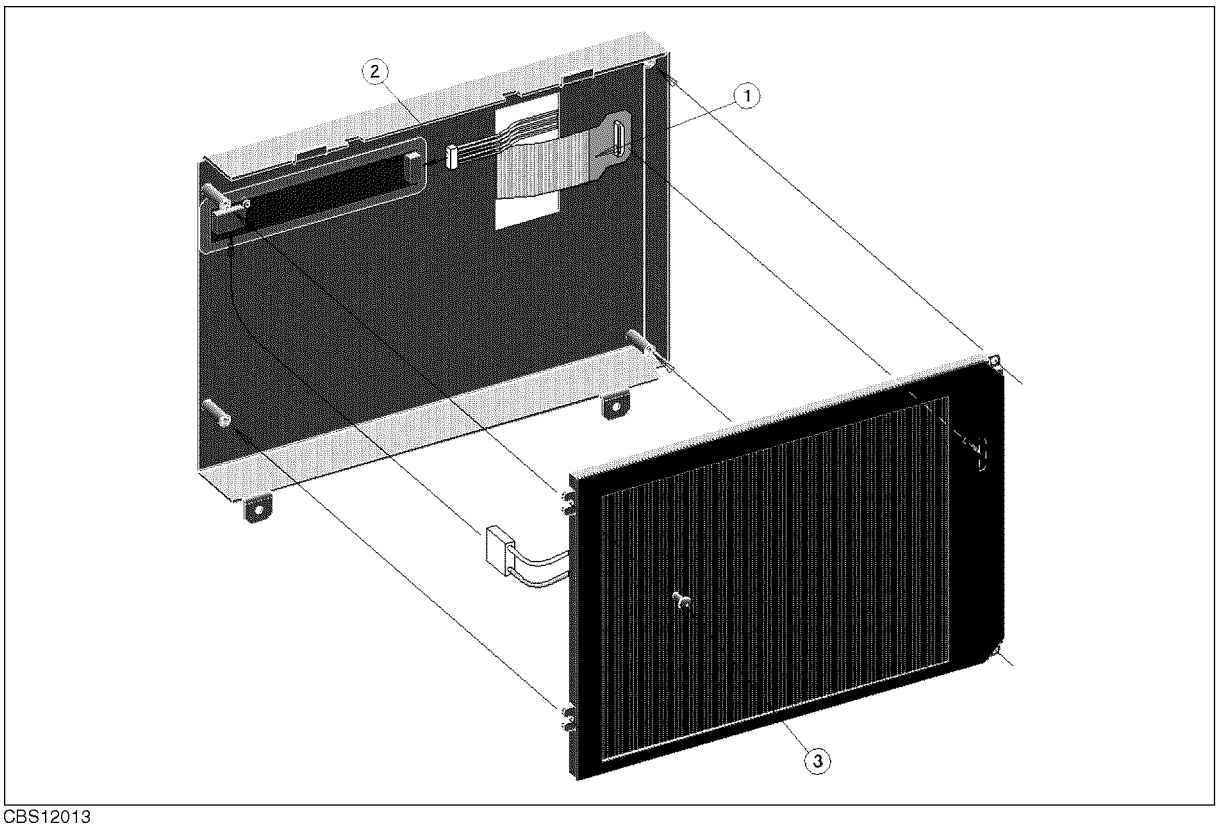
CBS12012

Figure 12-11. Front Assembly Parts 4/5

Table 12-13. Front Assembly Parts 4/5

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	2090-0534	8	1	A52 LCD 8.5IN	28480	2090-0534
2	04396-25071	8	1	GASKET	28480	04396-25071

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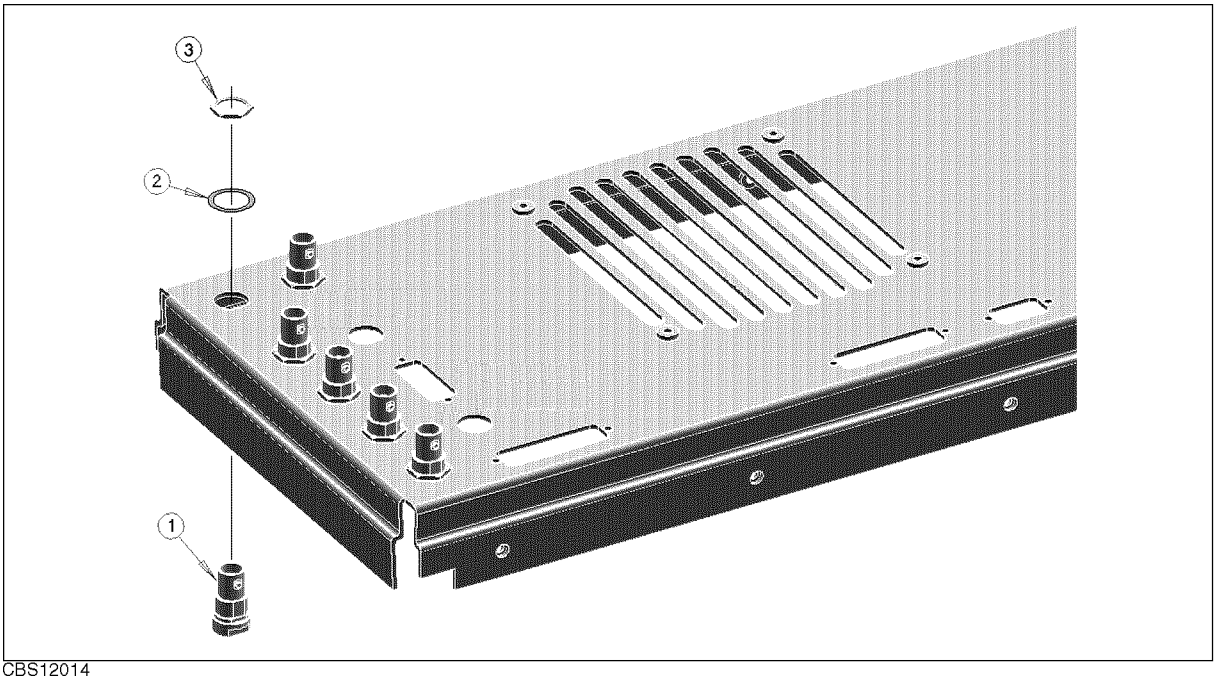
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Figure 12-12. Front Assembly Parts 5/5

Table 12-14. Front Assembly Parts 5/5

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61708	4	1	FLEX PCBD ASSY	28480	04396-61708
2	04396-61709	5	1	CABLE ASSY	28480	04396-61709
3	0515-1550	0	1	SCR M3-L 8 P-H	28480	0515-1550

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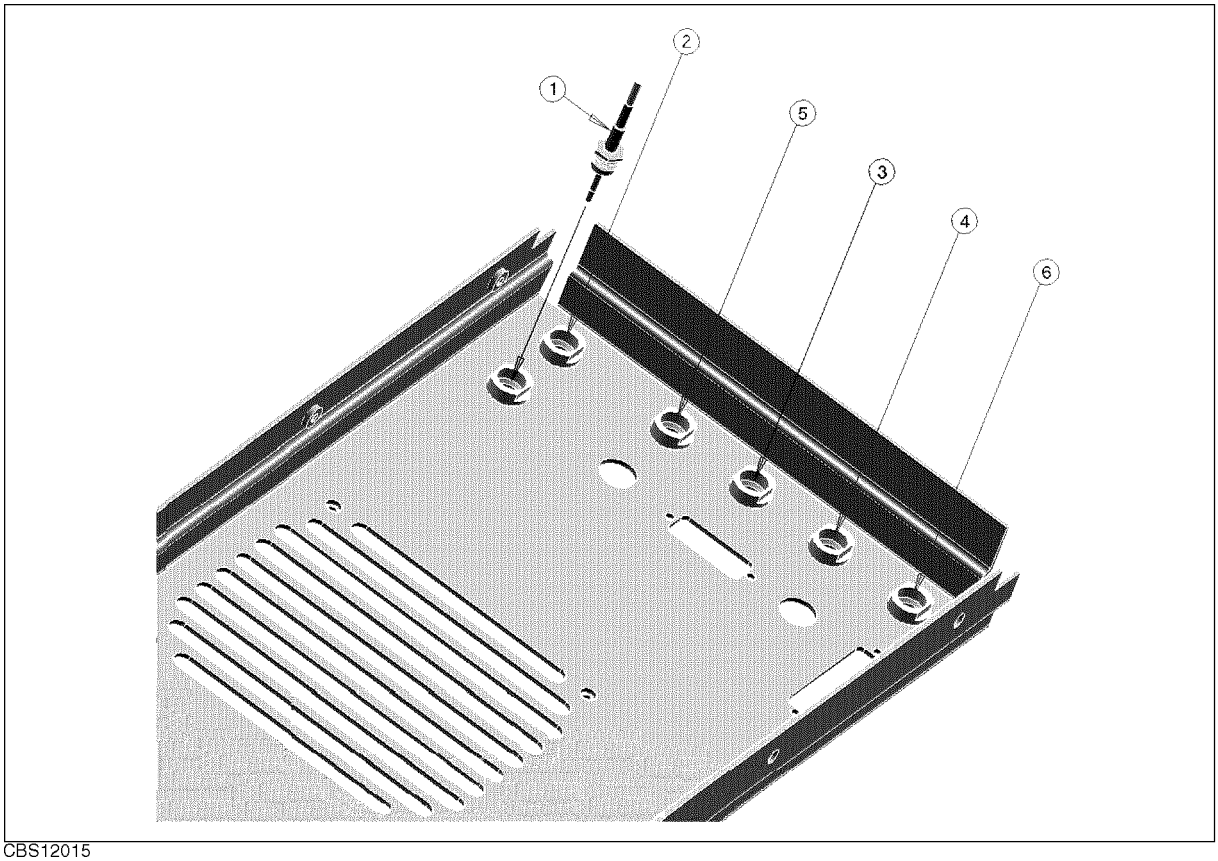
CBS12014

Figure 12-13. Rear Assembly Parts 1/7

Table 12-15. Rear Assembly Parts 1/7

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1250-0252	6	4	CONN-RF BNC	28480	1250-0252
2	2190-0102	8	4	WSHR-LK INTL T	28480	2190-0102
3	2950-0035	8	4	NUT-HEX-DBL-CHAM	28480	2950-0035

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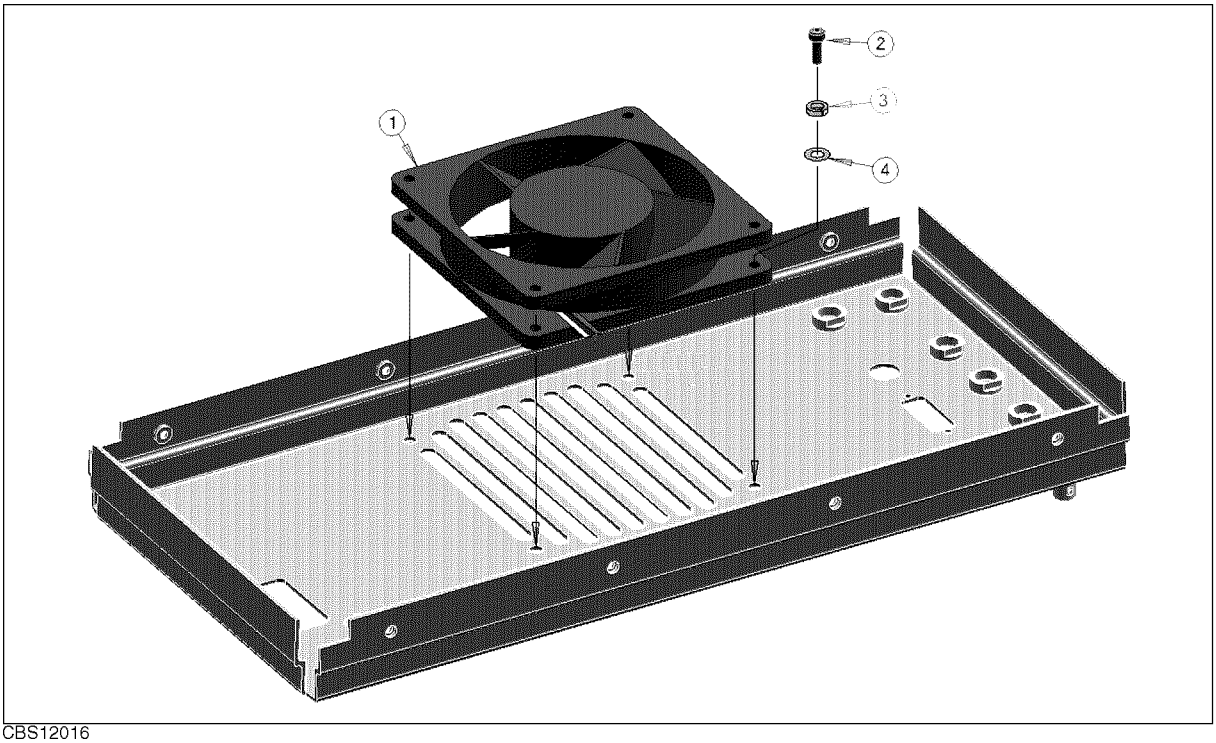
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Figure 12-14. Rear Assembly Parts 2/7

Table 12-16. Rear Assembly Parts 2/7

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61633	4	1	RF CBL ASSY	28480	04396-61633
2	04396-61634	5	1	RF CBL ASSY	28480	04396-61634
3	04396-61632	3	1	RF CBL ASSY	28480	04396-61632
4	04396-61635	6	1	RF CBL ASSY	28480	04396-61635
5	04396-61636	7	1	RF CBL ASSY “V” (Option 1D5 Only)	28480	04396-61636
6	04396-61637	8	1	RF CBL ASSY “T” (Option 1D6 Only)	28480	04396-61637

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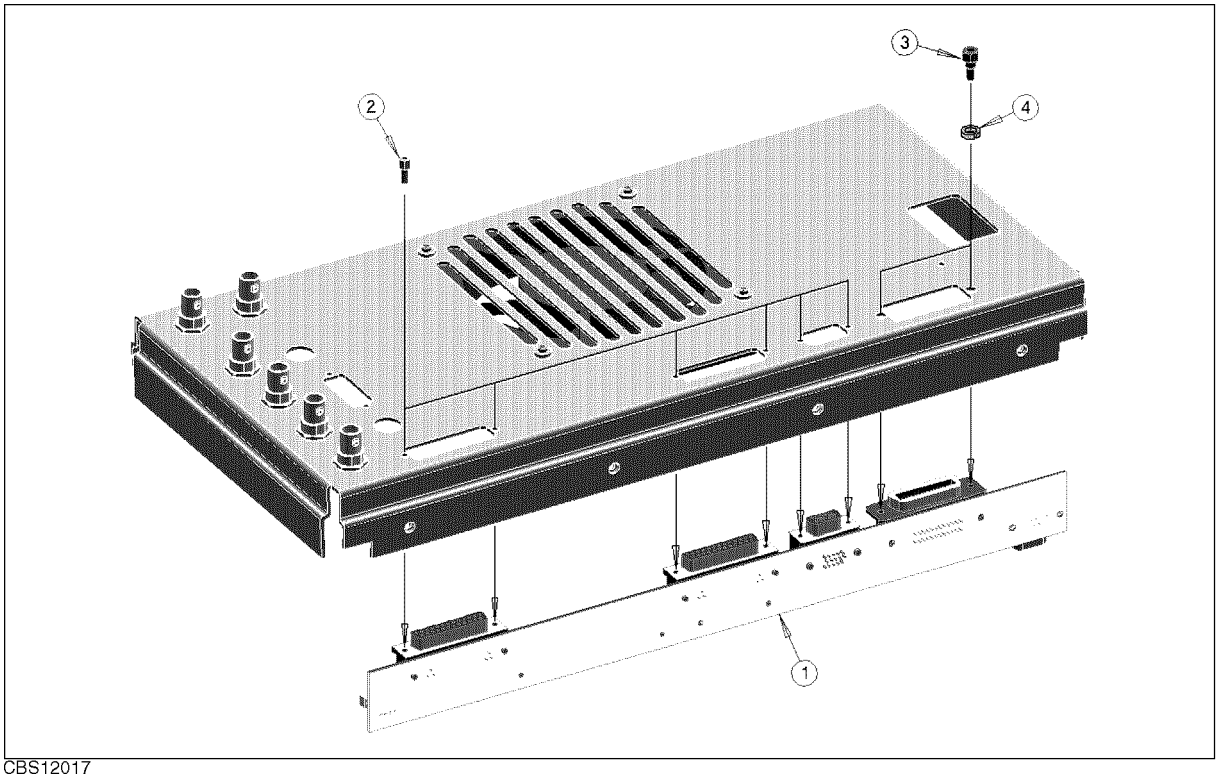
CBS12016

Figure 12-15. Rear Assembly Parts 3/7

Table 12-17. Rear Assembly Parts 3/7

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61001	0	1	FAN ASSY	28480	04396-61001
2	0515-1598	6	4	SCR SKT-HEAD	28480	0515-1598
3	2190-0586	2	4	WSHR-LK HLCL	28480	2190-0586
4	3050-0893	9	4	WSHR-FL	28480	3050-0893

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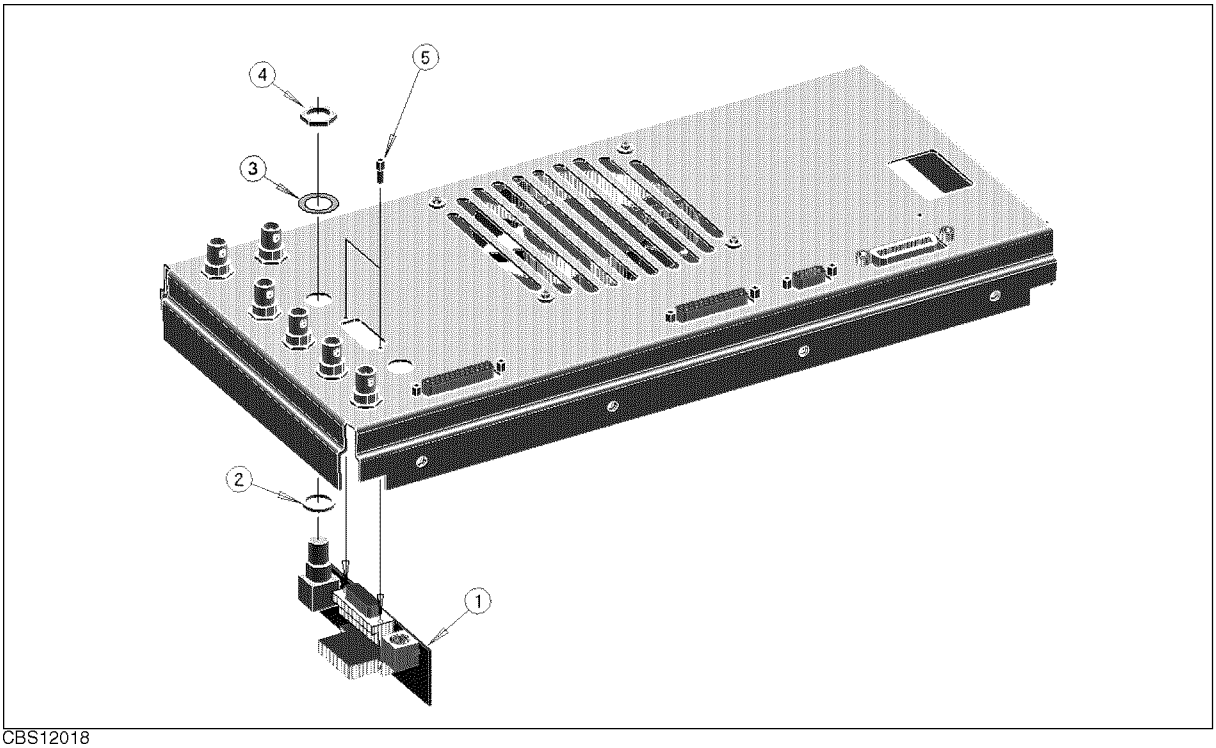
CBS12017

Figure 12-16. Rear Assembly Parts 4/7

Table 12-18. Rear Assembly Parts 4/7

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-66531	4	1	A31 I/O Connector	28480	E4970-66531
2	1251-7812	0	8	JACKSCREW	28480	1251-7812
3	0380-0644	4	2	STDF-HEX-M/FEM	28480	0380-0644
4	2190-0577	1	2	WSHR-LK HLCL	28480	2190-0577

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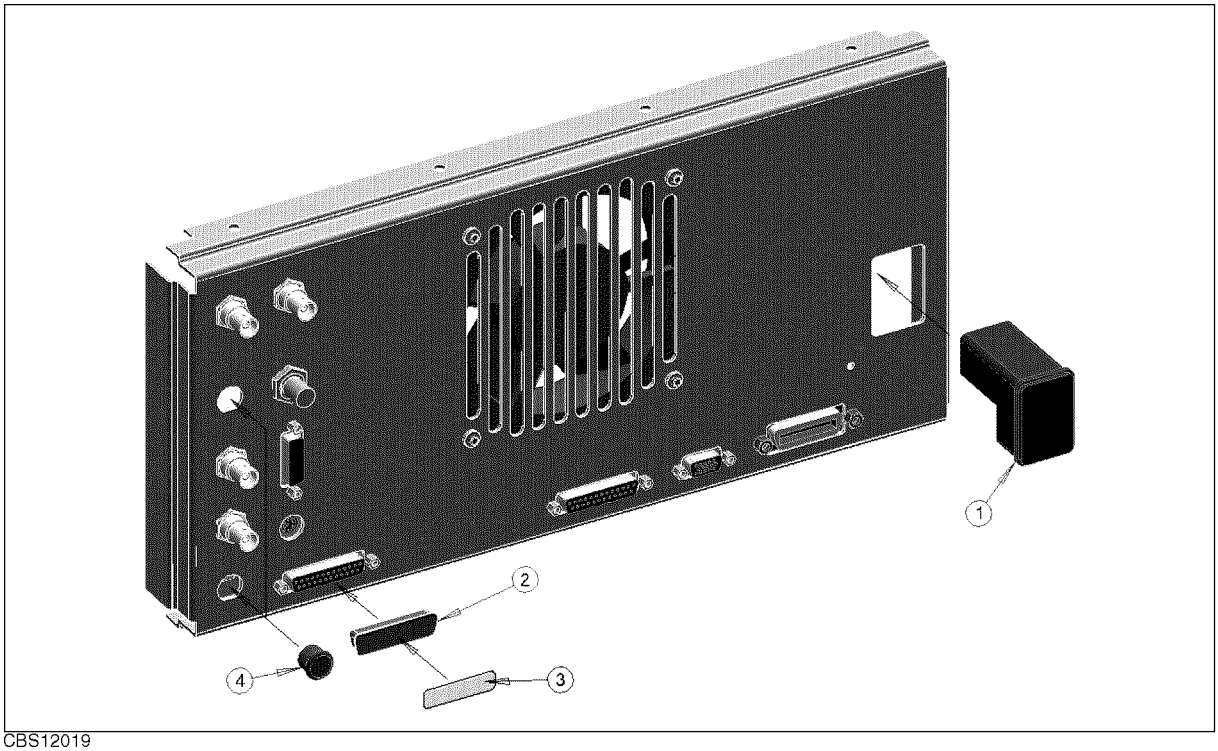
CBS12018

Figure 12-17. Rear Assembly Parts 5/7

Table 12-19. Rear Assembly Parts 5/7

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-66532	5	1	A32 IBASIC I/F	28480	E4970-66532
2	3050-1546	1	1	WASHER FLAT NM	28480	3050-1546
3	2190-0054	9	1	WSHR-LK INTL T	28480	2190-0054
4	2950-0054	1	1	NUT-HEX-DBL-CHAM	28480	2950-0054
5	1251-7812	0	2	JACKSCREW	28480	1251-7812

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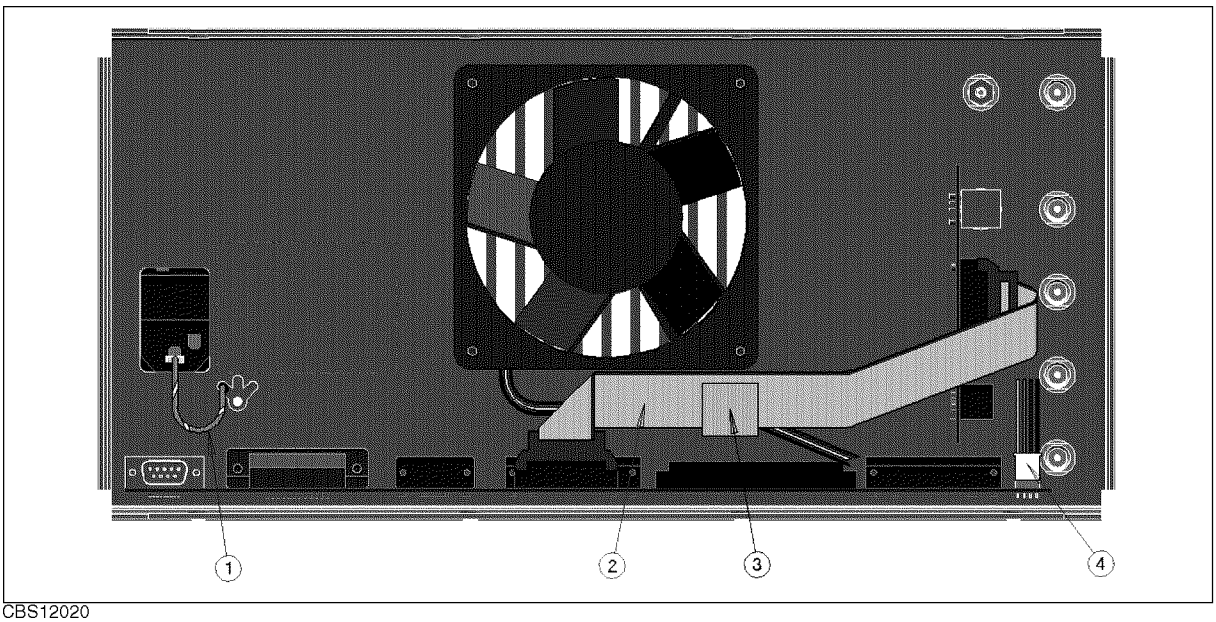
CBS12019

Figure 12-18. Rear Assembly Parts 6/7

Table 12-20. Rear Assembly Parts 6/7

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1252-6951	8	1	AC INLET	28480	1252-6951
	2110-0030	3	1	FUSE 5A 250V	28480	2110-0030
	2110-1134	0	1	FUSE DRAWER	28480	2110-1134
2	1252-4690	8	1	DUST COVER	28480	1252-4690
3	04396-87111	7	1	LABEL	28480	04396-87111
4	6960-0041	1	2	PLUG HOLE	28480	6960-0041

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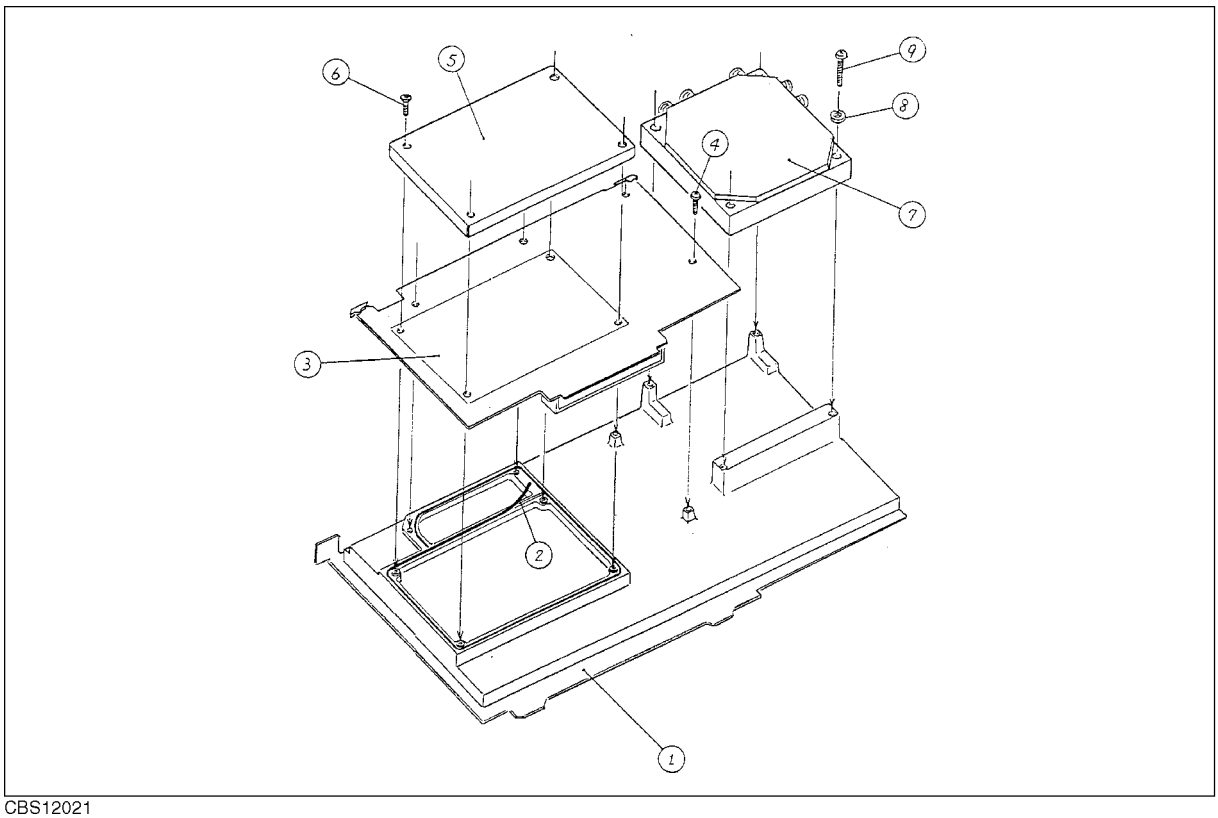
CBS12020

Figure 12-19. Rear Assembly Parts 7/7

Table 12-21. Rear Assembly Parts 7/7

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	E5100-61640	6	1	WIRE ASSY GND	28480	E5100-61640
2	04396-61706	2	1	CABLE ASSY	28480	04396-61706
3	1400-0611	0	1	CLAMP-CABLE	28480	1400-0611
4	04396-61682	3	1	WIRE ASSY	28480	04396-61682

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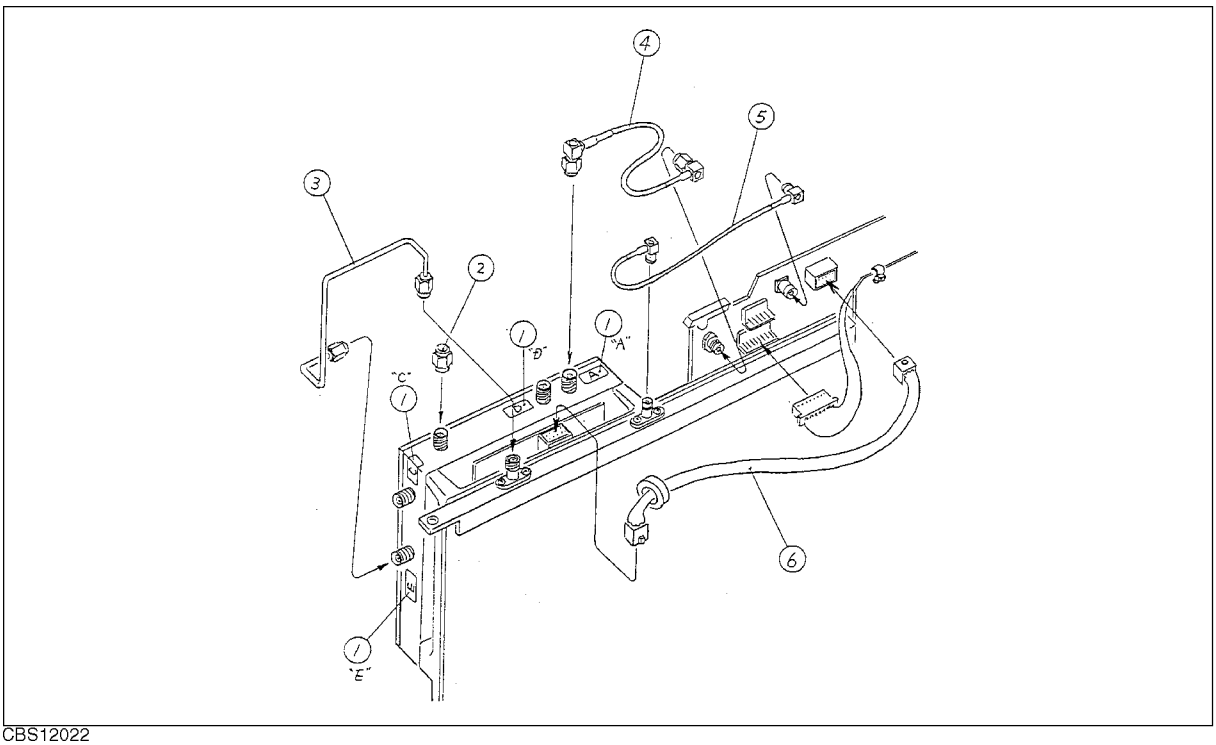
CBS12021

Figure 12-20. Main Frame Assembly Parts 1/19 (A3 Assemblies)

Table 12-22. Main Frame Assembly Parts 1/19 (A3 Assemblies)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-66513	9	1	A3A2 Second LO	28480	04396-66513
2	8160-0512	7	58	RFI D STRIP.062W	28480	8160-0512
3	04396-66503	7	1	A3A1 ALC	28480	04396-66503
4	0515-1550	0	4	SCR M3-L 8 P-H	28480	0515-1550
5	04396-00632	5	1	CASE-SHIELD	28480	04396-00632
6	0515-1005	0	4	SCR FL M3L10	28480	0515-1005
7	5086-7620	1	1	A3A3 Source Module	28480	5086-7620
8	2190-0584	0	4	WSHR-LK HLCL	28480	2190-0584
9	0515-0920	6	4	SCR-MACH M3X0.5	28480	0515-0920

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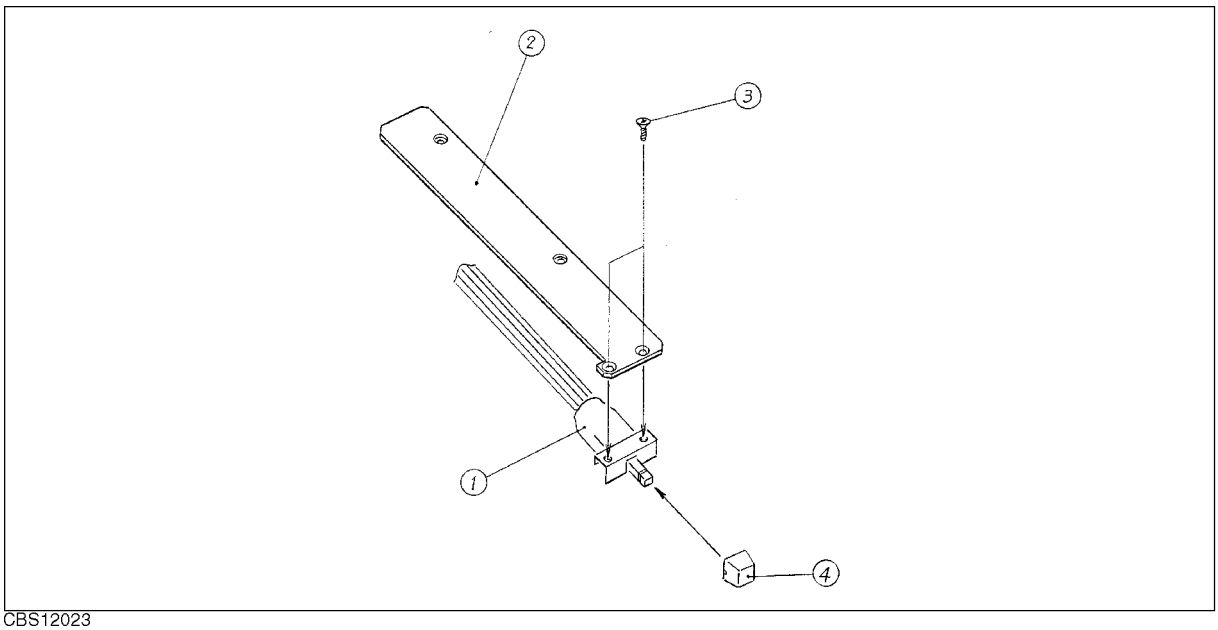
CBS12022

Figure 12-21. Main Frame Assembly Parts 2/19 (A3 Assemblies)

Table 12-23. Main Frame Assembly Parts 2/19 (A3 Assemblies)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-87102	6	1	LABEL	28480	04396-87102
2	1810-0118	1	1	TERMINATION-COAX	28480	1810-0118
3	04396-61605	0	1	RF CBL ASSY SRGD	28480	04396-61605
4	04396-61621	0	1	RF CBL ASSY	28480	04396-61621
5	04396-61622	1	1	RF CBL ASSY	28480	04396-61622
6	04396-61673	2	1	WIRE ASSY	28480	04396-61673

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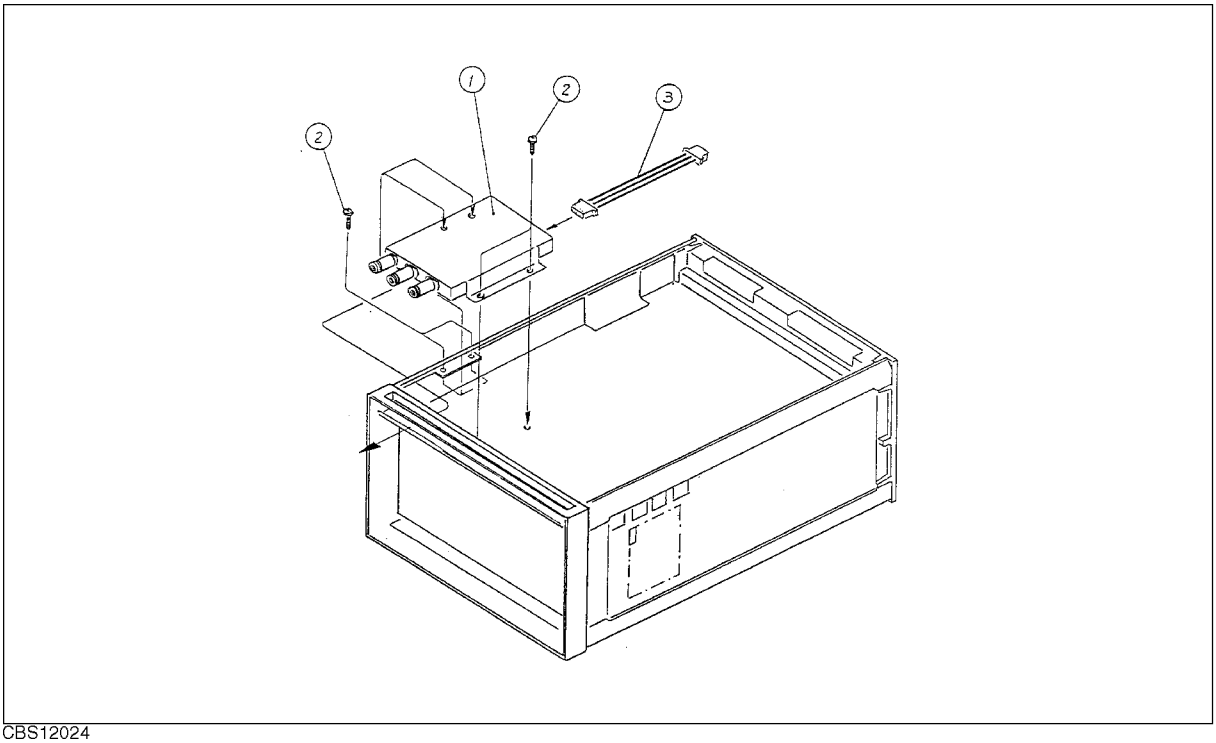
CBS12023

Figure 12-22. Main Frame Assembly Parts 3/19

Table 12-24. Main Frame Assembly Parts 3/19

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61701	7	1	CABLE ASSY	28480	04396-61701
2	04396-01274	3	1	HOLDER	28480	04396-01274
3	0515-0999		2	M2.5X0.45 L=6 FL	28480	HOLDER
4	5041-0564	4	1	KEY-Q-CORP WHT	28480	5041-0564

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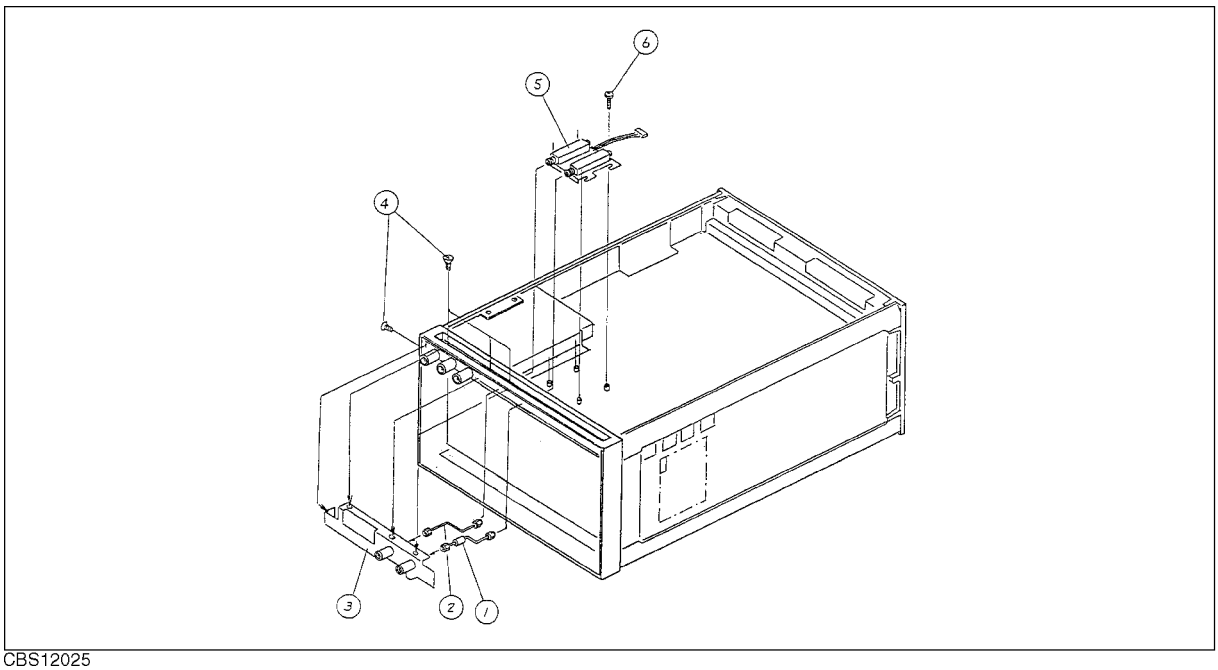
CBS12024

Figure 12-23. Main Frame Assembly Parts 4/19 (A9 Input Multiplexer Assembly)

Table 12-25.
Main Frame Assembly Parts 4/19 (A9 Input Multiplexer Assembly)

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-66509	3	1	A9 Input Multiplexer	28480	04396-66509
2	0515-1550	0	4	SCR M3-L 8 P-H	28480	0515-1550
3	04396-61680	1	1	WIRE ASSY	28480	04396-61680

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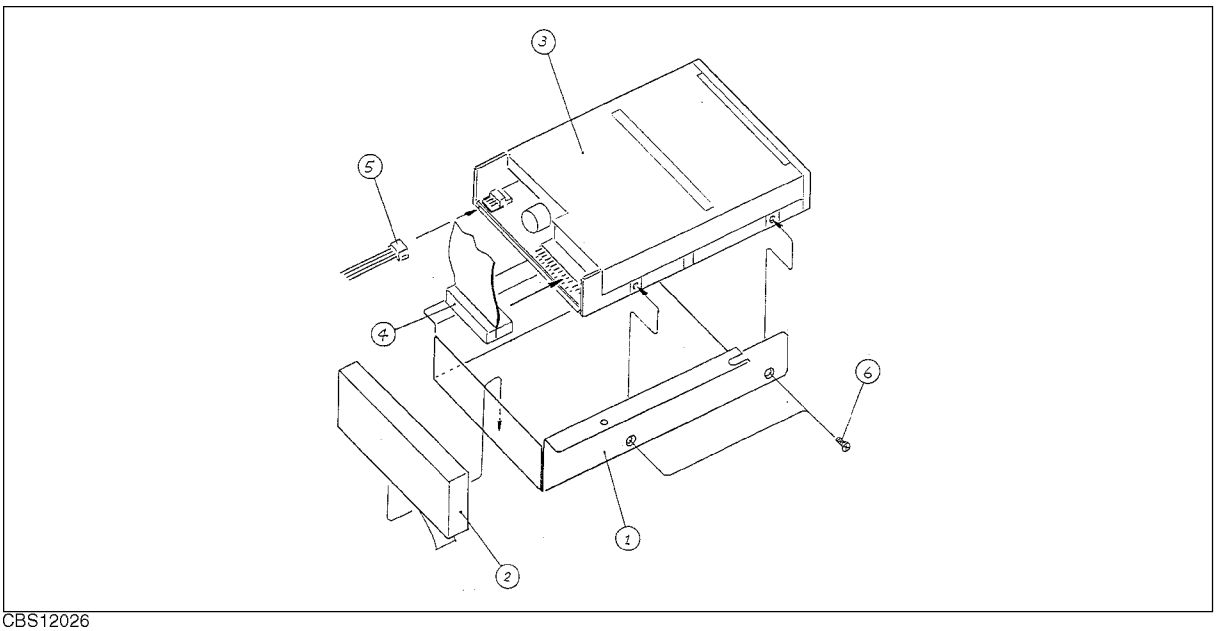
CBS12025

Figure 12-24. Main Frame Assembly Parts 5/19 (ATT & Angle Assemblies)

Table 12-26. Main Frame Assembly Parts 5/19 (ATT & Angle Assemblies)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61601	6	1	RF CBL ASSY SRGD	28480	04396-61601
2	04396-61602	7	1	RF CBL ASSY SRGD	28480	04396-61602
3	04396-64903	7	1	ANGLE ASSY	28480	04396-64903
4	0515-1011	8	4	SCR FL M4L6	28480	0515-1011
5				See ATT Assembly Parts	28480	
6	0515-1550	0	4	SCR M3-L 8 P-H	28480	0515-1550

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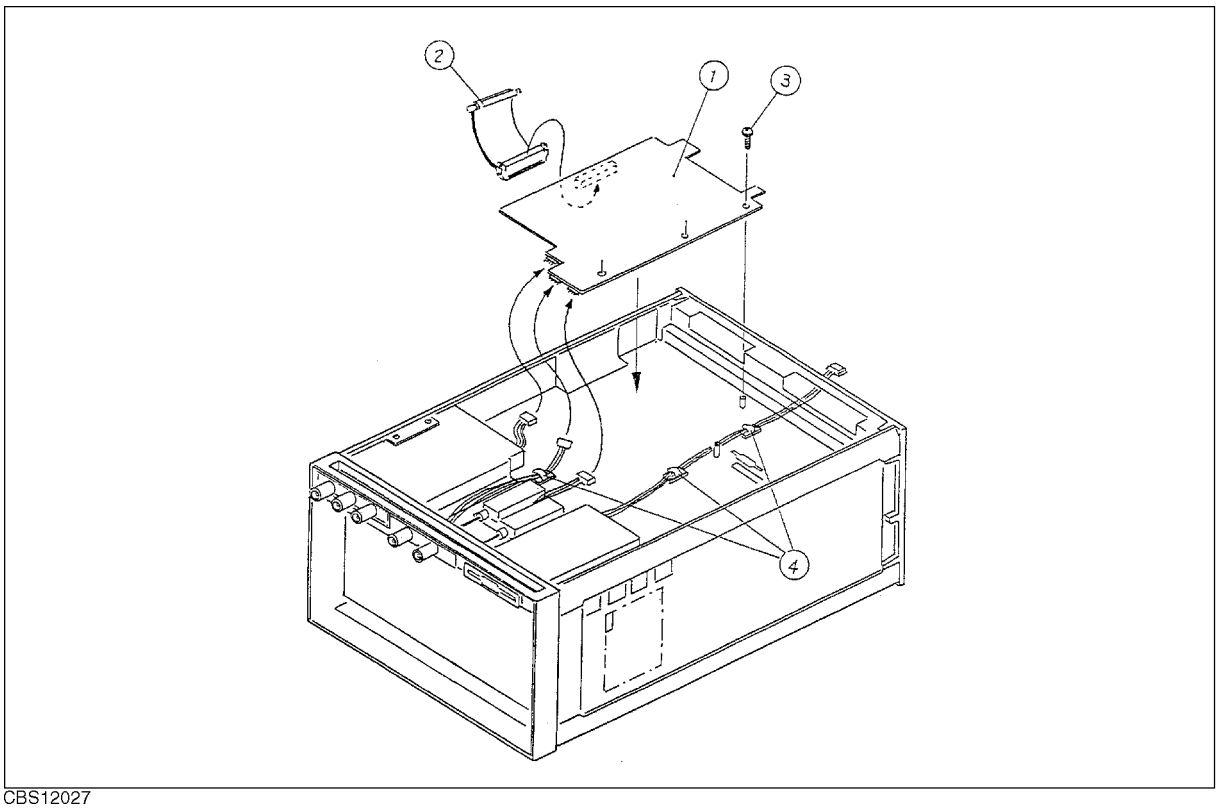
CBS12026

Figure 12-25. Main Frame Assembly Parts 6/19 (A53 FDD Assembly)

Table 12-27. Main Frame Assembly Parts 6/19 (A53 FDD Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-01275	4	1	ANGLE	28480	04396-01275
2	04396-25004	7	1	SPONGE	28480	04396-25004
3	0950-3208	1	1	A53 FDD 3.5 2MODE	28480	0950-3208
4	04396-61651	6	1	FLAT CBL ASSY	28480	04396-61651
5	04396-61672	1	1	WIRE ASSY	28480	04396-61672
6	0515-0914	8	24	SCR-MACH M3X0.5	28480	0515-0914

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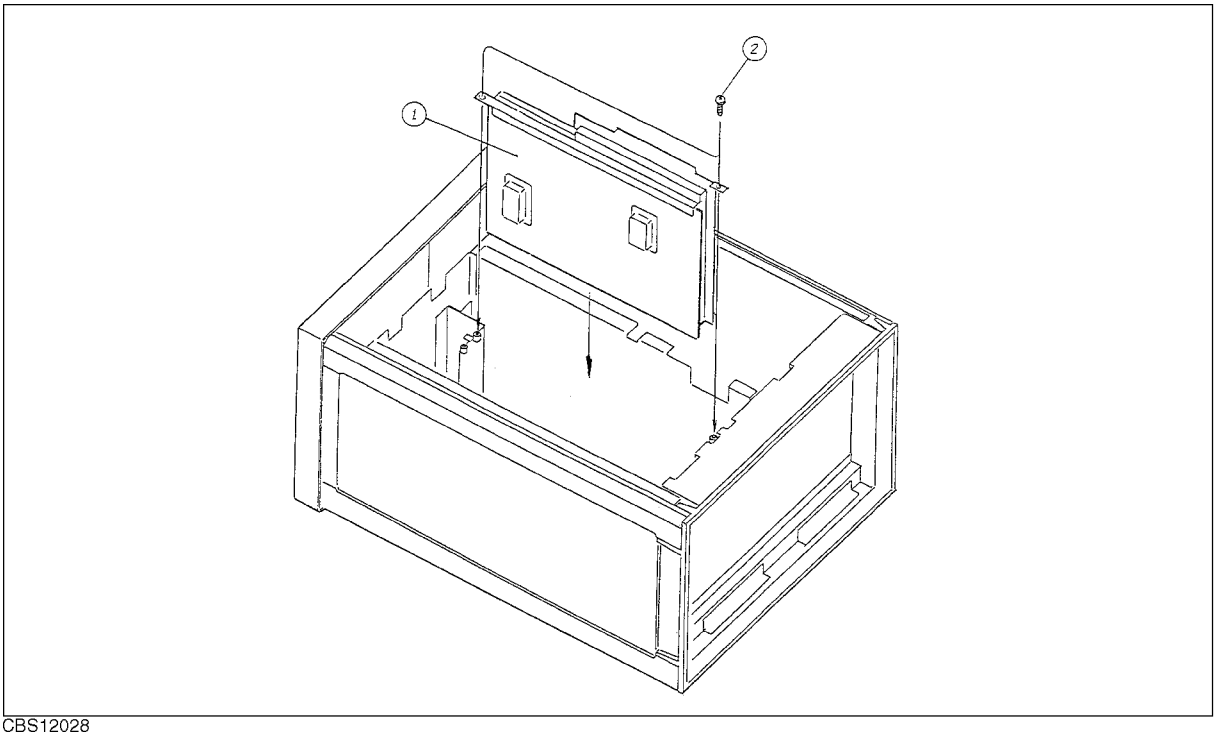
CBS12027

Figure 12-26. Main Frame Assembly Parts 7/19 (A20 Motherboard Assembly)

Table 12-28.
Main Frame Assembly Parts 7/19 (A20 Motherboard Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-66520	8	1	A20 Motherboard	28480	04396-66520
2	04396-61661	8	2	CA-ASSY FLAT 100	28480	04396-61661
3	0515-1550	0	3	SCR M3-L 8 P-H	28480	0515-1550
4	1400-1334	6	5	CLAMP CABLE	28480	1400-1334

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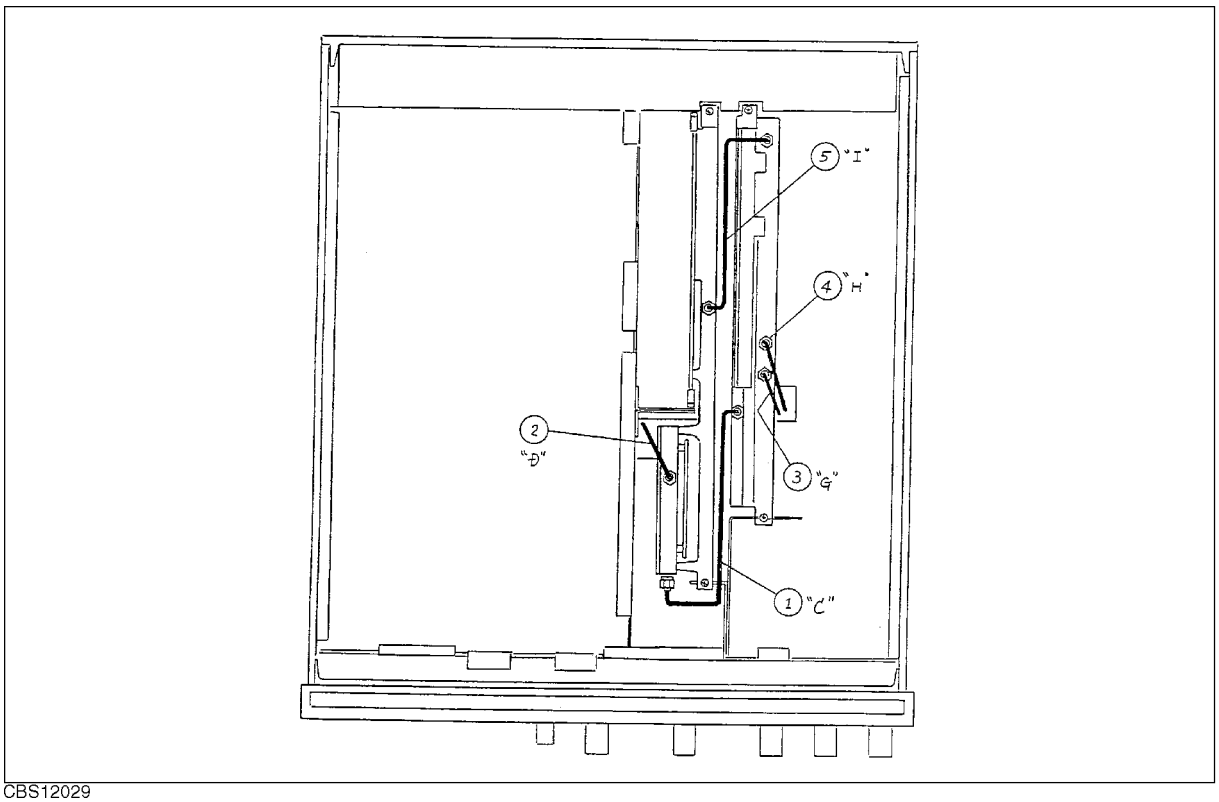
CBS12028

Figure 12-27. Main Frame Assembly Parts 8/19 (A4 First LO/Receiver RF Assembly)

Table 12-29.
Main Frame Assembly Parts 8/19 (A4 First LO/RReceiver RF Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61004	3	1	A4 First LO/Receiver RF	28480	04396-61004
2	0515-2079	0	8	SCR M4X8	28480	0515-2079

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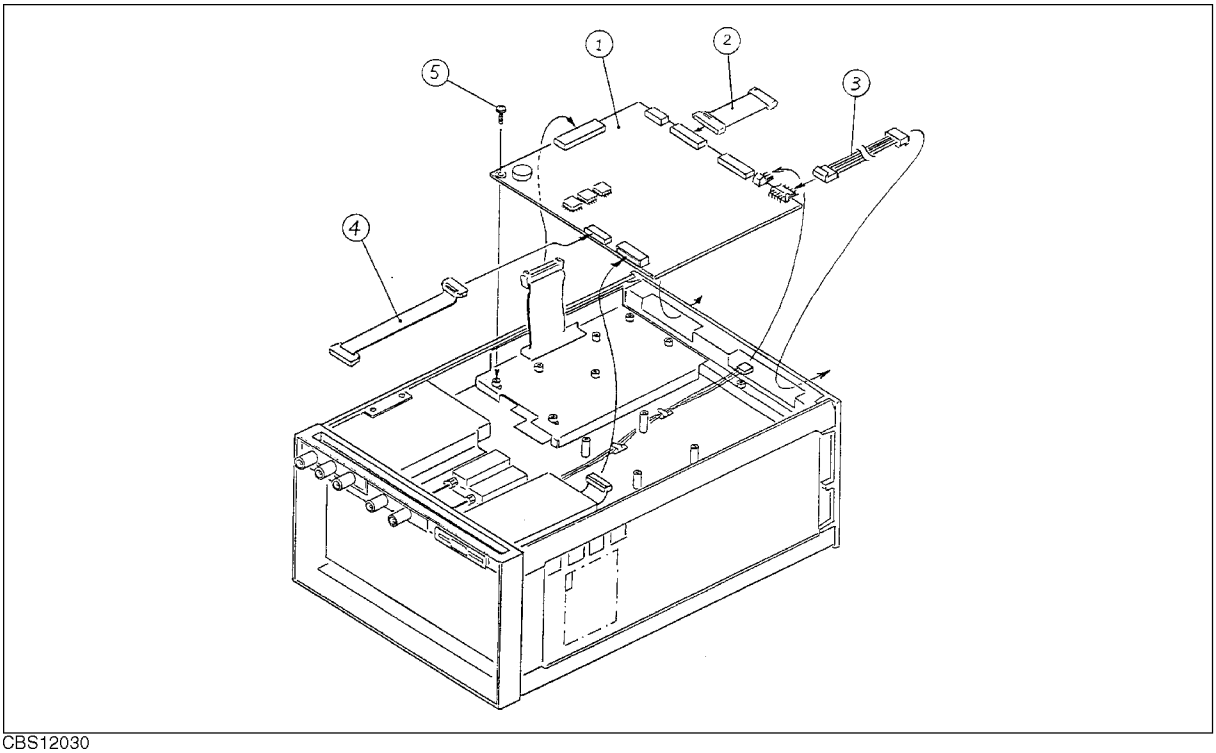
CBS12029

Figure 12-28. Main Frame Assembly Parts 9/19 (RF Cable Assemblies)

Table 12-30. Main Frame Assembly Parts 9/19 (RF Cable Assemblies)

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61603	8	1	RF CBL ASSY SRGD	28480	04396-61603
2	04396-61604	9	1	RF CBL ASSY SRGD	28480	04396-61604
3	04396-61607	2	1	RF CBL ASSY SRGD	28480	04396-61607
4	04396-61608	3	1	RF CBL ASSY SRGD	28480	04396-61608
5	04396-61609	4	1	RF CBL ASSY SRGD	28480	04396-61609

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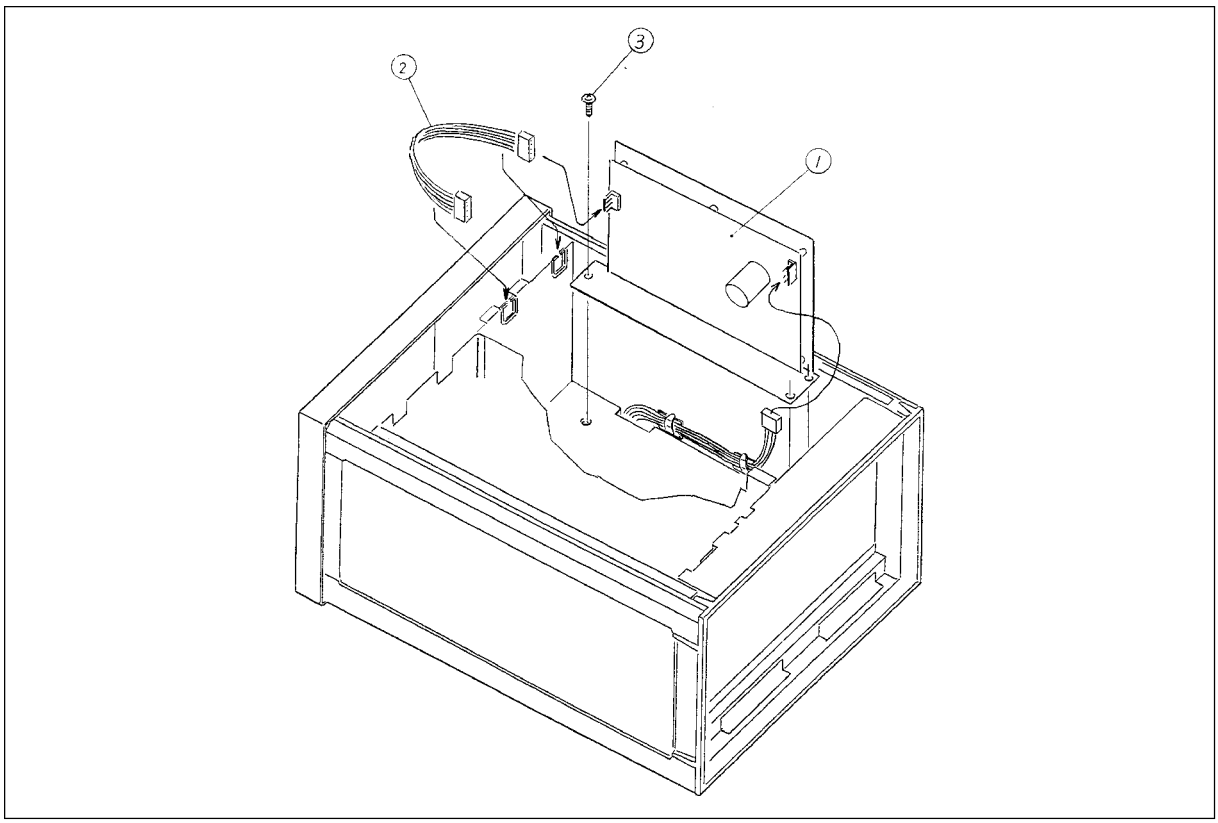
CBS12030

Figure 12-29. Main Frame Assembly Parts 10/19 (A1 CPU Assembly)

Table 12-31. Main Frame Assembly Parts 10/19 (A1 CPU Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-66501	8	1	A1 CPU ASSY	28480	E4970-66501
2	04396-61661	8	2	CA-ASSY FLAT 100	28480	04396-61661
3	04396-61671	0	2	WIRE ASSY	28480	04396-61671
4	04396-61662	9	1	CA-ASSY FLAT 40	28480	04396-61662
5	0515-1550	0	1	SCR M3-L 8 P-H	28480	0515-1550

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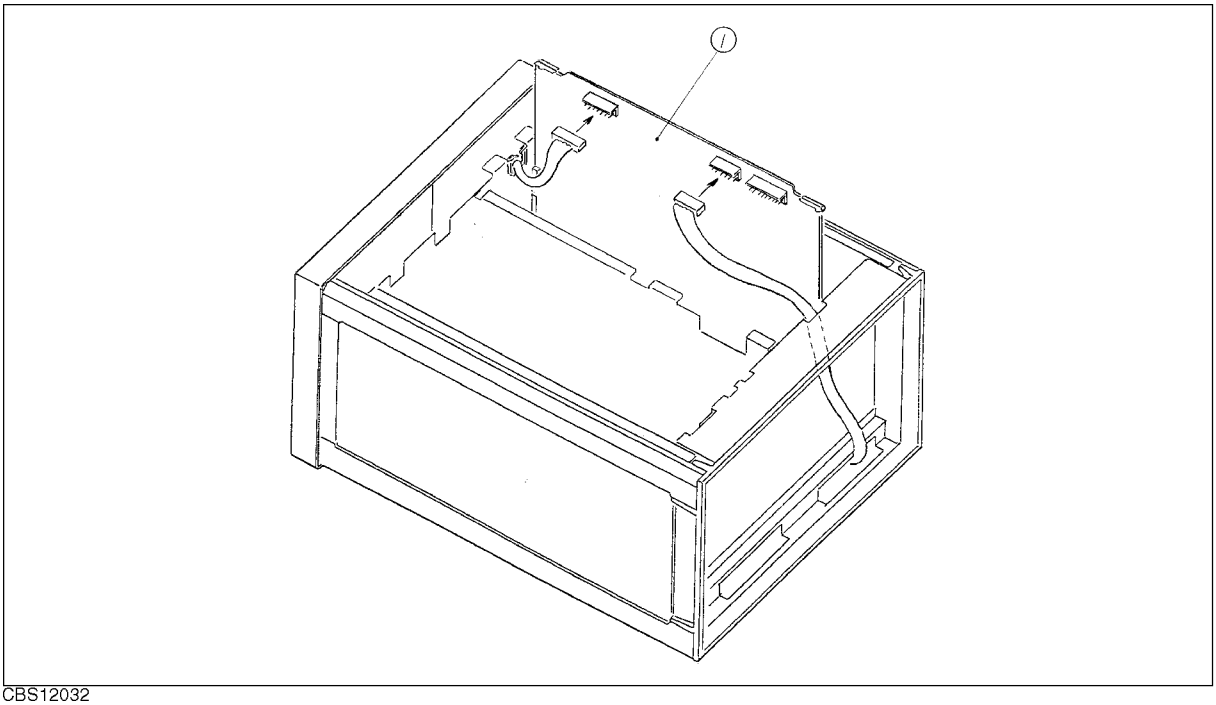
CBS12031

Figure 12-30. Main Frame Assembly Parts 11/19 (A40 Pre-regulator Assembly)

Table 12-32.
Main Frame Assembly Parts 11/19 (A40 Pre-regulator Assembly)

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	0950-3246	7	1	A40 Pre-regulator	28480	0950-3246
2	04396-61671	0	2	WIRE ASSY	28480	04396-61671
3	0515-1719	3	14	SCR M4X10	28480	0515-1719

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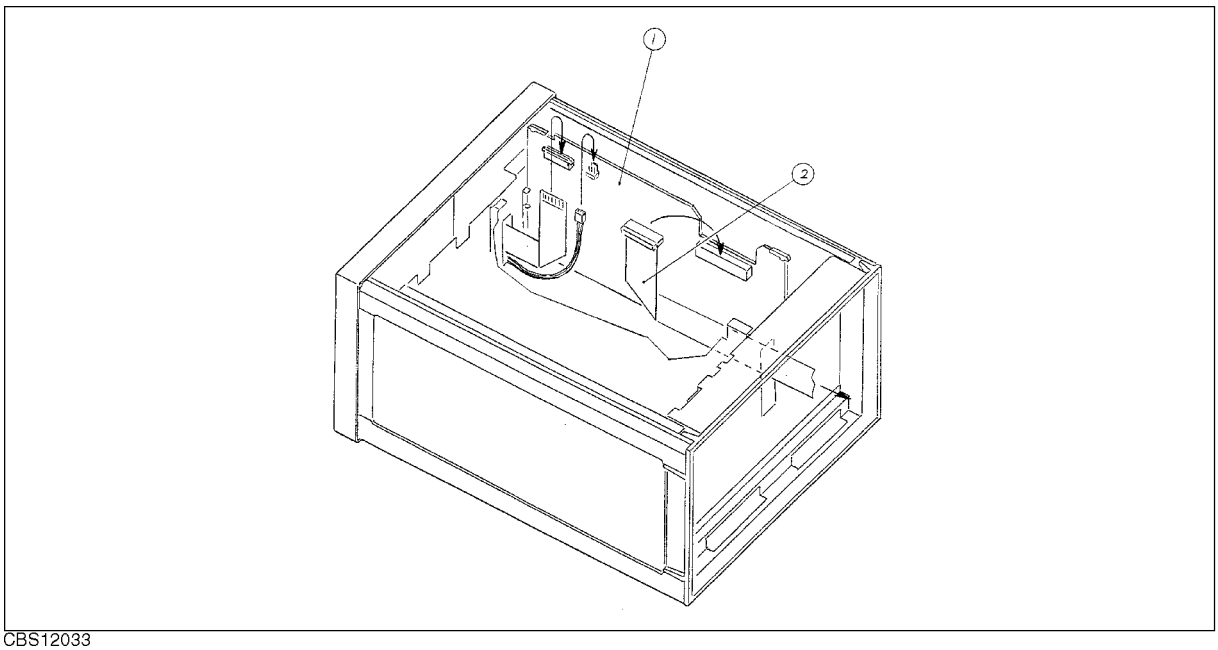
CBS12032

Figure 12-31. Main Frame Assembly Parts 12/19 (A50 DC-DC Converter Assembly)

Table 12-33.
Main Frame Assembly Parts 12/19 (A50 DC-DC Converter Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-66550	7	1	A50 DC-DC Converter	28480	E4970-66550

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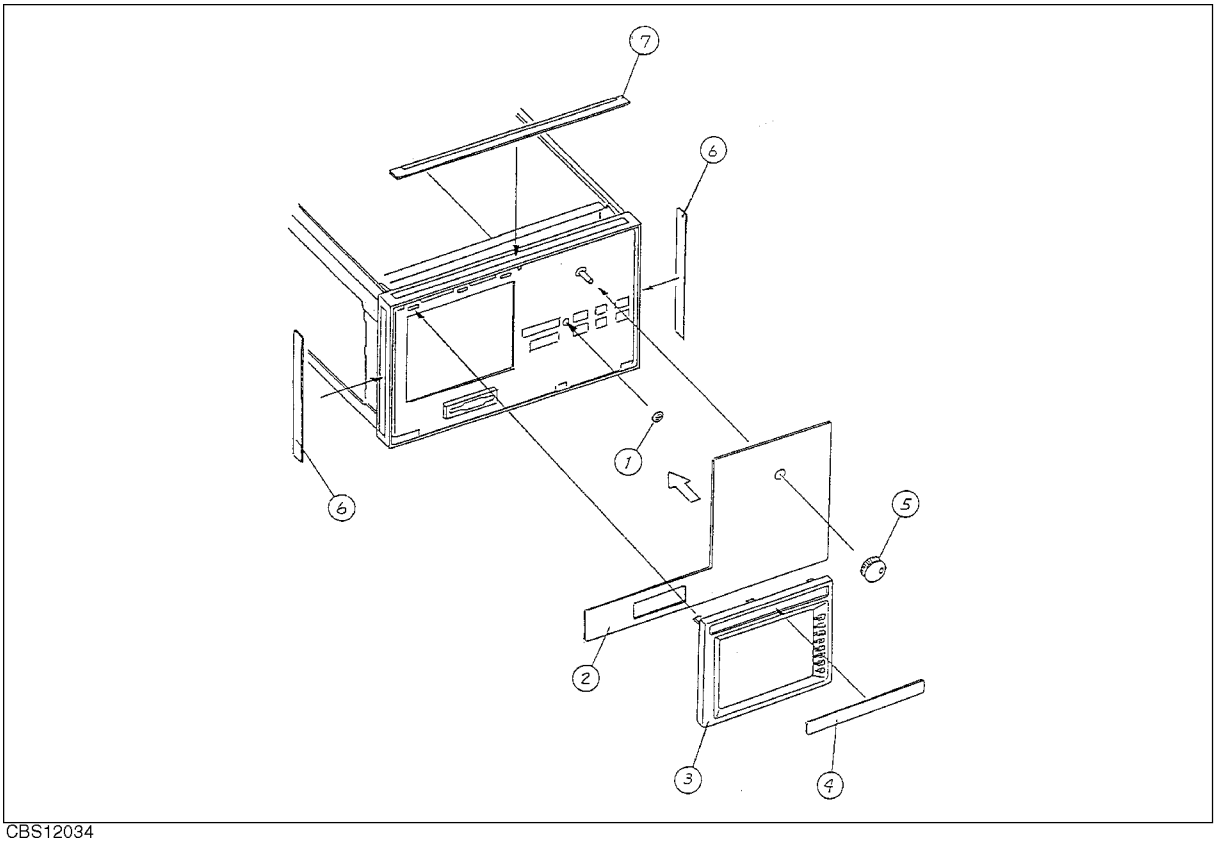
CBS12033

Figure 12-32. Main Frame Assembly Parts 13/19 (A51 GSP Assembly)

Table 12-34. Main Frame Assembly Parts 13/19 (A51 GSP Assembly)

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	E4970-66552	9	1	A51 GSP	28480	E4970-66552
2	04396-61707	3	1	CABLE ASSY	28480	04396-61707

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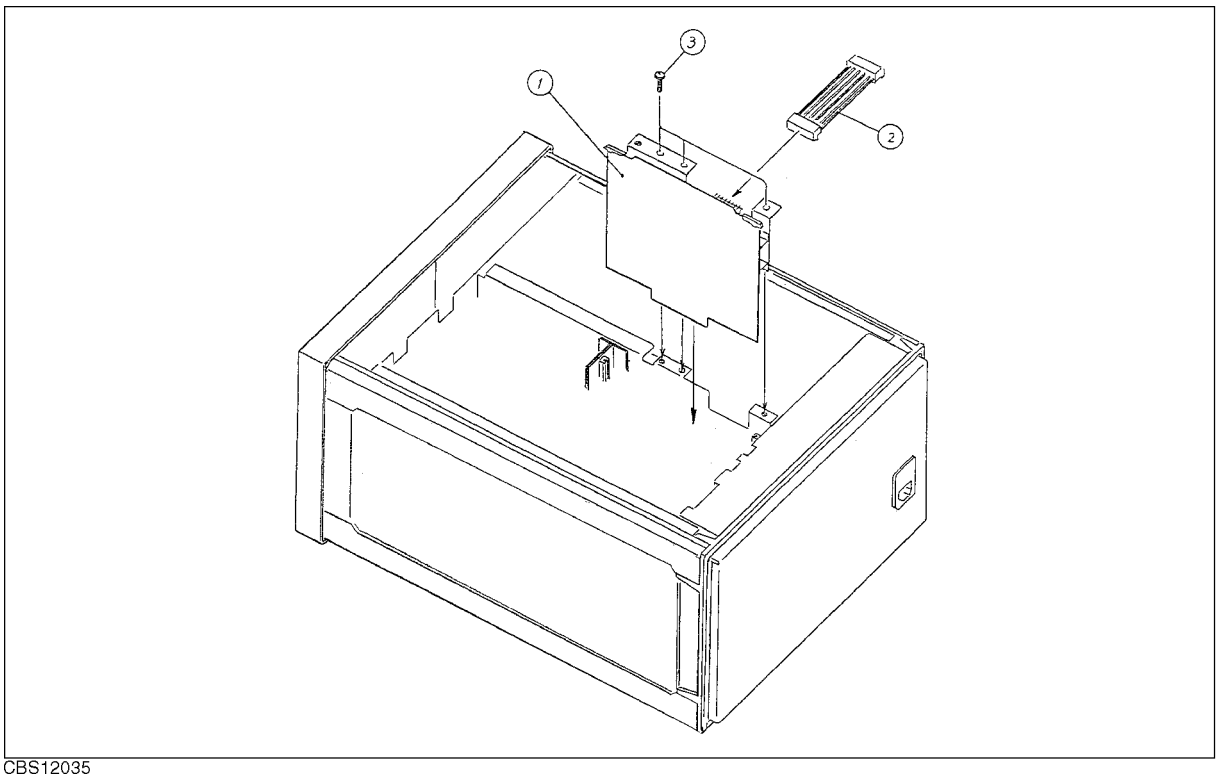
CBS12034

Figure 12-33. Main Frame Assembly Parts 14/19 (Front Bezel Assembly)

Table 12-35. Main Frame Assembly Parts 14/19 (Front Bezel Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04191-08000	0	1	SPRING	28480	04191-08000
2	04396-00271	8	1	PANEL FRONT	28480	04396-00271
3	04396-40051	6	1	BEZEL	28480	04396-40051
4	04396-87103	7	1	LABEL	28480	04396-87103
5	0370-3069	2	1	KNOB	28480	0370-3069
6	5041-9173	9	2	SIDE TRIM 221.5	28480	5041-9173
7	5041-9176	2	2	TRIM STRIP	28480	5041-9176

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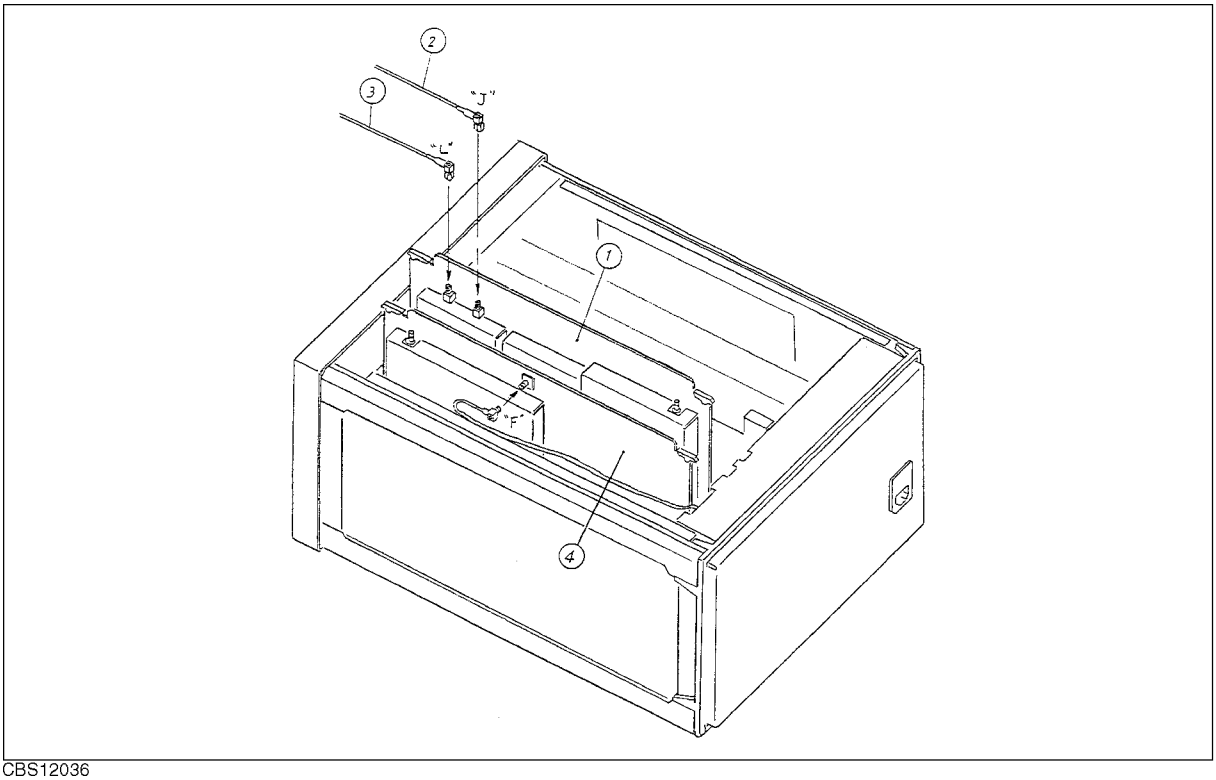
CBS12035

Figure 12-34. Main Frame Assembly Parts 15/19 (A2 Post Regulator Assembly)

Table 12-36.
Main Frame Assembly Parts 15/19 (A2 Post Regulator Assembly)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-66522	0	1	A2 Post Regulator	28480	04396-66522
2	04396-61674	3	1	WIRE ASSY	28480	04396-61674
3	0515-1550	0	3	SCR M3-L 8 P-H	28480	0515-1550

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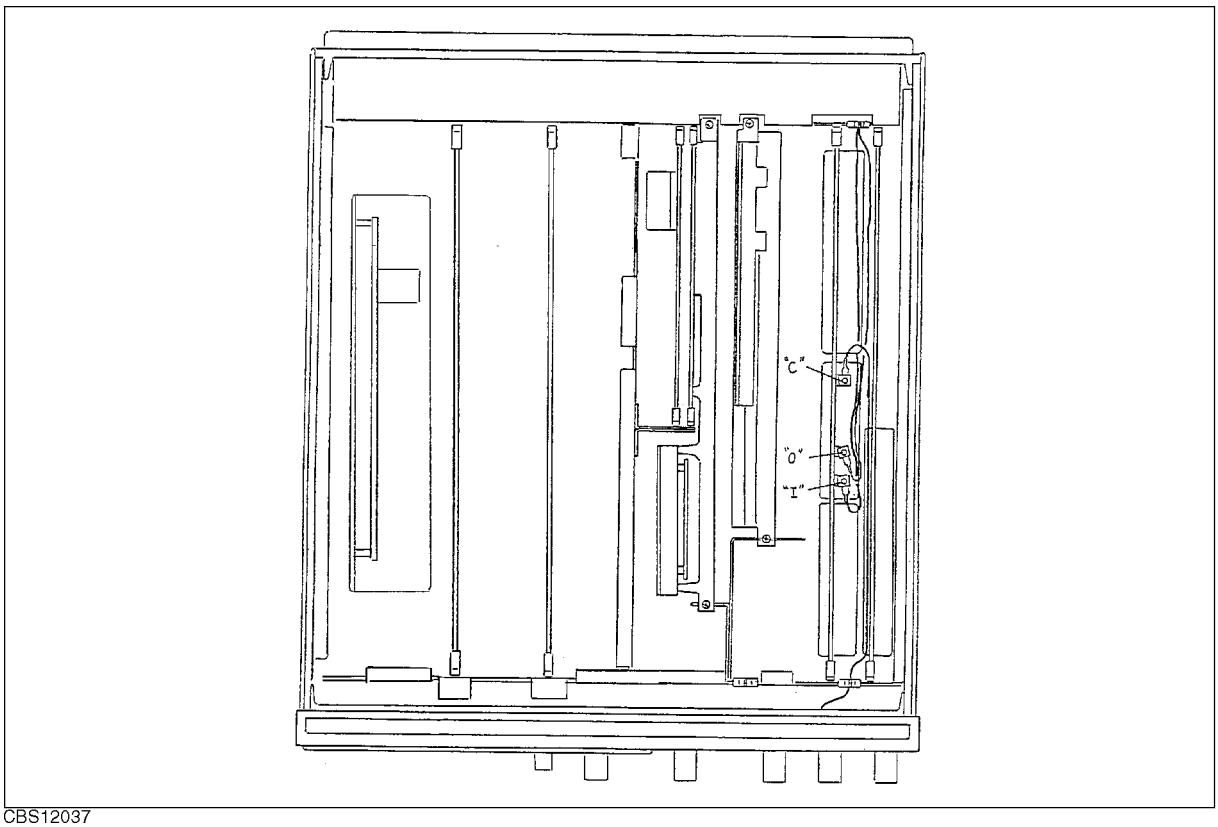
CBS12036

Figure 12-35. Main Frame Assembly Parts 16/19 (A5 and A6 Assemblies)

Table 12-37. Main Frame Assembly Parts 16/19 (A5 and A6 Assemblies)

Ref. Desig.	Agilent Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-66505	9	1	A5 Synthesizer	28480	04396-66505
2	04396-61625	4	1	RF CBL ASSY	28480	04396-61625
3	04396-61624	3	1	RF CBL ASSY	28480	04396-61624
4	04396-66506	0	1	A6 Receiver IF	28480	04396-66506

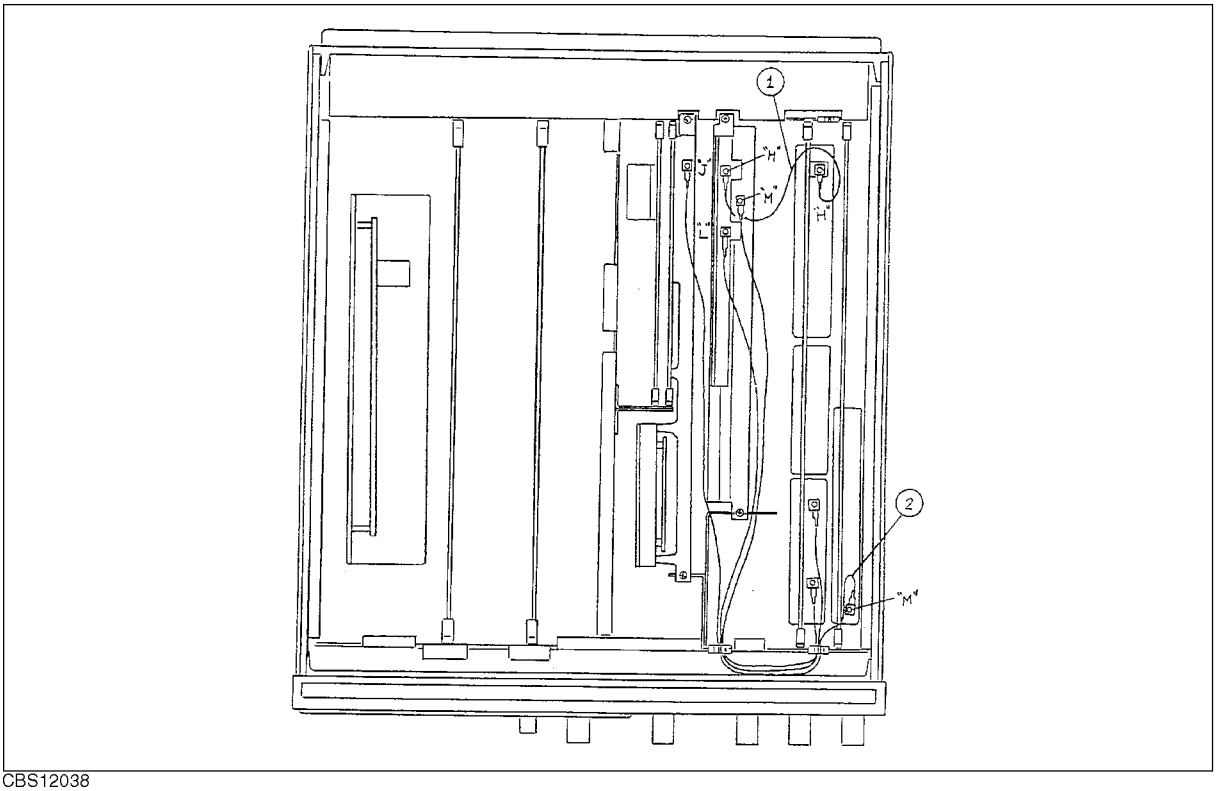
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CBS12037

Figure 12-36. Main Frame Assembly Parts 17/19

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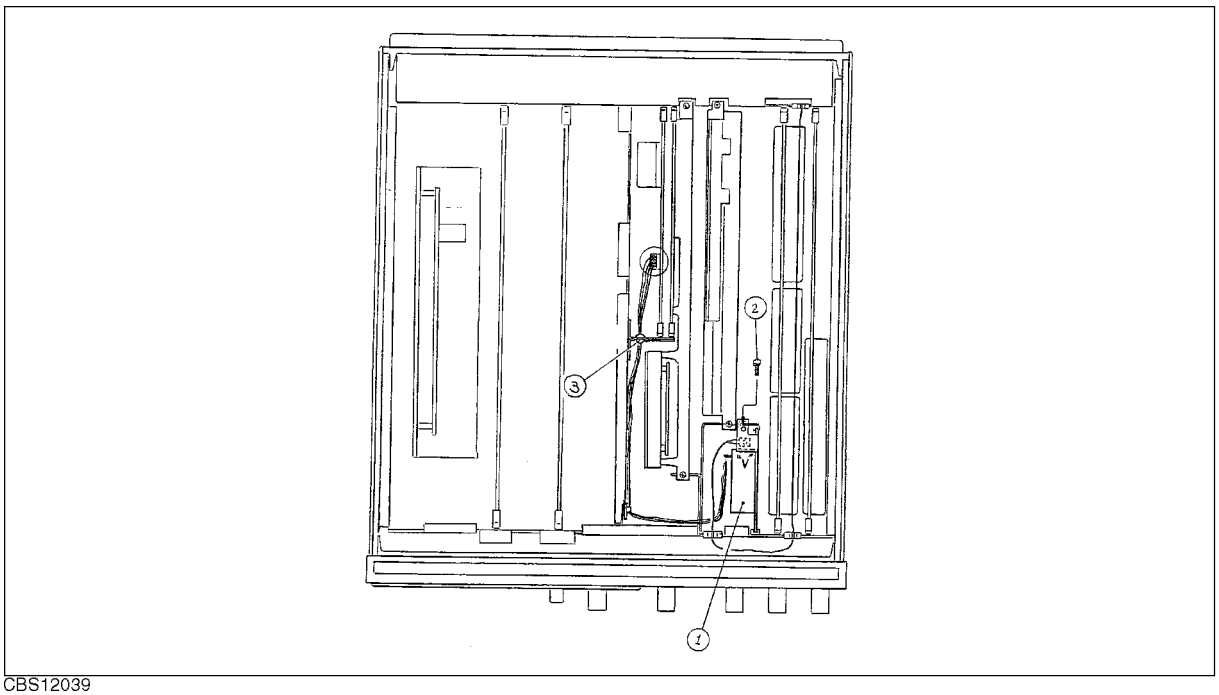
CBS12038

Figure 12-37. Main Frame Assembly Parts 18/19 (RF Cable Assemblies)

Table 12-38. Main Frame Assembly Parts 18/19 (RF Cable Assemblies)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61623	2	1	RF CBL ASSY	28480	04396-61623
2	04396-61626	5	1	RF CBL ASSY	28480	04396-61626

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CBS12039

Figure 12-38. Main Frame Assembly Parts 19/19 (Option 1D5)

Table 12-39. Main Frame Assembly Parts 19/19 (Option 1D5)

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-61060	1		A60 Freq Reference (opt.1D5)	28480	
2	0515-1550	0	1	SCR M3-L 8 P-H	28480	0515-1550
3	0400-0203	5	1	GROMMET-RND	28480	0400-0203

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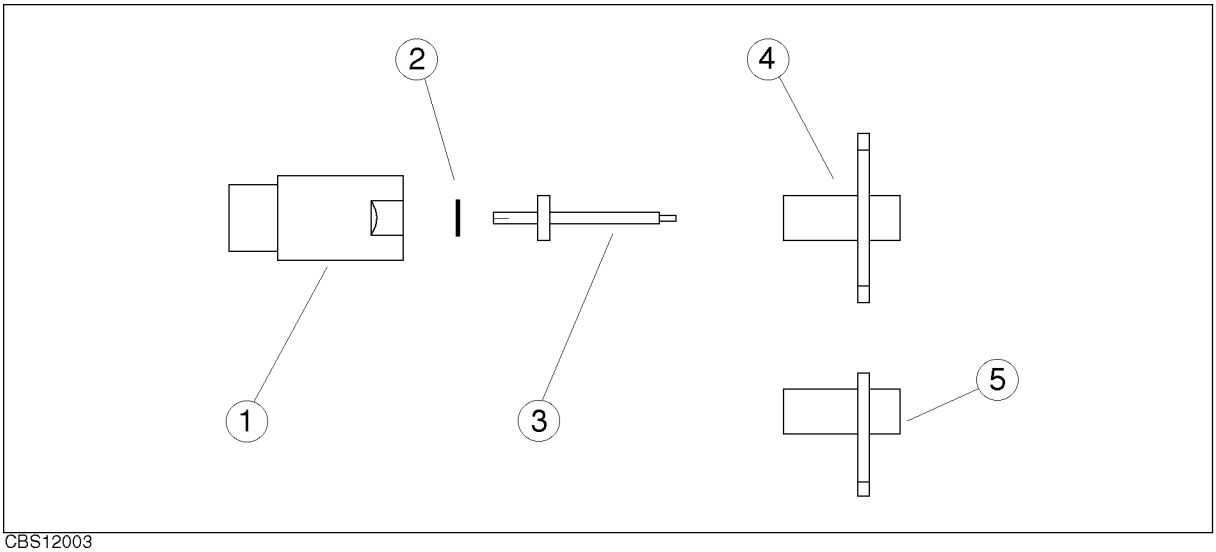


Figure 12-39. A9 N Type Connector Replacement

Table 12-40. A9 N Type Connector Replacement

Ref. Desig.	Agilent Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1250-0914		1	Outer Conducter	28480	1250-0914
2	08742-0006		1	Spacer	28480	08742-0006
3	04396-60002		1	Center Conducter	28480	04396-60002
4	04396-21001		1	Flange	28480	04396-21001
5	04396-21002		1	Flange	28480	04396-21002

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13

Post Repair Procedures

INTRODUCTION

This chapter lists the procedures required to verify the analyzer operation after an assembly is replaced with a new one.

POST REPAIR PROCEDURES

Table 13-1 *Post Repair Procedures* lists the required procedures that must be performed after the replacement of an assembly or the EEPROM. These are the recommended minimum procedures to ensure that the analyzer is working properly following the replacement.

When you replace an assembly or the EEPROM on the A1 CPU, perform the adjustments and updating correction constants (CC) listed in Table 13-1. Then perform the operational verifications and performance verifications listed in Table 13-1.

For the detailed procedure of the adjustments and updating correction constants, see the *Adjustments and Correction Constants* chapter. For the detailed operational verification procedures, see this manual's chapter specified in Table 13-1. For the detailed performance verification procedures, see the *Performance Test Manual* (p/n 04396-90120).

Table 13-1. Post Repair Procedures

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A1 CPU	Firmware Installation.[1]	*INSPECT THE POWER ON SEQUENCE* [2] *OPERATOR'S CHECK* [2] Internal Test 2: A1 VOLATILE MEMORY[3]
A1 EEPROM	 Step Pretune CC RF OUT Level CC Crystal Filter CC IF Gain Error CC Spectrum Analyzer Absolute Magnitude CC Network Analyzer Absolute Magnitude CC Network Analyzer Magnitude Ratio/Phase CC	*INSPECT THE POWER ON SEQUENCE* [2] *OPERATOR'S CHECK* [2] Source Level/Flatness Power Sweep Linearity Absolute Amplitude Accuracy Magnitude Ratio/Phase Frequency Response Resolution Bandwidth Switching Uncertainty IF Gain Switching Uncertainty Frequency Response

1 See the *Firmware Installation* procedure in this chapter.

2 See the *Troubleshooting* chapter.

3 See the *Service Key Menus* chapter.

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Table 13-1. Post Repair Procedures (continued)

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A2 Post-Regulator A50 DC-DC Converter	CAL OUT Level DC Offset and Hold Step	*INSPECT THE POWER ON SEQUENCE* [1] Frequency Accuracy Source Level Accuracy/Flatness Absolute Amplitude Accuracy Calibrator Amplitude Accuracy Frequency Response
A3A1 ALC	RF OUT Level CC	*INSPECT THE POWER ON SEQUENCE* [1] *OPERATOR'S CHECK* [1] Source Level Accuracy/Flatness Non-Sweep Power Linearity Power Sweep Linearity Harmonics/Non-Harmonic Spurious Input Crosstalk Other Spurious Residual Response
A3A2 2nd LO	Second LO PLL Lock Source Mixer Local Leakage RF OUT Level CC Spectrum Analyzer Absolute Magnitude CC Network Analyzer Absolute Magnitude CC	*INSPECT THE POWER ON SEQUENCE* [1] *OPERATOR'S CHECK* [1] Source Level Accuracy/Flatness Non-Sweep Power Linearity Power Sweep Linearity Harmonics/Non-Harmonic Spurious Input Crosstalk Absolute Amplitude Accuracy Noise Sideband Frequency Response Other Spurious Residual Response
A3A3 Source	RF OUT Level CC	*INSPECT THE POWER ON SEQUENCE* [1] *OPERATOR'S CHECK* [1] Source Level Accuracy/Flatness Non-Sweep Power Linearity Power Sweep Linearity Harmonics/Non-Harmonic Spurious Input Crosstalk

1 See the *Troubleshooting* chapter.

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Table 13-1. Post Repair Procedures (continued)

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A4 1st LO/Receiver RF	Final Gain RF OUT Level CC Spectrum Analyzer Absolute Magnitude CC Network Analyzer Absolute Magnitude CC Network Analyzer Magnitude Ratio/Phase CC	*INSPECT THE POWER ON SEQUENCE* [1] *OPERATOR'S CHECK* [1] Source Level Accuracy/Flatness Power Sweep Linearity Receiver Noise Level Input Crosstalk Absolute Amplitude Accuracy Magnitude Ratio/Phase Dynamic Accuracy Magnitude Ratio/Phase Frequency Response Displayed Average Noise Level Noise Sideband Frequency Response 2nd Harmonic Distortion 3rd Order Intermodulation Distortion Other Spurious Residual Response
A5 Synthesizer	40 MHz Reference Oscillator Frequency 520 MHz Level CAL OUT Level Comb Generator Step Pretune CC	*INSPECT THE POWER ON SEQUENCE* [1] *OPERATOR'S CHECK* [1] Internal Test 8: A5 STEP OSC Frequency Accuracy Calibrator Amplitude Accuracy Noise Sideband Other Spurious Residual Response
A6 Receiver IF	DC Offset and Hold Step 0°/90° Tracking Band Pass Filters Final Gain Crystal Filter CC IF Gain Errors CC Spectrum Analyzer Absolute Magnitude CC Network Analyzer Absolute Magnitude CC	*INSPECT THE POWER ON SEQUENCE* [1] *OPERATOR'S CHECK* [1] Receiver Noise Level Absolute Amplitude Accuracy Magnitude Ratio/Phase Dynamic Accuracy Magnitude Ratio/Phase Frequency Response Displayed Average Noise Level Amplitude Fidelity Resolution Bandwidth Accuracy/Selectivity Resolution Bandwidth Switching Uncertainty IF Gain Switching Uncertainty Noise Sideband Frequency Response 2nd Harmonic Distortion 3rd Order Intermodulation Distortion Other Spurious Residual Response

1 See the *Troubleshooting* chapter.

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Table 13-1. Post Repair Procedures (continued)

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A7 Output Attenuator	RF OUT Level CC	*INSPECT THE POWER ON SEQUENCE*[1] *OPERATOR'S CHECK*[1] Source Level Accuracy/Flatness Non-Sweep Power Linearity
A8 Input Attenuator	Final Gain Spectrum Analyzer Absolute Magnitude CC	*INSPECT THE POWER ON SEQUENCE*[1] *OPERATOR'S CHECK*[1] Input Attenuator Switching Uncertainty Frequency Response
A9 Input Multiplexer	Spectrum Analyzer Absolute Magnitude CC Network Analyzer Absolute Magnitude CC Network Analyzer Magnitude Ratio/Phase CC	*INSPECT THE POWER ON SEQUENCE*[1] *OPERATOR'S CHECK*[1] Receiver Noise Level Input Crosstalk Input Impedance Absolute Amplitude Accuracy Magnitude Ratio/Phase Dynamic Accuracy Magnitude Ratio/Phase Frequency Response
A20 MOTHERBOARD	None	*INSPECT THE POWER ON SEQUENCE*[1] *OPERATOR'S CHECK*[1]
A30 Keyboard	None	*INSPECT THE POWER ON SEQUENCE*[1] External Test 17: FRONT PANEL DIAG.[2]
A31 I/O Connector	None None	*INSPECT THE POWER ON SEQUENCE*[1] *TROUBLESHOOT GPIB SYSTEM*[1] *Inspect the Test Set*[3]
A32 I-BASIC Interface	None None	*INSPECT THE POWER ON SEQUENCE*[1] *Check the A32 I-BASIC Interface and mini DIN Key board*[4]
A40 Pre-Regulator	None	Internal Test 4: A2 POST REGULATOR[5]
A51 GSP	Display Background	*INSPECT THE POWER ON SEQUENCE*[1]
A52 LCD	None	*INSPECT THE POWER ON SEQUENCE*[1]
A53 FDD	None	*INSPECT THE POWER ON SEQUENCE*[1] External Test 18: DSK DR FAULTY ISOLN[5]
A60 High Stability Frequency Reference	10 MHz Reference Oscillator Frequency	*INSPECT THE POWER ON SEQUENCE*[1] Frequency Accuracy

1 See the *Troubleshooting* chapter.

2 See the *Service Key Menus* chapter.

3 See the *Accessories Troubleshooting* chapter.

4 See the *Digital Control Troubleshooting* chapter.

5 See the *Service Key Menus* chapter.

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A

Manual Changes

Introduction

This appendix contains the information required to adapt this manual to earlier versions or configurations of the analyzer than the current printing date of this manual. The information in this manual applies directly to the 4396B Network/Spectrum Analyzer serial number prefix listed on the title page of this manual.

Manual Changes

To adapt this manual to your 4396B, see Table A-1 and Table A-2, and make all the manual changes listed opposite your instrument's serial number and firmware version.

Instruments manufactured after the printing of this manual may be different from those documented in this manual. Later instrument versions will be documented in a manual changes supplement that will accompany the manual shipped with that instrument. If your instrument's serial number is not listed on the title page of this manual or in Table A-1, it may be documented in a *yellow MANUAL CHANGES* supplement.

In additions to change information, the supplement may contain information for correcting errors (Errata) in the manual. To keep this manual as current and accurate as possible, Agilent Technologies recommends that you periodically request the latest *MANUAL CHANGES* supplement.

For information concerning serial number prefixes not listed on the title page or in the *MANUAL CHANGE* supplement, contact the nearest Agilent Technologies office.

Turn on the line switch or execute the `*IDN?` command by GPIB to confirm the firmware version. See the *GPIB Command Reference* manual for information on the `*IDN?` command.

Table A-1. Manual Changes by Serial Number

Serial Prefix or Number	Make Manual Changes
JP1KE	

Table A-2. Manual Changes by Firmware Version

Version	Make Manual Changes

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Serial Number

Agilent Technologies uses a two-part, nine-character serial number that is stamped on the serial number plate (see Figure A-1) attached to the rear panel. The first four digits and the letter are the serial prefix and the last five digits are the suffix.

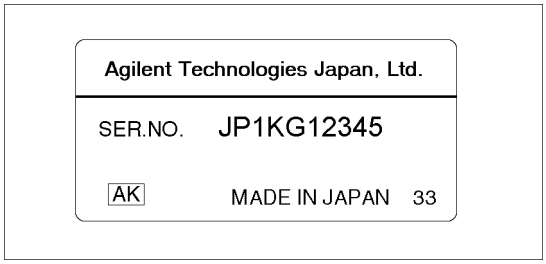


Figure A-1. Serial Number Plate

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B

A20 Motherboard Pin Assignment

This appendix provides the information about the A20 motherboard pin assignment on the circuit side, and signal name description. Figure B-1 and Figure B-2 show the A20 motherboard pin assignments. Table B-1 lists the signal names in alphabetical order.

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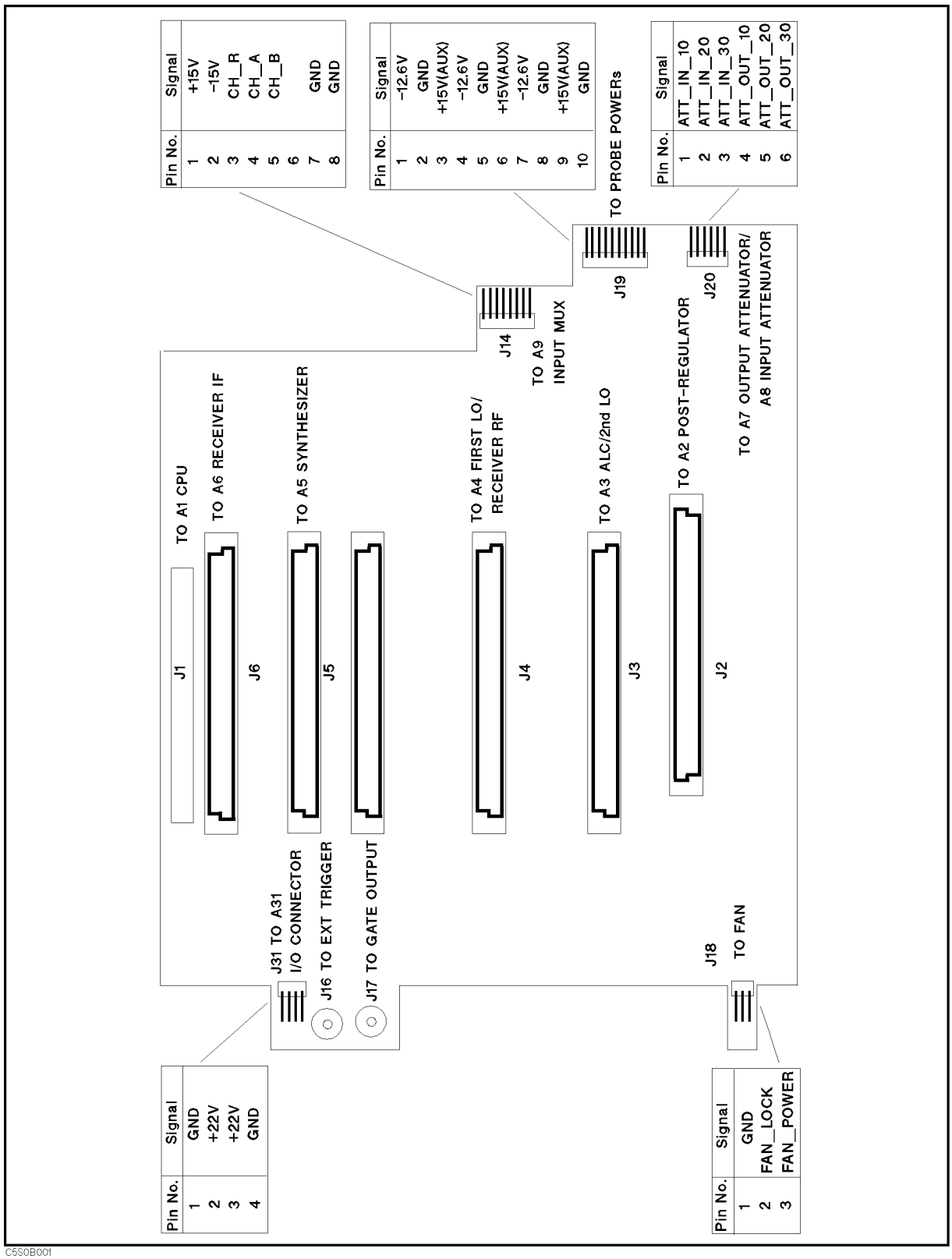
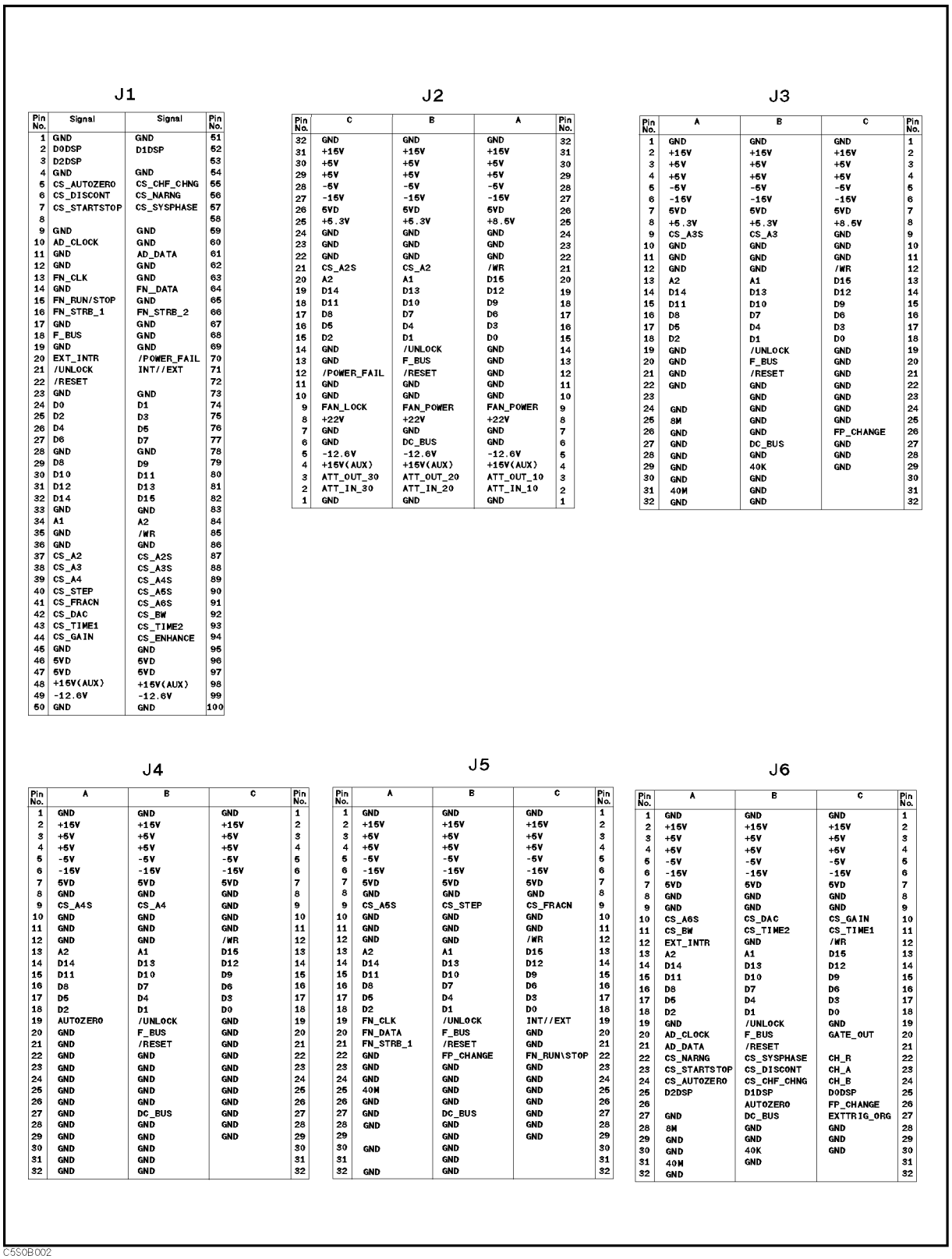


Figure B-1. Connector Locations On the A20 Motherboard Circuit Side

B-2 A20 Motherboard Pin Assignment

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J1

Pin No.	Signal	Signal	Pin No.
1	GND	GND	51
2	D0DSP	D1DSP	52
3	D2DSP		53
4	GND	GND	54
5	CS_AUTOZERO	CS_CHF_CHNG	55
6	CS_DISCONT	CS_NARNG	56
7	CS_STARTSTOP	CS_SYSPHASE	57
8			58
9	GND	GND	59
10	AD_CLOCK	GND	60
11	GND	AD_DATA	61
12	GND	GND	62
13	FN_CLK	GND	63
14	GND	FN_DATA	64
15	FN_RUN/STOP	GND	65
16	FN_STRB_1	FN_STRB_2	66
17	GND	GND	67
18	F_BUS	GND	68
19	GND	GND	69
20	EXT_INTR	/POWER_FAIL	70
21	/UNLOCK	INT//EXT	71
22	/RESET		72
23	GND	GND	73
24	D0	D1	74
25	D2	D3	75
26	D4	D5	76
27	D6	D7	77
28	GND	GND	78
29	D8	D9	79
30	D10	D11	80
31	D12	D13	81
32	D14	D15	82
33	GND	GND	83
34	A1	A2	84
35	GND	/WR	85
36	GND	GND	86
37	CS_A2	CS_A2S	87
38	CS_A3	CS_A3S	88
39	CS_A4	CS_A4S	89
40	CS_STEP	CS_A5S	90
41	CS_FRACN	CS_A6S	91
42	CS_DAC	CS_BW	92
43	CS_TIME1	CS_TIME2	93
44	CS_GAIN	CS_ENHANCE	94
45	GND	GND	95
46	5VD	5VD	96
47	5VD	5VD	97
48	+15V(AUX)	+15V(AUX)	98
49	-12.6V	-12.6V	99
50	GND	GND	100

J2

Pin No.	C	B	A	Pin No.
32	GND	GND	GND	32
31	+15V	+15V	+15V	31
30	+5V	+5V	+5V	30
29	+5V	+5V	+5V	29
28	-5V	-5V	-5V	28
27	-15V	-15V	-15V	27
26	5VD	5VD	5VD	26
25	+5.3V	+5.3V	+8.5V	25
24	GND	GND	GND	24
23	GND	GND	GND	23
22	GND	GND	GND	22
21	CS_A2S	CS_A2	/WR	21
20	A2	A1	D15	20
19	D14	D13	D12	19
18	D11	D10	D9	18
17	D8	D7	D6	17
16	D5	D4	D3	16
15	D2	D1	D0	15
14	GND	/UNLOCK	GND	14
13	GND	F_BUS	GND	13
12	/POWER_FAIL	/RESET	GND	12
11	GND	GND	GND	11
10	GND	GND	GND	10
9	FAN_LOCK	FAN_POWER	FAN_POWER	9
8	+22V	+22V	+22V	8
7	GND	GND	GND	7
6	GND	DC_BUS	GND	6
5	-12.6V	-12.6V	-12.6V	5
4	+15V(AUX)	+15V(AUX)	+15V(AUX)	4
3	ATT_OUT_30	ATT_OUT_20	ATT_OUT_10	3
2	ATT_IN_30	ATT_IN_20	ATT_IN_10	2
1	GND	GND	GND	1

J3

Pin No.	A	B	C	Pin No.
1	GND	GND	GND	1
2	+15V	+15V	+15V	2
3	+5V	+5V	+5V	3
4	+5V	+5V	+5V	4
5	-5V	-5V	-5V	5
6	-15V	-15V	-15V	6
7	5VD	5VD	5VD	7
8	+5.3V	+5.3V	+8.5V	8
9	CS_A3S	CS_A3	GND	9
10	GND	GND	GND	10
11	GND	GND	GND	11
12	GND	GND	/WR	12
13	A2	A1	D15	13
14	D14	D13	D12	14
15	D11	D10	D9	15
16	D8	D7	D6	16
17	D5	D4	D3	17
18	D2	D1	D0	18
19	GND	/UNLOCK	GND	19
20	GND	F_BUS	GND	20
21	GND	/RESET	GND	21
22	GND	GND	GND	22
23		GND	GND	23
24	GND	GND	GND	24
25	8M	GND	GND	25
26	GND	GND	FP_CHANGE	26
27	GND	DC_BUS	GND	27
28	GND	GND	GND	28
29	GND	40K	GND	29
30	GND	GND		30
31	40M	GND		31
32	GND	GND		32

J4

Pin No.	A	B	C	Pin No.
1	GND	GND	GND	1
2	+15V	+15V	+15V	2
3	+5V	+5V	+5V	3
4	+5V	+5V	+5V	4
5	-5V	-5V	-5V	5
6	-15V	-15V	-15V	6
7	5VD	5VD	5VD	7
8	GND	GND	GND	8
9	CS_A4S	CS_A4	GND	9
10	GND	GND	GND	10
11	GND	GND	GND	11
12	GND	GND	/WR	12
13	A2	A1	D15	13
14	D14	D13	D12	14
15	D11	D10	D9	15
16	D8	D7	D6	16
17	D5	D4	D3	17
18	D2	D1	D0	18
19	AUTOZERO	/UNLOCK	GND	19
20	GND	F_BUS	GND	20
21	GND	/RESET	GND	21
22	GND	GND	GND	22
23	GND	GND	GND	23
24	GND	GND	GND	24
25	GND	GND	GND	25
26	GND	GND	GND	26
27	GND	DC_BUS	GND	27
28	GND	GND	GND	28
29	GND	GND	GND	29
30	GND	GND		30
31	GND	GND		31
32	GND	GND		32

J5

Pin No.	A	B	C	Pin No.
1	GND	GND	GND	1
2	+15V	+15V	+15V	2
3	+5V	+5V	+5V	3
4	+5V	+5V	+5V	4
5	-5V	-5V	-5V	5
6	-15V	-15V	-15V	6
7	5VD	5VD	5VD	7
8	GND	GND	GND	8
9	CS_A5S	CS_STEP	CS_FRACN	9
10	GND	GND	GND	10
11	GND	GND	GND	11
12	GND	GND	/WR	12
13	A2	A1	D15	13
14	D14	D13	D12	14
15	D11	D10	D9	15
16	D8	D7	D6	16
17	D5	D4	D3	17
18	D2	D1	D0	18
19	FN_CLK	/UNLOCK	INT//EXT	19
20	FN_DATA	F_BUS	GND	20
21	FN_STRB_1	/RESET	GND	21
22	GND	FP_CHANGE	FN_RUN\STOP	22
23	GND	GND	GND	23
24	GND	GND	GND	24
25	40M	GND	GND	25
26	GND	GND	GND	26
27	GND	DC_BUS	GND	27
28	GND	GND	GND	28
29		GND	GND	29
30	GND	GND		30
31		GND		31
32	GND	GND		32

J6

Pin No.	A	B	C	Pin No.
1	GND	GND	GND	1
2	+15V	+15V	+15V	2
3	+5V	+5V	+5V	3
4	+5V	+5V	+5V	4
5	-5V	-5V	-5V	5
6	-15V	-15V	-15V	6
7	5VD	5VD	5VD	7
8	GND	GND	GND	8
9	GND	GND	GND	9
10	CS_A6S	CS_DAC	CS_GAIN	10
11	CS_BW	CS_TIME2	CS_TIME1	11
12	EXT_INTR	GND	/WR	12
13	A2	A1	D15	13
14	D14	D13	D12	14
15	D11	D10	D9	15
16	D8	D7	D6	16
17	D5	D4	D3	17
18	D2	D1	D0	18
19	GND	/UNLOCK	GND	19
20	AD_CLOCK	F_BUS	GATE_OUT	20
21	AD_DATA	/RESET		21
22	CS_NARNG	CS_SYSPHASE	CH_R	22
23	CS_STARTSTOP	CS_DISCONT	CH_A	23
24	CS_AUTOZERO	CS_CHF_CHNG	CH_B	24
25	D2DSP	D1DSP	D0DSP	25
26		AUTOZERO	FP_CHANGE	26
27	GND	DC_BUS	EXTTRIG_ORG	27
28	8M	GND	GND	28
29	GND	GND	GND	29
30	GND	40K	GND	30
31	40M	GND		31
32	GND			32

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Figure B-2. Pin Assignment On the A20 Motherboard Circuit Side

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Table B-1. Signal Name

Mnemonic	Description	Pin Assignment
+15V	+15 V Power Line	J14-1,J2-A31,J2-B31,J2-C31,J3-A2,J3-B2,J3-C2,J4-A2 ,J4-B2,J4-C2,J5-A2,J5-B2,J5-C2,J6-A2,J6-B2,J6-C2 ,J8-A2,J8-B2,J8-C2
+15V(AUX)	+15 V (AUX) Power Line	J1-48,J1-98,J19-3,J19-6,J19-9,J2-A4,J2-B4,J2-C4
+22V	+22 V Power Line	J2-A8,J2-B8,J2-C8,J31-2,J31-3
+5.3V	+5.3 V Power Line	J2-B25,J2-C25,J3-A8,J3-B8
+5V	+5 V Power Line	J2-A29,J2-A30,J2-B29,J2-B30,J2-C29,J2-C30,J3-A3 ,J3-A4,J3-B3,J3-B4,J3-C3,J3-C4,J4-A3,J4-A4,J4-B3 ,J4-B4,J4-C3,J4-C4,J5-A3,J5-A4,J5-B3,J5-B4,J5-C3 ,J5-C4,J6-A3,J6-A4,J6-B3,J6-B4,J6-C3,J6-C4,J8-A3 ,J8-A4,J8-B3,J8-B4,J8-C3,J8-C4
+8.5V	+8.5 V Power Line	J2-A25,J3-C8
–12.6V	–12.6 V Power Line	J1-49,J1-99,J19-1,J19-4,J19-7,J2-A5,J2-B5,J2-C5
–15V	–15 V Power Line	J14-2,J2-A27,J2-B27,J2-C27,J3-A6,J3-B6,J3-C6,J4-A6 ,J4-B6,J4-C6,J5-A6,J5-B6,J5-C6,J6-A6,J6-B6,J6-C6 ,J8-A6,J8-B6,J8-C6
–5V	–5 V Power Line	J2-A28,J2-B28,J2-C28,J3-A5,J3-B5,J3-C5,J4-A5,J4-B5 ,J4-C5,J5-A5,J5-B5,J5-C5,J6-A5,J6-B5,J6-C5,J8-A5 ,J8-B5,J8-C5
/POWER_FAIL	Power Failure Interrupt	J1-70,J2-C12
/RESET	A1 CPU Reset	J1-22,J2-B12,J3-B21,J4-B21,J5-B21,J6-B21,J8-B21
/UNLOCK	Phase Lock Loop Unlocked	J1-21,J2-B14,J3-B19,J4-B19,J5-B19,J6-B19,J8-B19
/WR	Write Enable	J1-85,J2-A21,J3-C12,J4-C12,J5-C12,J6-C12,J8-C12
40K	40 kHz Frequency Reference	J3-B29,J6-B30
40M	40 MHz Frequency Reference	J3-A31,J5-A25,J6-A31,J8-A25
5VD	+5 V Digital Power Line	J1-46,J1-47,J1-96,J1-97,J2-A26,J2-B26,J2-C26,J3-A7 ,J3-B7,J3-C7,J4-A7,J4-B7,J4-C7,J5-A7,J5-B7,J5-C7 ,J6-A7,J6-B7,J6-C7,J8-A7,J8-B7,J8-C7
8M	8 MHz Frequency Reference	J3-A25,J6-A28
GND	Ground	J1-100,J1-11,J1-12,J1-14,J1-17,J1-19,J1-1,J1-23 ,J1-28,J1-33,J1-35,J1-36,J1-45,J1-4,J1-50,J1-51 ,J1-54,J1-59,J1-60,J1-62,J1-63,J1-65,J1-67,J1-68 ,J1-69,J1-73,J1-78,J1-83,J1-86,J1-95,J1-9,J14-7 ,J14-8,J16-2,J19-10,J19-2,J19-5,J19-8,J2-A11 ,J2-A12,J2-A13,J2-A14,J2-A1,J2-A22,J2-A23,J2-A24 ,J2-A32,J2-A6,J2-A7,J2-A9,J2-B11,J2-B1,J2-B22 ,J2-B23,J2-B24,J2-B32,J2-B7,J2-C11,J2-C13,J2-C14 ,J2-C1,J2-C22,J2-C23,J2-C24,J2-C32,J2-C6,J2-C7 ,J3-A10,J3-A11,J3-A12,J3-A19,J3-A1,J3-A20,J3-A21 ,J3-A22,J3-A24,J3-A26,J3-A27,J3-A28,J3-A29,J3-A30 ,J3-A32,J3-B10,J3-B11,J3-B12,J3-B1,J3-B22,J3-B23 ,J3-B24,J3-B25,J3-B26,J3-B28,J3-B30,J3-B31,J3-B32 ,J3-C10,J3-C11,J3-C19,J3-C1,J3-C20,J3-C21,J3-C22 ,J3-C23,J3-C24,J3-C25,J3-C27,J3-C28,J3-C29,J3-C9 ,J31-1,J31-4,J4-A10,J4-A11,J4-A12,J4-A1,J4-A20 ,J4-A21,J4-A22,J4-A23,J4-A24,J4-A25,J4-A26,J4-A27 ,J4-A28,J4-A29,J4-A30,J4-A31,J4-A32,J4-A8,J4-B10 ,J4-B11,J4-B12,J4-B1,J4-B22,J4-B23,J4-B24,J4-B25 ,J4-B26,J4-B28,J4-B29,J4-B30,J4-B31,J4-B32,J4-B8 ,J4-C10,J4-C11,J4-C19,J4-C1,J4-C20,J4-C21,J4-C22 ,J4-C23,J4-C24,J4-C25,J4-C26,J4-C27,J4-C28,J4-C29

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Table B-1. Signal Name (continued)

Mnemonic	Description	Pin Assignment
GND	Ground (continued)	,J4-C8,J4-C9,J5-A10,J5-A11,J5-A12,J5-A1,J5-A22 ,J5-A23,J5-A24,J5-A26,J5-A27,J5-A28,J5-A30,J5-A32 ,J5-A8,J5-B10,J5-B11,J5-B12,J5-B1,J5-B23,J5-B24 ,J5-B25,J5-B26,J5-B28,J5-B29,J5-B30,J5-B31,J5-B32 ,J5-B8,J5-C10,J5-C11,J5-C1,J5-C20,J5-C21,J5-C23 ,J5-C24,J5-C25,J5-C26,J5-C27,J5-C28,J5-C29,J5-C8 ,J6-A19,J6-A1,J6-A27,J6-A29,J6-A30,J6-A32,J6-A8 ,J6-A9,J6-B12,J6-B1,J6-B28,J6-B29,J6-B31,J6-B8 ,J6-B9,J6-C19,J6-C1,J6-C28,J6-C29,J6-C30,J6-C8 ,J6-C9,J7-2,J8-A10,J8-A11,J8-A12,J8-A1,J8-A22 ,J8-A23,J8-A24,J8-A26,J8-A27,J8-A28,J8-A29,J8-A30 ,J8-A31,J8-A32,J8-A8,J8-A9,J8-B10,J8-B11,J8-B12 ,J8-B1,J8-B23,J8-B24,J8-B25,J8-B26,J8-B28,J8-B29 ,J8-B30,J8-B31,J8-B32,J8-B8,J8-B9,J8-C11,J8-C19 ,J8-C1,J8-C20,J8-C21,J8-C23,J8-C24,J8-C25,J8-C26 ,J8-C27,J8-C28,J8-C29,J8-C8,J8-C9
A1	Address Bus (Bit 1)	J1-34,J2-B20,J3-B13,J4-B13,J5-B13,J6-B13,J8-B13
A2	Address Bus (Bit 2)	J1-84,J2-C20,J3-A13,J4-A13,J5-A13,J6-A13,J8-A13
AD_CLOCK	A/D Sync Clock	J1-10,J6-A20
AD_DATA	A/D Serial Data	J1-61,J6-A21
ATT_IN_10	Input Attenuator 10 dB Select	J2-A2,J20-1
ATT_IN_20	Input Attenuator 20 dB Select	J2-B2,J20-2
ATT_IN_30	Input Attenuator 30 dB Select	J2-C2,J20-3
ATT_OUT_10	Output Attenuator 10 dB Select	J2-A3,J20-4
ATT_OUT_20	Output Attenuator 20 dB Select	J2-B3,J20-5
ATT_OUT_30	Output Attenuator 30 dB Select	J2-C3,J20-6
AUTOZERO	Auto Zero Control	J4-A19,J6-B26
CH_A	A Input Select	J14-4,J6-C23
CH_B	B Input Select	J14-5,J6-C24
CH_R	R Input Select	J14-3,J6-C22
CS_A2	A2 Register Select	J1-37,J2-B21
CS_A2S	A2 Reg. Select for Service Modes	J1-87,J2-C21
CS_A3	A3 Register Select	J1-38,J3-B9
CS_A3S	A3 Reg. Select for Service Modes	J1-88,J3-A9
CS_A4	A4 Register Select	J1-39,J4-B9
CS_A4S	A4 Reg. Select for Service Modes	J1-89,J4-A9
CS_A5S	A5 Reg. Select for Service Modes	J1-90,J5-A9
CS_A6S	A6 Reg. Select for Service Modes	J1-91,J6-A10
CS_AUTOZERO	Auto Zero Select	J1-5,J6-A24
CS_BW	Bandwidth Register Select	J1-92,J6-A11
CS_CHF_CHNG	Channel/Frequency Change	J1-55,J6-B24
CS_DAC	DAC Select	J1-42,J6-B10
CS_DISCONT	Discontinue Sense	J1-6,J6-B23
CS_ENHANCE	Enhance Board Register Select	J1-94,J8-C10

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Table B-1. Signal Name (continued)

Mnemonic	Description	Pin Assignment
CS_FRACN	Fractional N Register Select	J1-41,J5-C9
CS_GAIN	Gain Register Select	J1-44,J6-C10
CS_NARNG	Ranging Register Select	J1-56,J6-A22
CS_STARTSTOP	Sequencer Start/Stop Control	J1-7,J6-A23
CS_STEP	Step Register Select	J1-40,J5-B9
CS_SYSPHASE	System Phase Register Read	J1-57,J6-B22
CS_TIME1	Timer 1 Select	J1-43,J6-C11
CS_TIME2	Timer 2 Select	J1-93,J6-B11
D0	Data Bus (Bit 0)	J1-24,J2-A15,J3-C18,J4-C18,J5-C18,J6-C18,J8-C18
D0DSP	Data Bus (Bit 0) from DSP	J1-2,J6-C25
D1	Data Bus (Bit 1)	J1-74,J2-B15,J3-B18,J4-B18,J5-B18,J6-B18,J8-B18
D10	Data Bus (Bit 10)	J1-30,J2-B18,J3-B15,J4-B15,J5-B15,J6-B15,J8-B15
D11	Data Bus (Bit 11)	J1-80,J2-C18,J3-A15,J4-A15,J5-A15,J6-A15,J8-A15
D12	Data Bus (Bit 12)	J1-31,J2-A19,J3-C14,J4-C14,J5-C14,J6-C14,J8-C14
D13	Data Bus (Bit 13)	J1-81,J2-B19,J3-B14,J4-B14,J5-B14,J6-B14,J8-B14
D14	Data Bus (Bit 14)	J1-32,J2-C19,J3-A14,J4-A14,J5-A14,J6-A14,J8-A14
D15	Data Bus (Bit 15)	J1-82,J2-A20,J3-C13,J4-C13,J5-C13,J6-C13,J8-C13
D1DSP	Data Bus (Bit 1) from DSP	J1-52,J6-B25
D2	Data Bus (Bit 2)	J1-25,J2-C15,J3-A18,J4-A18,J5-A18,J6-A18,J8-A18
D2DSP	Data Bus (Bit 2) from DSP	J1-3,J6-A25
D3	Data Bus (Bit 3)	J1-75,J2-A16,J3-C17,J4-C17,J5-C17,J6-C17,J8-C17
D4	Data Bus (Bit 4)	J1-26,J2-B16,J3-B17,J4-B17,J5-B17,J6-B17,J8-B17
D5	Data Bus (Bit 5)	J1-76,J2-C16,J3-A17,J4-A17,J5-A17,J6-A17,J8-A17
D6	Data Bus (Bit 6)	J1-27,J2-A17,J3-C16,J4-C16,J5-C16,J6-C16,J8-C16
D7	Data Bus (Bit 7)	J1-77,J2-B17,J3-B16,J4-B16,J5-B16,J6-B16,J8-B16
D8	Data Bus (Bit 8)	J1-29,J2-C17,J3-A16,J4-A16,J5-A16,J6-A16,J8-A16
D9	Data Bus (Bit 9)	J1-79,J2-A18,J3-C15,J4-C15,J5-C15,J6-C15,J8-C15
DC_BUS	DC Bus	J2-B6,J3-B27,J4-B27,J5-B27,J6-B27,J8-B27
EXTTRIG_ORG	External Trigger	J16-1,J6-C27
EXT_INTR	External Trigger Interrupt	J1-20,J6-A12
FAN_LOCK	Fan Lock Sense	J18-2,J2-A10
FAN_POWER	Fan Power	J18-3,J2-B9,J2-C9
FAN_RETURN	Fan Power (Ground)	J18-1,J2-B10,J2-C10
FN_CLK	Fractional N Sync Clock	J1-13,J5-A19,J8-A19
FN_DATA	Fractional N Serial Data	J1-64,J5-A20,J8-A20
FN_RUN/STOP	Fractional N Run/Stop	J1-15,J5-C22,J8-C22
FN_STRB_1	Fractional N Chip 1 Enable	J1-16,J5-A21
FN_STRB_2	Fractional N Chip 2 Enable	J1-66,J8-A21

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Table B-1. Signal Name (continued)

Mnemonic	Description	Pin Assignment
FP_CHANGE	Frequency/Power Change	J3-C26,J5-B22,J6-C26,J8-B22
F_BUS	Frequency Bus	J1-18,J2-B13,J3-B20,J4-B20,J5-B20,J6-B20,J8-B20
GATE_OUT	Gate Output	J6-C20,J7-1
INT//EXT	External Reference Sense	J1-71,J5-C19

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Power Requirement

⚠Replacing Fuse

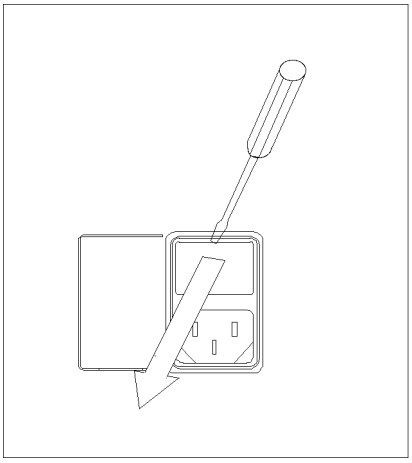
Fuse Selection

Select proper fuse according to the Table C-1.

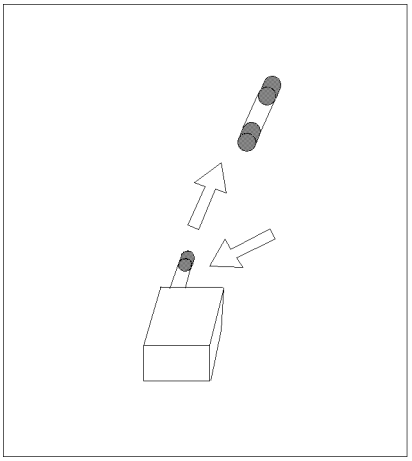
Table C-1. Fuse Selection

Fuse Rating/Type	Fuse Part Number
5A 250Vac UL/CSA type Time Delay	2110-0030

For ordering the fuse,contact your nearest Agilent Technologies Sales and Service Office.



Open the cover of AC line receptacle on the rear panel using a small minus screwdriver.



To check or replace the fuse, pull the fuse holder and remove the fuse. To reinstall the fuse, insert a fuse with the proper rating into the fuse holder.

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Power Requirements

The 4396B requires the following power source:

Voltage : 90 to 132 Vac, 198 to 264 Vac

Frequency : 47 to 63 Hz

Power : 300 VA maximum

Power Cable

In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power outlet, this cable grounds the instrument frame.
The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure C-1 for the part numbers of the power cables available.

Warning

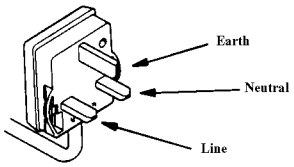


For protection from electrical shock, the power cable ground must not be defeated.

The power plug must be plugged into an outlet that provides a protective earth ground connection.

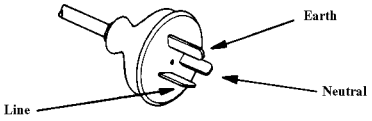
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OPTION 900 — United Kingdom



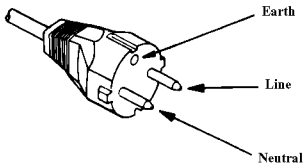
Plug : BS 1363A, 250V
Cable : 8120-1351

OPTION 901 — Australia / New Zealand



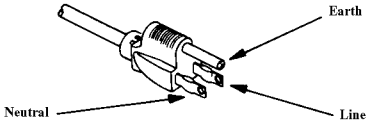
Plug : NZSS 198/AS C112, 250V
Cable : 8120-1369

OPTION 902 — European Continent



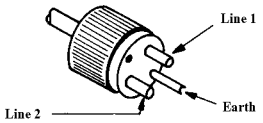
Plug : CEE-VII, 250V
Cable : 8120-1689

OPTION 903 — U.S. / Canada



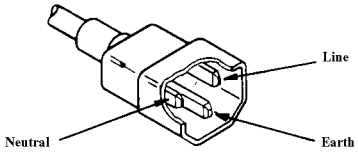
Plug : NEMA 5-15P, 125V, 15A
Cable : 8120-1378

OPTION 904 — U.S. / Canada



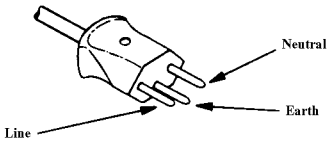
Plug : NEMA 6-15P, 250V, 15A
Cable : 8120-0698

OPTION 905* — Any country



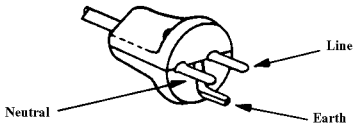
Plug : CEE 22-VI, 250V
Cable : 8123-1396

OPTION 906 — Switzerland



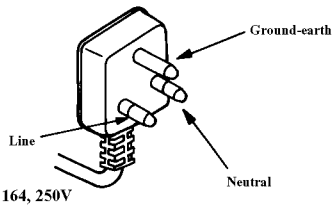
Plug : SEV 1011.1959-24507 Type 12, 250V
Cable : 8120-2104

OPTION 912 — Denmark



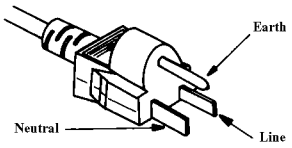
Plug : DHCR 107, 220V
Cable : 8120-2956

OPTION 917 — India / Republic of S.Africa



Plug : SABS 164, 250V
Cable : 8120-4211

OPTION 918 — Japan



Plug : JIS C 8303, 125V, 15A
Cable : 8120-4753

NOTE: Each option number includes a 'family' of cords and connectors of varoius materials and plug body configurations (straight, 90° etc.).

* Plug option 905 is frequently used for interconnecting system components and peripherals.

Figure C-1. Power Cable Supplied

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Error Messages

This section lists the service related error messages that may be displayed on the analyzer display or transmitted by the instrument over GPIB. Each error message is accompanied by an explanation, and suggestions are provided to help in solving the problem.

When displayed, error messages are usually preceded with the word CAUTION:. That part of the error message has been omitted here for the sake or brevity. Some messages are for information only, and do not indicate an error condition. Two listings are provided: the first is in alphabetical order, and the second in numerical order.

Error Messages in Alphabetical Order

234 1st LO LEAKAGE TEST FAILED

This message is displayed when an external test 25: S INPUT RESIDUALS fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

217 1st LO OSC TEST FAILED

The 1st LO OSC (first local oscillator) on the A4A1 1st LO does not work properly. This message is displayed when an internal test 9: A4A1 1ST LO OSC fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

218 2nd LO OSC TEST FAILED

The 2nd LO OSC (second local oscillator) on the A3A2 2nd LO does not work properly. This message is displayed when an internal test 10: A3A2 2ND LO fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

219 3rd LO OSC TEST FAILED

The 3rd LO OSC (third local oscillator) on the A6 receiver IF does not work properly. This message is displayed when an internal test 12: A6 3RD LO OSC fails. Troubleshoot the receiver group in accordance with the *Receiver Troubleshooting* chapter.

247 A-INPUT LEVEL COMPRESSION TEST FAILED

This message is displayed when an external test 33: A INPUT COMPRESSION fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

241 A-INPUT NOISE LEVEL OUT OF SPEC

This message is displayed when an external test 29: NA CROSSTALK & NOISE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

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245 **A/R RATIO ACCURACY OUT OF SPEC**

This message is displayed when an external test 32: A/R RATIO ACCURACY fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

246 **A/R RATIO RAW RESPONSE TEST FAILED**

This message is displayed when an external test 32: A/R RATIO ACCURACY fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

225 **A3 DIVIDER OUTPUT FREQUENCY OUT OF SPEC**

The output frequency of the divider circuit on the A3A1 ALC is out of its limits. This message is displayed when an internal test 11: A3A1 DIVIDER fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

224 **ALC TEST FAILED**

The ALC (Auto Level Control) circuit on the A3A1 ALC does not work properly. This message is displayed when an internal test 16: A3A1 ALC fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

260 **ALL EXT TEST FAILED**

This message is displayed when one of an external tests 53: ALL EXT 1 through 57: ALL EXT 5 fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

195 **ALL INT TEST FAILED**

This message is displayed when an internal test 0: ALL INT fails. Troubleshoot the analyzer in accordance with the *Digital Control Troubleshooting* chapter.

250 **B-INPUT LEVEL COMPRESSION TEST FAILED**

This message is displayed when an external test 35: B INPUT COMPRESSION fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

242 **B-INPUT NOISE LEVEL OUT OF SPEC**

This message is displayed when an external test 29: NA CROSSTALK & NOISE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

248 **B/R RATIO ACCURACY OUT OF SPEC**

This message is displayed when an external test 34: B/R RATIO ACCURACY fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

249 **B/R RAW RESPONSE TEST FAILED**

This message is displayed when an external test 34: B/R RATIO ACCURACY fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

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197 **BACKUP SRAM CHECK SUM ERROR**

The data (GPIB Address and so on) stored in the A1 CPU's BACKUP SRAM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

207 **CPU BACKUP SRAM R/W ERROR**

The A1 CPU's BACKUP SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

206 **CPU INTERNAL SRAM R/W ERROR**

The A1 CPU's internal SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

221 **DC OFFSET TOO BIG ON 0 DEG PATH**

The DC offset on 0° path of the A6 receiver IF is larger than its limit. This message is displayed when an internal test 14: A6 3rd IF DC OFFSET fails. Troubleshoot the receiver group in accordance with the *Receiver Troubleshooting* chapter.

222 **DC OFFSET TOO BIG ON 90 DEG PATH**

The DC offset on 90° path of the A6 receiver IF is larger than its limit. This message is displayed when an internal test 14: A6 3rd IF DC OFFSET fails. Troubleshoot the receiver group in accordance with the *Receiver Troubleshooting* chapter.

199 **DSP CHIP TEST FAILED**

The A1 CPU's DSP (Digital Signal Processor) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

208 **DSP SRAM R/W ERROR**

The DSP's SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

209 **DUAL PORT SRAM R/W ERROR**

The DSP's dual port SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

198 **EEPROM CHECK SUM ERROR**

The data (Correction Constants and so on) stored in the A1 CPU's EEPROM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Troubleshoot the A1 CPU in accordance with the *Digital Control Troubleshooting* chapter.

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194 EEPROM WRITE ERROR

Data cannot be stored properly into the EEPROM on the A1 CPU. This message is displayed when performing the display background adjustment or updating correction constants in the EEPROM using the adjustment program. Troubleshoot the A1 CPU in accordance with the *Digital Control Troubleshooting* chapter.

200 F-BUS TIMER CHIP TEST FAILED

The A1 CPU's F-BUS (Frequency Bus) timer does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

213 FAILURE FOUND FROM A/D MUX TO A/D CONVERTER

A trouble is found on the signal path from the A/D multiplexer to A/D converter on the A6 receiver IF. This message is displayed when an internal test 5: A6 A/D CONVERTER fails. Troubleshoot the A6 receiver IF in accordance with the *Receiver Troubleshooting* chapter.

212 FAN POWER OUT OF SPEC

The voltage of the fan power supply at the DC bus node 11 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with the *Power Supply Troubleshooting* chapter.

203 FDC CHIP TEST FAILED

The A1 CPU's FDC (Flexible Disk drive control) chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

196 FLASH MEMORY CHECK SUM ERROR

The data (Firmware) stored in the A1 flash memory are invalid. This message is displayed in the bootloader menu. Troubleshoot the A1 CPU in accordance with the *Digital Control Troubleshooting* chapter.

226 FLOPPY DISK DRIVE FAILURE FOUND

The A53 built-in FDD (floppy disk drive) does not work properly. This message is displayed when an external test 18: DSK DR FAULT ISOL'N fails. Replace the A53 FDD with a new one. See the *Digital Control Troubleshooting* chapter.

236 FRACTION SPURIOUS OUT OF SPEC

This message is displayed when an external test 27: FRACTION SPURIOUS fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

215 FRACTIONAL N OSC TEST FAILED

The fractional N oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 7: A5 FRACTIONAL N OSC fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

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211 **GND LEVEL OUT OF SPEC**

The voltage of the GND (Ground) at the DC bus node 26 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with the *Power Supply Troubleshooting* chapter.

205 **HP-HIL CHIP TEST FAILED**

The A1 CPU's HP-HIL control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

204 **GPIB CHIP TEST FAILED**

The A1 CPU's GPIB chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

255 **IF GAIN SWITCHING UNC. OUT OF SPEC**

This message is displayed when an external test 37: IF GAIN fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

229 **INPUT ATTENUATOR ACCURACY OUT OF SPEC**

This message is displayed when an external test 21: INPUT ATTENUATOR fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

202 **KEY CHIP TEST FAILED**

The A1 CPU's front keyboard control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

228 **OUTPUT ATTENUATOR ACCURACY OUT OF SPEC**

This message is displayed when an external test 20: OUTPUT ATTENUATOR fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

48 **PHASE LOCK LOOP UNLOCKED**

A phase lock loop (PLL) circuits within the analyzer does not work properly. Troubleshoot the analyzer in accordance with the *Digital Control Troubleshooting* chapter. When a **Svc** annotation is displayed (Service Modes are activated), this error message does not appear even if a PLL circuit is not working.

210 **POST REGULATOR OUTPUT VOLTAGE OUT OF SPEC**

A power supply voltage of the A2 post-regulator is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with the *Power Supply Troubleshooting* chapter.

49 **POWER FAILED ON—-**

Power failure occurs on the power lines listed in the message. One or some of +15 V, +5 V, −5 V, −15 V, and PostRegHot, follow the message. Troubleshoot the power supply functional group in accordance with the *Power Supply Troubleshooting* chapter.

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193 **POWER ON TEST FAILED**

An internal test fails in the power on sequence. This message is displayed when the power on selftest fails. Troubleshoot the analyzer in accordance with the *Digital Control Troubleshooting* chapter.

227 **POWER SWEEP LINEARITY OUT OF SPEC**

This message is displayed when an external test 19: POWER SWEEP LINEARITY fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

243 **R-INPUT LEVEL COMPRESSION TEST FAILED**

This message is displayed when an external test 30: R INPUT COMPRESSION fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

240 **R-INPUT NOISE LEVEL OUT OF SPEC**

This message is displayed when an external test 29: NA CROSSTALK & NOISE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

238 **R-INPUT TO A-INPUT CROSSTALK OUT OF SPEC**

This message is displayed when an external test 29: NA CROSSTALK & NOISE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

239 **R-INPUT TO B-INPUT CROSSTALK OUT OF SPEC**

This message is displayed when an external test 29: NA CROSSTALK & NOISE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

244 **RANGING ACCURACY TEST FAILED**

This message is displayed when an external test 31: RANGING fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

214 **REF OSC TEST FAILED**

The reference oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 6: A5 REFERENCE OSC fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

237 **RF OUT TO R-INPUT FLATNESS TEST FAILED**

This message is displayed when an external test 28: RF TO A LVL & FLTNESS fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

230 **RF OUT TO S-INPUT FLATNESS TEST FAILED**

This message is displayed when an external test 22: RF TO S LVL & FLTNESS fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

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201 **RTC CHIP TEST FAILED**

The A1 CPU's RTC (Real Time Clock) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See the *Digital Control Troubleshooting* chapter.

232 **S-INPUT LEVEL COMPRESSION TEST FAILED**

This message is displayed when an external test 24: S INPUT COMPRESSION fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

235 **S-INPUT NOISE LEVEL OUT OF SPEC**

This message is displayed when an external test 26: S INPUT NOISE LEVEL fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

233 **S-INPUT RESIDUAL RESPONSE OUT OF SPEC**

This message is displayed when an external test 25: S INPUT RESIDUALS fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

231 **S-INPUT TO A-INPUT CROSSTALK TEST FAILED**

This message is displayed when an external test 23: S TO A CROSSTALK fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

257 **SA NON-HARMONIC SPURIOUS OUT OF SPEC**

This message is displayed when an external test 39: SPURIOUS fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

251 **SA RES FILTER 3 DB BW OUT OF SPEC**

This message is displayed when an external test 36: RESOLUTION BANDWIDTH fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

252 **SA RES FILTER SHAPE FACTOR OUT OF SPEC**

This message is displayed when an external test 36: RESOLUTION BANDWIDTH fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

254 **SA RES FILTER SWITCHING UNC. OUT OF SPEC**

This message is displayed when an external test 36: RESOLUTION BANDWIDTH fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

253 **SA RES FILTER TRACE NOISE TEST FAILED**

This message is displayed when an external test 36: RESOLUTION BANDWIDTH fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

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223 **SAMPLE FREQUENCY OUT OF SPEC**

The sampling frequency of the sample/hold circuit on the A6 receiver IF is out of its limits. This message is displayed when an internal test 15: A6 SEQUENCER fails. Troubleshoot the receiver group in accordance with the *Receiver Troubleshooting* chapter.

256 **SIDE BAND LEVEL OUT OF SPEC**

This message is displayed when an external test 38: PHASE NOISE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

220 **SOURCE OSC TEST FAILURE**

The source oscillator on the A3A1 ALC does not work properly. This message is displayed when an internal test 13: A3A1 SOURCE OSC fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

216 **STEP OSC TEST FAILED**

The step oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 8: A5 STEP OSC fails. Troubleshoot the source group in accordance with the *Source Troubleshooting* chapter.

259 **X-TAL FILTER RAW RESPONSE TEST FAILED**

This message is displayed when an external test 40: X'TAL FILTER RESPONSE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

258 **X-TAL FILTER RESPONSE OUT OF SPEC**

This message is displayed when an external test 40: X'TAL FILTER RESPONSE fails. Troubleshoot the analyzer in accordance with the *Isolate Faulty Group Troubleshooting* chapter.

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48 PHASE LOCK LOOP UNLOCKED

49 POWER FAILED ON—-

193 POWER ON TEST FAILED

194 EEPROM WRITE ERROR

195 ALL INT TEST FAILED

196 FLASH MEMORY CHECK SUM ERROR

197 BACKUP SRAM CHECK SUM ERROR

198 EEPROM CHECK SUM ERROR

199 DSP CHIP TEST FAILED

200 F-BUS TIMER CHIP TEST FAILED

201 RTC CHIP TEST FAILED

202 KEY CHIP TEST FAILED

203 FDC CHIP TEST FAILED

204 GPIB CHIP TEST FAILED

205 HP-HIL CHIP TEST FAILED

206 CPU INTERNAL SRAM R/W ERROR

207 CPU BACKUP SRAM R/W ERROR

208 DSP SRAM R/W ERROR

209 DUAL PORT SRAM R/W ERROR

210 POST REGULATOR OUTPUT VOLTAGE OUT OF SPEC

211 GND LEVEL OUT OF SPEC

212 FAN POWER OUT OF SPEC

213 FAILURE FOUND FROM A/D MUX TO A/D CONVERTER

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214 **REF OSC TEST FAILED**

215 **FRACTIONAL N OSC TEST FAILED**

216 **STEP OSC TEST FAILED**

217 **1st LO OSC TEST FAILED**

218 **2nd LO OSC TEST FAILED**

219 **3rd LO OSC TEST FAILED**

220 **SOURCE OSC TEST FAILURE**

221 **DC OFFSET TOO BIG ON 0 DEG PATH**

222 **DC OFFSET TOO BIG ON 90 DEG PATH**

223 **SAMPLE FREQUENCY OUT OF SPEC**

224 **ALC TEST FAILED**

225 **A3 DIVIDER OUTPUT FREQUENCY OUT OF SPEC**

226 **FLOPPY DISK DRIVE FAILURE FOUND**

227 **POWER SWEEP LINEARITY OUT OF SPEC**

228 **OUTPUT ATTENUATOR ACCURACY OUT OF SPEC**

229 **INPUT ATTENUATOR ACCURACY OUT OF SPEC**

230 **RF OUT TO S-INPUT FLATNESS TEST FAILED**

231 **S-INPUT TO A-INPUT CROSSTALK TEST FAILED**

232 **S-INPUT LEVEL COMPRESSION TEST FAILED**

233 **S-INPUT RESIDUAL RESPONSE OUT OF SPEC**

234 **1st LO LEAKAGE TEST FAILED**

235 **S-INPUT NOISE LEVEL OUT OF SPEC**

236 **FRACTION SPURIOUS OUT OF SPEC**

237 **RF OUT TO R-INPUT FLATNESS TEST FAILED**

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238 R-INPUT TO A-INPUT CROSSTALK OUT OF SPEC

239 R-INPUT TO B-INPUT CROSSTALK OUT OF SPEC

240 R-INPUT NOISE LEVEL OUT OF SPEC

241 A-INPUT NOISE LEVEL OUT OF SPEC

242 B-INPUT NOISE LEVEL OUT OF SPEC

243 R-INPUT LEVEL COMPRESSION TEST FAILED

244 RANGING ACCURACY TEST FAILED

245 A/R RATIO ACCURACY OUT OF SPEC

246 A/R RATIO RAW RESPONSE TEST FAILED

247 A-INPUT LEVEL COMPRESSION TEST FAILED

248 B/R RATIO ACCURACY OUT OF SPEC

249 B/R RAW RESPONSE TEST FAILED

250 B-INPUT LEVEL COMPRESSION TEST FAILED

251 SA RES FILTER 3 DB BW OUT OF SPEC

252 SA RES FILTER SHAPE FACTOR OUT OF SPEC

253 SA RES FILTER TRACE NOISE TEST FAILED

254 SA RES FILTER SWITCHING UNC. OUT OF SPEC

255 IF GAIN SWITCHING UNC. OUT OF SPEC

256 SIDE BAND LEVEL OUT OF SPEC

257 SA NON-HARMONIC SPURIOUS OUT OF SPEC

258 X-TAL FILTER RESPONSE OUT OF SPEC

259 X-TAL FILTER RAW RESPONSE TEST FAILED

260 ALL EXT TEST FAILED

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