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DATA GENERATORS & DATA ANALYZERS

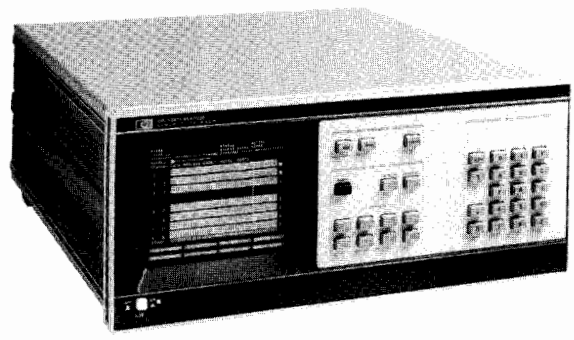
Data Generator/Analyzer System

Models 8180B, 8181B, 8182B

- Digital ac parametric and functional evaluation
- 50MHz, 16kbit vector memory depth
- 100ps timing/10mV level resolution
- Real-time data comparison
- Ease-of-use
- System Software



HP 8180B Data Generator



HP 8182B Data Analyzer

The Tool for At-Speed Evaluation of Digital IC's, Boards & Modules

The HP 8180B is a modular, high speed Data Generator for the stimulation of digital IC's and boards. For the analysis of a digital circuit's response, the HP 8182B provides capabilities for data capture and comparison, and for level and timing characteristics measurements. The Data Generators and Data Analyzers are matched in performance with regard to vector rates, vector memory depth and measurement accuracy and functionality.

Modular Configurations - From Stand-Alone to Complete Systems

On the bench, the Data Generators and Analyzers are fully operational without an external controller due to a softkey-driven, interactive operating concept.

In remote operation, all set-ups can be programmed with an external controller via the standard HP-IB interface. This enables interactive operation as well as full automation of Stimulus/Response setups.

For IC Test applications, HP is offering complete Systems including Testhead and System Software. This provides the turn-key solution required to test digital devices from MSI to VLSI integration, including ASIC's (Application Specific IC's).

The HP 81810S IC Design Verification System

Owing to the modular architecture which allows you to combine instrument modules as required, the system is extremely flexible in terms of functionality, performance and price. This enables you to tailor the system and achieve the optimum fit for applications like IC Design Verification, Prototype Evaluation, Failure Analysis, Low-Volume Production Test and Incoming Inspection.

Test System Modules

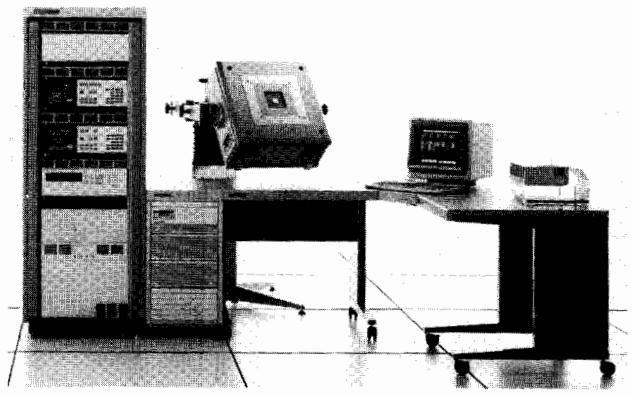
The HP 81810S is composed of the HP 8180B and HP 8181B Data Generator and Extender, the HP 8182B Data Analyzer, the HP 15466A Test Head (for up to 256 tester channels), a systemizing rack, the HP 4141B DC Source/Monitor, the HP 6624A Device Power Supply and a range of accessories. Also included is a HP 9000 series 300 workstation plus the System Software. All system modules except the controller can be installed in one or two racks, depending on the configuration.

System Software

The System Software provides a shell around the hardware resources and enables you to focus on the device under test rather than on the machine. Because it is easy to use, users need little training to work with this tool.

Softkey driven menus guide the user through parameter set-up, pattern editing, pin labeling etc. to enter device and test specific data. After a few key-strokes the user can then perform various tests e.g. functional truth-table verification or automatic level and edge search as required for measuring propagation delays or set-up and hold times.

The CAE link part of the software allows you to link directly to CAE design workstation or host computers running simulation programs. The software provides turn-key programs for downloading data vectors which are compatible with HILO3, FACTOR (SENTRY) and Mentor design station data formats. After downloading, the testvectors are readily available in the Test System for execution.



Applications that Reflect in Features

For at-speed functional verification of prototype circuits, the Generators and Analyzers offer programmable digital patterns at data rates up to 50 MHz. The linear vector memory depth of 16 Kbit/channel allows you to generate and capture the immense number of testvectors required for testing complex devices. Real-time comparison between "expected" data and captured data generates an "Error Map" which gives immediate feedback and increases throughput.

For thorough characterization of a circuits' performance limits, timing edges can be positioned with a best resolution of 100 ps and level pairs can be programmed with a 10 mV resolution. "Window Comparison" simultaneously checks proper upper and lower logic level and timing conditions. This makes the equipment the ideal tool for Critical Path Analysis of prototype circuits and for in-depth analysis of circuits failing a test.

Please refer to the semiconductor test section (page 526) to find information about the HP 82000, a fully integrated IC evaluation system. It features highest performance, like 200 MHz speed and ±250 ps accuracy on up to 384 true I/O pins.

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Specifications

Specifications apply for operating temperatures from 0°C to 50°C.

HP 8180B, 8181B Data Generator/Extender

Memory and Channels

Memory depth: 16384 bit/channel
Number of channels: up to 64 using HP 8180B with two HP 8181B Extenders. Up to 192 channels with 3 sets of equipment in parallel operation.
HP 8180B Channels
RZ (return-to-zero) channels: independent variable delay and width in each of up to 8 channels.
NRZ (non-return-zero) channels: Up to 16 channels minus the number of RZ channels. Fixed timing.
Strobe channel: NRZ data or clock. Fixed timing
Clock channels: independent delay and width in each of 2 channels. Clock 1 can be selected to run continuously in Break state (see 'Cycle modes').
HP 8181B Channels
NRZ: up to 24 channels. Fixed timing within an Extender, group delay with respect to HP 8180B.
Memory Loading
Codes: bin, oct, hex, dec (address codes: oct, hex, dec).
Entry: Keyboard or HP-IB.
Displayed channel order: user-defined.
Line edit: insert, delete, macro.
Channel edit: clear, set, copy, prbs, counts, entry mask.

Cycle Modes

Single, Auto, Initialization + Auto, Gated, Initialization + Gated. (Initialization data is output at the beginning of the first cycle only).
Break state: implemented by manual or external BREAK command or by strobe channel bit. Data is held at current address. Manual or external RUN command cause same cycle to continue.
Stop state: implemented by manual or external STOP command. Data is held at current address and the cycle is terminated. Manual or external RUN command trigger a new cycle.

Timing

Clock period: 20 ns to 950 ms (1.05 Hz to 50 MHz). Ext clock 0 to 50 MHz.
Delay
(relative to strobe channel): 0.0 ns to 950 ms, max 90% period −18ns.
Width: 10.0 ns to 950 ms, max 90% period −8ns.
Skew: ≤2ns for NRZ channels and RZ channels programmed for zero delay.
Resolution: 3 digits (best case 100 ps).
Accuracy: ±5% of programmed value ±1ns.
Jitter: ≤0.2% + 100 ps (+ additional 50 ps for delay and width).

Outputs

Output impedance: 50 Ohm
Data and clock: 4 different high level / low level pairs can be defined and assigned to any number of individual outputs. Each channel has independent normal / complement switching. Common 'off '.
Read-out: can be selected for 50 Ohm or high impedance load (common selection for all channels).

	50 Ohm load	High-impedance load
High level:	−1.50 to +5.50 V	−1.00 to +17.0 V
Low level:	−2.00 to +5.00 V	−2.00 to +16.0 V
Resolution:	3 digits (10 mV)	3 digits (best case 20 mV)
Amplitude:	0.5 to 5.5 V	1.0 to 17 V

Transitions:

10% to 90%	(3 + | 0.2 ampl |) ns	(3 + | 0.5 ampl |) ns

20% to 80% at ECL levels: 1.5 ns
Strobe: ECL/TTL selectable

HP 8182B Data Analyzer

Memory and Channels

Memory depth: 16384 bit/channel
Number of channels: up to 32. Up to 128 by parallel operation of four HP 8182B's.
Expected data memory: 16384 bit/channel, segmentable.
Codes: bin, oct, hex (address code: dec).
Entry: Keyboard, HP-IB or read-in from DUT.
Displayed channel order: user-defined.
Line edit: word mask (don't care), insert, delete.
Channel edit: clear, set, copy, mask (don't care), exchange.

Modes

Analysis / store-and-compare: synchronous sampling with variable analog sampling point delay or asynchronous sampling. Comparison with expected data, if required.
Displays: state list, timing diagram, or error map.
Glitch detection: down to 5 ns. Memory depth is halved when glitch detection is selected.
Trigger condition: can be selected to start or stop analysis.
Real-time compare: comparison of actual with expected data throughout a time window. Window has variable analog delay and width. Real-time and latched error output signals are provided.
Display: error map.
Trigger conditions: starts comparison.

Timing

External clock: 0 to 50 MHz.
Delay
(relative to external clock): 0.0 ns to 1 s, max 95% period - 1 ns
Compare window width: 10.0 ns to 1 s, max 95% period - 9 ns
Channel skew: ≤2 ns
Resolution: 3 digits (best case 100 ps).
Accuracy: ±5% of programmed value ±1 ns.
Internal clock: 1 Hz to 50 MHz (1-2-5) steps).

Inputs

Data: 6 different thresholds or dual threshold pairs can be defined and assigned to any number of individual inputs.
Clock: programmable threshold and selectable slope (positive, negative, both).
Input Impedance: 1 MOhm, <7pF.
Control signals: (100 kOhm / 50 Ohm selectable input impedance)
Trigger arm and ext stop signals: independent programmable thresholds and selectable slope (positive, negative, don't care).
Trigger qualifier and clock qualifier signals: independent programmable threshold and selectable levels (high, low, don't care).
Threshold range: −10.0 to +10.0 V.
Dynamic range: threshold ± 10 V.
Resolution: 3 digits (best case 10 mV).

Trigger

Trigger arm, word and qualifier, digital filter (1 to 16), clock and qualifier, delay (0 to 65535.)

Ordering and Literature

For Ordering Information (also on accessories) and detailed Technical Data Sheets and Application Notes on the products covered in this chapter, please contact your HP sales office.

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