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Service Guide

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Agilent Technologies 16753/54/55/56A and 16950A Logic Analyzers

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Agilent 16753/54/55/56A and 16950A Logic Analyzers—At a Glance

The 16753A, 16754A, 16755A, and 16756A are 600 MHz logic analyzer modules for the 16700-series or 16900-series logic analysis system.

The 16950A is 600 MHz logic analyzer module for the 16900-series logic analysis system.

The 16753/54/55/56A and 16950A logic analyzer modules offer high performance measurement capability.

Features

Some of the main features of the 16753/54/55/56A and 16950A are as follows:

- 64 data channels
- 4 clock/data channels
- 1 M to 64 M memory depth per channel (depends upon model or option chosen)
- 600 MHz maximum state acquisition speed
- 1.2 GHz, 128 M deep timing analysis on half channels
- “Eye scan” feature
- 4 GHz timing zoom with 64 k memory depth
- Expandable to 340 channels

Service Strategy

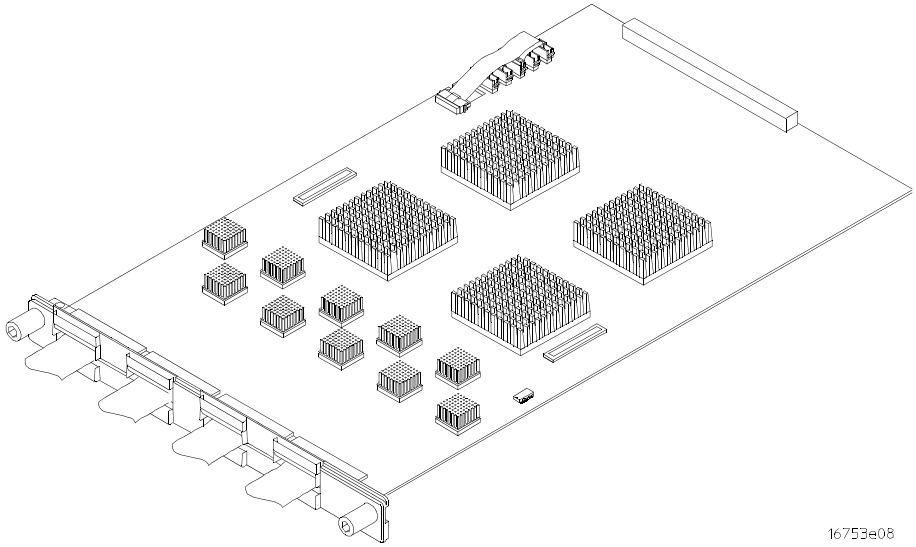
The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16753/54/55/56A or 16950A state and timing analyzer module.

The modules can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

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Application

This service guide applies to 16753/54/55/56A logic analyzer modules installed in 16700-series or 16900-series logic analysis system mainframes or to 16950A logic analyzer modules in a 16900-series logic analysis system mainframe.



The 16753/54/55/56A or 16950A Logic Analyzer

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In This Book

This book is the service guide for the 16753/54/55/56A and 16950A 600 MHz logic analyzer modules.

This service guide has eight chapters.

Chapter 1, “General Information,” beginning on page 9 contains information about the module, lists accessories for the module, gives specifications and characteristics of the module, and provides a list of the equipment required for servicing the module.

Chapter 2, “Preparing for Use,” beginning on page 15 tells how to prepare the module for use.

Chapter 3, “Testing Logic Analyzer Performance,” beginning on page 19 gives instructions on how to verify that the module meets its specifications.

Chapter 4, “Calibrating,” beginning on page 87 contains calibration instructions for the module (if required).

Chapter 5, “Troubleshooting,” beginning on page 89 contains explanations of self-tests and flowcharts for troubleshooting the module.

Chapter 6, “Replacing Assemblies,” beginning on page 113 explains how to replace the module and assemblies of the module and how to return them to Agilent Technologies.

Chapter 7, “Replaceable Parts,” beginning on page 121 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8, “Theory of Operation,” beginning on page 127 explains how the logic analyzer module works.

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1

General Information

This chapter lists the accessories, some of the specifications and characteristics, and the recommended test equipment.

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Accessories

One or more of the following accessories, sold separately, are required to operate the 16753/54/55/56A or 16950A logic analyzer.

Accessories	Agilent Part Number
Single-ended soft touch probe	E5390A
Differential soft touch probe	E5387A
Half-size soft touch probe	E5398A
100-pin single-ended probe	E5378A
100-pin differential probe	E5379A
38-pin single-ended probe	E5380A
Single-ended flying lead probe set	E5382A
Differential flying lead probe set	E5381A

Mainframe and Operating System

The 16753/54/55/56A logic analyzers require a 16700-series logic analysis system with operating system version A.02.70.00 or higher, or any 16900-series logic analysis system.

The 16950A logic analyzer requires a 16900-series logic analysis system.

To check your 16700-series logic analysis system's operating system version number, open the System Administration window, click the Admin tab, then click About...

If the proper version is not loaded, obtain a copy of the updated operating system software and install it in the logic analyzer mainframe. You can request a software upgrade at http://software.cos.agilent.com/16700 or by contacting your nearest Agilent Technologies Customer Support Center.

Three Cooling Fans Required in 16700A-series Mainframe

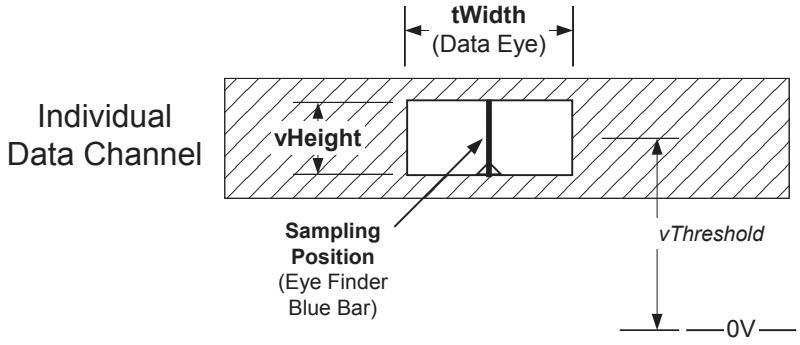
Earlier versions of the 16700A/01A/02A mainframe contained only two cooling fans and might not provide adequate cooling to ensure reliable performance. If the first six digits of the 16700A/02A serial number (located on the back of the instrument) are US3849 or higher, or the first six digits of the 16701A are US3902 or higher, the instrument is a three-fan model, which will supply sufficient cooling.

All 16700B/01B/02B and all 16900-series systems provide adequate cooling to ensure reliable performance.

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Specifications

The specifications are the performance standards against which the product is tested.



Specifications			
Parameter	**300 Mb/s mode**	**600 Mb/s mode**	**Notes**
Minimum master to master clock time	3.33 ns	1.67 ns	
tWidth (minimum)	1 ns	1 ns	Specified at probe tip. Eye width as measured by Eye Finder may be less.

Specifications verified under the following test conditions:			
Parameter	**300 Mb/s mode**	**600 Mb/s mode**	**Notes**
Vh	1.125 V		250 mV pp
Vl	0.875 V		
vThreshold	1 V		
rise/fall times	150-180 ps		
Probe	Agilent E5382A		

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Characteristics

The characteristics are not specifications, but are included as additional information.

	Full-Channel Mode	**Half-Channel Mode**
Maximum Conventional Timing Rate	600 MHz	1.2 GHz
Sample Rate, Timing Zoom	4 GHz	4 GHz
Channel Count per Card	68	34
Channel Count per Three-Card Module	204	102
Channel Count per Five-Card Module	340	170
Memory Depth 16753A	1 M Samples	2 M Samples
Memory Depth 16754A	4 M Samples	8 M Samples
Memory Depth 16755A	16 M Samples	32 M Samples
Memory Depth 16756A	64 M Samples	128 M Samples
Memory Depth 16950A Option 256	256 K Samples	512 K Samples
Memory Depth 16950A Option 001	1 M Samples	2 M Samples
Memory Depth 16950A Option 004	4 M Samples	8 M Samples
Memory Depth 16950A Option 016	16 M Samples	32 M Samples
Memory Depth 16950A Option 032	64 M Samples	128 M Samples
Memory Depth 16950A Option 064	1 M Samples	512 K Samples

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Environmental Characteristics

Probes

Maximum Input Voltage	± 40 V, CAT I. CAT I = Category I, secondary power line isolated circuits.

Operating Environment

Temperature	Instrument, 0 °C to 40 °C (+32 °F to 104 °F) when installed in a 16900A or 16902A mainframe. Instrument, 0 °C to 50 °C (+32 °F to 122 °F) when installed in a 16903A or 16700-series mainframe. Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 80% relative humidity at +40 °C (+104 °F), non-condensing.
Altitude	To 3000 m (10,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.2 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.5 g (0-peak), 5 minute resonant dwell at 4 resonances per axis. Operating power supplied by mainframe. Indoor use only. Pollution Degree 2. Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.

See the logic analyzer's online help system for a full listing of all specifications and characteristics.

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Recommended Test Equipment

Equipment	Critical Specification	Recommended Model/Part	Use†
Flying Lead Probe Set (Qty 2)	No substitute	Agilent E5382A	P, T
Ground Clips (Qty 10)	No substitute	16517-82105 (pkg of 20) (Included with E5382A Probe Set)	T
Stimulus Board	No substitute	16760-60001	T
Pulse Generator	≥ 310 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Agilent or HP 8133A Option 003	P, T
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, ΔV=250 mV.) Required for 8133A opt. 003.	Agilent or HP 15435A	P
Oscilloscope	Bandwidth ≥ 1.5 GHz, sampling rate ≥ 8 GSa/s	Agilent or HP 54845A or 54845B	P
SMA Coax Cable (Qty 2)	>18 GHz bandwidth	Agilent or HP 8120-4948	P
Male BNC to Female SMA Adapters (Qty 2)	>18 GHz bandwidth	Cambridge Products CP-AD507 (see www.cambridgeproducts.com)	P
SMA/Flying Lead Test Connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	No substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 23	P

† P = Performance Tests, T = Troubleshooting

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2

Preparing for Use

This chapter gives you instructions for preparing the logic analyzer module for use.

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Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed on page 13. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given on page 13. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20°C to +35°C (+68°F to +95°F)

Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40°C to +75°C (-40°F to +167°F)
- Humidity: Up to 90% at 65°C (+149°F)
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

One or more of the accessories listed on page 10 are required to operate the 16753/54/55/56A or 167950A logic analyzer module.

3 Inspect the product for physical damage.

Check the module and the supplied accessories for obvious physical or

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mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To configure and install the module

Instructions for configuring and installing the module into the mainframe can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16700B mainframe, go to www.agilent.com and enter **16700B installation guide** in the quick search box. Then scroll down to **Manuals, Guides & Notifications** to find the 16700B-Series Logic Analysis Systems Installation Guide.

To test the module

The logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, see "Testing Logic Analyzer Performance" on page 19. If you require a test to verify correct module operation using software self-tests, see "Do a self-test on the 16900-series logic analysis system" on page 38 or "Do a self-test on the 16700-series logic analysis system" on page 62.
- If the module does not operate correctly, see "Troubleshooting" on page 89.

To clean the module

- With the mainframe turned off and unplugged, use a cloth moistened with a mixture of mild detergent and water to clean the rear panel.
- Do not attempt to clean the module circuit board.

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3

Testing Logic Analyzer Performance

This chapter tells you how to test the performance of the 16753/54/55/56A or 16950A logic analyzer against the specifications listed on page 11.

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To ensure the 16753/54/55/56A or 16950A logic analyzer (also referred to as the module or the card) is operating as specified, software tests (self-tests) and a manual performance test are done. The logic analyzer is considered performance-verified if all of the software tests and the manual performance test have passed.

The specifications for the 16753/54/55/56A and 16950A logic analyzer define a minimum master to master clock time and a minimum data eye width at which data can be acquired. The manual performance test (minimum master-to-master clock time and minimum eye width test) verifies that the logic analyzer meets these specifications.

Mainframes

The 16753/54/55/56A logic analyzer modules can be tested in either a 16900-series mainframe or a 16700-series mainframe.

The 16950A logic analyzer module must be tested in a 16900-series mainframe.

In either case, the SMA/Flying Lead Test Connectors, the equipment required, and setup of the test equipment will be the same, except that the logic analyzer setup will differ.

The general instructions for performance test begin on page 23 with instructions for assembling the test connectors. Instructions specific to testing the module in a 16900-series mainframe begin on page 37. Instruction specific to testing the module in a 16700-series mainframe begin on page 61.

Test Strategy

Only specified parameters are tested. Specifications are listed on page 11. The test conditions defined in this procedure ensure that the specified parameter is as good as or better than specifications. No attempt is made to determine performance which is better than specifications. Not all channels of the logic analyzer will be tested; a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

Eye Finder is used to adjust the sampling position on every channel. Eye Finder must be used to achieve minimum data eye width performance.

First, the logic analyzer will be tested in the 300 Mb/s state mode. Then it will be tested in the 600 Mb/s state mode.

In the 300 Mb/s state mode all four clocks (Clk1, Clk2, Clk3 and Clk4) will be tested with their respective pods.

The 600 Mb/s mode has only one clock (Clk1). All tests in the 600 Mb/s mode will use clock Clk1.

All four pods will be tested, one pod at a time, in both 300 Mb/s state mode and 600 Mb/s state mode.

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The logic analyzer will be configured to acquire data on both edges of the clock, so the test frequency is set to half of the acquisition speed.

One-card Module

To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Multi-card Module

To perform a complete test on a multi-card module, perform the self-tests with the cards connected. Then, remove the multi-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into their original multi-card module configuration, reinstall it into the mainframe and perform the self-tests again. These steps are necessary to ensure that the clocks are tested on each module.

Instructions for removing and installing the module can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16900A mainframe, go to www.agilent.com and enter 16900A installation guide in the quick search box. Then scroll down to Manuals, Guides & Notifications to find the 16900A-Series Logic Analysis Systems Installation Guide.

Test Interval

Test the performance of the module against its specifications at two-year intervals.

Test Record Description

A Performance Test Record for recording the results of each procedure is provided in this chapter. You may want to make a copies of this, and fill-in a copy each time you test a module.

Test Equipment

A list of the recommended test equipment is provided. You can use any equipment that satisfies the specifications given. However, the instructions are written with the presumption that you are using the recommended test equipment.

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Equipment Required

The following equipment is required for the performance test procedure.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	≥ 310 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Agilent or HP 8133A option 003
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, ΔV=250 mV.) Required for 8133A opt. 003.	Agilent or HP 15435A
Oscilloscope	bandwidth ≥ 1.5 GHz, sampling rate ≥ 8 GSa/s	Agilent or HP 54845A/B or similar
SMA Coax Cable (Qty 2)	>18 GHz bandwidth	Agilent or HP 8120-4948
Flying Lead Probe Set (Qty 2)	no substitute	Agilent E5382A
Male BNC to Female SMA adapters (Qty 2)		Cambridge Products CP-AD507 (see www.cambridgeproducts.com)
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	no substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 23

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Assemble the SMA/Flying Lead Test Connectors

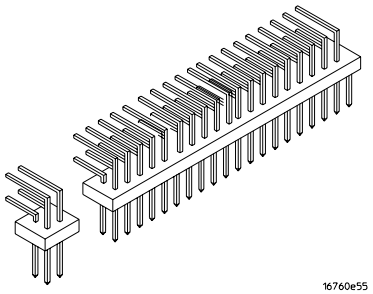
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the four required test connectors.

Materials Required

Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 8)		Johnson 142-0701-801 (see www.johnsoncomponents.com)
Pin Strip Header (Qty 1, which will be separated)	.100" X .100" Pin Strip Header, right angle, pin length .230", two rows, .120" solder tails	3M 2380-5121TN or similar 2-row with 0.1" pin spacing
SMA 50 ohm terminators (Qty 2)	Minimum bandwidth 2 GHz	Johnson 142-0801-866 50 ohm Dummy Load Plug
SMA m-m adapter (Qty 4)		Johnson 142-0901-811 SMA Plug to Plug or similar

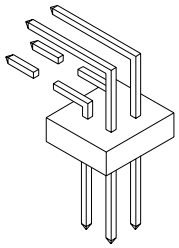
1 Prepare the pin strip header:

a Cut or cleanly break a 2 x 2 section from the pin strip.

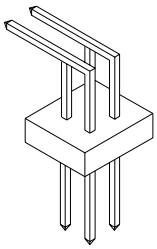


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b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.

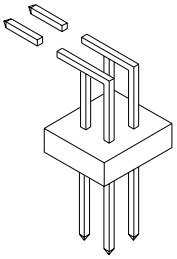


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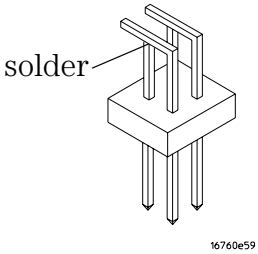


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c Trim about 2.5 mm from the outer leads.



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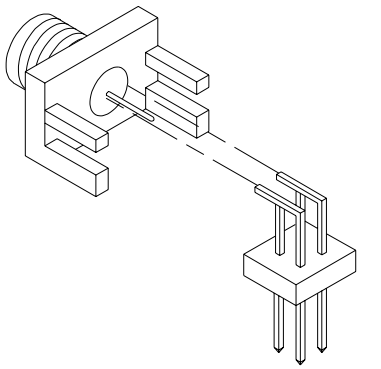
d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

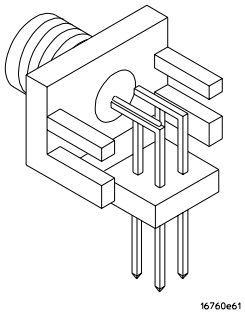
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2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.

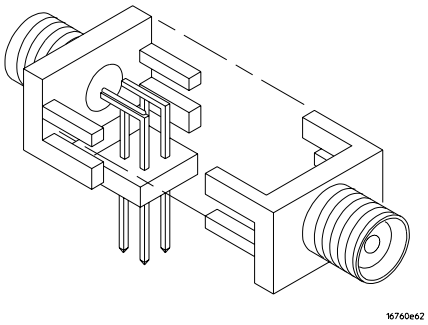


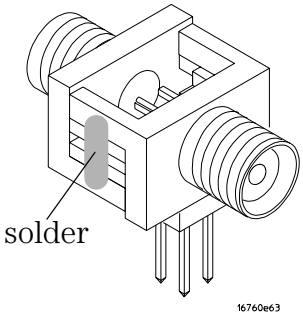


3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.





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c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

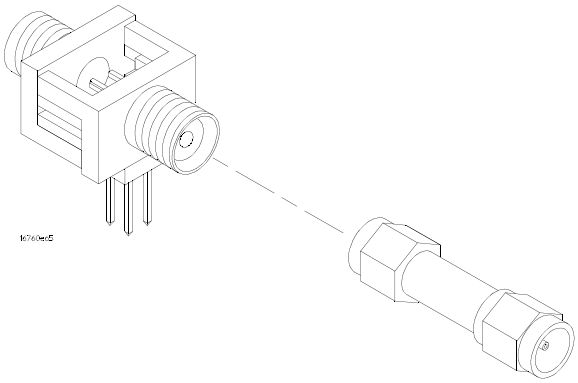
a Ensure that the following four points have continuity between them: The two pins on the left side of the pin strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

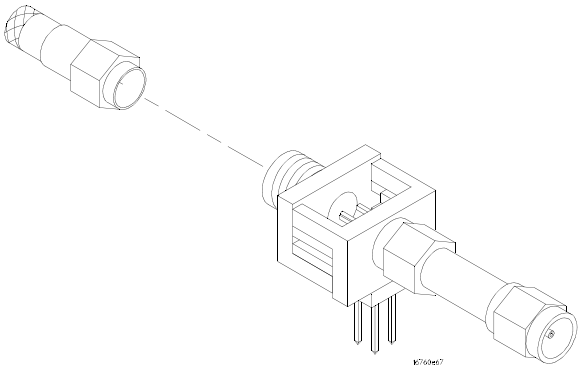
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

a Attach an SMA m-m adapter to one end of each of the four SMA/Flying Lead test connectors.

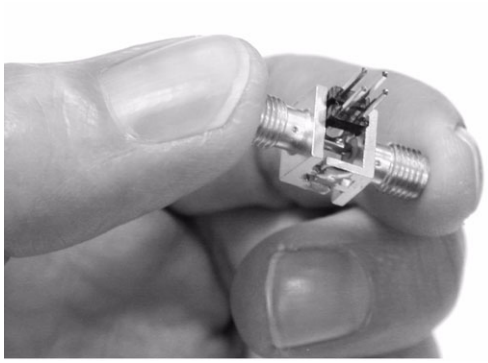


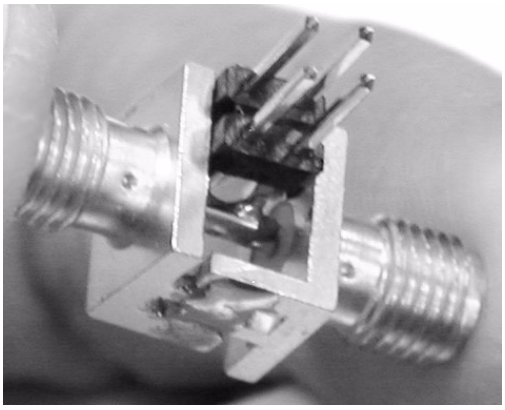
b Attach a 50 ohm terminator to the other end of just two of the SMA/ Flying Lead test connectors.



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c The finished test connector is shown in the pictures below.





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Set Up the Test Equipment

This section explains how to set up the test equipment for the minimum master-to-master clock time/minimum eye width test.

1 Turn on the required test equipment. Let all of the test equipment and the logic analyzer warm up for 30 minutes before beginning any test.

2 Set up the pulse generator according to the following table.

a Set the frequency of the pulse generator. In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 150 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

For example, if you are using an 8133A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 150 MHz plus 2% (153 MHz).

b Set the rest of the pulse generator parameters to the values shown in the following table.

Pulse Generator Setup

Timebase	Pulse Channel 2	Trigger	Pulse Channel 1
Mode: Int	Mode: Pulse ÷ 1	Disable (LED on)	Mode: Square
Freq: was set in previous step.	Delay: (not available in pulse mode)		Delay: 0 ps
	Width: Initially set to 1 ns. Change later (on page 35).		Width: (not available in square mode)
	Ampl: 0.25 V		Ampl: 0.25 V
	Offs: 1.0 V		Offs: 1.0 V
	Output: Enable (LED off)		Output: Enable (LED off)
	Comp: Normal (LED off)		Comp: Normal (LED off)
	Limit: Off (LED off)		Limit: Off (LED off)
	$\overline{\text{Output}}$: Enable (LED off)		$\overline{\text{Output}}$: Enable (LED off)

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3 Set up the oscilloscope.

a Set up the oscilloscope according to the following tables.

Oscilloscope Setup

Setup: Channel 1	Setup: Ch. 1 Probe	Setup: Channel 2	Setup: Ch. 2 Probe
On	Attenuation: 1.00:1	On	Attenuation: 1.00:1
Scale: 50 mV/div	Units: Volts	Scale: 50 mV/div	Units: Volts
Offset: 1 V	Attenuation Units: Ratio	Offset: 1 V	Attenuation Units: Ratio
Coupling: DC	External Gain: (n/a)	Coupling: DC	External Gain: (n/a)
Input: 50 ohm	Skew: (Set later. See page 33.)	Input: 50 ohm	Skew: 0.0 seconds
	External Offset: (n/a)		External Offset: (n/a)

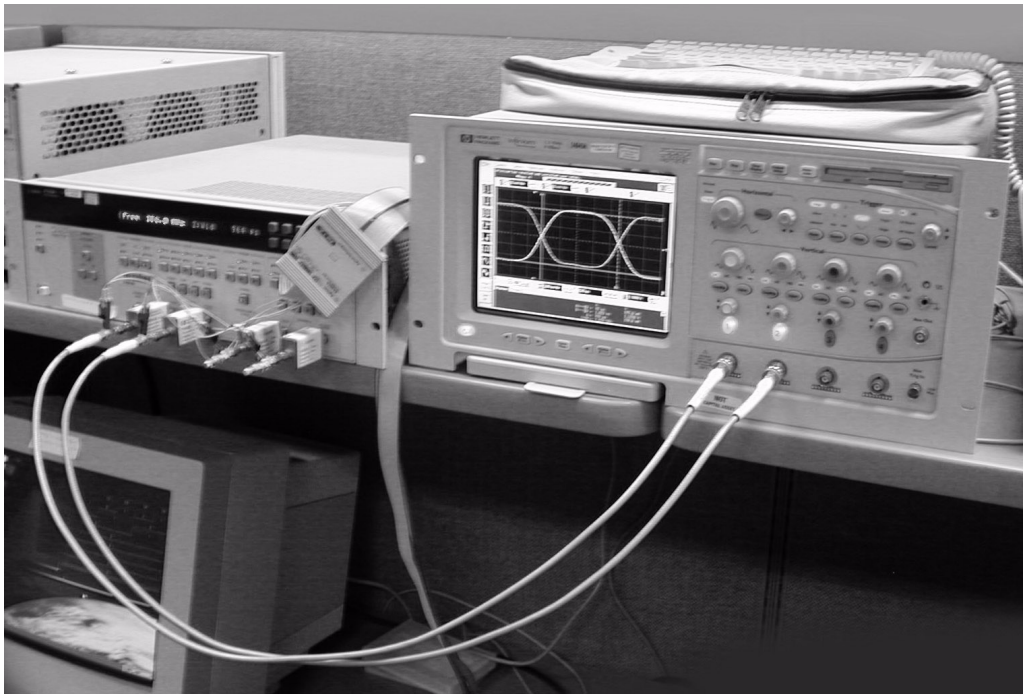
Setup: Channel 3	Setup: Channel 4
Off	Off

Setup: Horizontal	Setup: Trigger	Setup: Acquisition	Setup: Display
Scale: 500 ps	Mode: Edge	Sampling Mode: Equiv. Time	Waveforms: Connect dots
Position: 525 ps	Source: Channel 1	Memory Depth: Automatic	Persistence: Minimum
Reference: Center	Level: 1.00 V	Averaging: Enabled	Grid: On (and set intensity)
Delayed: not selected	Edge: Rising Edge	# of Averages: 4	Backlight Saver: as preferred
	Sweep: Auto		

Measure: Markers
Mode: Manual placement
All else: (n/a)

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Connect the Test Equipment

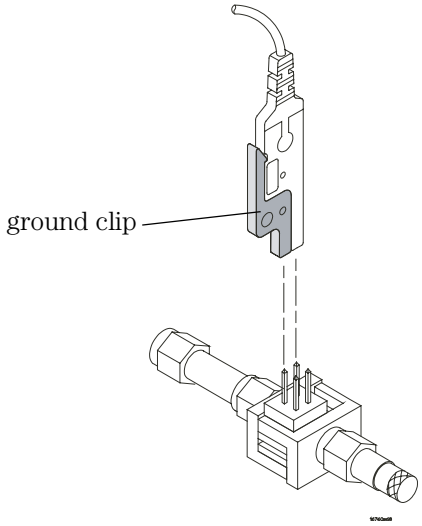


Connect the 16753/54/55/56A or 16950A Logic Analyzer Pod to the 8133A Pulse Generator

1. Connect a Transition Time Converter (if required—see page 22) to each of the four outputs of the 8133A pulse generator: Channel 1 OUTPUT, Channel 1 $\overline{\text{OUTPUT}}$, Channel 2 OUTPUT, Channel 2 $\overline{\text{OUTPUT}}$.
2. Connect the two SMA/Flying Lead test connectors (see "Assemble the SMA/Flying Lead Test Connectors" on page 23) *with* 50 ohm terminators to the Transition Time Converters at the 8133A pulse generator Channel 1 OUTPUT and Channel 1 $\overline{\text{OUTPUT}}$. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)
3. Connect the two SMA/Flying Lead test connectors *without* 50 ohm terminators to the Transition Time Converters at the 8133A pulse generator Channel 2 OUTPUT and Channel 2 $\overline{\text{OUTPUT}}$. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)
4. Connect an E5382A Flying Lead Probe Set to Pod 1 of the 16753/54/55/56A or 16950A logic analyzer.

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5 Connect the E5382A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the 8133A pulse generator's Channel 1 OUTPUT.

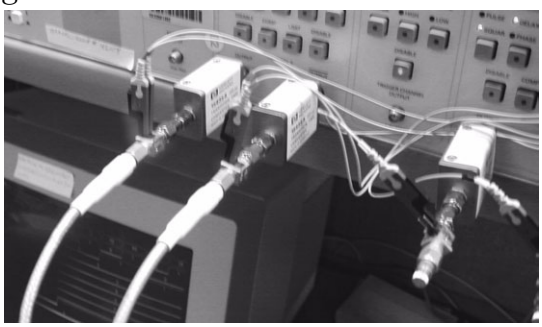


NOTE: Be sure to use the black ground clip (supplied with the E5382A Flying Lead Probe Set) and orient the leads so that the black clip is connected to one of the SMA/Flying Lead connector's ground pins!

6 Connect the E5382A Flying Lead Probe Set's $\overline{\text{CLK}}$ lead to the SMA/Flying Lead connector at the 8133A pulse generator's Channel 1 $\overline{\text{OUTPUT}}$. Again, be sure to use the black ground clip and orient the leads so that the black clip is connected to ground.

7 Connect the E5382A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 $\overline{\text{OUTPUT}}$.

8 Connect the E5382A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 OUTPUT.



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Connect the 8133A Pulse Generator Output to the 54845A Oscilloscope

9 Attach Male BNC to Female SMA adapters to Channels 1 and 2 on the 54845A oscilloscope.

10 Attach one end of an SMA cable to the Male BNC to Female SMA adapter on Channel 1 of the oscilloscope.

11 Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 OUTPUT of the 8133A pulse generator.

12 Attach one end of the other SMA cable to the Male BNC to Female SMA adapter on Channel 2 of the oscilloscope.

13 Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 $\overline{\text{OUTPUT}}$ of the 8133A pulse generator.

Verify and adjust the 8133A pulse generator DC offset

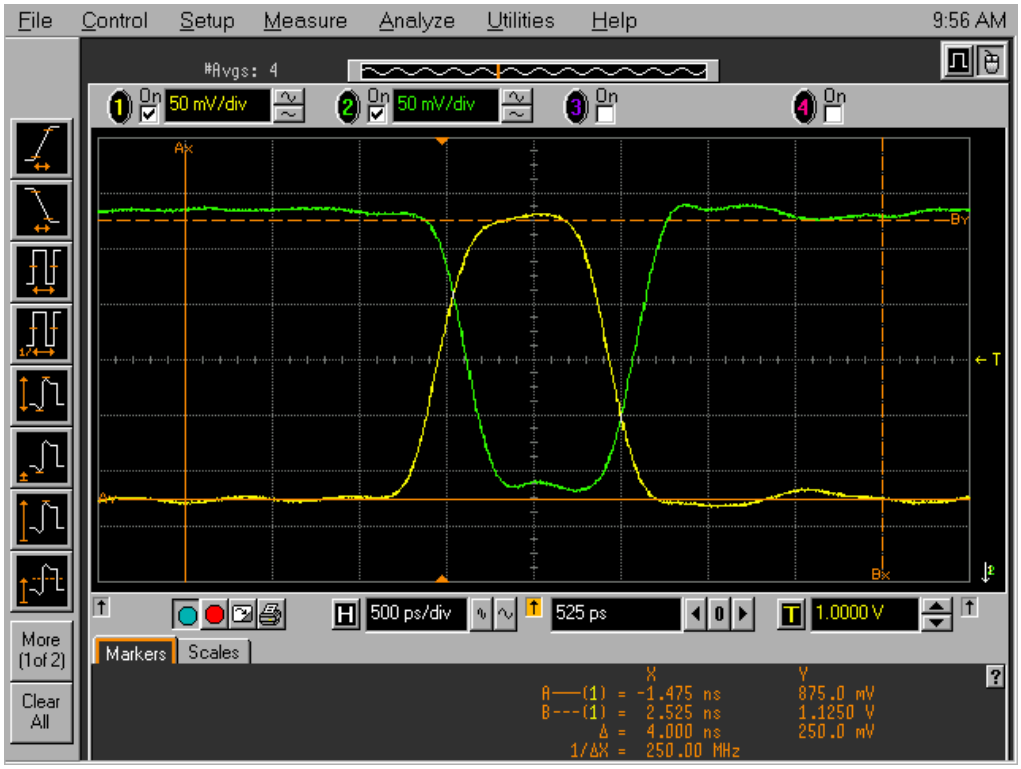
1 On the 54845A oscilloscope, select Measure from the menu bar at the top of the display.

2 Select Markers...

3 In the Markers Setup window set marker “Ay” to 0.875 V, and set marker

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"By" to 1.125 V.



4 Observe the waveforms on the oscilloscope display. If they are not centered within the "Ay" and "By" markers, adjust the 8133A pulse generator's Channel 1 OFFSET until the waveforms are centered as well as possible. (The resolution of the 8133A OFFSET setting is 20 mV.)

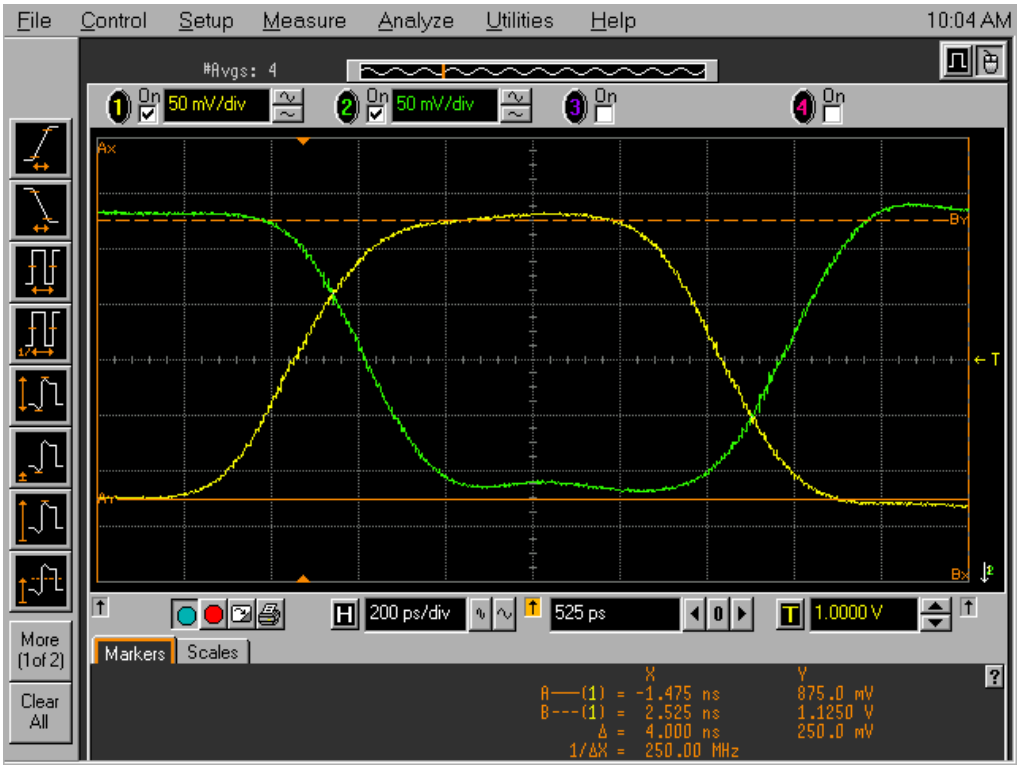
Deskew the oscilloscope

This procedure neutralizes any skew in the oscilloscope's waveform display.

1 On the 54845A oscilloscope, change the Horizontal scale from 500 ps/div to 200 ps/div. You can do this using the large knob in the Horizontal setup

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section of the front panel.



2 Select **Setup** from the menu bar at the top of the display.

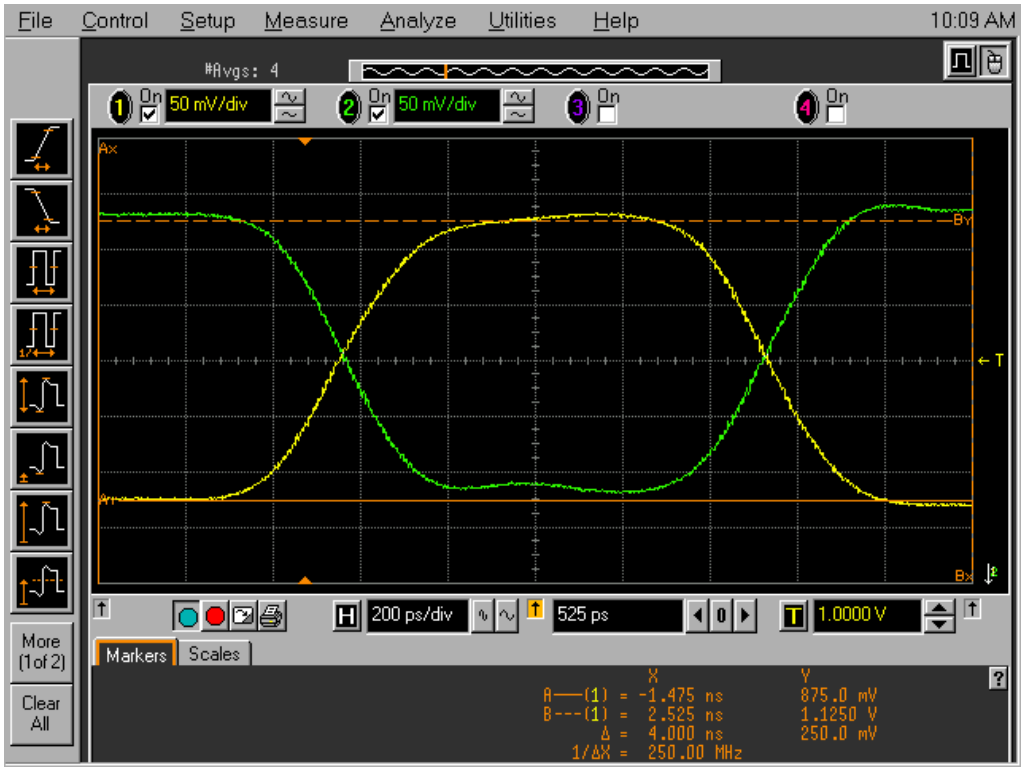
3 Select **Channel 1**.

4 Select **Probes**.

5 Click **Skew </>** to deskew Channel 1 and Channel 2 signals so that both channels cross the 54845A horizontal center line at the same time, at both ends of the eye (both crossings of the horizontal center line). The horizontal center of the graticule line is at 1 volt because the vertical offset

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was set to 1 volt in the oscilloscope setup described on page 29.



6 Select **Close** in the Probe Setup window.

7 Select **Close** in the Channel Setup window.

Set the 8133A pulse width

1 On the 8133A pulse generator, set the Channel 2 pulse width to 1 ns.

2 Observe the 54845A oscilloscope display. Change the Channel 2 pulse width of the 8133A pulse generator so that the pulse width measured at 1 volt on the oscilloscope is equal to 1 ns minus the measurement uncertainty and display resolution of the oscilloscope, further reduced by 35 ps for test margin.

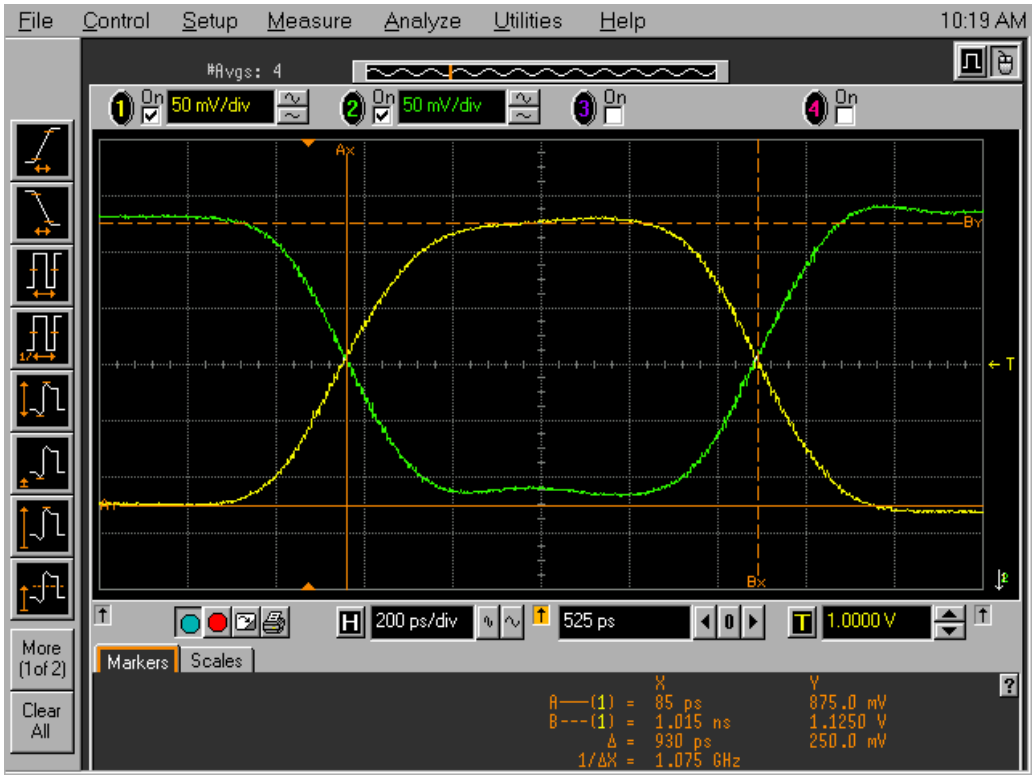
If you are using the 54845A/B oscilloscope, the measurement uncertainty is ±((0.007% * Δt) + (full scale/2x memory depth) + 30 ps) = ±30.15 ps. Add 5 ps for display resolution. Add 35 ps test margin.

1 ns - 30.15 ps - 5 ps - 35 ps = 930 ps. Set the pulse width as measured on

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the 54845A/B oscilloscope to 930 ps.

NOTE: On the oscilloscope move the Ax and Bx markers to the crossing points of the pulse and the horizontal center line. Read the pulse width at the bottom of the screen. It is displayed as "Δ=".



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Testing the Module Using a 16900-Series Mainframe

The following sections explain how to test the minimum master-to-master clock time and minimum eye width.

Use the following instructions to test the module using a 16900-series mainframe. If you are using a 16700-series mainframe, use the instructions beginning on page 61.

1 Record the 16753A, 16754A, 16755A, 16756A, or 16950A logic analyzer's model and serial number in the Performance Test Record (see page 60). Record your work order number (if applicable) and today's date.

2 Record the test equipment information in the "Test Equipment Used" section of the Performance Test Record.

3 Turn on the logic analysis system.

NOTE: Before testing the performance of the module, warm-up the logic analyzer and the test equipment for 30 minutes.

a Connect the keyboard and monitor to the rear panel of the logic analysis mainframe (16900A only).

b Connect the mouse to the rear panel of the mainframe.

c Plug in the power cord to the power connector on the rear panel of the mainframe.

d Turn on the main power switch on the mainframe front panel.

While the logic analysis system is booting, observe the boot dialogue for the following:

- ensure all of the installed memory is recognized
- any error messages
- interrupt of the boot process with or without error message

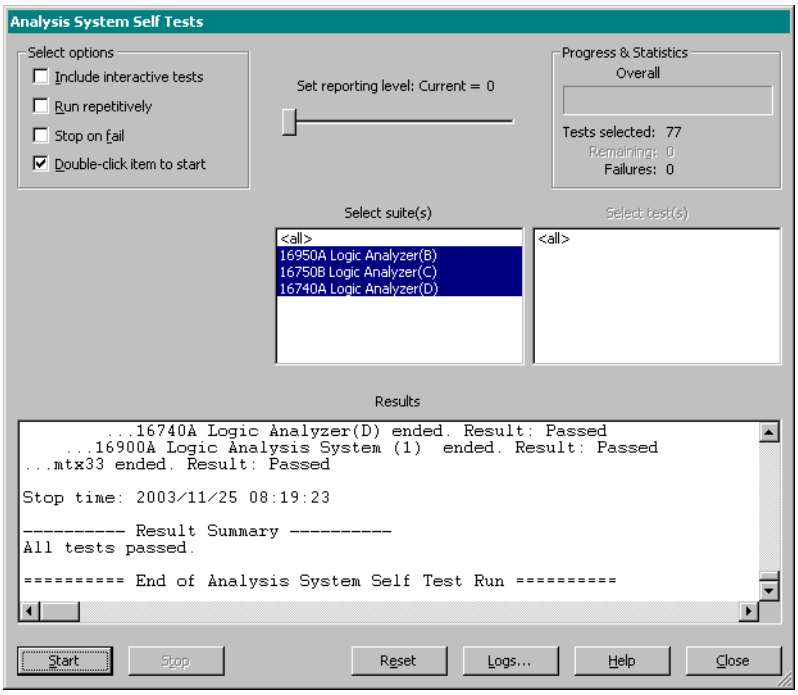
4 During initialization, check for any failures.

If an error or an interrupt occurs, refer to the Agilent Technologies 16900A-series Logic Analysis System Service Guide for troubleshooting information.

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Do a self-test on the 16900-series logic analysis system

a When the logic analysis system has finished booting, the Waveform window appears. Select Help→Self-Test... from the main menu. The Analysis System Self Tests window will appear.



b In the Select Suite(s) list, select <all>. This will cause <all> to be selected in the Select Test(s) list.

c Select Start. This will perform a complete system self-test.

The progress of the self tests is displayed in the Progress & Statistics area of the window.

d When the self-tests are complete, check the Results window to ensure that the Result Summary says that all tests passed. If all tests did not pass, refer to “Troubleshooting” on page 89.

e Select the Close button to close the Analysis System Self Tests window.

f If all module self-tests pass, then record “PASS” in the “Logic Analysis System Self-Tests” section of the Performance Test Record (page 60).

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Configure the 16900-Series Logic Analysis System

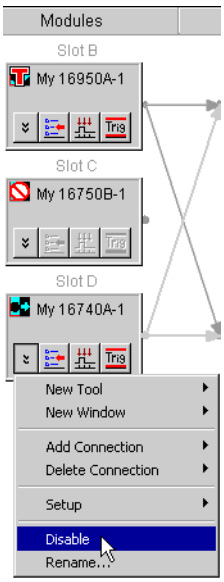
1 Exit the logic analysis application (from the main menu, choose File→Exit) and then restart the application. This puts the logic analysis system into its initial state.

2 Disable all logic analyzers other than the analyzer under test.

a Select the Overview tab at the bottom of the main window.

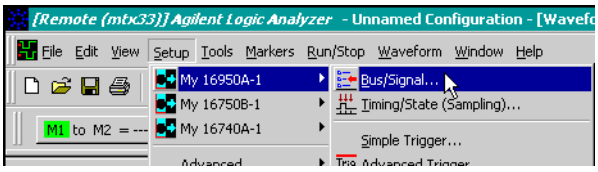


b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.



3 Set up the bus and signals.

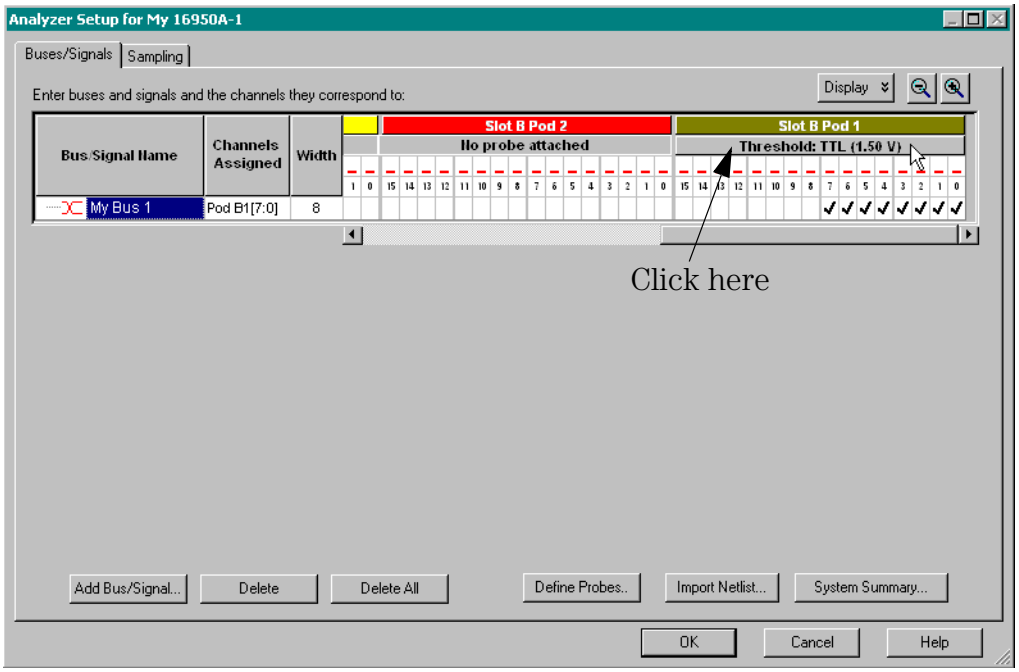
a From the Logic Analysis System main menu, select Setup→My 16950A→Bus/Signal....



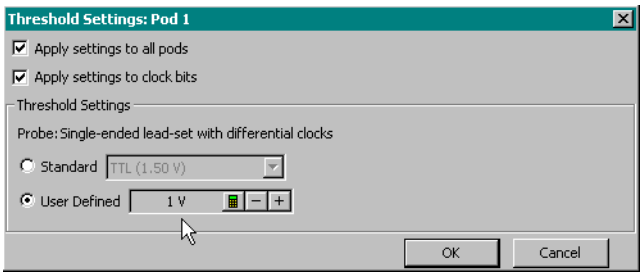
b In the Analyzer Setup window, choose the Threshold button for Pod 1. The Threshold Settings window will appear.

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NOTE: The E5382A probe must be connected to the logic analyzer pod as described on page 30.



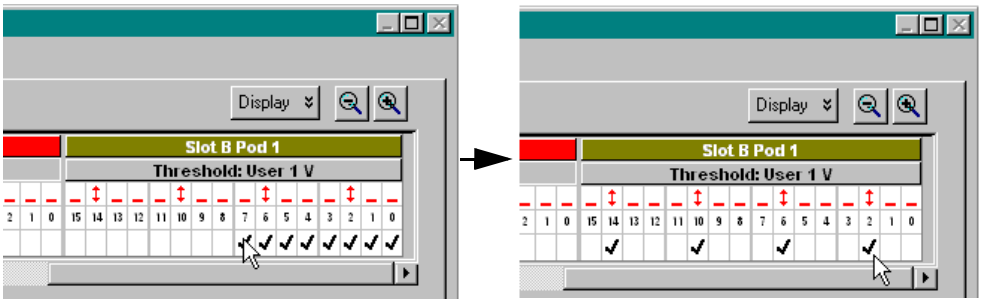
c Set the threshold value for Pod 1 of the 16950A logic analyzer to 1 V.



d The activity indicators will now show activity on the channels that are connected to the pulse generator. Un-assign all channels. Hint: you can do this quickly by clicking on the left-most check mark and dragging to the right across all of the other check marks. If you have a model 16902 or 16903A logic analysis system mainframe you can touch the

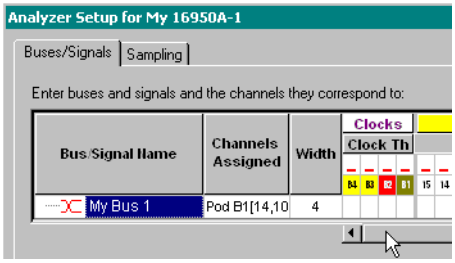
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touchscreen and drag across with your finger.

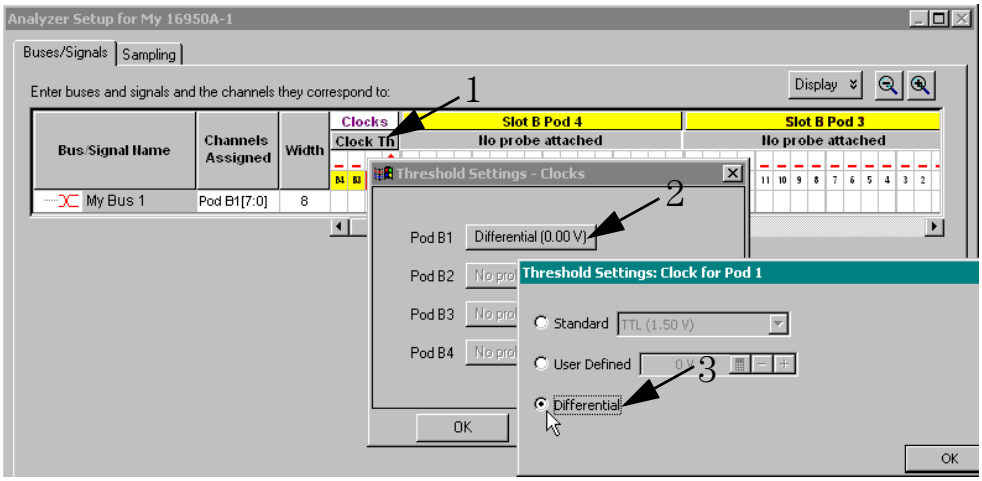


e Click (or touch) to select channels 2, 6, 10 and 14 as shown in the picture above.

f Drag the scroll bar all the way to the left.



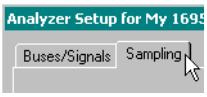
g Select the **Clock Thresholds** button and set the clock threshold to **Differential**. The activity indicator will show activity on clock 1.



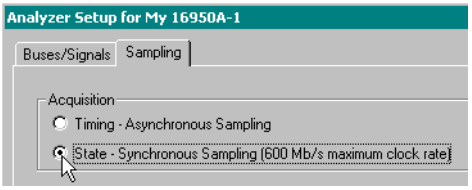
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4 Set the sampling mode.

a Select the **Sampling** tab of the Analyzer Setup window.

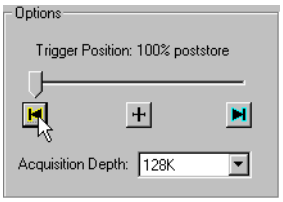


b Select **State Mode**.

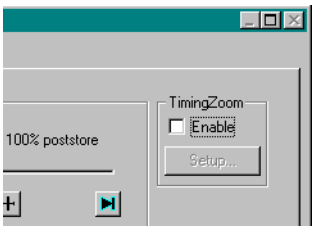


c Set the Trigger Position to **100% Poststore**.

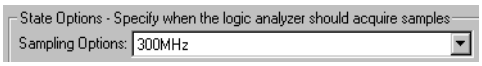
d Set the Acquisition Depth to **128K**.



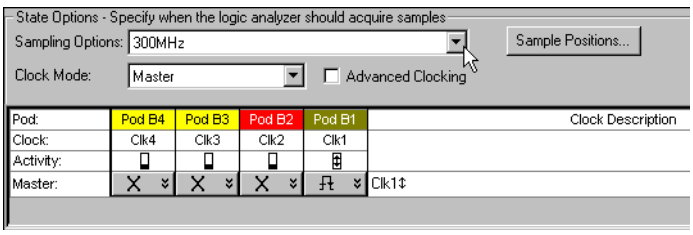
e Clear the Timing Zoom check box to turn Timing Zoom off.



f Ensure that the sampling speed is set to **300 MHz** in the Sampling Options box.

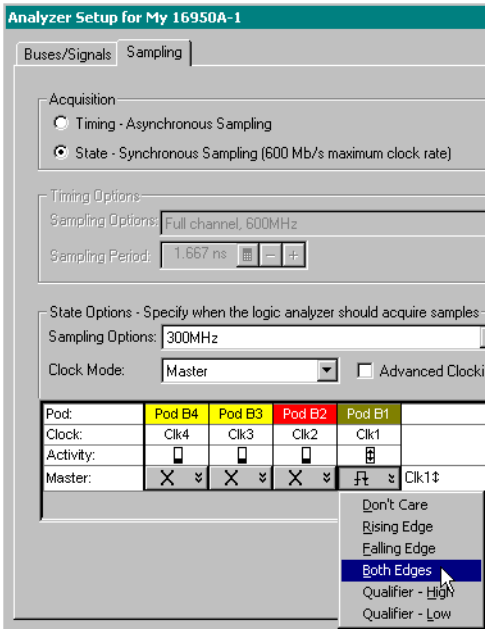


g Ensure that the Clock Mode is set to **Master**.



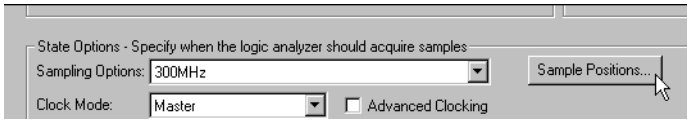
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h Set the clock mode to **Both Edges**.

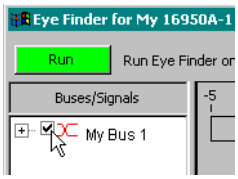


Adjust sampling positions using Eye Finder

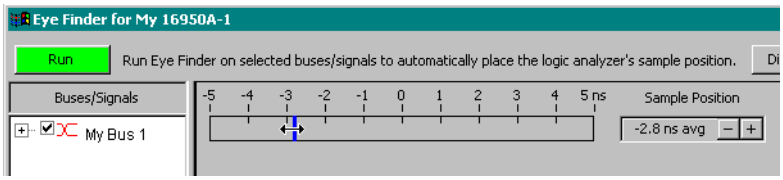
1 Select the **Sample Positions** button. The Eye Finder window will appear.



2 In the “Buses/Signals” section of the Eye Finder window, ensure that the check box next to “My Bus 1” is checked.

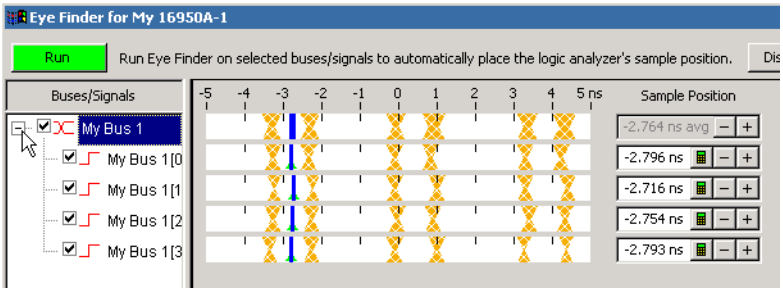


3 Drag the blue bar for “My Bus 1” to approximately -2.8 ns.



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4 Select the plus sign to expand bus “My Bus 1”.



Align the blue bars vertically

Initially, the blue bars will be vertically aligned. After running Eye Finder, the blue bars will not be vertically aligned because an independent sample position will be determined for each channel.

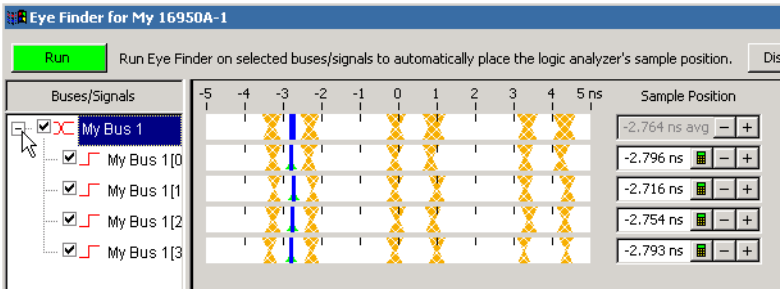
5 If the blue bars in the Eye Finder display are not vertically aligned:

a In the “My Bus 1” row, grab the right-most blue bar with the mouse pointer and move it all the way to the left. Release the mouse button. This will vertically align all of the blue bars.

6 Using the mouse pointer, grab the blue bar for “My Bus 1 (4 channels)” and move it to the recommended starting position of -2.8 ns. All of the blue bars will follow.

7 Select the Run button in the Eye Finder window.

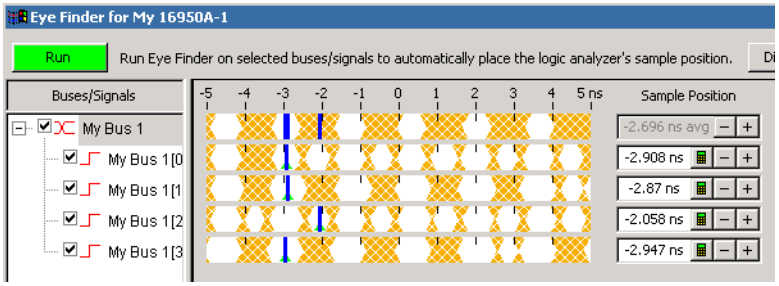
8 Ensure that an eye appears for each bit near the recommended starting position. Depending on your test setup, the eye position may vary. Any skew between channel 1 and channel 2 of your pulse generator will cause the eye position to shift to the left or right in the Eye Finder display. A shift of up to 0.5 ns should be considered normal. The important point is that your Eye Finder display should look similar to the picture below (although it may be shifted left or right), and Eye Finder must be able to place the blue bars in the narrow eye.



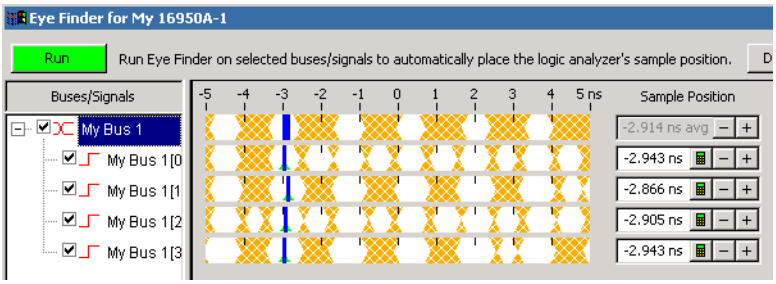
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To re-align a stray channel

If the blue bar for a particular bit does not appear in its eye near the recommended starting position, then do the following steps to realign the sampling position of the stray channel. In the following example, the sampling position of one channel (My Bus 1 [2]) must be realigned with the sampling position of the other channels. (The following example shows the analyzer in 600 Mb/s mode.)



1. Using the mouse, drag the sample position (blue line) of a stray channel (channel "My Bus 1 [2]" in the above example) so that it is in the same eye as the other channels. The Suggested Position from Eye Finder (green triangle) will also move to the new eye.
2. Repeat the above step for all remaining stray channels.
3. Select the Run button in the Eye Finder window. Eye Finder will recalculate the new sample positions based on the sample position changes. The following example shows all sampling positions aligned and in the correct eye.



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Test Pod 1 in 300 Mb/s Mode

The steps that follow include pass/fail criteria.

Determine PASS/FAIL (1 of 2 tests)

1 PASS/FAIL: If an eye exists near -2.8 ns for every bit, and Eye Finder places a blue bar in the narrow eye for each bit, then the logic analyzer passes this portion of the test. Record the result in the "Eye Finder locates an eye for each bit" section of the Performance Test Record (page 60).

2 If an eye does not exist near -2.8 ns for every bit or Eye Finder can not place the blue bar in the narrow eye, then the logic analyzer fails the test. Record the result in the "Eye Finder locates an eye for each bit" section of the Performance Test Record (page 60).

Close the Eye Finder and Analyzer Setup Windows

1 Select OK to close the Eye Finder window.

2 Select OK to close the Analyzer Setup window.

Configure the markers

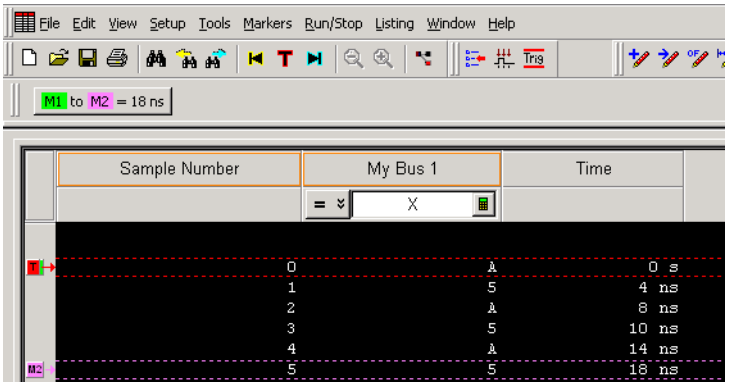
Data must be acquired before the markers can be configured. Therefore, you will need to run the analyzer to acquire data.

1 Switch to the Listing window by selecting the Listing tab at the bottom of the main window.

2 Select the Run icon .

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3 Data will appear in the Listing Window upon completion of the run.



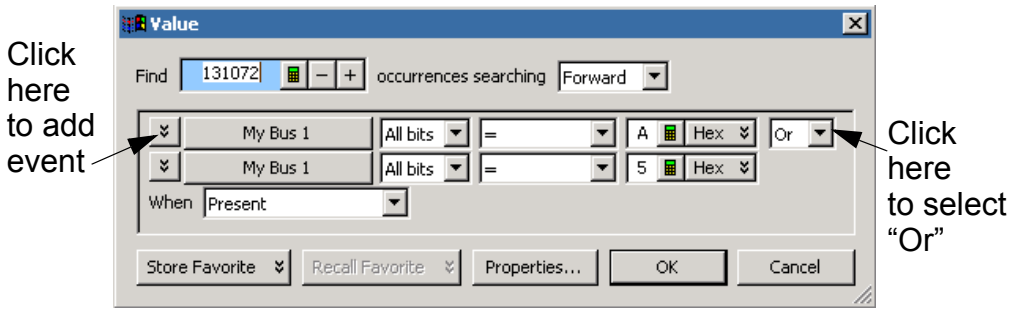
4 From the Main Menu choose Markers→New.



a You can accept the default name for the new marker.

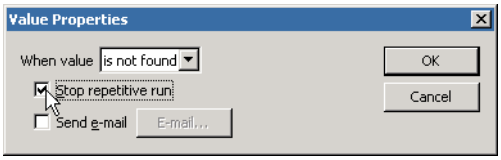
b Change the Position field to Value.

c Select the Occurs... button and create the marker setup shown below.



5 In the Value window, select the Properties... button.

6 In the Value Properties window, select Stop repetitive run when value is not found.



7 Select OK to close the marker Value Properties window.

8 Select OK to close the marker Value window. The system will search the display for the occurrences specified.

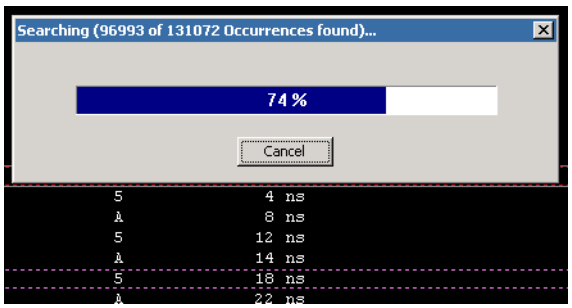
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9 Select OK to close the New Marker window.

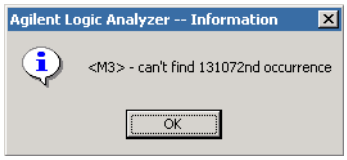
Determine PASS/FAIL (2 of 2 tests)

Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error window will appear.

1 Select the Run Repetitive icon . Let the logic analyzer run for about one minute. The analyzer will acquire data and the Listing Window will continuously update.



If the "can't find occurrence" window appears, then the logic analyzer fails the test.



Check your test setup. If the failure is not the result of a problem with the test setup, record the failure in the "Minimum Master to Master Clock Time/ Minimum Pulse Width" section of the Performance Test Record.

NOTE: Be sure that the black ground clip is making good contact with the ground pin on the test connector.

2 After about one minute, select the Stop button  to stop the acquisition.

If the "can't find occurrence" window does not appear, then the analyzer passes the test. Record "Pass" in the "Minimum Master to Master Clock Time/ Minimum Pulse Width" section of the Performance Test Record.

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NOTE:

As a point of curiosity, you may want to determine the absolute minimum pulse width and/or absolute maximum frequency at which data can be acquired. The "Performance Test Record" on page 60 does not include places for recording these values because the Performance Verification procedure only verifies that the logic analyzer meets specifications. Determination of additional parameters is not required, but may be performed at the discretion of the calibration laboratory.

On some pulse generators, the signal outputs may become unstable for a short period of time when the signal parameters are adjusted. Adjusting the pulse generator while the logic analyzer is running can cause a false failure.

If the error message is displayed immediately after making an adjustment to the pulse generator, select OK to close the error display window and re-run the logic analyzer.

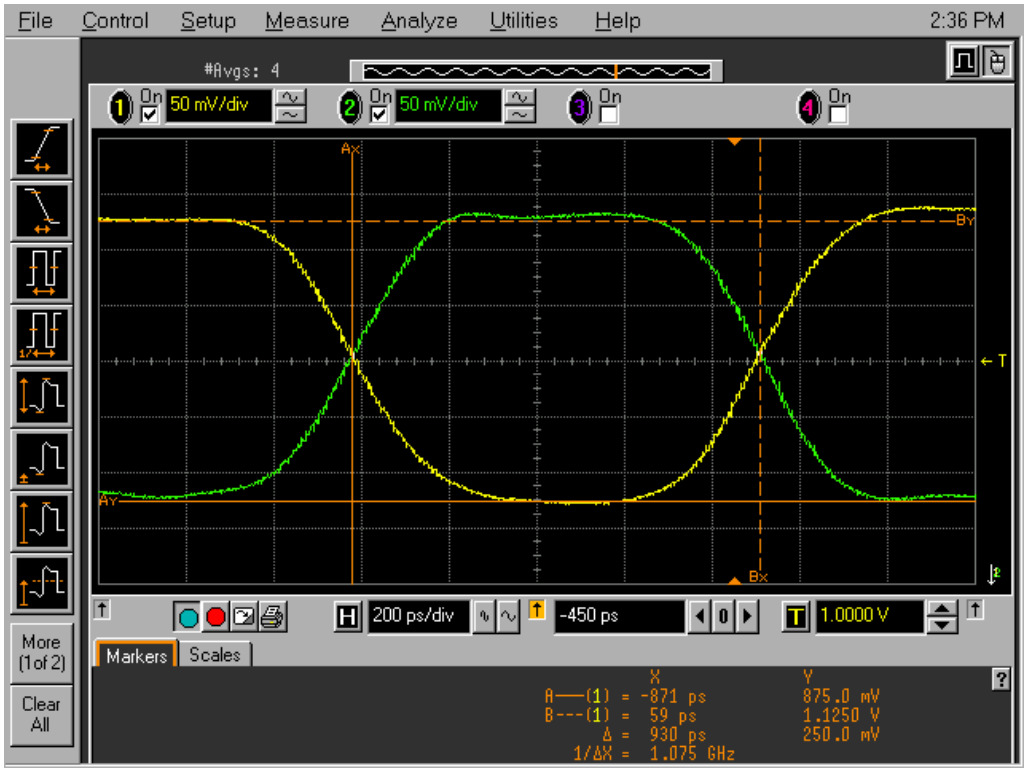
Test the complement of the bits (300 Mb/s mode)

Now test the logic analyzer using complement data.

1. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.
2. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -450 ps (or as required) to center the measured pulse on the oscilloscope display.
3. Verify the DC offset and adjust it if necessary. See page 32.
4. Deskew the oscilloscope if necessary. See page 33.
5. Adjust the oscilloscope's measurement markers to measure the pulse width. Set the markers so that Δ=930 ps (this assumes you are using the 8133A pulse generator and the Infiniium oscilloscope). Adjust the pulse generator so that the pulse width is 930 ps as measured by the markers.

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See page 35 for details.



6 Adjust the sampling positions (run Eye Finder). See page 43.

7 Determine pass or fail (1 of 2 tests). See page 46.

8 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main logic analyzer window.

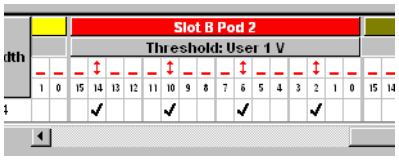
9 Select the Run Repetitive icon .

10 Determine pass or fail (2 of 2 tests). See page 48.

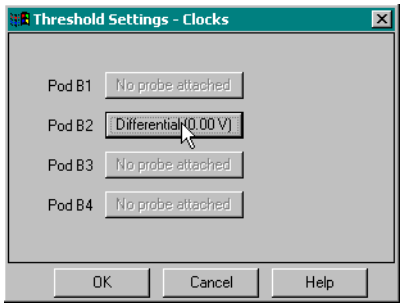
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Test Pod 2 in 300 Mb/s Mode

1. Disconnect the E5382A Flying Lead Probe Set from Pod 1 and connect it to Pod 2 of the logic analyzer. Do not remove the flying leads that are connected to CLK, $\overline{\text{CLK}}$, and the data channels.
2. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.
3. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.
4. Verify the DC offset and adjust it if necessary. See page 32.
5. Deskew the oscilloscope if necessary. See page 33.
6. Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 35.
7. From the Logic Analysis System main menu, select **Setup→My 16950A→Bus/Signal...**
8. Scroll to the right and unassign all Pod 1 bits.
9. Set the Pod 2 threshold to 1 volt (just as you did for Pod 1 on page 40).
10. Assign bits 2, 6, 10, and 14 of Pod 2.



11. Scroll to the left and select the **Clock Thresholds** button. In the "Threshold Settings - Clocks" window, select the **Pod 2** clock threshold button. The "Threshold Settings: Clock for Pod 2" window will appear. Set the Clk2 threshold to **Differential**.



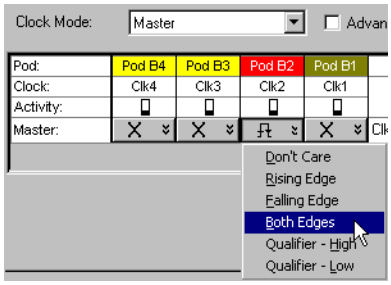
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12 Select the OK button to close the “Threshold Settings: Clock for Pod 2” window.

13 Select the OK button to close the “Threshold Settings - Clocks” window.

14 Select the Sampling tab (at the top of the window). In the State Options area, set clock Clk1 to Don’t Care.

15 Set Clk2 to Both Edges.



16 Adjust the sampling positions using Eye Finder. Be sure to expand “My Bus 1” and use the recommended starting position noted on page 44. Realign any stray channels if necessary. See page 45.

17 Determine pass or fail (1 of 2 tests). See page 46.

18 Select OK to close the “Analyzer Setup” window.

19 Switch to the Listing window by selecting the Listing tab at the bottom of the main logic analyzer window.

20 Select the Run Repetitive icon .

21 Determine pass or fail (2 of 2 tests). See page 48.

Test the complement of the bits (Pod 2, 300 Mb/s mode)

1 Test the complement of the bits. See page 49.

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Test Pods 3 and 4 in 300 Mb/s Mode

1 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate. Test using clock Clk3 for Pod 3 and clock Clk4 for Pod 4. Upon completion, the logic analyzer is completely tested in the 300 Mb/s mode.

Test Pod 1 in 600 Mb/s Mode

Clock "Clk1" will be used for testing all pods in the 600 Mb/s mode. Therefore two E5382A Flying Lead Probe sets will be required when testing pod 2.

1 Disconnect the E5382A Flying Lead Probe from Pod 4 of the logic analyzer and connect it to Pod 1 of the logic analyzer.

2 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

3 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.

4 Set the frequency of the pulse generator. The logic analyzer will be tested using a double-edge clock. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 300 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

   For example, if you are using an 8133A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 300 MHz plus 2% (306 MHz).

5 Verify the DC offset and adjust it if necessary. See page 32.

6 Verify the oscilloscope Deskew and adjust if necessary. See page 33.

7 Adjust the measured pulse width from the pulse generator to 1 ns (minus the test margin) as described on page 35.

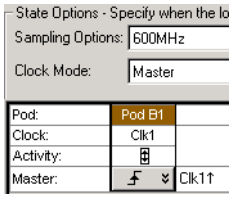
8 From the Logic Analysis System main menu, select Setup→My

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16950A→Timing/State (Sampling)...

9 In the State Options section, Sampling Options field, select the “600 MHz” mode. A warning will appear stating that one Pod pair is required for timetag storage. Select OK.

10 Ensure that the Clk1 mode is set to Rising Edge.



11 In the logic analyzer’s Buses/Signals window, unassign all bits.

12 Assign bits 2, 6, 10, and 14 of Pod 1.

13 Ensure that the Pod 1 threshold is set to 1 volt. See page 40.

14 Use the scroll bar at the bottom of the window to scroll to the left (if scrolling is necessary) and select the Clock Thresholds button. In the Clock Thresholds window, ensure that the Clk1 threshold is set to Differential.

a Select OK to close the Clock Thresholds window.

Determine and set Eye Finder Position (600 Mb/s mode)

15 Select the Sampling tab.

16 Select the Sampling Positions button.

17 In the Eye Finder window, expand “My Bus 1”.

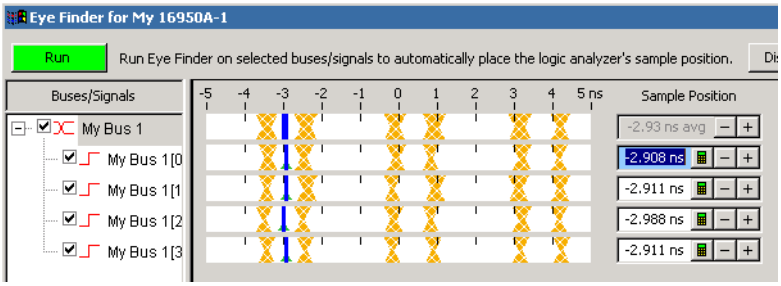
18 If the blue bars are not vertically aligned, align them. See page 44.

19 Grab the blue bar for “My Bus 1” and move it to approximately -2.9 ns. All blue bars will follow.

20 Run Eye Finder and note the average sampling position chosen by Eye Finder:_____ns. In the following example, the average sampling position is -2.93 ns. Note that in this step, you place the blue bars in the narrow window (not the wide window) that appears to the left of zero in the Eye Finder display. Then run Eye Finder. The position may be different based on your test setup. Bring stray channels into alignment if necessary. See

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page 45.



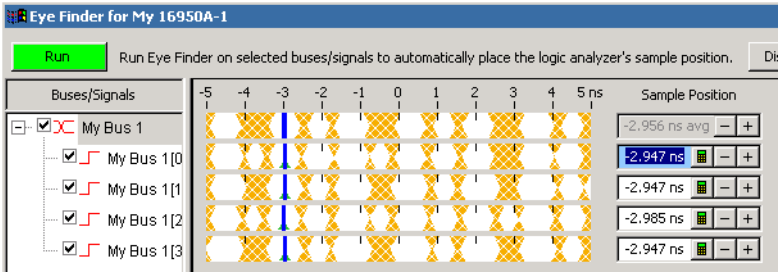
21 Select OK to close the Eye Finder window.

22 Set the Clk1 mode to "Both Edges."

23 Open the Eye Finder window, and align the blue bars vertically. See page 44.

24 Grab the blue bar for "My Bus 1" and move it to the recommended starting position you noted in the prior step.

25 Run Eye Finder again. Some eyes may close, but the eyes in the sampling position you chose on page 54 should remain open.



When you close the Analyzer Setup window a dialog will appear. Answer Yes to erase the data and continue.

26 Perform the procedure "Determine PASS/FAIL (1 of 2 tests)" on page 46.

27 Select the Run Repetitive icon .

28 Perform the procedure "Determine PASS/FAIL (2 of 2 tests)" on page 48.

Test the complement of the bits (Pod 1, 600 Mb/s mode)

Now test the logic analyzer using complement data.

1 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, select

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COMP.

2 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -450 ps (or as required) to center the measured pulse on the oscilloscope display.

3 Verify the DC offset and adjust it if necessary. See page 32.

4 Deskew the oscilloscope if necessary. See page 33.

5 Verify that the pulse width is set to 1 ns. See page 35.

6 Run Eye Finder and align stray channels if necessary.

7 Perform the procedure "Determine PASS/FAIL (1 of 2 tests)" on page 46.

8 Select the Run Repetitive icon .

9 Perform the procedure "Determine PASS/FAIL (2 of 2 tests)" on page 48

Test Pod 2 in 600 Mb/s Mode

1 Leave the first E5382A Flying Lead Probe Set connected to Pod 1 of the logic analyzer. Remove the Pod 1 flying leads 2, 6, 10, and 14 from the SMA/Flying Lead test connectors. Do not remove the flying leads that are connected to CLK and $\overline{\text{CLK}}$ flying leads.

2 Connect the second E5382A Flying Lead Probe Set to Pod 2.

3 Connect the Pod 2 E5382A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 OUTPUT.

4 Connect the Pod 2 E5382A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the 8133A pulse generator's Channel 2 $\overline{\text{OUTPUT}}$.

5 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

6 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.

7 Verify the DC offset and adjust it if necessary. See page 32.

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8 Deskew the oscilloscope if necessary. See page 33.

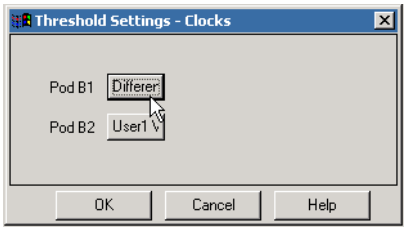
9 Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 35.

10 Unassign all Pod 1 bits.

11 Assign bits 2, 6, 10, and 14 of Pod 2.

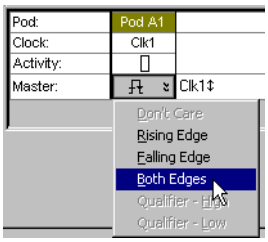
12 Ensure that the Pod 2 threshold is set to 1 volt (just as you did for Pod 1 on page 40).

13 Scroll to the left and select the **Clock Thresholds** button. In the "Threshold Settings - Clocks" window, ensure that the Pod 1 clock threshold is set to Differential. The Pod 2 clock setting doesn't matter.



a Select **OK** to close the threshold window(s).

14 Select the **Sampling** tab and verify that Clk1 is set to "Both Edges".



15 Adjust the sampling positions using Eye Finder. Be sure to expand "My Bus 1", align the blue bars vertically, and use the starting position you noted on page 54. Realign any stray channels if necessary. See page 45.

16 Determine pass or fail (1 of 2 tests). See page 46.

17 Switch to the Listing window.

18 Select the Run Repetitive icon .

19 Determine pass or fail (2 of 2 tests). See page 48.

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Test the complement of the bits (Pod 2, 600 Mb/s mode)

1 Test the complement of the bits on Pod 2. You can use the procedure "Test the complement of the bits (300 Mb/s mode)" on page 49 as a guideline.

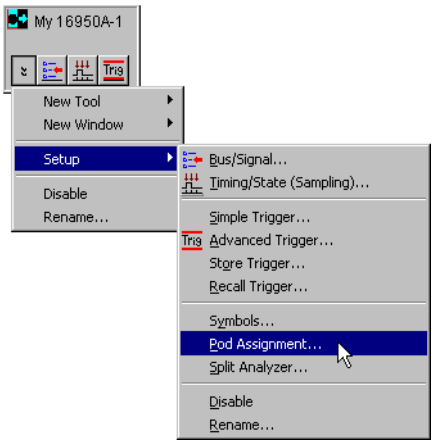
2 Upon completion, the logic analyzer is completely tested.

Test Pods 3 and 4 in 600 Mb/s Mode

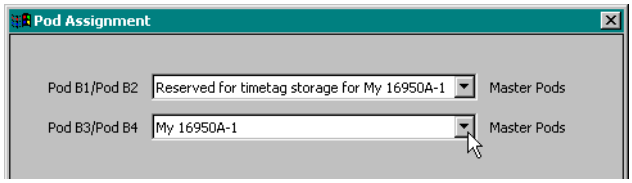
Pods 1 and 2 must be used for time tag storage when using Pods 3 and 4 in 600 Mb/s mode.

1 Select the Overview tab.

2 Select My 16950A→Setup→PodAssignment...



3 Reserve Pods 1 and 2 for timetag storage, and assign Pods 3 and 4 to My 16950A. The acquired data will be erased.



4 Re-configure the markers to search for 131071 occurrences instead of 131072 (see "Configure the markers" on page 46).

5 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate. You must use Clk1 on Pod 1 for all tests in

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the 600 Mb/s mode because the other clocks are not available in this mode. Upon completion, the logic analyzer is completely tested.

6 Complete the Performance Test Record on page 60.

Conclude the State Mode Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a From the Main Menu, choose File→Exit. At the dialog "Do you want to save the current configuration?" select No.

Ending and restarting the logic analysis session will re-initialize the system.

b Disconnect all cables and adapters from the pulse generator and the oscilloscope.

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Performance Test Record

LOGIC ANALYZER MODEL NO. (circle one): 16753A 16754A 16755A 16756A 16950A

Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Year/4000 hours Recommended next testing:

TEST EQUIPMENT USED

Pulse Generator Model No.	Oscilloscope Model No.
Pulse Generator Serial No.	Oscilloscope Serial No.
Pulse Generator Calibration Due Date:	Oscilloscope Calibration Due Date:

MEASUREMENT UNCERTAINTY

Clock Rate	**Pulse Width (Eye Width)**
Pulse Generator Frequency Accuracy: 8133A: 1% of setting	Oscilloscope Horizontal Accuracy: 54845B: ±[((0.007%) (Δt)+(full scale/(2x memory depth))+30 ps] ≅ 30 ps Oscilloscope Display Resolution: 54845B: ±5 ps
Setting: 150 MHz + 2% = 153 MHz 300 MHz + 2% = 306 MHz	Pulse Width setting: 930 ps PWmax(worst case): 930 ps+30 ps+5 ps = 965 ps

TEST RESULTS

Logic Analysis System Self-Tests (Pass/Fail):				
Performance Test: Minimum Master to Master Clock Time and Minimum Pulse Width				
	300 Mb/s mode		**600 Mb/s mode**	
Pulse Generator Settings	Freq: 150 MHz plus test margin Pulse Width: 1 ns less test margin		Freq: 300 MHz plus test margin Pulse Width: 1 ns less test margin	
Test Criteria	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail):				
Pod 2 Results (pass/fail):				
Pod 3 Results (pass/fail):				
Pod 4 Results (pass/fail):				

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Testing the module using a 16700-series Mainframe

The following sections explain how to test the minimum master-to-master clock time and minimum eye width.

Use the following instructions to test the module using a 16700-series mainframe. If you are using a 16900-series mainframe, use the instructions beginning on page 37.

NOTE: The 16950A module cannot be tested in a 16700-series mainframe. It must be tested in a 16900-series mainframe.

1 Turn on the logic analysis system.

NOTE: Before testing the performance of the module, warm-up the logic analyzer and the test equipment for 30 minutes.

a Connect the keyboard and monitor to the rear panel of the logic analysis mainframe (16700B only).

b Connect the mouse to the rear panel of the mainframe.

c Plug in the power cord to the power connector on the rear panel of the mainframe.

d Turn on the main power switch on the mainframe front panel.

While the logic analysis system is booting, observe the boot dialogue for the following:

- ensure all of the installed memory is recognized
- any error messages
- interrupt of the boot process with or without error message

2 During initialization, check for any failures.

If an error or an interrupt occurs, refer to the Agilent Technologies 16700B-series Logic Analysis System Service Guide for troubleshooting information. Note that if an Agilent 16753/54/55/56A module is temporarily installed in a mainframe only to test the performance of the module, then the mainframe may report that the module will require an operational accuracy calibration. This is expected, and step 4 in this procedure will clear this error message.

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Do a self-test on the 16700-series logic analysis system

a When the logic analysis system has finished booting and the System window appears (that is, a session has started), click on the System Admin icon.

b Under the Admin tab, click on Self-Test... in the query pop-up, select Yes to exit the current session.

The Self-Test closes the current session because the test algorithms leave the system in an unknown state. Re-launching the session at the end of the self-test will ensure the system is properly initialized.

c In the Self-Test window select Test All.

When the tests are finished, the Status will change to TEST passed or TEST failed. You can find detailed information about the test results in the Status Message field of the Self-Test window.

Some system CPU board tests may return a status of Untested because they require user action. Procedures to do these tests are found in the Agilent Technologies 16700B-series Logic Analysis System Service Guide. For the purposes of testing the Agilent 16753/54/55/56A module performance, running untested system CPU board tests are not required. If these tests are not done, the Agilent 16753/54/55/56A performance test is not affected.

d When the self-tests are complete, select Quit to exit the test menu.

e Record a PASS in the Performance Test Record if all module self-tests pass.

1 Start a session and perform operational accuracy calibration.

a In the Session Manager window, select "Start Session" to re-launch a logic analysis session.

b In the Logic Analysis System window, select the module icon, then select Setup and Trigger. A Setup and Trigger window will appear.

c In the Setup and Trigger window, click on the Calibration tab. Follow the instructions under the Calibration tab to perform an operational accuracy calibration on the Agilent 16753/54/55/56A module.

Repeat the above step for each single-card Agilent 16753/54/55/56A module installed in the mainframe that is being tested. If any calibration status returns "failed," then the Agilent 16753/54/55/56A module requires repair. If the calibration status returns "passed" for all pods, then record a PASS in the “Self Tests” section of the performance test record at the end of this chapter.

d Proceed to the next section when the operational accuracy calibration

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is complete.

Configure the 16700-Series Logic Analysis System

1 Configure the Sampling settings.

a In the Logic Analysis System window, select the 16753/54/55/56A logic analyzer icon, then select Setup and Trigger. A Setup and Trigger window will appear.

b In the logic analyzer Setup and Trigger window, select the Sampling tab.

c Under the Sampling tab, select Timing Zoom....

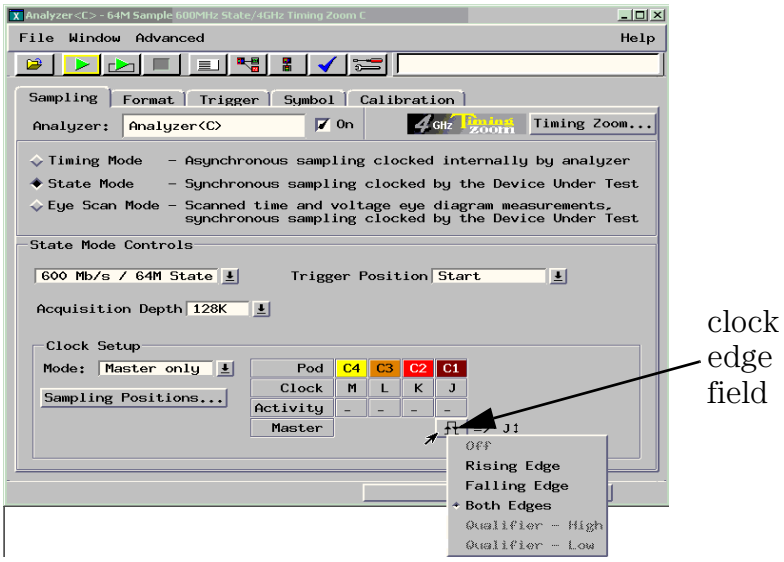
d Set Timing Zoom to Off.

e Close the Timing Zoom Controls window.

f Under the Sampling tab, select the State Mode button.

g Under State Mode Controls, ensure that "300 Mb/s / xxM State" mode is selected. ("xxM" indicates the module's memory depth.)

h Under Clock Setup, at the bottom of the J clock column, select the clock edge field and set the J clock to "Both Edges".



2 Configure the Acquisition settings.

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

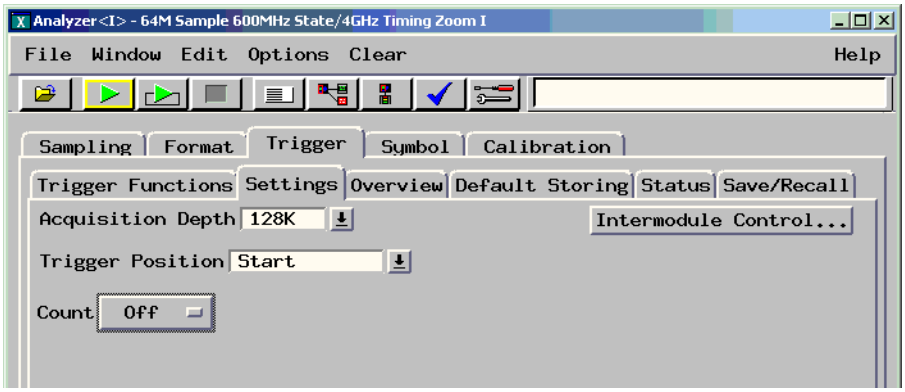
b Under the Trigger tab, select the Settings subtab.

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c Select the Acquisition Depth field, then select 128K.

d Select the Trigger Position field, then select Start.

e Select the Count field, then select Off.

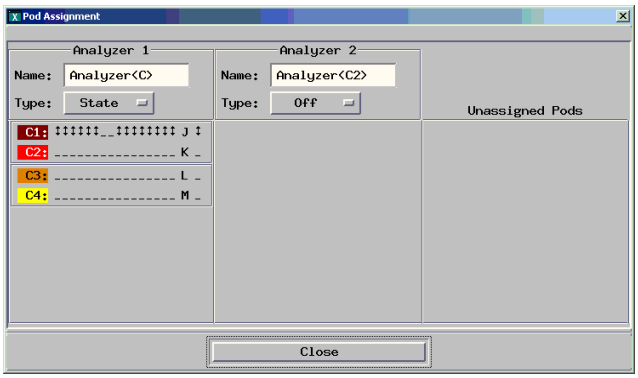


3 Configure the Format settings.

a In the logic analyzer Setup and Trigger window, select the Format tab.

b Under the Format tab, select Pod Assignment.

c In the Pod Assignment window, use the mouse to drag the pods from the Analyzer 2 column to the Analyzer 1 column.



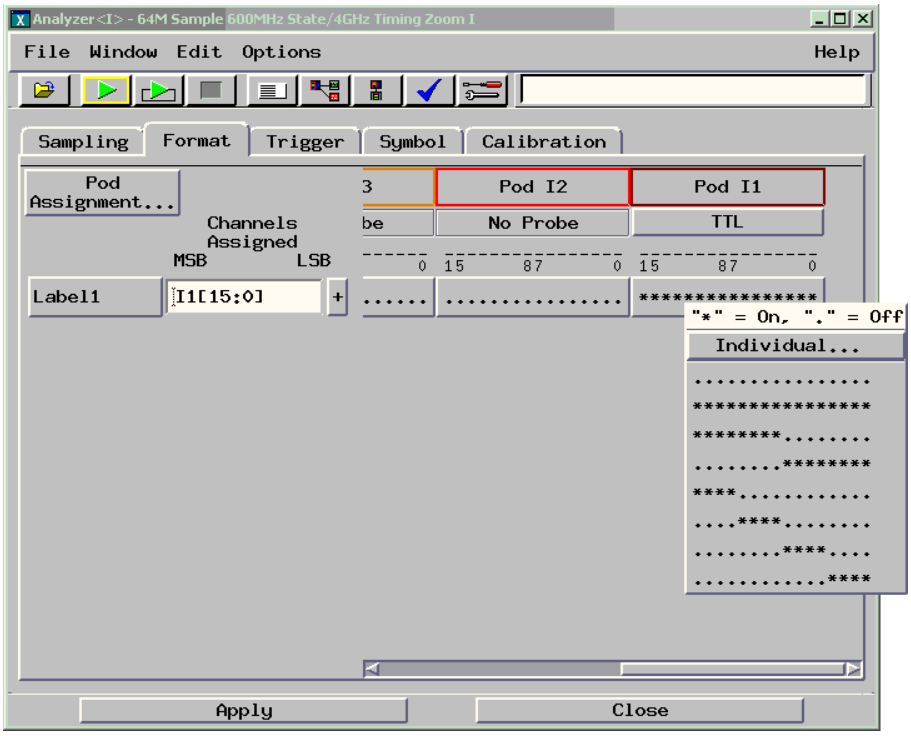
d Select Close to close the Pod Assignment window.

e Under the Format tab, use the scroll bar to scroll to the fields for Pod being tested (Pod 1).

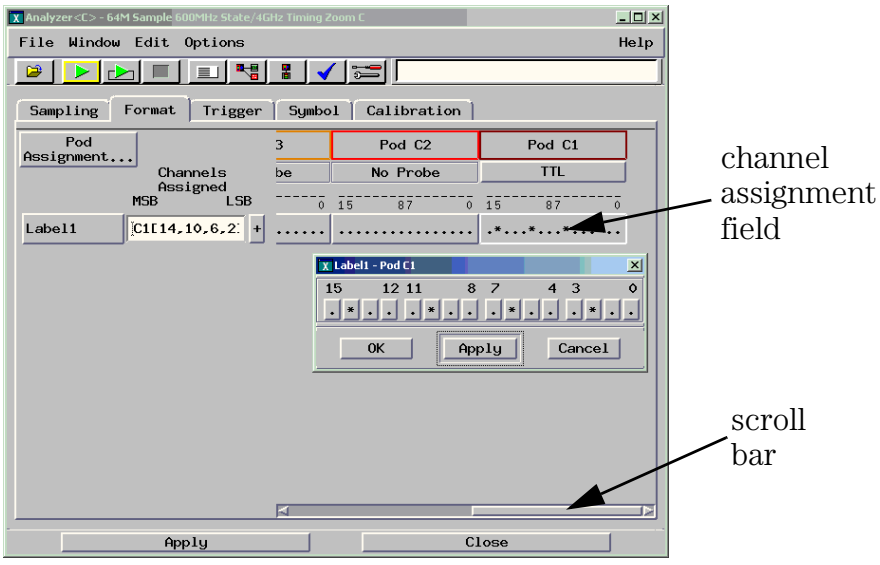
f Select the field showing the channel assignment for the pod being

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tested, then select Individual in the pop-up menu.



g Using the mouse, un-assign all data channels on all pods. Now assign channels 2, 6, 10, and 14 for the pod being tested. An asterisk (*) means that a channel is assigned.

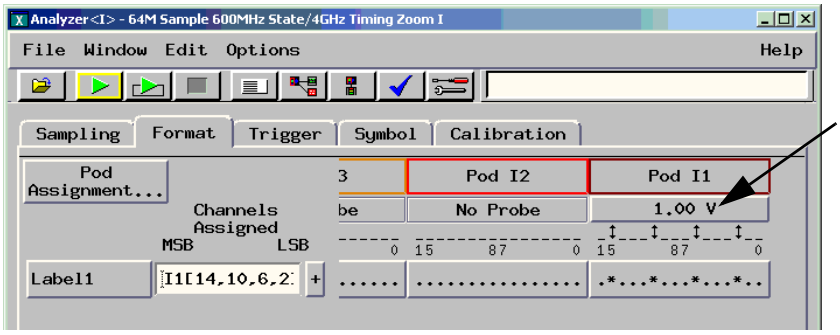


h Select OK to close the channel assignment window.

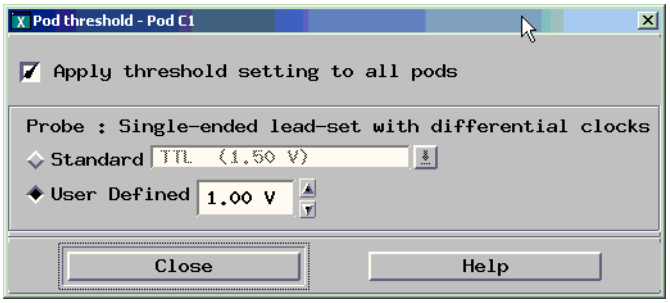
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4 Configure the clock and data thresholds.

a Select the threshold field for the pod that you are going to test. The Pod threshold window will appear. You must have the E5382A Flying Lead Probe attached to the pod you will be testing so that the pod threshold dialog will appear when you click on the pod threshold field.



b In the Pod threshold window, select User Defined and set the threshold value to 1 volt. The “Apply threshold settings to all pods” check box doesn’t matter.

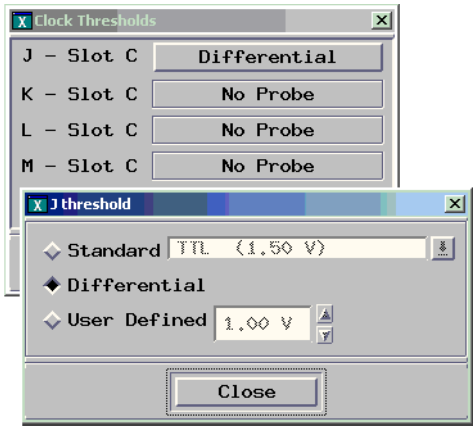


c Select Close to close the Pod threshold window.

d Under the Format tab, use the scroll bar at the bottom of the window to scroll to the left and select the “Clock thresh...” button. In the Clock Thresholds window, select the J clock threshold field, then in the J

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threshold window select Differential.



e Select Close to close the J threshold window. Select Close to close the Clock Thresholds window.

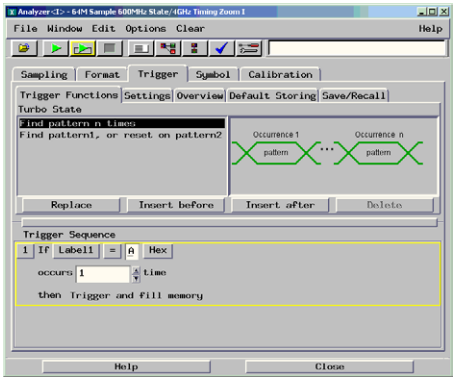
5 Configure the Trigger settings.

a In the logic analyzer Setup and Trigger window, under the Trigger tab, select the Trigger Functions subtab.

b Click on “Find pattern n times.”

c Select Replace.

d Enter “a” in the “Label 1 =” field as shown below.



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Adjust sampling positions using Eye Finder

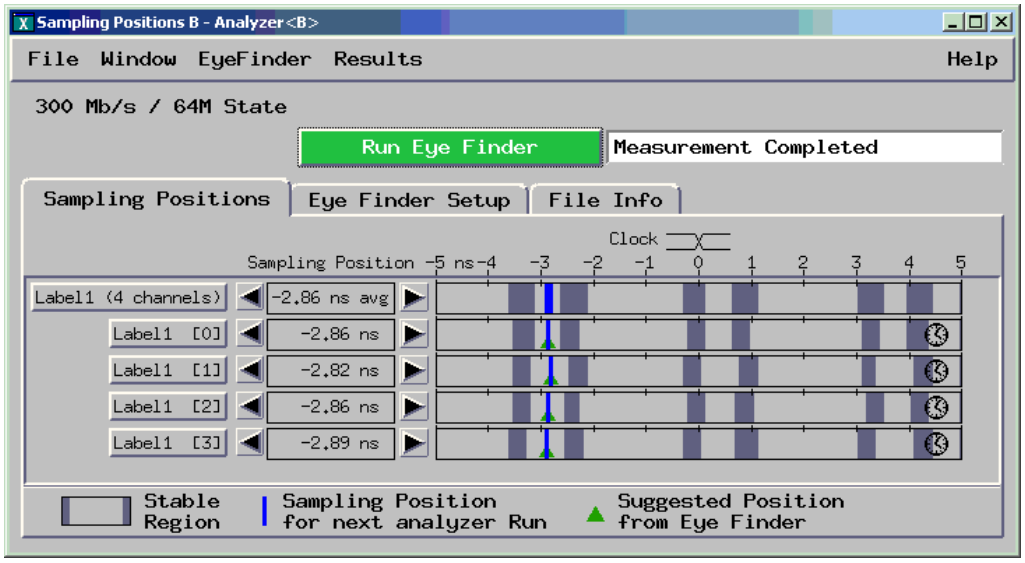
1. In the Setup and Trigger window, select the Sampling tab, then select the "Sampling Positions..." button. The Eye Finder window will appear.
2. From the menu bar in the Eye Finder window, select Results.
3. Select "Remove All Eye Finder Data" if this selection is available (if it is not ghosted).
4. Select "Label1 (4 channels)", then select Expand.

Align the blue bars vertically

5. If the blue bars in the Eye Finder display are not vertically aligned:
   a. In the "Label1 (4 channels) row, grab the right-most blue bar with the mouse pointer and move it all the way to the left. Release the mouse button. This will vertically align all of the blue bars.
6. Select the Sampling Positions tab in the Eye Finder window.
7. Using the mouse pointer, grab the blue bar for "Label 1 (4 channels)" and move it to the recommended starting position of -2.8 ns. All of the blue bars will follow.
8. Select Run Eye Finder (the large green bar).
9. Ensure that an eye appears for each bit near the recommended starting position. Depending on your test setup, the eye position may vary. Any skew between channel 1 and channel 2 of your pulse generator will cause the eye position to shift to the left or right in the Eye Finder display. A shift of up to 0.5 ns should be considered normal. The important point is that your Eye Finder display should look similar to the picture below (although it may be shifted left or right), and Eye Finder must be able to

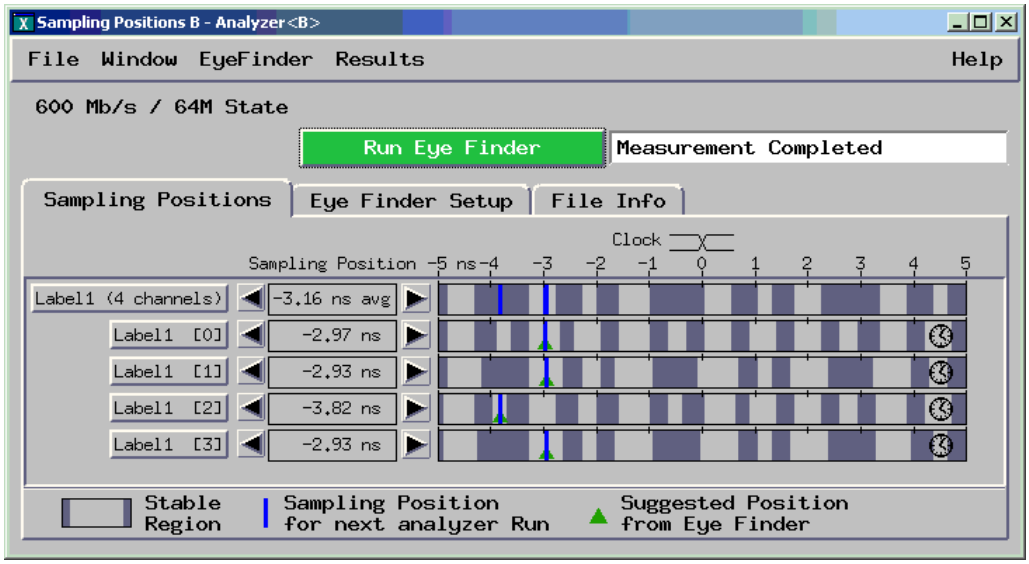
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place the blue bars in the narrow eye.



To re-align a stray channel

If the blue bar for a particular bit does not appear in its eye near the recommended starting position, then do the following steps to realign the sampling position of the stray channel. In the following example, the sampling position of one channel (Label1 [2]) must be realigned with the sampling position of the other channels. (The following example shows the analyzer in 600 Mb/s mode.)

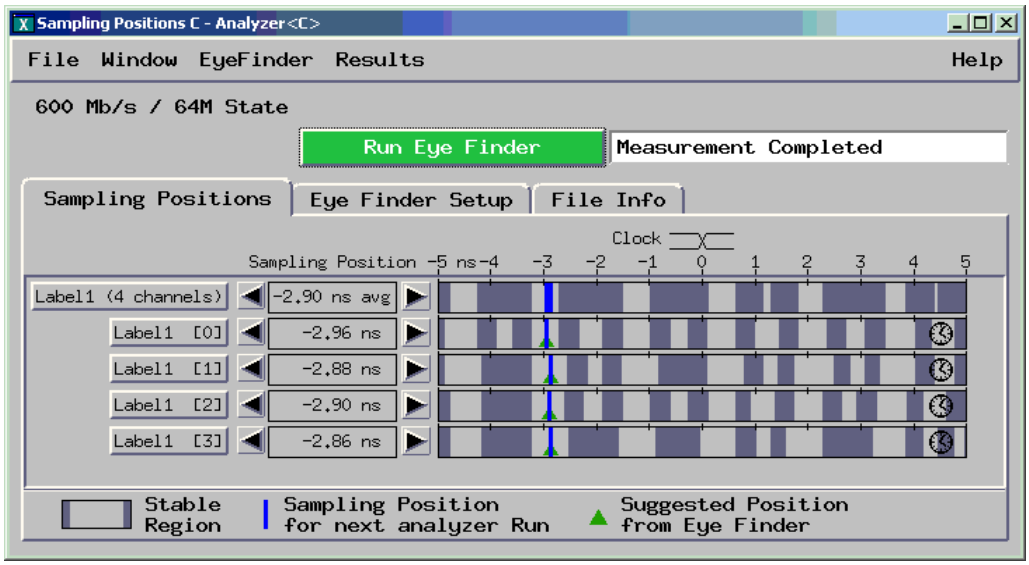


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1 Using the mouse, drag the sample position (blue line) of a stray channel (channel Label1 [2] in the above example) so that it is in the same eye as the other channels. The Suggested Position from Eye Finder (green triangle) will also move to the new eye.

2 Repeat the above step for all remaining stray channels.

3 Select Run Eye Finder. Eye Finder will recalculate the new sample positions based on the sample position changes. The following example shows all sampling positions aligned and in the correct eye.



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Test Pod 1 in 300 Mb/s Mode

The steps that follow include pass/fail criteria.

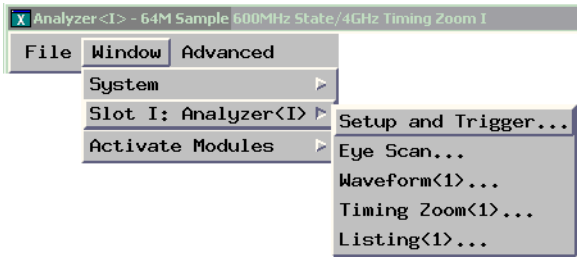
Determine PASS/FAIL (1 of 2 tests)

1 PASS/FAIL: If an eye exists near -2.8 ns for every bit, and Eye Finder places a blue bar in the narrow eye for each bit, then the logic analyzer passes this portion of the test.

2 If an eye does not exist near -2.8 ns for every bit or Eye Finder can not place the blue bar in the narrow eye, then the logic analyzer fails the test. Record the failure in the appropriate place on the Performance Test Record.

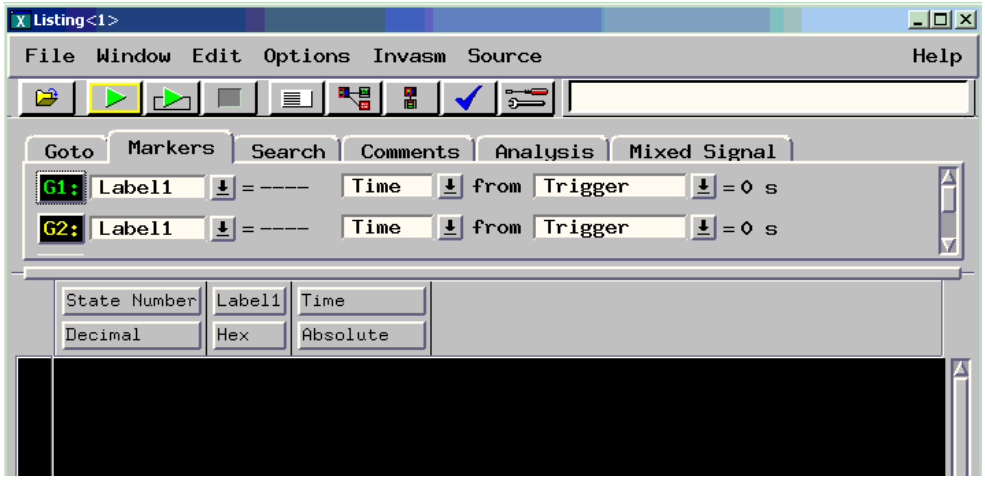
Open and configure the Listing window.

a In the Setup and Trigger window, select Window, then select Slot n: Analyzer<n> (where n is the slot the module under test is installed). At the pop-up menu, select Listing. The Listing window will appear.



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b In the Listing window, select the Markers tab.



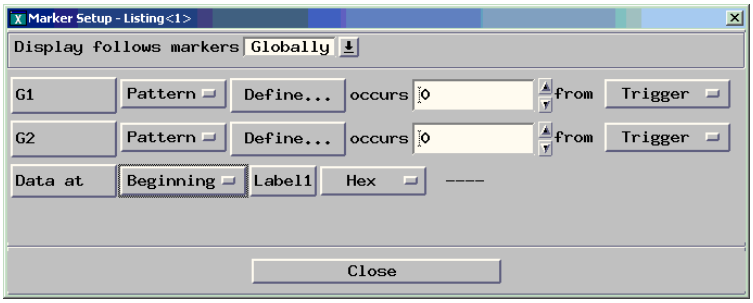
c Select the G1: field and the Markers Setup window will appear.

d Select the field immediately to the right of G1, and select Pattern.

e Select the field immediately to the right of G2, and select Pattern.

f Right-click on the Interval field (which is below G1 and G2) and select Delete.

g Select the field immediately to the right of “Data at” and select Beginning.



NOTE: Leave the marker Setup window open. You will be entering numeric values in the "occurs" field after acquiring the first run of test data.

1 Configure the Markers.

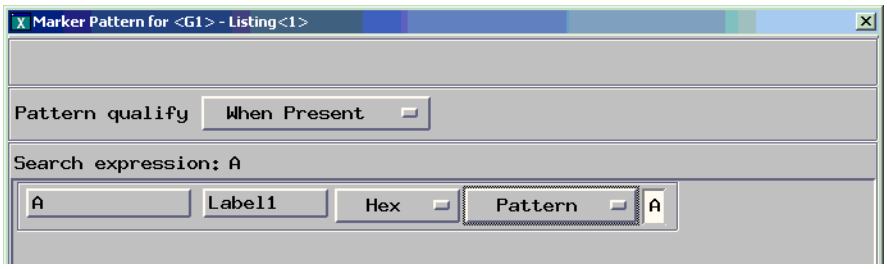
a In the logic analyzer Listing window, select the Run icon. This will load the logic analyzer memory with data so the markers can be configured.

NOTE: An error message will appear because the marker patterns are not yet specified.

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b Click OK to close the error message window.

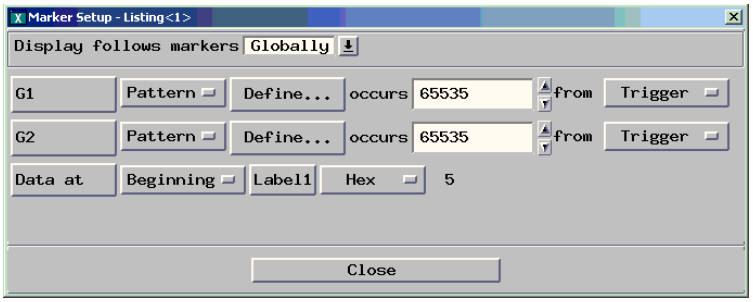
c In the Marker Setup window, select the G1 Define... field. The G1 Marker Pattern window will appear. In the pattern field, enter "a", then select Close.



d In the Marker Setup window, select the G2 Define... field. The G2 Marker Pattern window will appear. In the pattern field, enter "5", then select Close.

e In the Marker Setup window, select the 'occurs' value field that corresponds to marker G1. Enter 65535.

f In the Marker Setup window, select the 'occurs' value field that corresponds to marker G2. Enter 65535, then press Enter.



g Select Close.

2 Select the Run Repetitive icon in the Listing window.

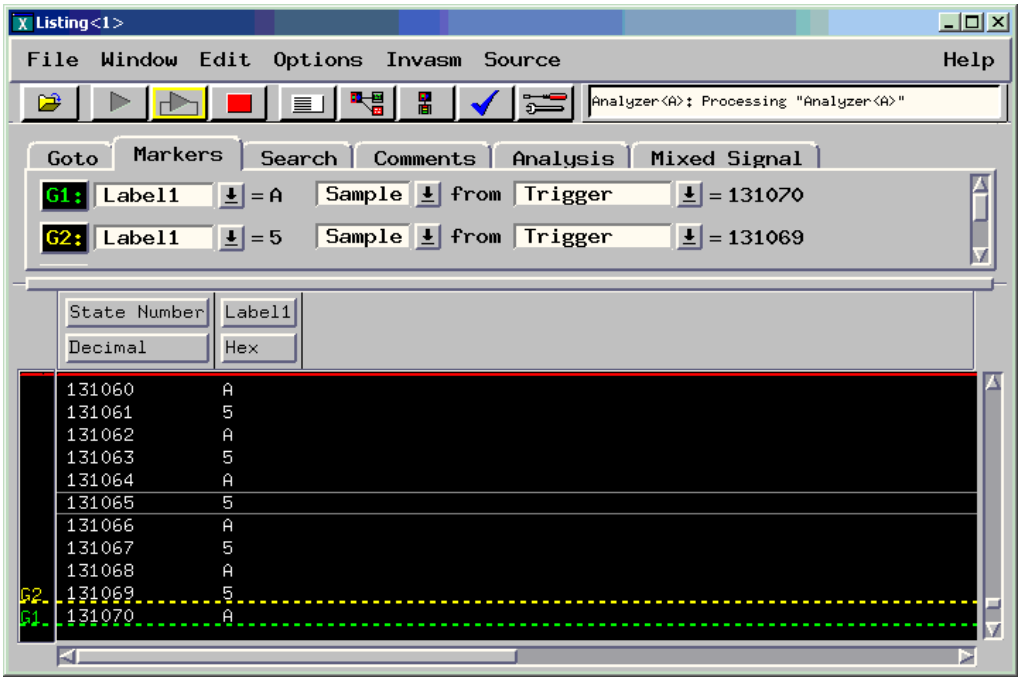
Determine PASS/FAIL (2 of 2 tests)

Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error window will appear. The window will be named 'Error - Listing', and it will say “Pattern NOT found for marker...”.

1 Let the logic analyzer run repetitive for about 1 minute. If no error

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message is displayed the test passes.



If the red error window "Error- Listing <1> Pattern NOT found..." appears during the minute or so that it runs repetitively, then the logic analyzer fails the test. Record the failure in the appropriate place on the Performance Test Record.



NOTE: Be sure that the black ground clip is making good contact with the ground pin on the test connector.

2 After approximately 1 minute click the red stop button in the Listing window.

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NOTE:

As a point of curiosity, you may want to determine the absolute minimum pulse width and/or absolute maximum frequency at which data can be acquired. The "Performance Test Record" on page 60 does not include places for recording these values because the Performance Verification procedure only verifies that the logic analyzer meets specifications. Determination of additional parameters is not required, but may be performed at the discretion of the calibration laboratory.

On some pulse generators, the signal outputs may become unstable for a short period of time when the signal parameters are adjusted. Adjusting the pulse generator while the logic analyzer is running can cause a false failure.

If the Pattern NOT found error message appears while making an adjustment to the pulse generator select OK to close the window. If the message appears again after you have stopped adjusting the pulse generator and allowed a short settling time for the pulse generator, then the logic analyzer fails the test.

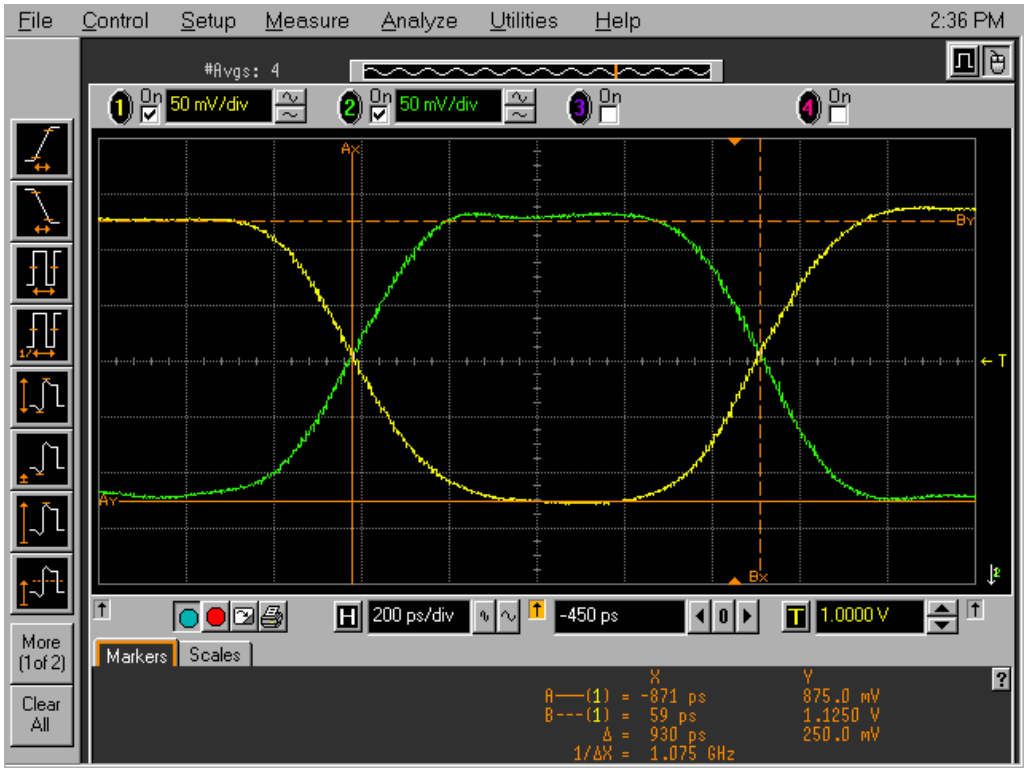
Test the complement of the bits (300 Mb/s mode)

Now test the logic analyzer using complement data.

1. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.
2. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to -450 ps (or as required) to center the measured pulse on the oscilloscope display.
3. Verify the DC offset and adjust it if necessary. See page 32.
4. Deskew the oscilloscope if necessary. See page 33.
5. Adjust the oscilloscope's measurement markers to measure the pulse width. Set the markers so that Δ=930 ps (this assumes you are using the 8133A pulse generator and the Infiniium oscilloscope). Adjust the pulse generator so that the pulse width is 930 ps as measured by the markers.

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See page 35 for details.



6 Adjust the sampling positions (run Eye Finder). See page 68.

7 Determine pass or fail (1 of 2 tests). See page 71.

8 Ensure that the Listing window is set up. See page 71.

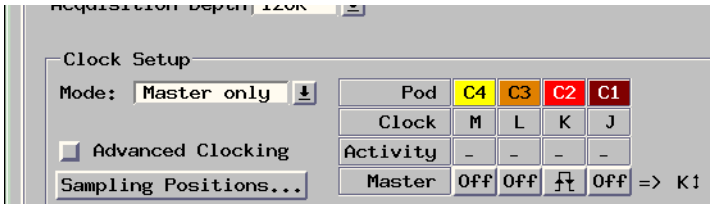
9 Select the Run Repetitive icon in the Listing window.

10 Determine pass or fail (2 of 2 tests). See page 73.

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Test Pod 2 in 300 Mb/s Mode

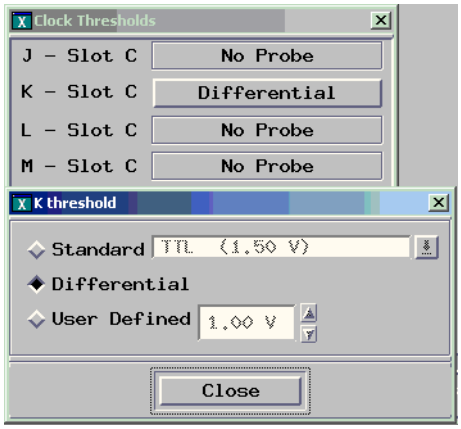
1. Disconnect the E5382A Flying Lead Probe Set from Pod 1 and connect it to Pod 2 of the logic analyzer. Do not remove the flying leads that are connected to CLK, $\overline{\text{CLK}}$, and the data channels.
2. On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.
3. Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.
4. Verify the DC offset and adjust it if necessary. See page 32.
5. Deskew the oscilloscope if necessary. See page 33.
6. Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 35.
7. In the logic analyzer's Setup and Trigger window, Format tab, scroll to the right and unassign all Pod 1 bits. A Warning window will appear stating that the trigger function has become invalid. Select OK to close the Warning window.
8. Assign bits 2, 6, 10, and 14 of Pod 2.
9. Set the Pod 2 threshold to 1 volt (just as you did for Pod 1 on page 66).
10. In the "Setup and Trigger..." window, select the Sampling tab. In the Clock Setup area, set the J clock to "Off" and set the K clock to "Both Edges".



11. Under the Format tab, use the scroll bar at the bottom of the window to scroll to the left and select the "Clock thresh..." button. In the Clock Thresholds window, select the K clock threshold field, then in the K

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threshold window select Differential.



a Select Close to close the K threshold window. Select Close to close the Clock Thresholds window.

12 Re-establish the trigger function:

a In the logic analyzer's Setup and Trigger window, select the Trigger tab, and the Trigger Functions subtab.

b Select "Find pattern n times" and select the "Replace" button.

c Enter "A" in the "Label 1 = " field.

13 Adjust the sampling positions using Eye Finder. Be sure to expand "Label1 (4 channels)" and use the recommended starting position noted on page 68. Realign any stray channels if necessary. See page 69.

14 Determine pass or fail (1 of 2 tests). See page 71.

15 Ensure that the Listing window is set up. See page 71.

16 Select the Run Repetitive icon in the Listing window.

17 Determine pass or fail (2 of 2 tests). See page 73.

Test the complement of the bits (Pod 2, 300 Mb/s mode)

1 Test the complement of the bits. See page 75.

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Test Pods 3 and 4 in 300 Mb/s Mode

1 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate. Test using the L clock for Pod 3 and the M clock for Pod 4. Upon completion, the logic analyzer is completely tested in the 300 Mb/s mode.

Test Pod 1 in 600 Mb/s Mode

The J clock will be used for testing all pods in the 600 Mb/s mode. Therefore two E5382A Flying Lead Probe sets will be required when testing pods 2, 3, and 4.

1 Disconnect the E5382A Flying Lead Probe from Pod 4 of the logic analyzer and connect it to Pod 1 of the logic analyzer.

2 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

3 Note that the signal on the oscilloscope has moved. Change the oscilloscope's horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.

4 Set the frequency of the pulse generator. The logic analyzer will be tested using a double-edge clock. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 300 MHz plus the frequency uncertainty of the pulse generator, plus a test margin of 1%.

   For example, if you are using an 8133A pulse generator, the frequency accuracy is ±1% of setting. Use a test margin of 1%. Set the frequency to 300 MHz plus 2% (306 MHz).

5 Verify the DC offset and adjust it if necessary. See page 32.

6 Verify the oscilloscope Deskew and adjust if necessary. See page 33.

7 Adjust the measured pulse width from the pulse generator to 1 ns (minus the test margin) as described on page 35.

8 In the logic analyzer "Setup and Trigger..." window, select the Sampling

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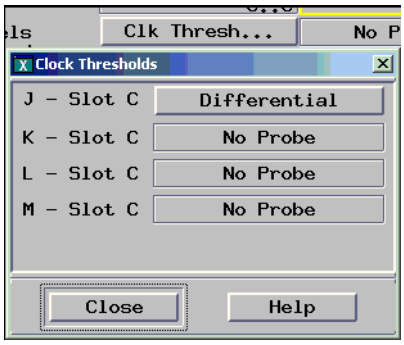
tab. In the “State Mode Controls” section, select the “600 Mb/s / xxM State” mode. (“xxM” indicates the module’s memory depth.) The mode will change to 600 Mb/s and the clock setup will change to J clock, Rising Edge. Do not change it to “Both Edges” yet.

9 In the logic analyzer’s Setup and Trigger window, Format tab, unassign all pod 4 bits.

10 Assign bits 2, 6, 10, and 14 of Pod 1.

11 Ensure that the Pod 1 threshold is set to 1 volt. See page 66.

12 Use the scroll bar at the bottom of the window to scroll to the left and select the “Clock thresh...” button. In the Clock Thresholds window, ensure that the J clock threshold is set to Differential.



a Select Close to close the Clock Thresholds window.

13 Re-establish the trigger function:

a In the logic analyzer’s Setup and Trigger window, select the Trigger tab, and the Trigger Functions subtab.

b Select “Find pattern n times” and select the “Replace” button.

c Enter “A” in the “Label 1 = “ field.

Determine and set Eye Finder Position (600 Mb/s mode)

14 In the Eye Finder (Sampling Positions) window, expand “Label1 (4 channels)”.

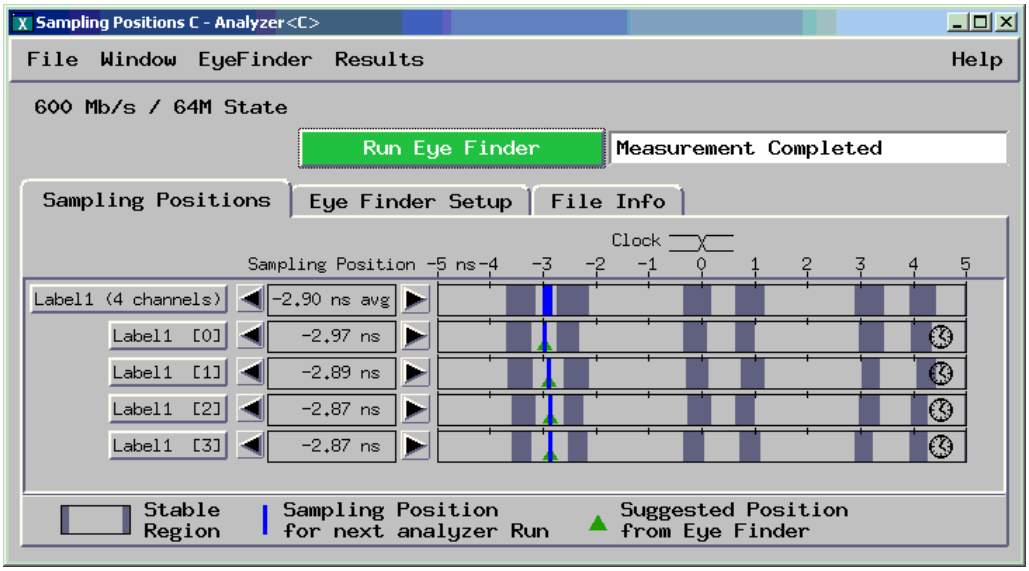
15 If the blue bars are not vertically aligned, align them. See page 68.

16 Grab the blue bar for “Label1 (4 Channels)” and move it to approximately -2.9 ns. All blue bars will follow.

17 Run Eye Finder and note the average sampling position chosen by Eye Finder:_____ns. In the following example, the average sampling position

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is -2.9 ns. Note that in this step, you place the blue bars in the narrow window (not the wide window) that appears to the left of zero in the Eye Finder display. Then run Eye Finder. The position may be different based on your test setup. Bring stray channels into alignment if necessary. See page 69.



18 In the “Setup and Trigger...” window, Sampling tab, Clock Setup area, set the J clock mode to “Both Edges.”

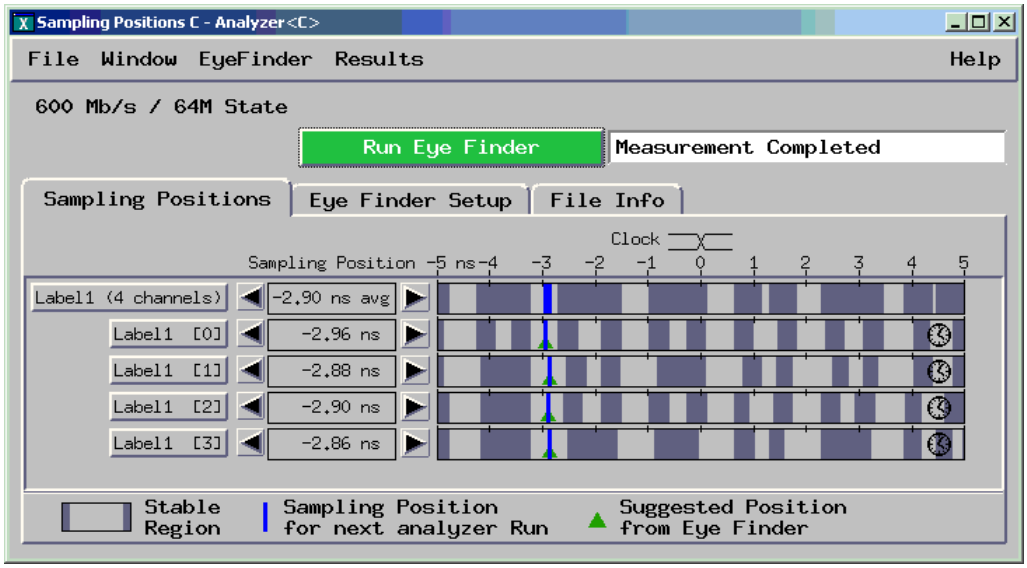
19 In the Eye Finder window, align the blue bars vertically. See page 44.

20 Grab the blue bar for “Label1 (4 Channels)” and move it to the recommended starting position you noted in the prior step.

21 Run Eye Finder again. Some eyes may close, but the eyes in the sampling

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position you chose on page 80 should remain open.



22 Perform the procedure “Determine PASS/FAIL (1 of 2 tests)” on page 46.

23 Select the Run Repetitive icon in the Listing window.

24 Perform the procedure “Determine PASS/FAIL (2 of 2 tests)” on page 48.

Test the complement of the bits (Pod 1, 600 Mb/s mode)

Now test the logic analyzer using complement data.

1 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, select COMP.

2 Note that the signal on the oscilloscope has moved. Change the oscilloscope’s horizontal position to -450 ps (or as required) to center the measured pulse on the oscilloscope display.

3 Verify the DC offset and adjust it if necessary. See page 32.

4 Deskew the oscilloscope if necessary. See page 33.

5 Verify that the pulse width is set to 1 ns. See page 35.

6 Run Eye Finder and align stray channels if necessary.

7 Perform the procedure “Determine PASS/FAIL (1 of 2 tests)” on page 71.

8 Select the Run Repetitive icon in the Listing window.

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9 Perform the procedure “Determine PASS/FAIL (2 of 2 tests)” on page 73

Test Pod 2 in 600 Mb/s Mode

1 Leave the first E5382A Flying Lead Probe Set connected to Pod 1 of the logic analyzer. Remove the Pod 1 flying leads 2, 6, 10, and 14 from the SMA/Flying Lead test connectors. Do not remove the flying leads that are connected to CLK and $\overline{\text{CLK}}$ flying leads.

2 Connect the second E5382A Flying Lead Probe Set to Pod 2.

3 Connect the Pod 2 E5382A Flying Lead Probe Set’s bits 6 and 14 to the SMA/Flying Lead test connector’s pin strip connector at the 8133A pulse generator’s Channel 2 OUTPUT.

4 Connect the Pod 2 E5382A Flying Lead Probe Set’s bits 2 and 10 to the SMA/Flying Lead test connector’s pin strip connector at the 8133A pulse generator’s Channel 2 $\overline{\text{OUTPUT}}$.

5 On the 8133A pulse generator, in the PULSE setup for CHANNEL 2, press the COMP button to return the outputs to normal.

6 Note that the signal on the oscilloscope has moved. Change the oscilloscope’s horizontal position to 525 ps (or as required) to center the measured pulse on the oscilloscope display.

7 Verify the DC offset and adjust it if necessary. See page 32.

8 Deskew the oscilloscope if necessary. See page 33.

9 Readjust the pulse width from the pulse generator as measured on the oscilloscope. See page 35.

10 In the logic analyzer’s Setup and Trigger window, Format tab, unassign all Pod 1 bits.

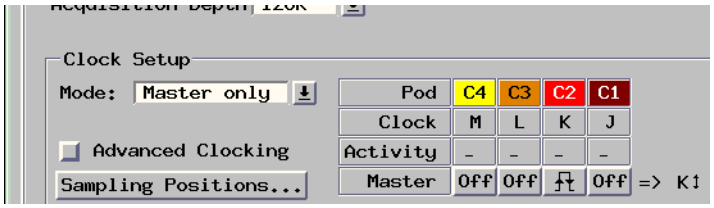
11 Assign bits 2, 6, 10, and 14 of Pod 2.

12 Ensure that the Pod 2 threshold is set to 1 volt (just as you did for Pod 1 on page 66).

13 In the “Setup and Trigger...” window, select the Sampling tab. In the Clock

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Setup area, ensure the J clock is set to “Both Edges”.



14 Under the Format tab, use the scroll bar at the bottom of the window to scroll to the left and select the “Clock thresh...” button. In the Clock Thresholds window, ensure that the J clock threshold is set to Differential. The K clock setting doesn’t matter.



a Select Close to close the threshold window(s).

15 Re-establish the trigger function:

a In the logic analyzer’s Setup and Trigger window, select the Trigger tab, and the Trigger Functions subtab.

b Select “Find pattern n times” and select the “Replace” button.

c Enter “A” in the “Label 1 = “ field.

16 Adjust the sampling positions using Eye Finder. Be sure to expand “Label1 (4 channels)”, align the blue bars vertically, and use the starting position you noted on page 54. Realign any stray channels if necessary. See page 45.

17 Determine pass or fail (1 of 2 tests). See page 71.

18 Ensure that the Listing window is set up. See page 71.

19 Select the Run Repetitive icon in the Listing window.

20 Determine pass or fail (2 of 2 tests). See page 73.

Test the complement of the bits (Pod 2, 600 Mb/s mode)

1 Test the complement of the bits on Pod 2. You can use the procedure “Test the complement of the bits (300 Mb/s mode)” on page 75 as a guideline.

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Test Pods 3 and 4 in 600 Mb/s Mode

1 Perform the normal and complement tests for each additional pod on the logic analyzer, changing the connection to the pod, channel assignments, thresholds, etc. as appropriate. You must use the J clock on Pod 1 for all tests in the 600 Mb/s mode because the other clocks are not available in this mode. Upon completion, the logic analyzer is completely tested.

2 Complete the Performance Test Record on page 86.

Conclude the State Mode Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a In the Logic Analysis System window, select the [X] in the upper right corner to close the window. At the query, select OK.

Ending and restarting the logic analysis session will re-initialize the system.

b Disconnect all cables and adapters from the pulse generator and the oscilloscope.

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Performance Test Record

LOGIC ANALYZER MODEL NO. (circle one): 16753A 16754A 16755A 16756A

Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Year/4000 hours Recommended next testing:

TEST EQUIPMENT USED

Pulse Generator Model No.	Oscilloscope Model No.
Pulse Generator Serial No.	Oscilloscope Serial No.
Pulse Generator Calibration Due Date:	Oscilloscope Calibration Due Date:

MEASUREMENT UNCERTAINTY

Clock Rate	**Pulse Width (Eye Width)**
Pulse Generator Frequency Accuracy: 8133A: 1% of setting	Oscilloscope Horizontal Accuracy: 54845B: ±[((0.007%) (Δt)+(full scale/(2x memory depth))+30 ps] ≅ 30 ps Oscilloscope Display Resolution: 54845B: ±5 ps
Setting: 150 MHz + 2% = 153 MHz 300 MHz + 2% = 306 MHz	Pulse Width setting: 930 ps PWmax(worst case): 930 ps+30 ps+5 ps = 965 ps

TEST RESULTS

Logic Analysis System Self-Tests (Pass/Fail):				
Performance Test: Minimum Master to Master Clock Time and Minimum Pulse Width				
	300 Mb/s mode		**600 Mb/s mode**	
Pulse Generator Settings	Freq: 150 MHz plus test margin Pulse Width: 1 ns less test margin		Freq: 300 MHz plus test margin Pulse Width: 1 ns less test margin	
Test Criteria	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail):				
Pod 2 Results (pass/fail):				
Pod 3 Results (pass/fail):				
Pod 4 Results (pass/fail):				

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4

Calibrating

This chapter gives you instructions for calibrating the logic analyzer.

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Calibration Strategy

The 16753/54/55/56A or 16950A logic analyzer does not require a periodic operational accuracy calibration. To test the module against the module specifications, refer to the “Testing Logic Analyzer Performance” chapter on page 19.

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5

Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies.

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The troubleshooting consists of flowcharts, self-test instructions, and a cable test.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wrist-straps and mats when you perform any service to this instrument or to the modules in it.

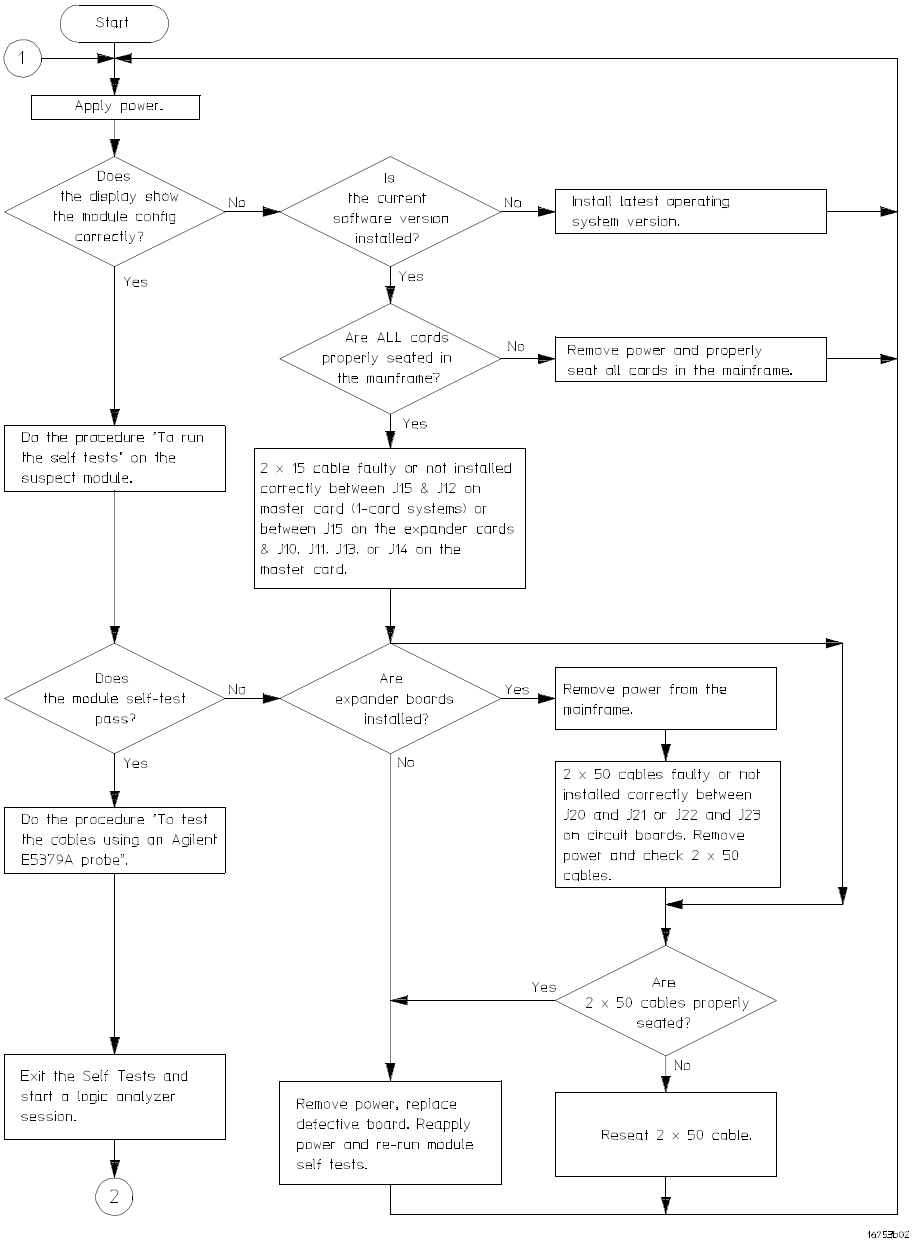
To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

Mainframe Operating System

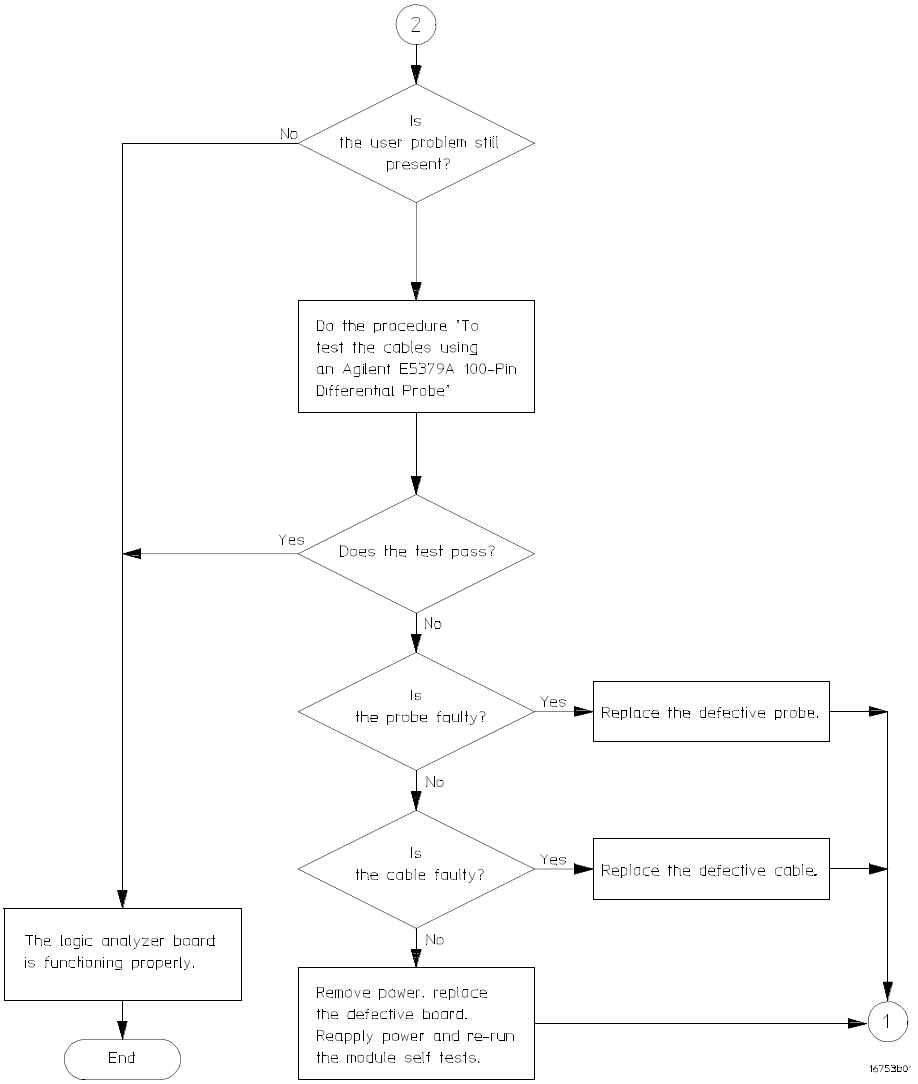
Before troubleshooting a 16753/54/55/56A or 16950A module, ensure that the required version of mainframe operating system is installed on the mainframe. The required operating system software versions are listed in “Mainframe and Operating System” on page 10.

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Troubleshooting Flowchart 1

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Troubleshooting Flowchart 2

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To run the self tests (16900-series mainframe)

1 See “Do a self-test on the 16900-series logic analysis system” on page 38.

To run the self-tests (16700-series mainframe)

Self-tests identify the correct operation of major, functional subsystems of the module. You can run all self-tests without accessing the module. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the module.

To run the self-tests:

1 In the System window, select the System Administration icon.

2 In the System Administration window, select the Admin tab, then select Self-Test.... At the Question window, select Yes. The logic analyzer session will end, the self test software will load, and the Self Test window will appear.

The tests can be run individually, or all the tests can be run by selecting Test All at the bottom of the Self Test window. Note that if Test All is selected, system tests requiring user action will not be run. See the “Agilent Technologies 16700B/16702B Logic Analysis System and 16701B Expansion Frame Service Guide” for more information about the mainframe self-tests. Module self-tests are described on page 94.

3 In the Self Test window under the System tab, select System CPU Board.

4 Run the floppy drive test.

a In the Self Test: System CPU Board window, select Floppy Drive Test.

b Insert a DOS-formatted disk with 300 KB of available space in the mainframe floppy drive.

c In the Test Query window, select OK.

The Test Query window instructs you to insert the disk into the disk drive. The other System CPU Board tests require similar user action to successfully run the test.

5 In the Self Test: System CPU Board window, select Close to close the window.

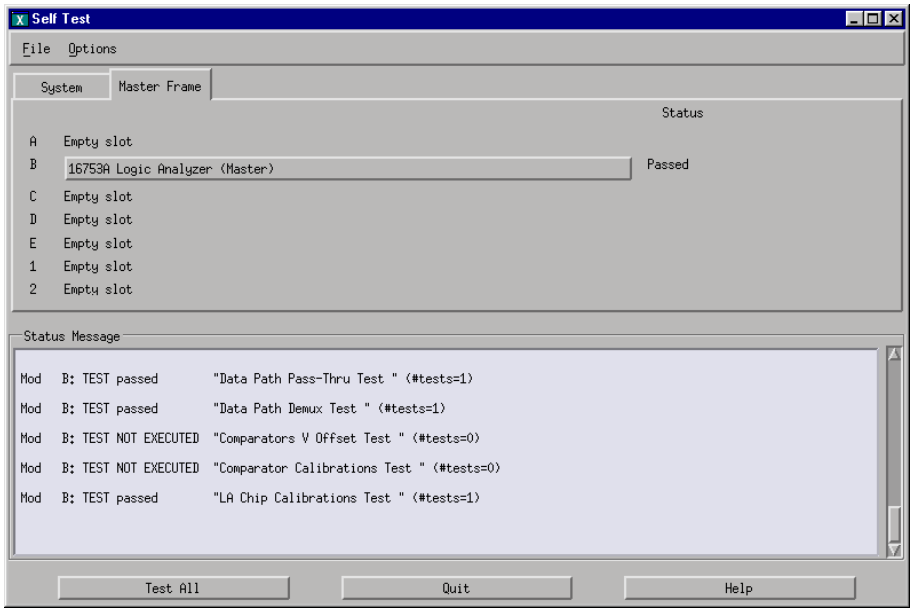
6 In the Self Test window, select 16700 System PCI Board. Select Test All to run all PCI board tests.

7 Refer to the mainframe (e.g. 16700B, 16702B, etc.) service manual for more information on system tests that are not executed.

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8 In the Self Test: 16700 System PCI Board window, select Close to close the window.

9 In the Self Test window, select the Master Frame tab. Select the 16753/54/55/56A module to be tested, then select Test All to run all the module tests. The module test status should indicate PASSED.



Self-Test Descriptions

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

Interface FPGA Register Test. The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. The FPGA must be working before any of the other circuits on the board will work. The backplane FPGA is used to configure the SDRAM controller FPGAs. Also, the FPGA generates the board ID code that is returned to identify the module and slot.

Load Memory FPGA Test. The purpose of this test is to verify that the SDRAM controller FPGAs can be loaded with their respective configuration data files. This test also reads and reports the value of configuration resistors and IC rev numbers.

Memory FPGA Register Test. The purpose of this test is to verify that the registers in the RAM FPGAs can be written and read back.

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EEPROM Test. The purpose of this test is to verify:
The address and data paths to the EEPROM
That each cell in the EEPROM can be programmed high and low
That individual locations can be independently addressed
The EEPROM can be block erased

ADC Test. The purpose of this test is to verify that the three test voltages can be properly read from the Analog to Digital converter. This verifies that the ADC reference voltages are properly connected and that the correct data can be read from the device.

Probe ID Read Test. The purpose of this test is to verify that the Probe ID values can be correctly read and to verify the functionality of the Digital to Analog Converter by testing the two Probe ID DAC outputs at various voltage levels.

Memory Data Bus Test. The purpose of this test is to check out the basic write/read access of the SDRAM from the module backplane bus. This test verifies the operation of the SDRAM data bus as well as some of the operation of the SDRAM control and address busses. This is the first test that accesses the SDRAM acquisition memory using the SDRAM controller FPGAs.

Memory Address Bus Test. The purpose of this test is to completely verify the SDRAM address lines (DDR_xxx_PORT_x_DDR and DDR_xxx_PORT_x_BA).

HW Assisted Memory Cell Test. The purpose of this test is to fully check all of the SDRAM memory locations in all SDRAM memory devices.

Memory Unload Modes Test. The purpose of this test is to check the various modes of unloading data from the SDRAM memories. These modes are setup by writing to registers in the SDRAM controller FPGAs. The SDRAM controller FPGAs sequence the data and perform data decoding based on the mode.

Memory DMA Unload Test. The purpose of this test is to check the various modes of unloading data from the SDRAM memories using DMA backplane transfers. This test is essentially the same as the unloadTest except that DMA backplane transfers are used to read the data from the board.

HW Accelerated Memory Search Test. This test verifies the FPGA based HW Accelerated Search function. It has two modes:
1. A quick test that focuses on the AND functions in the memory controller FPGAs that combine the pattern detected outputs from each FPGA and sends the result to the FPGAs on the master board via the 2x15 clock/cal signal cables (see page 124 for 2x15 cable part number). In doing this, it checks the basic PATTERN search capability of the FPGAs. This is the default mode.
2. An extended test that also checks each search mode of the FPGAs (NOT Pattern, Entering, Exiting, and Transition, in non-interleaved, interleaved tags, and half channel modes). No additional circuitry is tested, except for logic

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internal to the FPGAs.

Chip Registers Read/Write Test. The purpose of this test is to verify that each bit in each register of the Analysis chips can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

Analyzer Chip Memory Bus Test. The purpose of this test is to check the Analysis chip memory busses that go between the Analysis chips and the SDRAM controller FPGAs.

Comparators Programming Test. The purpose of this test is to verify the programming path to each of the comparators.

Comparator/DAC Test. This test uses the pod, bonus, and calibration DACs, the calibration oscillator (implemented in the interface FPGA), the comparators, the connections between the comparators and the Analysis chips, and the activity indicators in the Analysis chips. We verify that we can use the DACs to control the data input to the comparators. We verify that each comparator data channel produces output. We verify that each comparator output is connected to each ASIC data input.

Comparator Delay Test. The comparator delay test verifies the integrity of all the delay line elements for each delay line in the comparators. Each delay line consists of 11 delay elements. When set for maximum delay, all 11 elements are connected in series. If any element is faulty, then data will not propagate through the comparator. If this is the only test failing, then it is almost certainly a bad comparator.

Comparators V Offset Test. This test will not be executed if any probes are attached to any of the probe cables. This test verifies that the V Offset (offset null) taps for each data channel of each comparator can be independently programmed and that each tap has the expected effect on the V Offset adjustment. The tap settings are programmable inside each comparator chip. If this is the only test failing, then it is almost certain that is a bad comparator.

System Clocks (J/K/L/M/Psync) Test. The purpose of this test is to verify that the four clocks (J/K/L/M) are functional between the master board and all Analysis chips, and that the two Psync lines (A/B) are functional between the master board's Analysis chips and all Analysis chips in the module. This test verifies that the four clock lines (J/K/L/M) are driven from the master board and can be received by all Analysis chips, and that the Psync lines can be driven by each master chip on the master board and received by all other Analysis chips in the module.

System Backplane Clock Test. The purpose of this test is to verify the system backplane 100 MHz clock is functional to each Analysis chip and running at the correct frequency. This test also verifies that the PLL in each chip can be

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configured in bypass mode (PLL is not used), then verifies that the PLL can be enabled and used to generate additional clock frequencies.

Inter-chip Resource Bus Test. The purpose of this test is to verify that the Inter-chip Resource lines (ICRs) can be driven as outputs and received as inputs by each chip in the module. The Inter-chip Resource lines (ICRs) are the open drain signals external to the Analysis chips that combine the precombiner outputs from each chip for input to the postcombiners. These are the signals that are connected between same boards in a module using the flex circuit cabling. The signals are open drain outputs to allow the wire ANDing/ORing between the chips. The same pins are used for both output and input of the ICR signals.

Inter-module Flag Bits Test. The purpose of this test is to verify that the four Inter-module Flag Bit Output lines can be driven out from the master chip in the module and received by each chip in the module. In SVY frames eight flag signals available on the backplane. System software dedicates four of these as flag bit outputs from the modules and four as flag bit inputs. The 16753/4/5/6 module drives the four flag outputs from the master chip and can receive the four flag inputs on any chip. Instruments can use these flags to communicate between modules (or within the same module if desired).

Global and Local Arm Lines. The purpose of this test is to verify that the Local Arm signal can be received by each Analysis chip on the master board, and the Global Arm signal can be driven by each chip on the master board and received by all chips in the module (master and slave).

LA Chip Calibrations Test. The purpose of this test is to verify that each analysis chip in the module is able to successfully complete self-calibration.

The PV test works by configuring the module in various configurations and calling the real hardware driver code's calibration routines. The results of the calibration are then checked to see if cal passed or failed.

Comparator Calibrations Test. The purpose of this test is to verify that each of the comparator one-time calibrations can successfully be performed. This verifies that all of the calibration circuitry and components are within the tolerance limits required for proper calibration. This test is executed only if all probes are detached.

Timing Zoom Memory BIST (Built-In Self Test). This test verifies that the timing zoom SRAMs embedded in the analysis chips is functional. The test uses the built-in hardware self test for the SRAMs.

Timing Zoom Memory Addr/Data Test. This test verifies connectivity of components within the analysis chip. It verifies that the address, data, and clock lines of the timing zoom circuitry is correct.

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To exit the test system (16900-series mainframe)

1 Simply close the self-test window. No additional actions are required.all

To exit the test system (16700-series mainframe)

1 Select Close to close any module or system test windows.

2 In the Self Test window, select Quit.

3 In the session manager window, select Start Session to launch a new logic analyzer session.

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To test the cables (16900-series Mainframe)

This test allows you to functionally verify the logic analyzer cable and an Agilent E5379A probe.

Equipment Required

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001
Differential Probe	No Substitute	E5379A

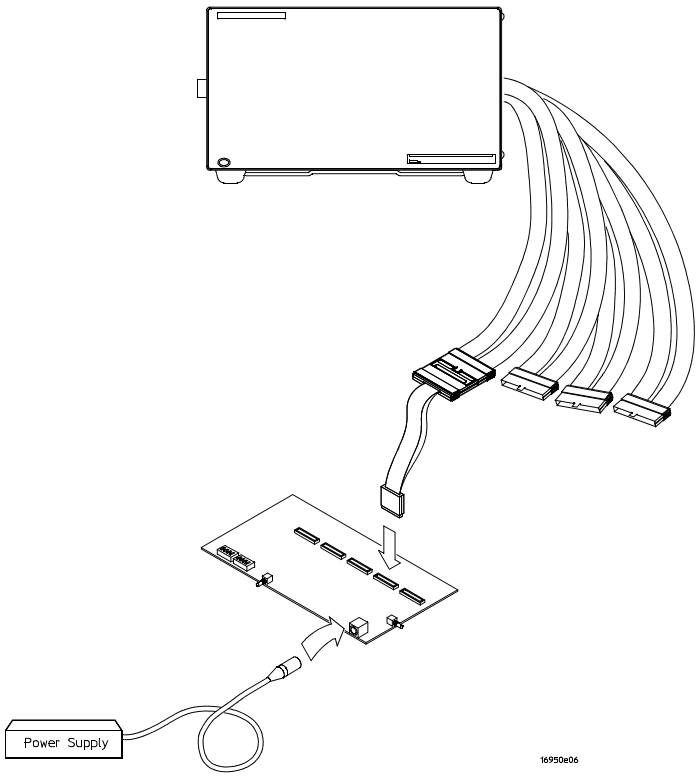
1 Connect the logic analyzer to the stimulus board.

a Connect an Agilent E5379A 100-pin differential probe to the logic analyzer cable (also called “Pod”) to be tested. Start with Pod 1.

b Connect the E5379A probe to connector “Pod 4” on the stimulus board.

c Connect the stimulus board power supply output to the stimulus board power supply connector J82.

d Plug in the stimulus power supply to line power. The green LED DS1 should illuminate showing that the stimulus board is active.



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2 Set up the stimulus board

a Configure the oscillator select switch S1 according to the following settings:

- S1 0 (Off)
- S2 1 (On)
- S3 0 (Off)
- Int

b Configure the data mode switch S4 according to the following settings:

- Even
- Count

c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

3 Exit the logic analysis application (from the main menu, choose File→Exit) and then restart the application. This puts the logic analysis system into its initial state.

4 Disable all analyzers except the one being tested. This simplifies the instructions and makes module initialization faster.

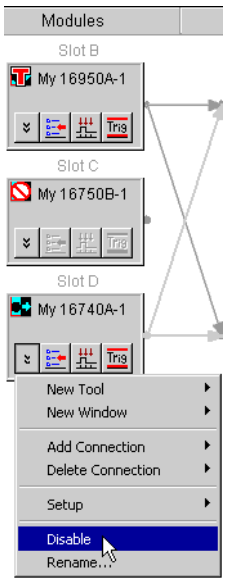
a Select the Overview tab at the bottom of the main window.



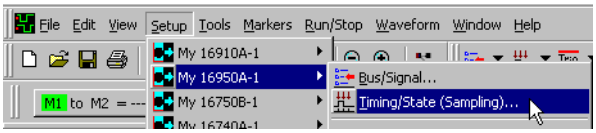
b Click on each unused logic analyzer and select disable. Only the logic

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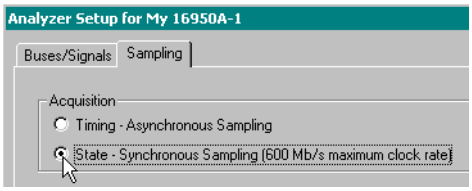
analyzer to be tested should remain enabled.



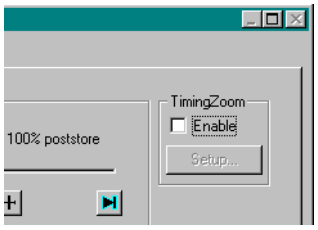
5 From the Logic Analysis System main menu, select **Setup→My 16950A→Timing/State (Sampling).....**



a Select **State Mode**.



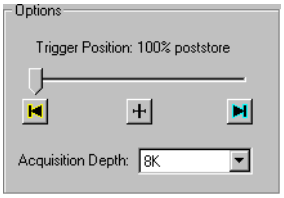
b Clear the Timing Zoom check box to turn Timing Zoom off.



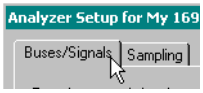
c Set the Trigger Position to **100% Poststore**.

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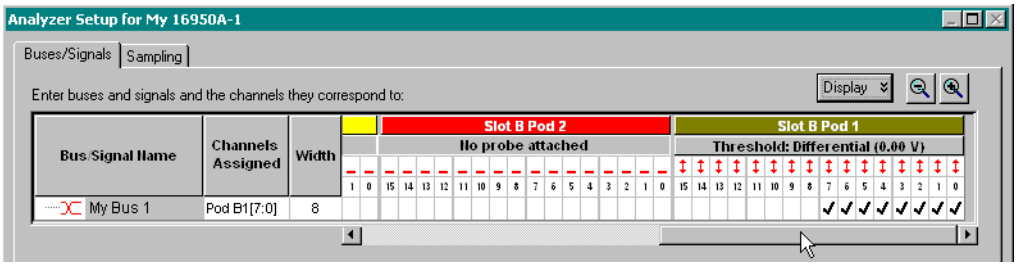
d Set the Acquisition Depth to **8K**.



6 Select the **Buses/Signals** tab.

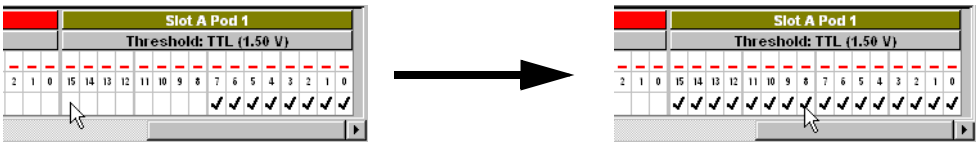


a Scroll if necessary to view the pod you are testing.



b Verify that the pod's threshold button says "**Threshold: Differential (0.00 V)**", as shown above. If it doesn't, ensure the correct probe (E5379A) is attached to the pod. The threshold is set to Differential automatically when the E5379A probe is attached.

c Channels 7 through 0 are already assigned by default. Assign channels 15 through 8 by clicking and dragging from the channel 15 box to the channel 8 box. Your display should look like the picture on the right when you're done.



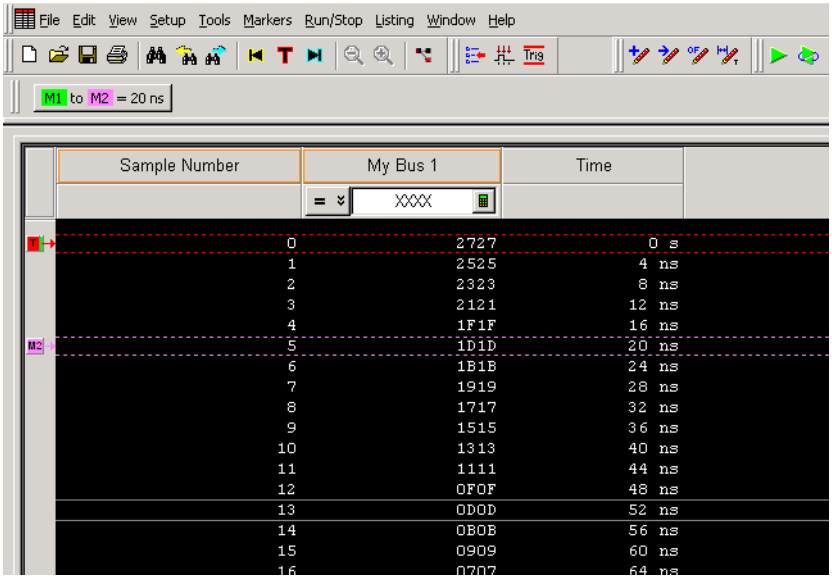
d Select **OK** to close the Analyzer Setup window.

7 Switch to the Listing window by selecting the **Listing** tab at the bottom of the main window.

8 Select the Run icon . The listing should look similar to the figure

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below when you scroll down a bit.



Scroll down at least 256 states to verify the data. My Bus 1 shows two 8-bit binary counters decrementing by 2. If the listing does not look similar to the figure, then there is a possible problem with the cable or probe. Cause for cable test failures include:

- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

If the test data is not correct, then perform the following step to isolate the failure.

9 Verify the failure

a Connect the probe to each of the other three logic analyzer cables, each in turn.

b Repeat step 6 through 8 to reconfigure the Format tab in the Setup and Trigger window. Deactivate the pod just tested. Activate the pod to be tested and assign all channels to “My Bus 1”.

c Select the Run button. The expected test data is the same as in step 8 above.

If the test data is now correct (that is, the error follows the cable) then the cable is suspect.

If the test data is still not correct (that is, the error follows the E5379A probe) the probe is suspect.

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Return to the troubleshooting flowchart.

To test the cables (16700-series Mainframe)

This test allows you to functionally verify the logic analyzer cable and an Agilent E5379A probe.

Equipment Required

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001

1 Connect the logic analyzer to the stimulus board.

a Connect an Agilent E5379A 100-pin differential probe to the logic analyzer cable (also called “Pod”) to be tested.

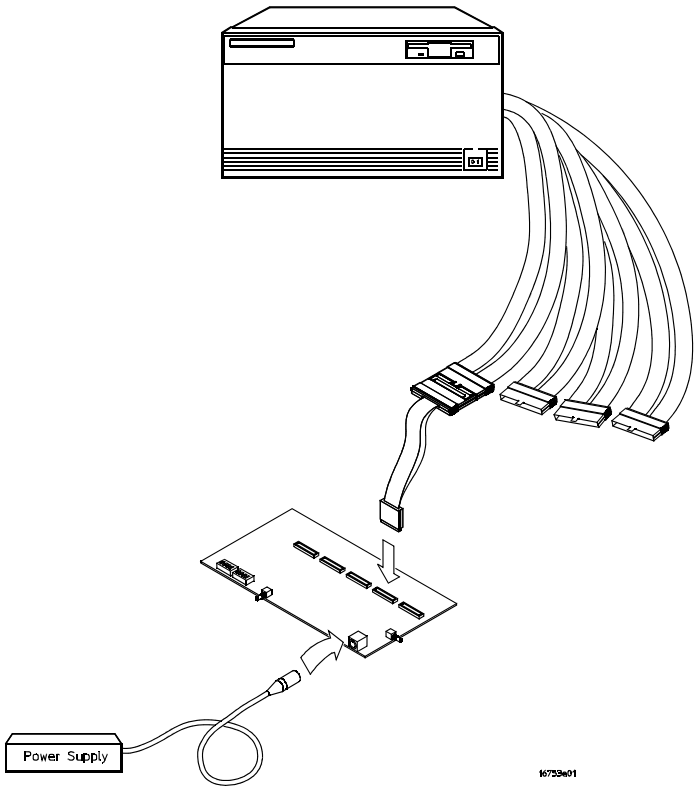
b Connect the probe input to the stimulus board connector Pod 4.

c Connect the stimulus board power supply output to the stimulus board power supply connector J82.

d Plug in the stimulus power supply to line power. The green LED DS1

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should illuminate showing that the stimulus board is active.



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2 Set up the stimulus board

a Configure the oscillator select switch S1 according to the following settings:

- S1 0 (Off)
- S2 1 (On)
- S3 0 (Off)
- Int

b Configure the data mode switch S4 according to the following settings:

- Even
- Count

c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

3 Set up the logic analyzer

a Open the Session Manager window and select “Start Session.”

b In the Logic Analysis System window, select the module icon, then select Listing. A Listing window appears. You will use this window later.

c In the Logic Analysis System window, select the module icon again, then select Setup and Trigger. A Setup and Trigger window appears.

4 Set up the Sampling tab

a In the logic analyzer Setup and Trigger window, ensure that the Sampling tab is selected.

b Under the Sampling tab, select State Mode.

c In the upper right area of the window, select the Timing Zoom... button

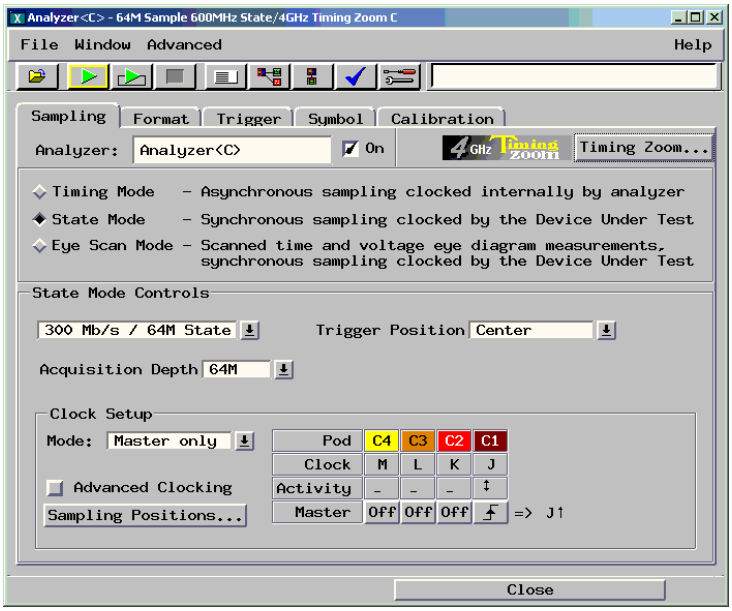
d Switch Timing Zoom off, and close the Timing Zoom window.

e In the Clock Setup area of the Sampling tab, ensure that the Mode is set to Master only.

f In the Clock Setup area of the Sampling tab, ensure that the clock edge

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field for J-clock is set to Rising Edge.

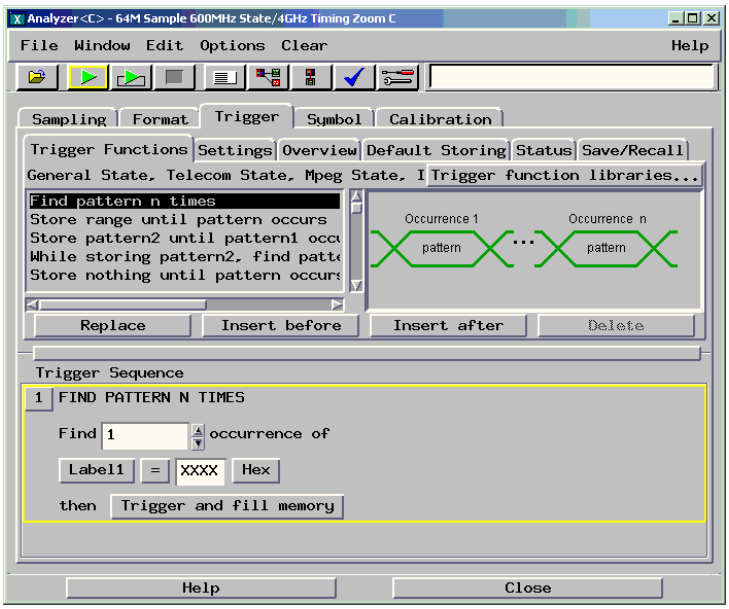


5 Configure the Trigger settings

a In the logic analyzer Setup and Trigger window, select the Trigger tab.

b Ensure that the Trigger Functions subtab is selected.

c On the Setup and Trigger window menu bar (at the top of the window), select Clear, then select Trigger Sequence. Ensure that the Trigger Sequence section of the window now shows FIND PATTERN N TIMES next to the "1".



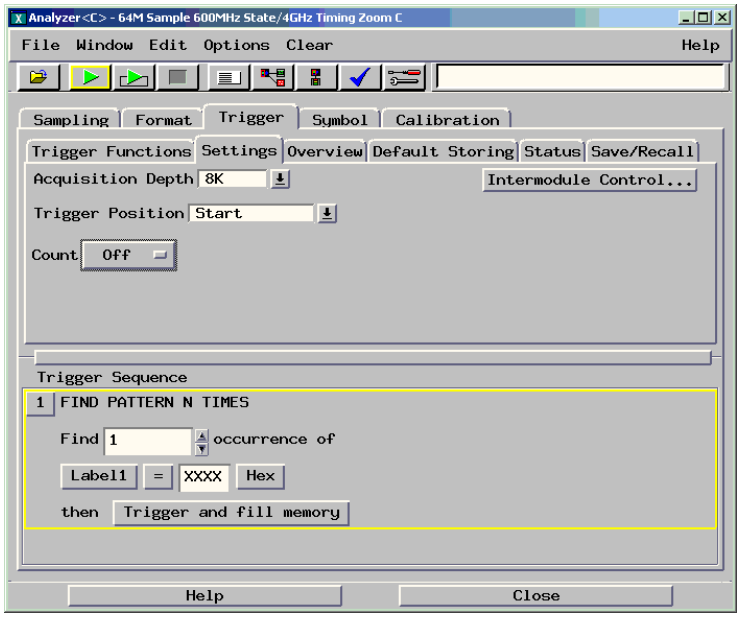
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d Under the Trigger tab, select the Settings subtab.

e Select the Acquisition Depth field, then select 8K.

f Select the Trigger Position field, then select Start.

g Select the Count field, then select Off.

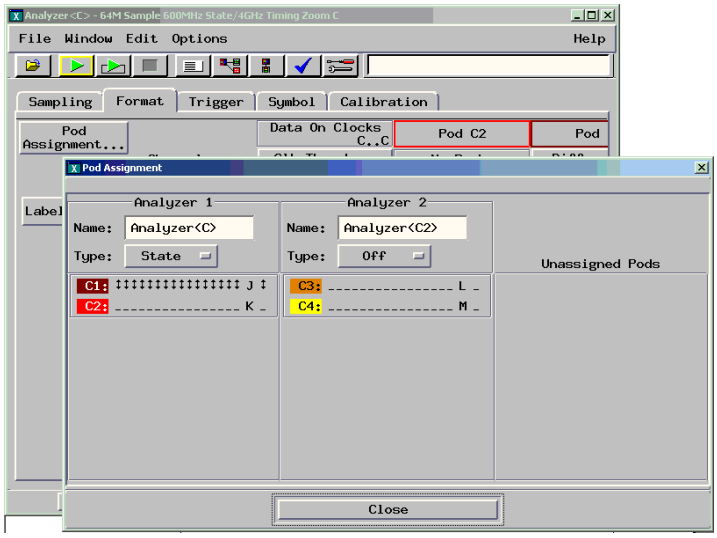


6 Configure the Format tab

a In the logic analyzer Setup and Trigger window, select the Format tab.

b Under the Format tab, select Pod Assignment.

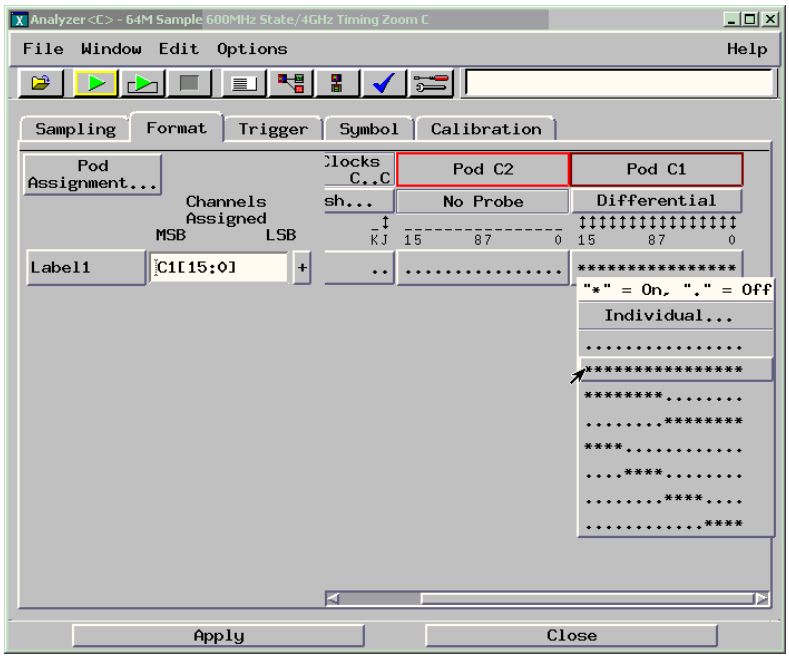
c In the Pod Assignment window, use the mouse to drag the pod under test to the Analyzer 1 column.



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d Select Close to close the pod assignment window.

e Under the Format tab, select the field showing the channel assignment for the pod under test, (you may need to use the scroll bar) then select "**********" to activate all channels.



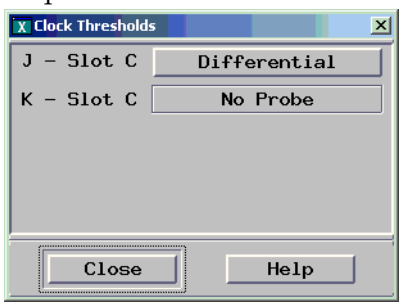
f Select the Apply button at the bottom of the window.

7 Verify the logic analyzer threshold setting

a Under the Format tab, select the CLK Thresh... field (you may need to use the scroll bar). The Clock Thresholds window will appear.

b Ensure that the threshold field associated with J-clock says Differential.

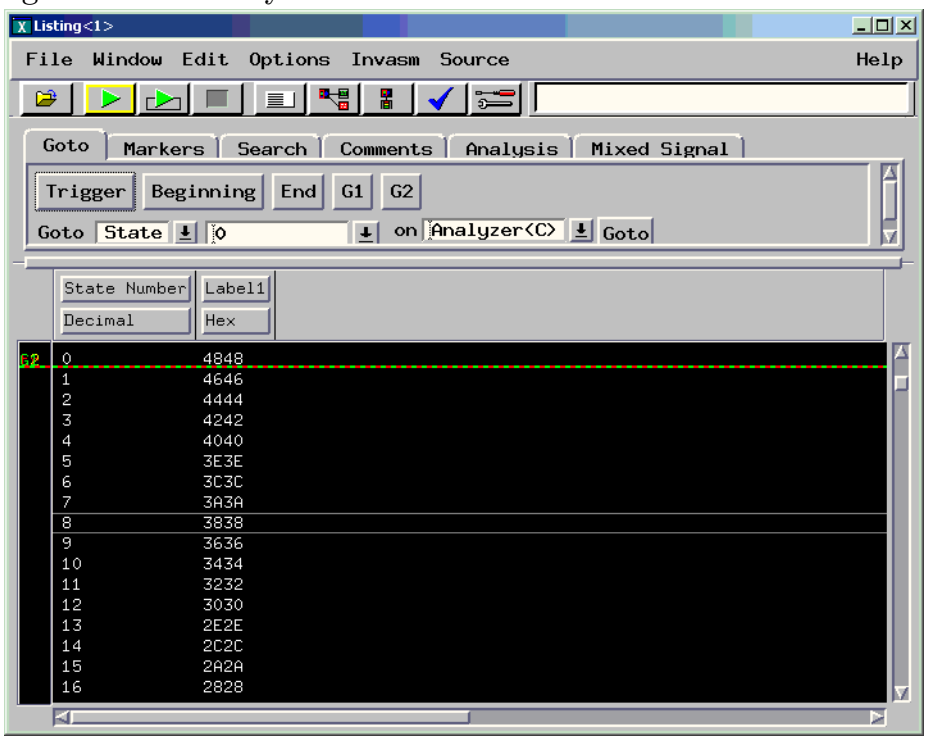
c If it doesn't, ensure the correct probe (E5379A) is attached to the pod. The threshold is set to Differential automatically when the E5379A probe is attached.



d Select Close to close the Clock thresholds window.

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8 In the Listing window, select Run. The listing should look similar to the figure below when you scroll down a bit.



Scroll down at least 256 states to verify the data. Label1 shows two binary counters that decrement by 2. If the listing does not look similar to the figure, then there is a possible problem with the cable or probe. Cause for cable test failures include:

- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

If the test data is not correct, then perform the following step to isolate the failure.

9 Verify the failure

a Reconnect the probe to each of the other three logic analyzer cables, each in turn.

b Repeat step 6 through 8 to reconfigure the Format tab in the Setup and Trigger window. Deactivate the pod just tested. Activate the pod to be tested and assign all channels to Label1.

c On the Listing window, select Run. The expected test data is the same as in step 8 above.

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If the test data is now correct (that is, the error follows the cable) then the cable is suspect.

If the test data is still not correct (that is, the error follows the E5379A probe) the probe is suspect.

Return to the troubleshooting flowchart.

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6

Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module as well as the instructions for returning assemblies.

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CAUTION: Turn off the instrument before installing, removing, or replacing a module in the instrument.

CAUTION: Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

Tools Required

- A T10 TORX screwdriver is required to remove screws connecting the probe cables and screws connecting the back panel.

To remove the module

Instructions for removing or installing the module into the mainframe can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16700B mainframe, go to www.agilent.com and enter **16700B installation guide** in the quick search box. Then scroll down to **Manuals, Guides & Notifications** to find the 16700B-Series Logic Analysis Systems Installation Guide.

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To remove the logic analyzer cable

1 Remove power from the instrument

a In the session manager, select Shutdown.

b At the query, select Power Down.

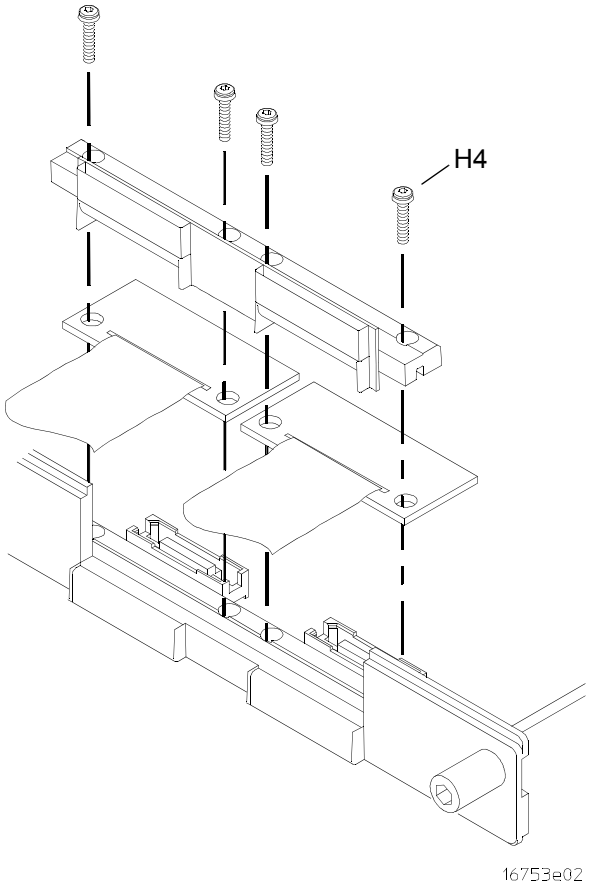
c When the “OK to power down” message appears, turn the instrument off.

d Disconnect the power cord.

2 Remove the logic analyzer cable clamp.

a Remove four screws that secure the logic analyzer cable clamp to the outside rear panel.

b Remove the cable clamp from the rear panel.



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3 Remove the logic analyzer cable.

a Gently lift the logic analyzer cable end connector from the circuit board connector (J1, J2, J3, or J4).

4 If the logic analyzer cable is faulty, replace the cable and follow the next procedure to install the replacement logic analyzer cable.

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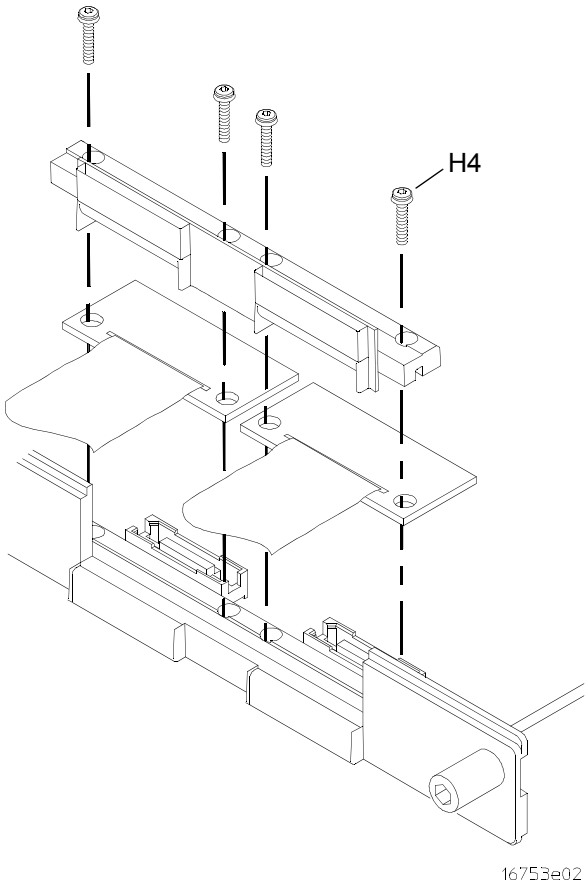
To install the logic analyzer cable

1 Connect the logic analyzer cable to the logic analyzer circuit board.

a Insert the logic analyzer cable to the logic analyzer circuit board.

b Align the logic analyzer cable end connector with the circuit board cable connector (J1, J2, J3, or J4) and gently apply pressure to seat the logic analyzer cable onto the circuit board connector.

c Insert the top and bottom logic analyzer cable clamps into the rear panel.



2 Secure the cable clamp to the rear panel.

a Install the four screws (H5) vertically through the cable clamp into both the cable clamp and the circuit board.

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b Tighten the cable clamp screws (H5) to 5 in/lb.

CAUTION: If you over tighten the screws, the threaded inserts on the rear panel, the threaded inserts on the circuit board, or the cable clamp itself might break. Tighten the screws only enough to hold the cable in place, approximately 5 in/lb.

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To replace the circuit board

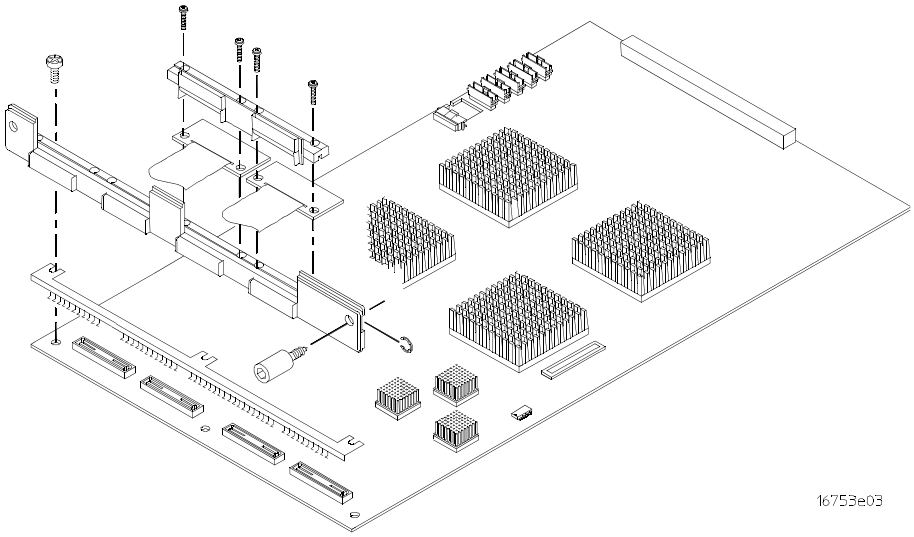
1 Remove the logic analyzer cables using the “To remove the logic analyzer cable” procedure on page 115.

2 Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.

3 Replace the faulty circuit board with a new circuit board. On the faulty board, make sure the 2x15 (30-pin) ribbon cable is connected between J15 and J12.

4 Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.

5 Install the logic analyzer cables using the procedure “To install the logic analyzer cable” on page 117.



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To return assemblies

Before shipping the module to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details. Information on contacting Agilent can be found at http://www.agilent.com.

1 Write the following information on a tag and attach it to the module.

- Name and address of owner
- Model number
- Serial number
- Description of service required or failure indications

2 Remove accessories from the module.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the module.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION: For protection against electrostatic discharge (ESD), package the module in ESD-safe material.

4 Seal the shipping container securely, and mark it FRAGILE.

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7

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your module.

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Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. Addresses and telephone numbers are located in a separate document shipped with the *Agilent Technologies 16900-Series (or 16700-Series) Logic Analysis System Service Manual*.

Exchange assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest

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Agilent Technologies Sales Office for information.

See Also “To return assemblies” on page 120.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator (if applicable)
- Agilent Technologies part number
- Total quantity included with the module (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- H Hardware
- J Connector
- MP Mechanical Part
- W Cable

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Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assemblies			
	16753-69510 16754-69510 16755-69510 16756-69510 16950-69510		Exchange Acquisition Board Assembly
Replacement Assemblies			
A1	16753-66510 16754-66510 16755-66510 16756-66510 16950-66510	1	Acquisition Board Assembly
	16760-60001	0	Stimulus Board Assembly (for cable test; see page 104 or page 99)
H1	16903-68713	2	Replacement thumb screws with sleeve, 2 sets
H1	16900-68713	2	Replacement thumb screws with sleeve, 6 sets
H2	16754-29101	1	Ground Spring
H3	0515-0375	8	M3.0x0.5 16mm T10 (Cable Clamp to Acquisition Board)
H4	0515-0430	3	MSPH M3.0x0.50 6mm T10 (Rear Panel to Acquisition Board)
	01650-94312	1	Label - Probe and Cable (on 90-pin connector)
MP1	16754-44101	1	Rear Panel
MP2	16754-41201	2	Logic Analyzer Cable Clamp
MP3	16753-94301 16754-94301 16755-94301 16756-94301 16950-94301	1	ID Label
W1	16754-61602	1	2x15 Cable
W2	16754-60002	1	2x50 Master/Expander Cable Kit (2 pieces)
W3	16760-61605	4	Logic Analyzer Cable

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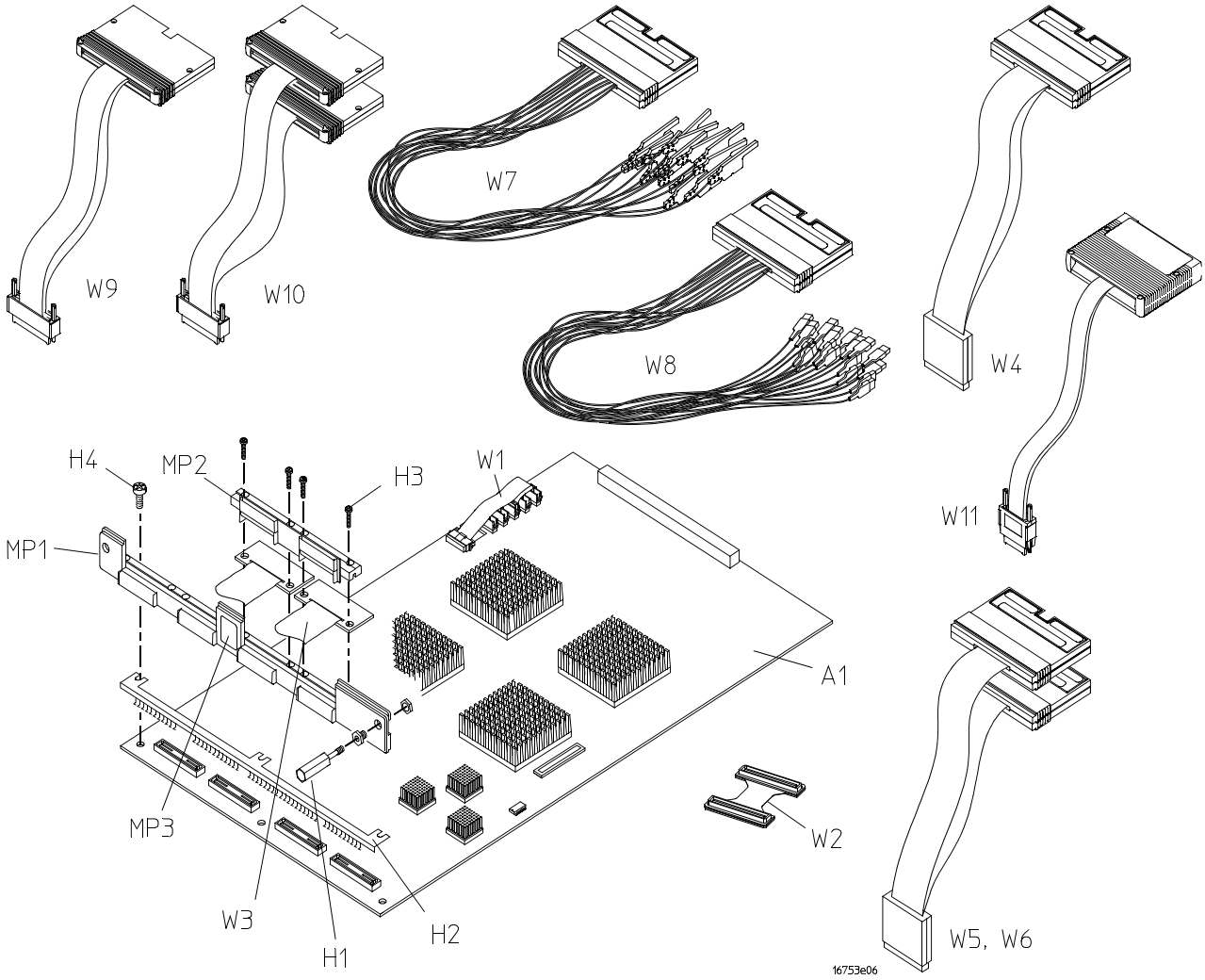
Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
Accessories for Connectivity to the System Under Test			
W4	E5379A		100-Pin Differential Probe (for Samtec connector)
W5	E5378A		100-Pin Single-Ended Probe (for Samtec connector)
W6	E5380A		38-Pin Single-Ended Probe (for MICTOR connector)
W7	E5382A		Single-Ended Flying Lead Probe
W8	E5381A		Differential Flying Lead Probe
W9	E5387A		Differential Soft Touch Connectorless Probe
W10	E5390A		Single-Ended Soft Touch Connectorless Probe
W11	E5398A		Half-Size Soft Touch Connectorless Probe
	1253-3620		Samtec Connector
	16760-02302		Shroud for 0.062” PC Boards
	16760-02303		Shroud for 0.120” PC Boards
	16760-68702		*Shroud/Connector Kit for 0.062” PC Boards
	16760-68703		*Shroud/Connector Kit for 0.120” PC Boards
	1252-7431		MICTOR Connector
	E5346-44703		MICTOR Shroud for 0.170” PC Boards
	E5346-44704		MICTOR Shroud for 0.125” PC Boards
	E5346-68700		*Shroud/Connector Kit for 0.125” PC Boards

*Shroud/Connector kits include connectors (Qty 5) and shrouds (Qty 5) for the indicated system under test circuit board thickness.

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Exploded View



Exploded view of the 16753/54/55/56A or 16950A logic analyzer

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8

Theory of Operation

This chapter presents the theory of operation for the logic analyzer card.

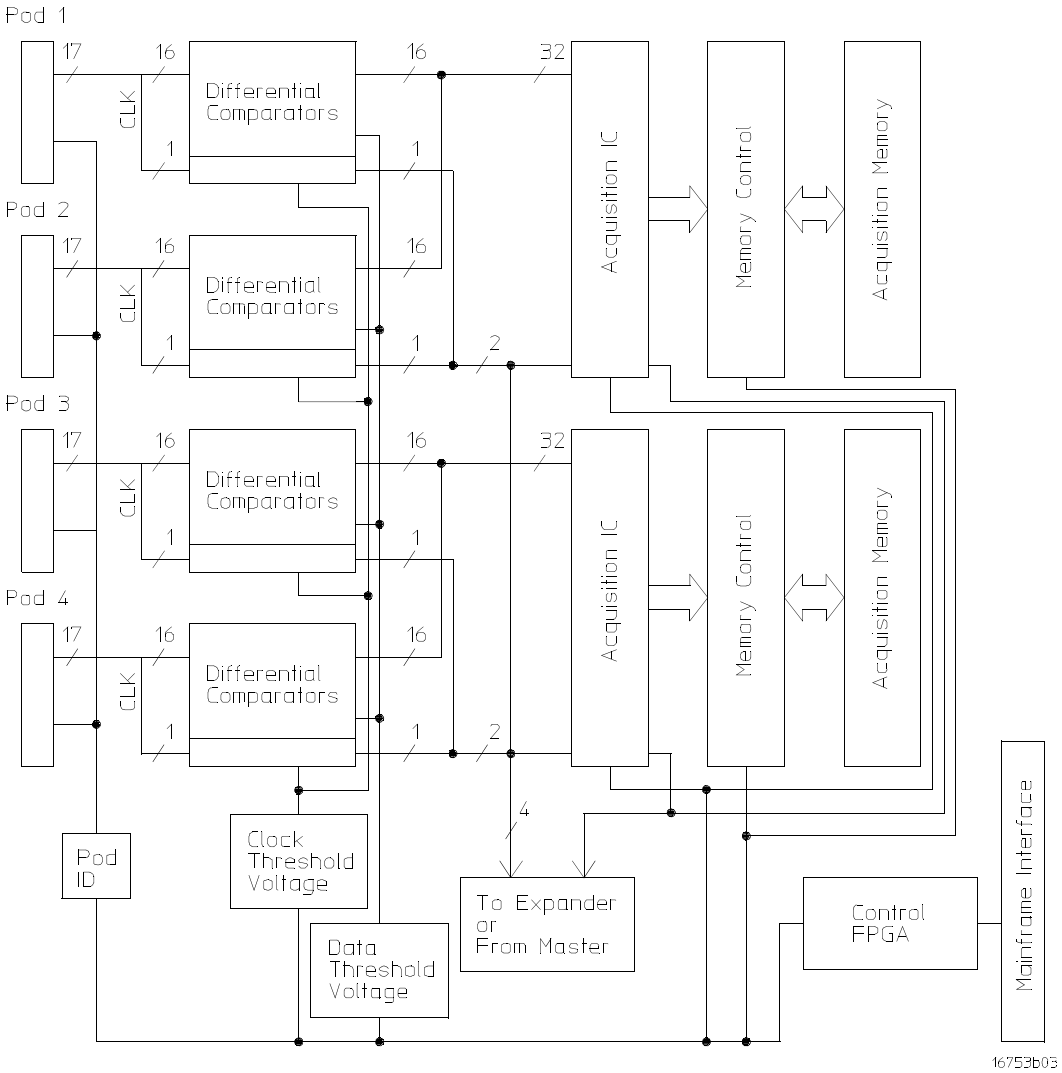
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The information in this chapter is to help you understand how the logic analyzer operates. This information is not intended for component-level repair.

Block-Level Theory

The block diagram of the 16753/54/55/56A or 16950A logic analyzer is shown below.

The 16753/54/55/56A or 16950A logic analyzer



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Probes. The 16753/54/55/56A or 16950A logic analyzer card contains 4 probe pods. Each pod is comprised of two cables and contains 16 differential data channels, a differential clock channel, a user supplied threshold voltage, two serial I2C programming lines for configuring analysis probes, +5 V for powering analysis probes, a probe identification line, and 50 ground signals. Each cable has a 90-pin probe cable connector.

The pods provide +5 Vdc ±5% auxiliary power to each 90-pin probe cable connector. Each connector can deliver up to 300 mA with a maximum of 1.0 A total from the analyzer card. A current limiting circuit protects the +5 V cable power from current overload. The VCC_Enable signal is used to control power to an analysis probe. This allows analysis probes to be connected without powering down the analyzer and yet insures a clean +5 Vdc ramp to the analysis probe when power is applied by software.

A variety of differential and single-ended probes can be connected to the logic analyzer cables. Each probe type is uniquely identified by a different resistor value connected between its probe ID signal and ground.

Comparators. The comparators are differential input/differential output devices that interpret incoming data and clock signals as either high or low. A threshold voltage provided by an internal digital-to-analog-converter (DAC) is coupled to the negative side of the differential signal through a precision resistor. Alternatively, this voltage can be provided to the data channels by a user supplied threshold line in the probe cables. There are separate internal DAC driven thresholds for the data and clock in each pod.

In order to achieve performance, an extensive calibration is performed on each comparator when the board is manufactured and the results of this calibration are stored as Calibration Constants in non-volatile memory on the logic analyzer board. These constants are loaded into the comparators at power on.

Acquisition IC. Each Acquisition IC processes 32 channels of data and 2 channels of clock information. The Acquisition ICs perform data sampling, sequencing, store qualification, pattern recognition, and counting functions. State or Timing sample clocks are sent from the Master card to the Acquisition ICs in each of the Expander cards in a multi-card module. Sampled data is decelerated and passed to the Memory Controller for storage in the Acquisition Memory RAM array.

The Acquisition ICs also contain the 4 GHz sample Timing Zoom circuitry and memory.

Memory Controller and Acquisition Memory. The Memory Controllers store data from the Acquisition ICs into the Acquisition Memory array which is composed of 256 Mbit DDR DRAMs. They also unload data from the memory array after an acquisition is complete, and they deliver the data to the mainframe display system through the mainframe interface connector. In addition they

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control refresh of the RAM array and can perform a search of stored data.

Master/Expander Connectors. Connectors J10 through J15 route state and timing clocks, calibration signals, data search signals, and control from the Master card to all cards in the module.

Connectors J20 through J23 route pattern recognition signals between all cards in a card set as well as control clocks from the Master card to other cards in the set.

Mainframe Interface and Control FPGA. The Mainframe interface consists of an FPGA and the Mainframe Interface Connector. The connector brings power onto the card and provides for control of the card by the analyzer mainframe. It also provides a path for unloading acquired data to the analyzer display.

The FPGA converts bus signals generated by the mainframe processor into control signals for the logic analyzer card. It also provides centralized functions for the card such as I2C, Calibration signals, Flag routing, and Timing mode sample clock.

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Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

• Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

• Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

• If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

• Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

• Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

• Do not install substitute parts or perform any unauthorized modification to the instrument.

• Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

• Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

• Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols



Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.



Hazardous voltage symbol.



Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Agilent Technologies
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901

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Agilent Technologies, Inc.
1900 Garden of the Gods Road
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