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HEWLETT PACKARD

HP 27112A

GENERAL PURPOSE I/O INTERFACE (GPIO)

Installation Manual

Card Assembly: 27112-60001
Date Code: B-2232

Manual Part Number 27112-90001

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This manual provides information for you to install and verify correct operation of the HP 27112A General Purpose I/O Interface (GPIO) card. You will also need the appropriate computer system installation manual. These two manuals should provide all the required information. If your installation is such that you need additional information concerning the GPIO card, order the HP 27132A Technical Reference Package from the nearest Hewlett-Packard Sales and Service Office.

Installation and Checkout

To install and check the operation of the GPIO card, follow the steps below in the order given:

1. Determine if your computer system can supply the power needed for the GPIO card. Refer to table 1 for power requirements.

2. Install jumpers in W1, W2, and W3, depending on whether 5-volt or 12-volt logic levels are to be used. The locations of W1, W2, and W3, and the positions of the jumpers for +5-volt or +12-volt operation are shown in figure 1.

3. Set the card's switches for proper operation in your system. Refer to tables 2, 3, and 4 for switch information. Actual switch settings will vary according to the computer system and the device which is connected to the GPIO card. However, switch settings for the HP 9885 disc drive (a typical device used with the GPIO) are shown below:

DEVICE	SW1								SW2				
	1	2	3	4	5	6	7	8	1	2	3	4	5
HP 9885 Disk Drive	C	C	C	C	C	C	O	C	O	O	O	C	O

O = open
C = closed

4. There are two one-shots (E15, see figure 1) on the GPIO card which generate the write delay and the internal handshake delay. The write delay one-shot provides approximately 100 nsec for the output data to settle. When extra long cables are used, or when the peripheral device requires additional settling time for the data, the delay can be increased by adding a capacitor between pins 1 and 4 of the socket at E16 (see figure 1 for location of E16).

   The formula for selecting the capacitor value is:

$$C = (T - 100)/1.5$$

   where

   C = additional capacitance (in pf)
   T = total time delay required in nsec

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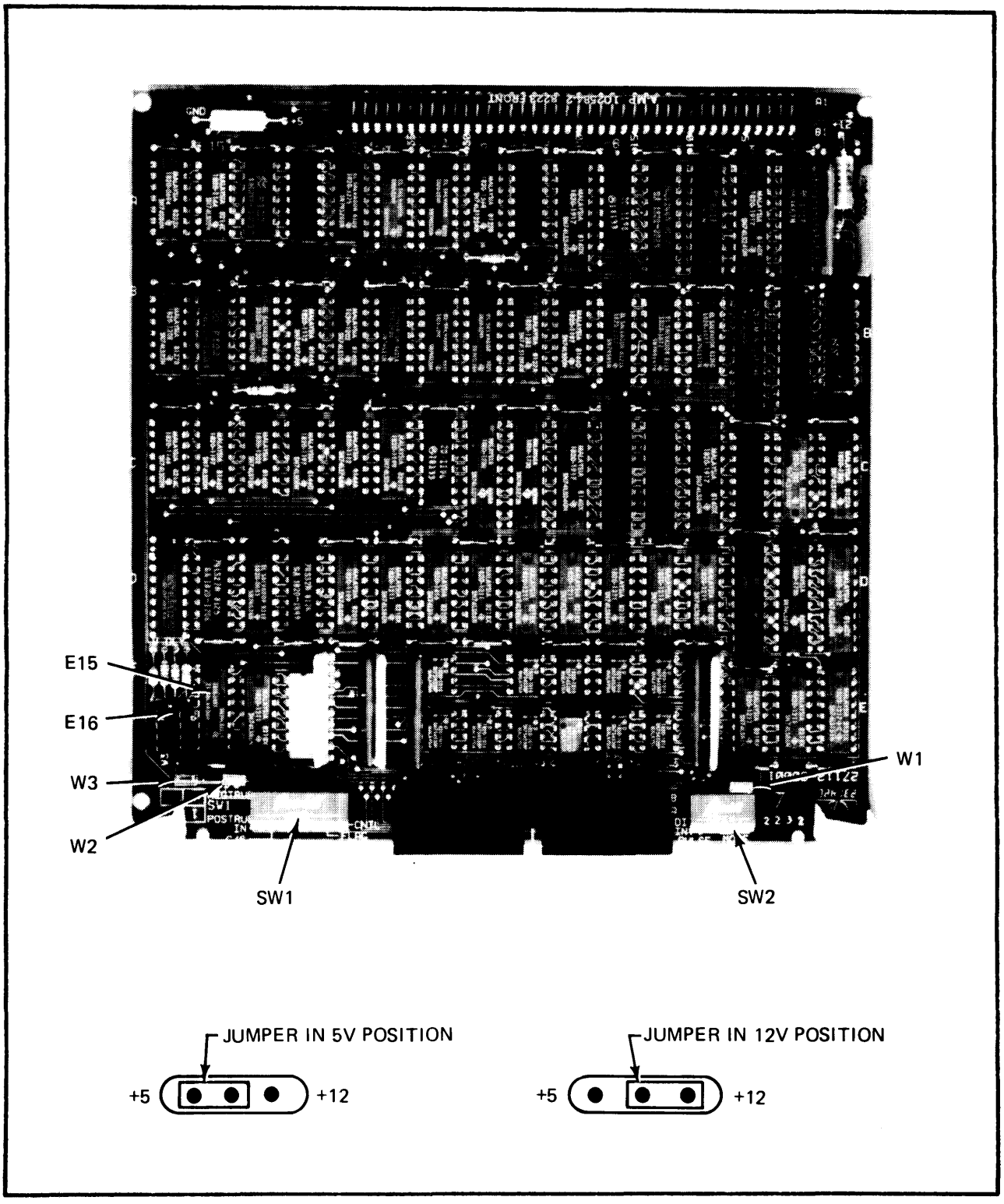


Figure 1. Switch and Jumper Locations

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The internal delay one-shot provides a delay of approximately 3 usec between the assertion of PCNTL and the assertion of FLAG. The delay can be increased by adding a capacitor between pins 5 and 8 of the socket at E16 (see figure 1 for location of E16).

The formula for the value of the capacitor is:

```
C = (T - 3000)/3
```

where,

```
C = additional capacitance (in pf)
T = total time delay required (in nsec)
```

5. Install the card in the appropriate slot in the computer. Refer to the computer system installation manual to determine the correct slot.

6. Connect the cable, supplied with the card, from J2 on the card to the peripheral device. If you have the test hood, which exercises more of the card's circuitry, and can be ordered (Hewlett-Packard part number 1251-8003), connect it to J2 instead of connecting the cable.

7. Turn on computer system power.

8. Run the card verification program. Refer to the appropriate host computer system manual for information on running this program.

9. If a test hood was used, turn off computer power and remove the test hood. Connect the cable and, if necessary, reset the switches for your application.

Reshipment

If the GPIO is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the GPIO.

Pack the card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

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Table 1. Power Requirements

VOLTAGE	+5V OUTPUT		+12V OUTPUT	
	CURRENT	POWER	CURRENT	POWER
+5V +12V	2.2A 0	10.9W 0	2.1A 0.15A	10.6W 1.8W
TOTAL DISSIPATION		10.9W		12.2W

Table 2. Configuration Switch SW1 Definitions

SWITCH ASSEMBLY SW1 - LOGIC SENSE SELECTION			
SWITCH	CONTROLS	OPEN	CLOSED
S1	DIN[15:0]	POSITIVE TRUE	NEGATIVE TRUE
S2	CTL[1:0] and STS[1:0]	POSITIVE TRUE	NEGATIVE TRUE
S3	PSET	POSITIVE TRUE	NEGATIVE TRUE
S4	PDIR	POSITIVE TRUE	NEGATIVE TRUE
S5	DOUT[15:0]	POSITIVE TRUE	NEGATIVE TRUE
S6	PEND	POSITIVE TRUE	NEGATIVE TRUE
S7	PFLAG	POSITIVE TRUE BUSY = HIGH READY = LOW	NEGATIVE TRUE BUSY = LOW READY = HIGH
S8	PCNTL	POSITIVE TRUE ACTIVE = HIGH IDLE = LOW	NEGATIVE TRUE ACTIVE = LOW IDLE = HIGH

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Table 3. Configuration Switch SW2 Definitions

SWITCH ASSEMBLY SW2 - HANDSHAKE CONFIGURATION			
SWITCH	CONTROLS	OPEN	CLOSED
S1	BIDIRECTIONAL BUS ENABLE	DISABLED	ENABLED
S2	INTERNAL HANDSHAKE ENABLE	DISABLED	ENABLED
S3	PULSE HANDSHAKE ENABLE	DISABLED	ENABLED
S4	INPUT CLOCK SEL 0	SEE TABLE 4	
S5	INPUT CLOCK SEL 1	SEE TABLE 4	

Table 4. Switch Settings for Data Input Register Clock Selection

SWITCH		MODE	DATA CLOCKED ON
SW2 - S5	SW2 - S4		
CLOSED	CLOSED	0	Backplane sync cycle completion
CLOSED	OPEN	1	Ready to busy edge of PFLAG (leading edge)
OPEN	CLOSED	2	Busy to ready edge of PFLAG (trailing edge)
OPEN	OPEN	3	Backplane sync cycle completion (Note that this mode is the same as mode 0)

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Table 5. Device Connector J2

GPIO CONN. PIN NO.	SIGNAL MNEMONIC	WIRE COLOR	9885 CONN. PIN NO.	SIGNAL DEFINITION
A1	GND	BLK	2	Ground
A2	DOUT 15	BRN	18	Data Output, bit 15
A3	DOUT 14	RED	19	Data Output, bit 14
A4	DOUT 13	ORN	20	Data Output, bit 13
A5	DOUT 12	YEL	21	Data Output, bit 12
A6	DOUT 11	GRN	22	Data Output, bit 11
A7	DOUT 10	BLU	23	Data Output, bit 10
A8	DOUT 9	VIO	24	Data Output, bit 9
A9	DOUT 8	GRY	25	Data Output, bit 8
A10	DOUT 7	WHT	26	Data Output, bit 7
A11	DOUT 6	WHT-BLK	27	Data Output, bit 6
A12	DOUT 5	WHT-BRN	28	Data Output, bit 5
A13	DOUT 4	WHT-RED	29	Data Output, bit 4
A14	DOUT 3	WHT-ORN	30	Data Output, bit 3
A15	DOUT 2	WHT-YEL	31	Data Output, bit 2
A16	DOUT 1	WHT-GRN	32	Data Output, bit 1
A17	DOUT 0	WHT-BLU	33	Data Output, bit 0
A18	GND	WHT-VIO	8	Ground
A19	PCNTL	WHT-GRY	10	Peripheral control
A20	PDIR	WHT-BLK-BRN	15	Peripheral direction
A21	GND	WHT-GRN-BLU	N/C	Ground
A22	PRESET	WHT-BLK-RED	5	Peripheral reset
A23	CTL0	WHT-BLK-ORN	4	Control Output Bus, bit 0
A24	CTL1	WHT-BLK-YEL	6	Control Output Bus, bit 1
A25	GND	WHT-BLK-GRN	11	Ground
N/C	Shield	Drain	1	Shield

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Table 5. Device Connector J2 (Continued)

GPIO CONN. PIN NO.	SIGNAL MNEMONIC	WIRE COLOR	9885 CONN. PIN NO.	SIGNAL DEFINITION
B1	GND	WHT-BLK-BLU	3	GROUND
B2	DIN 15	WHT-BLK-VIO	35	Data Input, bit 15
B3	DIN 14	WHT-BLK-GRY	36	Data Input, bit 14
B4	DIN 13	WHT-BRN-RED	37	Data Input, bit 13
B5	DIN 12	WHT-BRN-ORN	38	Data Input, bit 12
B6	DIN 11	WHT-BRN-YEL	39	Data Input, bit 11
B7	DIN 10	WHT-BRN-GRN	40	Data Input, bit 10
B8	DIN 9	WHT-BRN-BLU	41	Data Input, bit 9
B9	DIN 8	WHT-BRN-VIO	42	Data Input, bit 8
B10	DIN 7	WHT-BRN-GRY	43	Data Input, bit 7
B11	DIN 6	WHT-RED-ORN	44	Data Input, bit 6
B12	DIN 5	WHT-RED-YEL	45	Data Input, bit 5
B13	DIN 4	WHT-RED-GRN	46	Data Input, bit 4
B14	DIN 3	WHT-RED-BLU	47	Data Input, bit 3
B15	DIN 2	WHT-RED-VIO	48	Data Input, bit 2
B16	DIN 1	WHT-RED-GRY	49	Data Input, bit 1
B17	DIN 0	WHT-ORN-YEL	50	Data Input, bit 0
B18	GND	WHT-ORN-GRN	9	Ground
B19	PFLAG	WHT-ORN-BLU	13	Peripheral flag
B20	---	WHT-ORN-VIO	N/C	Not used
B21	PEND	WHT-ORN-GRY	16	Peripheral end
B22	---	WHT-YEL-GRN	17	Not used
B23	STS 0	WHT-YEL-BLU	14	Status Input Bus, bit 0
B24	STS 1	WHT-YEL-VIO	7	Status Input Bus, bit 1
B25	GND	WHT-YEL-GRY	12	Ground
---	---	N/C	34	Not used

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