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HP 27130A

EIGHT-CHANNEL MULTIPLEXER (MUX)

Technical Reference Manual

Card Assembly: 5061-4929
Date Code: A-2301

HEWLETT PACKARD

HEWLETT-PACKARD COMPANY
Roseville Networks Division
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Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual *will* contain new information, as *well* as updates.

First Edition.....June 1983

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CONTENTS

Section I — Page

GENERAL INFORMATION

- Physical Description..... 1-1
- Functional Description..... 1-1
- Equipment Supplied..... 1-3
- Identification..... 1-3
  - The Product..... 1-3
  - Printed Circuit Card..... 1-3
  - Manuals..... 1-4
- Specifications..... 1-4

Section II — Page

INSTALLATION

- Determining Current Requirements..... 2-1
- Firmware (EPROM) Installation..... 2-1
- Jumpers..... 2-3
  - Memory Configuration Jumper..... 2-3
  - Signature Analysis Jumper..... 2-3
- I/O Channel Interface..... 2-5
- Peripheral Device Interface..... 2-5
- Installing the MUX..... 2-12
- Checkout..... 2-13
- Reshipment..... 2-14

Section III — Page

PRINCIPLES OF OPERATION

- Functional description..... 3-1
  - System Clocks..... 3-3
  - Memory Address Space..... 3-3
  - I/O Address Space..... 3-6
  - Z-80B Microprocessor CPU..... 3-6
  - Z-80 SIO/2 (Serial I/O Controller)..... 3-6
  - CTC (Counter Timer Circuit..... 3-19
  - Interfacing to the BIC..... 3-19
  - Memory Interface Circuit (MIC)..... 3-24
    - Register 0 - MIC Configuration..... 3-24
    - Register 1 - DMA B Upper Byte of Memory Address..... 3-24
    - Register 2 - DMA Lower Byte of Memory Address..... 3-24
    - Register 3 - DMA B Configuration..... 3-25
    - Register 4 - Lower Byte of Transfer Byte Count..... 3-25
    - Register 5 - DMA B I/O Port Address..... 3-25
    - Register 6 - DMA A Upper Byte of Memory Address..... 3-25
    - Register 7 - DMA A Lower Byte of Memory Address..... 3-25
    - Register 8 - DMA A Configuration..... 3-26

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CONTENTS

Register 9 - Lower Byte of Transfer Byte Count..... 3-26
Register A - DMA A I/O Port Address..... 3-26
Register B - Interrupt Vector..... 3-26
Priority Interrupt Structure..... 3-27
Wait State Circuits for Interrupt Acknowledge..... 3-27
Diagnostic Hood for External Loop Back..... 3-28

Section IV Page
PROGRAMMING
MUX Programmable Features..... 4-1
Transactions..... 4-2
Connect Logical Channel Request Format..... 4-2
Capabilities..... 4-4
Receive Character Processing..... 4-4
Receive Error Conditions..... 4-5
Signal Character..... 4-5
Edit Mode..... 4-6
Backspace..... 4-6
Line Deletion..... 4-6
Software Handshake with the Device..... 4-7
Host ENQ/ACK Handshake..... 4-7
Device X-ON/X-OFF Handshake..... 4-8
Host X-ON/X-OFF Handshake..... 4-8
Single Text Termination..... 4-9
End-On-Count Text Termination..... 4-9
Alert 1 Mode..... 4-9
Type Ahead and Echoing..... 4-10
Receiving Transparent or Binary Data..... 4-11
Read Request Length..... 4-11
Host Initiated Text Termination..... 4-12
Transmit Character Processing..... 4-12
Automatic Output Separators Appendage..... 4-12
Transmitting Transparent or Binary Data..... 4-12
Buffer Flushing..... 4-12
Programming the Receiver and Transmitter..... 4-13
Parity in Transmitted or Received data..... 4-15
Break Detection..... 4-15
Handshake Timer..... 4-15
Additional Options..... 4-16
Error Handling..... 4-16
Quoting Character Mode Option..... 4-18
Conditional Output Separators Appendage..... 4-18
Speed Sense Mode..... 4-18
Asynchronous Events..... 4-19
Solicited Events..... 4-19
Diagnostics..... 4-20

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CONTENTS

Connect Logical Channel Request Definitions..... 4-21
Read Device Data, Request Code = 1..... 4-22
Write Device Data, Request Code = 2..... 4-22
Read Card Information, Request Code = 4..... 4-23
Subfunctions 0 through 33..... 4-23
Subfunction 249 - Read Data Status..... 4-23
Subfunction 250. Get Card RAM..... 4-23
Subfunction 254. Get Card Status..... 4-24
Write Card Configuration, Request Code = 5..... 4-25
Subfunction 0..... 4-25
Subfunction 1. Configure Read Option..... 4-28
Subfunction 2. End-On-Count Length..... 4-29
Subfunction 3. Alert 1 Read Mode..... 4-29
Subfunction 5. Transmission Mode..... 4-30
Subfunction 6. Backspace Character..... 4-30
Subfunction 7. Line Delete Character..... 4-30
Subfunction 8. Backspace and Other Options..... 4-31
Subfunction 9. Device Handshake Option..... 4-32
Subfunction 10. Baud Rate..... 4-33
Subfunction 11. Character Length..... 4-33
Subfunction 12. Number Of Stop Bits..... 4-34
Subfunction 13. Parity..... 4-34
Subfunction 18. Character Handshake Timer..... 4-35
Subfunction 21. Host Interrupt Mask..... 4-35
Subfunction 22. Host X-ON/X-OFF Characters..... 4-36
Subfunction 23. Device X-ON/X-OFF Characters..... 4-37
Subfunction 24. Host ENQ/ACK Characters..... 4-37
Subfunction 25. Host ENQ/ACK Pacing Counter..... 4-37
Subfunction 27. Single Text Terminator for Echoing CR-LF... 4-37
Subfunction 28. Output Separator..... 4-37
Subfunction 31. Additional Options..... 4-38
Subfunction 32. Single Text Terminator..... 4-39
Subfunction 33. Card Write Register..... 4-39
Subfunction 34. Set Port ID..... 4-40
Control Card, Request Code = 6..... 4-40
RTS and WTC Block Definitions..... 4-41
Event Block Description..... 4-42
Read Status Request Block Definitions..... 4-44
Identity Information Block Definitions..... 4-46
Default MUX Configuration..... 4-46
Subfunction Assignment Summary..... 4-48
Read Device Data..... 4-49
Write Device Data..... 4-49
Read Card Information..... 4-49
Write Card Configuration..... 4-49
Control Card..... 4-51

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CONTENTS

Section V — Page
MAINTENANCE..... 5-1

Section VI — Page
REPLACEABLE PARTS
Replaceable Parts..... 6-1
Ordering Information..... 6-1

Section VII — Page
SCHEMATIC DIAGRAMS..... 7-1

Appendix A — Page
ASCII CHARACTERS AND BINARY CODES..... A-1

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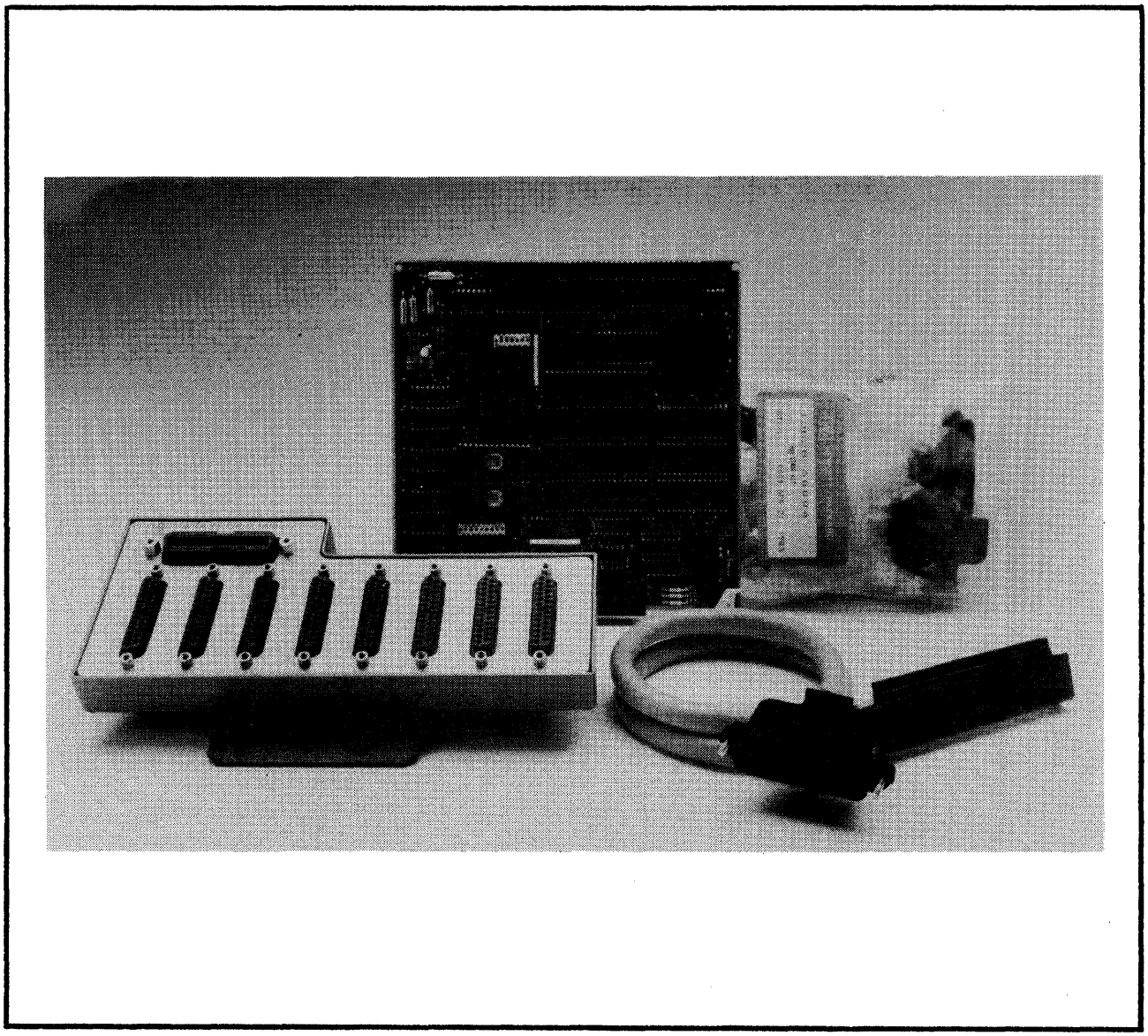


Figure 1-1. HP 27130A MUX

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GENERAL INFORMATION

SECTION I

This manual provides general information, installation, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard HP 27130A Eight-Channel Multiplexer (MUX). This chapter contains general information concerning the MUX, and includes a description and specifications.

PHYSICAL DESCRIPTION

The HP 27130A Eight-Channel Multiplexer (MUX) is shown in figure 1-1 and consists of a printed circuit card, a cable, an RS-232-C connection box, and an installation manual.

FUNCTIONAL DESCRIPTION

The HP 27130A Eight-Channel Multiplexer provides multiplexed connections between a Hewlett-Packard computer system and up to eight EIA RS-232-C/RS-423-A/RS-422-A type devices (not including modems).

Figure 1-2 shows a Hewlett-Packard computer system using CHANNEL I/O and the MUX. (CHANNEL I/O is a Hewlett-Packard standard defining the physical and electrical characteristics for an I/O system consisting of an I/O channel, an I/O channel adapter, and I/O cards. The MUX is one of the I/O cards.)

Note that the computer system CPU and memory communicate directly along a Memory/Processor Bus (MPB). I/O data to/from peripheral devices reaches the CPU/memory through the I/O channel, the I/O channel adapter, and an I/O card such as the MUX card. The I/O data is received from and transmitted to peripheral devices by the I/O card, which converts device-specific data to a format compatible with the I/O channel, and thus the computer. The I/O channel adapter (see figure 1-2) controls the flow of traffic between the I/O channel and the memory/processor bus.

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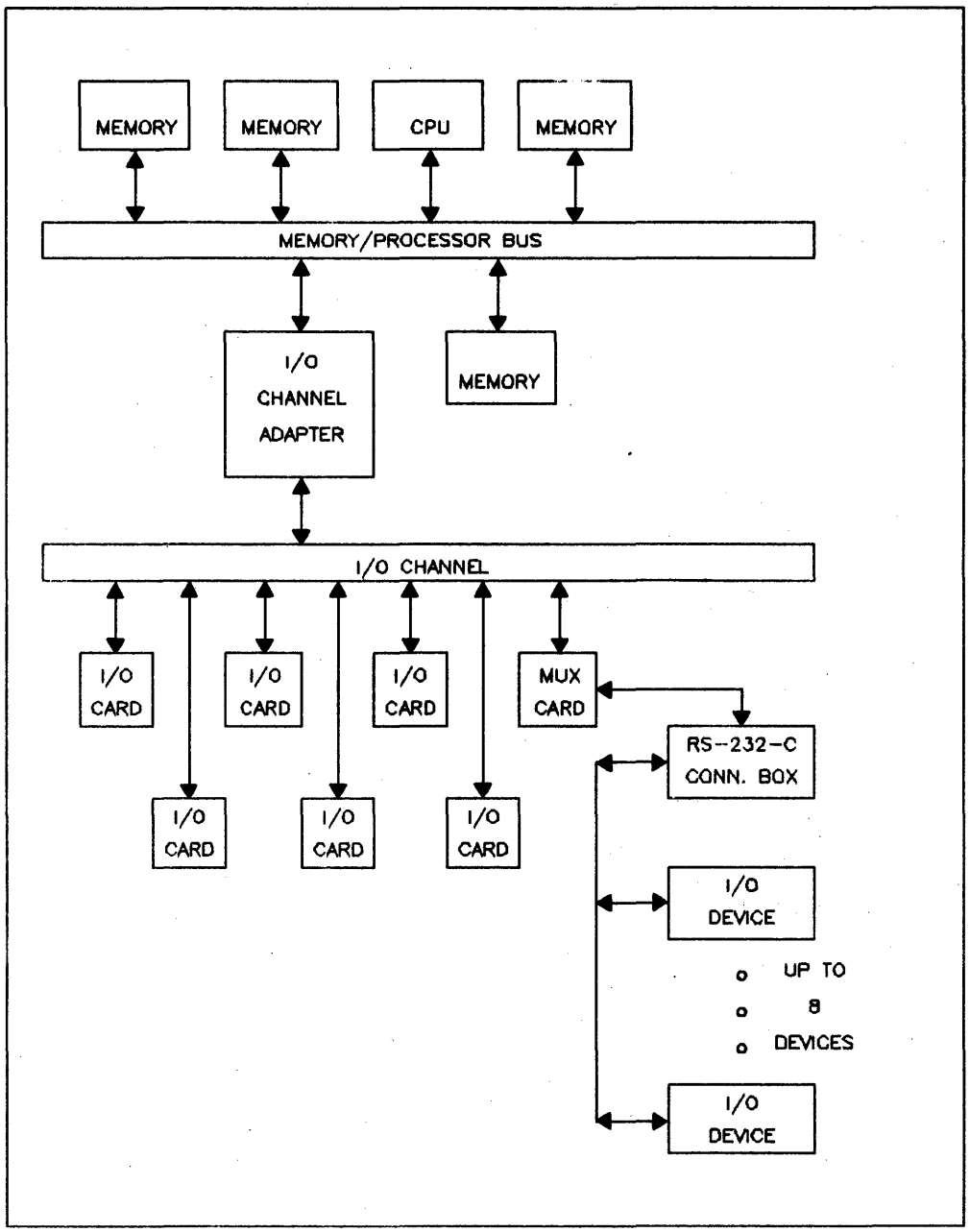


Figure 1-2. MUX in a Typical Hewlett-Packard Computer System

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The HP 27130A uses several of the Z-80A family of microprocessor components to relieve the host computer of much of the overhead. This permits a wide range of configurable transmission modes and formats, thus allowing connections to various CRT terminals, printing terminals, printers, and plotters.

EQUIPMENT SUPPLIED

The standard HP 27130A Eight-Channel Multiplexer consists of the following items (see figure 1-1):

Printed circuit card, part number 5061-4929

Seventy centimeter (27.5 inch) RS-232-C connection box cable, part number 8120-4076

RS-232-C connection box, part number 12828-60001

Extension cable kit, part number 12828-60004

EPROMs, part numbers 27130-80003 and 27130-80004

Installation manual, part number 27130-90001

IDENTIFICATION

The Product

Up to five digits and a letter (27130A in this case) are used to identify Hewlett-Packard products. The five digits identify the product; the letter indicates the revision level of the product.

Printed Circuit Card

The printed circuit card supplied with the HP 27130A product is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., A-2301). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the MUX card is:

5061-4929
A-2301

If the date code stamped on the card does not agree with the date code on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

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Manuals

The Installation Manual (part number 27130-90001, supplied with the HP 27130A product) and this manual (HP 27130 Technical Reference Manual, part number 27132-90006) are identified by name and part number. (Note that this manual is part of the HP 27132A Technical Reference Package.) The name, part number, and publication date are printed on the title page of each manual. If the manual is revised, the publication date is changed. In this manual, the "Printing History" page (page ii) records the reprint dates and manual update record. Reprint dates for the Installation Manual are printed on the title page.

SPECIFICATIONS

Table 1-1 lists the specifications of the MUX.

Table 1-1. Specifications

FEATURES

* Eight full-duplex asynchronous serial I/O ports
* EIA RS-232-C/RS-423-A compatible
* Simplex, echoplex, half-duplex, or full-duplex mode operation
* Asynchronous baud rates from 110 baud to 19.2K baud
* Programmable character size of 7 or 8 bits
* 1 or 2 stop bits
* Parity: programmable even, odd, forced 1, forced 0, or none
* Break detection
* Parity, overrun, and framing error detection
* Firmware based self-test
* Optional device handshakes: host or device controlled X-ON/X-OFF, or host controlled ENQ/ACK
* 16-bit parallel interface to I/O channel (backplane)

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Table 1-1. Specifications (Continued)

PHYSICAL CHARACTERISTICS

Size:	193.04 mm long by 171.45 mm wide by 16.383 mm thick (7.6 by 6.75 by 0.645 inches)
Weight:	283.5 grams (0.625 pound)
I/O Channel Interconnects:	80-pin connector, J1
Device Interconnects:	72-pin connector, J2

POWER REQUIREMENTS

	Current (amps)		Power Dissipation (watts)	
Voltage	(typical)	(2-sigma)	(typical)	(2-sigma)
+5V	1.672A	1.890A	8.36W	9.45W
+12V	0.052A	0.062A	0.62W	0.74W
-12V	0.075A	0.085A	0.90W	1.02W

MTBF = 32K HRS (6-19-86)

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INSTALLATION

SECTION II

This section provides information on installing and checking the operation of the MUX.

DETERMINING CURRENT REQUIREMENTS

The MUX circuit card obtains its operating voltages from the host computer power supply through the I/O channel. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the card are listed in the power requirements entry of table 1-1. Current requirements for all other I/O cards can be found in the appropriate Technical Reference Manuals.

FIRMWARE (EPROM) INSTALLATION

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD OR REMOVING OR REPLACING COMPONENTS.

The EPROMs are installed in sockets provided on the MUX card as shown in figure 2-1. Ensure that they are installed properly, and that they have not been damaged or loosened from their sockets during shipping.

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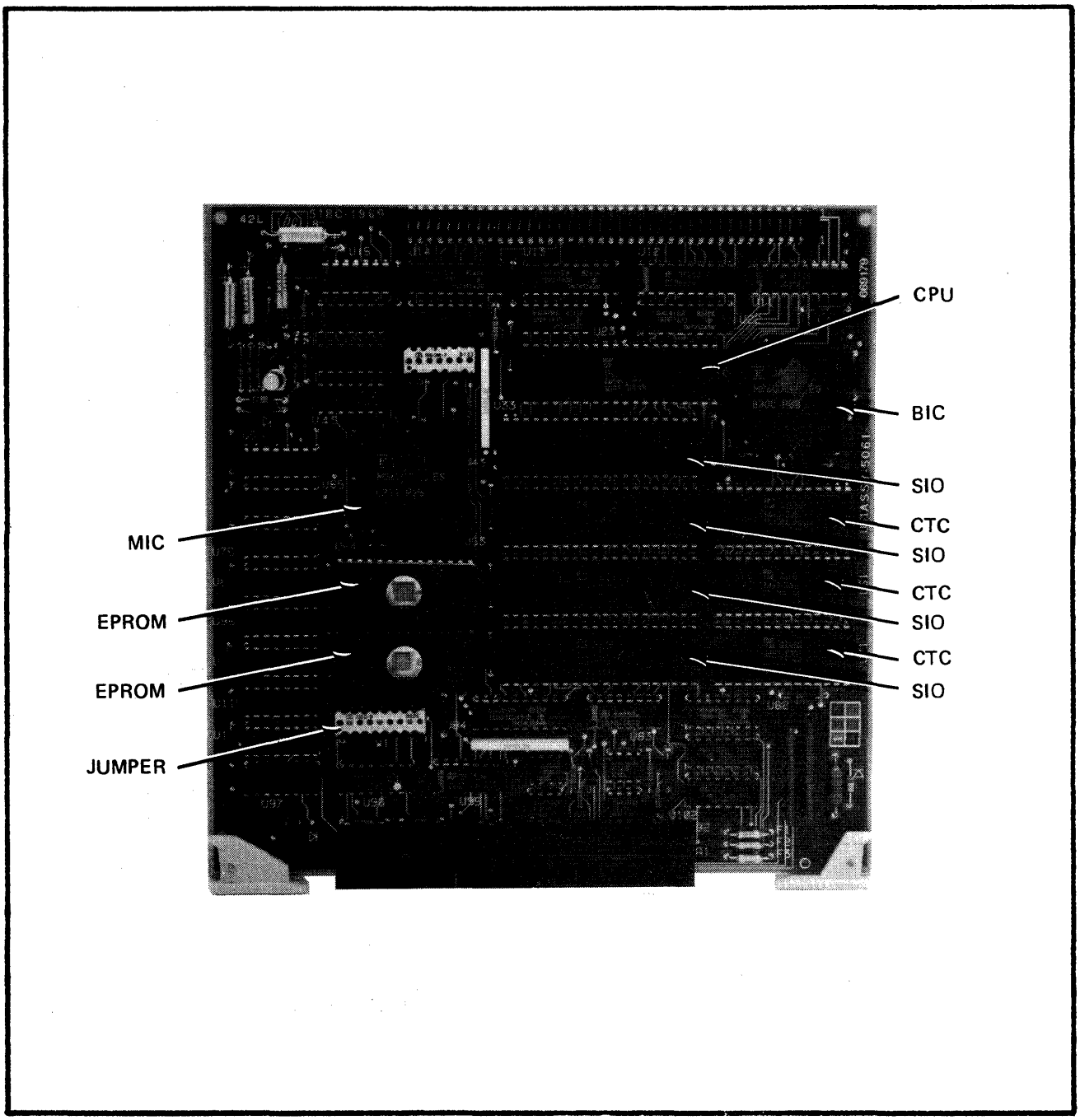


Figure 2-1. Component and Jumper Locations

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Additionally, when installing or removing EPROMs, guard against bending or breaking the pins on the component. These pins also can become folded between the component and its socket, which would result in intermittent operation of the MUX. In most cases, a bent or damaged pin can be straightened with careful use of needle-nose pliers.

JUMPERS

There are two jumpers on the MUX card: a Memory Configuration jumper, and a Signature Analysis jumper. The locations of these two jumpers are shown on figure 2-1.

Memory Configuration Jumper

The Memory Configuration jumper, W1, is an internally-connected, 18-pin dual in-line package (DIP) shunt network. The jumper is used to configure the two memory sockets (U64 and U74) to accomodate different kinds of EPROMs and static RAMs. The pin diagram of W1 is shown in figure 2-2, pin functions are listed in table 2-1.

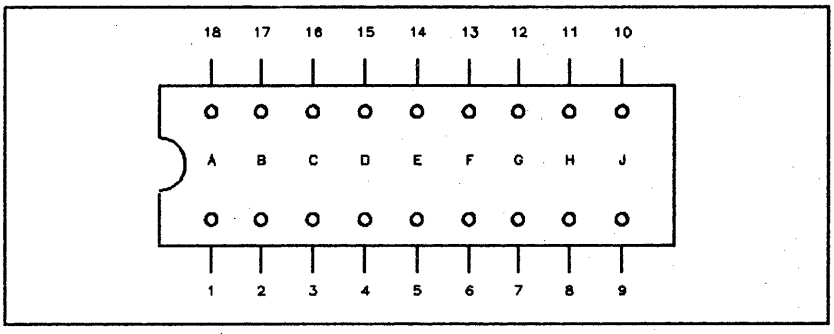


Figure 2-2. Memory Configuration Jumper

Signature Analysis Jumper

The Signature Analysis jumper, U34, is a 14-pin pre-programmed shunt network. The internal connections of this jumper are set at the factory and are shown in figure 2-3 for information only.

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Table 2-1. Functions of the Memory Configuration Jumper

JUMPER	FUNCTION
A	Installed only when a 16K byte EPROM is used in socket U64. Position A connects OCE2- of the Memory Interface Circuit (MIC) to pin 20 (CE-) of the EPROM in socket U64. This enables the EPROM in socket U64 whenever the lower 16K bytes of memory are addressed.
B	Installed only when a 4K or 8K byte EPROM is used in socket U64. Position B connects OCE0- of the MIC to pin 18 (CE-) of the 4K byte EPROM or pin 20 (CE-) of the 8K byte EPROM, depending on which EPROM is installed in socket U64. This enables the EPROM in socket U64 whenever the lower 8K bytes of memory are addressed.
C	Installed only when a 4K byte EPROM is used in socket U64. Position C connects +5V power to pin 24 (VDD) of the 4K byte EPROM.
D	Installed only when a 16K byte EPROM is used in socket U64. Position D connects A13 of the address bus to pin 24 (A13) of the 16K byte EPROM.
E	Installed only when an 8K byte EPROM is used in socket U74. Position E connects +5V power to pin 27 (VPP-) of the 8K byte EPROM.
F	Installed only when an 8K byte static RAM is used in socket U74. Position F connects WR- of the Z-80B CPU to pin 27 (WE-) of the static RAM, thus enabling the CPU to write to the RAM.
G	Installed only when a 2K byte static RAM is used in socket U74. Position G connects WR- of the Z-80B CPU to pin 21 (WE-) of the static RAM, thus enabling the CPU to write to the RAM.
H	Installed only when a 4K or 8K byte EPROM or an 8K byte static RAM is used in socket U74. Position H connects A11 of the Z-80B CPU address bus to pin 23 (A11) of the 4K or 8K byte EPROM or 8K byte RAM, depending on which device is installed in socket U74.
J	Installed to enable the MIC wait state signal when slow EPROMs (access time greater than 250 nsec) are used in U64 or U74.

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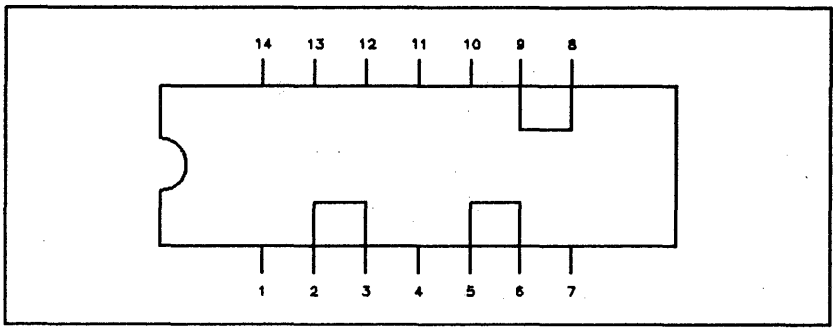


Figure 2-3. Signature Analysis Jumper Internal Connections

I/O CHANNEL INTERFACE

All interface between the MUX and the host computer occurs on the I/O channel. An 80-pin connector (J1) located on the MUX mates with a receptacle on the I/O channel. Connections to J1 are listed in table 2-2.

PERIPHERAL DEVICE INTERFACE

Interface between the MUX card and up to eight peripheral devices is via a 72-pin connector (J2) to a connection panel (RS-232-C Connection Box, part number 12828-60001) and from there, via eight separate connectors and eight cables, to the peripheral devices. A connection diagram for the connection box is shown in figure 2-4.

Connector J2 pin assignments are shown in table 2-3. Pin assignments for J2 and the connection panel are shown in table 2-4. Note that, in table 2-4, there are eight pairs of Send Data (SD) and Signal Ground (SG) lines, and eight pairs of Receive Data (RD) and Signal Ground (SG) lines; that is, one pair of Send Data lines and one pair of Receive Data lines for each of the eight connectors (J0 through J7) to the eight peripheral devices.

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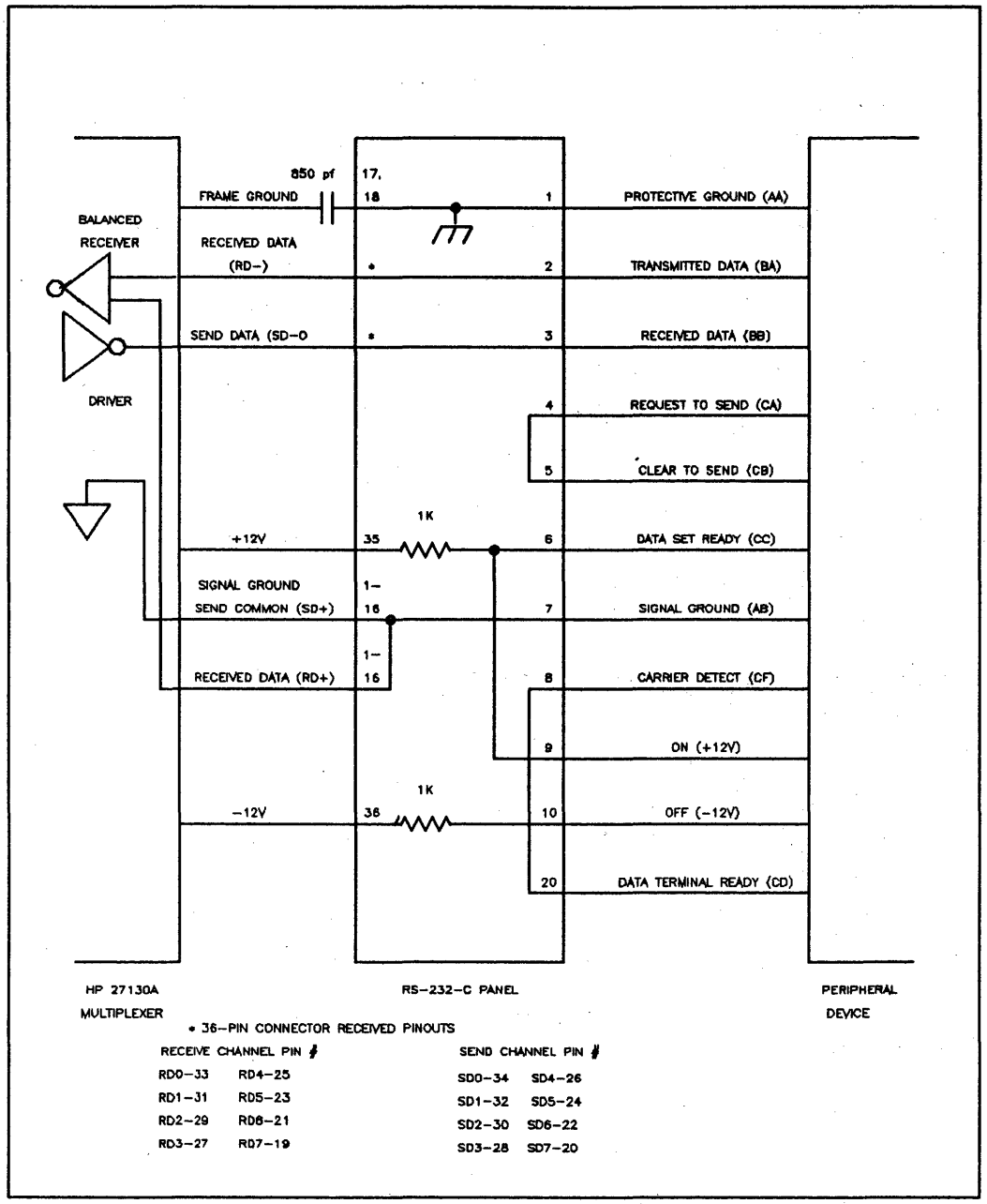


Figure 2-4. Connections from MUX to Connection Box to Device

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Table 2-2. I/O Channel Connector J1

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
A1	RES	Not used
A2	DB14-	Data Bus, Bit 14
A3	DB12-	Data Bus, Bit 12
A4	GND	Ground
A5	DB10-	Data Bus, Bit 10
A6	DB8-	Data Bus, Bit 8
A7	GND	Ground
A8	DB6-	Data Bus, Bit 6
A9	DB4-	Data Bus, Bit 4
A10	GND	Ground
A11	DB2-	Data Bus, Bit 2
A12	DB0-	Data Bus, Bit 0
A13	GND	Ground
A14	AD2-	Address Bus, Bit 2
A15	AD0-	Address Bus, Bit 0
A16	GND	Ground
A17	DOUT-	Data Out
A18	BP0-	Bus Primitive Bit 0
A19	CEND-	Channel End
A20	SYNC-	Synchronize
A21	GND	Ground
A22	CCLK	Common Clock
A23	GND	Ground
A24	BR-	Burst Request
A25	DBYT-	Device Byte
A26	MYAD-	My Address
A27	GND	Ground
A28	---	Not used
A29	---	Not used
A30	---	Not used
A31	RES	Not used
A32	PFW-	Power-Fail Warning
A33	PPON	Primary Power On
A34	GND	Ground
A35	AC-	Not used
A36	AC+	Not used
A37	-12	-12V
A38	+12	+12V
A39	+5S	Not used
A40	+5P	+5P

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Table 2-2. I/O Channel Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
B1	---	Not used
B2	DB15-	Data Bus, Bit 15
B3	DB13-	Data Bus, Bit 13
B4	GND	Ground
B5	DB11-	Data Bus, Bit 11
B6	DB9-	Data Bus, Bit 9
B7	GND	Ground
B8	DB7-	Data Bus, Bit 7
B9	DB5-	Data Bus, Bit 5
B10	GND	Ground
B11	DB3-	Data Bus, Bit 3
B12	DB1-	Data Bus, Bit 1
B13	GND	Ground
B14	AD3-	Address Bus, Bit 3
B15	AD1-	Address Bus, Bit 1
B16	GND	Ground
B17	UAD-	Unary Address
B18	BP1-	Bus Primitive Bit 1
B19	CBYT-	Channel Byte
B20	POLL-	Poll
B21	GND	Ground
B22	IOSB-	I/O Strobe
B23	GND	Ground
B24	ARQ-	Attention Request
B25	DEND-	Device End
B26	IFC-	Interface Clear
B27	GND	Ground
B28	---	Not used
B29	---	Not used
B30	RES	Not used
B31	ISPU	Not used
B32	NMI-	Non-Maskable Interrupt
B33	SPON	Secondary Power On (NOT USED BY MUX CARD)
B34	GND	Ground
B35	AC-	Not used
B36	AC+	Not used
B37	-12	-12V
B38	+12	+12V
B39	+5S	Not used
B40	+5P	+5P

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Table 2-3. Connector J2 Pin Assignments

J2 PIN NO.	J2 MNEMONIC	SIO MNEMONIC	J2 PIN. NO.	J2 MNEMONIC	SIO MNEMONIC
B25 B26 B27	SD0 (A) SG0 SD0 (B)	TxD0	B4 B6	RD0 (A) RD0 (B)	RxD0
A25 A26 A27	SD1 (A) SG1 SD1 (B)	TxD1	A4 B7	RD1 (A) RD1 (B)	RxD1
B28 B29 B30	SD2 (A) SG2 SD2 (B)	TxD2	A6 B8	RD2 (A) RD2 (B)	RxD2
A28 A29 A30	SD3 (A) SG3 SD3 (B)	TxD3	A8 B9	RD3 (A) RD3 (B)	RxD3
B31 B32 B33	SD4 (A) SG4 SD4 (B)	TxD4	A10 B10	RD4 (A) RD4 (B)	RxD4
A31 A32 A33	SD5 (A) SG5 SD5 (B)	TxD5	A12 B11	RD5 (A) RD5 (B)	RxD5
B34 B35 B36	SD6 (A) SG6 SD6 (B)	TxD6	A14 B12	RD6 (A) RD6 (B)	RxD6
A34 A35 A36	SD7 (A) SG7 SD7 (B)	TxD7	B15 B13	RD7 (A) RD7 (B)	RxD7

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Table 2-3. Connector J2 Pin Assignments (Continued)

J2 PIN NO.	J2 MNEMONIC	SIO MNEMONIC	J2 PIN NO.	J2 MNEMONIC	SIO MNEMONIC
A17 B17	SD0 SC0	TxD0	A21 B21	SD4 SC4	TxD4
A18 B18	SD1 SC1	TxD1	A22 B22	SD5 SC5	TxD5
A19 B19	SD2 SC2	TxD2	A23 B23	SD6 SC6	TxD6
A20 B20	SD3 SC3	TxD3	A24 B24	SD7 SC7	TxD7
A3 B3	HOOD_ON- HLED	CTSA0- ----	B14 A16	SG GND	---- ----
A2 B2	-12V +12V	---- ----	B1 A1	+5V GND(PWR)	----

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Table 2-4. RS-232-C/RS-423-A Cables

J2 PIN NO.	J2 MNEMONIC	PANEL PIN NO.	PANEL MNEMONIC	COLOR	PAIR NO.
--- *	-----	17,18	SHIELD	-----	---
A17	SD0	34	SD (J0)	LT RED	9
B17	SC0	16	SG (J0)	BLACK	9
A18	SD1	32	SD (J1)	DK GREEN	10
B18	SC1	14	SG (J1)	BLACK	10
A19	SD2	30	SD (J2)	DK VIOLET	11
B19	SC2	12	SG (J2)	BLACK	11
A20	SD3	28	SD (J3)	LT BLUE	12
B20	SC3	10	SG (J3)	BLACK	12
A21	SD4	26	SD (J4)	DK BLUE	13
B21	SC4	8	SG (J4)	BLACK	13
A22	SD5	24	SD (J5)	LT VIOLET	14
B22	SC5	6	SG (J5)	BLACK	14
A23	SD6	22	SD (J6)	BROWN	15
B23	SC6	4	SG (J6)	BLACK	15
A24	SD7	20	SD (J7)	DK RED	16
B24	SC7	2	SG (J7)	BLACK	16
B4	RD0 (A)	33	RD (J0)	NATURAL	1
B6 **	RD0 (B)	15	SG (J0)	BLACK	1
A4	RD1 (A)	31	RD (J1)	WHITE	2
B7 **	RD1 (B)	13	SG (J1)	BLACK	2
A6	RD2 (A)	29	RD (J2)	YELLOW	3
B8 **	RD2 (B)	11	SG (J2)	BLACK	3
A8	RD3 (A)	27	RD (J3)	ORANGE	4
B9 **	RD3 (B)	9	SG (J3)	BLACK	4
A10	RD4 (A)	25	RD (J4)	TAN	5
B10 **	RD4 (B)	7	SG (J4)	BLACK	5
A12	RD5 (A)	23	RD (J5)	PINK	6
B11 **	RD5 (B)	5	SG (J5)	BLACK	6
A14	RD6 (A)	21	RD (J6)	GRAY	7
B12 **	RD6 (B)	3	SG (J6)	BLACK	7
B15	RD7 (A)	19	RD (J7)	LT GREEN	8
B13 **	RD7 (B)	1	SG (J7)	BLACK	8

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Table 2-4. RS-232-C/RS-423-A Cables (Continued)

J2 PIN NO.	J2 MNEMONIC	PANEL PIN NO.	PANEL MNEMONIC	COLOR	PAIR NO.
B14 **	SG	--	-----	---	--
B2	+12V	35	ON	DK RED (SINGLE)	1
A2	-12V	36	OFF	DK BLUE (SINGLE)	2

* - Shield connected to chassis ground through a decoupling capacitor in J2 connector hood.
** - These signals bused together at connector J2.

INSTALLATION

CAUTION

ALWAYS ENSURE THAT THE POWER TO THE COMPUTER IS OFF BEFORE INSERTING OR REMOVING THE MUX CIRCUIT CARD AND CABLE. FAILURE TO DO SO MAY RESULT IN DAMAGE TO THE MUX.

CAUTION

SOME OF THE COMPONENTS USED ON THE PRINTED CIRCUIT CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

Install the MUX as follows:

1. Determine if your computer system can supply the power needed for the MUX card. Refer to table 1-1 in Section I for power requirements.

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2. Verify that the Memory Configuration jumper is configured correctly for the EPROMs/RAMs installed on the card. To verify that the jumper is configured correctly, determine what types of EPROMs/RAMs are installed in sockets U64 and U74, then refer to table 2-1 to verify that the correct jumpers are closed.

3. Install the card in the appropriate slot in the computer. Refer to the computer system installation manual to determine the correct slot. When installing the card, use care not to damage components or traces on the card or on adjacent cards. Press the MUX card firmly into place.

4. Connect the cable supplied with the card from J2 to the RS-232-C connection box. If you have the test hood, which exercises more of the card's circuitry, and can be ordered (Hewlett-Packard part number 0950-1659), connect it to J2 instead of connecting the cable.

CAUTION

BE SURE AND INSTALL THE DIAGNOSTIC TEST HOOD SO THAT ITS COMPONENT SIDE (THE SIDE WITH THE LED) MATCHES THE COMPONENT SIDE ON THE MUX CARD. DAMAGE TO THE MUX CARD CAN RESULT IF THE COMPONENT SIDES OF THE TWO DEVICES DO NOT MATCH.

START-UP

To start up and verify correct operation of the MUX, perform the following:

1. Turn on computer system power.

2. A self-test is contained on the card. The host computer system determines if the self-test is run automatically at power-on or must be invoked by the user. Refer to the appropriate manual for your system for a description of self-test initiation.

   a. If the diagnostic test hood is not installed when the self-test executes, the LED located on the card should light briefly and go out. This indicates that the card passed self-test. If the LED does not light at all, the card is defective. If the LED stays on, the card did not pass self-test. For either of these latter two cases, it is recommended that you return the card to Hewlett-Packard; refer to the next paragraph for reshipment information. If you wish to perform maintenance on the card, however, refer to Sections V, VI, and VII for maintenance information, replaceable parts lists, and schematic logic diagrams, respectively.

   b. If the diagnostic test hood is installed when the self-test executes, the conditions in step 2.a. should occur, plus the LED located on the test hood should light briefly and go out. If the LEDs (the one mounted on the card and the one on the diagnostic test hood) do not light at all, or if they light and stay on, the causes are the same as in step 2.a.

3. Refer to your system documentation for information on using the MUX in your system.

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RESHIPMENT

If the MUX is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the MUX.

Pack the card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

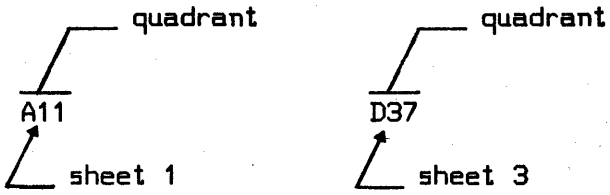
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PRINCIPLES OF OPERATION

SECTION III

FUNCTIONAL DESCRIPTION

A functional block diagram of the HP 27130 Eight-Channel Multiplexer is shown in figure 3-1. Reference will also be made to the schematic logic diagram contained in Section VII, figure 7-1. Note that figure 7-1 consists of five sheets. References to this figure will be as follows: A11, 7-1; C23, 7-1; D37, 7-1, etc., where the first digit (1, 2, 3, 4, or 5) refers to the sheet number; the combination of letters A through E and numbers 11 through 58 (A11, D37, etc.) refer to the quadrants on the individual sheets; and 7-1 refers to the figure number. For example,



Circuitry contained on the MUX card includes a Backplane Interface Circuit (BIC) gate array and its support circuits, a Z-80B microprocessor (CPU), three Z-80 Counter Timer Circuits (CTCs), four Z-80 Serial I/O circuits (SIO/2s), up to 16K bytes of EPROM in two 28-pin sockets, a Memory Interface Circuit (MIC) gate array, 64K bytes of dynamic RAM (48K available) RS-422-A/RS-423-A transmitters and receivers (compatible with RS-232-C and CCITT V.28), and I/O channel (backplane) and peripheral device panel (frontplane) connectors.

The heart of the MUX card is the Z-80B CPU (U33, see D24, 7-1), which through a program stored in EPROM controls the functions of the card.

The Backplane Interface Circuit (BIC, U41, see A14, 7-1) is a custom gate array integrated circuit which controls the communication and handshaking with the I/O channel (backplane). The BIC is accessed by the Z-80B CPU as an I/O device for control information, and through Direct Memory Access (DMA) for data transfer to memory.

The Counter Timer Circuits (CTC, U51, U61, and U71, see E43, 7-1) divide the system clock to provide baud rate clocks and other necessary clocks for the MUX. They are accessed by the Z-80B CPU as I/O devices.

The Memory Interface Circuit (MIC, U54, see A32, 7-1) is a custom gate array integrated circuit which handles dynamic refresh and address multiplexing for the 64K bytes of dynamic RAM. The MIC also contains the DMA controller, provides interrupt vectors for backplane interrupts, decodes addresses and provides wait states for the slow EPROMs, and provides reset for the for the rest of the MUX card.

The Serial I/O circuits (SIOs, U43, U53, U63 and U73, see A42, 7-1) and their associated multiplexers, receivers, and drivers (see figure 7-1, sheet 5), provide serial data communication to the frontplane connector J2.

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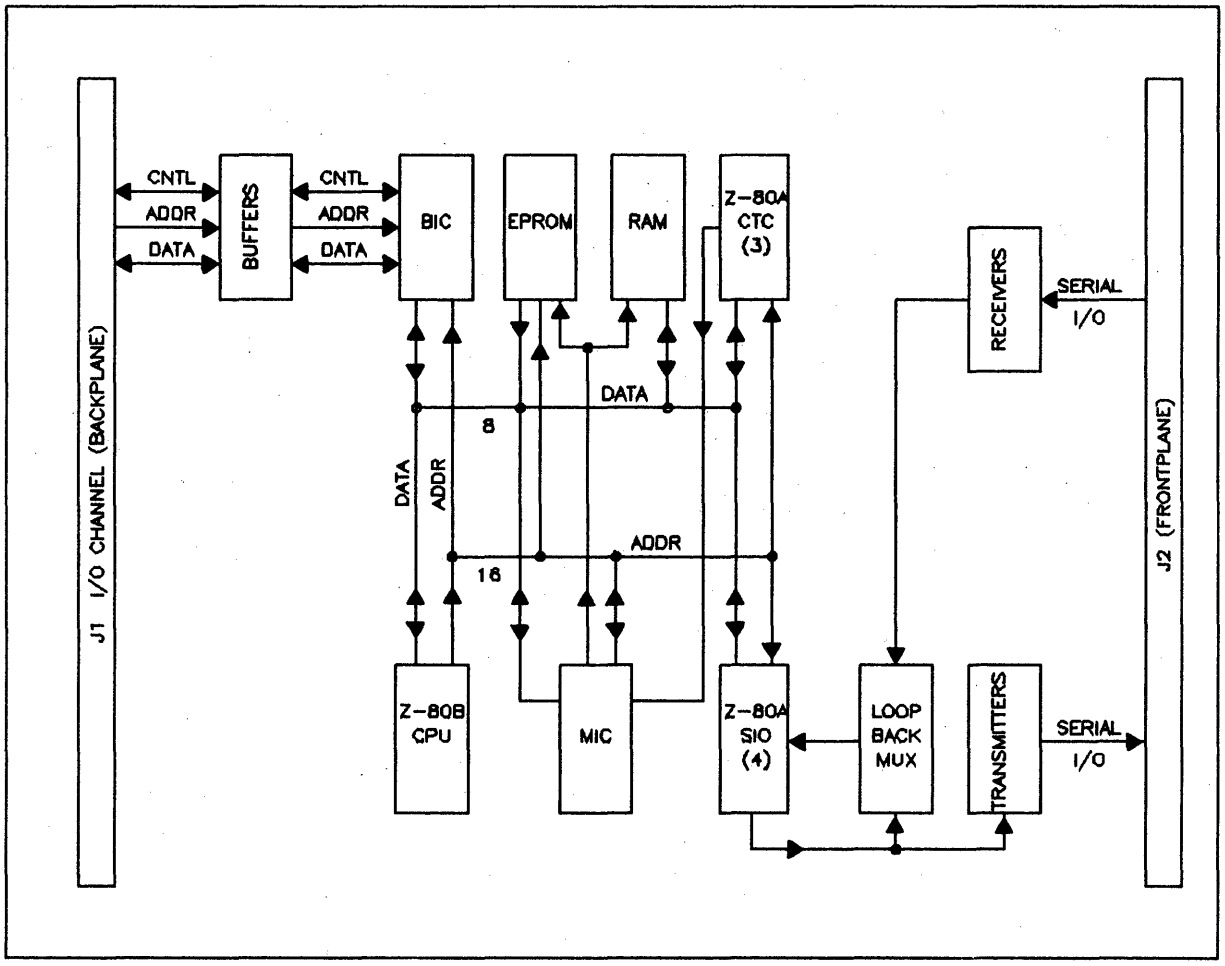


Figure 3-1. MUX Functional Block Diagram

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System Clocks

Three synchronized system clocks (1.8432 MHz, 3.6864 MHz, and 7.3728 MHz), all derived from the 14.7456 MHz clock signal CCLK+ (see A21, 7-1), perform the following functions:

1.8432 MHZ (PHI_CTC): Provides input to the CLK/TRG pins on the CTCs to generate baud rates and system timing intervals.

3.6864 MHz (PHI): Used to provide a system clock to the Z-80B CPU, the SIOs and MIC, and the CTCs.

7.3728 MHz (2_PHI): Drives the MIC.

Memory Address Space

The Z-80B CPU address space of 64K bytes is divided into several sections as shown in figure 3-2.

The two memory sockets, U64 and U74, are reserved for EPROMs and/or static RAMs. Socket U64 can be configured for 4K, 8K, or 16K byte EPROMs. Socket U74 can be configured for 4K byte EPROM, 8K byte EPROM, 2K byte static RAM, or 8K byte static RAM. Note, however, that when a 16K byte EPROM is installed in U64, socket U74 must be left empty to avoid bus contention.

The address space of U64 is from 0H to 3FFFH when this socket is configured for the 16K byte EPROM. The address space is from 0H to 1FFFH when the socket is configured for 4K or 8K byte EPROMs.

The address space of U74 is fixed between 2000H to 3FFFH.

The following types of EPROMs can be installed in socket U64:

4K by 8 (Intel 2732)
8K by 8 (Intel 2764)
16K by 8 (Intel 27128)

The following types of EPROMs and static RAMs can be installed in socket U74:

4K by 8 EPROM (Intel 2732)
8K by 8 EPROM (Intel 2764)
2K by 8 static RAM (Hitachi HM-6116)
8K by 8 static RAM (Hitachi HM-6164)

Memory Configuration jumper W1 is used to configure the two memory sockets. W1 contains nine jumper positions: A, B, C, D, E, F, G, H, and J. Positions A through D configure socket U64; positions E through H configure U74; and position J enables the WAIT- signal of the MIC to the Z-80B CPU. The MIC always asserts the WAIT- signal when the lowest 16K byte address is accessed. Position J should be closed (a jumper installed) when EPROMs/RAMs with access times greater than 250 nsec are used. The jumper is shown in Section II, figure 2-2.

NOTE

The jumpers are set at the factory and need no further adjustment unless the EPROMs or RAMS are changed.

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The 4K by 8 EPROMs and 2K by 8 static RAMs are 24-pin packages and are installed to the back of the sockets (pins 1, 2, 27, and 28 are not used).

Tables 3-1 and 3-2 show the settings of W1 for different types of EPROMs/RAMs.

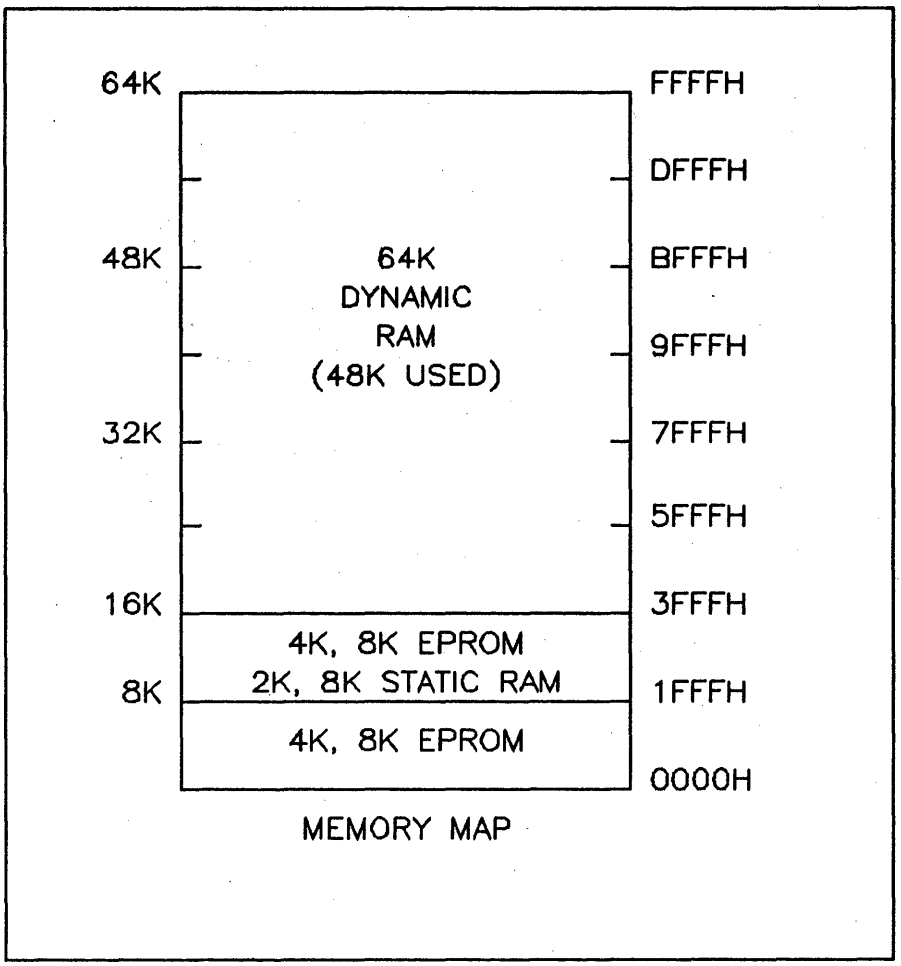


Figure 3-2. Memory Map

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Table 3-1. Memory Configuration Jumper (W1) Settings for Socket U64

ADDRESS SPACE	SETTINGS				SOCKET U64	COMMENTS
	A	B	C	D		
0000H-0FFFH (4K)	OPEN	CLOSED	CLOSED	OPEN	4K x 8 Intel 2732	
0000H-1FFFH (8K)	OPEN	CLOSED	DON'T CARE	OPEN	8K x 8 Intel 2764	
0000H 3FFFH (16K)	CLOSED	OPEN	OPEN	CLOSED	16K x 8 Intel 27128	Socket U74 must be empty

Table 3-2. Memory Configuration Jumper (W1) Settings for Socket U74

ADDRESS SPACE	SETTINGS				SOCKET U74	COMMENTS
	E	F	G	H		
2000H 2FFFH (4K)	DON'T CARE	OPEN	OPEN	CLOSED	4K x 8 Intel	4K byte EPROM configuration
2000H 3FFFH (8K)	CLOSED	OPEN	OPEN	CLOSED	8K x 8 Intel 2764	8K byte EPROM configuration
2000H 27FFH (2K)	OPEN	CLOSED	CLOSED	OPEN	2K x 8 Hitachi	2K byte static RAM configuration
2000H 3FFFH (8K)	OPEN	CLOSED	OPEN	CLOSED	8K x 8 Hitachi HM-6264	8K byte static RAM configuration

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I/O Address Space

The Z-80B CPU provides addressing capability for 256 distinct I/O port registers. The MUX card uses only 47 I/O port register addresses: 16 are reserved for the four Z-80 SIOs, 12 are reserved for the three Z-80 CTCs, 12 are reserved for the MIC, and seven are reserved for the BIC.

Table 3-3 shows the I/O addresses used by the card.

CAUTION

THE USE OF ANY OTHER ADDRESSES MAY CAUSE IMPROPER OPERATION.

Z-80B Microprocessor CPU

The Z-80B CPU (U33) is an MOS LSI microprocessor which operates from a single +5-volt supply, uses a single-phase clock, and has a typical instruction execution time of 1 microsecond. The data bus is eight bits wide, and the address bus is 16 bits wide. All CPU pins are TTL compatible.

The Z-80B CPU employs a register-based architecture which includes two sets of six general-purpose registers which can be used as individual 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter, and two index registers. The Z-80B CPU provides the intelligence for the MUX card to function as a preprocessor for the I/O devices, thus relieving the host computer of a considerable amount of processing.

The functions of the Z-80B CPU signals are shown in table 3-4.

Z-80 SIO/2 (Serial I/O Controller)

The MUX card uses four Z-80 SIO/2 controller circuits (U43, U53, U63, and U73, see A42, 7-1). The Z-80 SIO/2 is a programmable serial I/O controller with two independent full-duplex channels, each of which contains separate control and status lines. Each channel can be independently programmed. On the MUX card, each of the eight channels is used as a fully programmable asynchronous terminal controller.

Each SIO channel has two I/O addressable ports: one port for data transfer, and one for control information. Each control port has three read registers and eight write registers available for control information. The functions performed by the registers are shown in table 3-5.

Several of the SIO number 0 (U43) and SIO number 1 (U53) modem control output and modem status input signals are used for special functions, such as turning on the card's LED, sensing the diagnostic test hood, etc. These special functions are described in table 3-6.

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Table 3-3. I/O Address Space

I/O PORT FUNCTION	I/O ADDRESS LINES								I/O PORT ADDR
	7	6	5	4	3	2	1	0	
MIC Register 0	1	1	1	0	0	0	0	0	E0 H
MIC Register 1	1	1	1	0	0	0	0	1	E1 H
MIC Register 2	1	1	1	0	0	0	1	0	E2 H
MIC Register 3	1	1	1	0	0	0	1	1	E3 H
MIC Register 4	1	1	1	0	0	1	0	0	E4 H
MIC Register 5	1	1	1	0	0	1	0	1	E5 H
MIC Register 6	1	1	1	0	0	1	1	0	E6 H
MIC Register 7	1	1	1	0	0	1	1	1	E7 H
MIC Register 8	1	1	1	0	1	0	0	0	E8 H
MIC Register 9	1	1	1	0	1	0	0	1	E9 H
MIC Register 10	1	1	1	0	1	0	1	0	EA H
MIC Register 11	1	1	1	0	1	0	1	1	EB H
CTC 0: Channel 0	1	1	0	1	0	0	0	0	D0 H
CTC 0: Channel 1	1	1	0	1	0	0	0	1	D1 H
CTC 0: Channel 2	1	1	0	1	0	0	1	0	D2 H
CTC 0: Channel 3	1	1	0	1	0	0	1	1	D3 H
CTC 1: Channel 0	1	1	0	1	0	1	0	0	D4 H
CTC 1: Channel 1	1	1	0	1	0	1	0	1	D5 H
CTC 1: Channel 2	1	1	0	1	0	1	1	0	D6 H
CTC 1: Channel 3	1	1	0	1	0	1	1	1	D7 H
CTC 2: Channel 0	1	1	0	1	1	0	0	0	D8 H
CTC 2: Channel 1	1	1	0	1	1	0	0	1	D9 H
CTC 2: Channel 2	1	1	0	1	1	0	1	0	DA H
CTC 2: Channel 3	1	1	0	1	1	0	1	1	DB H
BIC Register 0	1	0	1	1	X	0	0	0	B0 H
BIC Register 1	1	0	1	1	X	0	0	1	B1 H
BIC Register 2	1	0	1	1	X	0	1	0	B2 H
BIC Register 3	1	0	1	1	X	0	1	1	B3 H
BIC Register 4	1	0	1	1	X	1	0	0	B4 H
BIC Register 5	1	0	1	1	X	1	0	1	B5 H
BIC Register 6	1	0	1	1	X	1	1	0	B6 H
BIC Register 7	1	0	1	1	X	1	1	1	B7 H
X = Don't care									

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Table 3-3. I/O Address Space (Continued)

I/O PORT FUNCTION	I/O ADDRESS LINES								I/O PORT ADDR
	7	6	5	4	3	2	1	0	
SIO 0: Channel A Data	0	1	1	1	0	0	0	0	70 H
SIO 0: Channel A Control	0	1	1	1	0	0	0	1	71 H
SIO 0: Channel B Data	0	1	1	1	0	0	1	0	72 H
SIO 0: Channel B Control	0	1	1	1	0	0	1	1	73 H
SIO 1: Channel A Data	0	1	1	1	0	1	0	0	74 H
SIO 1: Channel A Control	0	1	1	1	0	1	0	1	75 H
SIO 1: Channel B Data	0	1	1	1	0	1	1	0	76 H
SIO 1: Channel B Control	0	1	1	1	0	1	1	1	77 H
SIO 2: Channel A Data	0	1	1	1	1	0	0	0	78 H
SIO 2: Channel A Control	0	1	1	1	1	0	0	1	79 H
SIO 2: Channel B Data	0	1	1	1	1	0	1	0	7A H
SIO 2: Channel B Control	0	1	1	1	1	0	1	1	7B H
SIO 3: Channel A Data	0	1	1	1	1	1	0	0	7C H
SIO 3: Channel A Control	0	1	1	1	1	1	0	1	7D H
SIO 3: Channel B Data	0	1	1	1	1	1	1	0	7E H
SIO 3: Channel B Control	0	1	1	1	1	1	1	1	7F H

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Table 3-4. Z-80B CPU Signals

SIGNAL NAME	FUNCTION
A0 - A15 (Address Bus)	Tri-state output, active high. A0 - A15 are a 16-bit address bus (A0 is the least significant bit). This bus provides address capability for up to 64K of memory data exchanges, and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow direct addressing of up to 256 input or 256 output ports.
D0 - D7 (Data Bus)	Tri-state input/output, active high. D0 - D7 are an 8-bit bidirectional data bus used for data exchanges with memory and I/O devices.
M1- (Machine Cycle 1)	Output, active low. Indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
MREQ- (Memory Request)	Tri-state output, active low. Indicates that the address bus holds a valid address for a memory read or write.
IORQ- (Input/Output Request)	Tri-state output, active low. Indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write. IORQ- is also generated with M1- when an interrupt is being acknowledged. Interrupt acknowledge operations occur during M1 time, while I/O operations never occur during M1 time.

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Table 3-4. Z-80B CPU Signals (Continued)

SIGNAL NAME	FUNCTION
RD- (Read)	Tri-state output, active low. Indicates that the CPU wants to read data from memory or an I/O device. Memory or I/O device uses this signal to gate data onto the CPU data bus.
WR- (Write)	Tri-state output, active low. Indicates that the CPU data bus holds valid data for the addressed memory or I/O device.
RFSH- (Refresh)	Not used by the MUX card.
HALT-	Not used by the MUX card.
WAIT-	Input, active low. Indicates to the Z-80B CPU that the addressed memory or I/O devices are not ready for a data transfer. This signal allows memory or I/O devices of any speed to be synchronized to the Z-80B CPU.
INT- (Interrupt Request)	Input, active low. Generated by I/O devices. A request will be honored at the end of the current instruction if an internal Interrupt Enable flip-flop is enabled and if the BUSRQ- signal is not active.
NMI- (Non-Maskable Interrupt)	Not used by the MUX card. This signal is tied to +5V through a 3.3K ohm resistor.

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Table 3-4. Z-80B CPU Signals (Continued)

SIGNAL NAME	FUNCTION
RESET-	Input, active low. Forces the Z-80B CPU program counter to zero and initializes the Z-80B CPU.
BUSRQ- (Bus Request)	Input, active low. I/O devices and memory use this signal to request control of the CPU address bus, data bus, and tri-state control signals.
BUSAK- (Bus Acknowledge)	Output, active low. Asserted by the CPU to grant the requesting device control of the CPU address bus, data bus, and tri-state control signals.
CLK (Clock)	Single-phase CMOS level CPU clock input. Maximum input frequency is 4 MHz. This clock is driven at 3.6864 MHz (PHI signal) in the MUX card,

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Table 3-5. SIO Register Functions

WRITE REGISTERS	FUNCTION
WR0	Contains register pointers, CRC initialization information, initialization commands for operating modes
WR1	Transmit/receive interrupt and data transfer mode definition
WR2	Interrupt vector (channel B only)
WR3	Receive parameters and controls
WR4	Transmit/receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Synchronization character or SDLC address field
WR7	Synchronization character or SDLC flag
READ REGISTERS	FUNCTION
RR0	Transmit/recieve buffer status, interrupt status, and external status
RR1	Special receive condition status
RR2	Modified interrupt vector (channel B only)

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Table 3-6. SIO Special Functions

SIO NO.	SIO MNEMONIC	MUX CARD MNEMONIC	FUNCTION
0	RTSA- (OUTPUT)	EN_SED-	Active LOW. When asserted, the RS-232-C/RS-423-A single-ended drivers are enabled. Otherwise, the transmission lines (SDs) of the single-ended drivers are held in a MARK condition (negative voltage). To assert the EN_SED signal, a 1 must be written into bit 1 of SIO 0 channel A, register 5. On power up (reset), EN_SED is unasserted, i.e., the transmission lines (SDs) of the single-ended drivers are in a MARK condition.
0	DTRB- (OUTPUT)	EN_DD	Active HIGH. When asserted, the RS-422-A differential drivers are enabled. Otherwise, the transmission lines (SD(A), SD(B)) of the differential drivers are held in a high impedance state. To assert the EN_DD signal. a 0 must be written into bit 7 of SIO 0 channel B, register 5. On power up (reset), EN_DD is asserted. i.e., the differential drivers are enabled.

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Table 3-6. SIO Special Functions (Continued)

SIO NO.	SIO MNEMONIC	MUX CARD MNEMONIC	FUNCTION
0	RTSB- (OUTPUT)	LED	Active HIGH. When asserted, the MUX card LED is turned on.
1	RTSB- (OUTPUT)		To assert the LED signal, a 0 must be written into bit 1 of SIO 0 channel B, register 5 and SIO 1 channel B, register 5. On power up (reset), LED is asserted, i.e., the LED on the MUX card is on. Because a minimum of 6 mA is needed to turn on the LED, a 422 ohm resistor is used to supply the current. Two SIO modem control signals are used in parallel to shunt the current and turn off LED. The control circuit of the LED is shown in figure 3-3. In order to avoid a large current being sunk by only one of the two SIO control signals for a long period of time, thus damaging one of the SIOs, the time between programming the two SIO signals should be kept as short as possible.
0	DTRA- (OUTPUT)	LOOP-	Active LOW. When asserted, the self-test loop-back circuits are activated. The output of TXDs (transmit data) of each SIO is fed back to the input of RXDs (receive data) of the same channel, e.g., the data is sent from TXDA to RXDA of the same SIO. All eight channels are controlled by one loop-back circuit, therefore, it is not possible to loop back test only one channel while the other channels are still operating.

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Table 3-6. SIO Special Functions (Continued)

SIO NO.	SIO MNEMONIC	MUX CARD MNEMONIC	FUNCTION
			Both the single-ended and differential drivers should be disabled during the internal loop back test. This will avoid unintentional data transmission to the other systems through the frontplane drivers, thus causing unpredictable results. During the internal loop-back test, all the receivers are automatically disabled. Thus, the card is completely isolated from the frontplane receivers. To assert the LOOP signal, a 1 must be written into bit 7 of SIO 0 channel A, register 5. On power up (reset) LOOP- is unasserted, i.e., no loop back.
	CTSA- (INPUT)	HOOD_ON-	If the diagnostic hood is not installed, the HOOD_ON- signal is pulled to +5V by a 3.3K ohm resistor on the MUX card. If the diagnostic hood is installed, the state of HOOD_ON- is the complement of the state of the HLED- signal (i.e., 0-->1, 1-->0, HLED- --> HOOD-ON-). Figure 3-4 shows the circuit used to sense the diagnostic hood. This circuit is also used to turn the hood LED on and off. The state of the HOOD_ON- signal can be read from bit 5 of SIO 0 channel 1, register 0. A 0 indicates that HOOD_ON- is being pulled to +5V. A 1 indicates that HOOD_ON- is being pulled to ground. It is recommended that a string of 0s and 1s be written to the HLED- output, and read back through HOOD_ON- during self-test to verify that the diagnostic hood actually is installed.

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Table 3-6. SIO Special Functions (Continued)

SIO NO.	SIO MNEMONIC	MUX CARD MNEMONIC	FUNCTION
			On power up (reset), if the diagnostic hood is installed, the HOOD_ON- signal will be pulled to ground. If the diagnostic hood is not installed, the HOOD_ON- signal will be pulled to +5V.
0	RDYA- (OUTPUT)	DMA2-	Active LOW. DMA2- is tied to the IRQ2- input of the MIC. When RDYA- is programmed as RDYA- (READY-), it is a DMA handshake signal. To the MIC's DMA controller, DMA2- indicates that channel A of SIO 0 is ready to transfer data to or from memory. By using the MIC's DMA capability, channel A of SIO 0 (channel 0 of the MUX card) can support very high data rates. On power up (reset) DMA0- is floating.
0	RDYB- (OUTPUT)	DMA0-	Active LOW. DMA0- is tied to the IRQ0- input of the MIC. When RDYB- is programmed as RDYB- (READY-), it is a DMA handshake signal. To the MIC's DMA controller, DMA0- indicates that channel B of SIO 0 is ready to transfer data to or from memory. By using the MIC's DMA capability, channel B of SIO 0 (channel 1 of the MUX card) can support very high data rates. On power up (reset), DMA2- is floating.

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Table 3-6. SIO Special Functions (Continued)

SIO NO.	SIO MNEMONIC	MUX CARD MNEMONIC	FUNCTION
1	DTRB- (OUTPUT)	HLED-	Active LOW. When asserted, the LED on the diagnostic hood is on. To assert the HLED- signal, a 1 must be be written into bit 7 of SIO 1 channel B, register 5. On power up (reset), HLED- is unasserted, i.e., the LED on the diagnostic hood is off.

No modem control lines or modem status inputs are used.

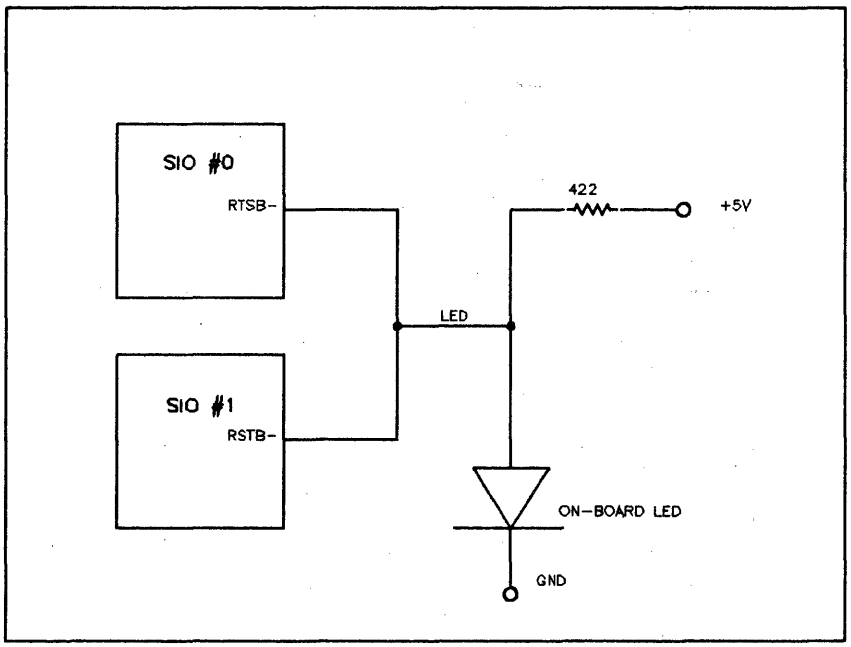


Figure 3-3. Control Circuit for the MUX Card LED

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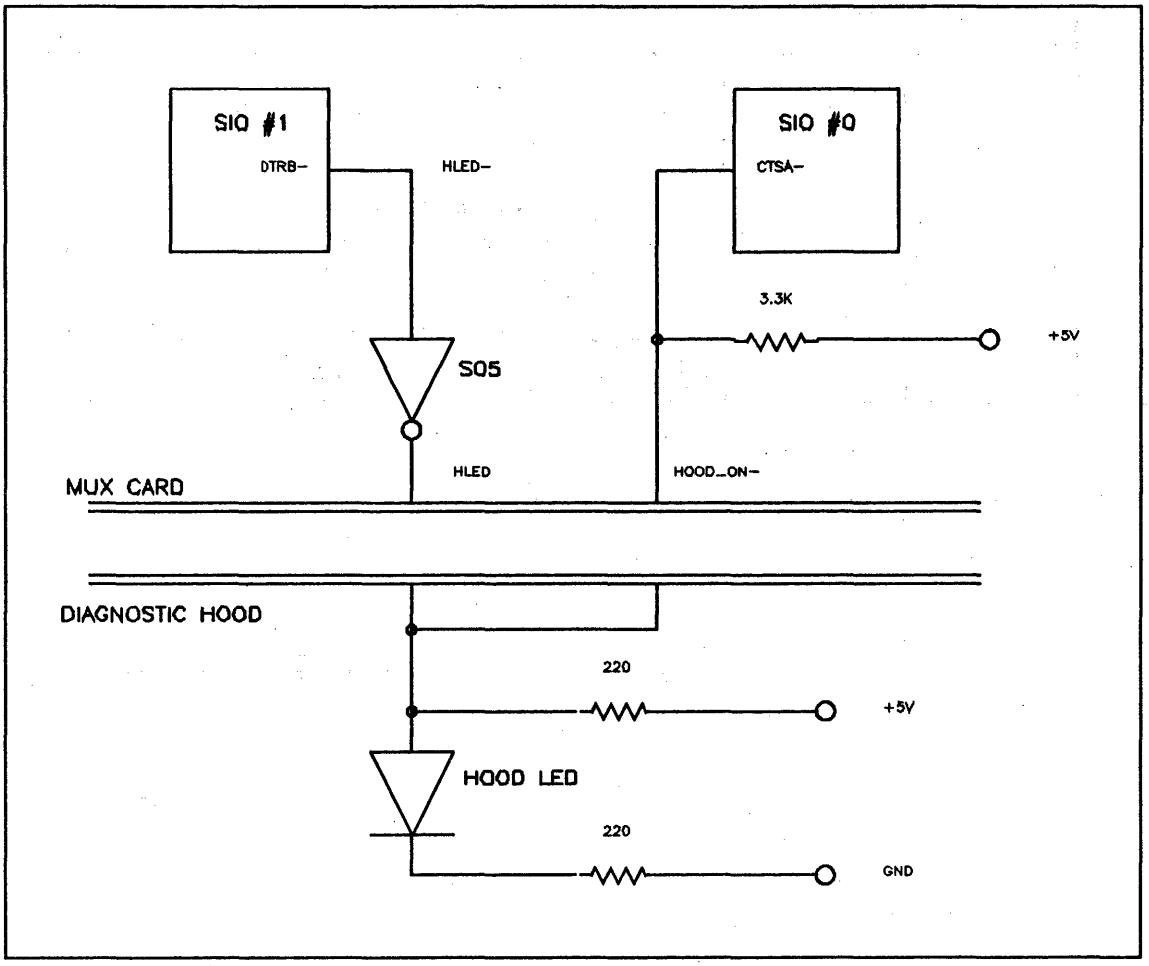


Figure 3-4. Diagnostic Hood LED Control Circuit and Hood Sense Circuit

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CTC (Counter Timer Circuit)

Three Z-80 CTC circuits (U51, U61, U71, see E43, 7-1) are used by the MUX card to provide baud rate and real-time clocks.

The Z-80 CTC circuit provides four independent counter/timer channels. Three of these timers can supply outputs for other devices; the fourth channel can only cause an interrupt to the Z-80B CPU.

Only the first CTC (CTC 0, U51) is tied to the MUX card's daisy-chain interrupt structure and is able to generate an interrupt to the Z-80B CPU. The fourth timer of CTC 0 is the real-time clock for the card's firmware.

CTC 1 (U61) and CTC 2 (U71) are not tied to the interrupt daisy chain, and they are not allowed to generate interrupts. These two CTCs are only used to generate baud rates.

The reason for eliminating CTC 1 and CTC 2 from the daisy-chain interrupt structure is to conform to the timing requirements of the Z-80B CPU during IACK and RETI cycles. See the "Wait State Circuit for Interrupt Acknowledge" paragraph for a timing analysis of the IACK and RETI cycles.

The inputs of all four clock triggers (CLK/TRG0 through CLK/TRG3) of all three CTCs are driven by the 1.8432 MHz clock (PHI_CTC clock, generated by U24, see A22, 7-1).

The functions of the CTC timer outputs are shown in table 3-7.

Note that the CTCs are I/O addressable ports to the Z-80B CPU; their addresses are defined in table 3-3.

Interfacing to the BIC

The Backplane Interface Circuit (BIC, see A14, 7-1) provides the half-duplex data path to the I/O channel (backplane). As used by the MUX card, the BIC is addressed as an I/O port by the Z-80B CPU (the same as the Z-80 SIO and CTC circuits). In other words, to read or write from the BIC registers, an IN or OUT instruction is executed to the I/O address of that register. The address space of the BIC is described in table 3-3.

Data can also be transferred between the BIC and memory directly under control of DMA channel B of the Memory Interface Circuit (MIC).

The BIC is not directly connected to the interrupt daisy chain structure of the MUX card. Instead, the BIC's BINT- (interrupt output, see E14, 7-1) signal is connected to the MIC's IINT- (interrupt input, see C31,7-1) signal. When the MIC is programmed for external interrupt (from the BIC), the MIC will generate an interrupt for the BIC. The MIC also provides an interrupt vector for the BIC when the Z-80B CPU acknowledges.

Descriptions of the BIC signals are shown in table 3-8.

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Table 3-7. CTC Timer Outputs

CTC NO.	CTC CH.	TIMER OUTPUT MNEMONIC	DRIVEN DEVICE INPUT MNEMONIC	FUNCTION
0	0	IRQH	IRQH of MIC	Request hold-off for DMA
0	1	BRG1	SIO 0 RXCB- & TXCB-	MUX card channel 1 baud-rate clock
0	2	BRG0	SIO 0 RXCA- & TXCA-	MUX card channel 0 baud-rate clock
0	3	INTERNAL	Cause zero count interrupt to Z-80B CPU	Real-time clock for firmware
1	0	BRG2	SIO 1 RXCA- & TXCA-	MUX card channel 2 baud-rate clock
1	1	BRG3	SIO 1 RXCB- & TXCB-	MUX card channel 3 baud-rate clock
1	2	BRG4	SIO 2 RXCA- & TXCA-	MUX card channel 4 baud-rate clock
1	3	Not available		Counter value can be read (polled) by Z-80B CPU

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Table 3-7. CTC Timer Outputs (Continued)

CTC NO.	CTC CH.	TIMER OUTPUT MNEMONIC	DRIVEN DEVICE INPUT MNEMONIC	FUNCTION
2	0	BRG5	SIO 2 RXCB- & TXCB-	MUX card channel 5 baud-rate clock
2	1	BRG6	SIO 3 RXCA- & TXCA-	MUX card channel 6 baud-rate clock
2	2	BRG7	SIO 3 RXCB- & TXCB-	MUX card channel 7 baud-rate clock
2	3	Not available		Counter value can be read (polled) by Z-80B CPU

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Table 3-8. BIC Chip Pin Connections

PIN NO.	SIGNAL MNEMONIC	BIC MNEMONIC	DESCRIPTION
1	D0	D0	Data Bus, Bit 0
2	D2	D2	Data Bus, Bit 2
3	D4	D4	Data Bus, Bit 4
4	D6	D6	Data Bus, Bit 6
5	END-	END-	Indicates end of data read or write
6	A0	A0	Register Address, Bit 0
7	A1	A2	Register Address, Bit 2
8	WR-	DS0-	Z-80B Write
9	RDY-	RDY-	Asserted by BIC when ready for data transfer
10	GND	AS-	Not used
11	---	DTACK-	Not used
12	BINT-	INT-	BIC Interrupt
13	NMI	NMI	Non-Maskable Interrupt
14	IFC	IFC	Interface Clear
15	POLL-	POLL-	Poll
16	SYNC_MYAD-	SYNC_MYAD-	In conjunction with DE, determines data bus drivers mode of operation
17	DOUT	DOUT	Data Out, specifies data bus direction
18	BP0	BP0	Bus Primitive, Bit 0. With BP1, specifies bus primitive operation
19	UAD	UAD	Unary Address, latches BIC channel address after a PPON or IFC
20	AD0	AD0	Address Bus, Bit 0
21	AD2	AD2	Address Bus, Bit 2
22	CEND	CEND	Channel End
23	DB0-	BIOD0-	Backplane I/O Data, Bit 0
24	DB1-	BIOD1-	Backplane I/O Data, Bit 1
25	DB3-	BIOD3-	Backplane I/O Data, Bit 3
26	DB5-	BIOD5-	Backplane I/O Data, Bit 5
27	DB7-	BIOD7-	Backplane I/O Data, Bit 7
28	DB9-	BIOD9-	Backplane I/O Data, Bit 9
29	DB10-	BIOD10-	Backplane I/O Data, Bit 10
30	DB11-	BIOD11-	Backplane I/O Data, Bit 11
31	DB13-	BIOD13-	Backplane I/O Data, Bit 13
32	DB15-	BIOD15-	Backplane I/O Data, Bit 15
33	BR	BR	Burst Request, indicates at least one more transfer after current one

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Table 3-8. BIC Chip Pin Connections (Continued)

PIN NO.	SIGNAL MNEMONIC	BIC MNEMONIC	DESCRIPTION
34	DBYT	DBYT	Device Byte, indicates that the current 16-bit transfer ends with an odd byte
35	IOSB	IOSB	I/O Strobe
36	D1	D1	Data Bus, Bit 1
37	D3	D3	Data Bus, Bit 3
38	D5	D5	Data Bus, Bit 5
39	D7	D7	Data Bus, Bit 7
40	GND	GND	Ground
41	A1	A1	Register Address, Bit 1
42	SEL-	CHSEL-	BIC Select, enables the BIC to to read or write
43	RD-	DS1-	Z-80B Read
44	DTR-	DTR-	Data Transfer Request
45	RESET-	RST-	Reset
46	ARQ	ARQ	Attention Request
47	+5	VCC	+5 V
48	SYNC	SYNC	Synchronize, signals that an addressed bus operation is to occur
49	MYAD	MYAD	My Address
50	BP1	BP1	Bus Primitive, Bit 1. With BP0, specifies bus primitive operation
51	AD1	AD1	Address Bus, Bit 1
52	AD3	AD3	Address Bus, Bit 3
53	CBYT	CBYT	Channel Byte, indicates that the current 16-bit transfer ends with an odd byte
54	GND	GND	Ground
55	DB2-	BIOD2-	Backplane I/O Data, Bit 2
56	DB4-	BIOD4-	Backplane I/O Data, Bit 4
57	DB7-	BIOD7-	Backplane I/O Data, Bit 7
58	DB8-	BIOD8-	Backplane I/O Data, Bit 8
59	DB12-	BIOD12-	Backplane I/O Data, Bit 12
60	DB14-	BIOD14-	Backplane I/O Data, Bit 14
61	---		Not used
62	DEND	DEND	Device End, indicates end of transfer
63	DE	DE	Direction Enable
64	PPON-	PPON-	Primary Power On

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Memory Interface Circuit (MIC)

The Memory Interface Circuit (MIC, see A31, 7-1) provides the following functions:

* Controls the RAM and EPROM memory circuits
* Provides two programmable DMA channels (memory to I/O channel only)
* Vectors backplane interrupts for the BIC

The MIC contains twelve programmable 8-bit registers (register 0 functions as a 3-bit register, five bits are not used) for configuring the DMA channels and the interrupt vectors. Four registers (registers 1, 2, 6, and 7) are write only, the other eight registers have read/write capability.

The registers and their functions are described on the following pages. Note that all register bits are positive true logic functions unless otherwise specified.

Register 0 - MIC Configuration. The functions of the bits of register 0 (read/write) are as follows:

Bit 7 = DM2 -	Selects whether IRQ1- or IRQ2- is the DMA request sensed by DMA channel B. If DM2 = 1, IRQ2- is sensed If DM2 = 0, IRQ1- is sensed
Bit 6 = XNT -	External Interrupt Enable. When XNT = 1, the IINT- line will be sensed as an interrupt by the MIC interrupt control.
Bit 5 = DEND -	When this bit = 1, the DEND- signal (pin 48 of the MIC) is disabled (should be 0).

Bits 4 through 0 are not used.

NOTE

All of the above bits are zeroed on reset.

Register 1 - DMA B Upper Byte of Memory Address. Register 1 (write only) contains the upper byte of the memory address used as a source/destination for DMA channel B. Note that this register is not affected by reset.

Register 2 - DMA Lower Byte of Memory Address. Register 2 (write only) contains the lower byte of the memory address used as a source/destination for DMA channel B. Note that this register is not affected by reset.

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Register 3 - DMA B Configuration. The functions of the bits of register 3 (read/write) are as follows:

Bit 7 = DMA channel B enable bit

1 = enable
0 = disable

Bit 6 = Transfer to/from memory

1 = to memory
0 = from memory

Bit 5 = Direction of memory address counter

1 = decrement counter
0 = increment counter

Bit 4 = DMA channel B interrupt enable

1 = enable interrupt
0 = disable interrupt

Bit 3
Bit 2 Upper four bits of transfer byte count for DMA B
Bit 1
Bit 0

NOTE

Bits 4 through 7 are zeroed on reset. Bits 0 through 3 are not affected by reset.

Register 4 - Lower Byte of Transfer Byte Count - Channel B. Register 4 (read/write) contains the lower byte of the transfer byte count for channel B. This register is not affected by reset.

Register 5 - DMA B I/O Port Address. Register 5 (read/write) contains the DMA B I/O port address. This register is not affected by reset.

Register 6 - DMA A Upper Byte of Memory Address. Register 6 (write only) contains the upper byte of the memory address used as a source/destination for channel A. Note that this register is not affected by reset.

Register 7 - DMA A Lower Byte of Memory Address. Register 7 (write only) contains the lower byte of the memory address used as a source/destination for channel A. Note that this register is not affected by reset.

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Register 8 - DMA A Configuration. The functions of the bits of register 8 (read/write) are as follows:

Bit 7 = DMA channel A enable bit

1 = enable
0 = disable

Bit 6 = Transfer to/from memory

1 = to memory
0 = from memory

Bit 5 = Direction of memory address counter

1 = decrement counter
0 = increment counter

Bit 4 = DMA channel A interrupt enable

1 = enable interrupt
0 = disable interrupt

Bit 3
Bit 2 Upper four bits of transfer byte count for DMA A
Bit 1
Bit 0

NOTE

Bits 4 through 7 are zeroed on reset. Bits 0 through 3 are not affected by reset.

Register 9 - Lower Byte of Transfer Byte Count - Channel A. Register 9 (read/write) contains the lower byte of the transfer byte count for channel A. This register is not affected by reset.

Register A - DMA A I/O Port Address. Register A (read/write) contains the DMA A I/O port address. This register is not affected by reset.

Register B - Interrupt Vector. Register B (read/write) contains interrupt vector information. Bits 3 through 7 of register B contain bits 3 through 7 of the interrupt vector address. Bits 1 and 2 of the register are modified automatically by the highest priority device requesting interrupt service. Table 3-9 shows how bits 1 and 2 are determined based on the interrupts sensed at interrupt acknowledge time. Bit 0 is always a logical zero. Note that this register is not affected by reset.

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Table 3-9. Interrupt Vector Bits

DMA A	DMA B	IINT	VECTOR BITS 2	1	0
1	X	X	0	0	0
0	1	X	0	1	0
0	0	1	1	0	0
X = Don't care					

Priority Interrupt Structure

All I/O devices connected to the MUX card can cause interrupts. These interrupts are prioritized according to the standard Z-80 priority chain. There is no non-maskable interrupt used on the MUX card. Interrupts from the host computer (via the BIC) to the MUX are prioritized within the MIC circuit. The MUX card interrupt priority structure is as follows:

```
Highest Priority  -  SIO/2 Number 0, Channel A
                  -  SIO/2 Number 0, Channel B
                  -  SIO/2 Number 1, Channel A
                  -  SIO/2 Number 1, Channel B
                  -  SIO/2 Number 2, Channel A
                  -  SIO/2 Number 2, Channel B
                  -  SIO/2 Number 3, Channel A
                  -  SIO/2 Number 3, Channel B
                  -  BIC
                  -  CTC Number 0, Channel 0
                  -  MIC DMA Channel A
Lowest Priority   -  MIC DMA Channel B
```

Wait State Circuits for Interrupt Acknowledge

On the MUX card, six devices (SIO 0, SIO 1, SIO 2, SIO 3, CTC 0, and MIC) are connected in a daisy chain interrupt structure. Due to the delay of the long daisy chain, a wait state must be added during an interrupt acknowledge cycle in order to conform to the timing requirements of the Z-80B CPU.

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Interrupt acknowledge to the devices listed above is accomplished by the Z-80B CPU executing a special M1- cycle (see D24, 7-1) in which IORQ- goes active instead of MREQ- and RD-. Whenever M1- goes active, all devices are inhibited from changing their interrupt status. This allows time for IEO- to propagate through the other devices in the chain before IORQ- goes active. As soon as IORQ- and M1- go active, the device that has its IEI signal high, and an interrupt pending, gates an 8-bit interrupt vector onto the data bus.

In order to guarantee that the MUX card's long daisy chain is stable before IORQ- is active, IORQ- is delayed by at least half of a T-state (see figure 3-6 for T-state timing). With this extended T-state, the total time between M1- going active and IORQ- going active is at least 710 nsec, which is long enough for the daisy chain to become stable.

Figure 3-5 shows the MUX card's wait circuit for an interrupt acknowledge cycle. The ZIORQ- and M1- signals are the inputs from the Z-80B CPU. IORQ- and WAIT- are the outputs from the wait circuit. IORQ- drives all the devices (SIOs, MIC, and CTC 0), WAIT- drives the input of a 74LS08 AND gate. The output of the AND gate drives the WAIT- input of the Z-80B CPU. Except during an interrupt acknowledge cycle, IORQ- always follows ZIORQ- of the Z-80B CPU with a maximum of 22 nsec delay. During an interrupt acknowledge cycle, IORQ- is asserted half a T-state after ZIORQ-, at the rising edge of the following T-state. At the same time, WAIT- is also asserted for one full T-state to add an additional wait state. IORQ- follows ZIORQ- on the rising edge (de-asserting edge).

The timing diagram of the wait state circuit is shown in figure 3-6.

DIAGNOSTIC HOOD FOR EXTERNAL LOOP BACK

A diagnostic test hood (part number 0950-1659) can be ordered and used to test the RS-232-C/RS-423-A single-ended drivers, the RS-422-A differential drivers, and the receivers. One diode and one resistor are used for each channel of the MUX card. A total of eight diodes and eight resistors are needed to test all eight channels of the MUX. A schematic diagram of one channel of the test hood, with the drivers and receivers for one MUX channel, is shown in figure 3-7.

When the single-ended drivers are being tested, the EN_SED- signal (RTSA- of SIO 0, see B42, figure 7-1) must be asserted (LOW level), and the EN_DD signal (DTRB- of SIO 0) must be unasserted (LOW level).

When the differential drivers are being tested, the EN_DD signal (DTRB- of SIO 0) must be asserted (HIGH level), and the EN_SED- signal (RTSA- of SIO 0) must be unasserted (HIGH level).

Using the diagnostic hood, the data sent from the transmit channels will loop back to the corresponding receive channels through the enabled drivers. For example, channel 1 loops back to channel 1, channel 2 loops back to channel 2, and so forth.

The diagnostic hood has an LED to indicate that the self-test firmware detected the presence of the hood. The control circuit for the hood LED and hood sensing is shown in figure 3-4.

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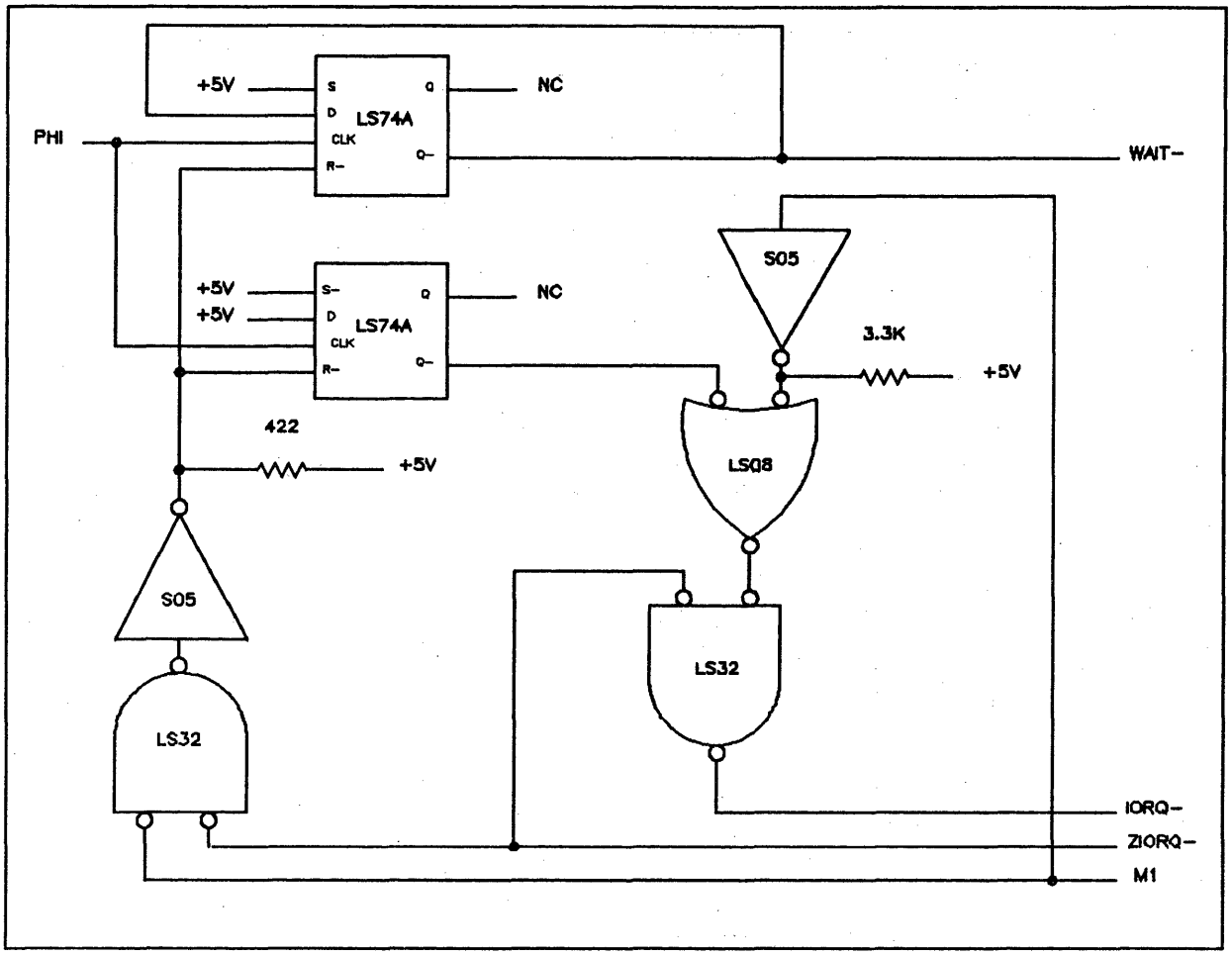


Figure 3-5. Wait State Circuit Schematic Diagram

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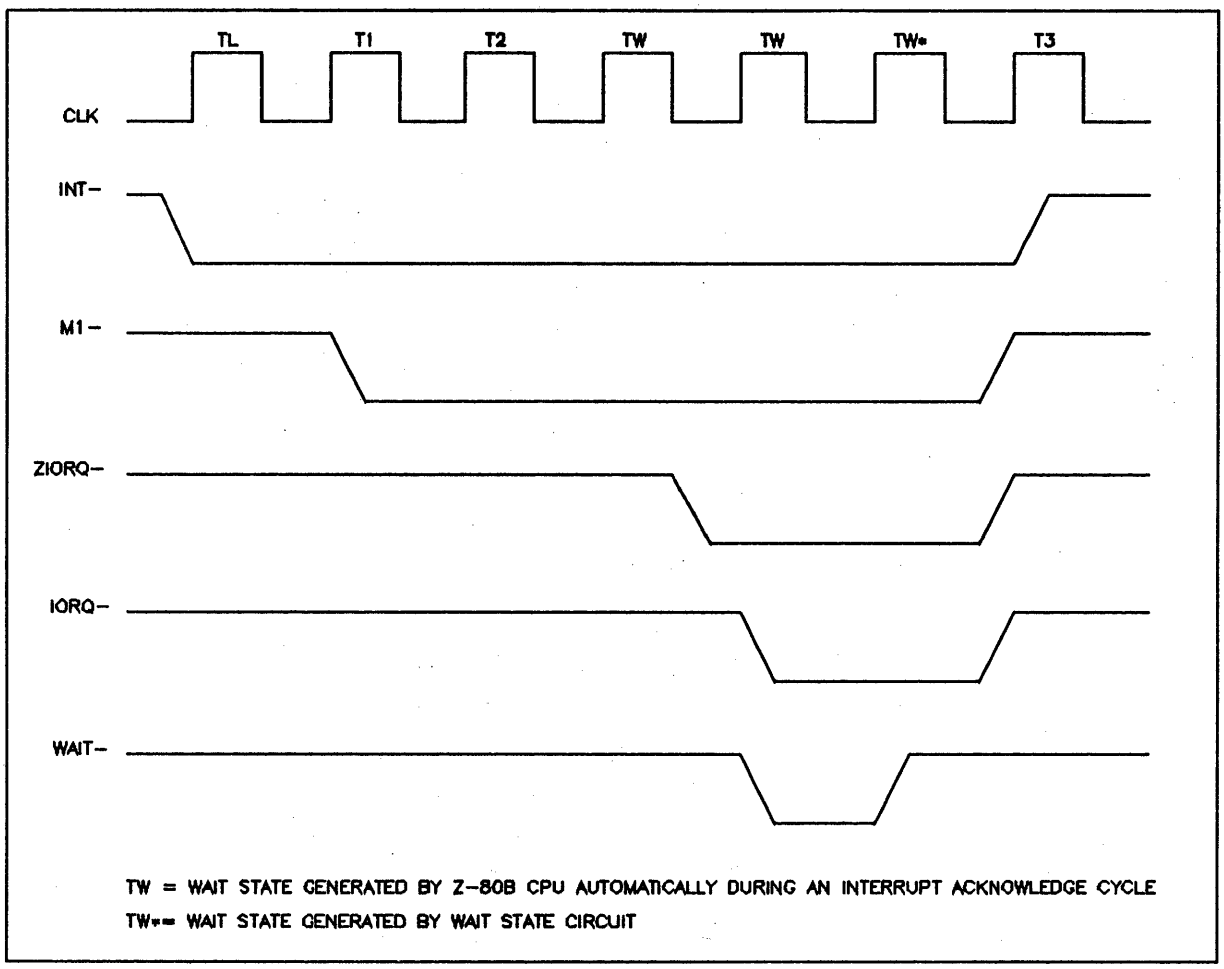


Figure 3-6. Wait State Circuit Timing Diagram

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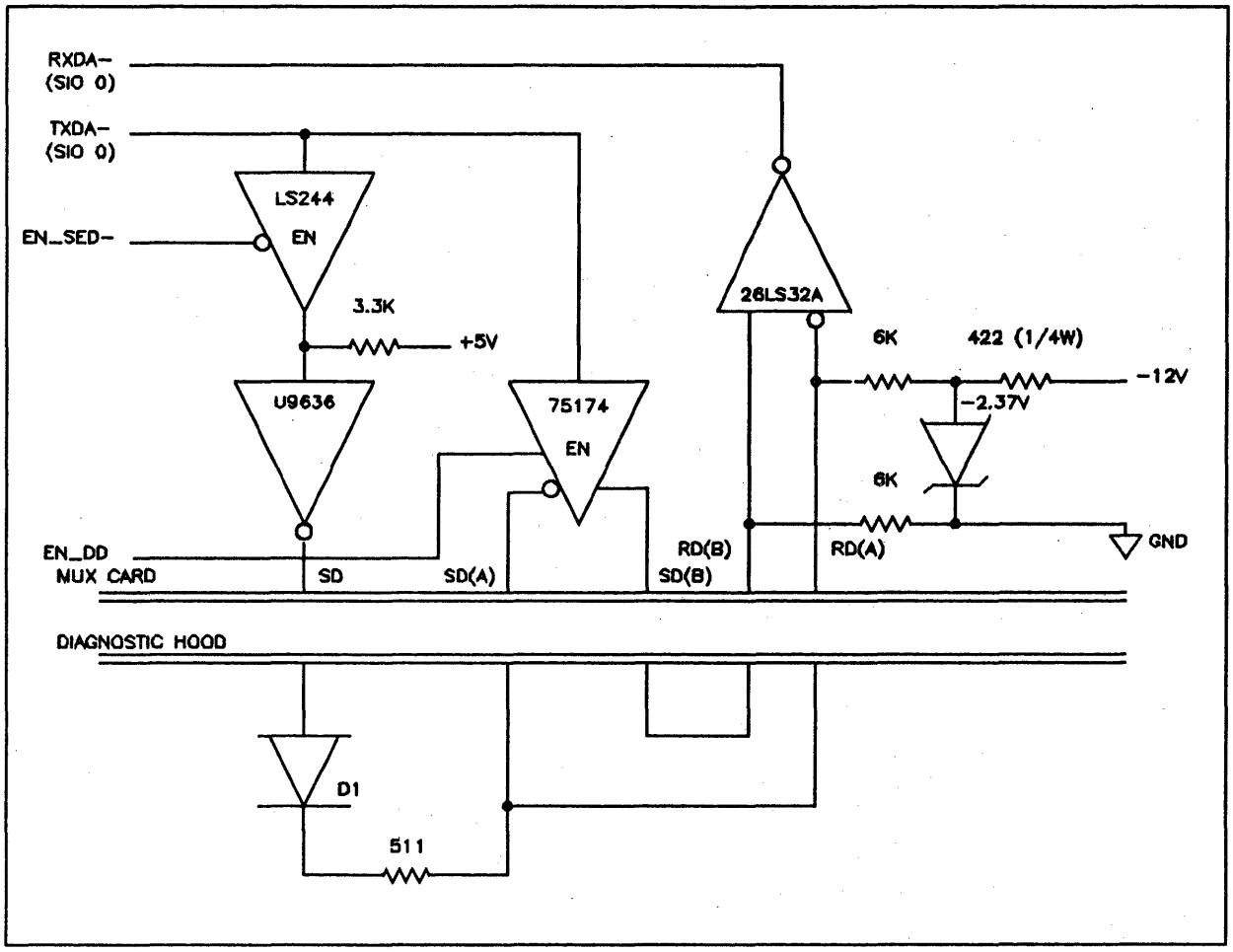


Figure 3-7. Diagnostic Test Hood Schematic Diagram

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When the single-ended drivers are enabled and the differential drivers are disabled, the receivers will be driven by the single-ended drivers. When a SPACE (>= +4 volts) is sent through SD, the D1 diode in the hood will be forward biased. The transmitted signal will pass through the hood to the receiver input (with a 0.7 volt drop). When a MARK (<= -4 volts) is sent through SD, the D1 diode will be reverse biased. The transmitted signal will be blocked. However, the MUX card fail-safe circuit will pull the input of the receiver (RD(A)) low, so that the transmitted data will be interpreted correctly. Because the differential drivers are disabled, the outputs of these drivers are in a high-impedance state, and they will not affect the single-ended drivers.

When the single-ended drivers are disabled, all the SD lines will be in a MARK condition (<= -4 volts) and the D1 diodes will be reverse biased. The reverse-biased D1 will isolate the single-ended drivers and let the differential drivers drive the receivers.

The 511-ohm resistors are used to protect the U9636 single-ended drivers during the power-up transient. During the power-up transient, it is possible to have the outputs of the U9836s at the HIGH state and the outputs of the 75174s at the LOW state. If the diagnostic test hood has been connected to the card during this period, D1 will be forward biased. Because the 75174s can sink a large amount of current, the 511 ohm resistors are used to limit the current that can be sourced by the U9636 drivers and protect them from being damaged.

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PROGRAMMING

SECTION IV

The HP 27130A Eight-Channel Multiplexer (MUX) is used for interfacing up to eight EIA RS-232-C/RS-422-A/RS-423-A devices to Hewlett-Packard computer systems using the CHANNEL I/O standard backplane. Many of the firmware features of the MUX are programmable by the user. In addition, each option can be enabled or disabled programmatically. The MUX firmware provides all necessary line protocol for the support of most terminals.

MUX PROGRAMMABLE FEATURES

Features and options of the MUX which can be controlled programmatically are as follows:

* Number of Data Bits Per Character (7 or 8)
* Number of Stop Bits (1 or 2)
* Transmission Mode (asynchronous only in simplex, half-duplex, full-duplex, or echoplex)
* Parity (none, odd, even, 0, or 1)
* Automatic Detection of Baud Rate by Command (baud rate defaults to 9600)
* Baud rate is programmable from 110 baud to 19,200 baud
* Break Detection
* Edit Mode Option to Process Backspace and Line Deletion
* Backspace Character
* Line Delete Character
* Single Text Terminator Character(s)
* Host ENQ/ACK Handshaking to Device, with a programmable timeout and a programmable pacing counter
* Interrupt on Handshake Timeout

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* Type Ahead Mode
* Automatic Output Separator(s) Appendage for Transmitted Text
* In Echoplex, the MUX may be enabled to echo a CR-LF for a Programmable Single Text Terminator

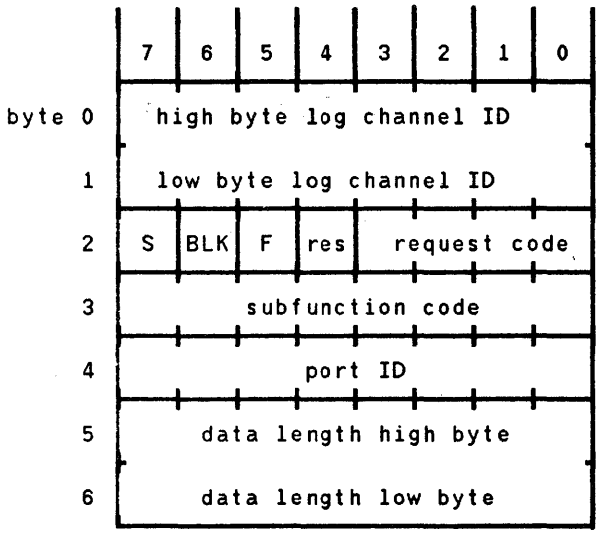
TRANSACTIONS

Each transfer between the MUX and the host computer is called a "transaction", and occurs over the I/O channel. Each transaction represents a single read or write (data, status, etc.)

Each read or write is preceded by a Connect Logical Channel (CLC) request block from the host computer. The CLC request is in response to an SRQ signal, requesting the next order, from the MUX.

CONNECT LOGICAL CHANNEL (CLC) REQUEST FORMAT

The Connect Logical Channel (CLC) request block has the following format:



where

log channel ID

Assigned by the host for each transaction. The card firmware will keep the ID with each transaction until it is completed.

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S bit

Used by all non-blocked read device data requests and by the last block of the blocked read device data request. If the S bit is set, any remaining data in the current read record will be available for the next read request. If the S bit is clear, any data remaining in the current record will be discarded after the read is completed.

BLK

0 = non-blocked data transfer

1 = blocked data transfer

F

Flush data before processing this request. Any data residing in the indicated port's receive buffer is flushed before a read is begun (RDD requests only).

request code

0 = Reserved

1 = Read Device Data (RDD)

2 = Write Device Data (WDD)

3 = Not used

4 = Read Card Information (RCI)

5 = Write Card Configuration data (WCC)

6 = Control Card (CC)

7 = Not used

8-15 = Reserved

subfunction code

The content of this field is dependent on the type of the request.

port ID

The port ID is the logical port to which the request is directed. The mapping of logical port to physical port (0 - 7) is defaulted as a one-to-one mapping (PID 0 = port 0, etc.) but can be reconfigured using WCC, SF 34 (Write Card Configuration , Subfunction 34).

A logical port is used to provide compatibility with other CHANNEL I/O cards which may not have a simple device addressing mode.

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data length

Required for all read or write requests. All other requests should contain zeros.

CAPABILITIES

The following paragraphs provide detailed descriptions of the MUX's capabilities.

Receive Character Processing

The receive interrupt processor is capable of offloading many of the functions usually found in the host computer. This allows more time for the host CPU to perform other functions. The order of processing each received character is as follows:

1. If the received character has an error condition, and the "ignore parity error" bit is set in the Write Card Configuration, Subfunction 13 (WCC, SF 13), the parity error condition is cleared.

2. It there still is an error after step 1, and the "ignore all errors" bit is set in WCC, SF 13, the character is discarded. Otherwise, the current receive record is marked "bad". If enabled by WCC, SF 31, the record is then made available for the host, or a substitute character is fetched to replace the bad one and processing continues.

3. If the character is a handshake character, and handshaking is enabled, check the character for an ACK if ENQ/ACK is enabled, or for XON or XOFF if XON/XOFF is enabled. If so, process the character and discard it.

4. If the character is a signal character, and signal character detection is enabled, generate the appropriate event and discard the character.

5. If the character is quotable, and quoting is enabled, check the previous character for the quoting character. If the quoting character is present, replace it with the received character, and skip the edit and terminating condition checks.

6. If the character is an edit character, and edit mode is enabled, check for backspace or line delete, and perform the edit function.

7. If the character is a single text terminator, and single text termination is enabled, terminate the record and make it available to the host. If termination stripping is disabled, add the character to the buffer.

If the received character does not match any of the conditions described in steps 1 through 7, the character now is added to the current record.

8. If the end-on-count option is enabled, a check against the end-on-count is made. If the count is exhausted, the current record is terminated with an "end-on-count" termination.

9. If the internal card end-on-count is reached, terminate the record.

10. If the Alert 1 mode is enabled, generate an event to notify the host that at least one character has been received, if this has not already been done for this record.

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The order of processing the received character listed in steps 1 through 10 is the precedence implemented by the MUX firmware. Only one type of termination is assigned to each receive record.

The following descriptions frequently use the term "current receive record". The "current receive record" is the currently active record that can receive data from the device. If the current receive record does not exist, a record is created and the character, or the termination condition, is added to the record.

Note that a condition may cause the generation of a record which contains no "data" (for example, Carriage Return (CR) is not data, it is line protocol). You should be aware that the text record may be of zero length. In this case, you will be notified of the condition that caused the termination in the request status block.

The host may post a read request to the card even when no receive data is available. The card will suspend the read request until a record is received. If no read request is pending, and the card has a record available for the host, an asynchronous event, if enabled, is sent to the host to start the read. See the paragraph "Asynchronous Event" for additional details.

Receive Error Conditions

The firmware will terminate the current receive record when any error condition is sensed. If the "Do Not Terminate On Error" option is set, the firmware will not terminate the record. Instead, a user specified replacement character will replace the bad incoming character, see the "Additional Options" paragraph for further details.

The firmware also has the option of ignoring parity errors (process the character as if the error did not exist), or to discard characters with any kind of error.

These errors include parity error, framing error, and data overrun.

Signal Character

When the Signal Character option is enabled, every received character is checked for a match to one of the four signal characters, which are programmable by the user. If a match occurs, the firmware will generate the appropriate status event.

The signal character is very similar to the use of the BREAK key on a terminal, except that you can specify any character for this function. For example, the EM character (control-Y) may be used to interrupt a program from a terminal.

If fewer than four signal characters are desired, the unused characters should be programmed as duplicates of a lower-numbered used character. The search for a matching signal character proceeds from Signal 1 to 4.

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Edit Mode

Edit mode may be enabled by setting the Edit Mode option in Write Card Configuration (WCC), Subfunction (SF) 1. Edit mode is disabled by clearing the Edit Mode option, or toggled by setting the "toggle edit" bit in the Read Device data request (RQ 1), subfunction bit 5. If toggled, the change in state is for the duration of the request only, and will revert back to the static definition (per WCC, SF 1) when the request completes.

When working at a terminal connected to the MUX card, several types of editing capabilities are available. The first is backspace to delete the previously typed character (several backspace modes are available), and another is to delete the current line. An additional "quoting mode" (explained in the "Additional Options" paragraph) allows the insertion of editing characters in the text buffer without causing any other action.

Note that editing can be performed on the current frontplane buffer *only*. Once a buffer has been terminated for any reason, it cannot be modified by the card.

Backspace. The firmware uses the character BS (hex 08) to indicate a backspace function. This character is generated by pressing the BACK SPACE key or by typing CNTL-H. In addition, you can programmatically change the backspace character to any desired character by using the WCC, SF 6.

Three options are available to indicate that a backspace has occurred when the card is in echoplex mode. The first option is "backspace echo". This option echoes a backslash character (5C hex), followed by the character that was deleted from the input buffer.

The second option is "backspace overwrite". This option is very useful for CRT-type terminals. The firmware will echo a backspace - space - backspace sequence for each BACK SPACE key hit, erasing the character from the screen.

The third option is "backspace only". This option echoes only the backspace character to move the cursor under the deleted character.

The Backspace option is programmable by using WCC, SF 8. Only one backspace option may be enabled at any time.

If you have used backspace to delete the current line, any further backspace will cause no action.

Line Deletion. The firmware uses the character DEL (hex 7F) as the line deletion character. As with the backspace character, you can program the line deletion character by using the WCC, SF 7.

The line deletion character causes the card to delete the current line, if any. If the card is in echoplex mode, it will write one backslash, then do a carriage-return/linefeed to indicate that the buffer was deleted.

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Software Handshake with the Device

Three software handshakes are available between the host and the device:

1. Host controlled ENQ/ACK handshake
2. Device controlled X-ON/X-OFF handshake
3. Host controlled X-ON/X-OFF handshake

Besides enabling the individual software handshake defined above by using the WCC, SF 9, you must also enable the Software Handshake option in WCC, SF 1. Handshakes may be toggled on or off for the duration of the request by setting the "toggle handshake" bit in the Read Device Data request (RQ 1) subfunction field. The handshakes will revert to the previous definition when the request completes.

The characters defined for the ENQ, ACK, X-ON, and X-OFF characters are programmable by using the WCC, SF 22, SF 23, and SF 24.

The following discussion will assume the default characters defined below.

handshake character	default ASCII character	hex value
ENQ	ENQ	05
ACK	ACK	06
X-ON	DC1	11
X-OFF	DC3	13

Host ENQ/ACK Handshake. This option is used to pace the data transfer from the card to the device to prevent the device from losing any data due to its slow internal processing speed.

The firmware sends an ENQ character after the pacing counter has counted down to zero. The card then waits for an ACK character before proceeding to transmit more characters from the transmit buffer. This will ensure that buffer space in the device is available.

You can program the pacing counter by using the Write Card Configuration, Subfunction 25 (WCC, SF 25). The default count is 80 bytes. The counter is decremented after each character is transmitted.

There is a programmable handshake timer to prevent the firmware from being hung if the ACK is lost or if the device is off-line and then comes on-line. The card will transmit an ENQ again until an ACK is received. You have the option of disabling the ENQ retry after the time-out by setting the "send message after ENQ timer time-out" bit in the Write Card Configuration, Subfunction 9 (WCC, SF 9). In this case the card will proceed with the data transmission from where it stopped.

If enabled, a handshake timeout will cause an event to be generated to the host.

The host ENQ/ACK timer is programmed by using the WCC, SF 18. The default value used is 5 seconds.

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CAUTION

DO NOT TOGGLE CHARACTER HANDSHAKES TO OFF WHILE WRITE DATA IS BEING TRANSMITTED. IF THE TRANSMITTER INITIATES AN ENQ/ACK HANDSHAKE DURING THE DURATION OF THE READ, THE ACK CHARACTER FROM THE DEVICE WILL BE TAKEN AS DATA (PLACED IN THE DATA BUFFER) AND THE TRANSMITTER WILL BE HUNG, PENDING A HANDSHAKE TIMEOUT IF ONE IS ENABLED. IF THE DEVICE SENDS AN XOFF CHARACTER TO STOP THE TRANSMITTER, THIS TOO WILL BE PLACED IN THE DATA BUFFER AND THE TRANSMITTER WILL *NOT* STOP. THE TX BUFFER EMPTY EVENT CAN BE USED TO ENSURE THAT A TRANSMIT OPERATION IS NOT TAKING PLACE.

If the transmitter does become "stuck", the "restart output" request (Control Card, Subfunction 5) can be used to continue transmitter operation. The handshake character, however, will remain in the receive buffer.

Device X-ON/X-OFF Handshake. This handshake protocol allows the device to pace the data transfer from the card to the device. The device will signal the card to stop transmitting data by sending an X-OFF character. The receiving device restarts data transmission by sending the X-ON character, or by sending any character if the Implicit Device X-ON option is enabled with WCC, SF 31.

An implicit device XON allows any received character to restart a transmission which was suspended because of a received XOFF. This is useful when communicating with a terminal where the user may press XOFF to suspend output.

The MUX firmware will stop data transmission as soon as the X-OFF character is received; however, up to two characters may be transmitted before the stoppage due to the SIO FIFO buffer.

If the handshake is disabled while output is in progress, a Restart Transmitter request may be needed to prevent outbound data from getting stuck on the card.

The handshake timer is programmed using WCC, SF 18. If this timer should timeout, an event, if enabled, will be generated to inform the host. Data transmission may be resumed with Control Card, SF 5.

Host X-ON/X-OFF Handshake. This handshake protocol allows the MUX to pace the data transfer from the device to the MUX. The MUX sends the X-OFF character (DC3 or CNTL-s) to the device to stop data transmission when there is less than about 71 bytes of space in the receive buffer. The MUX sends the X-ON character (DC1 or CNTL-q) when buffer space becomes available again.

If the device continues to transmit data to the MUX after the MUX has sent an X-OFF, the data will be added to the receive buffer until it overflows. Once the data buffer overflows, data will be lost. If echoing is enabled, the received data will be echoed even after the X-OFF, but not after an overflow.

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To prevent any deadlock situation, the MUX will transmit the X-ON character even if the device had sent an X-OFF character as part of the device X-ON/X-OFF handshake.

Single Text Termination

For single text termination, you have the option of determining which characters are to be used as the text terminator. An example of a single text terminator is the carriage-return character (CR, 0DH).

The single text terminator is not added to the buffer unless enabled by WCC, SF 8. The character is returned in the event status block and the request status block.

The Single Text Termination option is enabled by setting the End On Single Text Terminator option in the read device data subfunction code or in the data block of the WCC, SF 1. This option may also be toggled (on/off) for the duration of the read device data request by setting the "toggle STT" bit in the request subfunction.

The single text terminator characters are programmed by specifying the actual ASCII characters by using the WCC, SF 32. A maximum of eight characters per port may be designated as text terminators at any time.

End-On-Count Text Termination

The End-On-Count Text Termination option is enabled by setting the End-On-Count option in the read device data subfunction code or in the data block of the WCC, SF 1. The count is programmed by using the WCC, SF 2. When the count decrements to zero, the current receive record will be terminated with the message type indicating an end-on-count.

The End-On-Count option should not be confused with the internal card end-on-count which is set by the MUX firmware to 252 bytes. This internal count is used to manage the receive buffers on the card. When this count is exhausted, the current record will be terminated and will be made available to the host. The termination type will be set to "message terminated by the card, more data coming". This procedure allows the host to start reading data from the card while the card is still receiving data from the device.

Alert 1 Mode

When this mode is enabled, and if there is no read device data request pending on the card, and if none of the conditions discussed above were encountered to terminate the record, the firmware will notify the host by a "data available" event that at least one character was received. The host should post a read device data request upon receiving this notification. The card will return all characters received from the time that the alert event status was posted up to the execution of the read. The read buffer must be large enough to hold the maximum number of characters; otherwise, data will be discarded unless the S-bit is set.

If any of the text termination options discussed above are enabled, they may terminate the record early and the host will receive that text termination code and not the alert code for the message type.

If the alert 1 read mode is enabled and the host posts a read device data request, the card will *not* suspend the read when no data is available on the I/O channel-to-card interface module

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("backplane") or the MUX-to-device interface module ("frontplane"). Instead, you will receive a transmission log of zero length.

The alert 1 read mode is enabled by setting the alert 1 bit in the data block of the WCC, SF 3. When the mode is enabled, and there *is* data on the frontplane, and there is *no* data on the backplane, a "data available" event will be generated immediately.

In summary, the alert 1 read mode has the following characteristics:

1. If the backplane has no receive record, an event will be generated when the frontplane receives a character which does not meet any of the terminating conditions described above.

2. If the backplane has no receive record and the frontplane has an active record, the backplane will cause the frontplane to terminate the record to satisfy the read.

3. If the backplane and the frontplane both have no active record, the read will be terminated immediately with a transmission log of zero.

The text terminating code will be alert 1.

Type Ahead and Echoing

Type ahead mode allows the MUX to receive text before the host has posted a read for the text. The card has enough RAM space to buffer several text lines. This will allow the device to send many lines before stopping.

If the receive buffer should become full, any new incoming data will be lost. If echoplex is enabled, you will notice this when the typed character is not echoed.

NOTE

If you should change any of the read termination parameters, such as text termination, end-on-count, and so on, the new paramaters will not affect any text record that has already been terminated. If the frontplane has an active receive record, the text termination conditions will become active after the current record is terminated. Otherwise, the new read parameters will become effective immediately.

In echoplex mode, if a transmit record is active, any incoming characters will be echoed after the transmit record is empty. This should prevent incoming characters from interrupting any outgoing escape sequences which are less than or equal to 252 bytes. It will not, however, prevent a write from interrupting an escape sequence being echoed from the receiver, or if software handshaking is enabled, the handshake characters will not be prevented from interrupting any outgoing text.

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NOTE

THE MUX CARD HAS A 128-BYTE ECHO BUFFER FOR EACH PORT. IF THIS BUFFER SHOULD OVERFLOW, ECHO INFORMATION WILL BE LOST, ALTHOUGH THIS WILL NOT AFFECT ANY RECEIVE TEXT BUFFERS. AN OVERFLOW CAN BE CAUSED BY THE CARD RECEIVING (LOTS OF) DATA AFTER HAVING RECEIVED A DEVICE X-OFF, OR NOT YET HAVING RECEIVED AN ACK TO A HOST ENQ.

Character echoing is enabled by setting the echo bit in the data block of the WCC, SF 1. Character echoing may be toggled (on or off) for the duration of the request by setting the "toggle echo" bit in the subfunction. Echoing is only available for full-duplex transmission mode.

The card will not echo single text termination characters. However, the card can be enabled to echo a CR/LF for every CR received as a single text terminator by setting the "echo CR-LF for CR text terminator" in the data block of the WCC, SF 9. By using the WCC, SF 27, you may select which single text terminator in place of the CR to cause the CR-LF echoing.

Receiving Transparent or Binary Data

Transparent, or binary, data is defined to be data read with no processing by the firmware. The data is always terminated by using the End-On-Count option. All special processing such as software handshake, edit mode, and single text termination should be disabled. This may be done by changing the read configuration in WCC, SF 27; or by setting the read device data request subfunction bits "toggle edit", "toggle signal", and "toggle quoting" as necessary.

Note that data errors (parity, framing, overflow) will terminate the record unless specifically disabled (WCC, SF 31).

Function of Read Request Length

The read request will invoke special read processing when:

1. No current receive record is available on the backplane and

2. alert 1 mode is disabled.

If the special read processing is invoked, the firmware will perform two different types of actions depending on the status of the frontplane. If the frontplane has a current record which can satisfy the read request, the record will be terminated with the "text terminated by card, no more data" code and be given to the backplane to satisfy the read request.

NOTE

If the read request has the S-bit set, any future read requests will be satisfied by the remaining data in the current record until the buffer is exhausted.

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The preceding note has several implications. If the next read request exceeds the remaining data length, the read will be terminated early with the above termination code. Note that the read request length in this case will not be satisfied. If the read request length is less than the remaining data length, the read will be satisfied in total. If the S-bit is set, any data remaining will be saved for future read requests.

If the frontplane has no active receive read, or if the frontplane receive record is less than the read request length, the firmware will set the down-counter to the remaining count needed to satisfy the read. The firmware will suspend the read request until the receive record is available for the backplane (i.e., until either the down-counter hits zero, or a terminating condition is detected).

If a read request is terminated by the down-counter hitting zero, the termination code for the record is "card terminated read, no more data".

Host Initiated Text Termination

There are many occasions when the host would like to terminate data transfer early without losing what has already been read. For example, an application may require the read to be terminated by satisfying the length, or by timing out.

A control card request with subfunction 4 allows the host to terminate the frontplane receive record with the "host initiated text termination" termination code. If no read request is active, a receive record will be generated and it may or may not contain any data. However, no record is generated if there is no buffer space.

TRANSMIT CHARACTER PROCESSING

If echoing or software handshaking is enabled, the transmit interrupt processor will give priority to those characters before transmitting any user data. However, if a current transmit record is active, the echoing will be delayed until the current record is empty. See the paragraph "Type Ahead and Echoing" for additional details.

Automatic Output Separators Appendage

The firmware will append one or two characters to the transmitted message depending upon the write option. The Automatic Output Separators Appendage option is enabled by setting the "append output separator" option in the write device data subfunction code. The output separator text is programmed by using WCC, SF 28.

Transmitting Transparent or Binary Data

Transparent, or binary, data is defined to be data written with no processing by the firmware. This may be achieved by disabling options such as Automatic Output Separators Appendage. Furthermore, software handshaking must also be disabled to eliminate those characters from being transmitted within the user's binary data.

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BUFFER FLUSHING

Several control card requests are provided to flush or clear any receive or transmit records on the card. The control card request with subfunction 1 or 2 is used to flush the current backplane receive buffer, and to flush all the queued receive buffers, respectively. The control card request with subfunction 3 is used to flush all the queued transmit buffers.

The current backplane receive buffer is defined to be the record for the next host read. If the S-bit is set for the host read and if there is any data remaining, the remaining data is the current receive buffer. If the previous read has the S-bit set and there is no remaining data, the current backplane buffer is defined to be the next record for the host read.

If no buffer exists on the card, the control card request will be ignored.

PROGRAMMING THE RECEIVER AND TRANSMITTER

The selection of the transmission mode is programmed by using the WCC, SF 5.

Simplex receive and simplex transmit are provided to turn off the transmitter and receiver, respectively.

The character size for the receiver and the transmitter may be specified at 7 or 8 bits per character, not including an optional bit for even or odd parity. On transmit, the user data will be processed byte-by-byte, passing the 7 or 8 least significant bits in each byte to the transmitter, depending on the programmed character size. A parity bit will be added by the MUX if even or odd parity is enabled. On receive, the incoming data will be passed to the user's buffer into the 7 or 8 least significant bits of each byte, with the unused bits being zeros. The parity bit is never returned to the user. The character length is programmed by using WCC, SF 11. The format of an asynchronous message is shown in figure 4-1.

The baud rate and the number of stop bits are programmed by using the WCC, SF 10 and 12, respectively.

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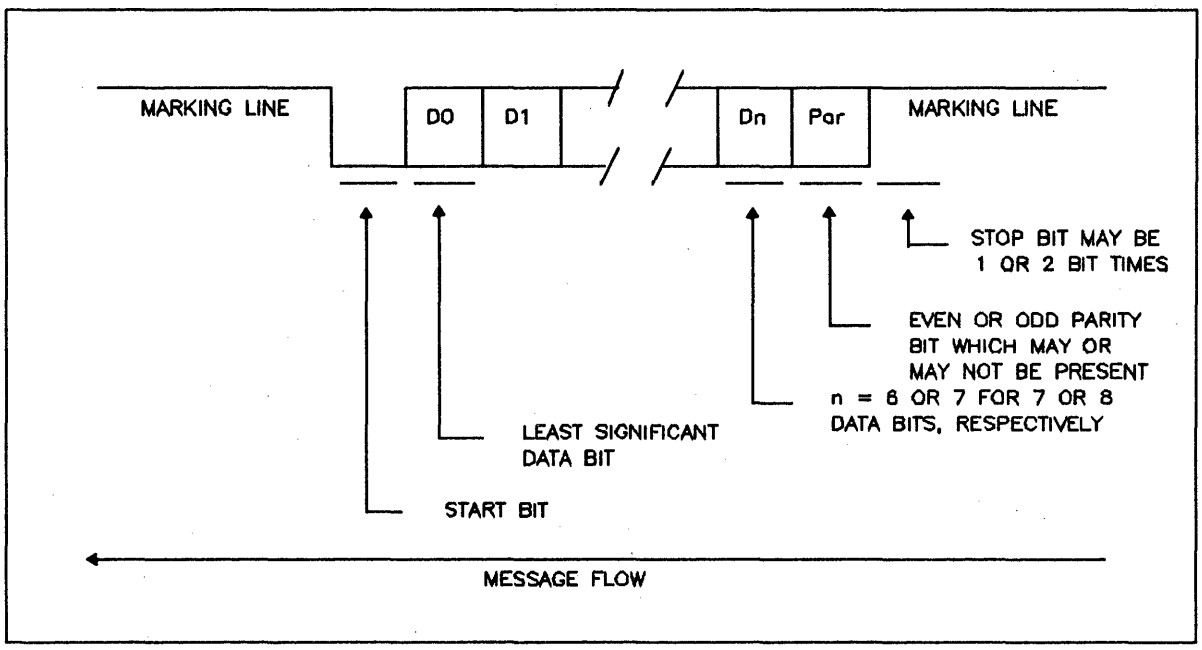


Figure 4-1. Asynchronous Message Format

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PARITY IN TRANSMITTED OR RECEIVED DATA

There are five parity options available for transmitted or received data:

no parity

odd parity

even parity

'0' parity

'1' parity

The first parity option generates no parity nor will it check for any parity. The character length specified is the actual data element sent and received.

The second and third parity options cause the generation and detection of parity for the transmitted and received data, respectively, by the SIO. An additional bit is added to the data element for parity.

The fourth and fifth parity options clear or set the most significant bit of every character transmitted. For the character length of 7 or 8 bits, the 7th or 8th bit, respectively, of the character will be clear or set before the character is transmitted. On incoming characters, the force parity bit will be stripped with no checking.

The parity option is programmed by using the WCC, SF 13.

BREAK DETECTION

The firmware notifies the host of receiving a break from the device by sending an unsolicited event status, if enabled.

HANDSHAKE TIMER

After sending an ENQ, the firmware will wait up to the specified timeout for the ACK. If the ACK is not received within the given time and if the ENQ retry is enabled, an ENQ will be sent again. This will continue until an ACK is received. The default value is five seconds. The clock resolution is one second. The timer can be programmed from 1 to 255 seconds by using the WCC, SF 18. A zero value will defeat the timer; that is, there will be no timeout.

If enabled, a handshake timeout will generate a "handshake timed out" event.

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ADDITIONAL OPTIONS

Six additonal options are available for special use, as follows:

1. Do not terminate the text record on errors
2. Quoting character mode
3. Conditional output separators appendage
4. Signal (interrupt) characters
5. Implicit device X-ON
6. Insert a null character into the receive buffer when a break is detected.

All six options are configured by using Write Card Configuration, Subfunction 31 (WCC, SF 31).

Error Handling

Under normal MUX firmware operation, the incoming text is terminated when any receive data error is encountered. Furthermore, the character causing the error is added to the text record for the host. This allows the host to detect the undesirable error condition.

If the Do Not Terminate Text Record On Error option is enabled, the firmware will not terminate the text record. The incoming character with the error will be replaced by the user-specified replacement character which has a default value of 7FH ("DEL"). The replacement character will be added to the text buffer and will be echoed, if echoing is enabled. The buffer, however, will be marked "bad" when eventually terminated and sent to the host.

Under normal operation, the incoming text is terminated when any error is encountered. Furthermore, the character causing the error is added to the text record for the host. This allows the host to detect undesirable error conditions.

If the "do not terminate text record on error" option is enabled, the MUX firmware will not terminate the text record. The incoming character with the error will be replaced by the user-specified replacement character which has a default value of 7FH ("DEL"). The replacement character will be added to the text buffer and will be echoed, if echoing is enabled.

If the "ignore parity" option in WCC, SF 13 is set, the firmware will ignore all parity error conditions. The character will be processed as if no error had occurred.

Finally, if the "ignore all SIO errors" option in WCC, SF 13 is set, all received characters with an error will not be processed. However, the error bit in the termination code will be set to indicate that an error had occurred and that characters have been discarded.

Figure 4-2 is a flowchart showing how a received character with an error is processed.

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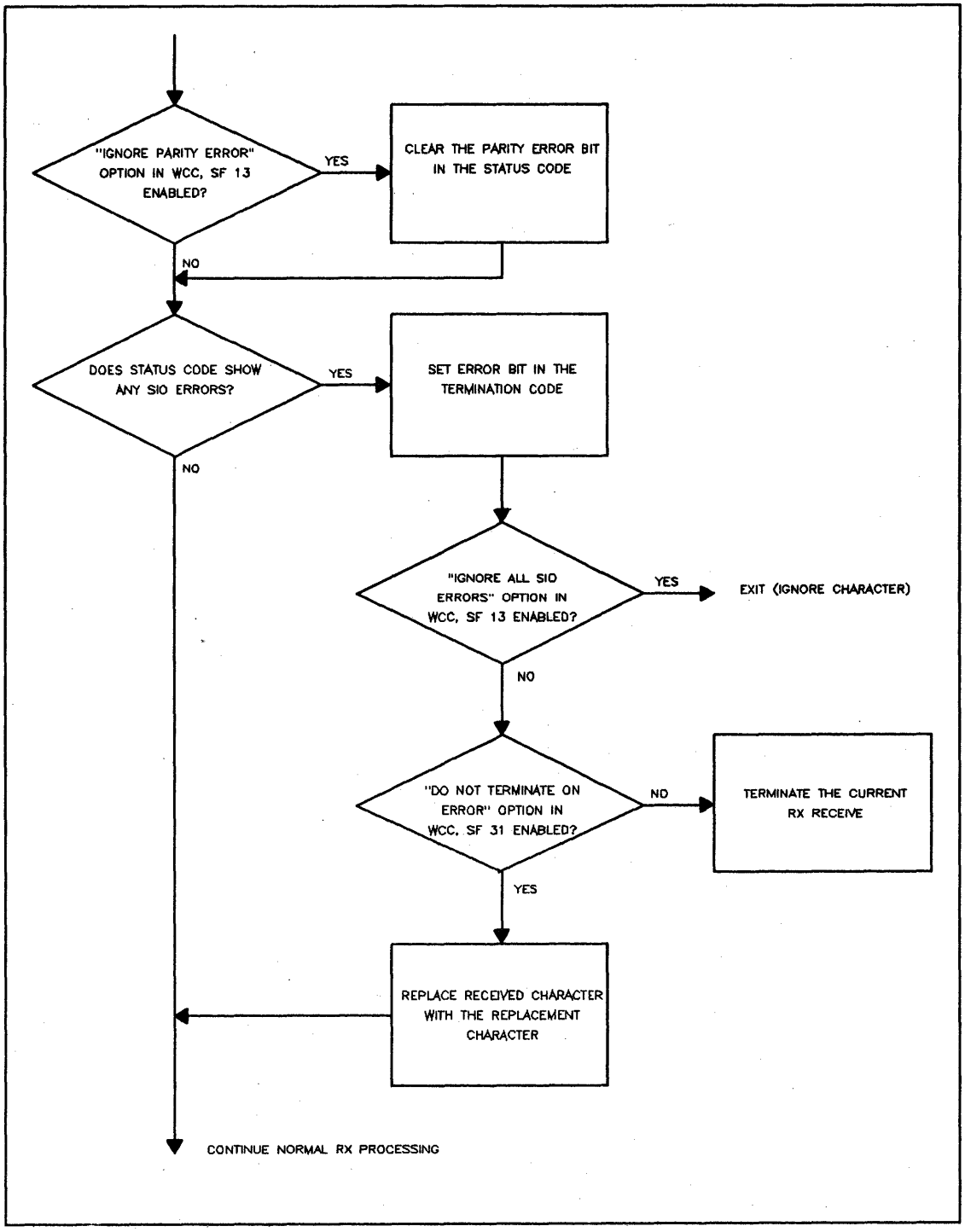


Figure 4-2. Error Handling Flow Chart

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Quoting Character Mode Option

When the Quoting Character Mode option is enabled, the editing characters (backspace and line delete) and a specific single text terminator are able to be treated literally by preceding them with the backslash ("\"). For example, if you type

\ DEL

DEL is put in the user's read buffer, and the line would not be deleted. You would be able to erase the "DEL" character as any other character typed, even though the echoing of such an erasure may not look right on the terminal.

If followed by any other character, the quoting character causes no special action and is placed in the text buffer as is any other character.

The quoting character and the specific single text terminator are programmable and have a default value of the backslash (\) character.

Conditional Output Separators Appendage

When the Conditional Output Separators Appendage option is enabled, the firmware will examine every outgoing character for the user-specified record separator, which has a default value of the linefeed character. If the user-supplied record separator is found, the firmware sends the output separators in place of the record separator.

If the Automatic Output Separators Appendage option is enabled, the output separators are also added to the end of each message.

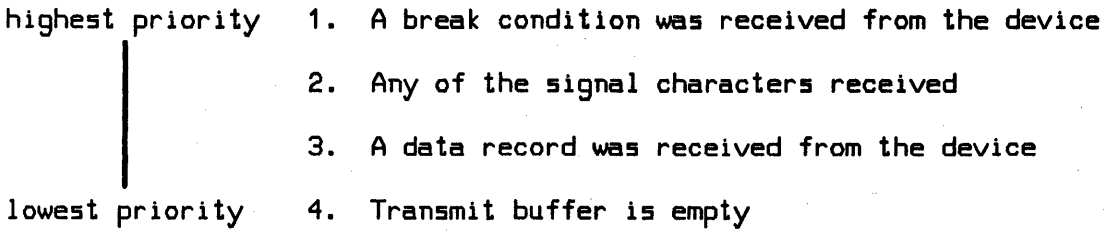
Speed Sense Mode

The Speed Sense mode, initiated by Control Card (CC) Subfunction 6, puts the card in a mode where the baud rate of incoming data is sensed and the channel configured accordingly. The firmware waits for a "start bit" and, in synchronous mode, samples the incoming data stream at 19200 baud. The resulting data is compared to known configurations of the 7-bit "carriage return" character (0D hex). If a match is discovered, the channel is configured for that baud rate, and an event is generated to inform the host of the baud rate and the state of the parity bit (the sense of bit position 8). Searching continues until a match is found, or until the Speed Sense mode is disabled by CC SF 7.

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ASYNCHRONOUS EVENTS

The host may poll the card or may be interrupt driven by the card for any asynchronous event which can be detected by the MUX firmware. There are four major categories of events. The events are listed below in the order of their priority.



The events may be enabled or disabled by using the WCC, SF 21. The event interrupt is enabled by setting the corresponding mask bit and disabled by clearing the bit.

If the interrupt mask for an event is disabled, you may poll for the event by using Read Card Information (RCI), Subfunction (SF) 254.

See the paragraph "Event Block Description" for a detailed description of the event block format returned to the host.

If all interrupt conditions are disabled, no asynchronous interrupts will occur.

SOLICITED EVENTS

The MUX will generate a solicited event upon completion of a speed sense operation. The event block contains the "speed sense completed" event code, the baud rate which was detected, and the sense of the parity bit in the carriage return character.

Because this event is solicited, it cannot be masked nor polled.

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DIAGNOSTICS

The MUX self-test performs diagnostic tests to detect malfunctions. Self-test is executed 'offline'. That is, it does not run concurrent with the standard MUX firmware. It is executed on a hardware reset of the card following a CHANNEL I/O "Addressed Device Clear" (DCL/DEN) or "Reset" (RES) assertion. It exercises the major components and data paths on the card. If no problems are found, the card is made functional and the standard MUX firmware is invoked. If a hardware malfunction is detected, the card is left disabled, indicating that self-test failed.

The following tests are performed by self-test:

* **ROM test:** To insure that no bits have changed on the ROM (EPROM), a cyclic redundancy check is done using the polynomial X**16+X**2+X+1. The test is performed in 4K segments to ensure accuracy of the CRC.

* **RAM test:** RAM is checked for both stuck-at-0 and stuck-at-1 conditions and address decoder failures.

* **ASYNC SIO Loopback test:** Verifies that the SIO can perform basic asynchronous transmit and receive functions. If a loopback hood is sensed, loopback is performed using both the internal and external line drivers.

* **CTC test:** Detects stuck-at faults in the data lines, system control, interrupt control (except CTC 1 and 2, which have no interrupt capability), and the four channel signals, for each CTC.

* **BIC test:** Checks the Backplane Interface Circuit (BIC) for functional faults. Checks for some stuck-at faults in internal BIC registers. The BIC circuitry is tested using the internal loopback functionality built into it. Testing of I/O channel driver and receiver hardware external to the BIC is not done by self-test. The combination of the host diagnostic and MUX loopback support in the 'standard' MUX firmware will exercise the host/MUX interface.

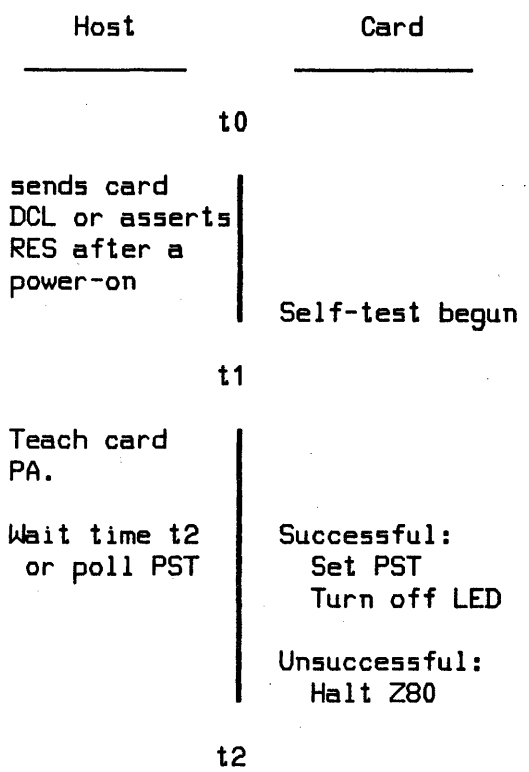
* **MIC test:** Checks the Memory Interface Circuit (MIC) for functional faults. The registers in the MIC which can be read and written to are checked for stuck-at-1 and stuck-at-0 faults, and both read and write DMA on both DMA channels are tested using SIO channel 0. Some MIC registers cannot be tested (they are write only), and the DMA test does not exercise all possible DMA configurations (time limitations).

Upon successful completion, self-test will set 'Passed Self-Test' status (PST), turn off the LED on the card, and invoke the standard MUX firmware. The standard firmware will then wait for the host to 'teach' it its Peripheral Address (PA).

If self-test fails, the LED is left on, the 'Passed Self-Test' status (PST) is not set, and the Z80 is 'Halted'.

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The following time-line illustrates the host/card interactions during the self-test sequence:



where:

t1 = 1.0 second

t2 = 3 seconds if RES, or 15 seconds if DCL/DEN; may be less

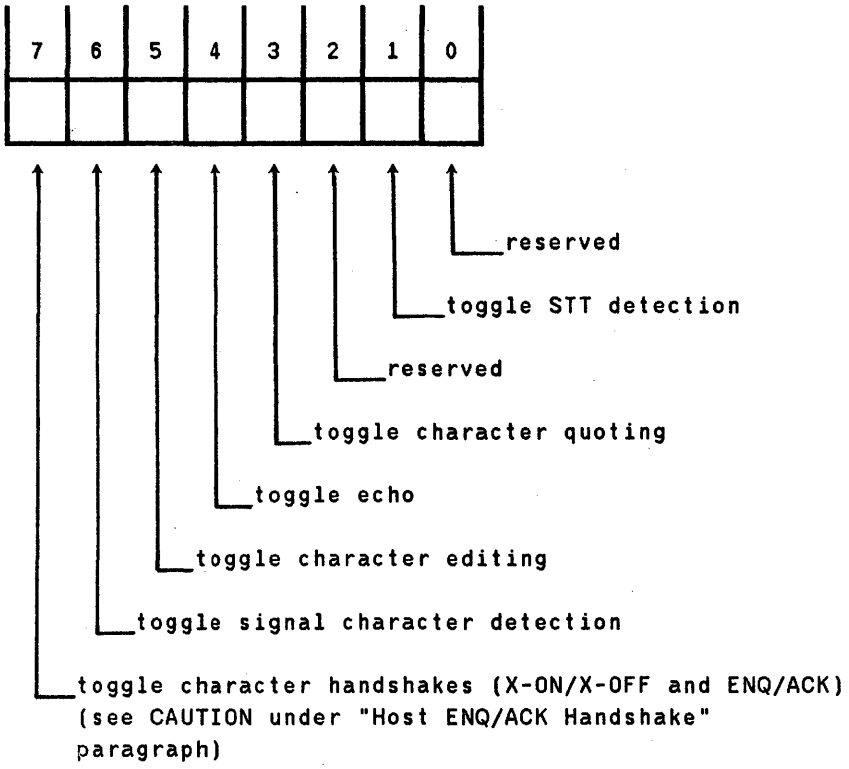
CONNECT LOGICAL CHANNEL REQUEST DEFINITIONS

The following paragraphs describe the subfunction options that are available for each Connect Logical Channel (CLC) request. See the paragraph "Connect Logical Channel (CLC) Request Format" for a description of the data format.

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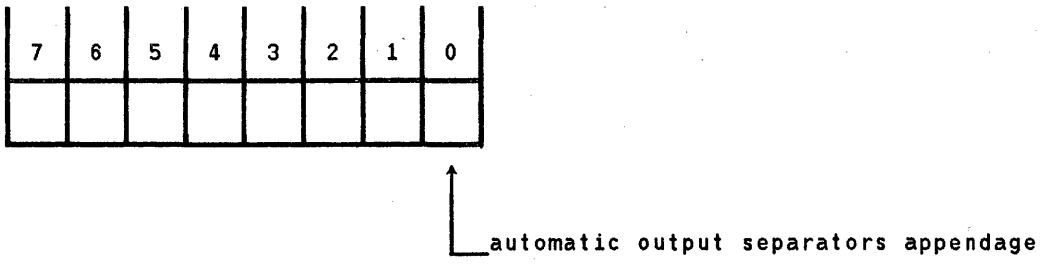
Read Device Data, Request Code = 1

Subfunction code



Write Device Data, Request Code = 2

Subfunction code



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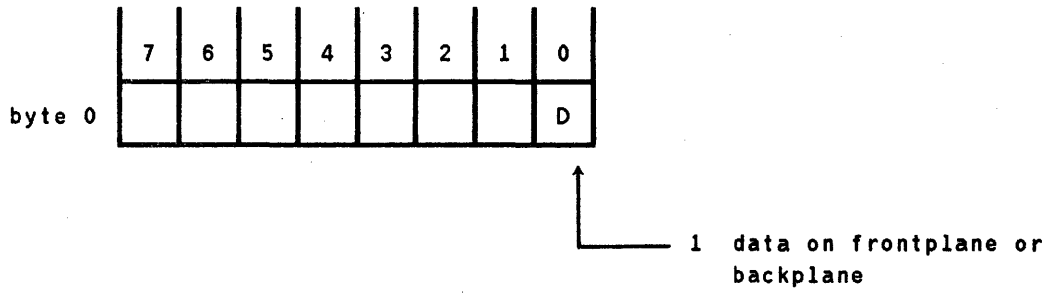
Read Card Information, Request Code = 4

For the read card information request, the residue count in the read request status block will reflect the number of bytes of information not returned in the request. This will always be nonzero when the requested data transfer length is not large enough to hold all the information requested.

Subfunctions 0 through 33 - Read Port Configuration. Subfunctions 0 through 33 read back the information defined in subfunctions 0 through 33 of the write card configuration, respectively.

Subfunction 249 - Read Data Status. Returns a byte which indicates the presence of any receive data (terminated or not) on the MUX for the indicated port. Received data exists on either the backplane or frontplane if the returned byte is non-zero.

The data block returns the following:

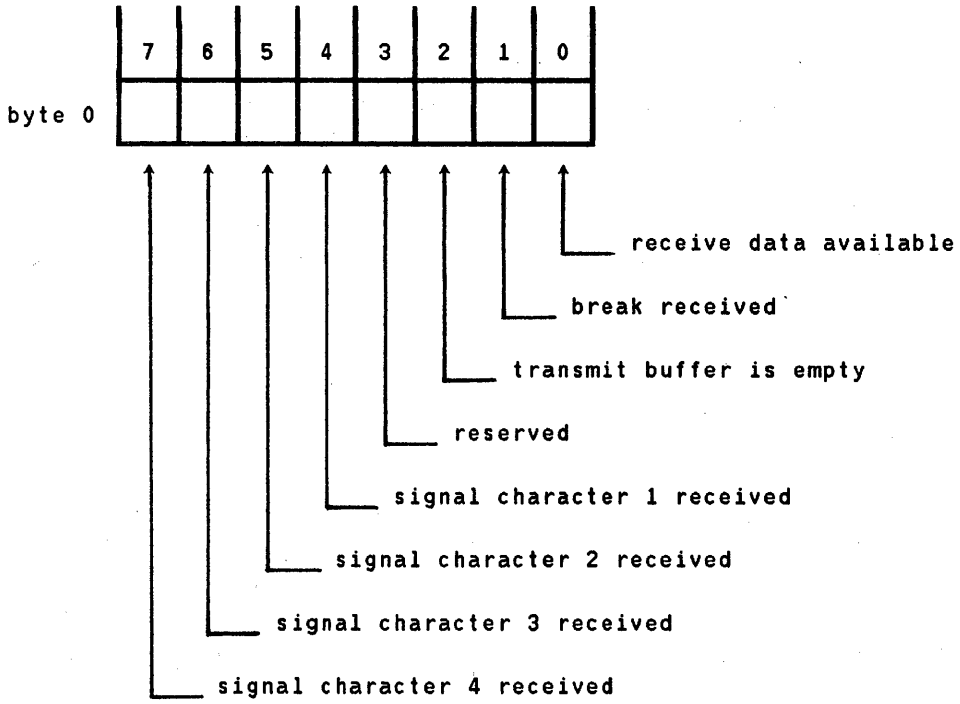


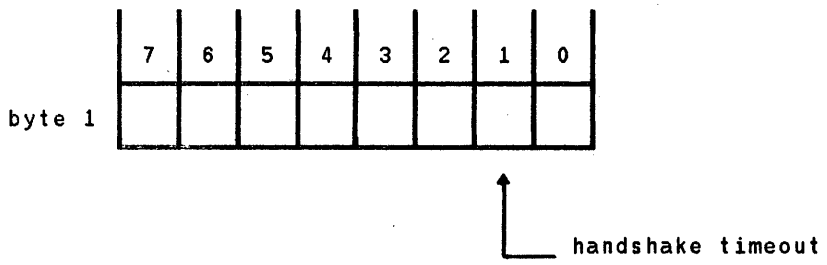
Subfunction 250. Get Card RAM. The uppermost 16K bytes of card RAM memory is sent to the host in the data block. (The other 32K bytes of RAM are not used by the MUX firmware.) The host buffer must be large enough to hold the data.

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Subfunction 254. Get card status. The following status is returned in the data block.

Data block





This status will be cleared each time it is read.

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Write Card Configuration, Request Code = 5

NOTE

The firmware will perform parameter validation where possible. Every write card configuration request data transfer length must match exactly the length specified for the request; otherwise, the illegal configuration parameter length error will be returned in the read request status block. If the data transfer length is not specified for the subfunction validation below, the length is assumed to be one byte. (Note that data transfers shorter than the required length are not zero-filled, and will give an error as stated above). If the subfunction code is not one of those described in this manual, an illegal subfunction error will be returned.

For each of the subfunctions defined in the following paragraphs, a brief description of the type of validation performed on the parameter passed in the data block will be given. If the parameter is not valid, an illegal configuration parameter value error will be returned.

Subfunction 0. This subfunction sets all of the configuration data defined in subfunctions 1 through 32. The data is position dependent according to each subfunction code. This subfunction allows one call to configure everything, instead of calling each individual item. After the initial configuration, a particular item can be changed as needed.

Note that if you use this subfunction, every item must be specified with new values. The default values or the previous values that were specified will be set to the new values given.

The data block is defined as follows:

```
byte   0: configure frontplane control

       1: high byte end-on-count length

       2: low byte end-on-count length

       3: alert 1 read mode option

       4: reserved

       5: transmission mode

       6: backspace character

       7: line delete character

       8: other options
```


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9: device handshake option

10: baud rate

11: character length

12: number of stop bits

13: parity

14: reserved

15: reserved

16: reserved

17: reserved

18: reserved

19: character handshake timer

20: reserved

21: reserved

22: host interrupt mask, first byte

23: host interrupt mask, second byte

24: host X-ON character

25: host X-OFF character

26: device X-ON character

27: device X-OFF character

28: host ENQ character

29: host ACK character

30: host ENQ/ACK counter

31: reserved

32: reserved

33: a single text terminator character for echoing CR-LF

34: number of output separators

35: 1st output separator character or null

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36: 2nd output separator character or null

37: reserved

38: reserved

39: reserved

40: reserved

41: reserved

42: additional options

43: replacement character for bad incoming character

44: quoting character

45: record separator character to invoke sending output separators

46: signal character 1

47: signal character 2

48: quotable single text terminator

49: number of single text terminators

50: 1st single text terminator character

51: 2nd single text terminator character

52: 3rd single text terminator character

53: 4th single text terminator character

54: 5th single text terminator character

55: 6th single text terminator character

56: 7th single text terminator character

57: 8th single text terminator character

58: signal character 3

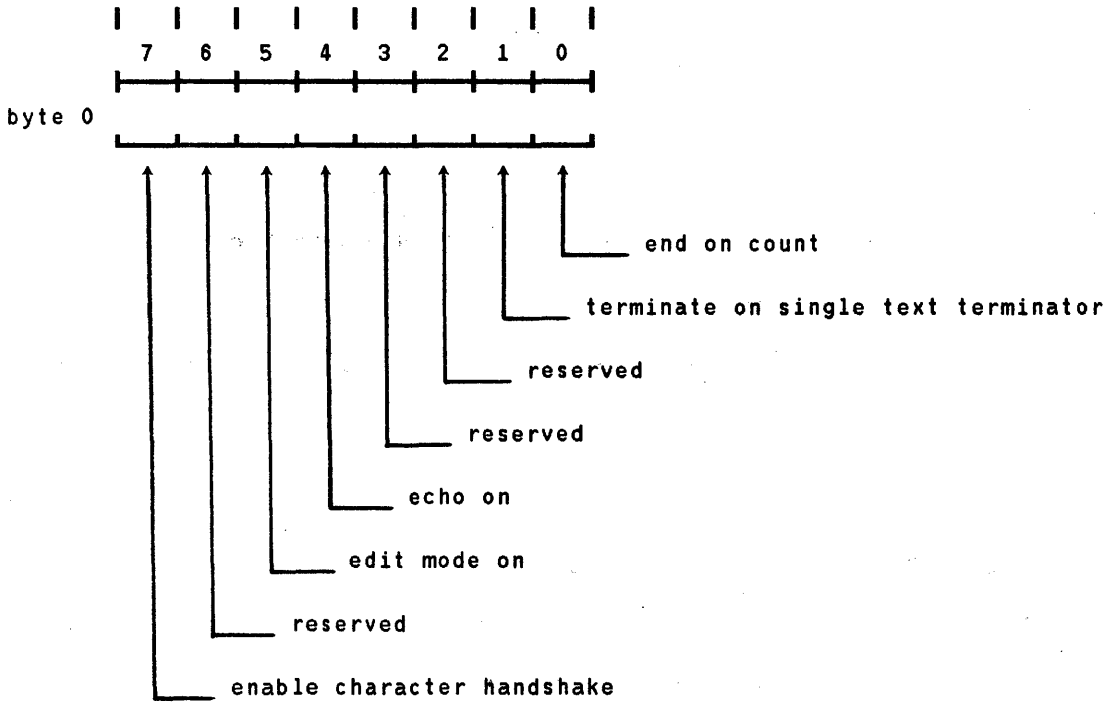
59: signal character 4

Validation: Data length must be 58 or 60 bytes

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Subfunction 1. Configure Read Option

Data block

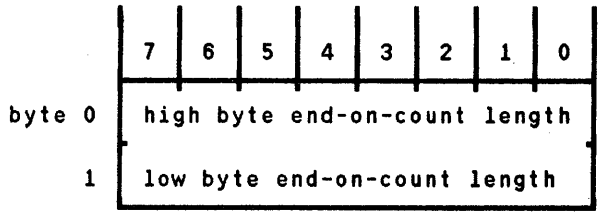


Validation: If the echo bit is set, the transmission mode must be full duplex. The transmission mode must be programmed first before setting the read option.

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Subfunction 2. End-On-Count Length.

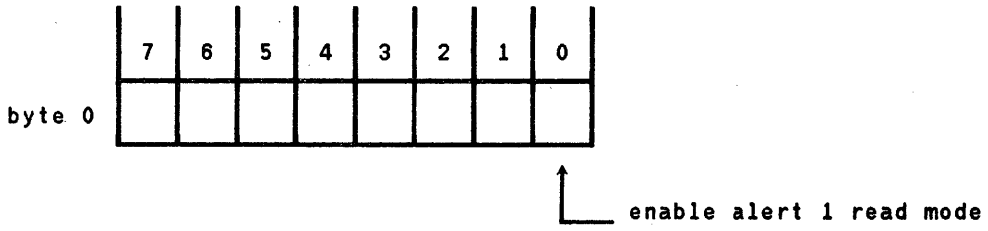
Data block



Validation: none

Subfunction 3. Alert 1 Read Mode.

Data block

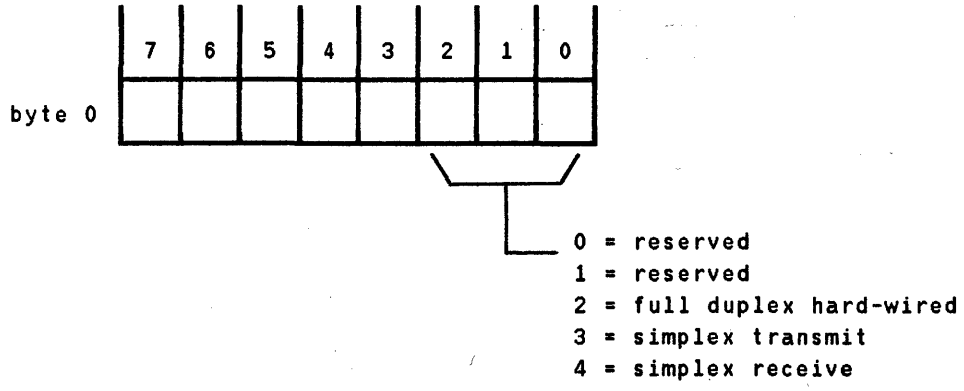


Validation: none

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Subfunction 5. Transmission Mode.

Data block



Validation: The parameter value must be within the range 2 through 4, inclusive. The transmission mode must be set before setting the read option. Note that the echo bit will be reset if the transmission mode is not full duplex.

Subfunction 6. Backspace Character. The character specified in the data block will be used as the backspace character for the edit mode.

Validation: none

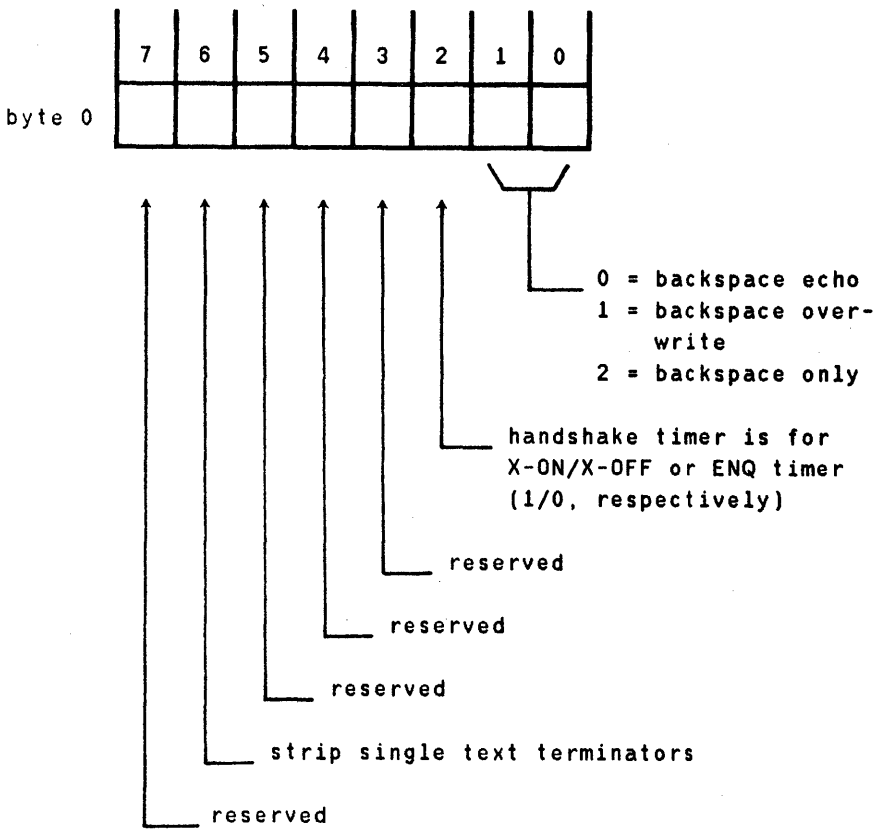
Subfunction 7. Line Delete Character. The character specified in the data block will be used as the line delete character for the edit mode.

Validation: none

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Subfunction 8. Backspace and Other Options

Data block

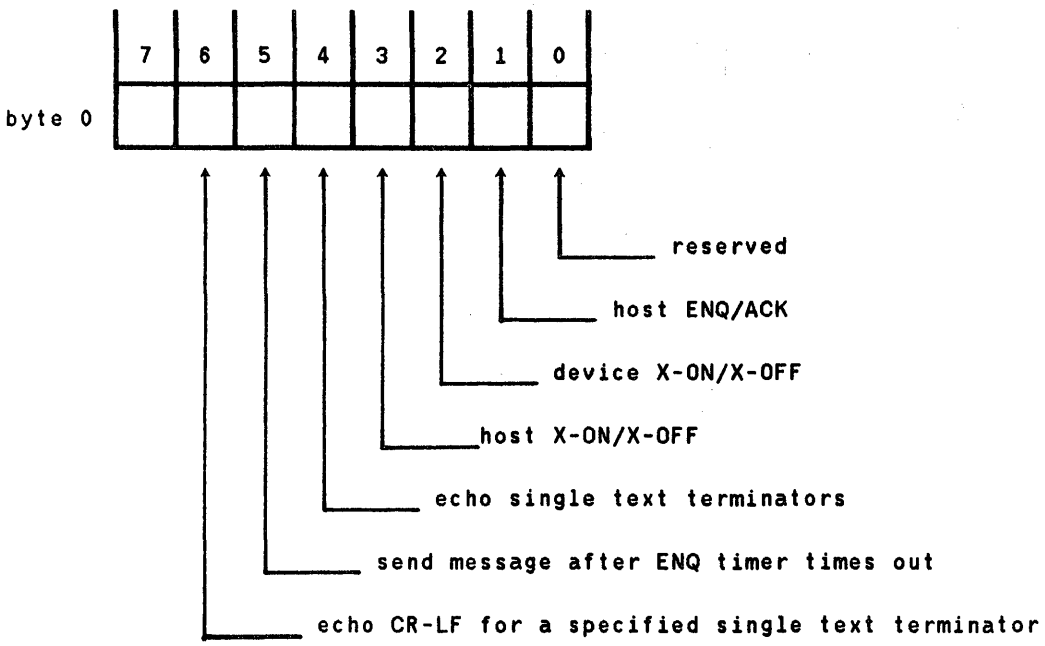


Validation: none

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Subfunction 9. Device Handshake Option

Data block

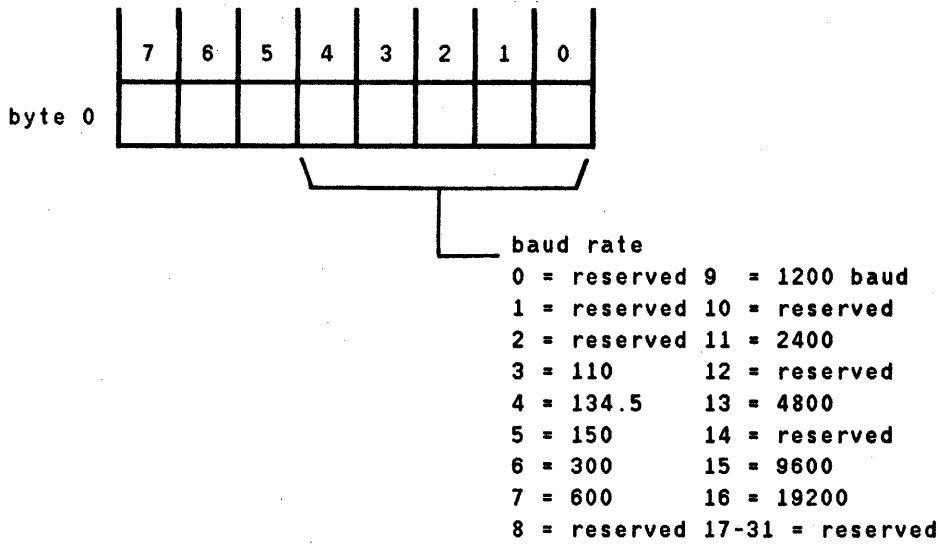


Validation: none

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Subfunction 10. Baud Rate.

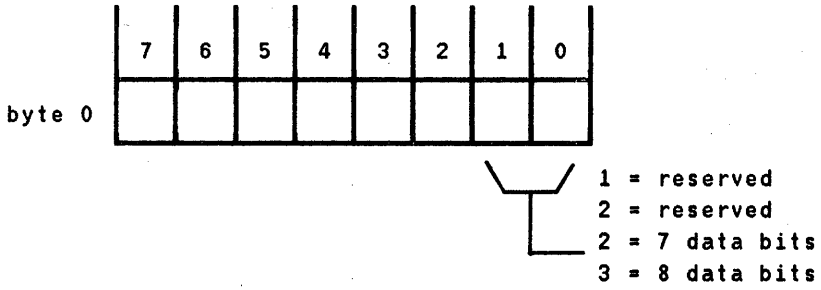
Data block



Validation: The value must be within the range 0 through 16, inclusive.

Subfunction 11. Character Length.

Data block

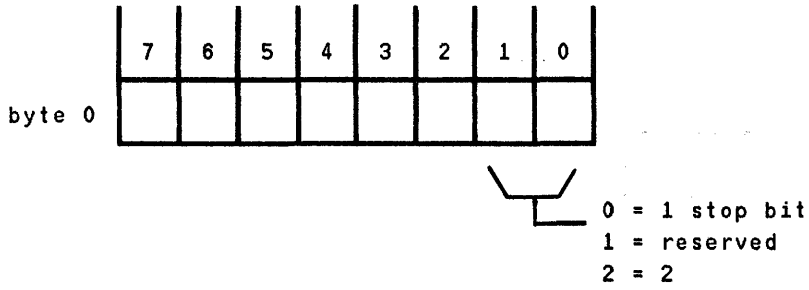


Validation: The value must be within the range 0 through 3, inclusive.

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Subfunction 12. Number Of Stop Bits.

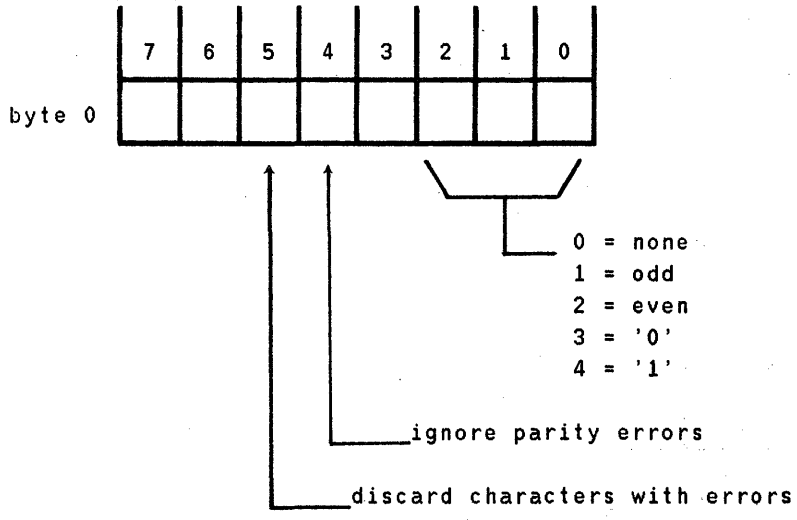
Data block



Validation: The value must be within the range of 0 through 2, inclusive.

Subfunction 13. Parity.

Data block



Validation: The value of bits 0-2 must be within the range 0 through 4, inclusive.

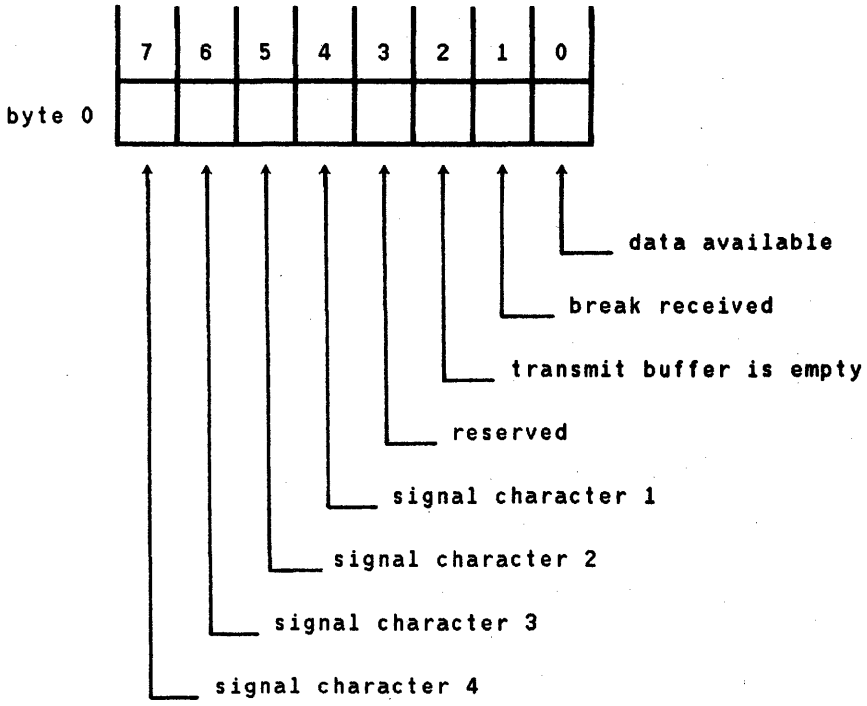
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Subfunction 18. Character Handshake Timer. Subfunction 18 sets the handshake timer in increments of 1 second. The timer can be programmed from 0 to 255 seconds.

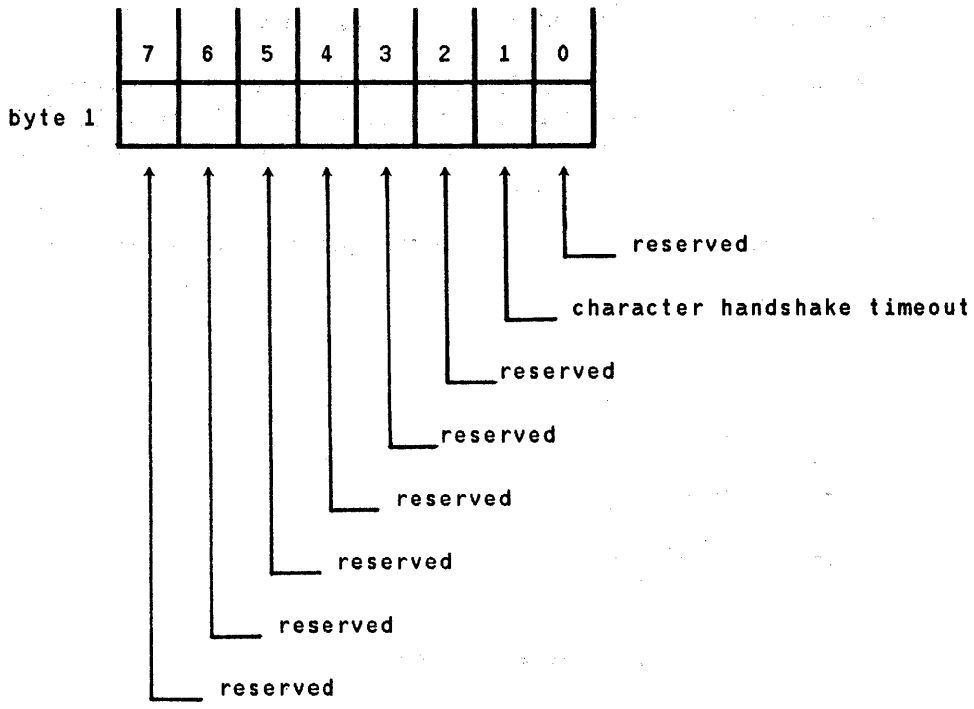
The timer is used for either the ENQ/ACK or device X-ON/X-OFF handshake. Because there is only one timer per port, the handshake for which the timer is used is selected by WCC SF 8. If the timer selected by WCC SF 8 is not the handshake enabled by WCC SF 9, no timer will be used.

Subfunction 21. Host Interrupt Mask. Subfunction 21 enables the specified unsolicited interrupt to the host.

Data block



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Validation: None. The data is not checked.

Subfunction 22. Host X-ON/X-OFF Characters.

Data Block

byte 0: character for host X-ON function
byte 1: character for host X-OFF function

Validation: Two bytes must be given.

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Subfunction 23. Device X-ON/X-OFF Characters.

Data block

byte 0: character for device X-ON function
1: character for device X-OFF function

Validation: Two bytes must be given.

Subfunction 24. Host ENQ/ACK Characters.

Data block

byte 0: character for host ENQ function
1: character for host ACK function

Validation: Two bytes must be given.

Subfunction 25. Host ENQ/ACK Pacing Counter.

Data block

byte 0: the number of characters to transmit before sending an ENQ and waiting for an ACK (count should be 1 to 255)

Validation: One byte must be given.

Subfunction 27. Single Text Terminator for Echoing CR-LF. Any one of the single text terminator characters may be specified to cause the echoing of the CR-LF characters. However, only one character may be used for the special echoing function. This character is specified in the data block for this subfunction.

Validation: none

Subfunction 28. Output Separator.

Data block

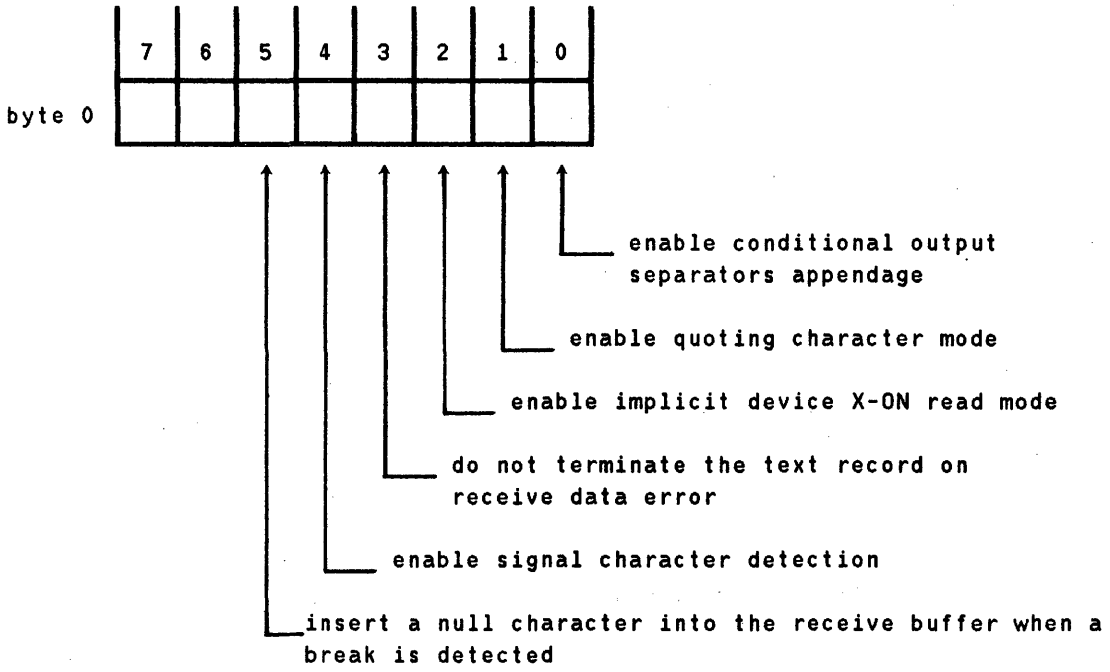
byte 0: 1st output separator character or null
1: 2nd output separator character or null

Validation: Length must be one or two characters.

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Subfunction 31. Additional Options.

Data block



byte 1: replacement character for the bad incoming character

byte 2: quoting character

byte 3: record separator character to invoke sending the output separators

byte 4: signal character 1

byte 5: signal character 2

byte 6: quotable single text termintor

byte 7: signal character 3

byte 8: signal character 4

Validation: Length must be seven or nine bytes.

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Subfunction 32. Single Text Terminator.

Data block

byte 0: 1st character to be used as a single text terminator

byte 1: 2nd character to be used as a single text terminator

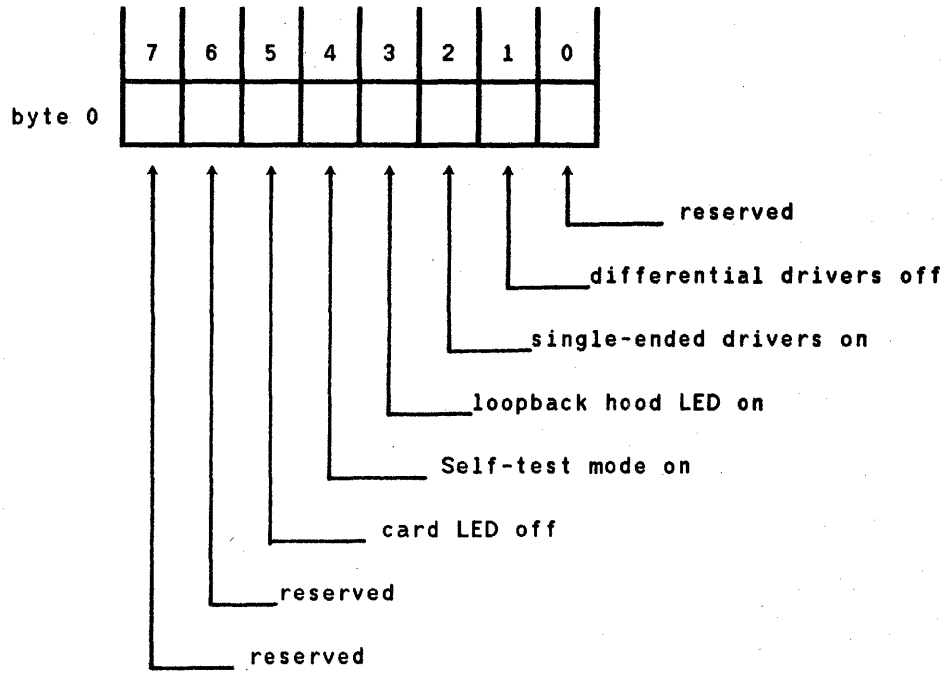
.
.
.

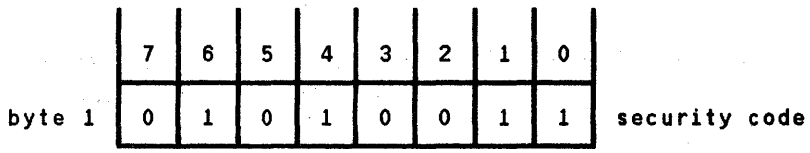
byte n: nth character to be used as a single text terminator

Validation: From one to eight characters may be specified.

Subfunction 33. Card Write Register. This subfunction is used for on-line diagnostics capability.

Data Block





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NOTE

The security code is used to prevent the user from inadvertently writing to this register.

Validation: Must be two bytes and have correct security code. The port ID field in the request is ignored, so any port may use this function.

Subfunction 34. Set Port ID. This request changes the mapping of logical port ID (the ID given in the request and event blocks) and the physical port address (0-7) of the device. The mapping defaults at power-up to a one-to-one mapping; i.e., ID 0 is port 0, etc.

The logical port ID is supplied in the request block Port ID field, and becomes associated with the physical port number in the data field. There is no restriction on the logical port ID, except that it should not duplicate any other ID.

Validation: The data must be between 0 and 7 inclusive.

Control Card, Request Code = 6

See the paragraph "Buffer Flushing" for additional details on this request code. A summary is shown below.

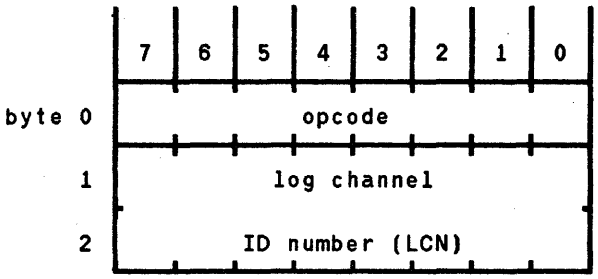
SUBFUNCTION	DESCRIPTION
0	No operation
1	Flush the current receive buffer
2	Flush all the queued receive buffers
3	Flush all the queued transmit buffers
4	Host initiated termination of frontplane record
5	Force restart of the transmitter if it was stopped due to waiting for ACK or X-ON handshake. This control request is usually used after turning off the handshake option to prevent deadlock.
6	Enter speed sense mode. When speed sense completes, an event will be generated.
7	Terminate speed sense mode. Speed sense mode (if enabled) is disabled. The port is reset to the previous baud rate, parity, and character size.

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8 Suspend transmitter. The transmitter on the indicated port will be suspended as if an X-OFF had been received. Either an X-ON (if enabled) or a Restart Transmitter (5 above) can be used to resume normal operation. This can be used to suspend output on receipt of some external event (e.g., BREAK).

RTS AND WTC BLOCK DEFINITIONS

The Read Transaction Status (RTS) and Write Transaction Code (WTC) block definitions are as follows:

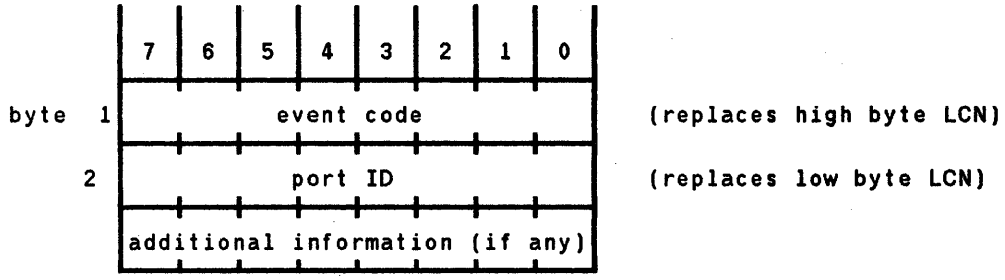


opcode	RTS description	WTC description
0	Nothing to do. The LCN field is not used.	Not used.
1	Switch to the transaction given in the LCN field.	Resume the transaction given in the LCN field.
2	Terminate the data transfer for the transaction given in the LCN field.	Terminate the data transfer for the transaction given in the LCN field.
3	Abort the transaction given in the TID field.	Abort the transaction given in the TID field.
4	Event sensed. The event block as defined below is returned to the host in place of the log channel ID number. The MUX card will return up to 6 bytes for the event block.	Acknowledgement to the event. Byte 1 is the port ID of the port to be acknowledged.

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5	Error in transaction given in the LCN field.	Not used.

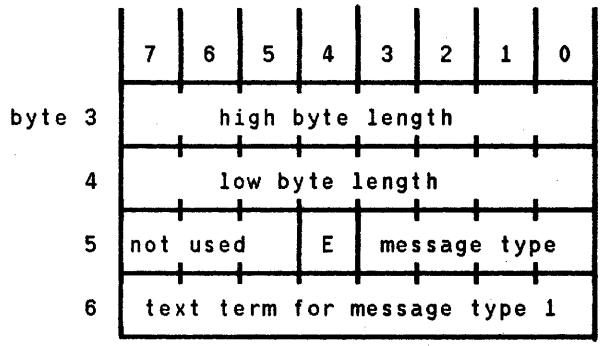
Event Block Description



event code

0 = reserved

1 = data message received. Message length and type are given in the information field.



message type

1 = text terminated on single text terminator. The text terminator which terminated the message is given in byte 6.

4 = text terminated by count

5 = text terminated by parity error

6 = text terminated by data overrun

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7 = text terminated by framing error

8 = alert 1; at least one character received

9 = text terminated by the card, more data coming

12 = text terminated by the card, no more data

13 = text terminated by buffer overflow

14 = text terminated by host

"E" = 1 = this record contains an error (Parity Error (PE), Framing Error (FE), Overrun Error (OV))

2 = break received from the device

3 = transmit buffer is empty

5 = signal character 1 received

6 = signal character 2 received

7 = signal character 3 received

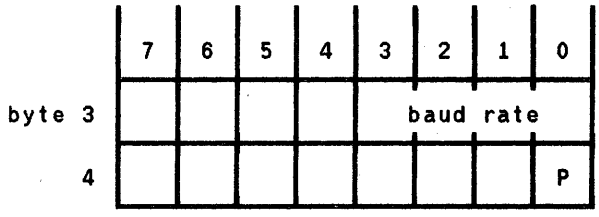
8 = signal character 4 received

9 = reserved

10 = character handshake timeout

11 - 253 = reserved

254 = speed sense completed



where baud rate is as defined for WCC SF 10
P = sense of bit in bit position 8 (parity)

255 = reserved

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port ID

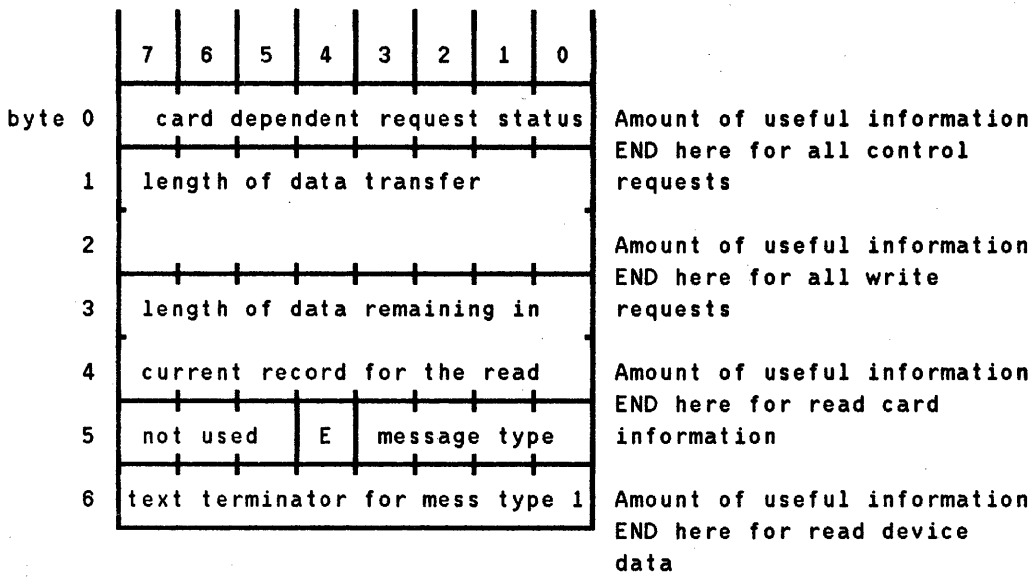
The port ID given is the logical port ID, as set by WCC, SF 34. This has a default one-to-one mapping to the physical port number if not changed.

additional information

The information contained in this field is dependent on the event code as given above.

Each event must be acknowledged before another event is received on that port.

READ STATUS REQUEST (RSR) BLOCK DEFINITION



card dependent request status

0 = no error

1 = illegal subfunction

2 = illegal configuration parameter values

3 = illegal configuration parameter length

4 = illegal request or request not implemented

5 = illegal port ID

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6 = data overrun in host write data (the host wrote more data than was specified in the request)

7 = block mode data transfer is not allowed for the request

8 = data transfer length is too large

9 = cannot execute control card request - not enough space

254 = transmit not allowed in simplex receive mode

255 = receive not allowed in simplex transmit mode

length of data transfer

This field gives the length in bytes of the data transfer initiated by the card for the host read or write request.

Note that the length does not reflect any early termination initiated by the host. For example, if the host started a host read request of 200 bytes and the card is able to send 200 bytes, the card will return the length as 200 even if the host invoked END to terminate the transfer early.

message type

1 = text terminated on single text terminator. The text terminator which terminated the message is given in byte 6

4 = text terminated by count

5 = text terminated by parity error

6 = text terminated by data overrun

7 = text terminated by framing error

8 = text terminated by alert one condition

9 = text terminated by the card, more data coming

12 = text terminated by the card, no more data

13 = text terminated by buffer overflow

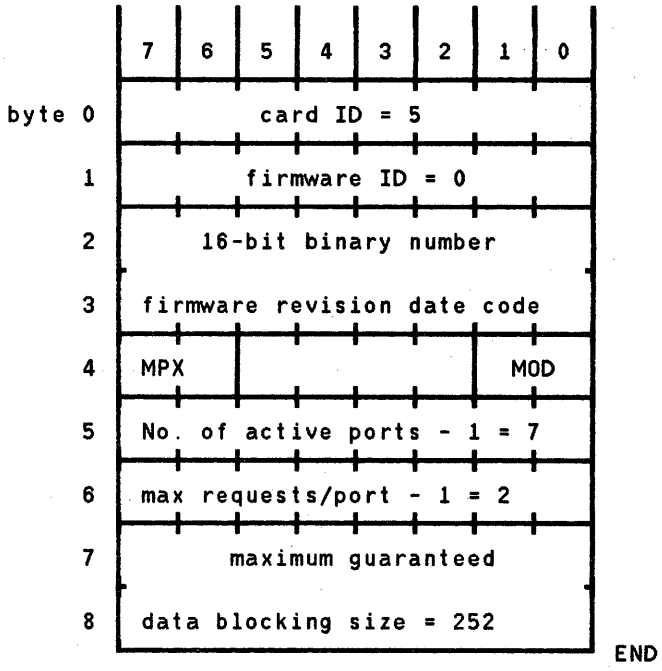
14 = host initiated text termination

"E" = record contains an error

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IDENTITY INFORMATION BLOCK DEFINITION

The following identity information block is returned by the MUX card for the IDY order.



MPX = 1 for in-channel multiplexing

MOD = 2 for both byte and word mode data transfers

DEFAULT MUX CONFIGURATION

Upon a reset or power up condition, the MUX will be set to the configuration states defined below:

* enable software handshake: no
* edit mode: disabled
* echoing: disabled
* terminate on single text terminator: disabled
* end on count: disabled
* end on count length: 252
* alert 1 read mode: disabled

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* transmission mode: full duplex
* backspace character: BS
* line delete character: DEL
* strip text terminator: enabled
* type of backspace: backspace echo
* echo CR-LF for a specified single text terminator: enabled
* send message after ENQ timeout: disabled
* echo single text terminator: disabled
* device X-ON/X-OFF handshake: disabled
* host X-ON/X-OFF handshake: disabled
* host ENQ/ACK handshake: disabled
* baud rate: 9600
* character length: 8 bits/character
* number of stop bits: 1
* parity: none
* host ENQ/ACK timer: 5 seconds
* host interrupt mask: all cleared to disable interrupts
* host X-ON character: DC1
* host X-OFF character: DC3
* device X-ON character: DC1
* device X-OFF character: DC3
* single text terminator for echoing CR-LF: CR
* host ENQ character: ENQ
* host ACK character: ACK
* host ENQ/ACK pacing counter: 80
* number of output separators: 2
* output separator characters: CR-LF

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* signal character detection: disabled
* do not terminate the text record on error: disabled
* quoting character mode: disabled
* conditional output separators appendage: disabled
* null character insertion into receive buffer for detected break: disabled
* replacement character for bad incoming character: DEL
* quoting character: \
* record separator to invoke sending output separators: LF
* signal character 1: 0FF hex
* signal character 2: 0FF hex
* signal character 3: 0FF hex
* signal character 4: 0FF hex
* quotable single text terminator character: EOT (Control-D)
* number of single text terminators: 1
* single text terminator character: CR

SUBFUNCTION ASSIGNMENT SUMMARY

A summary of all subfunction assignments is contained in the following paragraphs.

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Read Device Data

```
SUBFUNCTION = bit 7 - toggle character handshake
              bit 6 - toggle signal character detection
              bit 5 - toggle editing mode
              bit 4 - toggle echo
              bit 3 - toggle quoting mode
              bit 2 - reserved
              bit 1 - toggle single text termination mode
              bit 0 - reserved
```

These are in effect only for the duration of the request.

Write Device Data

```
SUBFUNCTION = bit 0 = 0 - no output separator appendage
                    = 1 - append output separators
```

```
SUBFUNCTION = 0 through 33 - see write card configuration

              249 - get receive buffer status

              250 - get the card RAM

              254 - get the card status
```

Write Card Configuration

```
SUBFUNCTION = 0 - configure subfunctions 1 through 32

              1 - configure the read option

              2 - end-on-count length

              3 - configure alert 1 mode

              4 - not used

              5 - transmission mode

              6 - backspace character

              7 - line delete character

              8 - other options
```


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9 - device handshake option

10 - baud rate

11 - character length

12 - number of stop bits

13 - parity

14 - not used

15 - not used

16 - not used

17 - not used

18 - character handshake timer

19 - not used

20 - not used

21 - host interrupt mask

22 - host X-ON/X-OFF characters

23 - device X-ON/X-OFF characters

24 - host ENQ/ACK characters

25 - host ENQ/ACK pacing counter

26 - not used

27 - single text terminator for echoing CR-LF

28 - output separator

29 - not used

30 - not used

31 - additional options

32 - single text terminator

33 - card write register

34 - set port ID

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Control Card

SUBFUNCTION = 0 - no operation

1 - flush the current receive buffer

2 - flush all the queued receive buffers

3 - flush all the queued transmit buffers

4 - host initiated frontplane receive text termination

5 - force restart of transmitter if waiting for handshake

6 - enter speed sense mode

7 - abort speed sense mode

8 - suspend transmitter

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MAINTENANCE

SECTION V

If the MUX card did not pass the self-test described in Section II, it is recommended that you return the card to Hewlett-Packard. If further testing is desired, however, a diagnostic test hood, which tests slightly more or the card's circuitry, can be ordered. The diagnostic test hood part number is 0950-1659.

To test the MUX card using the diagnostic test hood, perform the following:

1. Turn computer system power off.
2. Connect the test hood to connector J2 on the card.
3. Refer to the appropriate computer system manual to determine if the self-test is run automatically at power-on, or only when specifically invoked by you.
4. Turn on computer system power.
5. When the self-test executes, the LED located on the test hood and the LED located on the MUX card both should light briefly and go out if the card passed self-test. If the LEDs do not light at all, the card is defective. If the LEDs stay lit, the card did not pass self-test.

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE MUX CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR EXCHANGE OR REPAIR BY HEWLETT-PACKARD COMPANY. If such service is performed, the replaceable parts information in Section VI and the schematic logic diagrams in Section VII will be of assistance.

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REPLACEABLE PARTS

SECTION VI

This section contains information for ordering replaceable parts for the MUX card. Table 6-1 contains a list of replaceable parts, table 6-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 6-1, and figure 6-1 shows the locations of the parts on the MUX card.

REPLACEABLE PARTS

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 6-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

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To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Section 2).

2. Description and function of the part.

3. Quantity required.

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Table 6-1. HP 27130A Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	5061-4929	5	1	PCA-mrIO MUX	28480	5061-4929
C1	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C2	0160-4832	4	16	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0180-0100	3	1	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C7	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C8	0160-4835	7	8	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4807	3	2	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C11	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C21	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C28	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C30	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
CR1	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR2	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
CR3	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
CR4	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
F1	2110-0297	4	3	FUSE .5A 125V NTD .281X.093	28480	2110-0297
F2	2110-0297	4		FUSE .5A 125V NTD .281X.093	28480	2110-0297
F3	2110-0297	4		FUSE .5A 125V NTD .281X.093	28480	2110-0297
J1	1251-7276	0	1	CONN-POST TYPE .100-PIN-SPCG 80-CONT	28480	1251-7276
	1251-8205	7	1	CONN-HDR-72 PIN	28480	1251-8205
J2A	1251-7006	4	2	CONNECTOR 16-PIN M POST TYPE	28480	1251-7006
J2B	1251-8206	8	1	CONN-HDR-40 PIN	28480	1251-8206
J2C	1251-7006	4		CONNECTOR 16-PIN M POST TYPE	28480	1251-7006
Q1	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
R1	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R2	1810-0278	4	2	NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R3	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R4	0698-3447	4	2	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R5	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R6	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R8	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R9	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0698-4590	0	1	RESISTOR 422 1% .25W F TC=0+-100	24546	C5-1/4-T0-422R-F
R12	1810-0517	4	2	NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R13	1810-0517	4		NETWORK-RES 10-SIP6.0K OHM X 9	28480	1810-0517
R14	0757-0199	3	4	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R15	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R16	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R17	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R18	1810-0278	4		NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R19	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
U11	1820-2862	7	2	IC-DS 3667	28480	1820-2862
U12	1820-2862	7		IC-DS 3667	28480	1820-2862
U13	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U14	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U15	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U22	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U23	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U24	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U25	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U34	1810-0649	3	1	NTWK-SHUNT-PRGM	28480	1810-0649

See introduction to this section for ordering information
*Indicates factory selected value

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Table 6-1. HP 27130A Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U35	1820-0684	7	1	IC INV TTL S HEX 1-INP	01295	SN74S05N
U41	1820-2975	3	1	IC-BIC C2000	28480	1820-2975
U43	1820-2300	8	4	IC-Z80A SIO/2	28480	1820-2300
U45	1820-1645	2	1	IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
U51	1820-2301	9	3	IC-Z80A CTC	28480	1820-2301
U53	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U55	5180-0121	3	8	BURNIN 1818-1425	28480	5180-0121
U61	1820-2301	9		IC-Z80A CTC	28480	1820-2301
U63	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U65	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
U71	1820-2301	9		IC-Z80A CTC	28480	1820-2301
U73	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U75	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
U82	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
U83	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U84	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U85	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
U92	1820-2594	2	2	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U93	1820-2117	5	4	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U94	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U95	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
U96	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U97	1820-2831	0	2	ICD 75174 DRIVER	28480	1820-2831
U98	1820-2831	0		ICD 75174 DRIVER	28480	1820-2831
U102	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U103	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U104	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U105	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
U115	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
U125	5180-0121	3		BURNIN 1818-1425	28480	5180-0121
X1	1200-0539	7	1	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
X1	1810-0648	2	1	NTWK-SHUNT-PRGM	28480	1810-0648
X33	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
X34	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
X54	1200-1062	3	1	SKT-64 PIN SQ	28480	1200-1062
X64	1200-0567	1	2	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
X74	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	1820-2649	8	1	IC- Z80B-CPU	28480	1820-2649
	1820-2995	7	1	IC GATE-ARY CMOS	28480	1820-2995
	5041-3467	2	2	HPID EXTR HNDL	28480	5041-3467
	5180-1969	9	1	PCB-HPID MUX	28480	5180-1969

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*Indicates factory selected value

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Table 6-2. Manufacturer's Code List

MFR NO.	MANUFACTURER'S NAME	ADDRESS	ZIP CODE
01121	Allen-Bradley Company	Milwaukee, Wi.	53204
01295	Texas Instruments, Inc. Semiconductor Components Div.	Dallas, Tx.	75222
07263	Fairchild, Semiconductor Div.	Mountain View, Ca.	94042
24546	Corning Glass Works (Bradford)	Bradford, Pa.	16701
28480	Hewlett-Packard Co. Corporate HQ	Palo Alto, Ca.	93404
56289	Sprague Electric Co.	North Adams, Ma.	01247

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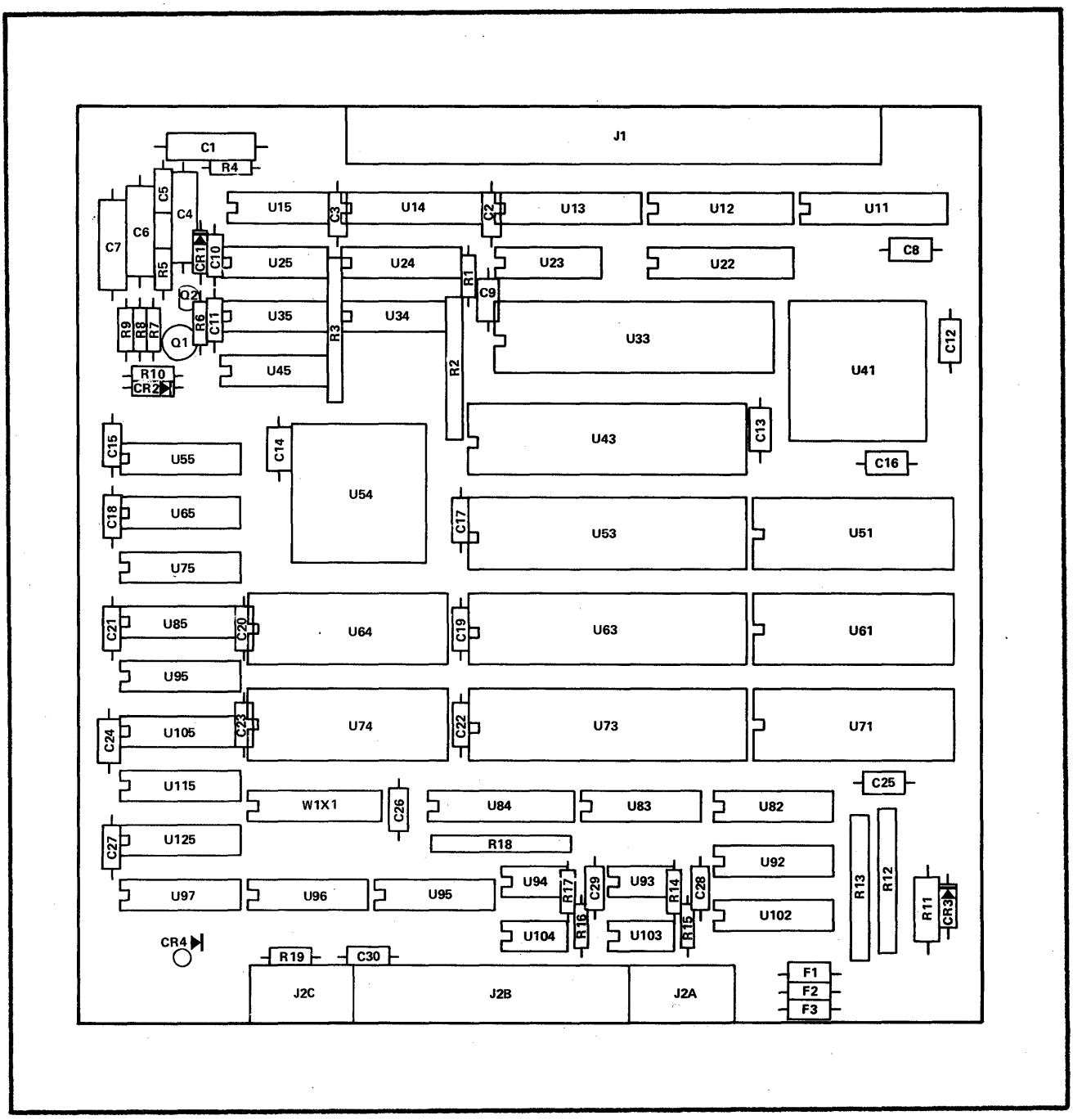


Figure 6-1. HP 27130A Parts Location Diagram

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SCHEMATIC DIAGRAMS

SECTION VII

This section contains schematic logic diagrams for the MUX card.

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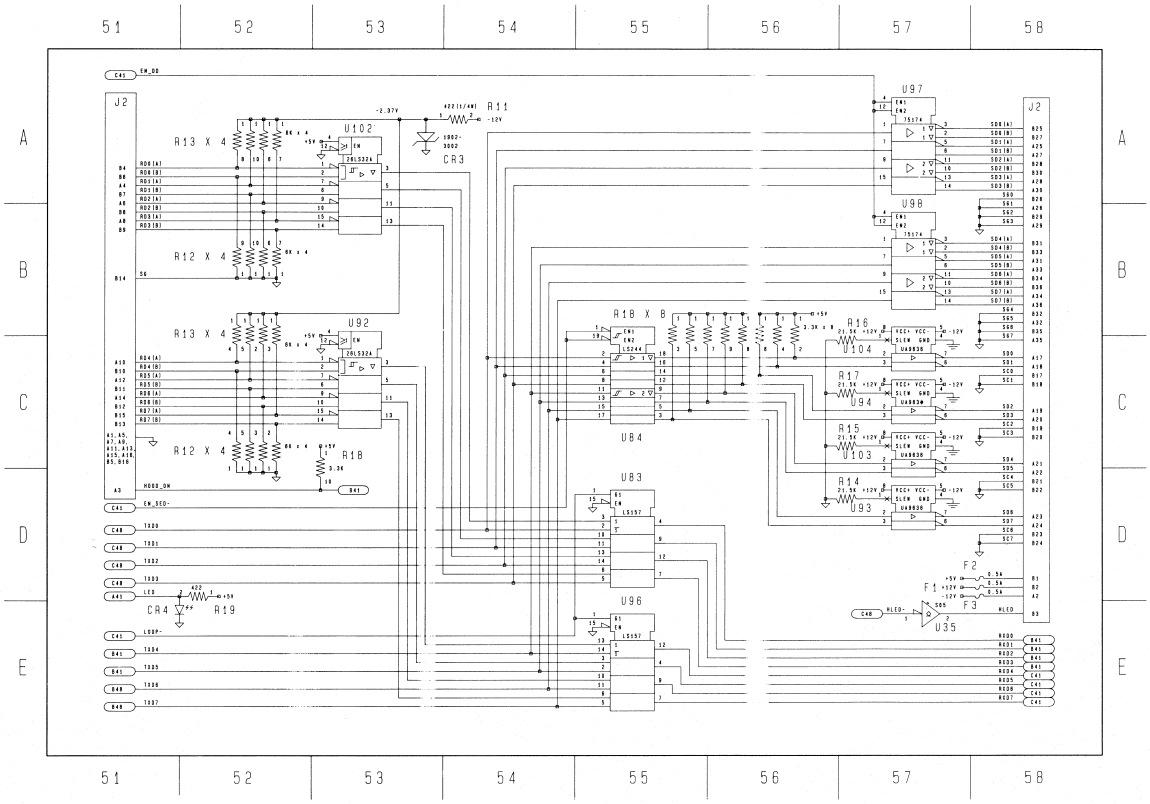


Figure 7-1. MUX Schematic Logic Diagram (Sheet 1 of 5)

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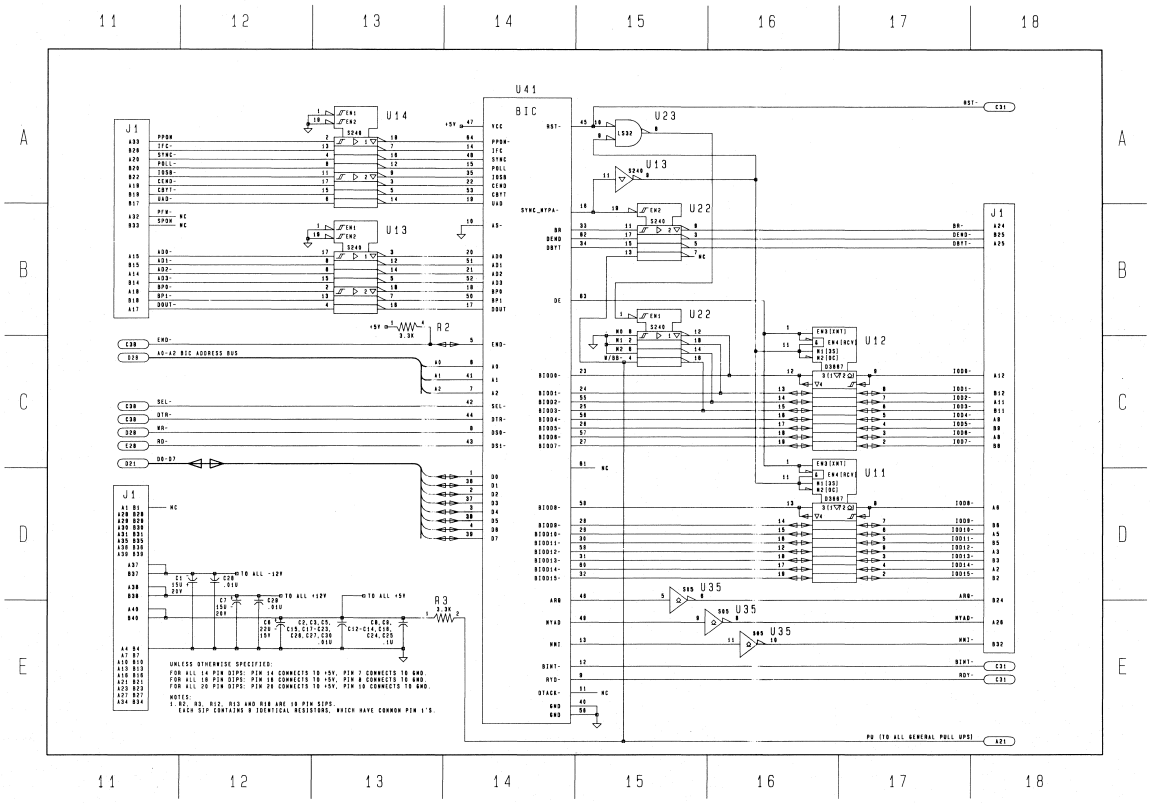


Figure 7-1. MUX Schematic Logic Diagram (Sheet 2 of 5)

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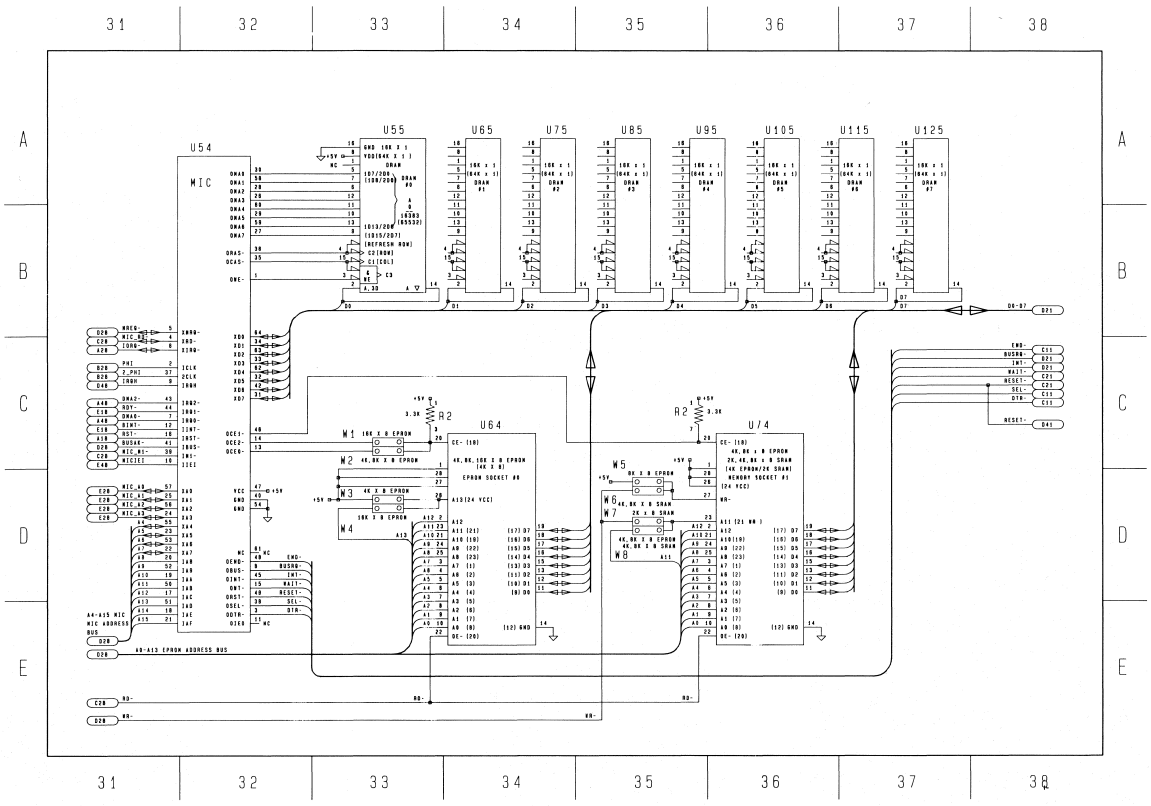


Figure 7-1. MUX Schematic Logic Diagram (Sheet 3 of 5)

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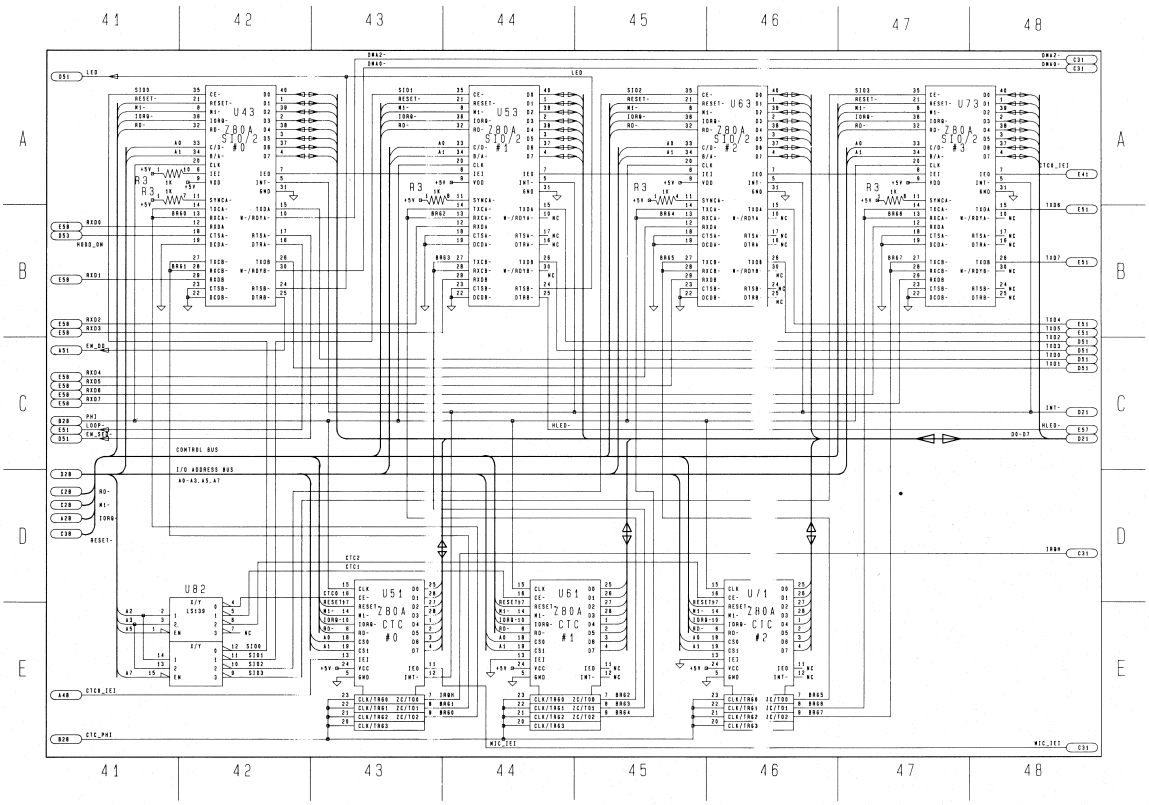


Figure 7-1. MUX Schematic Logic Diagram (Sheet 4 of 5)

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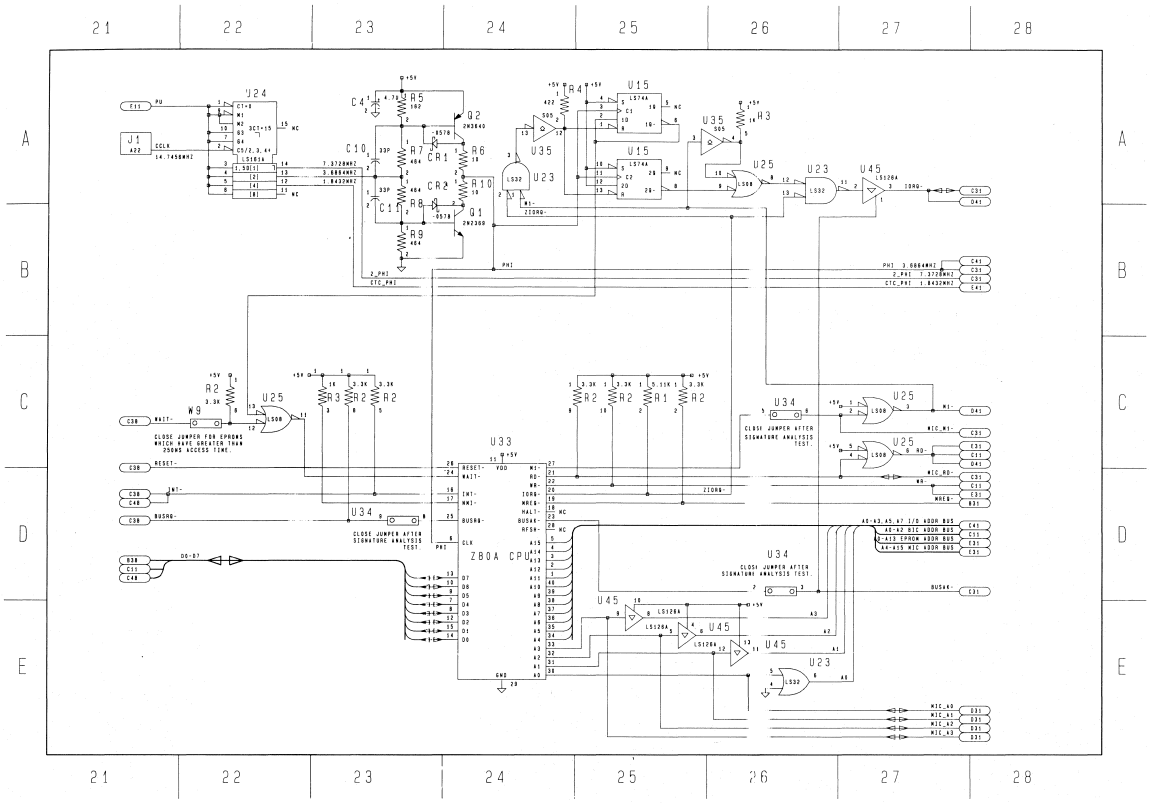


Figure 7-1. MUX Schematic Logic Diagram (Sheet 5 of 5)

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ASCII CHARACTERS AND BINARY CODES

APPENDIX

A

	0	1	2	3	4	5	6	7
0	NUL	DLE	sp	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3		3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

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INDEX

A

Additional options, 4-16
Address space, 3-6
Alert 1 read mode, 4-9
Appending automatic output separators, 4-12
Asynchronous events, 4-19
Automatic output separators, 4-12

B

Backplane interface circuit, 3-19
Backspace, 4-6
BIC, 3-19
Binary data, 4-11
Break detection, 4-15
Buffer flushing, 4-12

C

Cable, 1-3
Capabilities, alert 1 read mode, 4-9
    appending automatic output separators, 4-12
    appending conditional output separators, 4-18
    backspace, 4-6
    buffer flushing, 4-12
    device X-ON/X-OFF handshake, 4-8
    echoing, 4-10
    edit mode, 4-6
    end-on-count text termination, 4-9
    error handling, 4-16
    host ENQ/ACK handshake, 4-7

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INDEX

C (Continued)

host initiated text termination, 4-12
host X-ON/X-OFF handshake, 4-8
line deletion, 4-6
quoting character mode, 4-18
receive character processing, 4-4
receive error sensing, 4-5
signal character, 4-5
single text termination, 4-9
software handshake, 4-7
speed sense, 4-18
transmit character processing, 4-12
transmitting transparent or binary data, 4-12
type ahead, 4-10
Capabilities, 4-4
Checkout, 2-13
Conditional output separators appendage, 4-18
Configuration, default settings, 4-46
Connect Logical Channel (CLC) request format, 4-2
Connect Logical Channel request subfunction definitions, 4-21
Connection box, 1-3
Control card, request code - 6, 4-40
Control card subfunction, 4-51
Counter timer circuit, 3-19
CPU, 3-6
CTC, 3-19
Current requirements, 2-1

D

Default MUX configuration, 4-46
Description, 1-1
Device X-ON/X-OFF handshake, 4-8
Diagnostic hood, 3-28
Diagnostics, 4-20
Diagrams, parts location, 6-6

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E

Echoing, 4-10
Edit mode, 4-6
End-on-count text termination, 4-9
EPROM installation, 2-1
EPROMs, 1-3
Equipment supplied, 1-3
Error handling option, 4-16
Event block description, 4-42
Extension cable kit, 1-3

F

Firmware installation, 2-1
Functional description, 1-1, 3-1

H

Handshake timer, 4-15
Host ENQ/ACK handshake, 4-7
Host initiated text termination, 4-12
Host X-ON/X-OFF handshake, 4-8

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INDEX

I

I/O address space, 3-6
I/O cards, 1-1
I/O channel adapter, 1-1
I/O channel interface, 2-5
Identification, 1-3
Identity Information Block Definitions, 4-46
Installation, EPROM, 2-1
    firmware, 2-1
    manual, 1-4
    MUX, 2-12
Installing the MUX, 2-12
Interface, I/O channel, 2-5
    peripheral device, 2-5
    to the BIC, 3-19
    to the MIC, 3-24
Interrupt acknowledge, 3-27
Interrupt structure, 3-27

J

Jumpers, 2-3

L

Line deletion, 4-6

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M

Maintenance, 5-1
Manufacturer's code list, 6-5
Memory address space, 3-3
Memory configuration jumper, 2-3
Memory interface circuit, 3-24
Memory/processor bus, 1-1
MIC channel A lower byte of transfer byte count register, 3-26
MIC Channel B lower byte of transfer byte count register, 3-25
MIC configuration register, 3-24
MIC DMA A configuration register, 3-26
MIC DMA A I/O port address register, 3-26
MIC DMA A lower byte of memory address register, 3-25
MIC DMA A upper byte of memory address register, 3-25
MIC DMA B configuration register, 3-24
MIC DMA B I/O port address register, 3-25
MIC DMA B upper byte of memory address register, 3-24
MIC interrupt vector register, 3-26
Microprocessor, 3-6
MIC, Register 0, 3-24
    Register 1, 3-24
    Register 2, 3-24
    Register 3, 3-24
    register 4, 3-25
    register 5, 3-25
    register 6, 3-25
    register 7, 3-25
    register 8, 3-26
    register 9, 3-26
    register A, 3-26
    register B, 3-26
MPB, 1-1

O

Ordering parts, 6-1

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INDEX

P

Parity in transmitted or received data, 4-15
Parts location diagram, 6-6
Parts, ordering, 6-1
    replaceable, 6-1
Peripheral device interface, 2-5
Physical description, 1-1
Power requirements, 2-1
Printed circuit card, 1-3
Priority interrupt structure, 3-27
Programmable features, 4-1
Programming the receiver and transmitter, 4-13

Q

Quoting character mode option, 4-18

R

RAM installation, 2-1
Read card information subfunction, 4-49
Read card information write control request, 4-23
Read device data subfunction, 4-49
Read device data write control request, 4-22
Read request length, 4-11
Read status request, 4-44
Receive character processing, 4-4
Receive error conditions, 4-5
Receiver programming, 4-13
Receiving binary data, 4-11

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R (Continued)

Receiving transparent data, 4-11
Register 0, 3-24
Register 1, 3-24
Register 2, 3-24
Register 3, 3-24
Register 4, 3-25
Register 5, 3-25
Register 6, 3-25
Register 7, 3-25
Register 8, 3-26
Register 9, 3-26
Register A, 3-26
Register B, 3-26
Repair, 5-1
Replaceable parts, 6-1
Reshipment, 2-14
RTS and WTC block definitions, 4-41

S

Serial I/O Controller, 3-6
Service, 5-1
Signal character, 4-5
Signature analysis jumper, 2-3
Single text termination, 4-9
SIO/2, 3-6
Software handshake, 4-7
Solicited events, 4-19
Specifications, 1-4
Speed sense capability, 4-18
Subfunction assignment summary, 4-48
Subfunction definitions, 4-21

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S (Continued)

Subfunctions, 0 through 33, 4-23
0, 4-25
1 - configure read option, 4-28
2 - end-on-count length, 4-29
3 - alert 1 read mode, 4-29
5 - transmission mode, 4-30
6 - backspace character, 4-30
7 - line delete character, 4-30
8 - backspace and other options, 4-31
9 - device handshake option, 4-32
10 - baud rate, 4-33
11 - character length, 4-33
12 - number of stop bits, 4-34
13 - parity, 4-34
18 - character handshake timer, 4-35
21 - host interrupt mask, 4-35
22 - host X-ON/X-OFF characters, 4-36
23 - device X-ON/X-OFF characters, 4-37
24 - host ENQ/ACK characters, 4-37
25 - host ENQ/ACK pacing counter, 4-37
27 - single text terminator for echoing CR-LF, 4-37
28 - output separator, 4-37
31 - additional options, 4-38
32 - single text terminator, 4-39
33 - card write register, 4-39
34 - set port ID, 4-40
249 - read data status, 4-23
250 - get card RAM, 4-23
254 - get card status, 4-24
control card, 4-51
read card information, 4-49
read device data, 4-49
summary, 4-48
write card configuration, 4-49
write device data, 4-49
System clocks, 3-3

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T

Theory of operation, 3-1
Timer, 4-15
Transactions, 4-2
Transmit character processing, 4-12
Transmitter programming, 4-13
Transmitting binary data, 4-12
Transmitting transparent data, 4-12
Transparent data, 4-11
Type ahead, 4-10

W

Wait state circuits for interrupt acknowledge, 3-27
Write card configuration, request code = 5, 4-25
Write card configuration subfunction, 4-49
Write control requests, read card information, 4-23
read device data, 4-22
write device data, 4-22
Write device data subfunction, 4-49
Write device data write control request, 4-22

Z

Z-80B CPU, 3-6

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