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# GPIO Interface

## Technical Data

**For HP 9000 Series 300 Computer Systems**
**Product Number**
**HP 98622A**

The HP 98622A General Purpose I/O (GPIO) Interface is a flexible parallel interface that will send and receive up to 16 bits of data to a variety of devices. Several handshake modes are available to permit interfacing to a variety of equipment. Extended control and status lines are available for applications that require transferring control and status information outside the data path.

### Features

- 16 latched input lines
- 16 latched output lines
- Selectable handshake modes
- 10 handshake, control, and status I/O lines
- DMA compatibility for fast transfers
- Configurable data-in clock source
- Connections for flexible disk drive, multiprogrammer, or thermal printer interrupt capability

**Sample of Transfer Rates** *Table 1*

| | Input (bytes/s) | Output (bytes/s) |
|---|---|---|
| **BASIC 2.0** | | |
| Handshake | 63 K | 65 K |
| **BASIC Advanced Program Binary Capability** | | |
| Interrupt, burst | 65 K | 75 K |
| Fast handshake | 115 K | 115 K |
| DMA, regular | 540 K | 480 K |
| DMA, burst | 770 K | 670 K |
| **HPL 2.0** | | |
| Interrupt | 8 K | 8 K |
| Fast read/write | 89 K | 100 K |
| DMA, regular | 540 K | 480 K |
| DMA, burst | 770 K | 670 K |

### Functional Specifications

#### Maximum Transfer Rates

The sample of transfer rates in table 1 are the maximum rates that can be attained with the type of data transfer specified. Any delay generated by the peripheral or by additional program statements or options will cause the actual data transfer rate to be lower.

#### Data, Status, Control Lines

The 16 output lines provide high current/voltage drivers using open-collector buffers. Either positive- or negative-true logic is selectable. The 16 input lines are terminated by a resistive divider of 3 kW to +5 V and 62 kW to ground accepting standard TTL signal levels. Ten lines provide control, status, and handshake information between the peripheral and the GPIO Interface.

### Status and Control Lines Definitions

**PCTL Peripheral Control**
Handshake output, driven by interface; indicates the computer is ready for input data or new output data is available on output lines. PCTL is reset by a ready-to-busy transition on PFLG or by an interface reset.

**PFLG Peripheral Flag**
Handshake input, driven by peripheral; indicates the peripheral has completed the data transfer; also used to request peripheral interrupt when enabled.

**PSTS Peripheral Status**
Status input, driven by peripheral; indicates to the computer the readiness of the peripheral. PSTS is sampled by the computer whenever communication with the peripheral is requested.

**ST10, ST11 Extended Status**
Status input, driven by peripheral; sensed by computer; may be used for any purpose; examined by reading the HP 98622A peripheral status register.

**CTL0, CTL1 Extended Control**
Control output, driven by computer; sensed by the peripheral; may be used for any suitable purpose by the user; asserted by writing to the HP 98622A peripheral control register.

**I/O Direction**
Handshake output, driven by card; indicates to the peripheral the direction of type current data transfer.

**PRESET Peripheral Reset**
Control output, driven by card; used to initialize a peripheral when the computer is turned on, when the RESET key or CLEAR I/O key is pressed, or when the HP 98622A peripheral reset register is written to.

**EIR External Interrupt Request**
Control output, driven by peripheral; used to generate an interrupt request based on some external event or termination of a DMA buffer transfer. The current state can be examined by reading the HP 98622A peripheral status register. The interrupt is level detected, not edge sensitive. EIR should be held low until the interrupt is serviced.

## Electrical Characteristics
(See table 2.)

### DMA Capability

The HP 98622 can carry out DMA transfers via the optional two-channel HP 98620A DMA controller card. Word or Byte Mode as well as Regular or Burst DMA transfers are supported. The burst feature allows a higher data transfer rate and a shorter latency time.

### Interrupt Capability

Proper interrupt level settings allow a higher level request to interrupt a lower level data transfer. The HP 98622A is capable of generating interrupts to the computer under the following conditions:

- PCTL clear
- PCTL clear & PFLG ready
- EIR asserted

**Electrical Characteristics** *Table 2*

| | Minimum | Maximum |
|---|---|---|
| **Data Output and Control Output Lines** | | |
| Output Low Voltage @ 16 mA | | 0.4 V |
| Output Low Voltage @ 40 mA | | 0.7 V |
| Output High Voltage (open collector) | | 30.0 V |
| Output Low Current | | 40.0 mA |
| Output High Current @ Output High Voltage | | 0.25 mA |
| **Data Input Lines** | | |
| Input Low Voltage | | 0.7 V |
| Input High Voltage | 3.0 V | |
| Input Current @ Input Low Voltage = 0.4 V | | -2.3 mA |
| **Control Input Lines** | | |
| Input Low Voltage | | 0.5 V |
| Input High Voltage | 3.0 V | |
| Hysteresis | 0.4 V | |
| Input Low Current @ Input Low Voltage = 0.4 V | -3.3 mA | |

**Switched Configuration**

**Select Code**: The factory select code setting is 12; valid select codes are:

| | |
|---|---|
| HPL | 1-6, 8-15 |
| Pascal & BASIC | 8-31 |

**Interrupt Level**
The factory setting is 3; a valid interrupt level setting is from 3 to 6.

**Output Data Line Sense**
A 1-bit switch allows the input data lines to use either positive-true or negative-true logic even with fast read/write and DMA transfers.

**PFLG Line Sense**
A 1-bit switch allows the peripheral flag line to use either positive-true or negative-true logic.

**PCTL Line Sense**
A 1-bit switch allows the peripheral control line to use either positive-true or negative-true logic.

**PSTS Line Sense**
A 1-bit switch allows the peripheral status line to use either positive-true or negative-true logic.

**Handshake Mode**
A 1-bit switch allows selection of full or pulsed handshake mode.

**Data-In Clock Source**
A 6-bit switch allows selection of 3 different clocking transitions for input data. The upper input byte (8 lines) and lower input byte (8 bits) can have separate clock sources. The input bytes can be clocked when the register is read, on the ready-to-busy transition of PFLG, or on the busy-to-ready transitions of PFLG.

## Ordering Information

**Earliest Language Version Required**: BASIC 1.0, HPL 1.0, Pascal 1.0

**The HP 98622A includes:**

**98622-66501** General Purpose I/O Card
**98622-90000** Installation Manual

**HP 98622A Options:**

| | |
|---|---|
| **001** | 4.6-meter (15 ft) unterminated cable (5061-4209) |
| **003** | 4.6-meter (15 ft) terminated cable for HP 6940A/B Multiprogrammer (98622-66504, 50-pin, male connector) |

**Fuse for Replacement/Spare:** 2110-0712

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