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HP 98622A
GPIO Interface Installation

Manual Part No. 98622-90000



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Table of Contents

Chapter 1: General Information

Introduction 1-1
About This Manual 1-1
About the HP 98622 GPIO Interface 1-1
Technical Specifications 1-2
Options 1-3
Optional Peripheral Configurations 1-3
Handling the Interface Card 1-3

Chapter 2: Installation

Introduction 2-1
Configuring the Interface Card 2-1
Select Codes 2-1
Interrupt Levels 2-2
Data-In Clock Source 2-3
Read 2-3
Busy 2-3
Ready 2-3
Option Select 2-3
Jumper Configurations 2-4
DOUT CLEAR Jumper 2-4
BURST Jumper 2-4
PCTL Delay Adjustment 2-5
Increasing PCTL Delay 2-6
Time Delay Increase Formula 2-6
Decreasing PCTL Delay 2-8
Time Delay Decrease Formula 2-8
Interface Cables 2-11
Cable Preparation 2-11
Data Input Lines 2-12
Recommended Driver Circuits 2-12
Driver Specifications 2-13
Data Output Lines 2-14
Recommended Receiver Circuits 2-14
Receiver Specifications 2-15
Peripheral Information Lines 2-16
Peripheral Control Line 2-16
Peripheral Flag Line 2-16
Transferring Data 2-16
Handshake Mode 2-17
Peripheral Status Line 2-17
Extended Status Input Lines 2-17
Extended Control Output Lines 2-17

Input/Output Direction Control Line 2-17
Peripheral Reset Line 2-18
External Interrupt Request Line 2-18
Installing the Interface Card 2-22

Appendix A

Configuring 98622 Cards to Match 98032 Cards A-1

Appendix B

Replaceable Parts B-2

Figures

2-1 Select Code Switch 2-2
2-2 Interrupt Level Switch 2-2
2-3 Data-In Clock Source Switch 2-3
2-4 Option Select Switch 2-4
2-5 Jumper Locations and Pinouts 2-5
2-6 Selecting PCTL Delay Capacitor 2-7
2-7 Full Mode Timing Diagram 2-9
2-8 Pulse Mode Timing Diagram 2-10
2-9 Preparing the Interface Cable 2-11
2-10 Recommended Peripheral Driver Circuit 2-13
2-11 Recommended Peripheral Receiver Circuit 2-15

Tables

1-1 98622A Available Options 1-3
1-2 Option Interface Configuration 1-3
2-1 Interrupt Level Switch 2-2
2-2 Option Select Switch 2-4
2-3 Data Input Lines 2-12
2-4 Data Output Lines 2-14
2-5 Peripheral Information Lines 2-18
B-1 GPIO Board Parts B-2



Chapter 1
General Information

Introduction

About This Manual

This manual provides all the installation information required for the HP 98622A GPIO Interface. This information is presented in two chapters. Chapter 1 provides general information about the interface including an overview of the interface, technical specifications and available options.

Chapter 2 provides installation instructions for the interface including switch and jumper configurations. It also includes information for selecting the proper timing capacitor for various cable lengths. Pinout diagrams for the interface cable are provided to help you configure the peripheral.

About the HP 98622A GPIO Interface

The HP 98622A GPIO Interface contains all the circuitry required to provide a 16-bit bi-directional data exchange between the computer and a compatible peripheral. The GPIO Interface transfers data in a "full-duplex" mode. That is, it can have data on the output lines and be receiving data on the input lines at the same time.

Various switch and jumper configurations allow you to configure the Interface to meet a wide variety of peripheral requirements. Such parameters as data-in clock source, interface select code, selectable logic sense of: the data in, the data out or the various handshaking lines by setting switches on the interface printed circuit board. Burst enable and DOUT clear are available by using or deleting the appropriate jumpers on the board.

The Interface is shipped from the factory either as a Standard Interface (with no cable) or as an Option Interface (with a cable). The Option Interface is preconfigured for operation with a given peripheral (e.g., Option 004 which is configured for a 7.5 foot cable for the HP 9866 Printer). The Standard Interface needs to be configured to meet your peripheral's requirements.

Technical Specifications

The following list details the specifications for the GPIO Interface. It lists the parameters required for the peripheral drivers and receivers. Refer to Chapter 2 for a more detailed description of the various lines and their function.

Data Input Lines:	16 latched lines: DI0 thru DI15
Termination:	Resistive divider of 3 kohms to +5 V, 6.2 kohms to ground
Receiver Logic:	Exclusive OR
Input Voltage:	
Logic Low	0.8 V maximum
Logic High	2.0 V minimum
Input Current:	
Logic Low	0.8 mA (maximum) at 0.4 V
Logic High	40 μa at 2.7 V
User Logic:	Positive-or negative-true (selective via hardware or software)
Status and Handshake Input Lines:	PFLG, PSTS, STI0, STI1 (Same specs as Data Input)
Data Output Lines:	16 latched lines: DO0 thru DO15
Driver Logic:	Open collector
Output Voltage:	
Logic Low	0.4 V at 16 mA, 0.7 V at 40 mA.
Logic High	30 V maximum
User Logic:	Positive-or negative-true
Handshake and Control Output Lines:	PCTL, I/O , CTL0 , CTL1 , PRESET, EIR
Termination:	Resistive divider of 3 kohms to +5 V, 3.1 kohms to ground
Receiver Logic:	Schmitt Trigger
Input Voltage:	
Logic Low	0.6 V maximum
Logic High	1.9 V minimum
Input Current:	
Logic Low	−0.4 mA (maximum) at 0.4 V
Logic High	40 μa at 2.7 V

Options

Presently, there are four options available for the HP 98622A GPIO Interface. Table 1-1 lists all four options. All the options concern available cable lengths, types of cables and terminating connectors.

Table 1-1. 98622A Available Options

Option	Part No.	Description
001	5061-4209	4.6 M (15 ft) unterminated cable
002	5061-4211	0.8 M (2.5 ft) cable for 9885M disc
003	98622-66503	4.6 M (15 ft) cable for 6940B Multiprogrammer
004	5061-4212	4.6 M (7.5 ft) cable for 9866 printer

Optional Peripheral Configurations

Table 1-2 provides Interface configuring information for use with the optional HP peripherals. Refer to Chapter 2 for a description of the various lines and switch locations.

An "0" in any column means set that switch to "logic 0" – all other switches should be set to "logic 1".

Table 1-2. Option Interface Configuration

HP Model No.	PCTL	PFLG	PSTS	HSHK	DIN	DOUT	RD	BSY	RDY	RD	BSY	RDY
69401	1	0	0	1	1	1	0	1	1	0	1	1
9866	1	0	1	1	1	1	1	1	1	1	1	1
9885	1	1	1	1	1	1	1	0	1	1	0	1

Handling the Interface Card

As with all integrated circuit boards, do NOT handle the boards in a statically charged atmosphere. A static discharge can damage the ICs. Do NOT handle the board by the edge connector. Fingerprints can cause a bad connection when the board is plugged into the computer.

Notes

Chapter 2
Installation

Introduction

This chapter provides information concerning the installation of the GPIO Interface. A major part of the installation procedure is configuring the Interface to the peripheral. This chapter includes information for setting the select code, the interrupt level, the data-in clock source, and selecting the proper option (inverted/non-inverted data and/or handshake lines).

Configuring information also includes proper jumper selection and timing capacitor selection for the various interface cable lengths. Additional information includes pinout tables of the interface cables, receiver and driver circuits for the peripheral data lines, required handshake lines and a procedure for testing the Interface.

Configuring the Interface Card

There are four switches, mounted on the PC board, which can be set by the user. These switches allow the user to set the select code of the interface, the interrupt level, the data-in clock source, and inverted/non-inverted data and/or handshaking lines, and to select between full or pulsed mode of handshake.

Interface Select Codes

Each interface card has a unique code by which it can be selected by the computer software. The actual interface select code varies depending on the language of the operating system installed in the computer. Refer to the "I/O Programming" manual for the language installed in your computer for the correct select code for your application.

Generally, select codes 1 thru 6 are reserved for internal use by the computer (e.g., display, keyboard, etc.). Select code 7 is reserved for the built-in HP-IB interface. Depending on the language installed, select codes 8 and above can be used by interface cards.

For most installations, select code 12 will be used for the GPIO Interface. All GPIO Interface cards are shipped from the factory preset to select code 12. If your system requires a different select code, change the select code switch shown in Figure 2-1 to the proper value.

Note

When assigning an interface to a select code other than the preset code, check the select code assignments for the other interface cards. Do not assign the same select code to more than one interface.

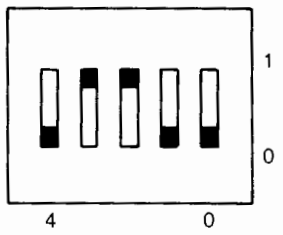


Figure 2-1. Interface Select Code Switch

Interrupt Level

The interrupt level switch (see Figure 2-2) sets the hardware priority level of the interrupt for the GPIO Interface. Interrupt levels 1 and 2 are reserved for internal use, while interrupt levels 3 thru 6 are available for the interfaces. Interrupt level 3 is the lowest priority with level 6 representing the highest priority. This allows a higher level request to interrupt a lower level data transfer.

Unlike the interface select code, all interfaces can be set to the same hardware interrupt level. As with the other interfaces, the GPIO Interface is factory preset to interrupt level 3. When the operating system encounters two or more interfaces set to the same interrupt level, they are handled on a first-come first-served basis. Simultaneous requests are handled by the operating system according to the program's software priority structure.

Use Table 2-1 to set the interrupt level switch:

Table 2-1. Interrupt Level Switch Settings

Interrupt Level (Hardware Priority)	Switch Setting 1	0
3	0	0
4	0	1
5	1	0
6	1	1

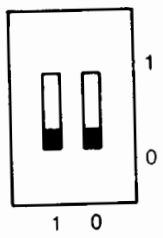


Figure 2-2. Interrupt Level Switch Setting Default

Data-In Clock Source

The sixteen data input lines are divided into two 8-bit bytes. The lower byte consists of data input lines DI0 thru DI7. The upper byte consists of data input lines DI8 thru DI15. Data-in clocking is selectable from any of three clock sources for both upper and lower bytes.

Figure 2-3 shows the Data-In Clock Source Switch. The right side of the switch selects the clock source for the lower byte. The left side selects the clock source for the upper byte. Closing any switch (logic 0) selects that source as the data-in clock source. See Figures 2-7 and 2-8 for timing diagrams.

Note

Select only one clock source (logic 0) for each byte. Selecting more than one source will cause improper operation.

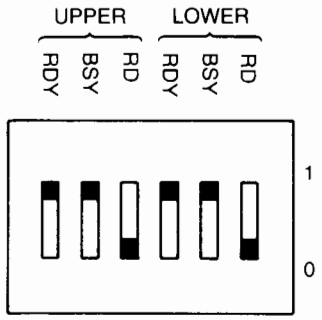


Figure 2-3. Data-In Clock Source Switch

The following paragraphs describe the three clocking transitions which can be selected to transfer data. The descriptions are applicable to either upper or lower byte.

RD. This mode causes the data to be clocked into the data input register when the register is read. It accomplishes this by clocking the register on the leading edge of the output enable signal of the register.

BSY. This mode clocks the data into the data input register when the PCTL line is cleared by a ready-to-busy transition on the PFLG line.

RDY. This mode clocks the data into the data input register on the busy-to-ready transition of the PFLG line. However, this transition **does not** clear the PCTL line; it is always cleared by the ready-to-busy transition of PCTL.

Option Select

Depending on the application (or peripherals) you will want to select either positive or negative true logic. As a user/programmer you have six options available for selecting positive or negative logic. Table 2-2 lists the six options in the same order as they are selectable by the Option Select Switch (see Figure 2-4). See Figures 2-7 and 2-8 for the timing relationship between these lines.

Table 2-2. Option Select Switch

Switch Position Name	DOUT	DIN	HSHK	PSTS	PFLG	PCTL
Function	Invert Data Out	Invert Data In	Full/Pulse Handshake	Invert PSTS	Invert PFLG	Invert PCTL
Logic 1 (Switch Open)	Low = 1	Low = 1	Full	Low = $\overline{OK}$	Low = Rdy	Low = Set
	High = 0	High = 0		High = OK	High = Bsy	High = Clr
Logic 0 (Switch Closed)	Low = 0	Low = 0	Pulse	Low = OK	Low = Bsy	Low = Clr
	High = 1	High = 1		High = $\overline{OK}$	High = Rdy	High = Set

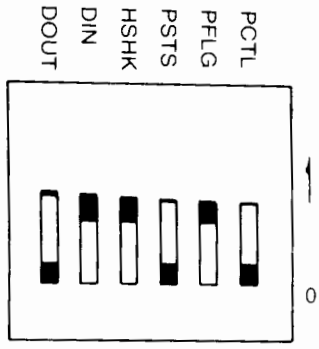


Figure 2-4. Option Select Switch

Jumper Configurations

DOUT CLEAR Jumper

Normally (no jumper), the contents of the data output registers are undefined at power up. They are also normally unchanged after an interface reset. With the DOUT CLEAR jumper installed, both data output registers (lower and upper) will be cleared at power up and after an interface reset.

Standard configuration from the factory is without the jumper. Install the jumper to add the DOUT CLEAR feature (see Figure 2-5).

BURST Jumper

The burst feature is used in conjunction with direct memory access (DMA). Normal operation (no DMA) is with the burst jumper installed (see Figure 2-5). Removing the jumper enables the burst feature.

The burst feature enables the direct memory access controller (DMAC) to hold the system bus for a short period of time following each DMA transfer to the interface. If the peripheral completes the data handshake during this time period, another DMA transfer can occur without the DMAC having to reacquire the system bus. This results in a higher data transfer rate and a shorter latency time.

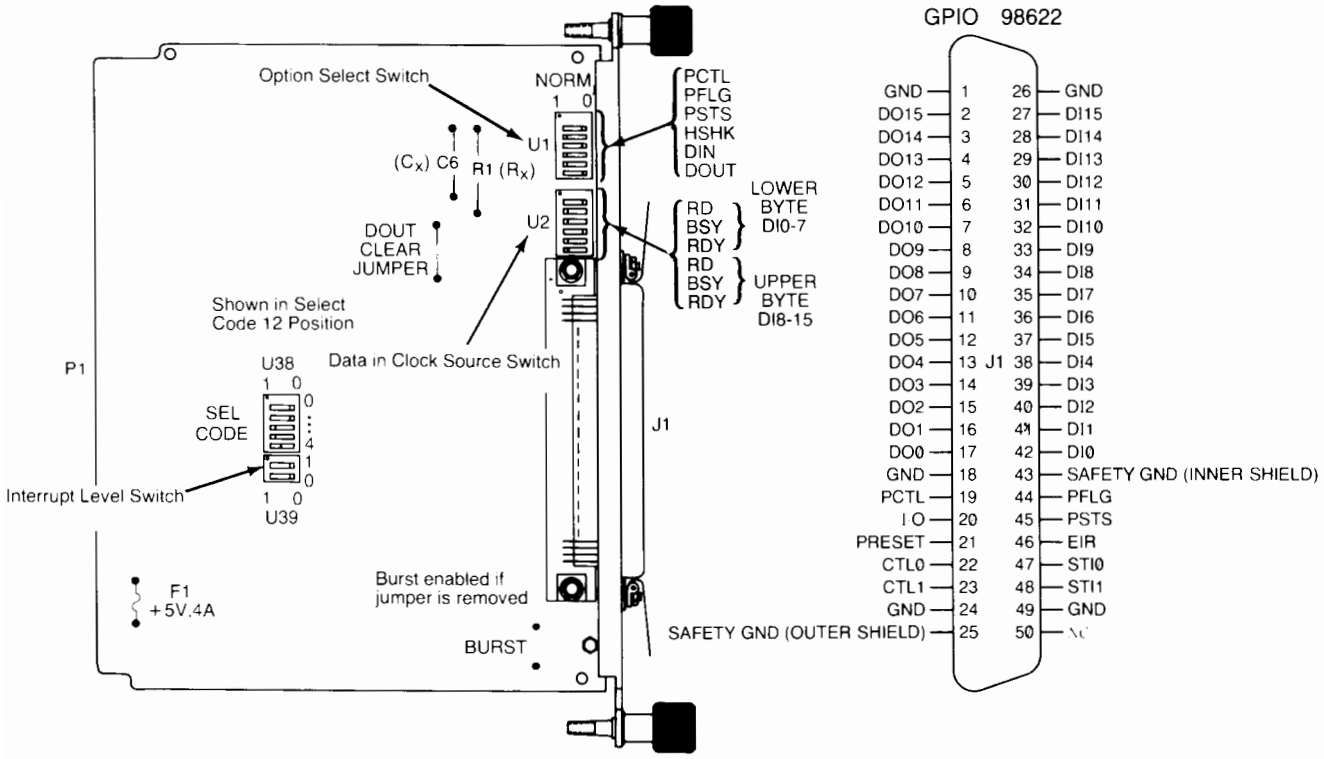


Figure 2-5. Jumper Locations and Pinouts

PCTL Delay Adjustment

In order to compensate for noise etc. on the input/output cable, the PCTL line has a built-in delay of approximately 250 ns. Depending on the application, it may be necessary to increase or decrease the amount of this delay. Figures 2-7 and 2-8 show the timing relationship between the PCTL line and the other peripheral information and control lines.

For DMA operation, PCTL is delayed for data output transfers only. For programmed transfers, PCTL is delayed for both input and output data transfers.

The following paragraphs describe how to set the PCTL delay.

Increasing PCTL Delay

When the interface is used in electrically noisy environments, or when extremely long cables are used, it may be necessary to increase the amount of output time delay to allow the data on the lines to settle. Adding a capacitor (Cx) increases this delay time.

Use the following formula to calculate the additional capacitance required to produce a desired time delay. Figure 2-6 graphically illustrates the relationship between capacitance and time delay. The location for physically attaching the capacitor to the interface board is shown in Figure 2-5.

Time Delay Increase Formula:

$$T_d = (C_f + C_x) \times .7R_f$$

where T_d = Time delay in seconds,
C_f = fixed capacitance (100 pF) in farads,
C_x = selected capacitance in farads
and R_f = fixed resistance (3.57 kΩ) in ohms.

Example: Determine the additional capacitance needed to produce a time delay of 350 ns.

Since $T_d = (C_f + C_x) \times .7R_f$,

$$C_x = \frac{T_d}{.7R_x} - C_f$$

$$= \frac{350 \text{ ns}}{.7 \times 3.57 \text{ k}\Omega} - 100 \text{ pF}$$

$$= 140 \text{ pF} - 100\text{pF}$$

$$= 40 \text{ pF}$$

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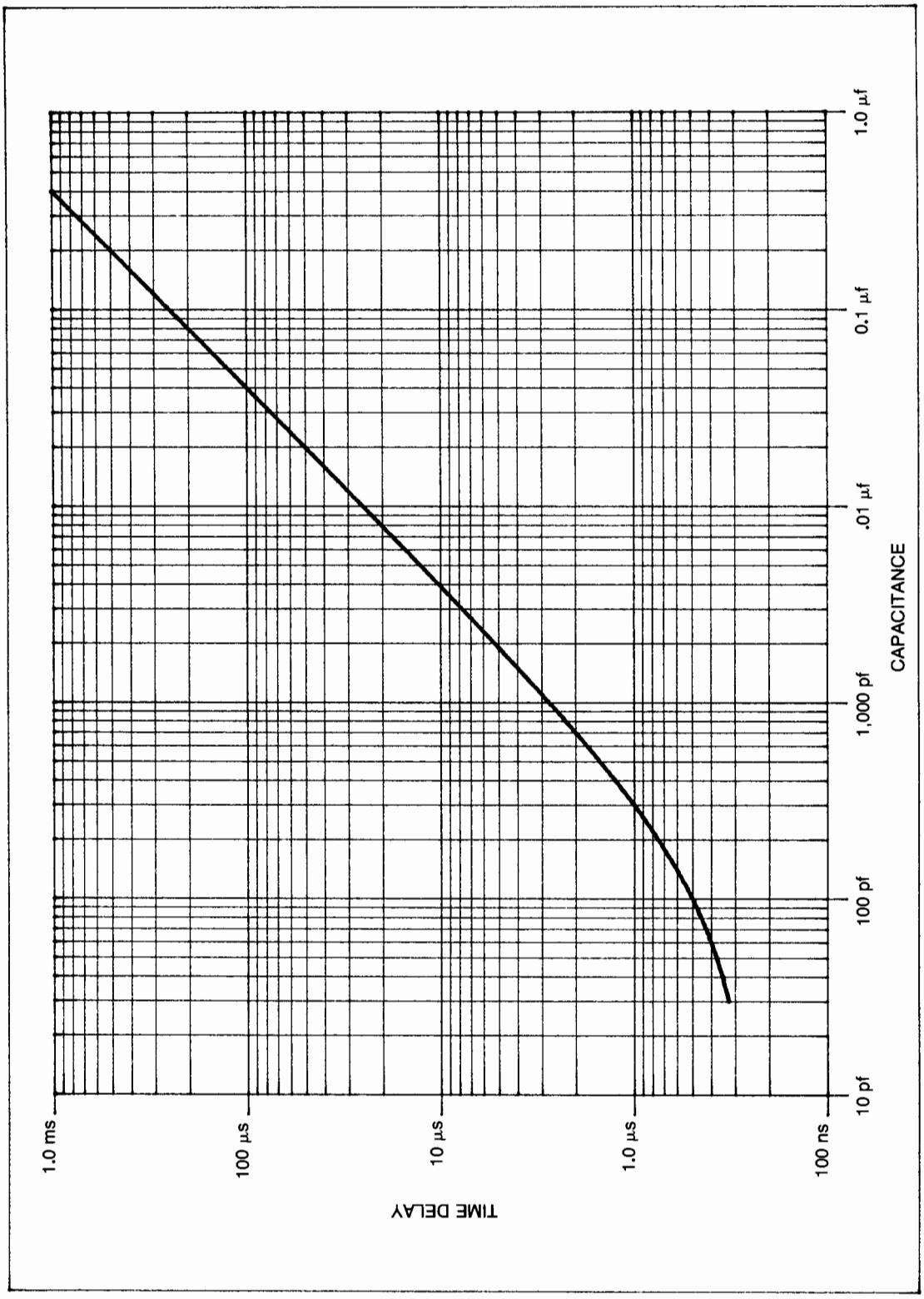


Figure 2-6. Selecting PCTL Delay Capacitor

Decreasing PCTL Delay

Occasionally, a system will require a delay of less than 250 ns. Adding a resistor (Rx) in parallel decreases the delay time.

Use the following formula to calculate the parallel resistor required to produce a desired time delay. The location for physically attaching the resistor to the interface board is shown in Figure 2-5.

Time Delay Decrease Formula:

$$Td = R_t \times .7C_f$$

where T_d = time delay in seconds,
C_f = fixed capacitance (100 pf) in farads

$$\text{and } R_t = \frac{R_f \times R_x}{R_f + R_x}$$

where R_f = fixed resistance (3.57 kΩ) in ohms
and R_x = selected resistance in ohms.

Example: Determine the parallel resistor needed to produce a time delay of 200 ns.

Since $Td = R_t \times .7C_f$

$$R_t = \frac{T_d}{.7C_f}$$

$$= \frac{200 \text{ ns}}{.7 \times 3.57 \text{ pf}}$$

$$= 2.8 \text{ k}\Omega$$

$$\text{and since } R_t = \frac{R_f \times R_x}{R_f + R_x}$$

$$R_x = \frac{R_f \times R_t}{R_f - R_t}$$

$$= \frac{3.57 \text{ k}\Omega \times 2.8\text{k}\Omega}{3.57 \text{ k}\Omega - 2.8 \text{ k}\Omega}$$

$$= \frac{10 \text{ k}\Omega}{.77}$$

$$= 13 \text{ k}\Omega$$

Note

Delay accuracy may deteriorate with an R_t of less than 2 kΩ(Rx<4.55 kΩ). Td should never be less than 100 ns (R_t <1.43 kΩ, Rx<2.39 kΩ).

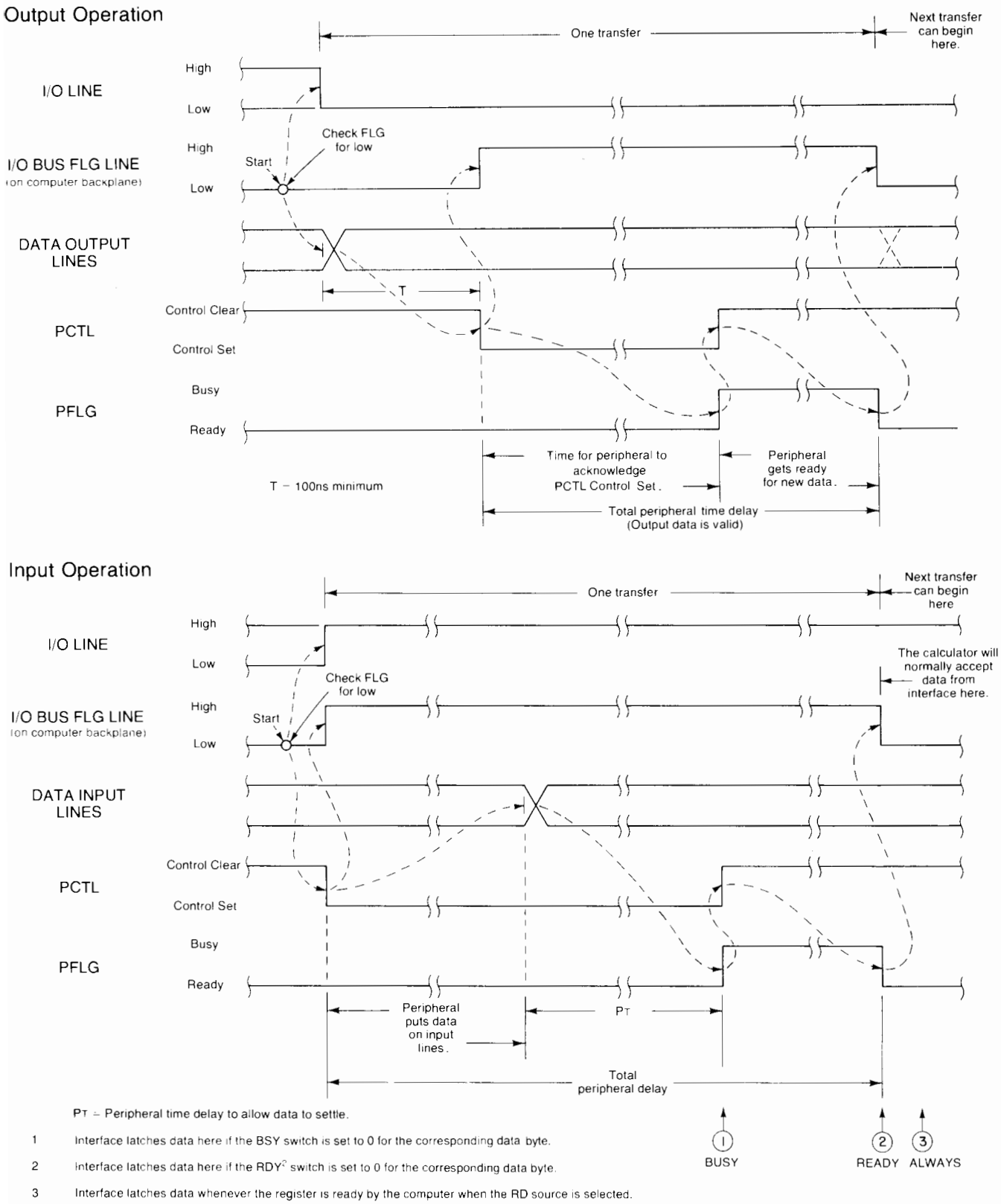
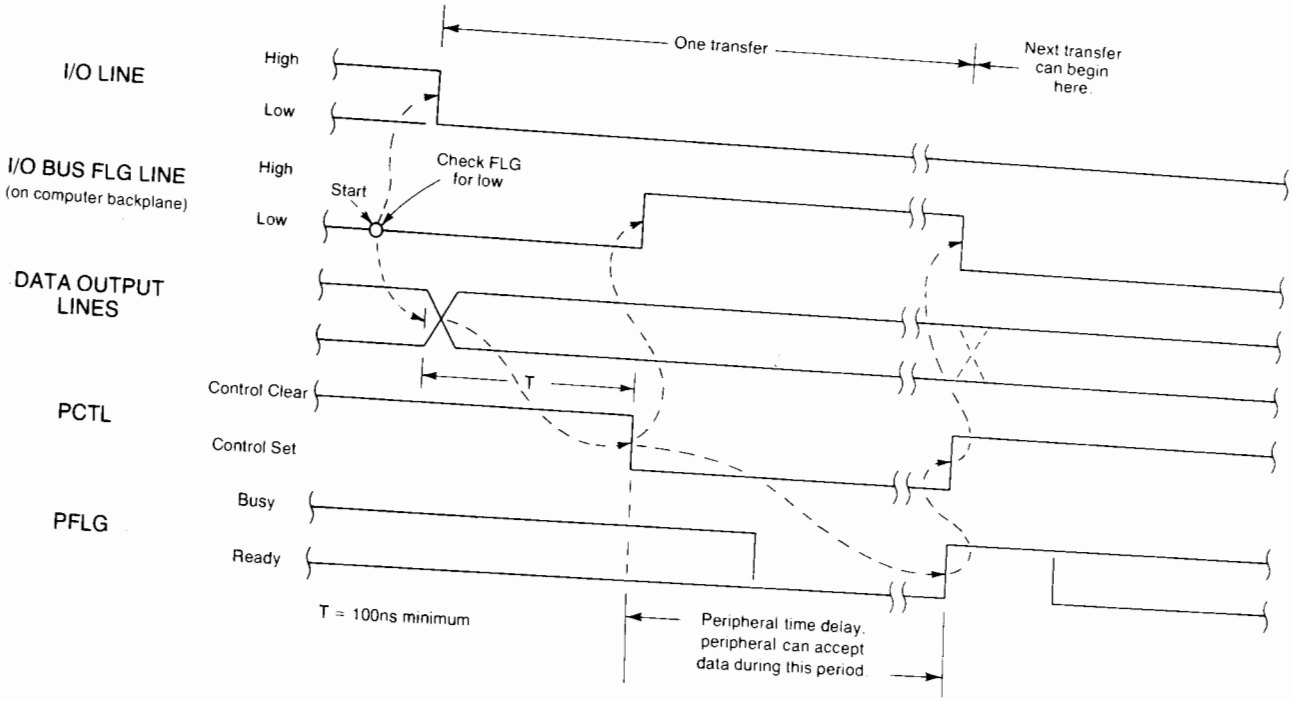
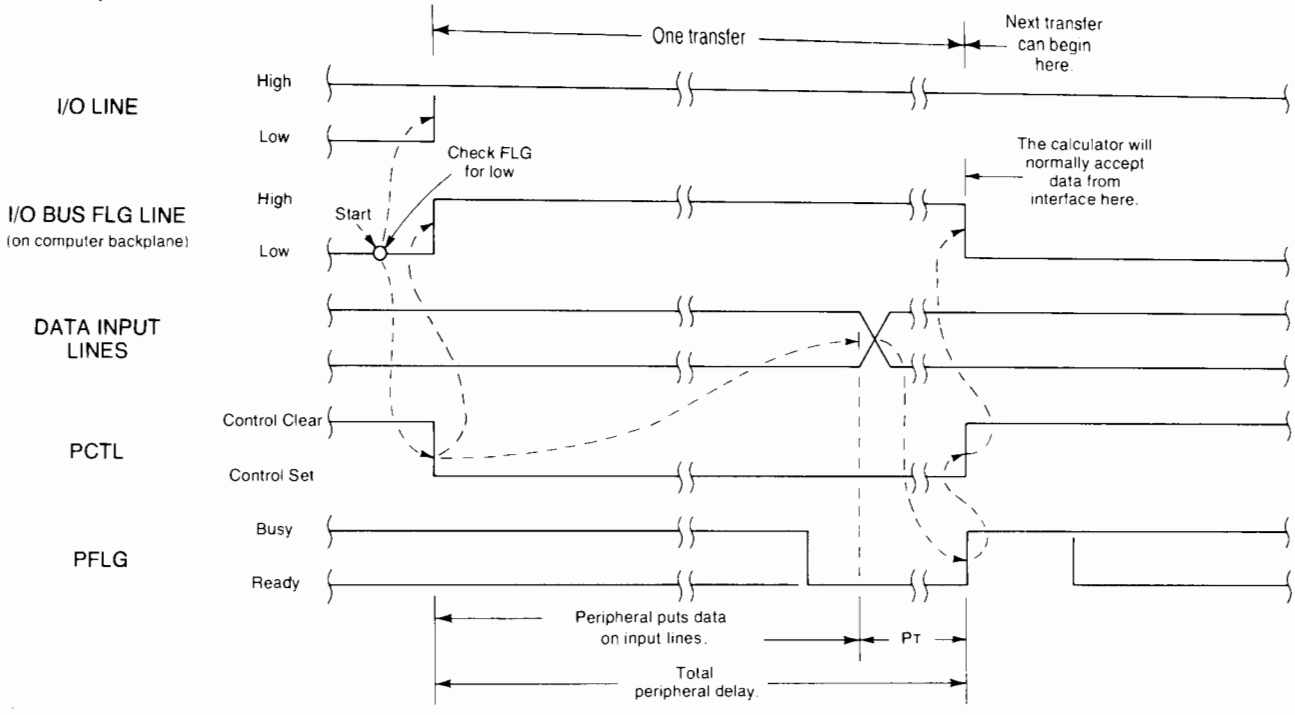


Figure 2-7. Full Mode Timing Diagram

Output Operation



Input Operation



PT = Peripheral time delay to allow data to settle.

1 Interface latches data here if the BSY switch is set to 0 for the corresponding data byte.

2 Interface latches data here if the RDY[2] switch is set to 0 for the corresponding data byte.

3 Interface latches data whenever the register is ready by the computer when the RD source is selected.

Figure 2-8. Pulse Mode Timing Diagram

Interface Cables

The following paragraphs provide detailed information concerning the various input/output and handshake lines for the GPIO Interface cable. Included are pinout tables along with recommended receiver and driver circuits. Information on preparing the cable is also included for those applications not using standard HP interface connectors.

Cable Preparation

Prepare the peripheral end of the interface cable as shown in Figure 2-9.

Note

Use heatshrink tubing or electrical tape to insulate the bare wire and shields.

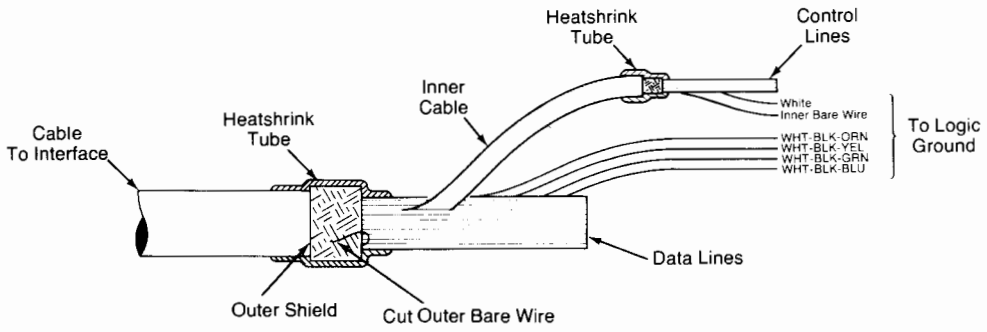


Figure 2-9. Preparing the Interface Cable

1. Cut the cable to the required length, allow sufficient length for slack.
2. Strip off approximately 10 cm (4 inches) of the outer plastic jacket.
3. Cut off all but approximately 1 cm (1/2 inch) of the outer shield.
4. Fold the outer shield back over the outer jacket.
5. Completely cover the end of the outer jacket and outer shield with heatshrink tubing or electrical tape.
6. Cut back the inner shield and its nylon jacket to within 2.5 cm (1 inch) of the outer jacket. (Do NOT cut off the bare inner wire.)
7. Completely cover the end of the inner shield and nylon jacket with heatshrink tubing or electrical tape.

Note

Do NOT allow the inner and outer shields to short together.

8. Strip and connect the cable wires as required to your peripheral/connector.
9. Connect the logic ground wires shown in Figure 2-9 to your peripherals logic ground.
10. Insolate unused wire with heatshrink tubing or electrical tape.

Data Input Lines

There are 16 data input lines labeled DI0 thru DI15 (refer to Table 2-3 for pinout assignments). Input line DI0 is the least significant bit (LSB) and DI15 is the most significant bit (MSB).

The interface operates with either positive or negative true logic. Refer to the "Option Select" section earlier in this manual for information concerning logic sense. Where possible, negative true logic is recommended.

Three choices of data-in clocking are available for each byte or for the 16-bit word. Refer to the "Data-In Clocking" section earlier in this manual for more information concerning clocking.

Table 2-3. Data Input Lines

Mnemonic		Connector Pin No.	Wire Color Code
	DI0	42	Black
	DI1	41	Brown
	DI2	40	Red
Low	DI3	39	Orange
Byte	DI4	38	Yellow
	DI5	37	Green
	DI6	36	Blue
	DI7	35	Violet
	DI8	34	White/Brown/Red
	DI9	33	White/Brown/Orange
	DI10	32	White/Brown/Yellow
High	DI11	31	White/Brown/Green
Byte	DI12	30	White/Red/Orange
	DI13	29	White/Red/Yellow
	DI14	28	White/Red/Green
	DI15	27	White/Red/Blue

Recommended Driver Circuits

Each of the data-input lines on the interface is connected to an exclusive OR gate. A resistive divider biases each input to approximately +3.4 volts when the cable is disconnected. Figure 2-10 shows the recommended peripheral driver circuits.

Note

Do NOT exceed 5.5 volts input to the data-input lines.

Driver Specifications: The following is a list of requirements for both the data input lines and the peripheral status and handshake input lines. Any driver circuit must match these input requirements.

Data Input Lines:

I_{in} low = 2.3 mA (V_{in} low = 0.4 V)

V_{in} max = 5.5 V

V_{in} high > 3 V

V_{in} low < 0.7 V

Peripheral Status and Handshake Lines:

I_{in} low = 3.3 mA (V_{in} low = 0.4 V)

V_{in} max = 5.5 V

V_{in} high > 3 V

V_{in} low < 0.6 V

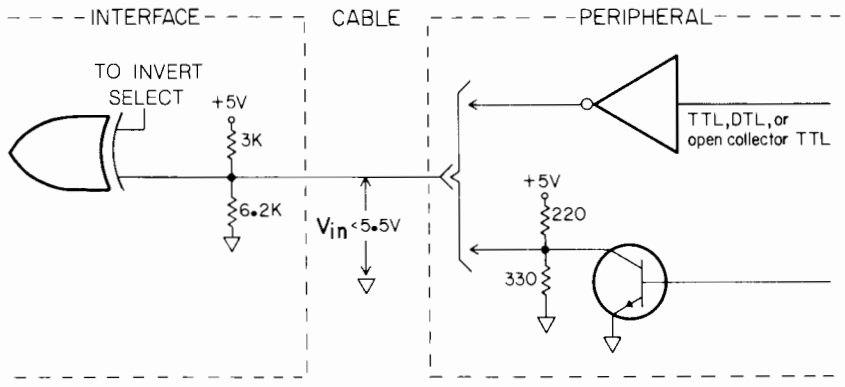


Figure 2-10. Recommended Peripheral Driver Circuit

Data Output Lines

There are 16 data output lines labeled DO0 thru DO15 (refer to Table 2-4 for pinout assignments). Output line DO0 is the least significant bit (LSB) and DO15 is the most significant bit (MSB).

The interface operates with either positive or negative true logic. Refer to the "Option Select" section earlier in this manual for information concerning logic sense. Where possible, negative true logic is recommended.

Table 2-4. Data Output Lines

Mnemonic		Connector Pin No.	Wire Color Code
Low Byte	DO0	17	White/Black
	DO1	16	White/Brown
	DO2	15	White/Red
	DO3	14	White/Orange
	DO4	13	White/Yellow
	DO5	12	White/Green
	DO6	11	White/Blue
	DO7	10	White/Violet
High Byte	DO8	9	White/Orange/Yellow
	DO9	8	White/Orange/Green
	DO10	7	White/Orange/Blue
	DO11	6	White/Orange/Violet
	DO12	5	White/Yellow/Green
	DO13	4	White/Yellow/Blue
	DO14	3	White/Yellow/Violet
	DO15	2	White/Yellow/Gray

Recommended Receiver Circuits

Each of the data-output lines on the interface is driven by an open collector buffer amplifier. The maximum current-sinking capability of each driver is 40 ma. with a breakdown voltage of 30 volts. (Do NOT apply a negative voltage to the output lines.) Figure 2-11 shows a recommended peripheral receiver circuit.

Receiver Specifications: The following is a list of requirements for both the data output lines and the handshake and control output lines. Any receiver circuit must match these output requirements:

V_{out} low
(I_{out} low = 16 mA) = 0.4 V max
(I_{out} low = 40 mA) = 0.7 V max

V_{out} high (open collector) = 30 V max
I_{out} low = 40 mA max
I_{out} high (Vout = 30 V) = 250 μa

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Since each driver has an open collector, the peripheral receiving circuit must have a positive pull-up voltage (do NOT exceed 30 volts). It must also be restricted to sourcing less than 40 mA.

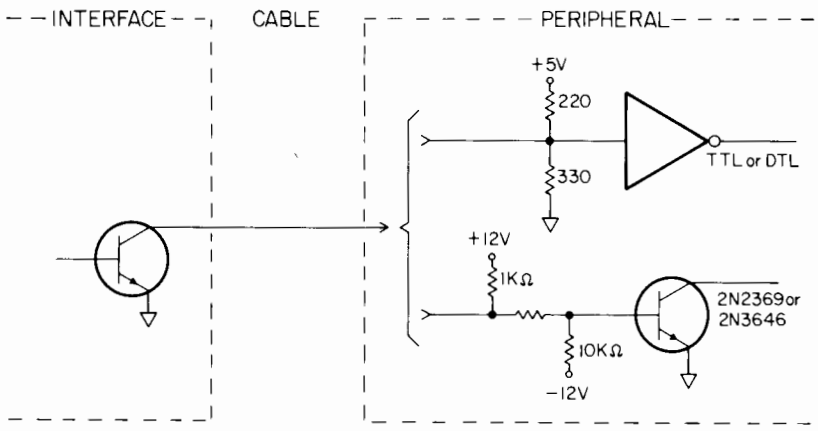


Figure 2-11. Recommended Peripheral Receiver Circuit

Peripheral Information and Control Lines

Ten lines control the exchange of information between the interface and the peripheral. Five of these lines are outgoing to control the peripheral. The other five are incoming to communicate the condition of the peripheral. Table 2-5 lists all the peripheral information lines and their pinout assignments. Figures 2-7 and 2-8 show the timing relationships between these lines and the data transfer.

All 5 incoming lines have Schmitt trigger receiver circuits. These circuits accept signals with slow rise and fall times. They also provide good noise immunity. Although the voltage on these lines must not exceed 5.5 volts, there are no restrictions on the input rise and fall times. Either of the driver circuits shown in Figure 2-10 can be used to drive these lines.

All 5 outgoing lines may be received by receiver circuits similar to those required by the data input lines (see Figure 2-11).

Peripheral Control Line

The peripheral control line (PCTL) is an outgoing line to the peripheral. It is paired with the peripheral flag line (PFLG) to synchronize (handshake) the computer with the peripheral.

PCTL has two states: control set (normally low) and control clear (normally high). The peripheral clears control on the PCTL line by a ready-to-busy transition on the PFLG line (see PFLG line).

PCTL is delayed to allow new output data to settle. This delay time is factory set to 250 ns. This delay can be increased or decreased as required by the application. (Refer to "PCTL Delay Adjustment" earlier in this manual.)

The logic sense of the PCTL line can be inverted in the hardware. Refer to the "Option Select" information earlier in this manual to invert the PCTL line using hardware configuration.

Peripheral Flag Line

The peripheral flag line (PFLG) is an incoming line from the peripheral. It is paired with the peripheral control line (PCTL) to synchronize (handshake) the computer to the peripheral. This line must be driven to complete a data transfer. If no handshake is required, connect PFLG to PCTL at the peripheral end of the interface cable and invert the PFLG (refer to the "Option Select" information earlier in this manual).

Transferring Data. PFLG has two states: ready (normally low) and busy (normally high). When the peripheral is ready to transfer data, it responds by asserting PFLG to ready. When the computer sets PCTL, the computer has initiated a data transfer either in or out depending on the state of the I/O line.

After the data transfer occurs, the peripheral responds by setting PFLG busy. This causes the computer to clear the PCTL line on the ready-to-busy transition. In the "full" handshake mode, the computer waits until the peripheral makes PFLG ready before initiating another data transfer. In the "pulse" handshake mode, the computer initiates the required data transfers without waiting.

Handshake Modes. Two modes of handshake are available: full and pulse. Full handshake mode is the factory set mode. Refer to the "Option Select" information earlier in this manual to configure the interface for pulse mode.

The logic sense of the PFLG line can be inverted by hardware configuration. Refer to the "Option Select" information earlier in this manual to invert the PFLG line using hardware configuration.

Peripheral Status Line

The peripheral status line (PSTS) is an optional incoming line from the peripheral. It signals the computer that all is "OK" with the peripheral. Conditions such as: the peripheral is powered down, interlocks are broken, or the peripheral is out of paper, etc., would cause a "not OK" signal to be sent to the computer.

PSTS has two states: not OK (OK is normally low) and OK (normally high). The logic sense of the PSTS line can be inverted by hardware configuration. Refer to the "Option Select" information earlier in this manual to invert the PSTS line using hardware configuration.

Note

Inverting the sense of the PSTS line allows detection of an open cable since it will float high (not OK).

Extended Status Input Lines

The optional extended status input lines ($\overline{\text{STI0}}$ and $\overline{\text{STI1}}$) provide two additional incoming status lines from the peripheral. They can be implemented by the user for any purpose that reflects the status of the peripheral.

$\overline{\text{STI0}}$ and $\overline{\text{STI1}}$ have two states: low (logic 1) and high (logic 0) and they can not be inverted. The state of these lines can be examined by reading the status register.

Extended Control Output Lines

The optional extended control output lines ($\overline{\text{CTL0}}$ and $\overline{\text{CTL1}}$) provide two additional outgoing output control lines to the peripheral. They can be used for any purpose to control the peripheral.

$\overline{\text{CTL0}}$ and $\overline{\text{CTL1}}$ have two states: control set (low) and control clear (high). These lines are latched and can be set or cleared (low = 1, high = 0) low by outputing to the control register. The states of these lines are undetermined at power up and unchanged after a reset.

Input/Output Direction Control Line

The optional Input/Output direction control line (I/$\overline{\text{O}}$) is an outgoing line to the peripheral. It is always valid during PCTL control set. I/$\overline{\text{O}}$ indicates to the peripheral which direction the data transfer is to go. I/$\overline{\text{O}}$ goes high for an input operation and low for an output operation.

Peripheral Reset Line

The optional peripheral reset line ($\overline{\text{PRESET}}$) is an outgoing line to the peripheral. $\overline{\text{PRESET}}$ is used to reset and/or initialize the peripheral. $\overline{\text{PRESET}}$ is pulsed low when the computer is first turned on and when the RESET key is pressed. It is also pulsed low when the reset bit is sent to the control register. The minimum $\overline{\text{PRESET}}$ pulse width is 12 μs. Refer to the I/O programming manual for the language installed in your computer for more information concerning the peripheral reset line.

External Interrupt Request Line

The external interrupt request line ($\overline{\text{EIR}}$) is an incoming line from the peripheral. The $\overline{\text{EIR}}$ line can be used to trigger an interrupt on an external event. $\overline{\text{EIR}}$ is also level sensitive and should be held low until the interrupt service routine has been invoked and acknowledges the request.

Table 2-5. Peripheral Information Lines

Line Name	Mnemonic	Connector Pin No.	Wire Color Code
Peripheral Control	PCTL	19	White/Gray
Peripheral Flag	PFLG	44	Gray
Peripheral Status	PSTS	45	White/Black/Gray
Extended Status	STI0	47	White/Brown/Blue
Extended Status	STI1	48	White/Brown/Violet
Extended Control Output	CTL0	22	White/Red/Violet
Extended Control Output	CTL1	23	White/Red/Gray
Input/Output Direction Control	I/O	20	White/Black/Brown
Peripheral Reset	PRESET	21	White/Black/Red
Ext. Interrupt Request	EIR	46	White/Brown/Gray

Installing the Interface Card

There are eight slots in the 9826 backplane. However, since each interface card connector panel takes up two slots, only four interface cards can be installed in the backplane. Memory cards can, however, be installed in the vacant slots behind the connector panels. Each interface card installed decreases by one the number of memory boards which may be installed.

Use the following procedure to install an interface card in the computer's backplane:

1. Set the switches on the interface card according to the instructions in the section on "Configuring the Interface Card" described earlier in this chapter.
2. Turn the computer power off.
3. Interface cards must be installed in one of the four slots just under a pair of cover bolt holes. The metal interface connector panel takes the place of a backplane cover.

Note

Remove the metal backplane covers one-by-one until you find an empty slot just under a pair of cover bolt holes.

Note

A memory or DMA card can be installed in the slot above the interface card.

5. Slide the interface card into the slot, component-side up, until it bottoms against the backplane motherboard. Then tighten the dog bolts until they are finger tight.
6. If there are no empty slots under a pair of cover bolt holes, rearrange the memory boards to accomodate the interface card. Reinstall the memory board in the slot above the interface card.
7. If there are no empty slots, a memory board or another interface card must be left out if this interface card is to be installed. If a RAM memory board is left out, make sure that it is the RAM board with the lowest address.
8. Connect the interface card to the peripheral using the correct cable.
9. Turn the computer and the peripheral on and operate them according to their appropriate operating manuals. If problems are encountered, call your nearest HP Sales/Service Office.

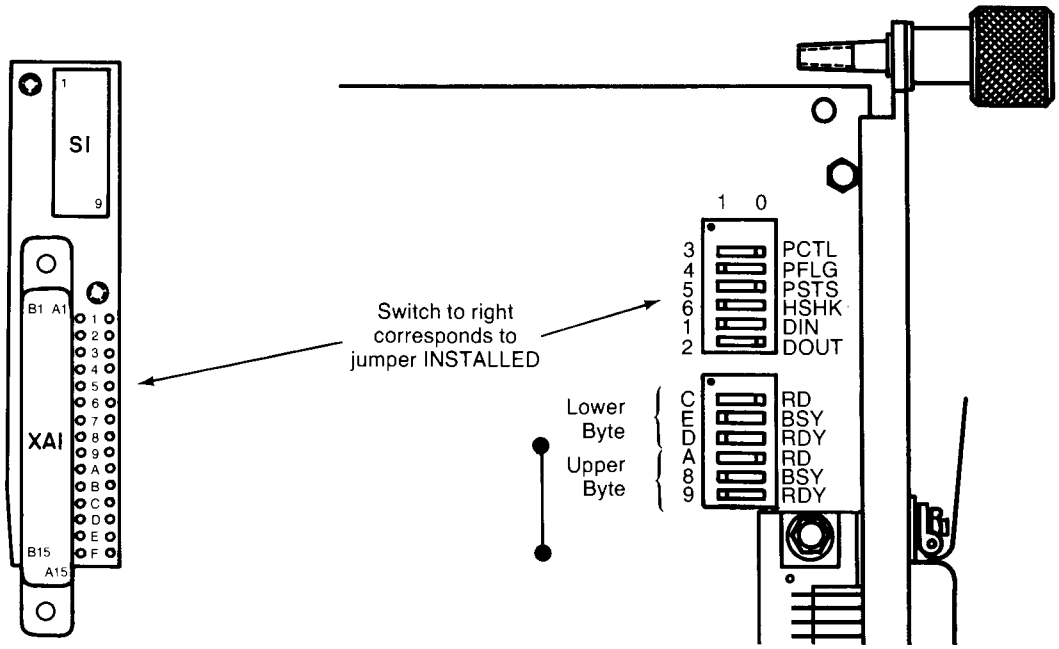
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Notes

Appendix A

Configuring 98622 Cards to Match 98032 Cards

Use the following chart to configure the 98622A GPIO card to match a 98032 card.



98032 Interface Jumpers
(Component side)

98622 Interface Switches
(Component side)

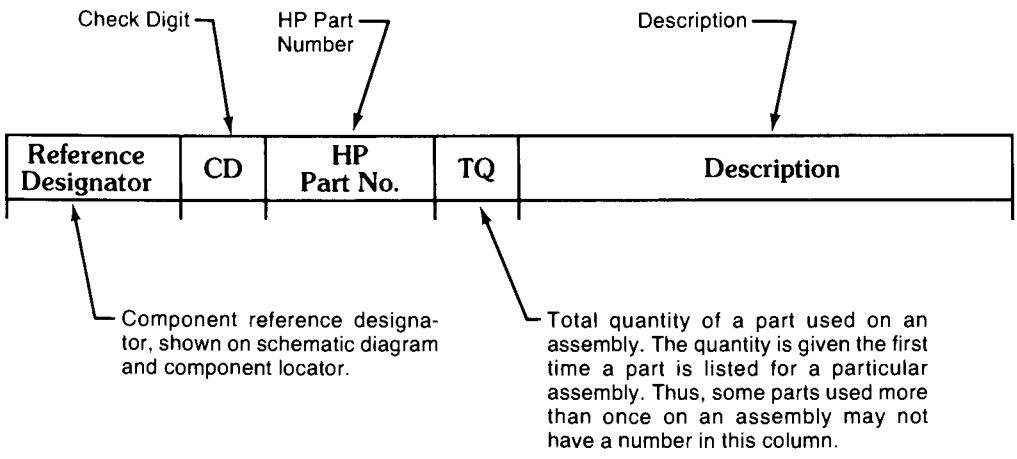
Appendix B
Replaceable Parts

Introduction

This chapter contains part number information for the 98622A GPIO interface.

The part number information is presented in this manner:

Table 1 lists the replaceable parts. Here is a description of each table column.



Parts may be ordered from Corporate Parts Center. The address is:

Corporate Parts Center
333 Logue Avenue
Mountain View, California 94042

The telephone number is: (415) 968-9200

Table B-1. GPIO Board Parts

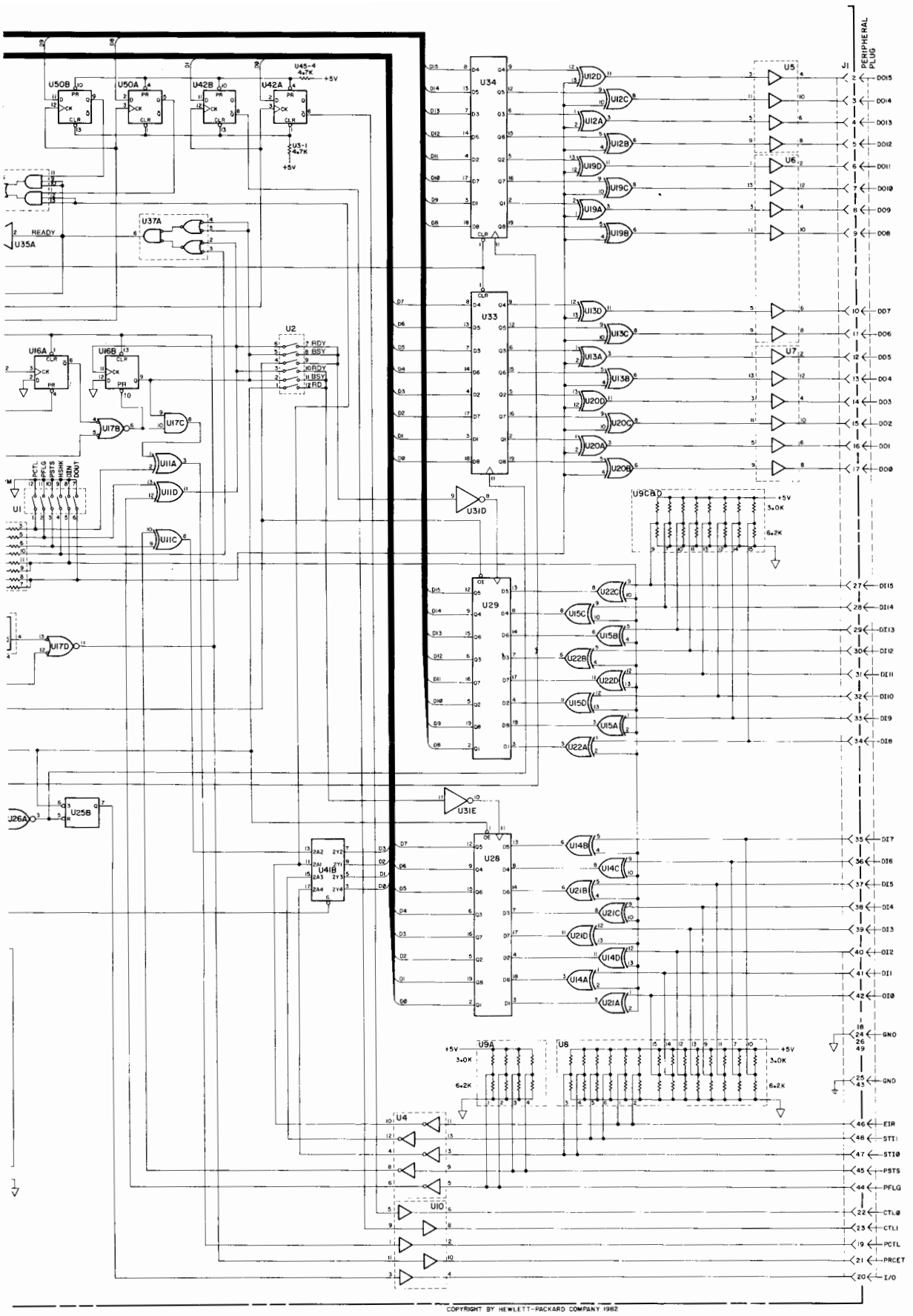
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	98622-66501	7	1	ASSEMBLY-GP I/O	28480	98622-66501
C2	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C3	0160-3847	9	12	CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C4	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C5	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C7	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C8	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C9	0160-3334	9	1	CAPACITOR-FXD .01UF +-10% 50VDC CER	28480	0160-3847
C10	0160-2204	8	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-3334
C11	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-2204
C12	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C13	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C14	0160-0205	7	1	CAPACITOR-FXD 10PF +-5% 500VDC MICA	28480	0160-3847
C15	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-0205
C17	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C19	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
C22	0160-3847	9		CAPACITOR-FXD .01UF +100-0% 50VDC CER	28480	0160-3847
F1	2110-0592	2	1	FUSE 4A 125V NTD .281X.093	28480	2110-0592
R2	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
R3	0698-3496	3	1	RESISTOR 3.57K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3572-F
R4	0698-3279	0	2	RESISTOR 4.99K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4991-F
R5	0698-3279	0		RESISTOR 4.99K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4991-F
U3	1810-0424	2	2	NETWORK-RES 16-DIP4.7K OHM X 15	11236	761-1-R4.7K
U4	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U5	1820-0668	7	4	IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
U6	1820-0668	7		IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
U7	1820-0668	7		IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
U8	1810-0481	1	2	NETWORK-RES 16-DIP MULTI-VALUE	28480	1810-0481
U9	1810-0481	1		NETWORK-RES 16-DIP MULTI-VALUE	28480	1810-0481
U10	1820-0668	7		IC BFR TTL NON-INV HEX 1-INP	01295	SN7407N
U11	1820-1211	8	8	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U12	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U13	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U14	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U15	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U16	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U17	1820-1201	6	3	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U18	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U19	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U20	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U21	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U23	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U24	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U25	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U26	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U27	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U28	1820-1997	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U29	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U30	1820-1782	8	1	IC MV TTL S MONOSTBL RETRIG/RESET DUAL	34335	AM26S02PC
U31	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U32	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U33	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U34	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U35	1820-1568	8	1	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
U36	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U37	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
U40	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U41	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U42	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U43	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U44	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U45	1810-0424	2		NETWORK-RES 16-DIP4.7K OHM X 15	11236	761-1-R4.7K
U46	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U47	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U48	1820-1645	2	1	IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
U49	1820-1427	8	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS156N
U50	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U51	1820-2740	0	1	IC COMPTR TTL LS MAGTD 2-INP 8-BIT	01295	SN74LS688N
U52	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U53	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N

See introduction to this section for ordering information
*Indicates factory selected value

Table B-1. GPIO Board Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	1251-7161	2	1	CONNECTOR-50 PST RING	28480	1251-7161
	3101-2506	4	1	SWITCH ASSEMBLY-ROCKER	28480	3101-2506
	3101-2508	6	1	SWITCH ASSEMBLY-ROCKER	28480	3101-2508
	3101-2509	7	2	SWITCH ASSEMBLY-ROCKER	28480	3101-2509

See introduction to this section for ordering information
*Indicates factory selected value



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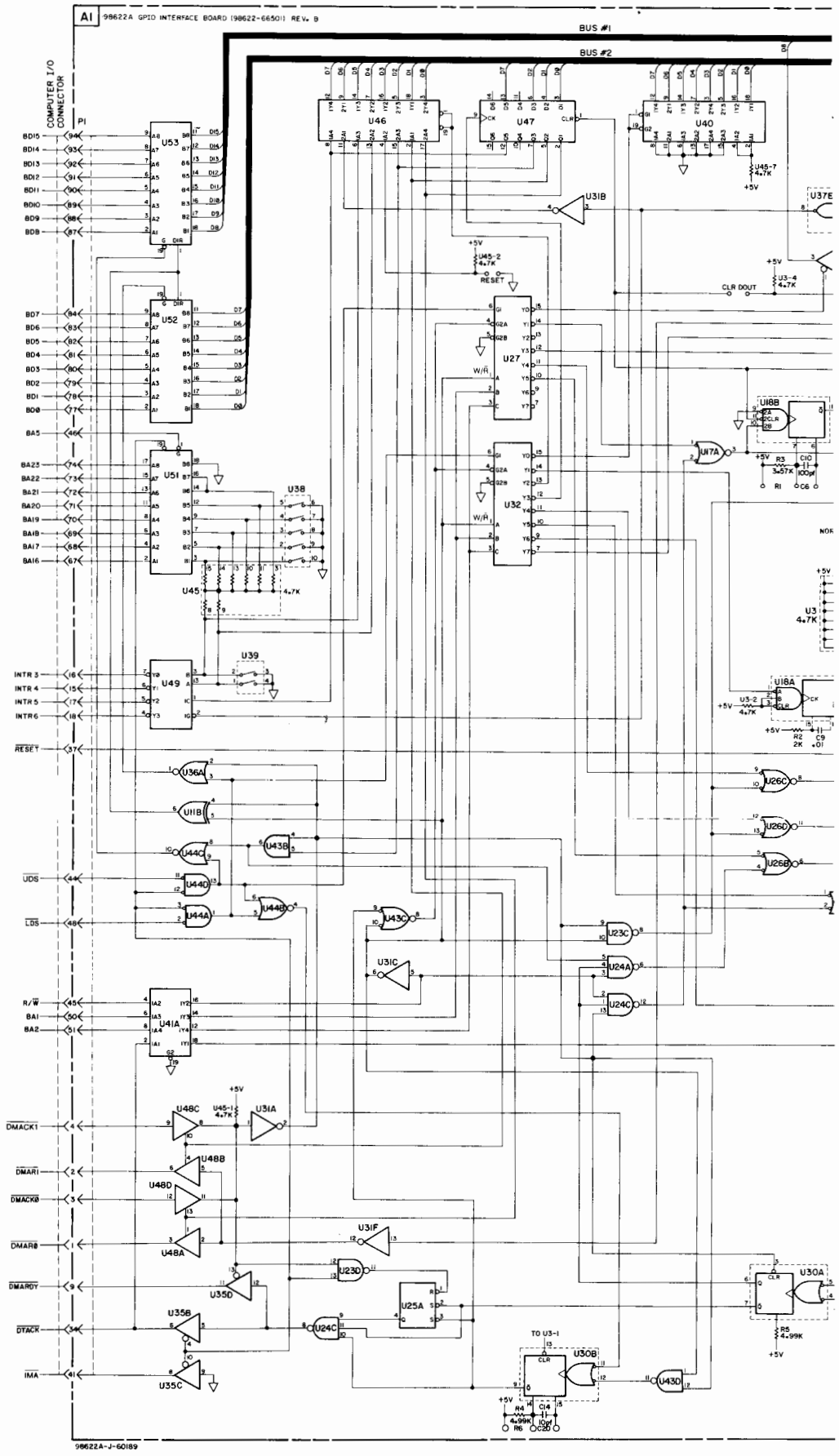
HEWLETT PACKARD

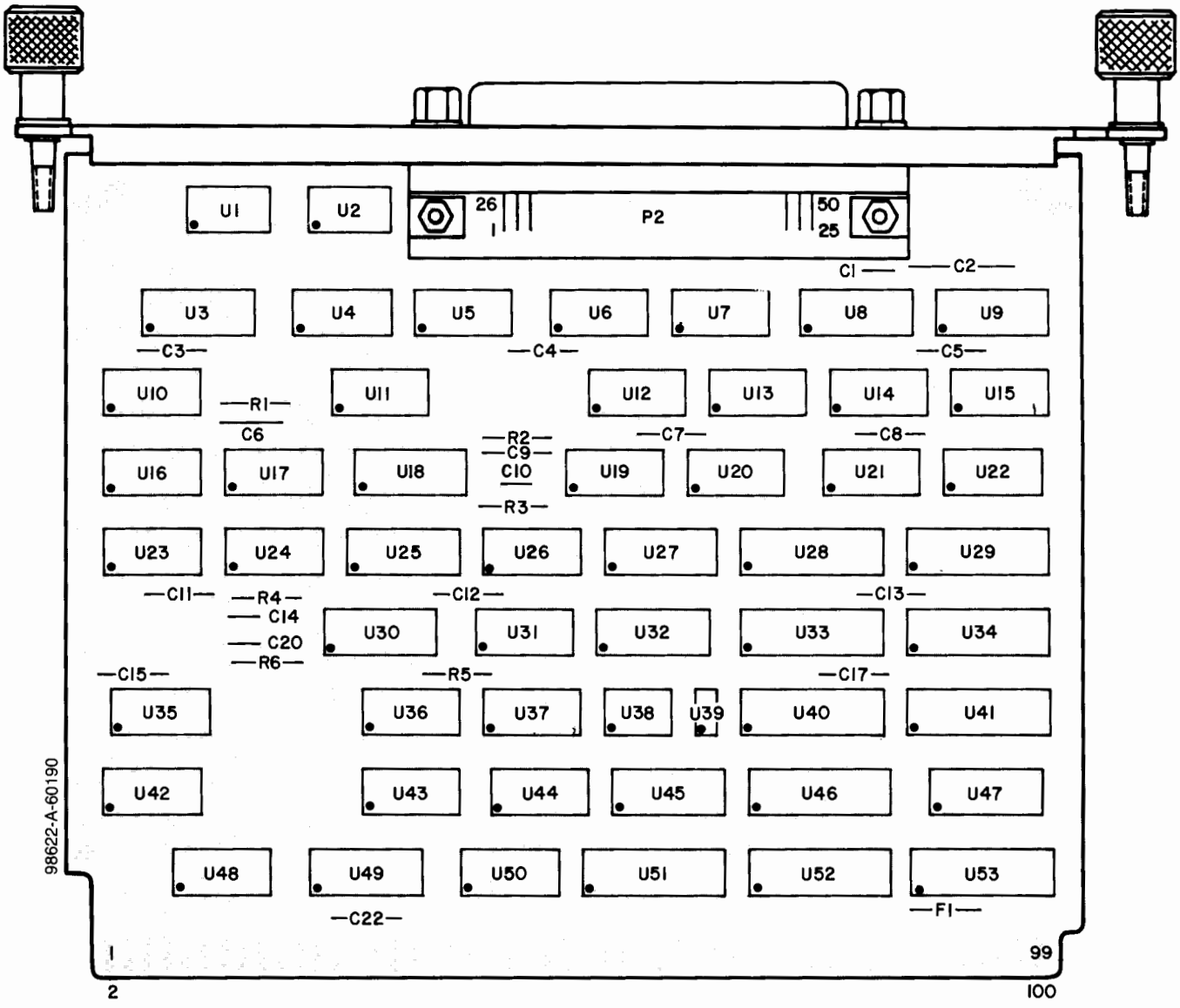
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

A1

98622A GPIO INTERFACE BOARD
SCHEMATIC DIAGRAM

Manual Part No. 98622-90000 Dwg Rev B Sheet 1 of 1


A1
98622A GPIO INTERFACE BOARD (98622-66501) REV. B
BUS #1
BUS #2
COMPUTER I/O CONNECTOR
P1
U53
U52
U51
U49
U46
U47
U40
U27
U32
U38
U39
U45
U45-2 4.7K
U45-7 4.7K
U3-4 4.7K
U3 4.7K
U3-2 4.7K
U45-1 4.7K
U31B
U31C
U31A
U31F
U36A
U11B
U44C
U44D
U44A
U43B
U43C
U43D
U48C
U48B
U48D
U48A
U41A
U23C
U24A
U24C
U23D
U35D
U35B
U35C
U25A
U18B
U18A
U17A
U26C
U26D
U26B
U30A
U30B
TO U3-1
R1 3.57K
C10 100pf
R2 2K
C9 .01
R3 4.99K
C14 10pf
R4 4.99K
R5 4.99K
R6
C15
+5V
RESET
CLR DOUT
W/R
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
BA5
BA23
BA22
BA21
BA20
BA19
BA18
BA17
BA16
INTR 3
INTR 4
INTR 5
INTR 6
RESET
UDS
LDS
R/W
BA1
BA2
DMACK1
DMAR1
DMACK0
DMAR0
DMARDY
DTACK
IMA
98622A-J-60189



COMPONENT SIDE
A1

HP Part No. 98622-66501 Rev B

SCHEMATIC NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN, PREFIX WITH ASSEMBLY OR SUBASSEMBLY DESIGNATION(S) OR BOTH FOR COMPLETE DESIGNATION.
2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.
   RESISTANCE IN OHMS
   CAPACITANCE IN MICROFARADS
3. A CURVED LINE MEETING A BUS DENOTES THAT LINE ENTERS THE BUS, A STRAIGHT LINE MEETING THE BUS DENOTES THAT LINE DOES NOT ENTER THE BUS.



Part No. 98622-90000
E1183

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