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TUE, JUL 27, 1982, 4:56 PM

98628/98629 Hardware External Reference Specification

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Chapter 1: Introduction

The 98628 card is a data communications card for the 9826 family of mainframes. With its microprocessor and peripheral chips, the interface can handle the protocol management and electrical levels of an asynchronous or synchronous (bit-oriented or byte-oriented) connection. The code currently being developed for the interface as part of the ALVIN project will handle the asynchronous and Data Link (slave only) protocols. This code will be described in other sections of this ERS. By changing the program on the card, other protocols may be implemented in the future. This may be done by downloading the card RAM from the mainframe or by changing the card's program ROM - no new mainframe code should be required.

The 98629 card interfaces between the 9826 family of mainframes and the GANGLIA peripheral manager. It is a loading option of th 98628 with different line receiver biasing, a new program ROM and an extra RAM chip.

This ERS describes the hardware for both the 98628 and 98629 interfaces. The '98628/98629' designation will be used to indicate a function common to both cards. Unique functions will be referred to with only the appropriate product number.

Chapter 2 gives the specifications for the card. Chapter 3 will describe the theory of operation. Chapter 4 discusses the interface to the remote device. Chapter 5 documents the test procedure for the card, including the signature analysis tests.

Chapter 2: Specifications

Physical Description:

Size: 13.5 centimeters by 17 centimeters

Weight: 310 grams (11 ounces)

Environmental Specifications:

Temperature: 0 to 45 degrees Celsius

Humidity 0 to 80%

Electrical Specifications:

Card Power Consumption:

98628:
+5 Volts at 715 mA typical (680 mA without ROM or RAM)
+12 Volts at 37 mA typical
-12 Volts at 60 mA typical

98629:
+5 Volts at 745 mA typical (680 mA without ROM or RAM)
+12 Volts at 37 mA typical
-12 Volts at 37 mA typical

Pod Power Consumption (supplied by the mainframe):

	+5 Typ	+12 Typ	-12 Typ
Current Loop Pod	200 mA	90 mA	80 mA
Modem Pod	100 mA	45 mA	45 mA
Data Link Pod	30 mA	160 mA	23 mA
Multipoint Pod	450 mA	400 mA	100 mA

Note: Due to its large power requirements, **the multipoint pod will not be supported.**

Electrical Interface Compatibility:

RS-232C, V.24/V.28
RS-449
RS-423, V.10
RS-422, V.11

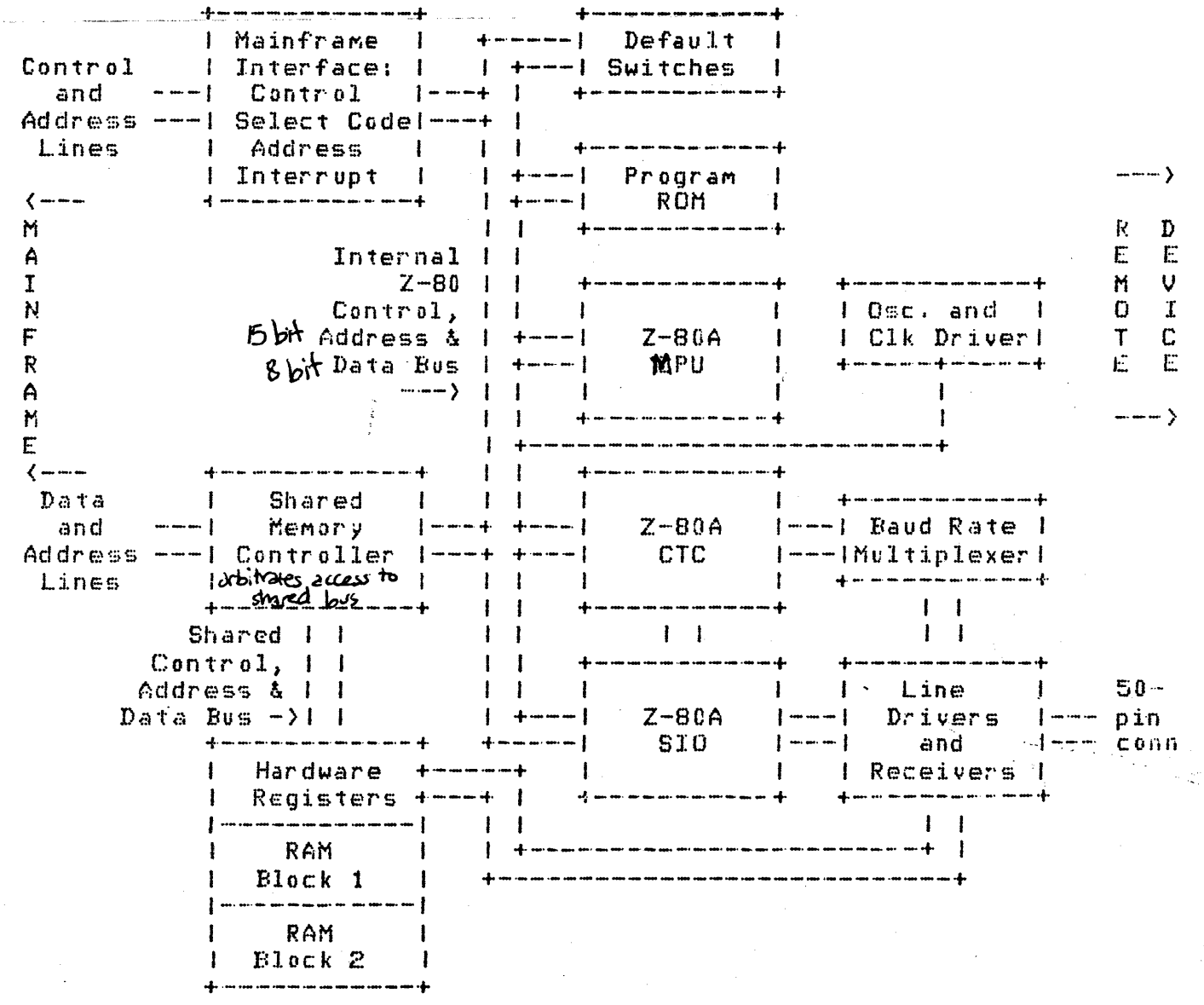
Data Rates:

Internal Clocking:	Asynchronous:	19.2K Baud
	Synchronous:	Limited by firmware
External Clocking:	Limited by firmware	

Chapter 3: Theory of Operation

This chapter of the ERS describes the operation of the 98628/98629 card hardware. First, the block diagram of the card will be discussed. Then, each of these blocks will be described in more detail at the component level.

Block Diagram



3.1: Busses

As shown in the block diagram, the Z80 microprocessor (MPU), Z80 serial I/O (SIO), Z-80 Counter Timer Chip (CTC), program ROM and default switches are tied together by the internal Z-80 15-bit address (ZA) bus and 8-bit data (ZD) bus. This bus belongs exclusively to the Z-80 MPU and cannot be accessed by the mainframe. No extra Z-80 WAIT states will be added when accessing devices on this bus.

The shared RAM and registers are connected by the Shared 15-bit address (SA) bus and 8-bit shared data (SD) bus. **The shared bus can be accessed either by the Z-80 MPU or by the mainframe.** The shared memory controller arbitrates access to this bus. Once a processor begins a memory cycle, it will run to completion. If there are overlapping memory requests to the shared memory, one of the processors will be put into the WAIT state until the other has completed its memory cycle. The **mainframe is given priority** in the case of simultaneous memory requests.

When the mainframe accesses shared memory, 15 bits of its address bus and 8 bits of its data bus are gated to the shared bus. This is the only connection to the mainframe bus - it cannot be accessed directly by the Z-80.

The remainder of this chapter will describe the operation of the card at the component level. All references to individual components (i.e. U1, R4, etc.) will refer to the revision A PC boards and schematic. The text will make more sense if the schematic is referenced. **Signal names followed by an apostrophe (') are negative true.**

3.2: Mainframe Interface Circuitry

3.2.1: Address Recognition

The Address Comparitor (U43) decodes the mainframe address lines to detect accesses to the card. Each I/O card has an unique address range depending on the select code. Address lines BA16 to BA20 are compared to the card select code from SW2. Address lines BA23 to BA21 are compared to '011' (the address space assigned to external I/O). The Address Comparitor is gated with the BAS' (Buffered Address Strobe) line from the mainframe to guarantee that the address is stable. The P=Q output of the Address Comparitor goes low when the card is addressed. This signal will be referred to as MY PA'.

When the card is accessed (MY PA' low), it pulls IMA' (I'm Addressed) line low (U35, 8-10) and enables the DTACK' (Data Acknowledge) buffer (U35, 11-13). DTACK' is originally high (inactive) but is later pulled low by the Shared Memory Controller circuitry.

BLDS' (Buffered Lower Data Strobe) from the mainframe, MY PA' and the output of the cycle enable flip flop (U23:1-4) are ANDed (U24:8-10; U4:11-13) to produce the mainframe shared memory request signal. This line is one of the inputs to the Shared Memory Controller. The cycle

enable flip flop guarantees that the Shared Memory Controller has ended of previous cycle before starting another.

3.2.2: Interrupts

The mainframe may enable or disable interrupts by writing to bit 7 of register 1. This bit is latched by the Interrupt Enable Flip Flop (U14, 1-6).

When the 98628/98629 firmware determines that service by the mainframe is required, it writes the condition to the Interrupt Cause Register (in RAM). The write will automatically reset the Interrupt Request Flip Flop (U23: 9-11). This flip flop is set when the interrupt cause register is read by the mainframe. If interrupts are enabled (Interrupt Enable Flip Flop=0), and service is requested (Interrupt Request Flip Flop=0) then the Interrupt Demultiplexer (U34) will be enabled. When enabled, the Interrupt Demultiplexer decodes the interrupt level switches (SW2, 6&7) and pulls on the appropriate interrupt request line (IR3' to IR4').

3.2.3: RESET

On power-up, the mainframe pulls on the RESET line to the I/O cards. On the 98628/98629, this will reset the Z-80 MPU by pulling on its RESET line and will clear the Reset Flip Flop (U15, 8-13).

The mainframe may also initiate a programmed reset of the card by writing a '1' to bit 7 of register 0. This reset is also latched by the Reset Flip Flop.

The Reset Flip Flop has the effect of:

* Disabling mainframe interrupts by setting the Interrupt Enable Flip Flop (U14: 1-6).
* Disabling mainframe interrupt requests by setting the Interrupt Request Flip Flop (U23: 9-12).
* Clearing the hardware Semaphore Flip Flop. (semaphore busy)
* Initializing the Z-80 CTC (U12) and Z-80 SIO (U27) by pulling on their RESET lines.
* Disabling the outputs of the Modem Control Latch (U6) to guarantee that the Terminal Ready and Request to Send lines will be in the 'OFF' state until initialized by the processor.
* Interrupting the Z-80 MPU with a nonmaskable interrupt (NMI). NOTE: On power-up, only the MPU RESET will be seen - the NMI will be ignored.
* Initializing the baud clock dividers (U13) for consistent test signatures.

3.3: Shared Memory Controller

3.3.1: Address Multiplexer/Latch

The address multiplexer/latches (U39-U42) drive the Shared Address (SA) Bus. Depending on the state of the Shared Memory Access Flip Flop (U17: 1-6) the address from the Z-80 or mainframe address bus is latched at the beginning of a shared memory cycle.

3.3.2: Read/Write Control Lines

In order to guarantee proper hold time for the shared memory read/write (R/W) control lines, the individual R/W lines from the Z-80 and mainframe are latched. The Z-80 RD' line is held by an RS flip flop (U23: 13-15) to the end of a cycle. The mainframe BR/W (Buffered Read/Write) line is latched at the beginning of a cycle (U39: 2,15).

The processor R/W lines are multiplexed (U32: 5-7) to give the appropriate shared memory R/W control. The output of the multiplexer (U32-7) is SRD' directly. When gated (U36: 3-6) with the shared memory timing flip flops, it becomes SWR'. The timing on these signals will be described in more detail later.

3.3.3: Data Bus Transceivers

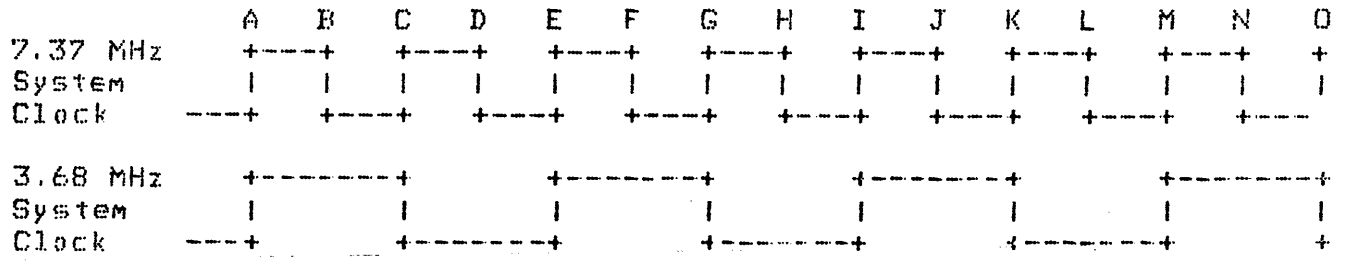
There are two data bus transceivers (U44 and U45) to connect the Shared Data Bus to either the Z-80 or the mainframe data bus. The direction of these transceivers is controlled by the associated read/write circuitry from the Z-80 or the mainframe. The appropriate transceiver is enabled during a memory cycle by the shared memory arbiter as described later. The Shared Data Bus is inverted (active low). Data is inverted by the transceivers when data is read or written.

3.3.4: Shared Memory Arbiter

The shared memory arbiter controls the shared memory resources and generates the appropriate control signals.

The two inputs to the arbiter are the shared memory request signals from the mainframe and the Z-80. As described above, the mainframe request signal is generated from MY PA',BLDS' and cycle enable. The Z-80 requests shared memory when ZMREQ'=0, ZA15=1 AND RFSH'=1 (U24: 1-3; U30: 5-6 & U4: 4-6). The appropriate request line is multiplexed (U32: 2-4) to give a shared memory request signal.

The arbiter is clocked by the 3.68 MHz and 7.37 MHz system clocks as illustrated below. The 3.68 clock is derived by dividing the 7.37 MHz clock (U19: 1-6).



Whenever a shared memory cycle is not in progress, the mainframe Shared Memory Request line is sampled on alternate falling edges of the 7.37 MHz clock (i.e. edges D, H & L) and is latched by the Shared Memory Access Flip Flop (U19: 8-13). This flip flop selects either the Z-80 or the mainframe to control the shared memory bus via the select lines to the multiplexers and transceivers. At the negative edge of the 3.68 MHz clock (i.e. B, G, K & O), the address from the selected processor (mainframe or Z-80) and BR/W are latched by the address multiplexer & latches (U39-U42). At the rising edge of the 3.68 MHz clock (i.e. edges A; E, I & M), the memory request line of the selected device is sampled by the first flip flop of the Shared Memory Timing Chain (U17: 1-6). If shared memory is requested, this flip flop will be cleared which starts a shared memory cycle:

* Disables (U24: 11-13 & U16: 4-6) the clock to the Shared Memory Access Flip Flop.
* Disables (U16: 1-3) the clock to the address multiplexer/latches (U39-U42).
* Generates SMREQ' to enable the Shared Memory Address Decoder (U31,9-15)
* If it is a write cycle, activates (U36: 3-6) the Shared Write (SWR') line.
* Enables (U24:4-6 & U32: 9-14) the appropriate data bus transceiver (U44 or U45) for the selected device.
* If the Z-80 is selected, releases the Z-80 WAIT' input (U16: 8-10; U36: 1,2,12,13, U4: 1-3).

At the next positive going 3.68 MHz clock edge, the next flip flop of the Shared Memory Timing Chain (U17, 8-13) is set which:

* Inhibits (U36: 3-6) the SWR' signal to end a memory write cycle.
* If the mainframe is selected, generates the DTACK' signal (U37: 8-10).

The arbiter will remain in this state until the selected device releases its request line which disables (U24: 4-6) the data bus transceiver. At the next positive edge of the 3.68 MHz clock, the first shared memory timing flip flop (U17: 1-6) will go inactive which:

* Clears the second timing flip flop (U17: 8-13) using its clear input.
* If the memory cycle was intitiated by the mainframe, re-enables mainframe memory requests by setting the enable flip flop (U23: 1-4).
* Releases the Z-80 RD' latch (U23: 13-15).

* Re-enables the clocks to the shared memory access flip flop (U19: 8-13) the address/muliplexer latches (U39-U42).

As an example, a write to shared memory from the mainframe would work as follows:

1) the mainframe begins its write to the 98628/98629 which generates the mainframe Shared Memory Request signal (U4-11).

2) At the negative 7.37 MHz clock edge (assume clock edge B), the Shared Memory Access Select Flip Flop will be set. This will enable the mainframe multiplexer inputs onto the Shared.buses.

3) At clock edge C, the address and BR/W lines will be latched (U39-U42).

4) At clock edge E, the first flip flop of the timing chain will be cleared. This will enable the SWR' and SMREQ' lines to the shared memory. It will also enable the mainframe data bus transceiver, U44 (the direction of this transceiver will be set by the BR/W latch, U39-15, from the mainframe).

5) At clock edge E, the second flip flop of the timing chain will change state. This inhibits the SWR' line to the memory, which terminates the write. It also generates the DTACK (Data Acknowledge) signal to the mainframe.

6) the mainframe will end the cycle by releasing the BLDS' line. This will cause the mainframe Shared Memory request line to drop disabling the data bus transceiver.

7) At the next positive 3.68 MHz clock edge, the shared memory timing flip flops will return to the idle state. The shared memory access flip flop and address latch clocks will restart.

8) The shared memory is ready for the next cycle.

As a second example, a Z-80 shared memory read would work as follows:

1) The Z-80 MPU initiates a shared memory read. This generates a shared memory request.

2) By default, the Shared Memory Access Select Flip Flop has selected the Z-80 to control the shared busses.

3) At the next negative edge of the 3.68 MHz clock (assume edge C), the address will be latched.

4) At clock edge E, the first timing chain flip flop is cleared. This enables the SMREQ' line, enables the data bus transceiver (U45) between the ZD and SD busses, and it releases the WAIT' line to the Z-80 MPU.

5) At clock edge I, the second timing chain flip flop changes state. This has no effect on a Z-80 read cycle.

6) When the read cycle is complete, the Z-80 will drop MREQ'. This will disable the bus transceiver (U45).

7) At the next positive 3.68 MHz clock edge, the shared memory timing flip flops will return to the idle state. The shared memory access flip flop and address latch clocks will restart.

8) The shared memory is ready for the next cycle.

If a memory cycle is already in progress when a processor tries to request shared memory, that processor will be held off via WAIT' (Z-80) or DTACK' (the mainframe) until it can get access to shared memory.

For more information on the shared memory timing, see the detailed timing diagrams.

3.4: Shared Memory

The Shared Memory Decoder (U31, 9-15) decodes shared address lines 13 and 14 to enable the following blocks of shared memory:

A13	A14	
0	0	Hardware Registers
0	1	RAM block 1 (U25)
1	0	RAM block 2 (U26)
1	1	Unused

3.4.1: Hardware Registers

Eight registers (four read and four write), have been implemented completely in hardware. These registers are selected when SA2 to SA14 are '0' (U38; U30: 10-11, U36: 8-11). The Hardware Register Decoder (U21) decodes shared address lines 0 and 1 and the shared read (SRD) line to enable the appropriate register.

Only bit 7 of write registers 0 and 1 is implemented. This bit is latched by the Reset Flip Flop (U15: 8-13) for register 0 and is latched by the Interrupt Enable Flip Flop (U14: 1-6) for register 1.

The upper nibble of read registers 0 & 1 is implemented by a tri-state multiplexer (U33). SA0 is used to select the appropriate inputs for a read. The lower four data lines (SD0' to SD3') are pulled high by pullup resistors (RP1-5, RP1-12, RP1-13 & RP1-14). Since the shared data bus is inverted (by the 74LS640 transceivers, U44 and U45), unless pulled low, these lines will read '0'. When reading register 0, the tri-state buffer (U35, 1-3) pulls SD2' low to read '1'.

Register 2 is the modem control and status register. Data written to register 2 is latched by the Modem Control Latch (U6). The Modem Status Buffer (U5) is enabled when reading register 2.

Register 3 implements a hardware semaphore. When reading this register, the state of the Semaphore Flip Flop (U14: 8-13) is gated onto SD7' by a tri-state buffer (U35: 4-6). At the trailing edge of the read pulse, this flip flop is set by clocking in a '1'. This implements the indivisible read and set operation. A write to register 3 clears the Semaphore Flip Flop by pulsing the CLEAR' input.

3.4.2: Shared RAM

There are two sockets on the 98628/98629 interface for shared RAM (U25 and U26). These sockets are wired to handle the byte-wide family static RAMs from Mostek. Although the largest RAM currently available is 2K bytes, provisions have been made for the future 8K byte RAMs.

The RAM sockets can accept either a 24 or 28 pin RAM. However, both sockets must use the same size of RAM. When using a 24-pin RAM, it should be even with the bottom of the socket - leaving pins 1, 2, 27 and 28 empty. W3 and W4 (the bottom 2 positions in the 8-pin jumper socket) are used to select the RAM size. For 28-pin RAMs, W3 should be installed; for 24-pin sockets, W4 should be installed.

For the 98628 code, the card will have one 2K-byte RAM in U25 (the U26 socket will be empty). The 98629 code will have a RAM in each socket to give 4K-bytes of RAM. Since 24-pin RAMs will be used, jumper W4 must be installed (jumper position W3 must be vacant).

The shared RAM can be used either for data memory or program memory. The mainframe can 'download' code into shared RAM for the Z-80 to execute.

The first two locations of the first block of RAM have special hardware for interrupts. The Interrupt Register Decoder (U22) decodes accesses to these registers and controls the Interrupt Request (U23: 9-12) and Command (U23: 5-7) flip flops. The Interrupt Request Flip Flop is used to request service of the mainframe. The Command Flip Flop is used to interrupt the Z-80 processor. The output of this flip flop is connected to the CTSB' input of the Z-80 SIO. If the Z-80 SIO is properly programmed, transitions on this line will generate an interrupt to the MPU.

Other RAMs may be used if they meet the following specifications:

1) The RAM is pin-compatible with the card socket wiring.
2) Supply current to the RAM does not cause the card to exceed the mainframe power specs (see chapter 2 for card power specs).
3) The following timing specifications are met:

   Read:
   - CE' active to data valid = 170 ns maximum
   - CE' active to data valid = 220 ns maximum
   - Address valid to data valid = 305 ns maximum
   - Read cycle time = 800 ns maximum

   Write:
   - Address valid to leading edge of WE' = 82 ns maximum
   - Data setup to trailing edge of WE' = 199 ns maximum
   - WE' active pulse width = 255 ns maximum
   - Data hold after trailing edge of WE' = 85 ns maximum
   - Address valid after trailing edge of WE' = 302 ns maximum
   - Write cycle time = 800 ns maximum
   - NOTE: Data may not be valid at the leading edge of WE'.

   For more information see the detailed timing diagrams.
4) The RAM has the following DC characteristics:

   Voltages:
   - Input low = .8 volts maximum
   - Input high = 2.0 volts minimum
   - Output low = .4 volts maximum
   - Output high = 2.4 volts minimum

   Currents:

Input low = 2 mA maximum (total for both RAM)
Input high = 860 uA maximum (total for both RAM)
Output low = 2 mA minimum (plus RAM loading)
Output high = 80 uA minimum (plus RAM loading)

NOTE: These are worst case specifications - they are not derated for higher reliability.

3.5: Z-80 Program ROM

The Program ROM is the only memory-mapped device on the internal Z-80 bus. This ROM is accessed whenever the Z-80 performs a memory read operation with address bit 15 = '0'.

The ROM will be socketed to facilitate ROM updates and exchanges. This will make it easy to change communications protocols by changing the card ROM.

The ROM socket (U29) is designed for 28-pin ROM's. For development 24-pin parts can be used by scraping off the short traces on the circuit side of the board under U29 and adding jumpers. Pin 26 is normally connected to ZA13 and pin 23 is normally connected to ZA11. The jumpers (between U29 and SW1) will connect these pins to +5 Volts.

The 98628 and 98629 code will be released in separate 8K-byte 37000 ROMs. Future software could use other ROMs if they meet the following specifications:

1) The ROM is pin-compatible with the card socket wiring.
2) Supply current to the ROM does not cause the card to exceed the mainframe power specs (see chapter 2 for card power specs).
3) The following ROM timing specs are met:
   Read cycle time = 500 ns minimum
   Address setup to leading edge of CE' = 71 ns maximum
   Address hold after trailing edge of CE' = 86 ns maximum
   Address to valid data = 398 ns maximum
   CE' active to valid data = 286 ns maximum
   OE' active to valid data = 398 ns maximum
   CE' low pulse width = 323 ns maximum
   CE' high pulse width = 187 ns maximum
   CE' inactive to tristate = 187 ns maximum
   NOTE: For more information refer to the detailed timing diagram or to the Z-80 data book.
4) The following DC electrical charcteristics are met:
   Voltage:
     Input low = .8 volts maximum
     Input high = 2.0 volts minimum
     Output low = .4 volts maximum
     Output high = 2.4 volts minimum
   Current:
     Input low = .67 mA maximum (limited by ZA0)
     Input high = 160 uA maximum (limited by ZA0)
     Output low = .46 mA minimum
     Output high = 80 uA minimum

   NOTE: These are worst-case specifications - they have not been derated for higher reliability.

3.6: Default Switches

The default switches are used to setup power-up parameters on the card. This bank of 8 DIP switches (SW1) is accessed 4-bits at a time using the 74LS257 tri-state multiplexer (U20). ZA0 selects between the upper and lower nibble. The multiplexer output is enabled when ZA5 and ZIORQ' are low as detected by 74LS139 decoder (U31: 1-7).

3.7: Oscillator and Clock Driver

The system timing is provided by a 7.3728 MHz oscillator (U18) with a divide-by-two stage (U19: 1-6) for correcting the duty cycle. The resulting 3.6864 MHz signal is used as the system clock. This system clock is used to clock the shared memory arbiter. After waveshaping by the clock driver (Q1, Q2 and associated circuitry), it is fed to the system clock inputs of the Z-80 processor and peripheral chips. It is also divided by 2 again (U15: 1-6) and used as an external input to the Z-80 Clock Timer Chip for faster baud rates.

3.8: Z-80 MPU

The Z-80 microprocessor unit, MPU, (U28) controls the 98628/98629 interface. In a data communications application, it handles the movement of data, error checking, status monitorring, and protocol management.

Since the CPU and peripheral chips are from the same family, the interface between these devices was greatly simplified. These chips have been connected to permit usage of the Z-80 vectorred interrupt scheme and SIO/CPU WAIT/READY feature.

3.9: Z-80 CTC

The Z-80 Counter Timer Chip, CTC, (U12) has four independent timers. Channels 0 and 1 are typically used as baud rate generators. The Zero Count/Timeout (ZC/TO) lines from these channels are passed through divide-by-two counters (U13) to correct the clock duty cycle. The external clock inputs to these channels are connected to a 1.84 MHz clock from the second clock divider flip flop (U15, 1-6) to extend the range of baud rates that can be generated.

CTC channels 2 and 3 are typically used for software timing. These timers may be based on the system clock (internal timing) or may be based on the baud rate clock using the external clock inputs.

3.10: Baud Rate Multiplexer

The Baud Rate Multiplexer (U11) is used to select the baud rate clock for the SIO. This clock may either be internally generated by the CTC or it may be input from the remote device via the line receivers.

This multiplexer is controlled by bits 6 and 7 of the Modem Control Latch (U6).

3.11: Z-80 SIO

The USART used on the 98628/98629 interface is the Z-80 Serial Input/Output, SIO, (U27) chip. This chip, under the control of the Z-80 MPU, serializes data to be transmitted and deserializes received data from the communications link. It also has some error detection capabilities. The Z-80 SIO has both asynchronous and synchronous capability to allow for future protocols without redesign

The Z-80 SIO has two independent full duplex channels. The 'A' channel is connected to the remote device via the line drivers and receivers. The 'B' channel receiver is connected to the 'A' channel transmitter to provide transmitted data trace capability.

The SIO can work together with the MPU for high speed data transfers using wait/ready. If enabled by the firmware, the SIO will put the CPU in a wait state unless a data is ready to be transferred. An interrupt can also abort the CPU from the WAIT state (U16: 11-13, U30: 1-2).

3.12: Line Drivers and Receivers

The line drivers on the 98628/98629 convert TTL voltage levels to the appropriate voltage levels to connect to a remote device. Drivers U1, U2, U3 and U7 implement the unbalanced EIA RS-232C (CCITT V.28) and EIA RS-423 (CCITT V.10) electrical interface standards. (NOTE: These standards are described in Chapter 5: Interface to the Device.) The rise and fall times of the drivers are set by the resistors connected to pin 1. The control signal drivers (U1, U2 and U7) have a 1M Ohm resistor to give approximately 100 microsecond transition times. The data and clock drivers (U3) use a 20K Ohm resistor to provide approximately 2.2 microsecond transitions. Unloaded, the output voltage levels of the drivers should be between +5 to +6 Volts ('ON') or -5 to -6 Volts ('OFF').

Driver U8 implements the differential drive EIA RS-422 (CCITT V.11) standard. The output levels of these drivers (measured to signal ground) should be between 0 and +5 volts. Capacitors (C28 and C29) may be added to the clock and data lines to slow down the signal edges for RFI purposes. They are not used by either the 98628 or 98629 implementations.

The line receivers (U9 and U10) convert the RS-232, RS-422 or RS-423 input voltage levels to TTL levels. In RS-232 or RS-423 mode, the noninverting inputs of the receivers (i.e. pins 2, 6, 10 and 14) are grounded by the cable and the inverting inputs (i.e. pins 1, 7, 9 and 15) are connected to the remote device. In RS-422 mode, both inputs

are driven by the remote device. The absolute maximum voltage levels on the inputs are positive and negative 25 Volts.

On the 98628, the receivers are biased with 6K Ohm resistors (resistor packs R15 and R16) so the receivers will detect the open-circuit case as 'OFF' (failsafe 'OFF'). The negative inputs are biased to -2.37 Volts generated by a Zener diode (CR2) and resistor (R9). The positive inputs are biased to ground. To meet the RS-232 power-down detection requirement, a 1.96K Ohm resistor (R12) is connected
in series with the DM line.

The 98629 does not load the receiver biasing components (R15, R16, CR2, C7 and R9). Instead, 100 Ohm (R18-R20) termination resistors are loaded across the CS, RD and ST lines to match the receivers to the line.

Except for the 98628 and 98629 receiver biasing differences, the differences between the RS-232, RS-423, and RS-422 implementations are all implemented by the cable - no changes are required on the PC board. See chapter 5, Interface to the Device, for more details.

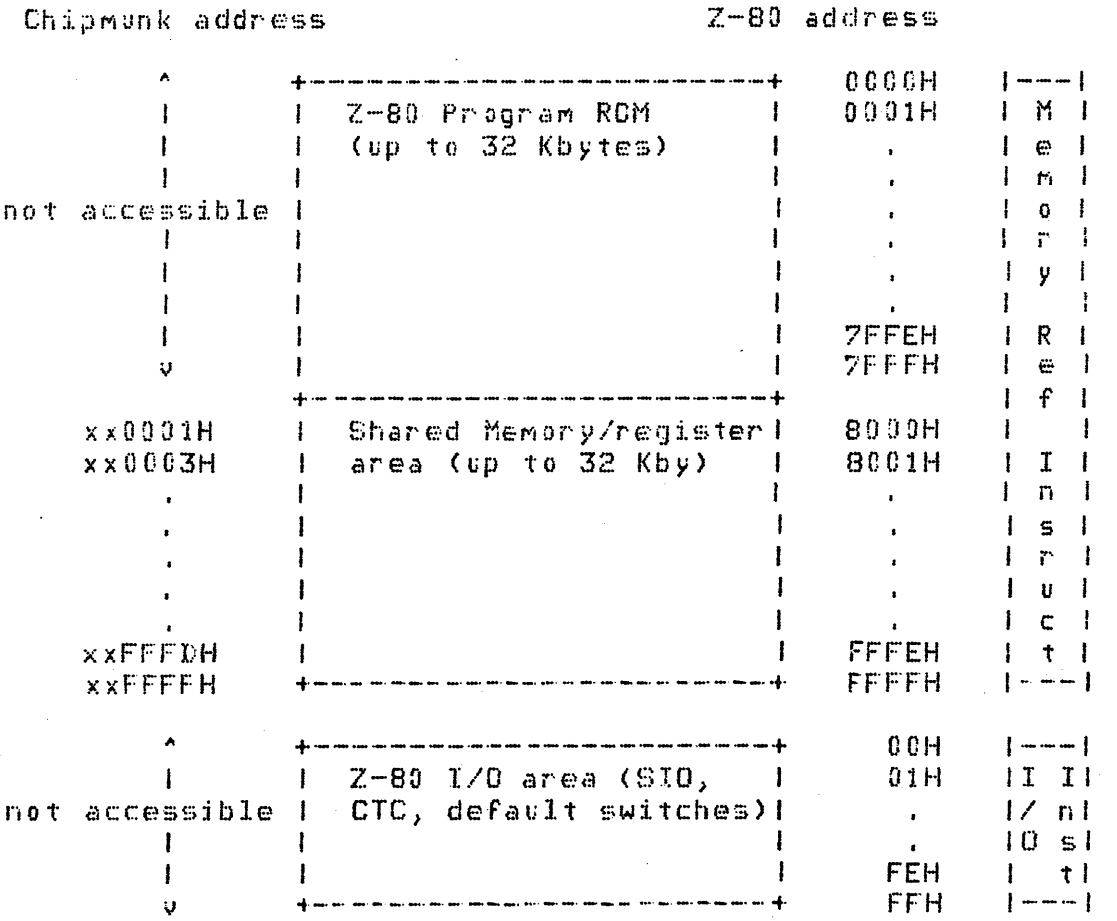
CHAPTER 4: Software Interface

This chapter looks at the registers and memory used to interface to the Z-80 and mainframe software.

The mainframe reserves a 32K word address space for each I/O card. 98628/98629 implements this space as shared registers and RAM. Only the lower byte of each word is implemented - access to the high order byte will result in a bus error.

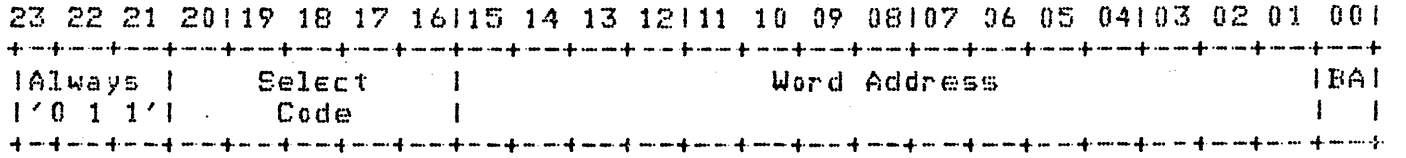
The Z-80 MPU has direct addressing capability of 64K-bytes for memory mapped devices. Memory-mapped devices are accessed using the LD family of instructions. In addition, the Z-80 MPU has a 256-byte address space for I/O devices. These I/O devices are accessed using the I/O instructions such as IN and OUT.

Memory Map



As shown by the memory map, the Z-80 and mainframe use different addresses for shared memory. The Z-80 addresses the shared memory between 8000H and FFFFH with each location implemented. The mainframe addresses shared memory from xx0001H to xxFFFDH with only the odd addresses used. The mainframe addressing scheme is illustrated below:

Mainframe I/O Card Addressing



Bits 21-23: Always '011' for I/O cards. Other codes used for memory internal peripherals.

Bits 16-20: Card select code from 0 to 31.

Bits 01-15: Word Address

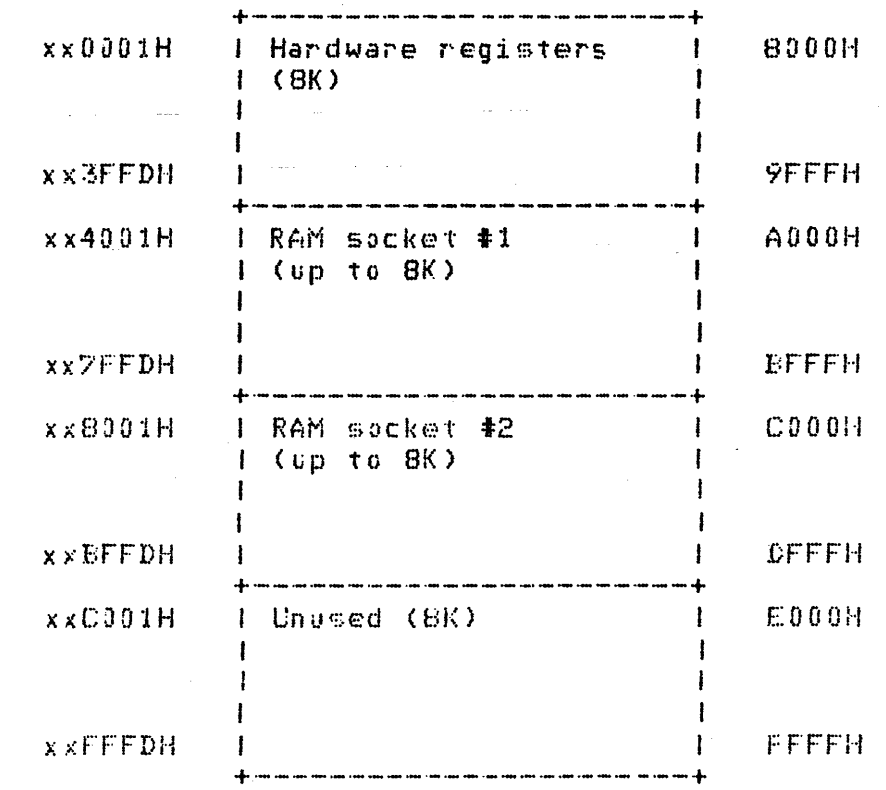
Bit 00: Byte address: 0=upper byte, 1=lower byte. Since 98628/98629 only implements the lower byte of each word, this bit must always be '1'.

Each of these memory blocks will now be described in more detail.

4.1: Z-80 Program ROM

The program ROM contains the code for the Z-80 microprocessor. This ROM may be changed to implement new communications protocols.

4.2: Shared Memory/Register area



4.2.1: Hardware Registers

The first four memory locations are hardware registers with the following bit definitions:

Reset/ID Register

Mainframe address: 0001H
Z-80 address: 8000H

	7	6	5	4	3	2	1	0
Write	RESET Card	Don't Care						

Bit 7: When written as a '1' the card is RESET and a nonmaskable interrupt (NMI) is generated to the Z-80. The Z-80 must clear this bit during its RESET routine.

Bits 0-6: Unimplemented

	7	6	5	4	3	2	1	0
Read	Remote Control	Unused	Smart Card	Card I.D.				
		'0'	'1'	'1'	'0'	'1'	'0'	'0'

Bit 7: If bit 7='1', then this is the remote control interface.

Bit 6: This bit is reserved for future use.

Bit 5: This bit is always a '1' indicating that this interface has a microprocessor and uses one of the smart card drivers.

Bit 0-4: These bits give the ID code unique to this card.

Interrupt/DMA Register

Mainframe address: 0003H
Z-80 address: 8001H

	7	6	5	4	3	2	1	0
Write	Int Enable			Don't Care				

Bit 7: A '1' written to this bit enables the card to interrupt, '0' disables interrupts.

Bits 0-6: These bits are unimplemented.

	7	6	5	4	3	2	1	0
Read	Int En'd	Int Request	Interrupt Level		'0'	'0'	'0'	'0'

Bit 7: This bit indicates the current status of the mainframe interrupt enable flip flop ('1'=interrupts enabled, '0'= interrupts disabled).

Bit 6: If this bit is a '1', the card is requesting an interrupt.

Bits 4-5: These bits give the card interrupt level as set by the switches.

Bits 0-3: These bits are defined for DMA. Since this card does not implement this feature, these bits will read '0'.

Semaphore Register

Mainframe address: 0005H
Z-80 address: 8002H

Write: A write to this register will clear the semaphore. The actual data written is a don't care.

	7	6	5	4	3	2	1	0
Read	Semaph.	Undefined						

Bit 7: This bit gives the status of the semaphore: '0'=not busy, '1'=busy. The semaphore is automatically set after it is read.

Bits 0-6: These bits are not implemented and therefore may read garbage.

Modem Control/Status Register

Mainframe address: 0007H
Z-80 address: 8003H

	7	6	5	4	3	2	1	0
Write	Rx baud int/ext	Tx baud int/ext	OCD4	OCD3	OCD2	OCD1	TR	RS

Bit 7: This bit sets the SIO receiver clock internal (bit 7='1') or external (bit 7='0').

Bit 6: This bit sets the SIO transmitter clock internal(bit 6='1') or external (bit 6='0')

Bits 2-5: These active high bits control the optional circuit drivers (OCDs) to the remote device. The exact definition of each signal depends on the cable or pod in use as summarized below:

OCD1: SR - Signal Rate Select (RS-232 & RS-449 cables)

OCD2: SRS - Secondary Request to Send (RS-232 cables)
CSI - Clear to Send Inhibit (Multipoint pod)
AUTO - Auto Dial/Answer (HP modem)

OCD3: LL - Local Loopback (RS-449 cables)
MM - Monitor Mode (Multipoint pod)

OCD4: RL - Remote Loopback (RS-449 cables)

Bit 1: This active high bit controls the Terminal Ready (TR) line to the remote device.

Bit 0: This active high bit controls the Request to Send (RS) line to the remote device.

	7	6	5	4	3	2	1	0
Read	Undefined		SIO Ch A WAIT	OCR2	OCR1	CS	RR	DM

Bits 6-7: These bits are unimplemented and may be read in either state.

Bit 5: This bit indicates the state of the WAIT/READY line from channel A of the SIO. When high, this line is in the WAIT state.

Bits 3-4: These active high bits indicate the status of the optional character receivers (OCRs) from the remote device. Their exact definition will depend on the cable or pod in use as specified below:

OCR1: IC - Incoming Call (RS-232 & RS-449 cables)

OCR2: SRR - Secondary Receiver Ready (Secondary Data Carrier Detect) (RS-232 cables)
RSD - Request to Send from Downstream (Multipoint Daisy Chain pod)
SI - Signal Rate Indicator (Modem pod)

Bit 2: This active high signal indicates the status of the Clear to Send (CS) line from the remote device.

Bit 1: This active high signal indicates the status of the Receiver Ready (RR - Data Carrier Detect for RS-232) line from the remote device.

Bit 0: This active high bit indicates the status of the Data Mode (DM - Data Set Ready for RS-232) line from the remote device.

4.2.2: RAM Registers

There are 2 RAM sockets on the 98628/98629 interface. The currently available 1K-byte 4801 and 2K-byte 4802 can be used. As larger static RAM densities become possible, 4K-byte and 8K-byte components may also be used.

RAM locations 4001H and 4003H (mainframe word addressses) have additional hardware to generate interrupts. Accesses to these registers will have the following effect:

Register	Mainframe Access	Z-80 Access
4801H Write	No effect	Generate mainframe inter.
4801H Read	Clear mainframe inter.	No effect
4803H Write	Generate Z-80 inter.	No effect
4803H Read	No effect	Clear Z-80 interrupt

See the software section of this ERS for the definition of the other RAM locations.

4.3: I/O-Mapped Devices

The following devices are I/O mapped on the internal Z-80 bus. They are accessed with I/O statements such as IN and OUT. To avoid enabling two devices at one time, the addresses should be used EXACTLY as shown.

4.3.1: Z-80 SIO

70H: Channel A Data
71H: Channel A Control/Status
72H: Channel B Data
73H: Channel B Control/Status

The Z-80 SIO has two independent full-duplex channels. Channel A is used to communicate with the remote device. Channel B on the SIO has two uses:

1) Providing vectored interrupts for mainframe requests.
2) Providing trace information for transmitted data.

For high-speed operation, the WAIT/READY feature of the SIO can be used in conjunction with the Z-80 MPU block move instruction. An interrupt will pull the microprocessor out of a WAIT state. This makes it possible to set up a timer as a 'watchdog' to catch 'hang' conditions.

See the Z-80 SIO Technical Manual for more details on the SIO.

4.3.2: Z-80 CTC

B0H: Channel 0
B1H: Channel 1
B2H: Channel 2
B3H: Channel 3

The Z-80 CTC has four independent timers. They may be used for the following functions:

Timer C: This timer may be used to generate the internal transmit baud rate for the SIO. It may be used in timer mode for the lower baud rates or in counter mode for the higher baud rates. There is an overlap range in which either choice is possible. If an internal transmit baud clock is not needed, then the timer can be used for software timing. The time constants (TC) written to the CTC can be calculated as follows:

Baud Rate Generator:
Counter Mode:
Async (x16 clock): TC = 57,600/Baud Rate
(Range: 225 to 57.6K baud)
Sync (x1 clock): TC = 921,600/Baud Rate
(Range 3.6K to 922K baud)
Timer Mode (Prescalar = 16)
Async (x16 clock): TC = 7200/Baud Rate
(Range: 28.1 to 7200 baud)
Sync (x1 clock): TC = 115,200/Baud Rate
(Range: 449 to 115K baud)

Software Timer: Same as timer 2 (internal clock only)

Timer 1: This timer is used to generate the receive baud rate. It behaves in the same manner as timer 0.

Timer 2: This timer is used to do software timing. In timer mode, this timer provides real-time interrupts. In counter mode, it will provide interrupts based on the transmit baud clock from the baud rate multiplexer. The time constant (TC) can be calculated from the following equations:

Internal Clock:
Prescalar=16: Time Period = TC x 4.34 microsec.
Prescalar=256: Time Period = TC x 69.4 microsec.

External Clock:
Async (x16 clock): Time Period = TC/16 bit times
Sync (x1 clock): Time Period = TC bit times

The output of timer 2 is used as a clock for the transmitter of channel B of the SIO. The channel B transmitter can be used in conjunction with this timer for very long timeouts.

Timer 3: This timer behaves in the same manner as timer 3 except that in counter mode it is slaved to the receive clock from the baud rate multiplexer.

For more information, see the Z-80 CTC Technical Manual.

4.3.3: Default Switches

D0H: Switch Block A (upper nibble)
D1H: Switch Block B (lower nibble)

The default switches are used to select some of the default operating parameters (i.e. baud rate, bits/character, etc). The exact definition of these switches is dependent on the card software.

Chapter 5: Interface to the Device

98628 is designed to support the following electrical interface standards:

EIA RS-232C (similar to CCITT V.24/V.28)
EIA RS-422 (similar to V.11)
EIA RS-423 (similar to V.10)

Each of these standards will be briefly described here. For more information, refer to the appropriate standard.

5.1: Electrical Standards

5.1.1: RS-232C

RS-232C was adopted by the Electronics Industry Association (EIA) in 1969. It provides for asynchronous and synchronous data communications at rates up to 20 kilobits per second. A cable length of 50 feet (15 metres) or shorter is recommended; however, longer cables are permissible if the load capacitance does not exceed 2500 picofarads. A 25 pin D subminiature connector has become the defacto RS-232 standard.

The CCITT international standards organization split RS-232C into two standards V.24 and V.28. These standards specify an interface that is very similar (but not identical) to RS-232. V.24 specifies the functional characteristics and V.28 specifies the electrical characteristics.

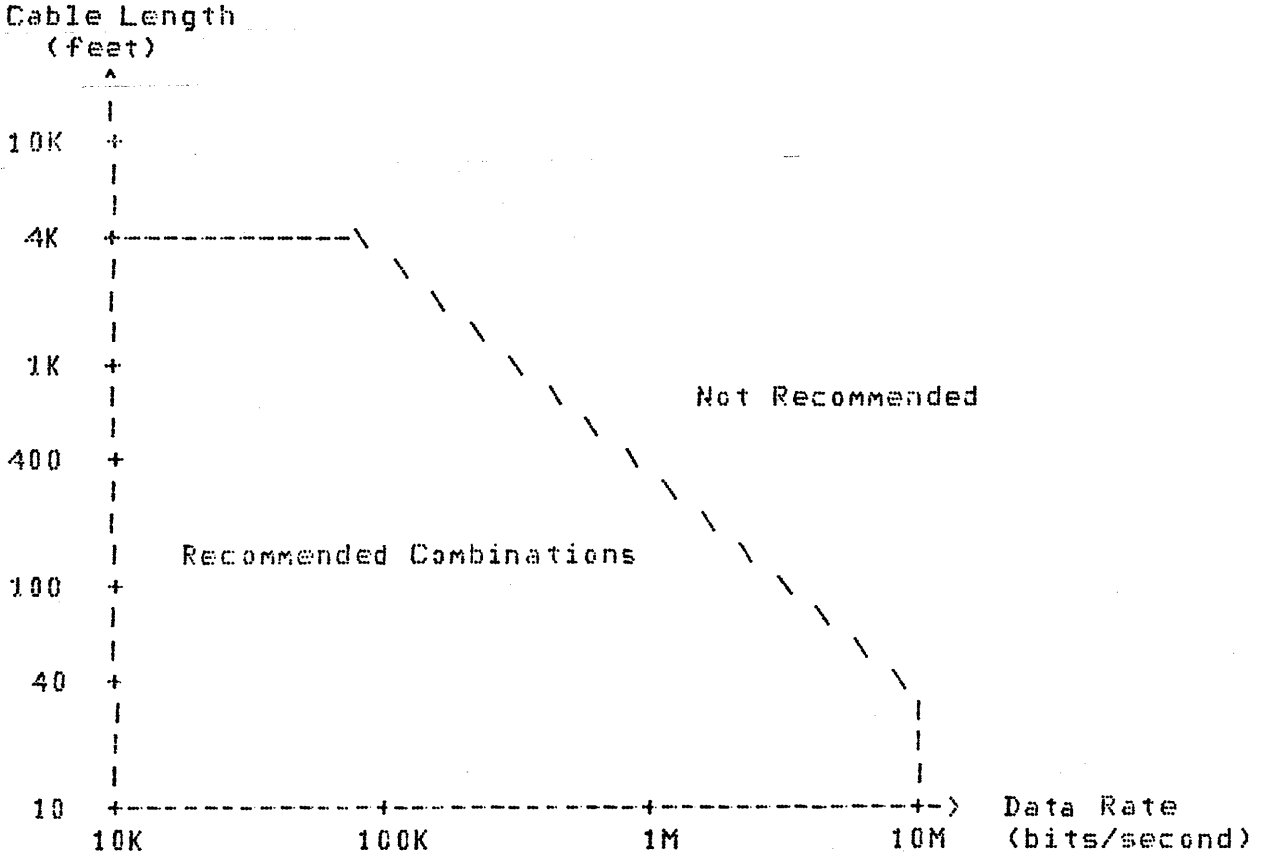
5.1.2: RS-449/422/423

RS-449, RS-422 and RS-423 were developed to provide longer signalling distances and higher data rates than RS-232C. RS-449 defines the functional characteristics of the interface. RS-422 and RS-423 describe the electrical characteristics of the interchange circuits.

RS-449 specifies 27 interchange circuits - essentially a superset of the RS-232 lines. Two connectors are specified: a 37-pin connector for the primary channel and an optional 9-pin connector for the secondary channel. These connectors belong to the same family as the RS-232 connector.

5.1.3: RS-232C/RS-449 Compatibility

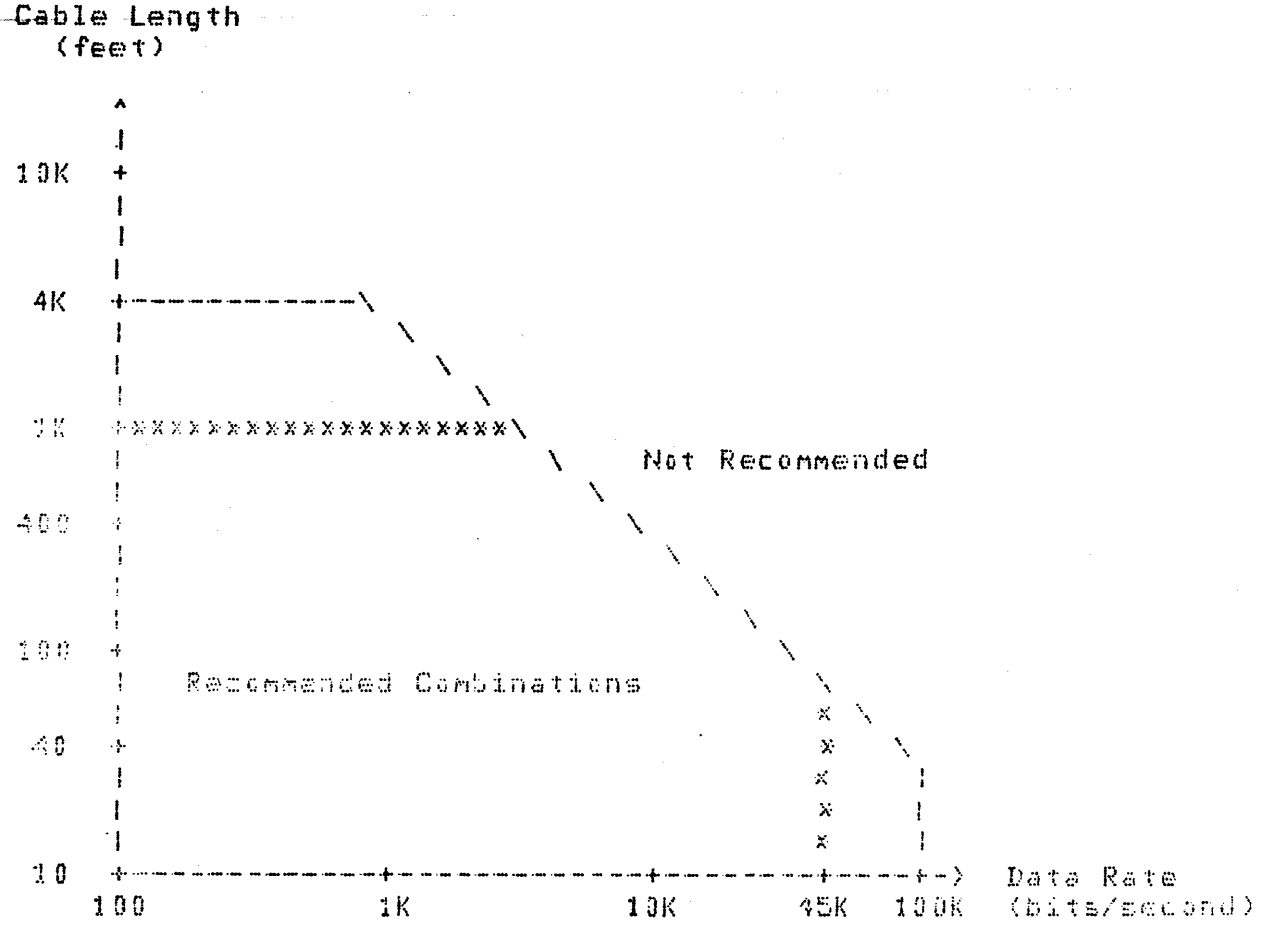
RS-422 specifies a balanced, twisted-pair interchange circuit for high-speed operation. **The maximum cable length and maximum data rate ~~are interdependent.~~** The cable below illustrates the recommended combinations.



RS-422 Modulation Rate Versus Cable Length

RS-423 defines an unbalanced interchange circuit that can be compatible with RS-232C. The RS-423 data rates and cable length are also interdependent as shown by the dashed lines in the chart below.

With the RS-423 waveshaping used on 98628, the combinations of baud rate and cable length are further restricted to the area bounded by the asterisks ('*'). Provisions were made for this type of an implementation by the RS-423 standard.



RS-449 and RS-423 were specified with RS-232C compatibility in mind. When connecting an RS-232C device to a RS-449/423 device, the worst case specifications of both standards must be met. This limits the signalling rate to 20 kilobaud and the cable length to 50 feet. The chart below compares the RS-232C, CCITT V.24 and RS-449 signals. Throughout this ERS, the RS-449 names will be used to identify signals.

RS-449		RS-232C		CCITT V.24	
SG	Signal Ground	AB	Signal Ground	102	Signal Ground
SC	Send Common			102a	DTE Common
RC	Receive Common			102b	DCE Common
IS	Term. in Service				
IC	Incoming Call	CE	Ring Indicator	125	Calling Indicator
TR	Terminal Ready	CD	Data Term. Ready	108/2	Data Term. Ready
DM	Data Mode	CC	Data Set Ready	107	Data Set Ready
SD	Send Data	BA	Transmitted Data	103	Transmitted Data
RD	Receive Data	BB	Received Data	104	Received Data
TT	Terminal Timing	DA	Tx Timing (DTE)	113	Tx Timing (DTE)
ST	Send Timing	DB	Tx Timing (DCE)	114	Tx Timing (DCE)
RT	Receive Timing	DD	Receiver Timing	115	Rec. Timing (DCE)
RS	Request to Send	CA	Request to Send	105	Request to Send
CS	Clear to Send	CB	Clear to Send	106	Ready for Sending
RR	Receiver Ready	CF	Data Carrier Det.	109	Received Line Signal Detect
SQ	Signal Quality	CG	Signal Quality Detector	110	Data Signal Quality Detect
NS	New Signal				
SF	Select Frequency			126	Select Tx Freq.
SR	Signalling Rate Selector	CH	Data Signal Rate Selector (DTE)	111	Data Signalling Rate Sel. (DCE)
SI	Signalling Rate Indicator	CI	Data Signal Rate Selector (DCE)	112	Data Signalling Rate Sel. (DCE)
SSD	Secondary Send Data	SBA	Secondary Trans'd Data	118	Transmitted Back. Channel Data
SRD	Secondary Receive Data	SBB	Secondary Rec'd Data	119	Received Back. Channel Data
SRS	Secondary Request to Send	SCA	Secondary Request to Send	120	Trans. Back. Chan Line Signal
SCS	Secondary Clear to Send	SCB	Secondary Clear to Send	121	Backward Channel Ready
SRR	Secondary Receiver Ready	SCF	Secondary Data Carrier Detect	122	Back. Chan. Rec. Line Sig. Det.
LL	Local Loopback			141	Local Loopback
RL	Remote Loopback			140	Remote Loopback
TM	Test Mode			142	Test Indicator
SS	Select Standby			116	Select Standby
SB	Standby Indicator			117	Standby Indicator

5.1.4: DTD Electrical Interface Standards

The interface to the remote device on 98628 is consistent with the Electrical Interface Standards for D.T.D (Data Terminals Division) products. This compatibility makes it possible for 98628 to leverage the pods built by DTD.

The physical connection to the outside world is a 50-pin connector on the rear panel of the interface card. This connector is of the same family as the standard HPIB connector.

The DTD standard specifies four levels of implementation. 98628 will implement standard C, the most complete level of implementation. The pin numbers of the 50 pin connector are defined as follows:

		<-- To DCE -->						<-- From DCE -->	
	OCD3	<--	26	*	+	*	1	-->	OCD4
	SD(A)	<--	27	*	|	*	2	-->	SD(B)
	RS(A)	<--	28	*	|	*	3	-->	RS(B)
	TR(A)	<--	29	*	|	*	4	-->	TR(B)
	Dummy ON	<--	30		|		5	-->	Dummy OFF
	OCR3	-->	31		|		6	-->	OCR4
	TT(C)		32	*	|	*	7	-->	TT(u)
	TT(A)	<--	33	*	|	*	8	-->	TT(B)
			34		|	*	9	<--	OCR1
	+5 V Supply		35	*	|	*	10		+12 V Supply
	+5 V Supply		36	*	|	*	11		-12 V Supply
	SD(C)		37	*	|	*	12	-->	SD(u)
	RS(C)		38	*	|	*	13	-->	RS(u)
	TR(C)		39	*	|	*	14	-->	TR(u)
	OCD1	<--	40	*	|	*	15	-->	OCD2
	ST(A)	-->	41	*	|	*	16	<--	ST(B/C)
	RD(A)	-->	42	*	|	*	17	<--	RD(B/C)
	RT(A)	-->	43	*	|	*	18	<--	RT(B/C)
	CS(A)	-->	44	*	|	*	19	<--	CS(B/C)
[RS-232C]	DM(A)	-->	45	*	|	*	20	<--	DM(B/C)
	RR(A)	-->	46	*	|	*	21	<--	RR(B/C)
	CCR2	-->	47	*	|	*	22		RC
	SG		48	*	|	*	23		SC
			49		|	*	24		Shield
			50		+	*	25	<--	DM(A) [RS-422/423]

* Implemented by 98628.

(A), (B) represent the pairs of conductors used on differential drivers or receivers as specified by RS-422. (C) represents the ground side of an unbalaced driver or differential receiver as specified in RS-422 and (u) represents the primary output circuit of an unbalanced RS-423 driver. RS-423 drivers will have linear 2.2 microsecond

waveshaping to guarantee interoperability with RS-232C circuits.

To meet the European requirements for V.10, V.11 and V.24, two DM(A) lines are needed. Pin 45 will be used for RS-232, pin 25 for RS-422 and RS-423.

5.2: Cables

5.2.1: RS-232C Cables

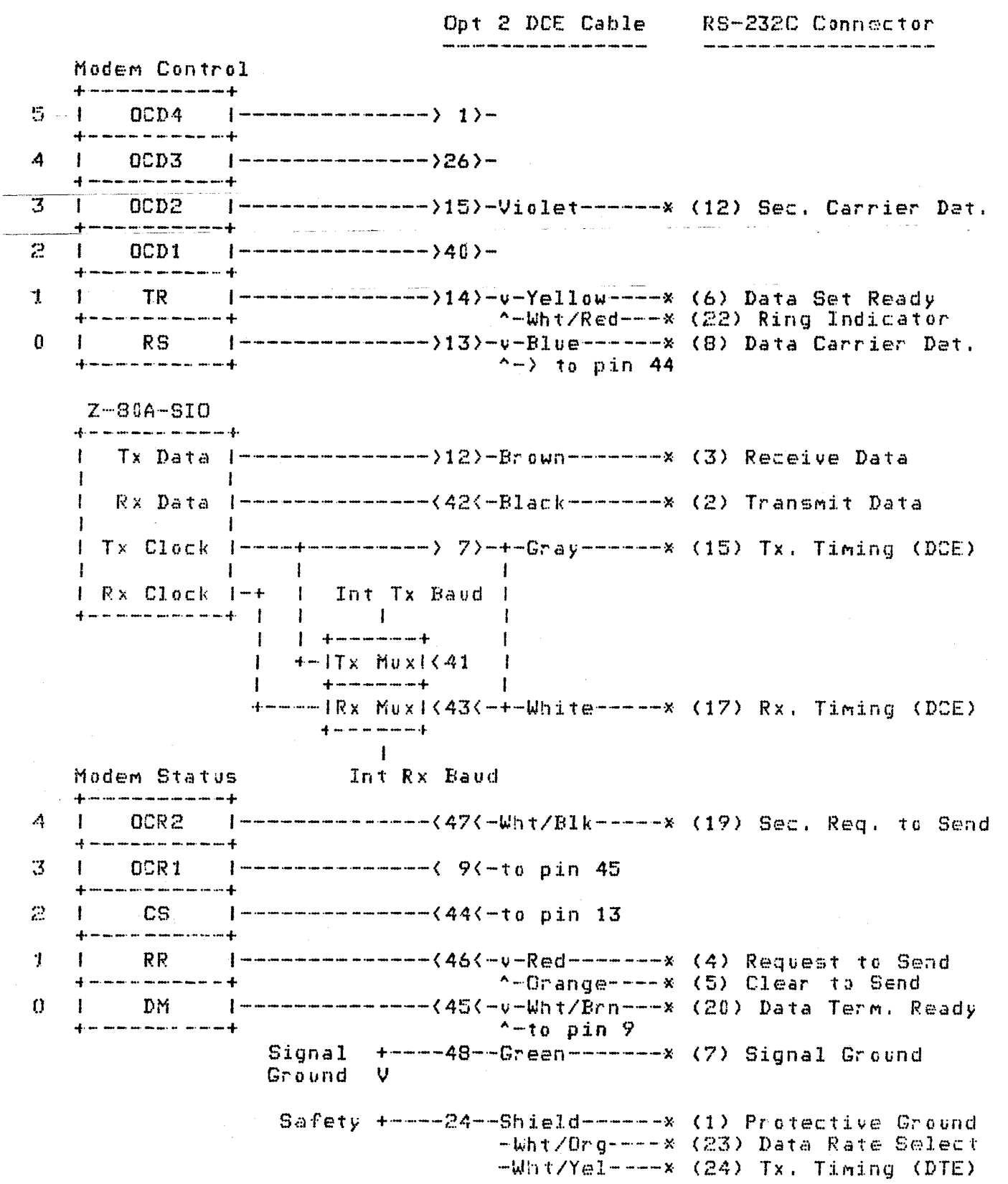
The 98628A will share two RS-232C option cables with the 98626A interface card:

Option 001: DTE Cable (similar to 98046 Option 1 Cable)
Option 002: DCE Cable (similar to 98046 Standard Cable)

These cables will be shipped with the test connectors currently being built for the 98046 cables (DTE: HP P/N 1251-6625. DCE: HP P/N 1251-6624).

Data Terminals Division makes a family of RS-232C cables that are compatible with the 98628; however, we do not plan to support them. The Option 001 DTE cable is the same as the DTE 13222M European Modem Cable with the exception of improved shield grounding.

A functional illustration of these cables is shown on the pages that follow. The 98628 components are shown to the left and the cable to the right. The cable colors and pin numbers at each connection are given. For all RS-232C cables, the negative inputs of the receivers are tied together with Receive and Send Common. These pin numbers are: 16 [ST(B/C)], 17 [RD(B/C)], 18 [RT(B/C)], 19 [CS(B/C)], 20 [DM(B/C)], 21 [RR(B/C)], 22 [RC] and 23 [SC].

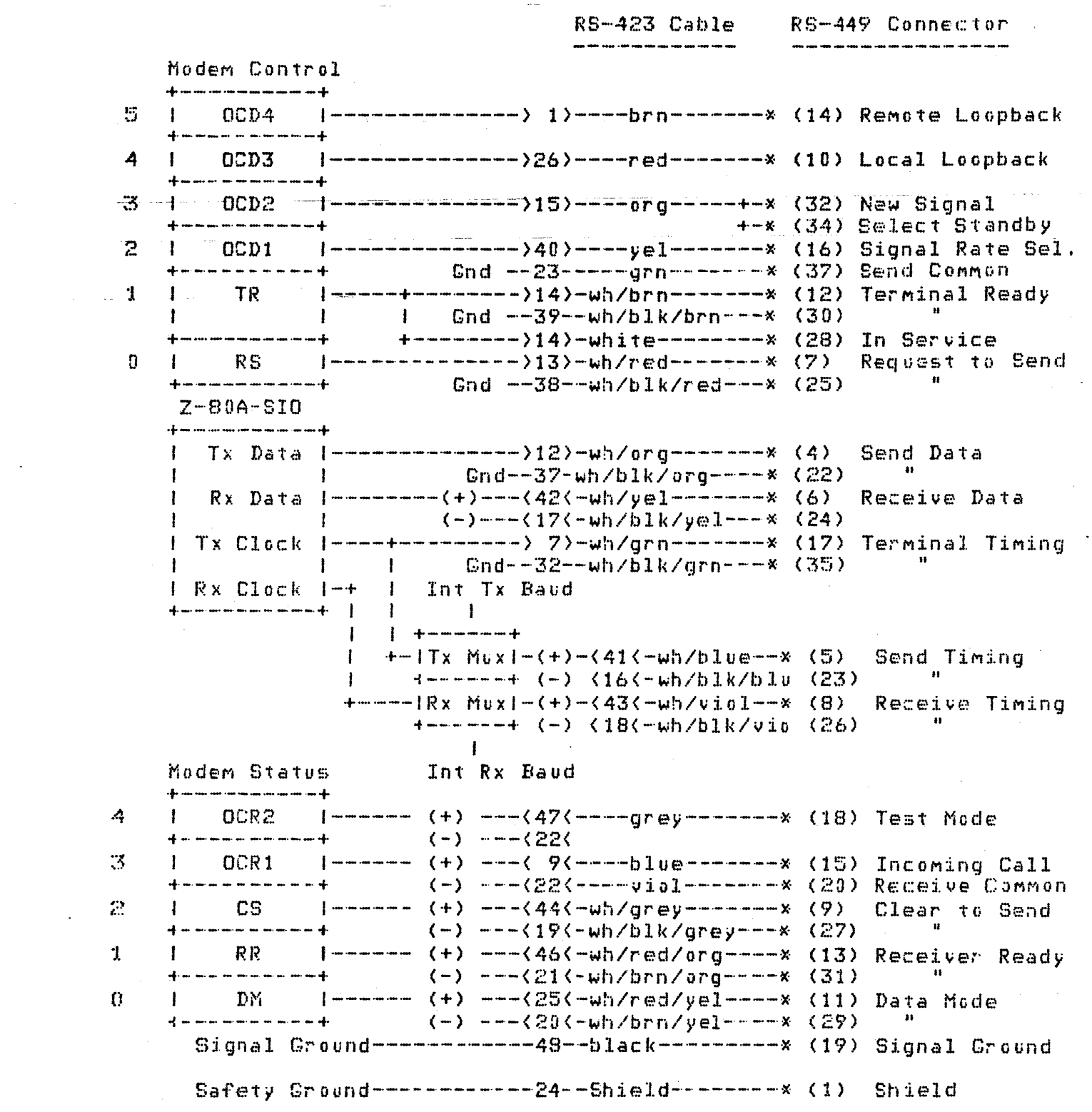

Opt 2 DCE Cable
RS-232C Connector
Modem Control
5 OCD4) 1)-
4 OCD3)26)-
3 OCD2)15)-Violet x (12) Sec. Carrier Det.
2 OCD1)40)-
1 TR)14)-Yellow x (6) Data Set Ready
Wht/Red x (22) Ring Indicator
0 RS)13)-Blue x (8) Data Carrier Det.
to pin 44
Z-80A-SIO
Tx Data)12)-Brown x (3) Receive Data
Rx Data (42(-Black x (2) Transmit Data
Tx Clock) 7)-Gray x (15) Tx. Timing (DCE)
Rx Clock
Int Tx Baud
Tx Mux (41
Rx Mux (43(-White x (17) Rx. Timing (DCE)
Int Rx Baud
Modem Status
4 OCR2 (47(-Wht/Blk x (19) Sec. Req. to Send
3 OCR1 (9(-to pin 45
2 CS (44(-to pin 13
1 RR (46(-Red x (4) Request to Send
Orange x (5) Clear to Send
0 DM (45(-Wht/Brn x (20) Data Term. Ready
to pin 9
Signal Ground 48-Green x (7) Signal Ground
Safety 24-Shield x (1) Protective Ground
Wht/Org x (23) Data Rate Select
Wht/Yel x (24) Tx. Timing (DTE)

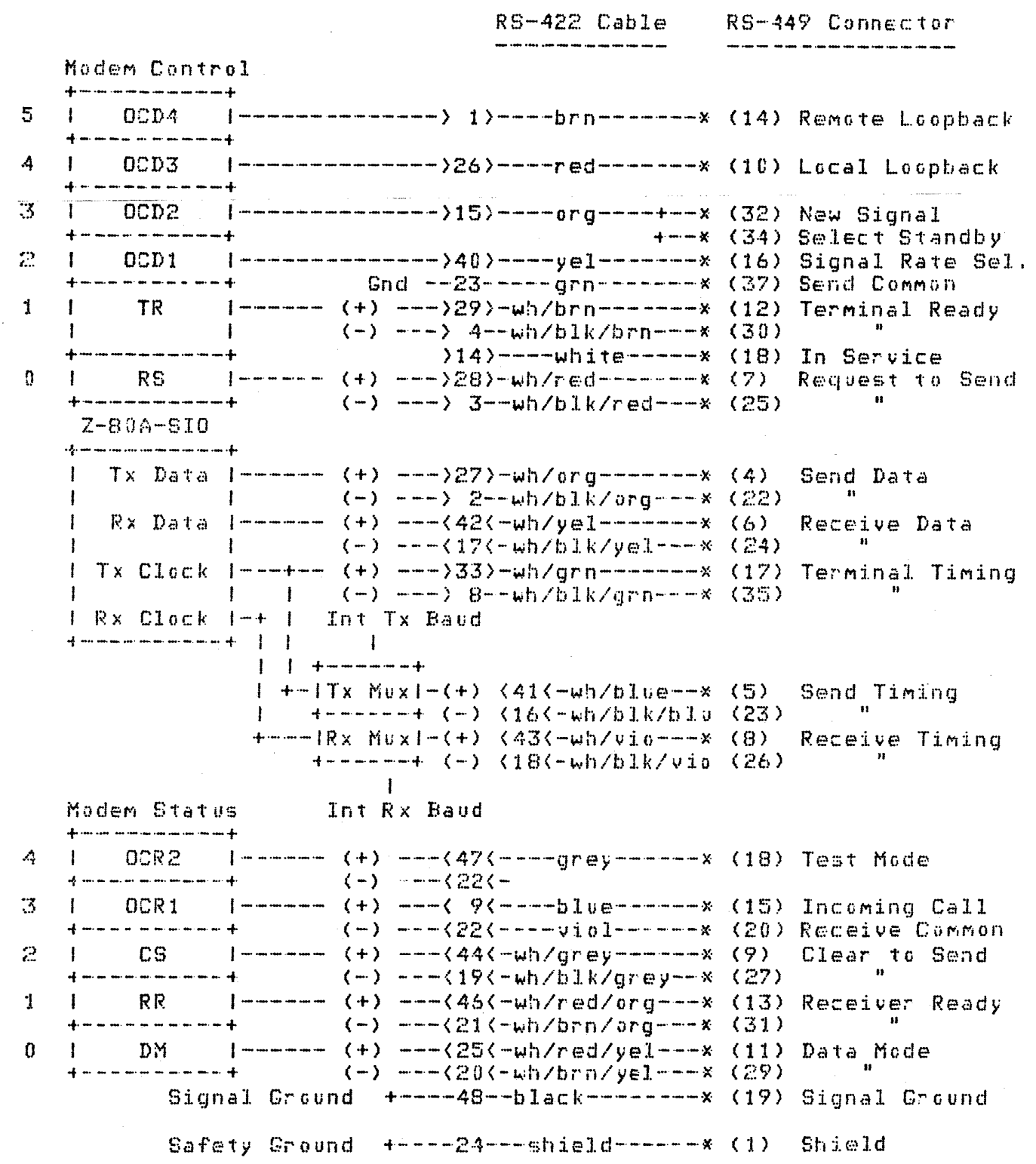
5.2.2: RS-449 Cables

One RS-449 DTE cable will be built for 98628 - for RS-423. No RS-449 DCE (female) cables are planned at this time. A user needing this capability can use a modem eliminator cable. The RS-422 cable needs three 100 ohm terminating resistors installed between the two lines of RD, ST, and RT and so will not be built at this time.

Both RS-449 cables are intended for direct or modem connections in the US or Europe. Since the secondary channel requires a second 9-pin connector, the 'Secondary Request to Send' and 'Secondary Receiver Ready' lines are not implemented for economy reasons.

The drawings on the next two pages illustrate the RS-449 cables.


RS-423 Cable
RS-449 Connector
Modem Control
OCD4
OCD3
OCD2
OCD1
TR
RS
Z-80A-SIO
Tx Data
Rx Data
Tx Clock
Rx Clock
Int Tx Baud
Tx Mux
Rx Mux
Modem Status
Int Rx Baud
OCR2
OCR1
CS
RR
DM
Signal Ground
Safety Ground
Remote Loopback
Local Loopback
New Signal
Select Standby
Signal Rate Sel.
Send Common
Terminal Ready
In Service
Request to Send
Send Data
Receive Data
Terminal Timing
Send Timing
Receive Timing
Test Mode
Incoming Call
Receive Common
Clear to Send
Receiver Ready
Data Mode
Signal Ground
Shield


RS-422 Cable
RS-449 Connector
Modem Control
OCD4
OCD3
OCD2
OCD1
TR
RS
Z-80A-SIO
Tx Data
Rx Data
Tx Clock
Rx Clock
Int Tx Baud
Tx Mux
Rx Mux
Int Rx Baud
Modem Status
OCR2
OCR1
CS
RR
DM
Signal Ground
Safety Ground
Remote Loopback
Local Loopback
New Signal
Select Standby
Signal Rate Sel.
Send Common
Terminal Ready
In Service
Request to Send
Send Data
Receive Data
Terminal Timing
Send Timing
Receive Timing
Test Mode
Incoming Call
Receive Common
Clear to Send
Receiver Ready
Data Mode
Signal Ground
Shield

5.3: Pods

5.3.1: HP Data Link Adapter

HP the Data Link (DL) Adapter, 13264A, converts the RS-232C signals from 98628 to the differential signal needed by the DL link. This pod is manufactured by the Grenoble (France) Division.

The lines from the 50-pin connector implemented by BILBO are:

pin 10: +12V Supply (160 mA typical)
pin 11: -12V Supply (23 mA typical)
pin 12: Send Data
pin 13: Request to Send
pin 23: Send Common (used as logic ground)
pins 35 and 36: +5V Supply (30 mA typical)
pin 42: Receive Data
pin 44: Clear to Send
pin 48: Signal Ground (used as 'Not Power On' signal)

The 'B' inputs to the receivers are also tied to logic ground.

Transmission on the link is inhibited until the 'Not Power On' signal goes low (when the pod is connected to 98628). After power up, the link drivers are in their high impedance state unless the 'Request to Send' (RS) line is active. Whenever RS is raised, BILBO immediately responds with 'Clear to Send' (CS). Data from the 'Transmit Data' line is then sent to the link by the drivers.

The BILBO link receivers sense the link, convert the signals to RS-232C and send the data to 98628 as 'Receive Data'. Data is received by the pod at all times - even when it is transmitting.

5.3.2: Current Loop Converter

The Current Loop Converter, 13266A, provides a 20 mA interface for the 98628. With default switches and wiring options, the current loop interface can be configured with active or passive driver and receiver elements.

Current loop is used in applications that require data communications over longer distances than are possible with standard RS-232C. It is also commonly used in electrically 'noisy' environments.

The lines from 98628 that are implemented by the Current Loop Pod are:

pin 10: +12V Supply (90 mA max.)
pin 11: -12V Supply (80 mA max.)
pin 12: Send Data
pin 13: Request to Send
pin 17: RD(B) (used as logic ground)
pin 23: Send Common (used as logic ground)
pins 35 & 36: +5V Supply (200 mA max.)

pin 42: Received Data
pin 44: Clear to Send
pin 46: Receiver Ready
pin 48: Signal Ground (used as logic ground)
The 'B' inputs to the receivers are also tied to logic ground.

None of the modem control lines is used by the current loop pod. Therefore, their state is a complete don't care to the pod. However, as a convenience to the mainframe, the 'Request to Send' (RS), 'Clear to Send' (CS) and 'Receiver Ready' (RR) lines from 98628 are connected together.

5.3.3: 300 Baud Modem

The 300 baud modem, 13265A, is a Bell 103/113 compatible asynchronous modem for connecting directly to the US Public Switched Telephone Network. This modem is originate only with both auto dial and manual originate capabilitiy.

The lines implemented by the Modem Pod include:
pin 10: +12V Supply (45 mA)
pin 11: -12V Supply (45 mA)
pin 12: Send Data
pin 14: Terminal Ready
pin 15: CCD2 (Auto dial/answer)
pins 35 & 36: +5V Supply (100 mA)
pin 42: Received Data
pin 44: Clear to Send
pin 45: Data Mode
pin 46: Receiver Ready
pin 48: Signal and power ground

Refer to the '13265A 300 Baud Modem Pod External Reference Specification' for more information on controlling the modem.

5.3.4: Daisy Chain Pod

Due to the power required by the Daisy Chain Pod, it will not be be supported by 98628.

Chapter 6: Testing and Service

This chapter describes the tools for testing and debugging the 98628 serial I/O interface card. These tools will be used for:

- hardware development testing
- production testing and debug
- customer hardware assurance tests
- service test and debug

98628 has four main test tools:

1) 3060 Board Test
2) Power-up Self-Test
3) Comprehensive Test Program
4) Signature Analysis Tests

6.1: 3060 Board Test

The 3060 board test will be used by Production to test the loaded PC boards. This test will be specified and written by the Chipmunk testing group.

6.2: Power-Up Self-Test

This test is included in the 98628 and 98629 ROMs and is run each time the card is powered up. After the test, the card will 'log in' to Chipmunk with the status of the test. If the card failed, a BASIC error will be generated. If for some reason the card cannot log in, Chipmunk will ignore the card and give errors for all card accesses (except for READIO and WRITEIO). See the 98628 firmware specifications for more details.

The power-up self-test performs the following tests:

- ROM checksum
- Shared RAM alternating bit pattern test
- Clock Timer Chip timeout tests
- Serial I/O register access tests
- Z-80 interrupt test
- Semaphore tests

On completion of these tests, 98628 will interrupt the mainframe with the 'log in'.

6.3: Comprehensive Test Program

The comprehensive test program is available in two different forms: one for the customer/service personnel and the other for production testing. The customer/service test is contained on floppy disc number 09826-10029. The production test version is on floppy number ET-14657.

The 98628 ROM code requirements for any HPL test program are as follows:

A. Card ID at location A017 (Hex) (card address):
   ID = FF (Hex) hangs in loop after RESET;
   ID = FE (Hex) releases RESET FF, hangs until ID = 0, then jumps to location A008 (Hex).

B. Card self-test failure information must be stored in location A016 (Hex) (card address).

C. Command Register must be read (to clear Command FF) before checking card ID.

The common section of the test checks the parts of the card that do not depend on the cable type. The unique section will vary somewhat depending on the type of pod, cable or test connector.

6.3.1: Test Connectors

The test connectors are wired as follows:

Signals	5061-4248 (ESK unbalanced)	5061-4247 (ESK balanced)		5061-4220 (RS-449)	
SD-->RD	12-->42	27-->42	2-->17	4--> 6	22-->24
TT-->RT	7-->43	33-->43	8-->18	17--> 8	35-->26
RS-->ST	13-->41	28-->41	3-->16	7--> 5	25-->23
TR-->CS	14-->44	29-->44	4-->19	12--> 9	30-->27
OCD1-->OCR1	40--> 9	40--> 9		16-->15	
OCD2-->OCR2	15-->47	15-->47		No connection	
OCD3-->DM	26-->45	26-->25		10-->11	
OCD4-->RR	1-->46	1-->46		14-->13	
GND	16 - 23	20 - 23		20,29,31,37	
IS-->OCR2				28-->18	

1251-6624 (RS-232C DCE)

SD-->RD	2--> 3
..-->RT	24-->17 (24 does not connect to anything)
RS-->RR	8--> 4
TR-->DM	6-->20
OCD2-->OCR2	12-->19

1251-6625 (RS-232C DTE)

```
  SD-->RD              2--> 3
  TT-->RT             24-->17
  RS-->RR,CS,OCR1      4--> 8, 5,22
  TR-->DM             20--> 6
OCD1-->ST             23-->15
OCD2-->OCR2           19-->12
  ..-->..             14-->25   (14 and 25 do not connect to anything)
```

6.3.2: Common Test Module

A. Interface Hardware
   1. Check card I.D. register (should read X101 0100)
   2. Check interrupt/DMA Register (should read (00XX 0000)
   3. Check setting and clearing semaphore

B. RAM Memory Test
   1. Checkerboard memory test executed from the mainframe.
   2. Rotate walking '0' and walking '1' through a memory location.

C. Z-80 CPU Tests
   1. Verify Z-80 cleared RESET FF (U15: 8-13) at the end of its reset routine.
   2. Download Z-80 diagnostic code to card RAM. Code is as follows:

```
                                NAME "RAM allocation"
                                ORG  8000H
8000            RESET_ID:       DEFS 1
8001            INT_DMA:        DEFS 1
                IRFF:           EQU  01000000B
8002            SEMAPHORE:      DEFS 1
8003            MODEM_LINES:    DEFS 1
                                ORG  0A000H
                RAM_SIZE:       EQU  2*1024
                RAM_END:        EQU  $+RAM_SIZE-1
                STACK_TOP:      EQU  RAM_END
A000            INT_COND:       DEFS 1

                ;COMMAND:  M/F Address = M+2
                ;DATA:  M/F Address = M+4
                ;ADDRESS:  M/F Address:
                ;             Upper Byte (Also I/O) = M+6
                ;             Lower Byte = M+8
                ;TEST COMMAND REGISTER:  M/F Address = M+10
```

```
A001                COMMAND:        DEFS 1
A002                DATA:           DEFS 1
A003                ADDRESS:        DEFS 2
A005                TEST_COMMAND:   DEFS 1

                                    PROG

                                    ORG 0A008H
A008 1816                           JR   CMD_WAIT

                                    ORG  0A020H
A020 3AA005         CMD_WAIT:       LD   A,[TEST_COMMAND]
A023 E60F                           AND  00001111B

                    ;Command 0:     NOP

A025 28F9                           JR   Z,CMD_WAIT

A027 ED4BA003                       LD   BC,[ADDRESS]

                    ;Command 1:     DATA --> Memory[ADDRESS]

A02B 3D             CMD1:           DEC  A
A02C 2006                           JR   NZ,CMD2
A02E 3AA002                         LD   A,[DATA]
A031 02                             LD   [BC],A
A032 1836                           JR   DONE

                    ;Command 2:     Memory[ADDRESS] --> DATA

A034 3D             CMD2:           DEC  A
A035 2006                           JR   NZ,CMD3
A037 0A                             LD   A,[BC]
A038 32A002                         LD   [DATA],A
A03B 182D                           JR   DONE

                    ;Command 3:     DATA --> I/O[ADDRESS]

A03D 3D             CMD3:           DEC  A
A03E 2007                           JR   NZ,CMD4
A040 3AA002                         LD   A,[DATA]
A043 ED79                           OUT  [C],A
A045 1823                           JR   DONE

                    ;Command 4:     I/O[ADDRESS] --> DATA

A047 3D             CMD4:           DEC  A
A048 2007                           JR   NZ,CMD5
A04A ED78                           IN   A,[C]
A04C 32A002                         LD   [DATA],A
A04F 1819                           JR   DONE
```

```
                        ;Command 5:  Instruction Test Program

A051 3D         CMD5:           DEC   A
A052 201C                       JR    NZ,CMD6

                        ;Check Accumulator

A054 3E55                       LD    A,55H
A056 CB07                       RLC   A
A058 C64B                       ADD   A,4BH
A05A 2F                         CPL

                        ;Check Stack

A05B F5                         PUSH  AF
A05C AF                         XOR   A
A05D F1                         POP   AF
A05E 08                         EX    AF,AF'

                        ;Check Secondary Accumulator

A05F AF                         XOR   A
A060 08                         EX    AF,AF'
A061 FE0A                       CP    0AH

                        ;Hang if Bad

A063 38FE       BAD_CARRY:      JR    C,BAD_CARRY
A065 20FE       BAD_ACCUM:      JR    NZ,BAD_ACCUM

                        ;Test Primary Registers

A067 CDA0DF                     CALL  REG_TEST

A06A AF         DONE:           XOR   A
A06B 32A005                     LD    [TEST_COMMAND],A
A06E 18B0       CHECK_CMD:      JR    CMD_WAIT

                        ;Command 6:  JUMP to Memory[ADDRESS]

A070 3D         CMD6:           DEC   A
A071 2004                       JR    NZ,CMD7
A073 2AA003                     LD    HL,[ADDRESS]
A076 E9                         JP    [HL]

                        ;Command 7:  Arbiter Test Program

A077 3D         CMD7:           DEC   A
A078 203F                       JR    NZ,CMD8
A07A 11FFFD                     LD    DE,-3
```

```
                        ;Memory address to test

A07D DD21A6FF                   LD    IX,0A6FFH
A081 210300                     LD    HL,00300H
A084 3AA002                     LD    A,[DATA]

                        ;WRITE_LOOP:  Write alternate locations
                        ;             to accumulator

A087 DD7700     WRITE_LOOP:     LD    [IX+0],A
A08A DD2B                       DEC   IX
A08C DD2B                       DEC   IX
A08E DD2B                       DEC   IX
A090 A7                         AND   A
A091 ED5A                       ADC   HL,DE
A093 20F2                       JR    NZ,WRITE_LOOP

                        ;Check alternate locations

A095 DD21A6FF                   LD    IX,0A6FFH
A099 210300                     LD    HL,00300H
A09C DD4600     READ_LOOP:      LD    B,[IX+0]
A09F B8                         CP    B
A0A0 2804                       JR    Z,TEST_OK

                        ;If bad read, 0-->DATA

A0A2 AF                         XOR   A
A0A3 32A002                     LD    [DATA],A
A0A6 DD2B       TEST_OK:        DEC   IX
A0A8 DD4600                     LD    B,[IX+0]
A0AB DD2B                       DEC   IX
A0AD DD4600                     LD    B,[IX+0]
A0B0 DD2B                       DEC   IX
A0B2 A7                         AND   A
A0B3 ED5A                       ADC   HL,DE
A0B5 20E5                       JR    NZ,READ_LOOP

                        ;RETURN without clearing TEST_COMMAND

A0B7 18B5                       JR    CHECK_CMD

                        ;Command 8:  Check for interrupts

A0B9 3D         CMD8:           DEC   A
A0BA 200E                       JR    NZ,CMD9
A0BC 3EA2                       LD    A,0A2H
A0BE ED47                       LD    I,A
A0C0 3E80                       LD    A,128
A0C2 FB                         EI
A0C3 00                         NOP
A0C4 F3                         DI
```

```
A0C5 32A002                     LD    [DATA],A
A0C8 18A0                       JR    DONE

                ;Generate spurious interrupt

A0CA 3D         CMD9:           DEC   A
A0CB 209D                       JR    NZ,DONE
A0CD 32A000                     LD    [INT_COND],A
A0D0 3EFF                       LD    A,0FFH
A0D2 328001                     LD    [INT_DMA],A
A0D5 06FF                       LD    B,255

                ;WAIT_LOOP:     Wait 900 uS

A0D7 10FE       WAIT_LOOP:      DJNZ  WAIT_LOOP
A0D9 AF                         XOR   A
A0DA 328001                     LD    [INT_DMA],A
A0DD 188B                       JR    DONE

                ;REG_TEST:      Load 16-bit registers

A0DF 21B740     REG_TEST:       LD    HL,0B740H
A0E2 1150F3                     LD    DE,050F3
A0E5 01664D                     LD    BC,0664DH

                ;Verify secondary registers

A0E8 D9                         LXX
A0E9 210001                     LD    HL,1
A0EC 110002                     LD    DE,2
A0EF 010003                     LD    BC,3
A0F2 D9                         LXX

                ;Check 16-bit functions

A0F3 EB                         LX    DE,HL
A0F4 09                         ADD   HL,BC
A0F5 ED52                       SBC   HL,DE

                ;Hang if bad

A0F7 20FE       BAD_16B_REG:    JR    NZ,BAD_16B_REG
A0F9 C9                         RET

                ;  Miscellaneous Instructions

A0FA 3D                         DEC   A
A0FB ED4D                       RLTI
```

3. Rotate walking '0' and walking '1' through a memory
4. Run downloaded Z-80 register test.

D. Arbiter Tests
1. Check simultaneous shared memory reads and writes by the mainframe and Z-80 processors.

E. Mainframe to Card Interrupt Test
1. Verify Z-80 interrupt from mainframe write to COMMAND register.

F. Z-80 CTC Tests
1. Cascade timers and verify 1 second timeout. (timers 1&2 in timer mode, timers 2&3 in counter mode).
2. Verify interrupts on timers 1 & 2 in counter mode.
3. Verify interrupts on timers 2 & 3 in timer mode.

G. Z-80 SIO Tests
1. Check all bits/character, stop bits and parity options at 300 baud.
2. Check transmitter all sent indication.
3. Check overrun error detection.
4. Check parity error detection.
5. Check transmit and recieve BREAK.

H. Default Switch Test
1. Production Test: Check that all switches are set to their default values. An optional interactive switch test is also available.
2. Customer/service test: Display settings of all switches.

I. Card to Mainframe Interrupt Test
1. Verify that card interrupt is detected by mainframe.

J. RUN UNIQUE TEST FOR CABLE OR POD.

K. Card Self-Test
1. Run card powerup test and check for errors.
1. Run ROM checksum test.
2. Run shared memory alternating bit pattern test.
3. Run Z-80 CTC timeout tests.
4. Run Z-80 SIO register and interrupt test.
5. Run semaphore test.

6.3.3: ESK Connector and Shared Resource Link Unique Tests

A. Check all standard asynchronous baud rates up to 19.2K baud.

B. Check Modem Control Register (MCR)/Modem Status Register (MSR) Loopback:
   1. MCR=00 0000 --> MSR=XXX0 0000
   2. MCR=00 0001 --> MSR=XXX0 0000
   3. MCR=00 0010 --> MSR=XXX0 0100
   4. MCR=00 0100 --> MSR=XXX0 1000
   5. MCR=00 1000 --> MSR=XXX1 0000
   6. MCR=01 0000 --> MSR=XXX0 0001
   7. MCR=10 0000 --> MSR=XXX0 0010

C. Check external clocking
   1. Tx baud generator internal and Rx baud generator external.
   2. Tx baud generator external - toggle MCR bit 0 to clock.

D. Check auto enables
   1. MCR bit 1 controls Tx autoenables.
   2. MCR bit 5 controls Rx autoenables.

E. Check synchronous modes of operation (baud rate up to 20K baud).

6.3.4: RS-232 DTE Cable Unique Tests

A. Check all standard asynchronous baud rates up to 19.2K baud.
B. Check Modem Control Register (MCR)/Modem Status Register (MSR) Loopback:
   1. MCR=00 0000 --> MSR=XXX0 0000
   2. MCR=00 0001 --> MSR=XXX0 1110
   3. MCR=00 0010 --> MSR=XXX0 0001
   4. MCR=00 0100 --> MSR=XXX0 0000
   5. MCR=00 1000 --> MSR=XXX1 0000
   6. MCR=01 0000 --> MSR=XXX0 0000
   7. MCR=10 0000 --> MSR=XXX0 0000
C. Check external clocking
   1. Tx baud generator internal and Rx baud generator external.
   2. Tx baud generator external - toggle MCR bit 2 to clock.
D. Check auto enables
   1. MCR bit 0 controls Tx autoenables.
   2. MCR bit 0 controls Rx autoenables.

6.3.5: RS-232 DCE Cable Unique Tests

A. Check all standard asynchronous baud rates up to 19.2K baud.
B. Check Modem Control Register (MCR)/Modem Status Register (MSR) Loopback:
   1. MCR=00 0000 --> MSR=XXX0 0000
   2. MCR=00 0001 --> MSR=XXX0 0110
   3. MCR=00 0010 --> MSR=XXX0 1001
   4. MCR=00 0100 --> MSR=XXX0 0000
   5. MCR=00 1000 --> MSR=XXX1 0000
   6. MCR=01 0000 --> MSR=XXX0 0000
   7. MCR=10 0000 --> MSR=XXX0 0000
C. Check clock loopback on cable (Tx baud generator internal/Rx

baud generator external).

D. Check auto enables
   1. MCR bit 0 controls Tx autoenables.
   2. MCR bit 0 controls Rx autoenables.

6.3.6: RS-449 DTE Cable Unique Tests

A. Check all standard asynchronous baud rates up to 19.2K baud.
B. Check Modem Control Register (MCR)/Modem Status Register (MSR) Loopback:
   1. MCR=00 0000 --> MSR=XXX0 0000
   2. MCR=00 0001 --> MSR=XXX0 0000
   3. MCR=00 0010 --> MSR=XXX0 0100
   4. MCR=00 0100 --> MSR=XXX0 1000
   5. MCR=00 1000 --> MSR=XXX0 0000
   6. MCR=01 0000 --> MSR=XXX0 0001
   7. MCR=10 0000 --> MSR=XXX0 0010
C. Check external clocking
   1. Tx baud generator internal and Rx baud generator external.
   2. Tx baud generator external - toggle MCR bit 0 to clock.
D. Check auto enables
   1. MCR bit 1 controls Tx autoenables.
   2. MCR bit 5 controls Rx autoenables.

6.3.7: Data Link and Current Loop Pod Unique Tests

A. Check all standard asynchronous baud rates up to 19.2K baud.
B. Check Modem Control Register (MCR)/Modem Status Register (MSR) Loopback:
   1. MCR=00 0000 --> MSR=XXXX X0XX
   2. MCR=00 0001 --> MSR=XXXX X1XX
   3. MCR=00 0010 --> MSR=XXXX X0XX
   4. MCR=00 0100 --> MSR=XXXX X0XX
   5. MCR=00 1000 --> MSR=XXXX X0XX
   6. MCR=01 0000 --> MSR=XXXX X0XX
   7. MCR=10 0000 --> MSR=XXXX X0XX
C. Check auto enables
   1. MCR bit 0 controls Tx autoenables.

6.3.8: Modem Pod Unique Tests

A. Check all standard asynchronous baud rates up to 300 baud.

6.4: Signature Analysis Tests

The signature analysis tests will be used in conjunction with the comprehensive test program for production troubleshooting. This test could also be used by the field for component level repairs in the future.

This test will consist of two parts. The first part will be driven by a 5001D Microprocessor Exerciser with a custom test EPROM. The second part will be driven by a program in Chipmunk to test the mainframe interface including the shared RAM and registers.

Test Configuration

Required Equipment:
- 5001D Microprocessor Exerciser Unit
- SA EPROM ET14662
- 5004 or 5005 Signature Analyzer
- Mainframe test stimulus board 09826-66541
- 9826 mainframe and extender board
- Balanced test connector

Configuration:
- Remove the Z80 processor (U28) and insert in the 40 socket on the 5001D exerciser.
- Insert the ribbon cable DIP plug from the 5001D into the processor socket on the board, aligning pin 1 on the plug with pin 1 of the socket.
- Insert the test program EPROM into the 24 pin socket on the 5001D.
- Connect the Start, Stop, Clock, and Ground wires from the signature analyzer to the output pins on the edge of the 5001D.
- Apply power to the board. The two displays on the 5001D should light up. If the displays light dimly, the 40 pin plug is reversed.

Testing:
- Select internal or external ROM as required with the slide switch on top of the 5001D.
- Select the test number by pushing the two buttons underneath the two seven-segment displays. Both decimal points will light, until the 'ENTER' button is pressed to start the test.
- The GATE indicator on the signature analyzer should be blinking. If not, something is wrong. Check the connections and the test number.
- Touch the test probe to the desired test point. The light in the probe will flash if it is seeing pulses, light brightly if it is a constant +5, or go out if it is constantly grounded. The notation "ALWAYS LOW" or "ALWAYS HIGH" means the probe light is totally out, or brightly on. When a signature is followed with "BLINKING", it means the probe light must be flashing.

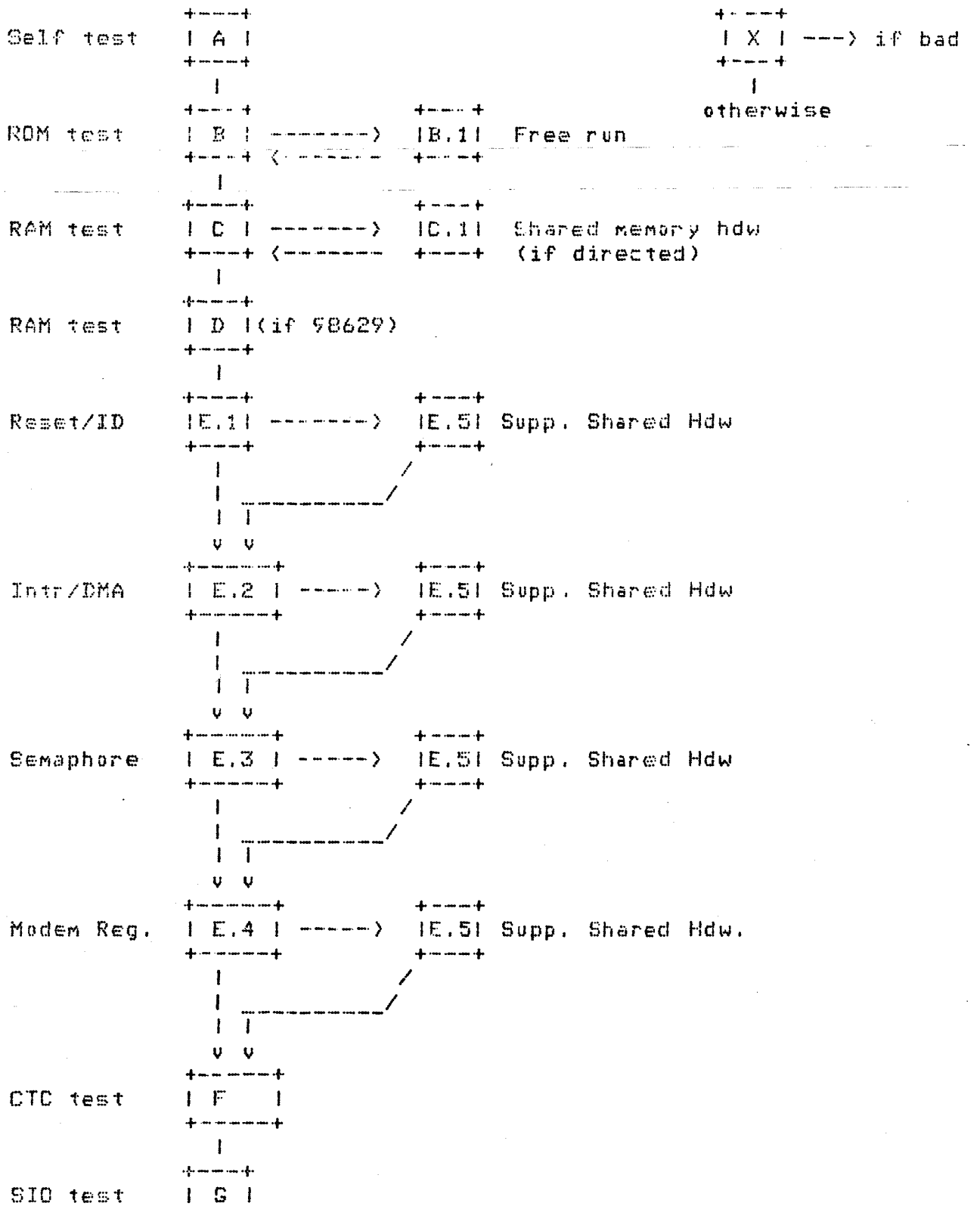
Indenting system:
The signatures listed in this document are prioritized using an indentation system. Highest priority are the lines closest to the left edge. If those higher priority signatures match, the more indented tests underneath need not be performed. If the original test fails, the faulty component can be located by tracing through the more detailed, indented signatures.

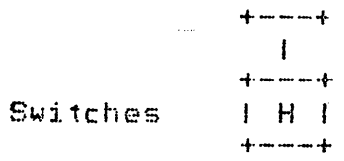
Example:

```
1)  ...U32-2:     8126
2)  ......U4-6    07FF  replace U4
3)  ......U24-2   673P  replace U30
4)  ......U24-1   8126  replace U24
5)  ...U32-4      P1H4
6)  ......U16-6   8126  replace U17
7)  ...U17-5      P1H4
```

Test the signature shown in line 1. If it is good, then go to line 5. If it is bad, then test lines 2,3,and 4, and follow the replacement instructions on the line with the bad signature. If line 5 is good then go to line 7. Otherwise test line 6.

Signature Analysis Test Flow Chart




Switches
H

TEST A: Z-80 Self Test

Test Description:
This test runs an exhaustive test of the instruction set of the Z-80 microprocessor. If successful, the microprocessor is operational. Otherwise, it must be replaced.

Setup:
Reset mainframe
Select 5001D test #0 (internal ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge

Signatures:
NOTE: All signatures are taken on the pins of the Z-80A MPU in the 5001D socket.
If there is no gate, check system clock by following pin 6 procedure.

...Pin 11 (Vcc):	PA55	
.....Pin 6 (Phi):	BLINKING	
.....U18-8:	BLINKING	Replace U18
.....U19-3:	BLINKING	W1 missing or defective
.....U19-1:	always '1'	R13 pullup bad or shorted
.....U19-4:	always '1'	R14-3,7 bad or shorted
.....U19-5:	BLINKING	Replace U19
.....U19-6:	BLINKING	Replace U19
.....U28-6:	BLINKING	Bad clock driver
.....If pin 6 OK, then replace Z-80 CPU.		

Test B: Z-80 ROM Test

Test Description:
This test reads all ROM locations and serializes the data through X0 on the 5001D. The Z-80 data bus, Z-80 address bus and Program ROM (U29) are tested. If this test fails run test #B.1; otherwise continue with test C.

Setup:
Reset mainframe
Select 5001D test #1 (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge

Signatures:
..X0 Output from 5001D: 98628 Opt 100: 1U7U
98629: 33A7 -- EPROM, 61PC -- ROM

Test B.1: Z-80 Free Run

Test Description:
In this test, a NOP instruction is forced onto the Z-80 CPU data bus by the 5001D exerciser. This causes the Z-80 to read its entire 64K-byte address space. This test will check the Z-80 data and address buses. If test B was successful, this test may be skipped.

Setup:
Reset mainframe
Select 5001D test #0 (external ROM)
Clock: Rising edge
Start: Rising edge
Stop: Falling edge

Signatures: (all signatures taken on the PC board)

Address Bus:

...U28-1 (ZA11):	1293	Replace Z-80 CPU
...U28-2 (ZA12):	HAP7	Replace Z-80 CPU
...U28-3 (ZA13):	3C96	Replace Z-80 CPU
...U28-4 (ZA14):	3827	Replace Z-80 CPU
...U28-5 (ZA15):	755P	Replace Z-80 CPU
...U28-30 (ZA0):	UUUU	Replace Z-80 CPU
...U28-31 (ZA1):	5555	Replace Z-80 CPU
...U28-32 (ZA2):	CCCC	Replace Z-80 CPU
...U28-33 (ZA3):	7F7F	Replace Z-80 CPU
...U28-34 (ZA4):	5H21	Replace Z-80 CPU
...U28-35 (ZA5):	0AFA	Replace Z-80 CPU
...U28-36 (ZA6):	UPFH	Replace Z-80 CPU
...U28-37 (ZA7):	52F8	Replace Z-80 CPU
...U28-38 (ZA8):	HC89	Replace Z-80 CPU
...U28-39 (ZA9):	2H70	Replace Z-80 CPU
...U28-40 (ZA10):	HPP0	Replace Z-80 CPU

Control Line:

...U29-20 (ZMREQ):	BLINKING	W2 missing or bad Z-80 CPU

Data Bus:
If the logic probe dos not blink when testing the data lines, the line may be shorted by another device on the bus.

...U29-11 (ZD0) blinking	Replace ROM (U29)
...U29-12 (ZD1) blinking	Replace ROM (U29)
...U29-13 (ZD2) blinking	Replace ROM (U29)
...U29-15 (ZD3) blinking	Replace ROM (U29)
...U29-16 (ZD4) blinking	Replace ROM (U29)
...U29-17 (ZD5) blinking	Replace ROM (U29)
...U29-18 (ZD6) blinking	Replace ROM (U29)
...U29-19 (ZD7) blinking	Replace ROM (U29)

Test C: RAM Test

Test Description:

This test checks the lower block of shared RAM (U25). The test is as follows:

1) Write checkerboard to memory.
2) Read checkboard from memory.
3) Write checkerboard inverted to memory.
4) Read checkerboard inverted from memory.
5) Write the high order of even addresses to itself and the low order to the next (odd) address of memory.
6) Read the addressed from memory.
7) Repeat the test.

This is the first test to access shared memory. If the tests fail, the problem may either be with the U25 RAM or with the shared memory circuitry. If the SA logic probe does not blink when testing the data lines, they may be shorted by another device on the bus.

Setup:

Reset mainframe
Select 5001D test #2 (external ROM)
Clock: Rising Edge
Start: Rising edge
Stop: Falling Edge
+5 Signature: 60U2

Signatures:

The pin numbers on U25 refer to socket pin numbers, not to the RAM chip pin numbers!

	ALVIN	THEO EPROM	THEO ROM	
...U29-11 (ZD0):	Z98C	U1AH	7PU1	
U29-12 (ZD1):	26H1	U3CU	P913	
U29-13 (ZD2):	648H	U22S	536H	
U29-15 (ZD3):	25H8	950C	PAH6	
U29-16 (ZD4):	U98U	670C	H7U4	
U29-17 (ZD5):	66F1	U42A	1842	
U29-18 (ZD6):	692A	CUC9	P920	
U29-19 (ZD7):	PF52	FF89	0U1C	
U28-24 (WAIT'):	60U2 BLINKING			
.....U25-11 (SD0):	0P87			Replace U45
.....U25-12 (SD1):	99C9			Replace U45
.....U25-13 (SD2):	2159			Replace U45
.....U25-15 (SD3):	1959			Replace U45
.....U25-16 (SD4):	4U8P			Replace U45
.....U25-17 (SD5):	PPCH			Replace U45

```
......U25-18 (SD6):  CC20                Replace U45
......U25-19 (SD7):  PF03                Replace U45
......U25-27 (SWR'): 60U2                W4 installed?, run test C.1
......U25-22 (SRD'): 8127                Run test C.1
......U25-20 (CE'):  673P                Run test C.1
......U42-10:  ALWAYS LOW                Run Test C.1
......U42-11         AA9C                Run Test C.1
......U25-3 (SA7):  UA14                 Replace U41
......U25-4 (SA6):  A825                 Replace U40
......U25-5 (SA5):  P75H                 Replace U40
......U25-6 (SA4):  2U75                 Replace U40
......U25-7 (SA3):  FA66                 Replace U40
......U25-8 (SA2):  5U83                 Replace U39
......U25-9 (SA1):  4896                 Replace U39
......U25-10 (SA0): A46A                 Replace U39
......U25-21 (SA10):66A4                 Replace U41
......U25-24 (SA9): H1U9                 Replace U41
......U25-25 (SA8): 0HC5                 Replace U41
......U28-4 (ZA14):  0000 BLINKING       Replace Z-80 CPU
......U28-3 (ZA13):  07FF BLINKING       Replace Z-80 CPU
......U31-13 (SA14): 0000 BLINKING       Replace U42
......U31-14 (SA13): 07FF BLINKING       Replace U42
......If one of the primary signatures was bad and all secondary
      signatures are good, then replace U25.
```

Test C.1: Shared Memory Test

Test Description:
This test will check the shared memory controller logic.

Setup:
Reset mainframe
Select 5001D test #2 (external ROM)
Clock: Falling Edge
Start: Rising edge
Stop: Falling Edge
+5 Signature: 60U2

Signatures:

...U32-2: 8126	
......U4-4 (RFSH'): 60U2 BLINKING	Replace Z-80 CPU
......U4-5 (ZA15): 07FF	Replace Z-80 CPU
......U4-6: 07FF	Replace U4
......U24-2: 673P	Replace U30
......U24-1: 8126	Replace U24
...U32-3: ALWAYS LOW	
......U24-9: ALWAYS HIGH	Mainframe on test 0?, replace U4
......U24-10: ALWAYS LOW	Replace U24
......U4-11: 0000 BLINKING	Replace U4
...U32-4: P1H4	
......U16-4: 8126	Replace U17.
......U16-6: 60U2 BLINKING	Replace U16
......U24-13: BLINKING	Replace U24
......U19-9: ALWAYS LOW	Replace U19
......U32-4: P1H4	Replace U32
...U17-5: P1H4	Replace U17
...U17-6: 8126	Replace U17
...U17-8: 60U2 BLINKING	Replace U17
...U32-7: FHA5	
......U23-15 (ZRD'): FHA5	Replace Z-80 CPU
......U23-13: AH57	Replace U23
......U32-7: FHA5	Replace U32
...U32-9: P1H4	Replace U32
...U32-12: ALWAYS HIGH	Replace U32
...U36-6 (SWR'): P1H4	Replace U36
...U16-3: 8126	Replace U16
...U4-3 (WAIT'): 60U2 BLINKING	
......U12-13: ALWAYS HIGH	Replace U27
......U12-11: ALWAYS HIGH	Replace U12
......U16-8: P1H4	Replace U16
......U16-12: ALWAYS LOW	Replace U30
......U16-13: ALWAYS HIGH	R14-6 or U27 bad
......U16-11: ALWAYS HIGH	Replace U16
......U4-2: 60U2 BLINKING	Replace U36
......U4-3: 60U2 BLINKING	Replace U4

Test D: U26 RAM Test (98629 only)

Test Description:
This test checks the U26 RAM (used on the 98629 but not the 98628). It is identical to test C except for the address space tested.

Setup:
Reset mainframe
Select 5001D test #3 (external ROM)
Clock: Rising edge
Start: Rising edge
Stop: Falling edge

...U29-11 (ZD0):	298C	
U29-12 (ZD1):	26H1	
U29-13 (ZD2):	648H	
U29-15 (ZD3):	25H8	
U29-16 (ZD4):	U98U	
U29-17 (ZD5):	H062	
U29-18 (ZD6):	HU89	
U29-19 (ZD7):	PF52	

If all of these signatures were good, continue with Test F.
Otherwise, check the following points.

...U28-4 (ZA14):	07FF	Replace Z-80 CPU
.....U31-13 (SA14):	07FF	Replace U42
...U28-3 (ZA13):	0000 BLINKING	Replace Z-80 CPU
.....U31-14 (SA13):	0000 BLINKING	Replace U42
.....U26-20 (CE'):	673P	Replace U31
.....U26-22 (SRD'):	8127	SRD bad
.....U26-23 (SWR'):	60U2 BLINKING	SWR bad

If these signatures are OK then the U26 RAM is bad.

Test E.1: RESET/ID Register Test
Test Description: This test writes a walking '1' to the RESET/ID register; it then reads the register.

Setup:
Reset mainframe
Select 5001D test #10 (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge
+5 Signature: 275C

Signatures:

...U15-10 (R14-4): ALWAYS HIGH	R14 pullup bad
...U15-8 (RST): CF50	Replace U15
...U15-9 (RST'):9C0C	Replace U15
...U5-9 (SD0): 0A47	R14 pullup bad
...U5-7 (SD1): 1040	R14 pullup bad
...U5-5 (SD2): 01HC	Replace U35
...U5-3 (SD3): 0815	R14 pullup bad
...U33-4 (SD4): 1U11	Replace U33
...U33-7 (SD5): 2471	Replace U33
...U33-9 (SD6): 4F15	Replace U33
...U33-12(SD7): HC9H	Replace U33

Test E.2: Interrupt/DMA Register Test
Test Description:
This test is the same as test E.1 except that only the interrupt/DMA registers are accessed.

Setup:
Reset mainframe
Select 5001D test #11 (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge
+5 Signature: PFHF

Signatures:

...U33-10 (Int Req FF): UC17	Replace U23
...U33-13 (Int En FF): PAUU	Replace U14
...U5-9 (SD0): AU14	R14 pullup bad
...U5-7 (SD1): 0UF4	R14 pullup bad
...U5-5 (SD2): 507P	R14 pullup bad
...U5-3 (SD3): P58C	R14 pullup bad
...U33-4 (SD4): A64P (P121 for 98629)	Replace U33
...U33-7 (SD5): 6C78	Replace U33
...U33-9 (SD6): C67C	Replace U33
...U33-12(SD7): 81PC	Replace U33

Test E.3: Semaphore Test
Test Description:
This test is the same as test E.1 except that only the semaphore is tested.

Setup:
Reset mainframe
Select 5001D test #12 (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge

+5 Signature: FHF0

Signatures:
...U35-5 (Sem FF): AF02 Replace U14
...U35-6 (SD7): U941 Replace U35

Test E.4: Modem Register Test
Test Description:
This test is the same as test E.1 except that only the modem register is accessed.

Setup:
Reset mainframe
Select 5001D test #13
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge

+5 Signature: 766P

Voltage Checks:
U7-5: -11.3 volts +/- 10% Check CR1 or F1
U7-8: +12 volts +/- 10%
Signatures:
...U5-9 (SD0): 85CU
...U5-7 (SD1): 0109
...U5-5 (SD2): 0774
...U5-3 (SD3): 1671
...U5-13 (SD4): 18A5
...U5-11 (SD5): 0524

.....U6-2 (MCR3): 6A87 Replace U6
.....U6-5 (MCR7): 4777 Replace U6
.....U6-6 (MCR0): A7F2 Replace U6
.....U6-9 (MCR4): 7328 Replace U6
.....U6-12 (MCR5):F339 Replace U6
.....U6-15 (MCR1):5574 Replace U6
.....U6-16 (MCR6):8312 Replace U6
.....U6-19 (MCR2):9A2C Replace U6
.....U7-6 (OCD3): 4UUA Replace U7

```
.....U7-7 (OCD4): 17U2                        Replace U7
.....U2-6 (OCD2): F32H                        Replace U6
.....U2-7 (OCD1): CC7C                        Replace U6
.....U1-6 (RS):   258U                        Replace U1
.....U1-7 (TR):   HFH4                        Replace U1
.....U9-9 (CS):   231A (none for 98629)       Bad Test Connector
.....U9-10 (CS):  5574 (none for 98629)       Bad Test Connector

.....U9-11:       5574                        Replace U9
NOTE: Take the next two signatures (without the test connector
        on a 98629) only if the preceding one is bad.  If these next
        two signatures are then good, then the test connector is bad.
.......U8-13 (TR): 231A                       Replace U8
.......U8-14 (TR): 5574                       Replace U8

.....U9-13 (ST):  A7F2
NOTE: Take the next two signatures (without the test connector
        on a 98629) only if the preceding one is bad.  If these next
        two signatures are then good, then the test connector is bad.
.......U8-5 (RS):  H1AF                       Replace U8
.......U8-6 (RS):  A7F2                       Replace U8

.....U10-1 (DM):  4LUA                        Bad Test Connector
.....U10-2 (DM):  ALWAYS LOW                  Bad Test Connector
.....U10-3:       3994                        Replace U10
.....U10-6 (RR):  ALWAYS LOW                  Bad Test Connector
.....U10-7 (RR):  17U2                        Bad Test Connector
.....U10-5:       619F                        Replace U10
.....U10-9 (OCR1):CC7C                        Bad Test Connector
.....U10-10(OCR1) ALWAYS LOW                  Bad Test Connector
.....U10-11:      FH15                        Replace U10
.....U10-14(OCR2) ALWAYS LOW                  Bad Test Connector
.....U10-15(OCR2) F32H                        Bad Test Connector
.....U10-13:      C543                        Replace U10
```

Test E.5: Supplemental Shared Hardware Test

Test Description:
This test writes a walking '1' to all shared hardware control registers; then it reads the shared hardware status registers.

This test is only run if there is a problem with tests E.1-E.4.

Setup:
Reset mainframe
Select 5001D test #4 (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge
+5 Signature: 5HHC
Test connector must be installed
Interrupt level and remote control switches must be set to default values.

Signatures:

.....U30-9 (Int Level):	0000 (5HHC for 98629)	Correct switch position
.....U30-3 (Int Level):	0000	Correct switch position
.....U33-14 (Rem Control):	HIGH	Correct switch position
.....U30-4:	ALWAYS HIGH	Replace U30
.....U30-8:	ALWAYS HIGH (0000 for 98629)	Replace U30
.....U28-3 (ZA13):	875H	Replace Z-80 CPU
.....U28-4 (ZA14):	0000 BLINKING	Replace Z-80 CPU
.....U42-12 (SA14):	0000 BLINKING	Replace U42
.....U42-13 (SA13):	875H	Replace U42
.....U42-14 (SA12):	0000 BLINKING	Replace U42
.....U31-12:	99AC	Replace U31
.....U36-9:	432F	Replace U38
.....U36-10:	432F	Replace U38
.....U36-11:	9CFC	Replace U30
.....U36-8:	1PU7	Replace U36
.....U37-3:	933A	Replace U37
.....U37-6:	99AC	Replace U37
.....U37-11:	HA86	Replace U37
.....U22-1:	30U1	Replace U30
.....U23-5:	ALWAYS HIGH	Replace U22
.....U23-6:	ALWAYS HIGH	Replace U22
.....U23-10:	ALWAYS HIGH	Replace U22
.....U23-11:	U1PP	Replace U22
.....U23-12:	ALWAYS HIGH	Replace U22
.....U23-9:	5P8F	Replace U23
.....U21-4	7F0F	Replace U21
.....U21-5:	A8PU	Replace U21
.....U21-6:	CCUA	Replace U21
.....U21-7:	411U	Replace U21
.....U21-9:	5HHC	Replace U21

.....U21-10:	5HHC	Replace U21
.....U21-11:	5HHC	Replace U21
.....U21-12:	5HHC	Replace U21
.....U4-8:	A73P	Replace U4
U34-9 (IR6'):	0000	Replace U34
U34-10 (IR5'):	0000	Replace U34
U34-11 (IR4'):	0000	Replace U34
U34-12 (IR3'):	0000	Replace U34

Test F: CTC (U12) Test

Test Description:
This test sets up each of the CTC channels for a timeout; waits for timeout; then, repeats the test.

Setup:
Reset mainframe
Select 5001D test #5. (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge
+5 Signature: 3AH0

Signatures:

...TP3:	23H2	
TP4:	5548	
U12-9 (ZC/TO2):	P407	
U12-12 (ZINT'):	19P0	
.....U12-10 (ZIORQ'):	AU84	Replace Z-80 CPU
.....U12-13 (IEI):	ALWAYS HIGH	Replace U27
.....U12-14 (ZM1'):	5P78	Replace Z-80 CPU
.....U12-22:	BLINKING	Replace U15
.....U12-23:	BLINKING	Replace U15
.....U13-3:	677C	Replace U12
.....U13-6:	23H2	Replace U13
.....U13-11:	5F1F	Replace U12
.....U13-8:	5548	Replace U13
.....U11-2:	0000 BLINKING	Replace U6
.....U11-14:	0000 BLINKING	Replace U6
.....U11-7:	23H2	Replace U11
.....U11-9:	5548	Replace U11
.....U12-12 (ZINT'):	19P0	R14-15 or U12 bad

.....Replace U12

Test 9: SIO (U28) Test

Test Description:

This test sets up the Z-80 SIO and Z-80 CTC to transmit and receive a character. Most parts of th system have been checked by now including the modem latches line drivers, line receivers, and Z-80 CTC. This test will basically check the Z-80 SIO and its interface to these other parts.

Setup:

Reset mainframe
Select 5061D test #6 (external ROM)
Clock: Rising Edge
Start: Rising Edge
Stop: Falling Edge
+5 Signature: HUHC

	Alvin	Theo (EPROM)	Theo (ROM)
Signatures:			
...U27-15 (TxDA):	6425	HU36	HU36
U27-12 (RxDA):	6425	HU36	HU36
U27-5 (ZINT'):	06A8	06A8	06A8
U28-24 (WAIT'):	HUHC	HUHC	HUHC
U29-11 (ZD0):	A2FU	C65A	8297
U29-12 (ZD1):	CCHA	9PAA	H95C
U29-13 (ZD2):	0489	732P	C8C9
U29-15 (ZD3):	C9PP	83A6	96F6
U29-16 (ZD4):	7209	7594	9272
U29-17 (ZD5):	7P6P	U936	8H36
U29-18 (ZD6):	6P9P	0998	1792
U29-19 (ZD7):	P38C	774P	4153

	Alvin	Theo	
.....U8-9:	U624	AF5U	Replace U12
.....U8-10 (TTB):	U624	U9CU	Replace U8
.....U8-11 (TTA):	29UU	7384	Replace U8
.....U9-7 (RTA):	29UU	7384	Bad test connector
.....U9-6 (RTB):	0000	U9CU	Bad test connector
.....U9-5:	C25C	AF5U	Replace U9

Alvin & Theo:

.....U8-7:	ALWAYS HIGH	Replace U6
.....U8-6 (RSB):	ALWAYS HIGH	Replace U8
.....U8-5 (RSA):	0000 BLINKING	Replace U8
.....U9-15 (STA):	0000 BLINKING	Bad test connector
.....U9-14 (STB):	0000 HUHC	Bad test connector
.....U9-13:	ALWAYS HIGH	Replace U9

	Alvin	Theo	
.....U27-13:	UHUC	none	Replace U11
.....U27-14:	U624	AF5U	Replace U11
.....U8-1:	6425	HU36	Replace U27
.....U8-2 (SDB):	6425	HU36	Replace U8
.....U8-3 (SDA):	CCUP	00PH	Replace U8
.....U3-7 (SDU):	CCUP	00PH	Replace U3
.....U9-1 (RDA):	CCUP	00PH	Bad test connector
.....U9-2 (RDB):	0000	HU36	Bad test connector
.....U9-3:	6425	HU36	Replace U9
.....U28-24 (Z-80 WAIT'):	HUHC		R14-6 or U27 bad
.....Replace U27			

Test H: Default Switch Test

Test Description:

This test checks the default switches and buffers. These switches only used for powerup default conditions and have no other effect o the card operation. If their function is of nc concern, this test be skipped. Two signatures are shown for each switch - one for the 'OFF' postion, the other for 'ON'. For a complete test, toggle each switch when testing.

Setup:

Reset mainframe
Select 5001D test #7 (external ROM)
Clock: Rising edge
Start: Rising edge
Stop: Falling edge

+5 Signature: 07U3

Signatures:

Switch position:	'ON'		'OFF'		
	Alvin	Theo	Alvin	Theo	
...U20-4:	07U2	07P8	06U0	06PA	
.....U20-3:	HIGH		LOW		Sig. bad: replace U20 Sig good: R17-2 or SW1 bad
...U20-7:	0320	0169	0222	006C	
.....U20-6:	HIGH		LOW		Sig. bad: replace U20 Sig. good: R17-9 or SW1 bad
...U20-9:	0581	07F4	0483	06F6	
.....U20-10:	HIGH		LOW		Sig. bad: replace U20 Sig. good: R17-1 or SW1 bad
...U20-12:	0583	0765	0481	0667	
.....U20-13:	HIGH		LOW		Sig. bad: replace U20 Sig. good: R17-8 or SW1 bad

Change to 5001D test #8 (external ROM).

...U20-4:	07U2	07P8	06U0	06PA	
.....U20-2:	HIGH		LOW		Sig. bad: replace U20 Sig good: R17-13 or SW1 bad
...U20-7:	0320	0169	0222	006C	
.....U20-5:	HIGH		LOW		Sig. bad: replace U20 Sig. good: R17-12 or SW1 bad
...U20-9:	0581	07F4	0483	06F6	
.....U20-11:	HIGH		LOW		Sig. bad: replace U20 Sig. good: R17-11 or SW1 bad
...U20-12:	0583	0765	0481	0667	
.....U20-14:	HIGH		LOW		Sig. bad: replace U20

TUE, JUL 27, 1982, 4:56 PM

Parts not tested

Set and clear of command FF.
Arbiter collisions (simultaneous accesses by Z-80 and M/F).

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