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Agilent ParBERT 81250

Agilent E4866A ParBERT 10.8 Gb/s Generator Module
Agilent N4868A ParBERT Booster Module
Agilent E4867A ParBERT 10.8 Gb/s Analyzer Module

Technical Specifications

Technical Specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10° to 40° ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminate with 50 Ohms to ground at ECL levels if not specified otherwise.

E4866A/E4867A

There is one E4866A module for Generator 10.8 Gbit/s and one E4867A module for the Analyzer 10.8 Gbit/s. N4868A is a Booster Module for the E4866A Generator.

Clock Timing

The generator provides complementary data and single-ended clock output. Both clock out and data out can be moved with the variable delay, but it is the same delay for both. The analyzer also has a variable sampling delay. This consists of two parts:
1) the start delay with a large range
2) the time delay of the ±1 period without stopping.

Data capabilities

PRBS/PRWS and memory-based data are defined by segments. Segments are assigned to a generator for a stimulating pattern. On an Analyzer it defines the expected pattern where the incoming data are compared to. The expected pattern can be setup with mask bits. The segment length resolution is the resolution to which the length of a pattern segment can be set. The segment length resolution is 256 bits for a total of 32 Meg memory.

AC coupling behind sampling circuit

The AC coupling does not impact the performance of the analyzer as long as the input data is balanced or the following limitations are not exceeded:

1. For infinite time period a mark density from 9/10 to 10/9 is tolerated.
2. All zero or all one patterns must not be longer than 20000 bits or 2 us.
3. When data recovers from imbalanced pattern to a balanced pattern a settling time of maximum 200us takes effect.

Table 1: E4866A Timing Specifications (@ 50 % of amplitude, 50 Ohm to GND)	
Data range	9.5 Gbit/s to 10.8 Gbit/s
Clock range	9.5 GHz to 10.8 GHz
Delay Range	0 to 300 ns
Delay Resolution	1 ps
Accuracy	±20 ps ± 50 ppm relative to the zero-delay placement.
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency

Table 2: E4866A Pattern and Sequencing	
Segment length resolution	256bits
Patterns:	
Memory-based	up to 33,554,432bits
PRBS/PRWS	2n-1, n= 7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n=7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n-1, n= 7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n= 7, 9, 10, 11, 15
Clock patterns	Divide or multiply by 1, 2, 4,

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Table 3: Parameters for Clock output E4866A 10.8GHz	
Output	1, single ended, AC coupled, to be used into 50 Ohm
Duty cycle	50% typical;
Maximum external voltage	-2.2V to +3.3 V
Amplitude/Resolution	0.5Vpp fixed typ.
Transition times (20%-80%)	sine wave
Clock Jitter	< 2ps RMS

Table 4: Parameters for Data output E4866A 10.8 Gbit/s with N4868A Booster *		
Outputs	1, differential, 50 Ohm typ.	1, differential or 2, single-ended
Data formats	NRZ	NRZ
Amplitude / Resolution	0.3V to 1.8 V / 10 mV	1.0V to 2.5V
Accuracy HiLevel /Amplitude	±2% ±10mV	±5% ±50mV
External termination voltage	-2V to +1.5V	AC Coupled
Output voltage window	-2.0 to +2.7 V	
Maximum external voltage	-2.2V to +3.3 V	
Enable / Disable	Relay	-
Transition times (20%-80%)	< 60ps	<20ps (15ps typ.)
Overshoot/ringing	10% +20mV typ.	-
Jitter	< 25ps peak-to-peak	<25ps peak-to-peak (20ps typ.)

*** Booster input to be driven with 1.8V amplitude from E4866A Generator**

E4867A Analyzer Module

Table 5: E4867A Timing Specifications (@ 50% of amplitude, 50 Ohm to GND)	
Data range	9.5 Gbit/s to 10.8 Gbit/s
Delay (between channels)	Can be specified as leading edge delay (start delay) in fraction of bits in each channel, fine delay can be changed with-out stopping the instrument
Start Delay Range	0 to 300 ns (not limited by period)
Fine Delay Range	±1Period (w/out stopping)
Resolution	1 ps
Accuracy	±20 ps ±50 ppm relative to the zero-delay placement.
Skew between modules of same type	50 ps typ. after deskewing at customer levels and unchanged system frequency

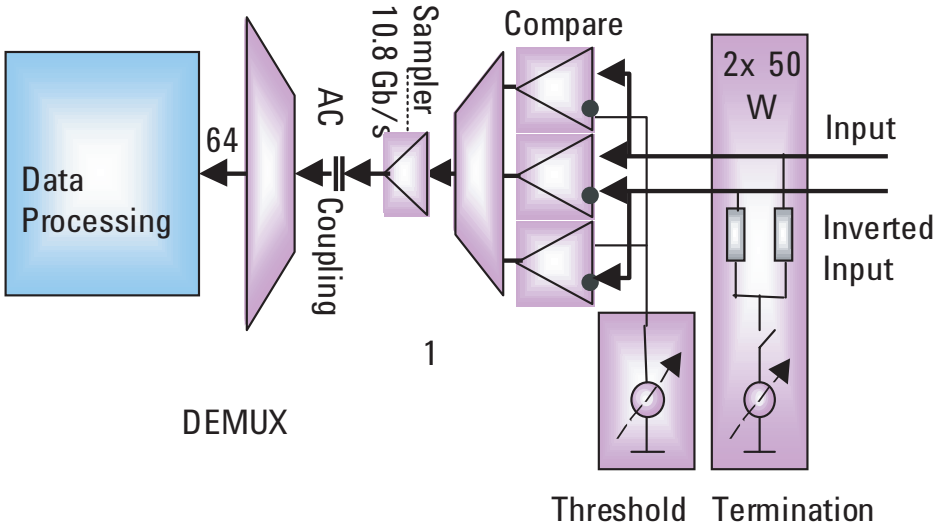


Figure 1: Internal AC Coupling of E4867A Analyzer

In general every time a sequence is started this AC coupled behavior has to be taken into account. There are two different methods of dealing with it, without getting invalid results.

1. Whenever possible use the synchronization feature (Bit Sync. or Auto Delay Alignment) followed by a balanced pattern according to the specification above. In this case no recovery time is needed after starting a sequence.
2. If for some resason synchronization is impossible, use a preamble instead. The length of such a data segment will correspond to the specified settling time. The pattern of the preamble as well as the following data segment must not exceed the maximum tolerated imbalance (9/10 to 10/9).

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Table 6: E4867A Pattern and Sequencing	
Segment length resolution	256bits
Patterns:	
Memory based	up to 33,554,432
PRBS/PRWS	2^n-1, n= 7, 9, 10, 11, 15, 23, 31
Marker Density	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n= 7, 9, 10, 11, 15
Errored PRBS/PRWS	2^n-1, n= 7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n= 7, 9, 10, 11, 15
User	Data editor, file import
Analyzer expected Data	
Mark Density	9/10...10/9
Max consecutive 0 or 1	20000 or 2 us
Data recovery from imbalanced	200 us
Analyzer Auto-synchronization	on PRBS or Memory-based Data manual or automatic by: Bit synchronization* with or without automatic phase alignment. Automatic delay alignment around a start sample delay BER Threshold: 10^{-4} to 10^{-9}

***Bit synchronization on data is achieved by detecting a 48Bit unique word at the beginning of the segment. (Don't cares can be programmed within the detect word). In this mode memory-based data cannot be sent within the same system. If several inputs synchronize, the delay difference between the terminals must be smaller ±5 segment length resolution.**

Synchronization

Synchronization is the method of automatically adjusting the proper bit phase for data comparison on the incoming bit stream. The synchronization can be performed on PRBS/PRWS and memory-based data (it is not possible with a mix of PRxS and memory-based data).
There are two types of sychronization:
- Bit synchronization
- Auto delay alignment

Bit synchronization is able to cover a bit aligment for a totally unknown number of cycles. Using memory-based data, the first 48 Bit within the expected data segment will work as DETECT word where the incoming data are compared to. When the incoming data match with this Detect Word, the further analysis is started.

Auto Delay aligment will be performed using the analyzer sampling delay. So there is a limited range while this is possible of 10 ns. Using Auto delay alignment will provide synchronization with an absolute timing relation between a group of analyzer channels. Therefore skew measurements will be possible.

Input/Output

Addressable technologies:

CML, SSTL-2, ECL (terminated to 0 V/-2 V), LVPECL, (terminated to 1.3V)

Generator Out

The Generator output can be used as single-ended or differential. Enable/Disable relay provide on/off switching. Switched off will provide internal termination. It is recommended either to turn off or externally terminate unused outputs.

The generator outputs can work into 50 Ohm center tapped termination or 100 Ohm differential termination. The proper termination scheme can be chosen from the editor to adapt proper level programming.

Analyzer Input

The analyzer input provides more than 90% eye opening with an “ideal” input signal (10ps transition time). This is a superior performance for characterization tasks.

The analyzer channels can be operated:
- Single-ended normal
- Single-ended compliment
- Differential

For termination there is always 50 Ohm connected to a programmable termination voltage. In differential mode there is an additional, selectable 100 Ohm differential termination. Independently of the selected termination, one can select whether the analysis of the incoming signal is performed on the input, the complimentary input or true differentially.

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Booster N4868A

The N4868A delivers either 1 differential channel or 2 single-ended channels. The N4868A 001 delivers either 2 differential or 4 single-ended channels. For differential operation it is recommended that the N4869A cable kit be used with phase adjustment capability for the differential path. For the N4868A -001 two cable kits would be needed if both are used as differential. The N4868A -001 can also be used 1x differential and 2x single-ended to boost the clock output of the E4866A beside the differential data.

Table 7: Parameters for Analyzer Module E4867A 10.8 Gbit/s		
Inputs	1, differential or single-ended	
Impedance	50 Ohm typ. 100 Ohm differential if termination voltage is switched off	
Input sensitivity	100 mV typ.,single-ended and differential	
Internal termination voltage	-2.0 to +2.0 V, can be switched off	
Threshold voltage range	-2.0 to + 2.0 V	
Threshold resolution	1 mV	
Threshold accuracy	± 2% ±20 mV	
Maximum input voltage range three ranges selectable:	-2V to + 0V, -1V to +1V, 0V to 2V	
Maximum differential voltage	1.2V	
Enable/Disable	Relay	
Bandwidth, equivalent transition time (20%-80%)	35ps typ.	
Minimum detectable Pulse Width	Data:	80 ps typ.
	Continuous clock:	40 ps typ.
Phase Margin with ideal input signal with E4866A Generator.	>1 UI -15ps > 1 UI -33ps	

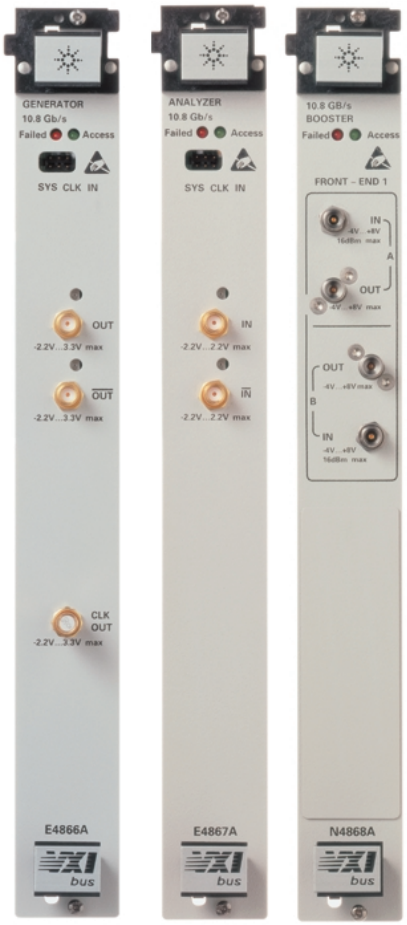


Figure 2: E4866A/E4867A/N4868A Modules

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Related Literature	Publication Number
• *Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Product Overview*	*5968-9188E*
• *10GbE Technology and Device Charaterization, Product Note*	*5988-6960EN*
• *LVDS Technology and Device Characterization*	*5988-7214EN*

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