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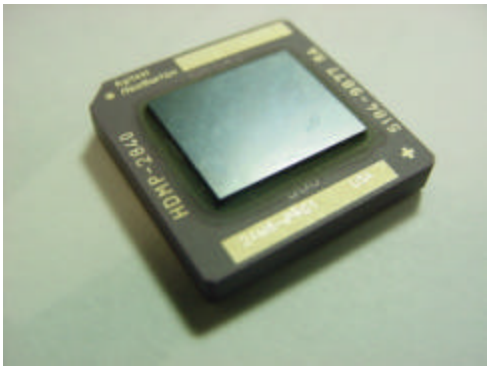
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8-Port, 4x InfiniBand™ Switch (HDMP-2840)



Product Brief

Applications

- **System Area Networks (SAN)**
- **Servers and Workstations**
- **Clustering**
- **IO Adapters**
- **Data Networks**
- **High Speed Backplanes**

Features:

Hardware

- 8 Independent InfiniBand data ports supporting the 4x or 1x InfiniBand links
- Aggregate switch bandwidth of 160 Gbps and aggregate switch data rate of 128 Gbps
- Each 4x port supports bit rates up to 10Gbps in each direction allowing a 16 Gbps full duplex data rate per port
- Integrated SerDes for reduced system cost, power consumption, and latency
- Unloaded fall-through switch latency of about 110 ns including integrated SerDes
- Fully non-blocking internal switch architecture and support for Cut-Through, and Store and Forward Switching Algorithms
- VL Arbitration: 32 high priority and 32 low priority
- Support for both Unicast and Multicast packets
- Unicast Forwarding table size of 16k entries
- Multicast Forwarding table of 512 entries
- Error handling and packet checking for all data, link and management packets in Hardware including ICRC check and generation
- Internal SRAM for Packet Buffering and Queuing
- Support 8 Programmable Virtual lanes (VLs)
- Programmable partition key checking: check inbound packets only, outbound packets only, both inbound and outbound packets, or disable checks
- Support for 16 Partition Keys per port
- Integrated CPU interface to support optional external processor for advance management functions
- I2C support for system configuration via external NVRAM, system bringup and system diagnostics
- IEEE 1149.1 TAP compliance
- Implemented in 0.18 micron 1.8V, 6 metal layer CMOS process technology
- 400-pin, 22 mm Ceramic BGA Flip Chip package

Software

- Feature-rich management capabilities including SMA, PMA, BMA
- Support extended management functionality such as SNMP Tunneling and subnet management, via the CPU interface to an optional external processor
- SMA support for SMP traffic and pass-thru SMP traffic as well as trap and notice management
- Support for all required InfiniBand performance and diagnostic counters
- Support Vendor-specific configuration and programming

InfiniBand

- Compliant with InfiniBand architecture specification 1.0 requirements
- Exceeds or conforms to IBTA profiles A and B

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Description

The HDMP-2840 is a highly integrated, cost effective 8 – port 4 – channel switching solution.

Each port can run at 4x or 1x operating mode, which is defined as four pairs of full-duplex differential signals, or one pair of full-duplex differential signals, respectively.

The HDMP-2840 combines SerDes (SERializer-DESerializer) technology with additional logic to support a 2.0 Gbps InfiniBand data rate (2.5 GHz signaling).

Each port contains an independent Physical layer (Phy) and link. The SerDes Phy block includes the analog transceiver
Through “8B/10B” coding/decoding logic and elastic buffers for rate matching and lane de-skew. The Phy transmitter block accepts 10-bit wide parallel data and serializes this data into a high-speed serial data stream. The high-speed outputs are capable of interfacing directly to connectors and copper cables for electrical transmission or to fiber optic modules for optical transmission.

The Phy/Link block completes the required Phy functionality and provides an interface to the Data Link layer. The block contains the sync and idle character insertion, Phy training controller, and character recognition logic.

The InfiniBand™ specified Link block supports 8 programmable Virtual Lanes (VLs) and other functions such as Link state and status, error detecting and recording, flow control generation, and output buffering.

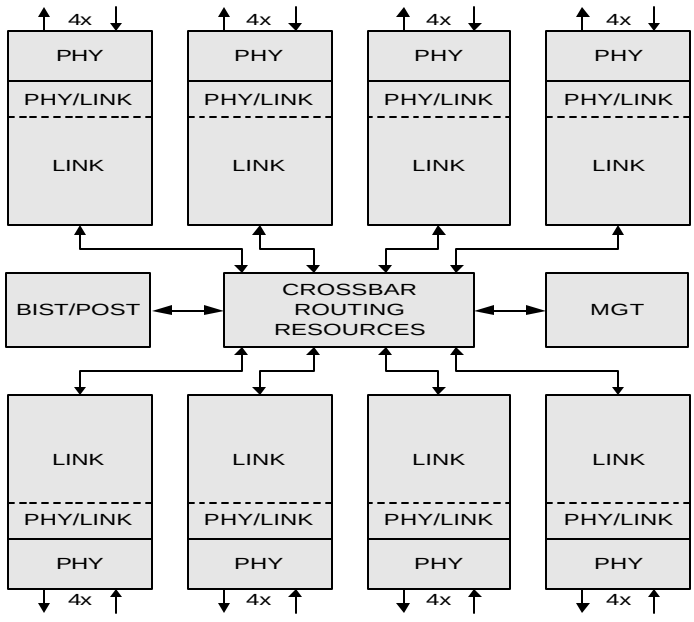


Figure 1: HDMP-2840 Functional Block Diagram

The input Virtual Lanes (VLs) within the Link are configurable to a programmable number of VLs and Maximum Transfer Units (MTUs) to support either one or two VLs at a MTU of 4096 B, or four VLs at a MTU of 2048 B, or eight VLs at a MTU of 1024 B.

The HDMP-2840 Crossbar is designed with input buffers that can be drained faster than they can be filled. Each of the HDMP-2840’s eight ports is treated in identical fashion in the crossbar.
The Crossbar includes two additional internal ports for IB Management and internal BIST/POST.

The MGT block includes agents for various programming, quality of service, performance monitoring, and error detecting services. These agents include PMA, the Performance Management Agent, SMA, the Subnet Management Agent, and BMA, the Baseboard Management Agent.

The HDMP-2840 can be configured to use an external processor for management-related functions that may be implemented in firmware. The CPU interface sends and receives both general services management and subnet management traffic in addition to other capabilities such as on chip initialization and diagnostics.

The HDMP-2840 requires an external differential clock generator at 62.5 MHz as a reference clock. All internal clocks, including the transmit Phy clocks, are synthesized from this reference clock per the InfiniBand™ specification.

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