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HEWLETT PACKARD

ANALOG-TO-DIGITAL CONVERTER CARD MODEL 69751A

OPERATING MANUAL

FOR SERIAL NUMBERS 2029A-0461 AND ABOVE*

*For cards with serial numbers above 2029A-0461, a manual change page may be included.

*For cards with serial numbers below 2029A-0461, refer to Appendix A.

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Section I
GENERAL INFORMATION

1-1 SCOPE OF MANUAL

1-2 This manual covers the installation, pre-operation, and theory of operation for the Analog-to-Digital Converter Card, Model 69751A. This manual does not include servicing instructions or information on the programming of the card. Programming examples for the Analog-to-Digital Converter card are given in Chapter 7 of the 6942A Multiprogrammer User's Guide. Additional documents that contain general information on I/O cards are:

- 6942A Multiprogrammer User's Guide for HP 9825/35/45 Controllers (HP 06942-90003).
- 6942A Multiprogrammer User's Guide for HP 85 Controllers (HP 06942-90011).
- 6942A Multiprogrammer User's Guide for HP 9826 Controllers (HP 06942-90013).
- 6942A Multiprogrammer Technical Data (HP 5952-4078).
- 6942A Multiprogrammer Installation and Assembly Level Service Manual (HP 6942A-90006).

1-3 Any of these documents can be ordered directly from your local Hewlett-Packard sales office. Give the applicable HP manual part number as indicated above.

1-4 DESCRIPTION

1-5 The Analog-To-Digital Converter card can measure bipolar dc voltages in one of the following ranges: ± 100 mV, ± 1 V, ± 10 V, or ± 100 V. A voltage measurement can be initiated by a programmed instruction or by an external trigger signal. Three manual range switches on the card select either the ± 100 mV, ± 1 V, or ± 10 V range. Input voltages in the ± 100 V range are connected to the card's divide-by-ten attenuator. Sixteen optional dc input ranges (8 bipolar and 8 unipolar) are also available. Instructions for modifying and recalibrating the A/D card for the optional dc input ranges are provided in Section V of this manual.

1-6 As shipped from the factory, the A/D card is set to to measure input voltages in the ± 10 V (− 10.240 V to + 10.235 V) range with an LSB of .005 volts. To use the card in a range other than the standard (± 10 V), change the LSB of the card to correspond to the range selected (e.g. the ± 100 V range requires an LSB of .05 V). The range switch settings are described in Section III of the manual. The LSB value can be set either by using a Set Format (SF) instruction or by changing jumpers on the card.

1-7 The A/D card uses a high performance sample/hold amplifer and a successive approximation A/D converter circuit which provides a high conversion speed and excellent accuracy characteristics. The dc input voltage is guarded to maintain high input impedance. Optically coupled isolators are used to isolated the dc input voltage from the data lines.

1-8 The converted 12-bit digital word, indicating the magnitude and sign of the measured voltage, is stored on the card and is always available for readback to the Multiprogrammer mainframe memory using card subaddress 0. As many as 1339 readings can be stored in mainframe memory. The M ıltiprogrammer firmware converts the digital word to decimal form for readback to the controller. The controller can read back the voltage value using the appropriate HP-IB extended talk address.

1-9 The 12-bit data word (voltage reading) is also routed to the A/D card's edge connector so that the A/D card can be used in conjunction with the 69790B Memory card to make measurements at rates that exceed the throughput of the controller. Up to 33,000 readings per second can be transferred from the A/D Converter card to the Memory card via the edge external connectors on each card. Each reading can be initiated by program commands or by an External Trigger (EXT) signal. Either the 69736A Timer Pacer or the 69735A Pulse Train Output card can be used to externally trigger the A/D Converter. The 69736A Timer/Pacer is programmed in a convenient seconds-milliseconds-microseconds format for programmable delay or continuous triggering. The 69735A Pulse Train Output card produces a programmable number of trigger pulses at a programmable rate. Chapter 7 in the 6942A Multiprogrammer User's Guide, HP Part No. 06942-90003, gives sample multiple card programs for the 69751A A/D, 69790A Memory, 69736A Timer/Pacer, and the 69735A Pulse Train output cards.

1-10 SPECIFICATIONS

1-11 Specifications and other supplemental data for the Analog-to-Digital Converter Card are given in Table 1-1.

1-12 CARD AND MANUAL IDENTIFICATION

1-13 Hewlett-Packard I/O cards are identified by a two-part serial number, for example, 1912A-88040. This number appears on a label affixed to the component side of the circuit card. The breakdown of the serial number is explained using the example number 1912A-00840.

Table 1-1 Specifications and Supplemental Data

Switch Selectable Input Voltage Ranges:

Nominal Range	Actual Range	Resolution
± 10 V	−10.240 to +10.235	5 mV
± 1 V	−1.0240 to +1.0235	500 μV
±100 mV	−0.10240 to +0.10235	50 μ V

Accuracy of Switch Selectable Voltage Ranges:

At 20-30°C ambient temperature outside mainframe,
for 24 hours: ±0.15% of full scale.
for 90 days: ±0.25% of full scale.
At 0-55°C ambient temperature outside mainframe,
for 24 hours: 0.4% of full scale.
for 90 days: ±0.5% of full scale.

Attenuator Input Voltage:

Nominal Range	Actual Range	Resolution
±100 V	−102.24 to +102.35	50 mV

Accuracy of ±100 V Attenuator Input Range:

At 20-30°C ambient temperature outside mainframe,
for 24 hours: ±400 mV.
for 90 days: ±500 mV.
At 0-55°C ambient temperature outside mainframe,
for 24 hours: ±750 mV.
for 90 days ±850 mV.

Input Impedance:

Range	Impedance
±10 V, ± 1 V	10,000 MΩ shunted by 15 pF.
±100 mV, ±100 V	10 MΩ shunted by 20 pF.

Conversion Time:

30μs per conversion max.

Settling Time:

Range	Settling Time (to within 0.01%)
±100 mV	40 μsec.
± 1 V	16 μsec.
± 10 V	15 μsec.
±100 V	1 msec.

Specification is for a step change equal to 50% or less of the full scale range (e.g. a 10 volt step on the ± volts range). Settling times to 0.1% are approximately 70% of those specified for settling to 0.01%.

Common Mode Rejection:

AC Rejection with 1Ω in the LO input lead:
120 db at 60 Hz
80 db at 10 kHz
AC Rejection with 1kΩ in the LO input lead:
60 db at 60 Hz
20 db at 10 kHz

Maximum DC or Peak AC with respect to the mainframe common (earth ground) must be less than/equal to 250 volts.

Sample/Hold Aperture Time:

200 nanoseconds max.

Switch-to-Hold Delay:

less than 1 μsec. and constant within ±200 nsec. with respect to an External Trigger.

Voltage Rating:

Voltage between either the analog input or the isolated common and ground must not exceed 250 Vdc or ac.

External Digital Outputs:

12-bit data output. In the high state, the outputs will source up to 200μA at 3.8 V minimum. In low state, the outputs will sink up to 70 mA at 0.4 V maximum.

All output control lines at the edge connector are open collector and have these specifications:
Logic High = 3.7 V while sourcing 200 μA.
Logic Low = 0.5 V while sinking 7 mA.

All input control lines at the edge connector are applied to schmitt trigger circuits and have these specifications:
Logic High = 2.0 V to 5.0 V (or no connection).
Logic Low = 0 V to 0.I5 V (short to ground).

Temperature Range:

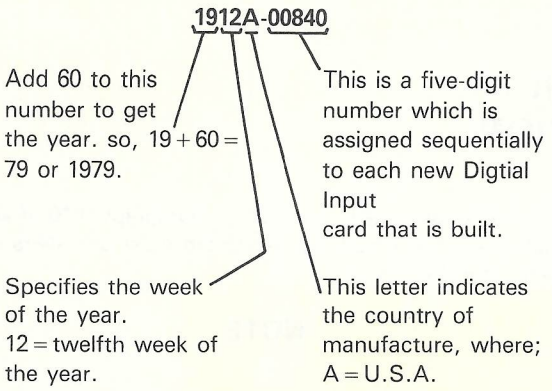
From 0°C to +70°C operating in the mainframe (allow 15°C internal rise in temperature when operating in the mainframe at up to +55°C ambient); from −40°C to +80°C storage.

Card Dimensions:

299.722 mm x 132.08 mm (11.8 in. x 5.2 in.)

+5 V Current Drain:

150 mA



1-14 The first part of this serial number (year and week) indicates the last date when a significant design change was made.

1-15 Each I/O card is equipped with a handle that is marked to identify the card type (e.g. A/D Converter). The handle is located at the card's outer edge and facilitates the removal and installation of the card.

1-16 OPTIONS

1-17 To obtain additional Operating Manuals when the A/D Converter card is shipped, request Option 910 when ordering the card. One additional manual will be shipped with each Option 910 ordered.

1-18 ACCESSORIES

1-19 One external connector is shipped with each I/O card. Order model 14703A when extra connectors are required to fabricate cables for several different applications.

1-20 A deinsertion tool is available to remove the contacts from the connector. This tool can be ordered from Hewlett-Packard (HP P/N 8710-0690).

Section II
INSTALLATION

2-1 NEW CARD INSPECTION

2-2 Before it left our factory, the card was inspected for electrical and mechanical flaws. As soon as you receive it , check to make sure it has not been damaged in shipment. If it has been damaged, report it to the carrier immediately, and notify the nearest HP Sales Office. Warranty information is printed on the inside cover of this manual.

2-3 The shipping invoice on the carton lists everything which should be inside. Check to make sure that you have received everything on the invoice. If anything is missing, report it to the nearest HP Sales Office. The Sales Offices are listed at the rear of this manual.

2-4 SHIPPING THE CARD

2-5 Save the shipping carton and packaging materials. You may need them to ship the card in the future. If the carton is lost, you can order a new one from an HP Sales Office. Ship the card only in a package designed for it. When you ship the card to an HP Service center for repairs, attach a tag to it identifying the owner. On the tag, give the model number and a brief description of the problem.

2-6 CARD INSTALLATION

2-7 The steps for preparing and installing an A/D Converter card are outlined below. Follow the sequence of steps carefully, to make sure that the card is installed properly. You may not have to perform all of the steps, but check each step to make sure that the card is set up properly. Each step is explained in detail in the following paragraphs.

1. Select analog input range.
2. Check data type and LSB "wake-up" values.
3. Select isolated bias supplies.
4. Install card in multiprogrammer.
5. Make connections to card's edge connector.
6. Turn on and perform verification.

2-8 Select Analog Input Range

2-9 As shipped from the factory, the A/D Converter card is configured to convert analog input signals in the ±10 V range (nominal). Signals in the ±100 mV or ±1 V range can be selected by changing the card's range switch setting (see paragraph 3-4). Voltages in the ±100 V range must be connected to the card's ÷10 attenuator (see paragraph 3-34).

2-10 In addition to the four standard ranges (±100 mV, ±1 V, ±10 V, ±100 V), range jumpers allow the card to monitor 16 optional ranges (8 bipolar and 8 unipolar ranges). The selection of optional range is described in paragraph 3-10. If an optional range is selected, the A/D card must be calibrated as described in Section V.

NOTE

Table 2-1 lists each of the jumpers on the A/D card and specifies how the jumpers are set when the card is shipped from the factory. The jumper locations are shown on Figure 7-1 in the rear of the manual. Instructions for changing the jumper positions are given in the Section III paragraph listed in the table.

Table 2-1. As-Shipped Jumper Connections

Jumper Number	In/ Out	Purpose	Paragraph
W1	out	External Bias Pos Input	
W2	out	External Bias Common	
W3	out	External Bias Neg Input	3-20
W4	out	Negative Regulator Bypass	
W5	out	Positive Regulator Bypass	
W6	out		
W7	in		
W8	out	Range Jumpers	3-8
W9	in		
W10	out		
W11	out	MSB Not Inverted	
W12	in	MSB Inverted	3-11
W13	out	Trigger Polarity Select	3-21
W14	in		
W15	in		
W16	in	Data type Jumpers	3-13
W17	out		
W18	out		
W19	out		
W20	out		
W21	out	LSB Jumpers	3-13
W22	in		
W23	in	Bidirectional Data Transceivers Jumper	3-23
W24	out		
W25	out	Isolated Bias No. (200 mA)	3-19
W26	out		
W27	out		
W28	out	Isolated Bias No. 2 (400 mA)	3-19
W29	out		
W31	in		
W31	in	Isolated Bias No. 1 1 A)	3-19
W32	in		

2-11 Data Type and LSB "Wake-Up" Values

2-12 Each card model is manufactured with jumpers that are positioned to specify the data type and LSB values that become effective for that card when power is applied. The A/D is shipped with jumpers set allowing bipolar readings in the ± 10 V range. If another range is selected, the data type and/or LSB values must be changed as described in paragraph 3-13.

2-13 Select Isolated Bias Supplies

2-14 The bias voltage for the analog circuits on the A/D card can be obtained from a mainframe isolated supply or from an external isolated supply.

2-15 Mainframe Isolated Power Supplies. The 6942A and 6943A mainframes contain three ± 18 V supplies with outputs isolated from the digital common and from each other up to voltages of 250 Vdc or 250 V peak. These supplies are used to power the analog circuitry of many I/O cards. Three separate supplies are provided so that individual cards or groups of cards can be electrically isolated from each other when necessary. All models of cards that use these supplies are equipped with jumpers so that any one of the three supplies can be used to power the card. When shipped from the factory, all cards are jumpered to ± 18 V Supply No. 1. Jumpers may have to be changed on one or more cards if several are installed in one mainframe or if some cards must be isolated from others. The jumpers used for ± 18 V supply selection are described in paragraph 3-19. The current requirements for all I/O card models that use the isolated supplies are in the following paragraphs.

2-16 Here are the current ratings of the three ± 18 V supplies and the current requirements of the six card models that use isolated mainframe power.

	Positive Output	Negative Output
± 18 V Supply No. 1	1.0 A	0.60 A
± 18 V Supply No. 2	0.4 A	0.25 A
± 18 V Supply No. 3	0.2 A	0.15 A

	Positive Input	Negative Input
69720A D/A Voltage Converter	80 mA	40 mA
69721A D/A Current Converter	110 mA	60 mA
69751A A/D Converter	150 mA	80 mA
69752A 64-Chan. FET Scanner	60 mA	40 mA
69755A 16-Chan. FET Scanner	45 mA	20 mA
69755A Counter/Totalizer	120 mA	15 mA

2-17 Power supply loading calculations can be based on the figures for the positive supply outputs and card requirements. If these are within limits, the negative supply loadings are also within limits. Once an overall plan for isolated biasing is developed, selection of an internal (mainframe) bias source for a particular 69751A card involves installation of the three jumpers associated with the selected source and removal of the external bias jumpers as well as the jumpers for the other two internal bias sources.

CAUTION

Apply power with jumpers for more than one internal bias source installed will blow fuses in the mainframe and may result in damage to the bias sources, to circuits on the 69751A card, or to other cards connected to one of the short-circuited bias sources.

2-18 External Isolated Power Supplies. A regulated or unregulated external isolated supply can be used instead of the isolated mainframe supply. If a decision is made to use an external bias source, the mainframe supply jumpers must be removed and the external supply jumpers installed as described in paragraph 3-20.

2-19 Install the Card in the Multiprogrammer

2-20 To install the A/D Converter card in the mainframe, proceed as follows:

CAUTION

Before installing or removing I/O cards from the Multiprogrammer, always turn the power off to prevent damage to the cards or the mainframe.

a. Select a slot for the card in the Multiprogrammer mainframe. The card is programmed by sending data to the slot in which the card is installed. Slot 0 has the highest interrupt priority, and slot 15 has the lowest.
b. Remove the rear cover of the Multiprogrammer and slide the card into the slot, with the components on the right. Push it in until it touches the connector.
c. Pull the card's extractor handle down to engage the notch at the bottom of the card cage, then push it back up to lock the card in the connector.

2-21 Make Connections to Card's Edge Connector

2-22 Use the edge connector shipped with the card to connect the analog input, external digital outputs and control signals to the card as needed. This connector and associated input and output signals for the A/D card are described in paragraphs 3-31 through 3-38. Note that if the EXTERNAL TRIGGER input is used, the TRIGGER DELAY BYPASS switches must be set to the appropriate positions (see paragraph 3-25).

2-23 You will have to assemble the connector on your own cable. The instruction sheet packed with the connector tells how to assemble the connector. When you have assembled the cable and tested it to make sure that all connections are correct, you can connect it to the card's edge and replace the Multiprogrammer's rear cover. The rear cover helps to hold the card-edge connectors in place and protects the cards and connectors.

2-24 Turn-On and Perform Verification

2-25 After the card is installed and the external connections completed, you can run either of two test programs in the 6942A Multiprogrammer User's Guide. The tests are:

a. The self-test error detection and card ID utility program, described in Chapter 2 of the User's Guide. The program checks the card's Universal Control Chip and Input Data Storage, and reads the Card ID/Status Buffer.

b. Example 7-27 of the User's Guide, which can be run to convert an externally applied voltage to a display value.

Section III
PRE-OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 The purpose of this section is to provide the User with additional information that may be required for either of the following reasons:

- The User wishes to change the card's switches or jumpers from their "as shipped" positions to some new positions.
- The User requires additional information on the edge connector I/O signals in order to make interconnections to external equipment.

3-3 Since the above actions can affect the operation of the card, the information in this section should be read before implementing any card changes. The information is presented in the following sequence.

- Range Switches
- Card Jumpers
- Trigger Delay Bypass Switches
- External Edge Connector Signals

3-4 RANGE SWITCHES (Table 3-1)

3-5 Range switches on the card must be set to the applicable input range. Range switch assembly S1 consists of four individual OPEN/CLOSE type switches designated S1-1 through S1-4. Switches S1-1, S1-3, and S1-4 are labeled ±100 mV, ±1 V, and ±10 V, respectively (see Figure 7-1). Switch S1-2 is not used. The S1-1 S1-3, and S1-4 switches allow the card to measure voltage in the corresponding input range by setting the gain of the card's analog input amplifier. The ±10 V switch (S1-4) is also used for the ±100 V input range. Voltages in the ±100 V range are connected to the card's divide-by-ten attenuator as described in paragraph 3-34. To select the desired range, the applicable switch is closed and the other two switches are opened. The switch settings for each of the four standard input ranges and the associated LSB (minimum voltage step change) are listed in Table 3-1.

3-6 CARD JUMPERS

3-7 As mentioned in Section I, the A/D Converter card is

Table 3-1. Range Switch Settings

INPUT VOLTAGE RANGE	RANGE SWITCH SETTINGS**			LSB***
	S1-1	S1-3	S1-4	(Min. Volt. Step)
	(±100 mV	(±1 V)	±10 V	
±100 mV (+102.35 to −1024.0 mV)	CLOSE	OPEN	OPEN	0.5 mV
±1 V (+1023.5 to −1024.0 mV)	OPEN	CLOSE	OPEN	.5 mV
±10 V (+10.235 to −10.240 V)	OPEN	OPEN	CLOSE	.005 V
±100 V (+102.35 to −102.40 V)	OPEN	OPEN	CLOSE	.05 V

* The card is shipped with switches set for ±10 V/±100 V ranges. Voltages in the ±100 V range must be connected to card's divide-by-ten attenuator.

** Range Switch S1-2 is not used.

*** When using an SF instruction, the allowable range of values for the LSB parameter is from .001 to 65.535.

**** LSB wake-up value, see paragraph 3-13.

shipped with certain jumpers in place. When the User wishes to change a jumper(s), the information in the following paragraphs should be referenced to see what jumper arrangements are possible. The jumpers are shown in Figure 7-1 and are described in the following paragraphs.

3-8 Range Jumpers (Table 3-2)

3-9 In addition to the range switches (±100 mV, ±1 V, and ±10 V) and the divide-by-ten attenuator (±100 V range), the card is equipped with range jumper options W6 through W12. As shipped from the factory, only range jumpers W7, and W9, and W12 are installed allowing the card to monitor bipolar voltage in any standard input range (±100 mV, ±1 V, ±10 V, or ±100 V). The card is also calibrated at the factory to operate in any standard input range (see Section V). The range jumper options allow the card to be converted to monitor any one of 16 optional ranges. If an optional range is selected, the card must be recalibrated. Section V describes calibration procedures for the optional input voltage ranges.

3-10 Table 3-2 shows the optional range jumpers, range switch settings and scaling resistor (R16) values for 16 optional input voltage ranges. Each of four jumper configurations yields four ranges. Once the jumper configuration is selected and the card is calibrated, the desired range is selected using switch 1.

3-11 Most Significant Bit Jumpers W11, W12

3-12 This pair of jumpers is used to provide complementing or non-complementing of bit position 12 of the 12-bit converted digital word. As can be seen in Table 3-2, for BIPOLAR analog signals W11 is removed and W12 is installed (complementing occurs). For UNIPOLAR analog signals, W11 is installed and W12 is removed (non-complementing).

3-13 Data Type and LSB Jumpers (Tables 3-3 and 3-4)

3-14 Each card model is manufactured with jumpers that are positioned to specify the data type and the LSB value that becomes effective for that card when the system is first energized. A/D Converter cards are shipped with data type and LSB

Table 3-2. Optional Input Voltage Ranges

OPTIONAL VOLTAGE RANGES	** LSB	RANGE JUMPERS							RANGE SWITCHES***		
		W6	W7	W8	W9	W10	W11	W12	S1-1	S1-3	S1-4
BIPOLAR RANGES (R16 = 121Ω)											
±50mV(+51.175 to −51.200mV)	.025mV	0	1	0	0	1	0	1	CLOSE	OPEN	OPEN
±0.5V(+511.75 to −512.00mV)	.25mV	0	1	0	0	1	0	1	OPEN	CLOSE	OPEN
± 5V(+5117.5 to −51220.0mV)	2.5mV	0	1	0	0	1	0	1	OPEN	OPEN	CLOSE
*±50V(+51.175 to −51.20V)	.025V	0	1	0	0	1	0	1	OPEN	OPEN	CLOSE
(R16 = 61.9Ω)											
±25mV(+25587.5 to −25600.0μV)	12.5μV	0	1	1	0	1	0	1	CLOSE	OPEN	OPEN
±0.25V(+255.875 to −256.00mV)	.125mV	0	1	1	0	1	0	1	OPEN	CLOSE	OPEN
±2.5V(+2558.75 to −2560.00mV)	1.25mV	0	1	1	0	1	0	1	OPEN	OPEN	CLOSE
*±25V(+25587.5 to −25600.0mV)	12.5mV	0	1	1	0	1	0	1	OPEN	OPEN	CLOSE
UNIPOLAR RANGES (R16 = 121)											
0 to +100mV (0 to +102.375mV)	.025mV	1	0	0	0	1	1	0	CLOSE	OPEN	OPEN
0 to +1V (0 to +1023.75mV)	.25mV	1	0	0	0	1	1	0	OPEN	CLOSE	OPEN
0 to +10V (0 to +10237.5mV)	2.5mV	1	0	0	0	1	1	0	OPEN	OPEN	CLOSE
*0 to +100V (0 to +102.375V)	.025V	1	0	0	0	1	1	0	OPEN	OPEN	CLOSE
(R16 = 61.9Ω)											
0 to +50mV (0 to +51187.5μV	12.5μV	1	0	1	0	1	1	0	CLOSE	OPEN	OPEN
0 to +0.5V (0 to +511.875mV)	.125mV	1	0	1	0	1	1	0	OPEN	CLOSE	OPEN
0 to +5V (0 to +5118.75mV)	1.25mV	1	0	1	0	1	1	0	OPEN	OPEN	CLOSE
*0 to +50V (0 to +51187.5mV)	12.5mV	1	0	1	0	1	1	0	OPEN	OPEN	CLOSE

1 = JUMPER IN, 0 = JUMPER OUT

*These inputs must be connected to card's divide-by-ten attenuator

**When using an SF instruction, the allowable range of values for the LSB parameter is from .001 to 65.535.

***Range switch S1-2 is not used.

Table 3-3. A/D Converter Card, Data Type Jumpers

Data Type Code	Description	W18	W17	W19	W15	W14	W16
1*	Two's Complement input word is returned to controller in decimal form	0	0	0	1	1	1
2	Sign-Magnitude input word is returned to controller in decimal form	0	0	1	1	1	0
3	Unsigned binary input word is returned to controller in decimal form	0	1	0	1	0	1
4	(Special Autorange code used only with 69736A Timer/Pacer Card)	-	-	-	-	-	-
6	Unsigned BCD input word is returned to controller in decimal form	1	0	1	0	1	0
7	Unsigned binary input word is returned to controller in octal form	1	1	0	0	0	1

*When the card is shipped, its jumpers are arranged to select the starred data type when the power is applied to the system.

Table 3-4. A/D Converter Card, LSB Jumpers

LSB Code	LSB Value	Jumper Arrangement		
		W20	W21	W22
0	0.001	1	1	1
1	0.025	1	1	0
2	0.1	1	0	1
3	0.5	1	0	0
4	0.01	0	1	1
5	0.05	0	1	0
6	0.005*	0	0	1
7	1.0	0	0	0

1 = Jumper In 0 = Jumper Out

*When the card is shipped, its jumpers are arranged to select the starred LSB value when power is applied to the system.

jumpers W14 through W22 arranged as indicated in Tables 3-3 and 3-4. This configuration assigns the card a data type in which input data in two's complement binary form, with an LSB value of .005 V, is returned to the controller in decimal form. Thus, when power is turned-on, the A/D card is configurated to measure a bipolar range of voltage readings from +10.235 to −10.240 volts.

3-15 The card's data type and LSB jumpers can be repositioned to select one of the other data types and LSB values listed in Tables 3-3 and 3-4, thus making a different data type or LSB value effective at system turn-on. Changing the jumpers to select data type 3 and an LSB of 2.5 mV allows a unipolar range of voltage readings from 0 to +10237.5 mV (see Section V).

3-16 As an alternative to changing the jumpers on the card, it is also possible to program a card's data type and LSB value to be different from those established by its jumpers by using a Set Format (SF) instruction. Any of the data types of Table 3-3 can be used, but programmed LSB values are not limited to those in Table 3-4. Any desired LSB value between 0.001 and 65.535 can be programmed. Before they are returned to the controller, then, input data values are scaled to correspond to units appropriate to the process to which the card is dedicated. (See Chapter 5 of the 6942A User's Guide for instructions on using the Set Format instruction.)

3-17 External and Mainframe Isolated Bias Supply Jumpers (Table 3-5)

3-18 The ±15 V bias voltage for the card's input amplifier, sample and hold amplifier, and A/D converter circuits can be obtained from a mainframe isolated supply or from an external isolated supply. As shipped from the factory, an A/D card's jumpers are arranged to select Isolated Supply No. 1 in the mainframe (see Table 3-5).

3-19 **Mainframe Isolated Power Supply.** The isolated ±18 V supplies in the mainframe are designated 1, 2 and 3. For maximum flexibility, they have three different nominal current capacities: Supply No. 1 is rated at 1 A, Supply No. 2 is rated at 400 mA, and Supply No. 3 is rated at 200 mA. For the purpose of planning the loading of these supplies, each A/D Converter card can be considered to be a 150 mA load. Up to nine A/D Converter cards may be used in a mainframe when the isolated power supply jumpers are positioned to bias up to six cards from Supply No. 1, two cards from Supply No. 2, and one card from Supply No. 3. See paragraph 2-16 for the current drains of the other cards that can use these isolated ±18 V supplies. Table 3-5 lists the A/D card jumper connections for each of the ±18 V isolated supplies.

CAUTION

Use of the mainframe bias sources with W4 and W5 installed will compromise the accuracy of the 69751A High Speed A/D card and may damage components in the analog subsystem.

3-20 **External Isolated Power Supplies.** A regulated or unregulated external isolated supply can be used to power the card's input amplifier, S/A amplifier, and A/D Converter circuits. If a regulated external supply with ±15 V outputs is used, the on-board ±15 V regulators are bypassed by installing jumpers W4 and W5 (see Table 3-5). Note that if the on-board regulators are bypassed, the card must be recalibrated as described in Section V. A regulated or unregulated external supply with ±17.7 V to ±20 V outputs can be used if the on-board regulators are made operational by removing jumpers W4 and W5. (Each A/D Converter card draws approximately 150 mA from an external isolated supply.)

Table 3-5. A/D Converter Card, Isolated Power Supply Jumpers

		Jumpers													
		W1	W2	W3	W4	W5	W24	W25	W26	W27	W28	W29	W30	W31	W32
Mainframe Isolated Power Supplies	±18 V Supply 1*	0	0	0	0	0	0	0	0	0	0	0	1	1	1
	±18 V Supply 2	0	0	0	0	0	0	0	0	1	1	1	0	0	0
	±18 V Supply 3	0	0	0	0	0	1	1	1	0	0	0	0	0	0
External Isolated Power Supplies	Regulated or Unregulated +17.7 to 19.9 V	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Regulated ±15 V	1	1	1	1	1	0	0	0	0	0	0	0	0	0

*When the card is shipped, its jumpers are arranged to select the starred isolated power supply when power is applied to the system.

CAUTION

Reversal of the positive and negative external bias inputs will result in catastrophic failure of the hybrid A/D converter with a high probability of other damage to the 69751A card as well. Do not apply bias power until the connections are throughly checked.

3-21 Trigger Polarity Select Jumper

3-22 This jumper (W13) is removed prior to shipment making the Trigger Polarity Select (TPS) control line a logic high. If this jumper is installed, the TPS control line is held at a logic low level. The purpose of the Trigger Polarity Select signal is discussed in Table 3-6.

3-23 Bidirectional Data Transceivers Jumper

3-24 This jumper (W23) is installed at the factory and, normally is never removed. This jumper estalishes pin 9 of tri-state integrated circuits U31 and U32 (see Figure 7-2) at ground. With pin 9 grounded, the open or isolated state of the transceivers is not used. Jumper W23 is temporarily removed during factory testing to allow the outputs of the transceiver to assume an open state for test purposes.

3-25 TRIGGER DELAY BYPASS SWITCH

3-26 Most of the system's I/O cards can be cycled through an external trigger input to the card, but in some applications the 13 to 17 microsecond delay between the trigger signal and the A/D card's cycling does not allow sufficiently close synchronization with the external event. Trigger Delay Bypass Switches (S2), see Figure 7-1, on the A/D card allow it to be triggered externally with a delay of only 1 microsecond if it can be assumed that the external trigger will not occur while the card is being cycled through software.

CAUTION

Only one of the three switches, designated S2-1, S2-2, and S2-3, should be closed at a time.

3-27 S2-1 is normally closed, allowing the card to be cycled either through software or through an external trigger. with S2-1 closed, the 13 to 17 microsecond delay is in effect for external triggers.

3-28 If S2-2 is closed, the external trigger input is actuated by a positive-going signal and the delay is reduced to 1 microsecond. With this switch closed, the card can be cycled only through an external trigger and not through software.

3-29 If S2-3 is closed, the external trigger input is actuated by a negative-going signal and the delay is reduced to 1 microsecond. Again, the card can be cycled only through an external trigger and not through the software.

3-30 If is not necessary to install or remove jumper W13 to change the external triggers's input logic sense when S2-2 or S2-3 is closed.

3-31 EXTERNAL EDGE CONNECTOR SIGNALS

3-32 One dual 36-pin edge connector is supplied with each I/O card for interfacing field wiring to the card. Instructions for making up the mating connector and hood assembly are provided in Chapter 2 of the 6942A User's Guide.

3-33 The pin assignments of the input and output signals available at the edge connector supplied with the card are shown in Figure 3-1. The lettered pins are on the component side of the card, numbered pins on the opposite side.

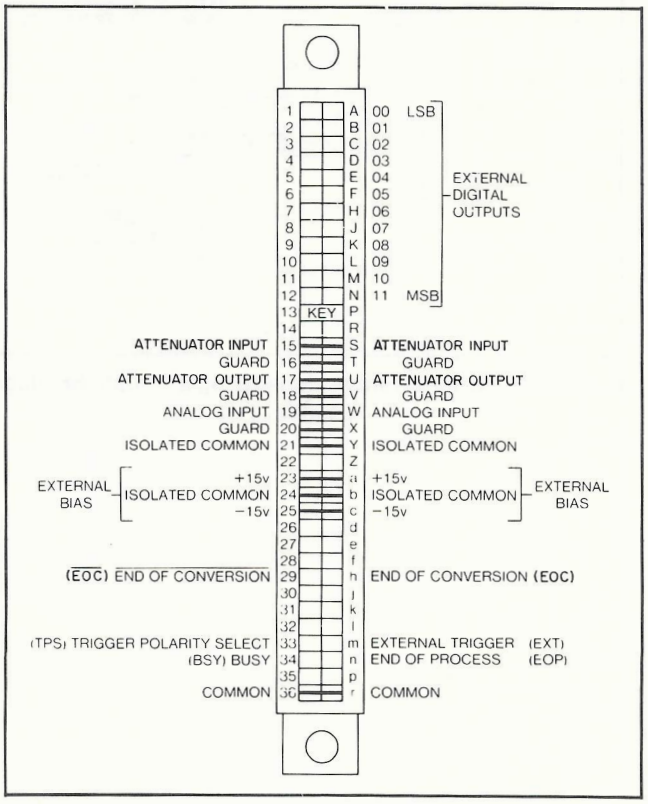


Figure 3-1. A/D Converter Card, External Edge Connector

CAUTION

To maintain voltage rating, do not install contacts or dummy pins in positions 14, 27, R, or e.

3-34 Analog Input

3-35 The dc input voltage to be measured is connected between the analog input (pins W, 19) and the isolated common (pins Y, 21) of the edge connector. Voltages in the ±10 V, ±1 V, or ±100 mV range are connected directly to the analog input. Voltages in the ±100 V range, however, must be connected to the attenuator input (pins S, 15) and a jumper wire connected between the attenuator output (pins U, 17) and the analog input (pins W, 19).

3-36 A guard circuit on the card prevents input signal leakage when high impedance sources are connected to the analog input. The GUARD pins on the edge connector allow this protection to be extended to the analog voltage source. Figure 3-2 illustrates GUARD connections using a double shielded cable.

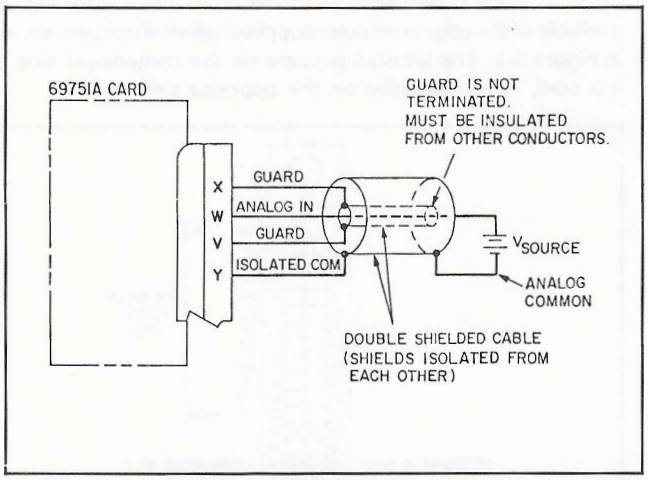


Figure 3-2. Guard Connections Using a Double Shielded Cable

3-37 I/O Control Signals

3-38 Table 3-6 describes the control signals and bias voltages which interconnect between the A/D Converter card and the Customer's equipment. The electrical specifications of these signals are given in Table 1-1 of Section I. The direction of control signal flow between the A/D card and the Customer's equipment is illustrated in Figure 3-3.

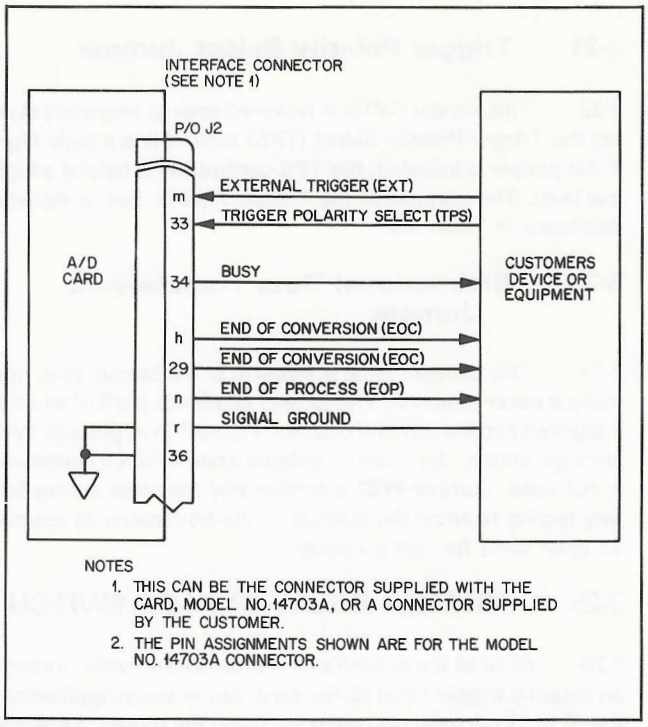


Figure 3-3. External I/O Control Signals, Interface Diagram

Table 3-6. Card's External I/O Control Signals, Interface Diagram

I/O Control Signal	Pin No.	TTL Level	Description
TRIGGER POLARITY SELECT also TPS (card input)	33	High	With pin 33 at a logic high and S2-1 closed, a low-to-high transition of the EXTERNAL TRIGGER line cycles the card. This is the as shipped state of pin 33.
		Low	With pin 33 low (or jumper W13 installed) and S2-1 closed, a high-to-low transition of the EXTERNAL TRIGGER line cycles the card.
EXTERNAL TRIGGER also EXT (card	m	Edge Sensitive	This signal can be used to cycle the externally. For example, after a Write First (WF) rank instruction is used to cycle the card the TRIGGER POLARITY SELECT line determines the triggering edge.
BUSY	34	High	Busy goes high when the card is cycled either by an instruction or externally by the EXT. While Busy is high, the input analog voltage is being converted to digital.
		Low	Busy goes low at the end of conversion or when no conversion is in progress.
END OF CONVERSION also EOC	h	High	Goes high at the end of an analog to digital conversion and remains high for approximately 1 to 3 microseconds.
		Low	Conversion not completed.
$\overline{\text{END OF CONVERSION}}$ Also EOC	29		Logical complement of pin h.
END-OF-PROCESS also EOP (card output)	n	High	Goes high when EOC goes high. EOP remain high for a minimum of 2μs and stays high for a time dependent on the program. Pin n going high can be used as an indication that the operation is completed and the converted digital word at edge connector can be read.
		Low	EOP is set low by the Multiprogrammer in response to an interrupt request.
EXTERNAL BIAS +15 V −15 V Isolated Common	 23,a 25,c 24,b		These pins permit external application of +15 V instead of local +15 V. These pins permit external application of −15 V instead of local −15 V. These pins are used together with the +15 V pins or −15 V pins to provide common return.

Section IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the A/D Converter card. The theory assumes that the reader is familiar with the instruction set and the basic operation of the 6942A Multiprogrammer. First, a brief description is given on the basic operation and features of the card. A detailed block diagram discussion then follows. This section concludes with an example of the processing of an input instruction in making an A/D conversion (voltage measurement).

4-3 OVERALL OPERATION

4-4 Power Turn-On

4-5 When power is applied to the A/D Converter card, the circuits on the card are first cleared. Then a self test is initiated by the Multiprogrammer to test the circuits of the A/D Converter card. The self-ID, data type, size, and LSB parameters of the card are read and stored in the Multiprogrammer memory as part of the wake-up sequence.

4-6 Tracking the Input Analog Signal

4-7 Immediately after power turn on, a sample and hold amplifier begins tracking whatever input analog voltage exists at the input edge connector. During this time, the A/D Converter card is operating in a "sample" mode, meaning that, although no data conversion is taking place, the output voltage of the sample and hold amplifier is continuously following (or tracking) the changes in the amplitude of the input analog signal. The A/D Converter card remains in this mode until the card is cycled. While in the sample mode, a high guard amplifier eliminates input signal leakage which could prevent accurate voltage measurements. In addition, a variable gain input amplifier operating on the input voltage level permits analog signals to be measured from ±25 millivolts to ±100 volts full scale depending upon the setting of various jumpers and switches on the card.

4-8 Measuring the Input Analog Signal Voltage

4-9 To measure the voltage of the input analog signal, the card must be cycled to make an A/D conversion. The actual conversion is performed by a successive approximation A/D converter chip which can perform 12-bit A/D conversions at rates up to 33KHz. The card can be cycled in one of two ways:

1. by the Multiprogrammer (under program control) by issuing an Input Instruction like an IP or a Cycle Card Instruction "CY".
2. by an external trigger applied to the edge connector of the card.

4-10 In either case, when the card is cycled, the following events occur in the sequence given (see Figure 4-1):

a. BUSY and GATE signals go high. BUSY going high indicates that a conversion is in progress. This signal appears at the edge connector and can also be read by the program by inspecting bit 1 of the status register with a Read Stuats (RS) instruction. The BUSY signal remains high until the end of the conversion.
b. The GATE signal is used to generate a CONVERT signal which commands the A/D converter chip to being a conversion. The A/D converter responds by asserting a HOLD command which switches the sample and hold amplifier from "sample" mode to "hold" mode. In this mode, the output voltage of the S/H amplifier is frozen at whatever voltage value exists when the HOLD command is received. The purpose of the S/H amplifier is to present a constant voltage to the A/D converter while the conversion is being performed.
c. The A/D converter reads the voltage at the S/H amplifier output and begins an analog to digital conversion. During the conversion, a 12-bit binary word is shifted bit-by-bit into a temporary serial data register.

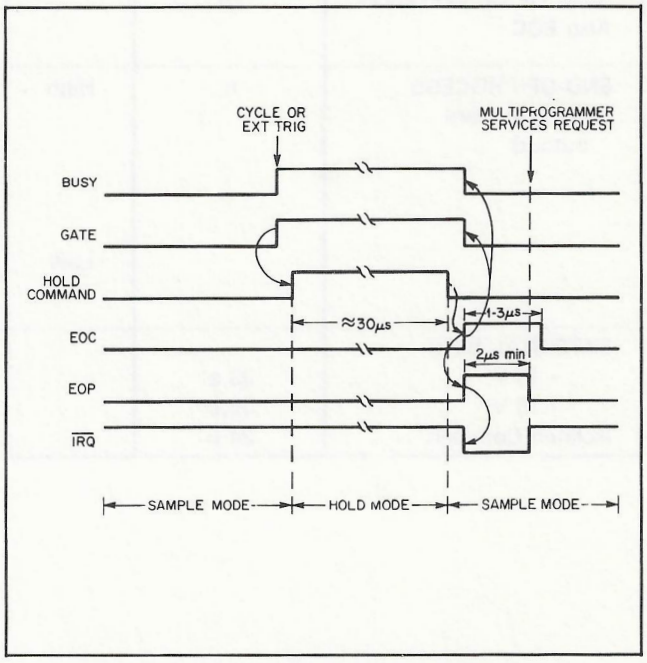


Figure 4-1. Analog-to-Digital Converter, Control Signal Timing

4-11 Storing the Converted Digital Word

4-12 The A/D converter chip completes the conversion in approximately 30 μsec. After this time has elapsed, these events take place:

a. The End-of-Conversion (EOC) signal goes high to indicate that the conversion is completed.

b. BUSY goes low to indicate that no conversion is in progress.

c. The End-of-Process (EOP) signal also goes high at this time, and if the card is armed, an interrupt request signal (IRQ) is returned to the Multiprogrammer from the A/D card. When the IRQ signal is generated, the Multiprogrammer responds by clearing the ARM, EOP and GAFF flags on the A/D card. The GAFF flag is internal to the Universal Control chip on the card and is set by instructions, such as; IP, II, IE, and CY to allow multiple cards to be cycled in parallel (or simultaneously). Refers to Chapter 4 in the 6942A Multiprogrammer User's Guide for more information on cycling cards in parallel.

d. The 12-bit word shifted into the serial register is changed into a 2' s complement binary word (unless jumper W12 is removed and W11 installed) and is loaded into an input data storage register for the subsequent transfer to the Multiprogrammer.

e. The 2's complement digital word is also applied to the edge connector to be read by the external device. The 12-bit binary word at the edge connector is valid only while the EOP signal is high and BUSY is low.

f. The S/H amplifier is switched back to the "sample" mode preparatory to making the next conversion.

4-13 Reading the Converted Digital Word

4-14 If the card was cycled with an External Trigger signal or with a Cycle Card Instruction, the converted digital word remains in the input data storage register until another instruction (for example, a Read Value instruction) is issued referencing subaddress 03 to read the data word. If the card was cycled as part of an input instruction like Input Parallel, IP, the converted data word is automatically read by the Multiprogrammer immediately after the conversion.

4-15 DETAILED BLOCK DIAGRAM DISCUSSION (FIGURE 4-2)

4-16 The following paragraphs described the functional circuits as represented in the detailed block diagram of Figure 4-2.

4-17 When the A/D Converter card is installed in a slot position in the Multiprogrammer, 6942A, or in the Extender chassis, 6943A, the card is assigned the address of that slot position. Once installed, the card connects to: the data lines (B0-B15), the control lines, and to the power input lines of the backplane.

4-18 Universal Control Chip (UCC)

4-19 Control chip (U33) supervises all the operations taking place on the A/D Converter card. The UCC establishes the timing sequence for the various control signals used on the card.

4-20 When power is applied to the card, the PCR control signal goes high and clears the input data storage register and the return buffer circuits on the card. The PCR signal is of sufficient duration to ensure that the control signal generators (EOF and clock generator one-shots) have settled to their quiescent states. The card is then ready to process any instruction issued at the controller that addresses the card. When an instruction is issued, the following input control lines set up the UCC for a particular operation:

a. CAD - This is the card address line which goes high to select the A/D Converter card when the card is addressed in an instruction.

b. R/ $\overline{W}$ - This is the read/write line. It is high for a Read value, Read Status instruction or an input data operation and is low for a write operation.

c. $\overline{SADO}$, $\overline{SAD1}$ - These two lines supply a subaddress to the card.

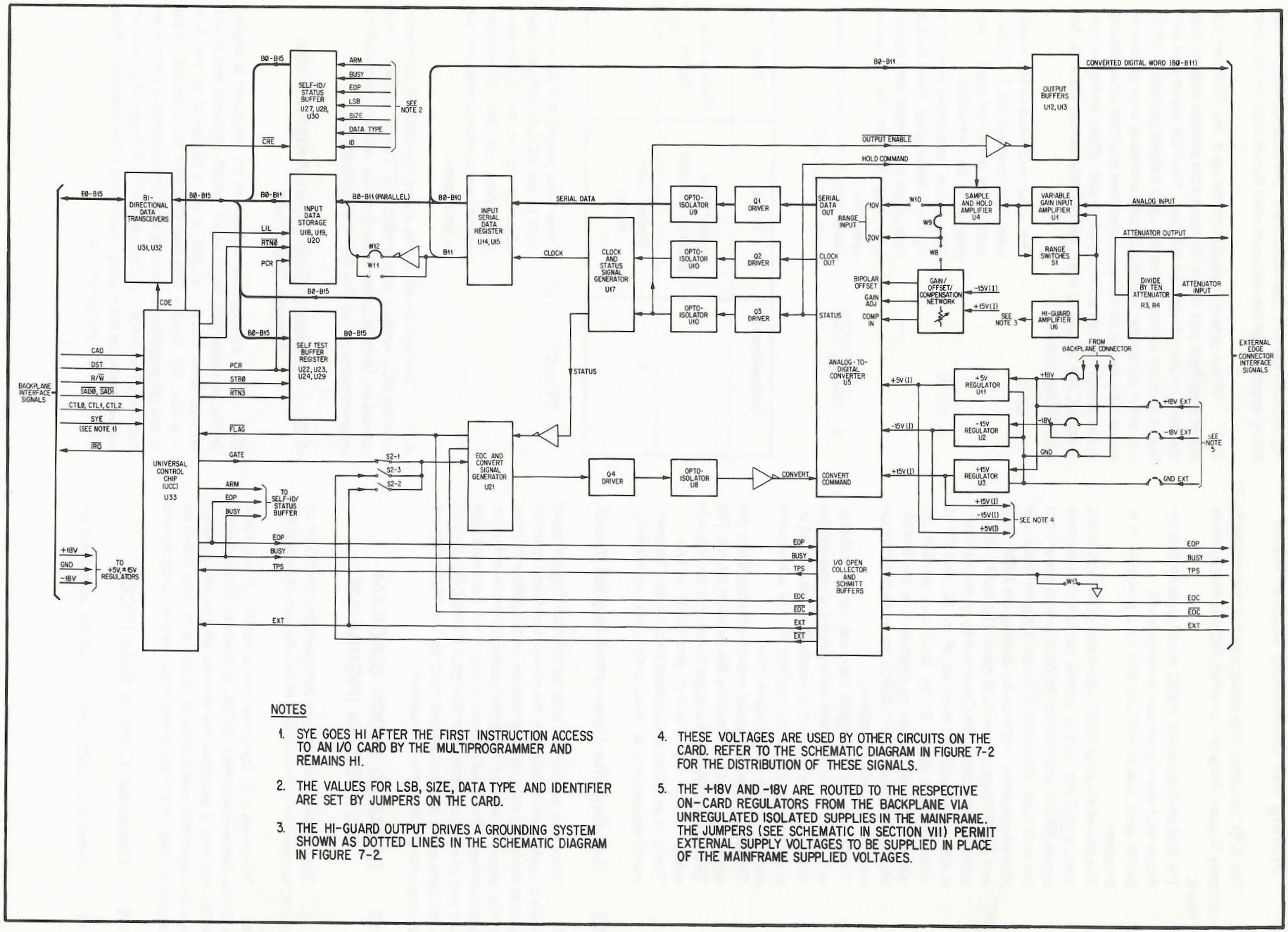
Subaddress	Read	Write
0	Input Data Storage Register	Return Data Buffer
3	Return Data Buffer	—

d. CTL0,CTL1,CTL2 - These lines supply a 3-bit control code to the UCC to indicate what operation is to be performed. Depending on the instruction issued, one or more codes are sent in succession.

4-21 The logic levels on the above control lines are loaded into the UCC when a data strobe (DST) pulse occurs. These signals are then decoded to produce the various control signal outputs required for the indicated operation.

4-22 Variable Gain Input Amplifier and Range Switches

4-23 The analog input voltage to be measured is applied to the non-inverting input of U1 which provides the proper voltage level from −10.240 V to ±10.235 V to the S/H amplifier, U4. Diodes CR1 and CR2 limit the maximum input to the U1 amplifier protecting it against excessive voltage excursions. The range switches determine the gain of U1 and are set according to the analog input range to be measured. Refer to Section III, paragraph 3-4.



NOTES

1. SYE GOES HI AFTER THE FIRST INSTRUCTION ACCESS TO AN I/O CARD BY THE MULTIPROGRAMMER AND REMAINS HI.
2. THE VALUES FOR LSB, SIZE, DATA TYPE AND IDENTIFIER ARE SET BY JUMPERS ON THE CARD.
3. THE HI-GUARD OUTPUT DRIVES A GROUNDING SYSTEM SHOWN AS DOTTED LINES IN THE SCHEMATIC DIAGRAM IN FIGURE 7-2.
4. THESE VOLTAGES ARE USED BY OTHER CIRCUITS ON THE CARD. REFER TO THE SCHEMATIC DIAGRAM IN FIGURE 7-2 FOR THE DISTRIBUTION OF THESE SIGNALS.
5. THE +18V AND -18V ARE ROUTED TO THE RESPECTIVE ON-CARD REGULATORS FROM THE BACKPLANE VIA UNREGULATED ISOLATED SUPPLIES IN THE MAINFRAME. THE JUMPERS (SEE SCHEMATIC IN SECTION VII) PERMIT EXTERNAL SUPPLY VOLTAGES TO BE SUPPLIED IN PLACE OF THE MAINFRAME SUPPLIED VOLTAGES.

Figure 4-2. 69751A A/D Converter, Detailed Block Diagram

4-24 Amplifier U1 provides unity gain (X1) in the ± 10 V range, a gain of 10 (X10) in the ±1 V range, and a gain of 100 (X100) in the ± 100 mV range. Potentiometer R2 is used to adjust the offset of the U1 input state. Potentiometer R15 is a fine gain adjustment for the ± 100 mV range. Adjustment procedures are provided in Section V. Analog inputs in the ± 10 V, or ± 1 V, or ± 100 mV range are connected between edge connector pins J2-19 and J2-21.

4-25 Divide-by-Ten Attenuator

4-26 This network reduces the input impedance to 10 meghoms and allows input voltages in the ± 100 V range to be measured. When this attenuator is used, the analog input signal is applied to pins J2-15,S. A jumper must be connected between J2-17, U (ATTENUATOR OUTPUT) and J2-19, W (ANALOG INPUT). When this network is used, the guard amplifier does not track the 10:1 divider input; only the high-impedance input at J2-19 is tracked. The ± 10 V range switch is also used for the ± 100 V range.

4-27 High-Guard Amplifier

4-28 High-guard amplifier U6 eliminates input signal leakage which can prohibit accurate voltage measurements. The high guard amplifier output develops the same potential as the analog input signal. The guard potential is applied to the guard conductors (shown as dotted line connections in Figure 7-2) which surround the input and feedback conductors where leakage could occur. Since the conductors are at the same potential, leakage current does not flow. The guard potential is available at edge connector pins J2-16,T,18,V,20,X (see Figure 3-1) so that the protection can be extended beyond the 69751A card to the analog voltage source if desired.

4-29 The analog signal to be measured is connected between the ANALOG INPUT (J2-19,W) and the ISOLATED COMMON (J2-21-Y) pins of the edge connector. The analog input signal as well as the guard connections are described in Section III.

4-30 Sample and Hold Amplifier

4-31 The sample and hold amplifier U4 is a high performance circuit that has excellent dc accuracy and a low drop rate (voltage decay at the output when in the hold mode). The sample and hold amplifier (X1 amplification stage) continuously samples the analog signal from the input amplifier for application to the A/D converter, U5. When the A/D converter's STATUS signal goes from the "ready" state (low) to the "busy" state (high), the sample and hold amplifier is switched from the sample mode to the hold mode and "freezes" the A/D's analog input to the value present just when the "hold" command was received. The sample and hold amplifier has a very fast acquisition time (typically 5μsec.) and an aperture time of 200nsec. Acquisition time is the time required for the sample and hold amplifier output to settle within a specified percentage of its final value when it is switched from hold to sample. Aperture time is the time required for the sample and hold amplifier to switch from sample to hold.

4-32 Analog-to-Digital (A/D) Converter

4-33 A/D converter, U5, converts the bipolar analog input received from the sample and hold amplifier into an equivalent serial 12-bit digital word. Potentiometers R18 and R19 are used to set the A/D's gain and offset errors to zero. Complementary Offset Binary (COB) coding is utilized on the A/D's serial data output line to represent the bipolar input signal range − 10.240 V to + 10.235 V.

4-34 The A/D converter is a successive approximation decoder with a conversion speed of 30μsec. It includes an internal clock, a precision D/A converter, comparator, and reference. Data is transferred out serially (one bit at a time) with corresponding A/D CLOCK to the data transfer control circuits. The serial data is synchronous with the A/D chip's internal clock and is available only during the conversion period. The most significant bit, B11, appears first followed by bits B10, B09, B08, etc. The conversion is initiated when the CONVERT COMMAND is received. The STATUS signal is also directed from the A/D chip through an optically coupled isolator to the output buffers and to the clock and status generator. Normally, only the CLOCK signal is used to control shifting of serial data into the input data register. However, the CLOCK pulses are "OR'ed" with the STATUS signal to ensure that the last serial data bit is always properly shifted into the input data register 0 (see the timing sequence description in paragraph 4-72

4-35 The serial data is assembled in the serial data register into an offset binary, parallel binary word that is proportional to the analog signal "frozen" at the A/D input when the conversion was inititated. Note that the input serial data register's MSB output is inverted to provide two's complement coding.

4-36 Once the conversion is completed, the control logic within the A/D converter switches the STATUS signal back to "ready" returning the S/H amplifier to the "sample" mode. The "busy" to "ready" transition of the STATUS signal also triggers the end-of-conversion (EOC) one-shot. The EOC signal is applied to the FLAG input of the UCC to signal the UCC that the conversion is completed. In addition, the EOC signal and its complement ($\overline{EOC}$) are routed to the card's edge connector so that they can be used to synchronize data transfers with an external device. Data (positive true) is available to the external device at the external edge connector.

4-37 Gain/Offset/Compensation Network

This network is used to perform calibration procedures on the A/D Card during Installation or when range jumpers are changed. Refer to Section V for further discussion of Calibration.

4-38 Voltage Regulators +5, +15, and −15 VDC

4-39 Bias power for the isolated circuits may be obtained from one of three internal isolated bias sources (as shipped connection (or from an external source connected to the appropriate pins of the edge connector.

4-40 Current Drivers

4-41 Transistors Q1, Q2, and Q3 are connected as emitter followers and provide the current drive required by the optical isolators.

4-42 Optically Coupled Isolators

4-43 All analog circuits on the 69751A card, including the hybrid successive approximation A/D converter, are isolated from the mainframe. CPU data common by means of optical isolators. This permits the measurement of low level signals in the presense of common mode voltages as high as 250 VDC or peak AC. The 69751A High Speed A/D card is designed so that the analog system (consisting of the input amplifier, the sample and hold amplifier, the A/D converter, and related circircuits) are electrically isolated by means of optocouplers from data common and earth ground. This technique provides all of the benefits traditionally associated with floating voltmeter measurements.

4-44 The high speed optically coupled gates achieve isolation and coupling with a propagation delay of only 45nsec (typical). A simplified schematic of an optically coupled gate is given in Figure 6-2. Note that the enable input (pin 7) is open circuited (no external pull-up resistor is required for a logic "1" enable input).

4-45 Input Serial Data Register

4-46 Serial data from the A/D converter chip is shifted into the serial data register by a clock which is generated within the A/D chip (U5) when a converison is being performed. Jumpers W11 and W12 select the logic sense of the most significant bit (MSB) of the 12-bit digital word in this register. All of the bipolar ranges use 2's complement coding. Jumper W11 is removed and W12 is installed to select the inverted logic sense required for 2's complement codes. The 69751A card is shipped with W11 and W12 in this configuration. Unipolar ranges use straight binary coding which requires that W11 be installed and W12 removed.

4-47 Input Data Storage

4-48 Initially, this register is cleared on power turn on. It is loaded with the 12-bit data word from the serial data register when a load input latch (LIL) control signal occurs. LIL is produced when the EOC control signal is generated after an analog conversion.

4-49 The contents of this register are transferred to the Multiprogrammer by an input instruction (e.g. IP) which references subaddress zero. Subaddress zero results in a low going $\overline{\text{RTN}}$ pulse which places the contents of the register on the B0-B11 lines to the backplane via the bi-direcitional transceivers.

4-50 EOC and Convert Signal Generators

4-51 The EOC generator produces a 1.5μsec. (nominal width) pulse delayed approximately 1μsec. from the end of the data conversion. The delay time allows the data to settle at the buffered output at the edge connector. The EOC generator is triggered by the status generator at the end of every conversion. The convert generator is triggered by one of three signals depending on the position of switch S2.

1. by a low-to-high going GATE signal when position 1 of S2 is selected. (This is the as-shipped setting of S2). The GATE may be generated by internal instructions (software) or by an EXT TRIGGER. With S2-1 closed there is a propagation delay of approximately 5μsec through the UCC for EXT TRIGGERS.
2. by a high-to-low going EXT TRIGGER signal, applied to pin m of the edge connector, when position 2 of S2 is selected. Wtih S2-2 closed, the propagation delay through the UCC is bypassed. With S2-2 closed, the ocnvert generator can be triggered only by an EXT TRIGGER and not through software.
3. by a low-to-high going EXT TRIGGER signal, applied to pin m of the edge connector, when position 3 of S2 is selected. With S2-3 closed, the propagation delay through the UCC is bypassed. With S2-2 closed, the convert generator can be triggered only by an EXT TRIGGER and not through software.

CAUTION

Only one of the three switches, S2-1, -2, or -3, should be closed at a time.

4-52 Normally, S2 is set to position 1 so the GATE signal triggers the convert generator. The CONVERT command then starts the A/D conversion cycle. If an EXT TRIGGER (instead of an internal instruction) is used to generate GATE, the 5μsec UCC propagation delay may not allow sufficiently close synchronization with the externla device. Consequently, when using EXT TRIGGER's) to initiate A/D conversion cycles, open S2-1 and close either S2-2 or S2-3.

4-53 Clock and Status Signal Generators

4-54 These are one shot circuits that are triggered by the CLOCK and STATUS signals from the A/D converter. During each A/D conversion cycle, the STATUS signal goes high and

is coupled to the status generator via an optical isolator. The isolator inverts the STATUS signal so that its trailing edge (low-to-high transition) triggers the status one-shot. The clock one-shot is continuously triggered by the serial clock from the A/D converter.

4-55 Output Buffers

4-56 These are open collector AND gates that buffer the 12-bit parallel digital word before it is applied to the edge connector. The data becomes valid when the OUTPUT ENABLE signal from the A/D converter chip is low indicating conversion completed (or ready).

4-57 Bidirectional Data Transceivers

4-58 These tri-state transceivers determine whether data can be written from the Multiprogrammer into the card or read from the card into the Multiprogrammer. The direction of data flow is set by the level of CDE--a low level lets the Multiprogrammer write data to the card, and a high level lets it read data from the card. Although the transceivers are tri-state logic, jumper W23 establishes pin 9 at ground so that the isolated or high impedance state is never used.

4-59 Self Test Buffers

4-60 During the card test performed at power-on, Multiprogrammer writes several words of test data to card subaddress Write 0. The data is stored in the Self Test Buffer. The test data is stored in the buffer when STBO is pulsed high. The Multiprogrammer then reads the data from the buffer from subaddress Read 3. The buffer is enabled for reading when RTN3 is pulsed low.

4-61 Self-ID/Status Buffers

4-62 These buffers are also tri-state and their outputs are held in an open or isolated condition while the CRE control line is high. When a self-ID status operation is decoded from the control lines, CRE goes low and RTN3 is high. This connects the inputs of the self-ID/status buffers to the backplane data lines.

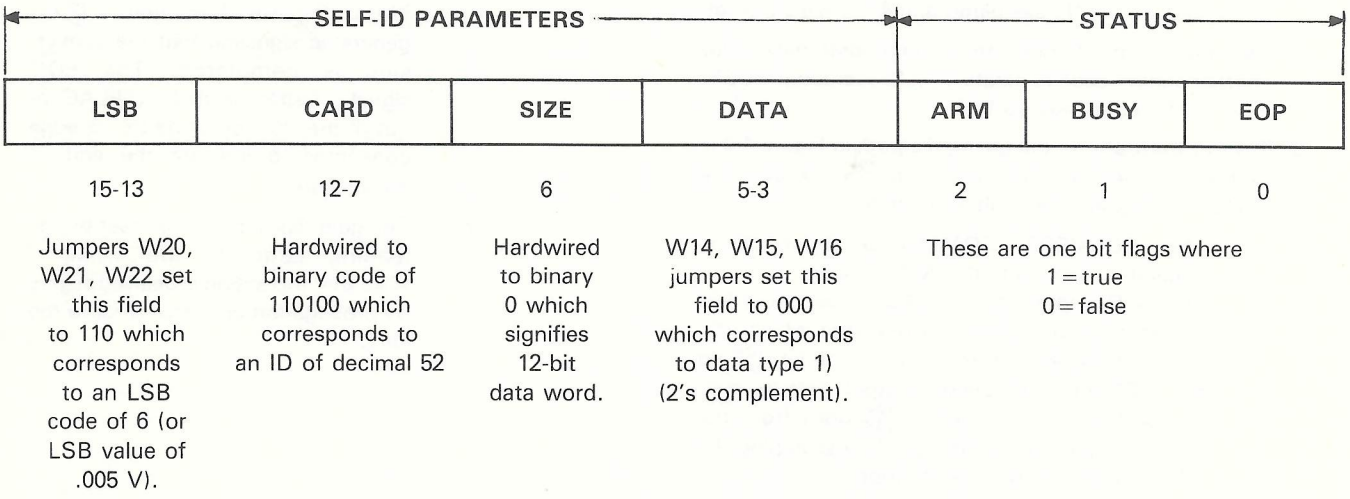
4-63 The 16-bits (B0-B15) are read back during self-test or when an RS instruction is programmed. During self-test, bits B3-B15 are stored in the Multiprogrammer memory while status bits B0-B2 are ignored. When a Read Status (RS) instruction is issued, status bits B0-B2 are stored in Multiprogrammer memory while bits B3-B15 are ignored.

4-64 The self-ID bits B3-B15 specify the "wake-up" values of the LSB, card ID, size, and data type parameters. The values of the parameters determine how the Multiprogrammer firmware will process the data it sends to or receives from the card. Status bits, B0-B2, are used by the Multiprogrammer to check the status of the card during operation. The status information is provided by UCC outputs, ARM, BSY, and EOP.

4-65 Note that the data type and LSB jumpers establish default entires that are stored during system initialization. These values are not necessarily the same values established by subsequent execution of a Set Format, SF instruction.

4-66 I/O Buffers and Schmitt Triggers

4-67 The I/O control signals are explained in detail in Section III. All of the signal lines are pulled-up to +5 V. The TPS input signal has a jumper option (W13) available which can tie the TPS input line low (see Table 3-6).



4-68 The 69751A can accept EXT TRIGGER signals that are either low true or high true. This feature simplifies interfacing with the external system when synchronization with that system is desired. In addition the trigger circuits on the 69751A offer a series of switch options which permit the UCC on the card to be bypassed for either positive or negative true external trigger inputs (see Table 3-6). Direct triggering of the analog subsystem on the card (trigger bypass mode) removes aperture uncertainties associated with the UCC and reduces the total trigger delay to less than 1μsec. The trigger bypass mode carries the penalty that internal triggering is disabled which effectively decouples control of data conversions and transfers from backplane commands (see paragraph 3-25).

4-69 The End-of-Conversion signal is available at the edge connector in its true (EOC) and complemented form($\overline{EOC}$). The EXTERNAL TRIGGER (EXT) signal is applied directly to the EXT input of the UCC chip and to switch S2. EXT and TPS are the only input control signals that can be applied to the edge connector. EOP, BUSY, EOC, and $\overline{EOC}$ are output signals.

4-70 PROCESSING AN INPUT PARALLEL (IP) INSTRUCTION

4-71 This discussion explains the processing of a typical input type instruction. Assume that an Input Parallel (IP) instruction issued by the controller which addresses a single A/D card in slot 2. The format of the controller instruction is...

"IP,2T"

4-72 When this instruction is executed, the following operations occur in the sequence indicated:

1. **Addressing the A/D Converter Card** - the slot position (slot 2) specified by the IP instruction is decoded and the CAD line to the A/D card goes high. In addition, the R/$\overline{W}$ lines, SAD0, $\overline{SAD1}$ lines, and the three-bit, control-code lines are decoded. The ARM and GAFF (Group Address F/F, see paragraph 4-12) flags are set.
2. **Cycling the card**- next, the Multiprogrammer sends another control code to initate a cycle operation. BUSY, and GATE commands go high.
3. **Timing Sequence** - the timing diagram in Figure 4-3 illustrates the events that follow once the GATE (1) signal goes high at T_1 time.
   a. The CONVERT COMMAND pulse (2) is generated and starts the A/D process.
   b. The A/D's internal clock (3) (2μsec nom.) is started triggering the clock one-shot which produces 0.5μsec (nom.) clock pulse (6) to shift (8) the 12-bit parallel output shift register.
   c. The A/D's STATUS signal (4) goes from the "Ready" state to the "Busy" state switching the S/H amplifier to the "hold" mode.

T_2: At this time, the first data bit B11 (MSB) is present at the A/D serial output (5) and is shifted into the 12-bit shift register input (9) on the trailing edge of the second clockpulse.

T_3 - T13: Data bits B10-B00 are shifted serially(one at-a-time) into the 12-bit parallel output shift register. The 12-bit register is comprised of 4-bit shift register U14 cascaded with 8-bit shift register U15. Register U14 is shifted on the trailing edge while register U15 is shifted on the leading edge of each clock/shift pulse (8).

At T^{13}, the leading edge of the 13th clock pulse shifts bits B11 (MSB) through B04 into their proper positions in the position of the 12-bit shift register.

Also, at T^{13}, the STATUS signal (4) goes from the "Busy" to the "Ready" state triggering the status one-shot (7) which holds the 13th clock/shift pulse (8) high from approximately 1μsec. The lengthened 13th clock pulse ensures that the last four bits (B03-B00) are shifted into the U14 position of the shift register (see T^{14}). The "Busy" to "Ready" STATUS transition also switches the S/H amplifier back to the "Sample" mode.

T_{14}: The status one-shot (7) terminates causing the following actions to take place simultaneously.

a. The data transfer is completed. Bits B03 through B00 (LSB) are shifted into their proper positions in the U14 portion of the 12-bit shift register on the trailing edge of the 13 clock/shift pulse (8). The shift register will retain this data until another conversion cycle is initiated.

b. The $\overline{EOC}$ pulse (1sec. nom.) (2) is generated signaling that the conversion is completed. The $\overline{EOC}$ signal is routed to the UCC FLAG input of the UCC chip and to the edge connector to indicate the end of conversion.

c. The gate flip-flop (1) is reset by the leading edge of the $\overline{FLAG}$. Note that this action is delayed slighty by propagation delays internal to the UCC

4. **End-of-Process and Interrupt Request** -When FLAG is returned, EOP goes high and BUSY and GATE are cleared. Since ARM is also high, a program interrupt request (IRQ)is sent to the Multiprogrammer.

5. **Clearing the UCC** - After servicing the interrupt request, the Multiprogrammer sends a clear control code. The storage registers are not affected, but the ARM, EOP, and GAFF are cleared by the clear control code.

6. **Reading the Data Word** - The Multiprogrammer sends the last control code to the card which places the contents of the Input Storage Register on the input data lines to the Multiprogrammer. The data word is then transferred to Multiprogrammer memory. Once the data word from an IP instruction has been read, additional Controller instructions can be issued at the controller to display the value.

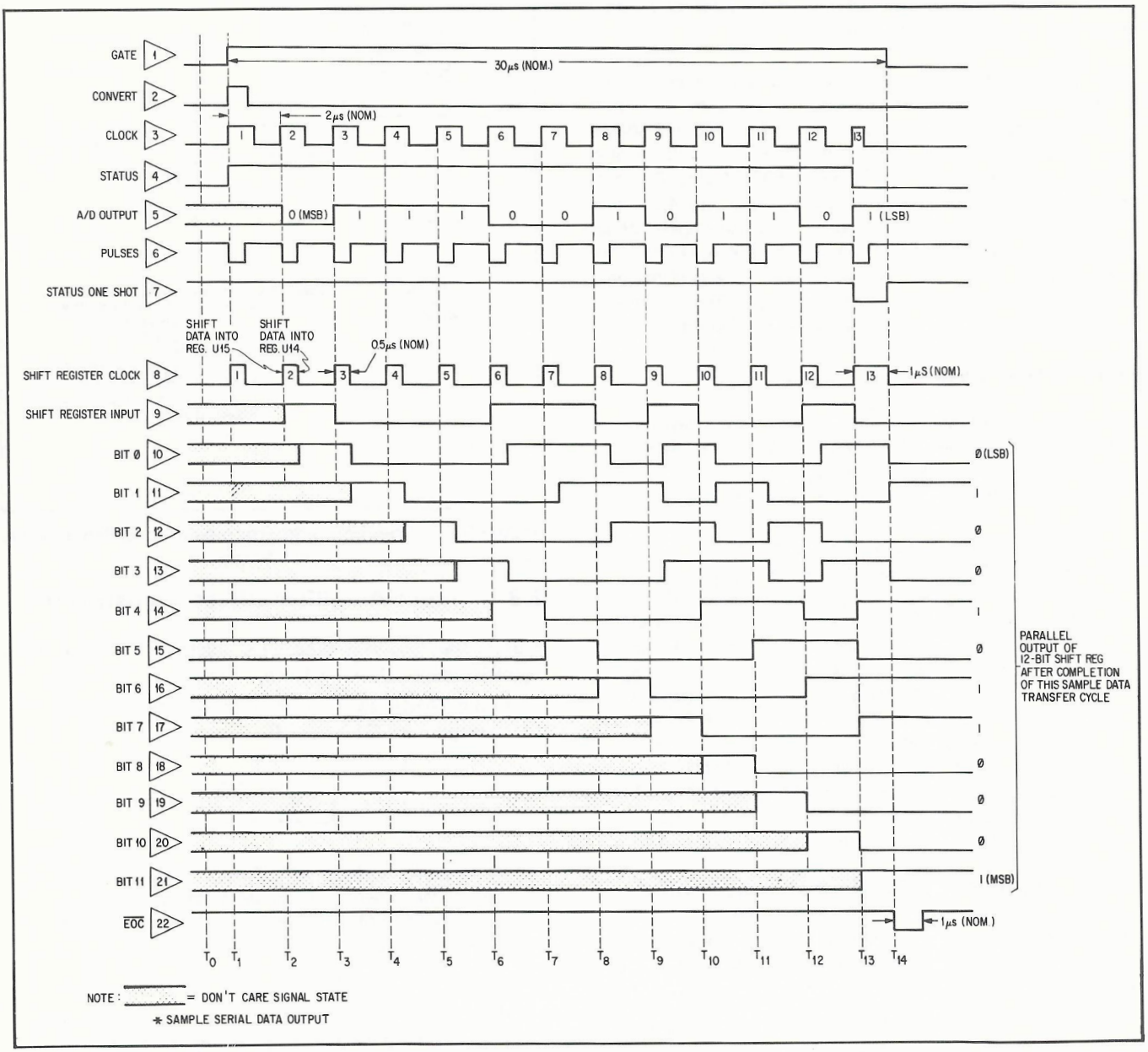


Figure 4-3. Data Transfer Timing Diagram

Section V
CALIBRATION PROCEDURES

5-1 INTRODUCTION

5-2 This section provides calibration procedures for the standard input and optional input ranges.

5-3 Calibration may be required if incorrect readings are obtained when performing the sample test program in Chapter 7 of the appropriate User's Guide. The calibration procedures must be performed after components are replaced in the analog input or A/D conversion circuits on the 69751A card. The procedures consists of adjusting the analog input amplifier offset and the A/D converter offset and gain. The input amplifier offset adjustment is performed first followed by the A/D converter adjustments. A procedure is also provided to adjust the gain of the input amplifier in the ± 100 mV range. The locations of the adjustment potentimeters are shown in Figure 7-1.

5-4 Test Setup (Figure 5-1)

5-5 Proper calibration requires the use of extremely sensitive and accurate instruments. The voltage source (e.g. HP 6131C) must be very stable and accurately set. Use the following test setup when performing the calibration procedures.

a. Plug extender card into slot 2 of 6942A.
b. Plug 69751A card into extender card.
c. Connect voltage source (e.g., HP 6131C Digital Voltage Source) to the 69751A card's analog input pins as shown in the Figure 5-1. Note that a precision attenuator is used to produce the ± 1 V and ± 100 mV test voltages. The output of a 6131C can be set by a controller (programmable calculator or computer) or by HP Pocket Programmer HP 14533B.
d. Connect 6942A to desktop computer (9825, 9835, or 9845) equipped with HP-IB Interface card (HP98034A).
e. Turn power on. Allow 30 minutes warm-up prior to performing the checkout or troubleshooting procedures.

5-6 Input Amplifier Offset Adjustment

5-7 The input amplifier offset adjustment consists of adjusting the output of amplifier stage U1 to precisely 0 V with 0 V (short circuit) applied to the card's analog input terminals. To adjust the offset of U1, proceed as follows:

a. Set RANGE switches on card for ± 100 mV input range (only S1-1 closed).
b. Short card's analog input terminals by connecting a jumper between edge connector pins J2-W and J2-Y.
c. Use DVM to measure output at U1-6 (TP1). Connect DVM common isolated common (J2-Y).
d. Adjust potentiomenter R2 for reading of 0.000 V ± 0.001 V on DVM.

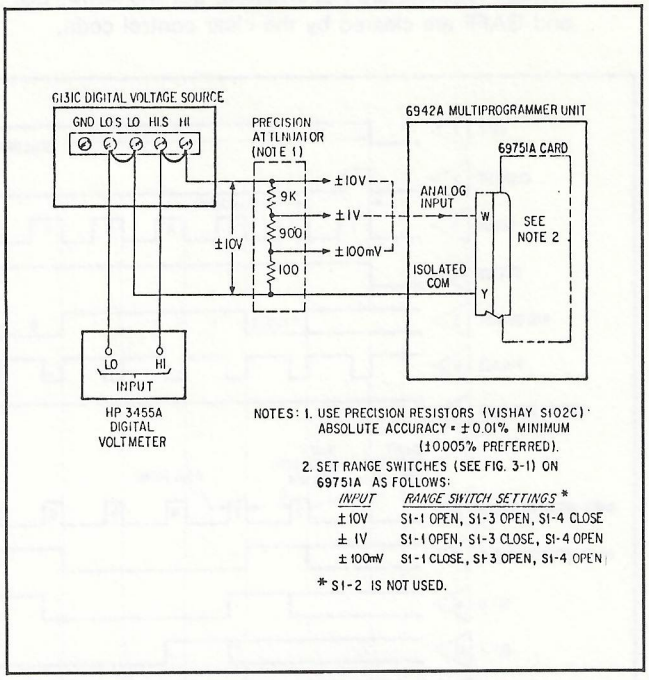


Figure 5-1. Checkout and Troubleshooting Procedures, Test Setup

5-8 Input Amplifier Offset Adjustment

5-9 The following procedure adjust the gain of input amplifier stage U1 in the 100 mV range.

a. Set RANGE switches on cards to ± 100 mV input range (only S1-1 closed).

CAUTION

Ensure that only ± 100 mV switch (S1-1) is closed. Potentiometer R14 may be damaged if it is turned fully CCW (0 ohms) and the ± 10 V switch S1-4 is also closed.

b. Connect test voltage (± 100 mV attenuator output, see test setup in Figure 5-1). Set voltage source output to precisely + 10.000 V. The precision attentuator will provide an input of + 0.1000 V to card.
c. Use DVM to measure output at U1-6 (TP1). Connect DMV common to isolated common (J2-Y).
d. Adjust postentiometer R14 for reading of − 10.000 V on DVM.

5-10 A/D Converter Offset and Gain Adjustments

5-11 These adjustments consist of adjusting the offset (maximum negative digital output) of the A/D converter. The A/D converter has a given digital output code for a small range of analog input signals (the nominal width of the range being one LSB). If properly adjusted, the converter will switch from one output code to the adjacent output code when the input signal (dc source voltage) is halfway between two. With the test voltage set at the halfway point, the potentiometer (offset or gain control) can be adjusted until the A/D converter output switches at just that point. By using this technique and a visual display of the A/D reading at the desktop controller, the offset and gain adjustments can be accurately performed.

5-12 Offset Adjustment. To adjust the offset (maximum negative output) of the A/D converter, proceed as follows:

a. Set RANGE switches on the card for ± V input range (only S1-4 closed).
b. Connect the test voltage (±10 V attenuator output, see testup in Figure 5-1). Set voltage source to precisely −10.2375 V.
c. Initiate continuous A/D conversions and display the voltage readings at the desktop computer by running the following program.
d. Observe the desktop computer display and adjust the offset control (R19) until the A/D value on the display is just switching from −10.235 V to −10.240 V.

9825

```
0: fxd 3;wrt 723;"IP2T"
1: red 72301;A;dsp A
2: gto 0
*5293
```

9835/45

```
10   OUTPUT 723;"IP2T"
20   ENTER 723.01;A
30   DISP A
40   GOTO 10
```

5-13 Gain Adjustment. To adjust the gain (maximum positive output) of the A/D converter, proceed as follows:

a. Repeat test described in paragraph 5-12 (steps a through c), except set the voltage source to precisely +10.2325 V.
b. Observe the desktop computer display and adjust the gain control (R18) until the voltage reading on the display is just switching from +10.230 V to +10.235.
c. Repeat the offset adjustment (paragraph 5-12, steps a through d) and steps a and b above until both adjustments are correct.
d. Turn off Multiprogrammer and voltage source. Remove test connections.

5-14 OPTIONAL INPUT VOLTAGE RANGES

5-15 Jumper options expand the 69751A A/D Converter Card's measurement capabilities to include the 16 optional ranges (8 bipolar and 8 unipolar) listed in Table 3-2.

5-16 As described in the previous sections of this manual, the card is shipped from the factory ready to take voltage measurements in any of the standard bipolar ranges (±100 mV, ±1 V, or ±10 V/ ±100 V). The card's range switches must be set to correspond with the applicable input.

5-17 To convert the 69751A card to measure voltages in any of the optional ranges, the range jumpers must be changed, A/D scaling resistor R16 replaced, and the card recalibrated. Table 3-2 lists the jumper connections, switch settings, resistor values, and LSB (minimum voltage step change) for each optional range. The physical and electrical locations of the range jumper options and resistor R16 are shown on the schematic (Figure 7-2) and jumper location diagram (Figure 7-1. Procedures for converting and calibrating the card to measure voltages in any of the optional ranges are provided in the following paragraphs.

5-18 ±50 mV, ±0.5 V/ ±50 V Biopolar Ranges

a. Connect range jumpers and set range switches for ±5 V input (see Table 3-2.)
b. Replace resistor R16 with a fixed film 121Ω, 1% 1/8 W resistor HP Part No. 0757-0403.
c. Use the test setup of Figure 5-1 except add a 10k resistor in the precision attenuator as shown in Figure 5-2.

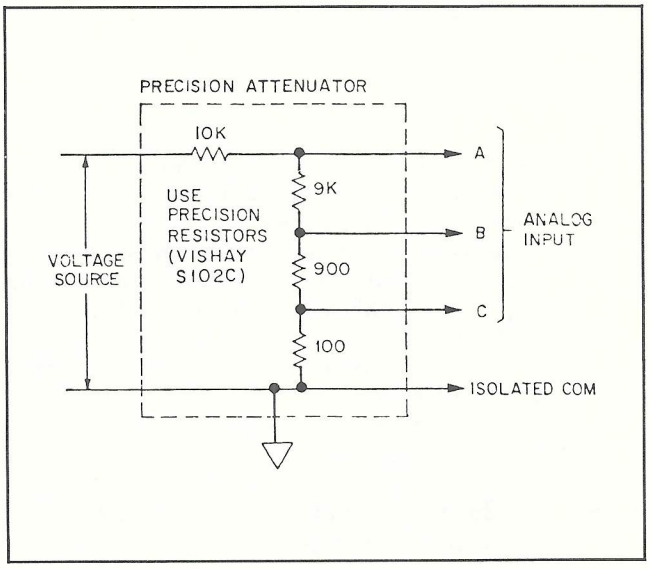


Figure 5-2. Precision Attenuator for ±5 V and 0 to +5 V Calibration

d. Perform the input amplifier adjustment procedures in paragraphs 5-6 through 5-9 except change step b in paragraph 5-9 to read Connect test voltage (precision attenuator output C) to the analog input of the 9751A card. Set voltage source to precisely 10.00 V. The precision attenuator will provide an analog input of 0.0500 V.

e. Adjust the A/D converter offset as follows:
   1. Set RANGE switches on the card for ±5 V input range (only S1-4 closed).
   2. Connect the test voltage (precision attenuator output A) to the analog input of the 69751A card. Set voltage source to precisely −10.2375 V. The precision attnuator will provide an analog input of −5.11875 V.
   3. Initiate continuous A/D conversions and display the voltage readings at the desktop computer by running the following program. Note that a Set Format (SF) instruction is used to set the LSB value to 2.5 millivolts so that the readings displayed will be in the 5,000 millivolt range.
   4. Observe the desktop computer display and adjust the offset control (R19) until the millivolts reading on the display is just switching from −5117.5 to −5120.0.

9825

```
0: wrt 723,"SF,2,3,1,2.5,12T"
1: fxd 3;wrt 723,"IP,2T"
2: red 72301,A;dsp A
3: gto 1
*12559
```

9835/45

```
10   OUTPUT 723;"SF,2,3,1,2.5,12T"
20   OUTPUT 723;"IP,2T"
30   ENTER 723.01;A
40   DISP A
50   GOTO 20
```

f. Adjust the A/D converter gain as follows:
   1. Repeat steps e1 through e3 above, except set the voltage source to precisely +5.11525 V.
   2. Observe the desktop computer display and adjust the gain control (R18) until the millivolts reading on the display is just switching from +5115.0 V to +5117.5 V.

g. Repeat the offset (step e) and gain (step f) adjustments until both are correct.

h. Turn of the Multiprogrammer and voltage source. Remove test connections.

5-19 ±25 mV, ±0.25 V, ±2.5 V/±25 V Bipolar Ranges

a. Connect range jumpers and set range switches for ±2.5 V input (See Table 3-2).

b. Replace resistor R16 with a fixed film 61.9Ω, 1%, 1/8 W resistor HP Part No. 0757-0276.

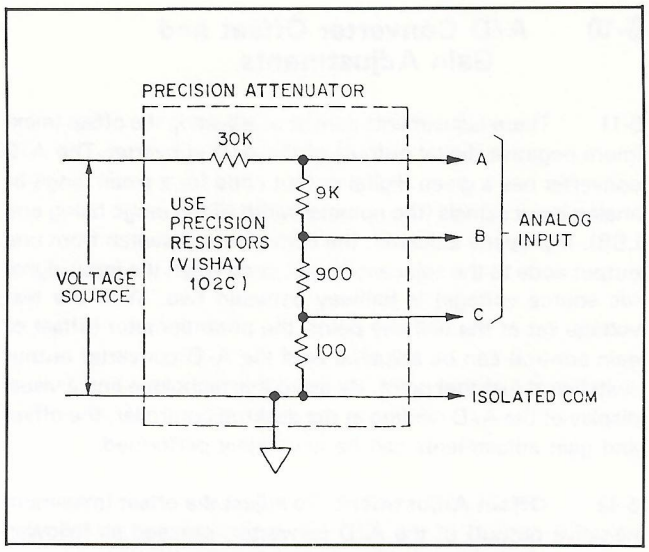


Figure 5-3. Precision Attenuator for ±2.5 V Calibration

c. Use the test setup of Figure 5-1 except add a 30k resistor to the precision attenuator as shown in Figure 5-3.

d. Perform the input amplifier adjustment procedures in paragraphs 5-6 through 5-9 except change step b in paragraph 5-9 to read: Connect test voltage (precision attenuator output C) to the analog input of the 69751A card. Set voltage source to precisely 10.00 V. The precision attenuator will provide an analog input of 0.0250 V.

e. Adjust the A/D converter offset as follows:
   1. Set RANGE switches on the card for ±2.5 V input range (only S1-4 closed).
   2. Connect the test voltage (precision attenuator output A) to the analog input of the 69751A card. Set voltage source to precisely −10.2375 V. The precision attenuator will provide an analog input of −2.559 V.
   3. Initiate continuous A/D conversions and display the voltage readings at the desktop computer by running the following program Note that a Set Format (SF) instruction is used to set the LSB value to 1.25 millivolts so that the readings displayed will be in the 2,500 millivolts range.

9825

```
0: wrt 723,"SF,2,3,1,1.25,12T"
1: fxd 3;wrt 723,"IP,2T"
2: red 72301,A;dsp A
3: gto 1
*11809
```

9835/45

```
10   OUTPUT 723;"SF,2,3,1,1.25,12T"
20   OUTPUT 723;"IP,2T"
30   ENTER 723.01;A
40   DISP A
50   GOTO 20
```

4. Observe the desktop computer display and adjust the offset control (R19) until the millivolts reading on the display is just switching from −2558.75 to −2560.00.

f. Adjust the A/D converter gain as follows
   1. Repeat steps e1 through e3 above, except set the voltage source to precisely +10.2325 V.
   2. Observe the desktop computer display and adjust the gain control (R18) until the millivolts reading on the display is just switching from +2557.50 V to +2558.75 V.

g. Repeat the offset (step e) and gain (step f) adjustments until both are correct.

h. Turn off the Multiprogrammer and voltage source. Remove test connections.

5-20 0 to +100 mV, 0 to +10 V/0 to +100 V Unipolar Ranges

a. Connect range jumpers and set range switches for 0 to +10 V input (see Table 3-2).

b. Replace resistor R16 with a fixed film 121Ω, 1%, 1/8 W resistor HP Part No. 0757-0403.

c. Use the Test setup of Figure 5-1 except change the voltage source and precision attenuator outputs to 0 to +10 V, 0 to +1 V, and 0 to +100 mV.

d. Perform the input amplifier adjustment procedures in paragraphs 5-6 through 5-9.

e. Perform the A/D converter zero adjustment as follows:
   1. Set RANGE switches on the card for 0 to +100 mV range (only S1-1 closed).
   2. Connect the test voltage (0 to 100 mV attenuator output) to the analog input of the 69751A cad. Set voltage source to precisely +0.125 V. The precision attenuator will provide an analog input of +0.00125 V.
   3. Initiate continuous A/D conversions and display the voltage readings at the desktop computer by running the following program. Becuase the dc input voltage is unipolar, an SF instruction sets the data type to unsigned binary (code 3). In addition, the LSB value is set to 2.5 millivolts.
   4. Observe the desktop computer display and adjust the offset control (R19) until the millivolts reading on the display is just switching from 0 to +2.5 V.

f. Adjust the A/D converter gain as follows:
   1. Repeat setps e1 through e3 above, except use the 0 to +10 V attenuator output, set Range switches for 0 to 10 V range (S1-4 closed), and set the voltage source to precisely +10.23625 V.
   2. Observe the desktop computer display and adjust the gain control (R18) until the millivolts reading on the display is just switching from +10235.0 to +10237.5 V.

g. Repeat the offset (step e) and gain (step f) adjustments until both are correct.

h. Turn off the Multiprogrammer and voltage source. Remove test connections.

9825

```
0: wrt 723,"SF,2,3,3,2.5,12T"
1: fxd 3;wrt 723,"IP,2T"
2: red 72301,A;dsp A
3: gto 1
*12437
```

9835/45

```
10    OUTPUT 723;"SF,2,3,3,2.5,12T"
20    OUTPUT 723;"IP,2T"
30    ENTER 723.01;A
40    DISP A
50    GOTO 20
```

5-21 0 to +50 mV, 0 to +0.5 V, to +5 V/0 to +50 V Unipolar Ranges

a. Connect range jumpers and set range switches for 0 to +5 V input (see Table 3-2).

b. Replace resistor R16 with a fixed film 61.9Ω, 1%, 1/8 resistor HP Part No. 0757-0276.

c. Use the test setup of Figure 5-1, except add a 10k resistor to the precision attenuator as shown in Figure 5-2.

d. Perform the input amplifier adjustment procedures in paragraphs 5-6 through 5-9 except change step b in paragraph 5-9 to read: Connect test voltage (precision attenuator output C) to the analog input of the 69751A card. Set voltage source to precisely 10.00 V. The precision attenuator will provide an analog input of 0.0500 V.

e. Perform the A/D converter zero adjustments as follows:
   1. Set RANGE switches on the card to 0 to +50 mV range (only S1-1 closed).
   2. Connect the test voltage (precision attenuator output C) to the analog input of the 69751A card. Set voltage source to precisely +0.125 V. The precision attenuator will provide an analog input of +0.000625 V.
   3. Initiate continuous A/D conversions and display the voltage readings at the desktop computer by running the following program. Because the dc input voltage is unipolar, an SF instruction sets the data type to unsigned binary (code 3). In addition, the LSB value is set to 1.25 millivolts.
   4. Observe the desktop computer display and adjust the offset control (R19) until the millivolts reading on the display is just switching from 0 to 1.25 V.

9825

```
0: wrt 723,"SF,2,3,3,1.25,12T"
1: fxd 3;wrt 723,"IP,2T"
2: red 72301,A;dsp A
3: gto 1
*11687
```

9835/45

```
10   OUTPUT 723;"SF,2,3,3,1.25,12T"
20   OUTPUT 723;"IP,2T"
30   ENTER 723.01;A
40   DISP A
50   GOTO 20
```

f. Adjust the A/D converter gain as follows:
   1. Repeat steps e1 through e3 above, except use the 0 to +10 V attenuator output, set Range switches for 0 to 5 V range (S1-4 closed), and set the voltage source to precisely +10.23625 V.
   2. Observe the desktop computer display and adjust the gain control (R18) until the millivolts reading on the display is just switching from +5117.5 V to +5118.75 V.

g. Repeat the offset (step e) and gain (step f) adjustments until both are correct.

h. Turn off the Multiprogrammer and voltage source. Remove test connections.

Section VI
PARTS LIST

6-1 INTRODUCTION

6-2 This section contains information on ordering replacement parts for the Analog-To-Digital Converter Card, Model 69751A. Table 6-1 lists the electrical and mechanical components of the card. Table 6-2 lists the parts comprising the external I/O connector assembly supplied with the card. Figure 6-1 illustrates how the parts in Table 6-2 are assembled.

6-3 HOW TO ORDER PARTS

6-4 You can order parts from your local Hewlett-Packard sales office. Refer to the list of sales offices at the end of this manual for the office nearest you. When ordering parts include the following information:

a. the Hewlett-Packard part number.
b. a description of the part.
c. the quantity desired.
d. the model number of the card (69751A) on which the part is used.

6-5 If you wish to order a part directly from the manufacturer, locate the manufacturer's address listed below.

Manufacturer's Federal Supply Codes

Code	Manufacturer	Address
01121	Allen-Bradley Co.	Milaukee, WI
01295	Texas Instruments, Inc. Semiconductor-Components Division	Dallas, TX
03508	General Electric Co. Semiconductor Products Department	Auburn, NY
04713	Motorola Semiconductor Products, Inc.	Phoenix, AZ
06665	Precision Monolithics, Inc.	Santa Clara, CA
19701	Mepco/Electra Corp.	Mineral Wells, TX
24546	Corning Glass Works	Bradford, PA
27014	National Semiconductor Corp.	Santa Clara, CA
28480	Hewlett-Packard Co.	Palo Alto, CA
3L585	RCA Corp. Solid State Division	Somerville, NJ
56289	Sprague Electric Co.	North Adams, MA
8E175	Burr Brown Co	Tucson, AZ

Table 6-1. 69751A Parts List

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
C1	0160-0205	1	fxd mica 10pf +-5% 500Vdc	28480	
C2,3	0160-0263	4	fxd cer 0.22uf +-20% 50Vdc	28480	
C4	0160-0127	4	fxd cer 1uf +-20% 25Vdc	28480	
C5	0160-0263		fxd cer 0.22uf +-20% 50Vdc	28480	
C6,7	0180-0116	5	fxd elect TA 6.8uf +-10% 35V	56289	150D685X9035B2
C8	0160-4888	1	fxd cer 2400pf +-10% 160Vdc	28480	
C9	0160-0127		fxd cer 1uf +-20% 25Vdc	28480	
C10	0150-0050	2	fxd cer 1000pf +80-20% 1KVdc	28480	
C11	0160-4722	13	fxd cer 0.1uf +80-20% 50Vdc	28480	
C12,13	0180-0116		fxd elect TA 6.8uf +-10% 35V	56289	150D685X9035B2
C14	0160-0127		fxd cer 1uf +-20% 25Vdc	28480	
C15	0160-0263		fxd cer 0.22uf +-20% 50Vdc	28480	
C16	0160-0127		fxd cer 1uf +-20% 25Vdc	28480	
C17	0180-0116		fxd elect TA 6.8uf +-10% 35V	56289	150D685X9035B2
C18	0180-0228	1	fxd elect TA 22uf +-10% 15V	56289	150D226X9015B2
C19-22	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C23,24	0160-0990	4	fxd mica 100pf +-2% 300Vdc	28480	
C25	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C26,27	0160-0990		fxd mica 100pf +-2% 300Vdc	28480	
C28	0150-0050		fxd cer 1000pf +80-20% 1KVdc	28480	
C29-35	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C36-38	0180-0155	3	fxd elect TA 2.2uf +-20% 20V	56289	150D225X0020A2
CR1,2	1901-0586	2	gen prp 30V 250mA	28480	
Q1-4	1854-0477	4	NPN SI	04713	2N2222A
R1	0757-0442	1	fxd film 10K 1% 1/8W	24546	C4-1/8-T0-1002-F
R2	2100-3773	1	trmr 100K 10% 17-turn	28480	
R3	0699-0297	1	fxd film 9M 0.1% 3/4W	28480	
R4	0699-0296	1	fxd film 1M 0.1% 3/4W	28480	
R5	0699-0291	1	fxd film 101 0.1% 0.225W	28480	
R6	0699-0292	1	fxd film 900 .01% 0.15W	28480	
R7	0699-0293	1	fxd film 9K 0.1% 0.15W	24546	
R8	0757-0280	2	fxd film 1K 1% 1/8W	24546	C4-1/8-T0-1001-F
R9	0757-0288	1	fxd film 9.09K 1% 1/8W	19701	MF4C1/8-T0-9091F
R10	0757-0464	1	fxd film 90.9K 1% 1/8W	24546	C4-1/8-T0-9092FF
R11,12	0698-3455	2	fxd film 261K 1% 1/8W	24546	C4-1/8-T0-2613-F
R13	0757-0435	1	fxd film 3.92K 1% 1/8W	24546	C4-1/8-T0-3921-F
R14	2100-3779	1	trmr 20K 10% 17-turn	01121	64P203
R15	0757-0280		fxd film 1K 1% 1/8W	24546	C4-1/8-T0-1001-F
R16	0757-0408	1	fxd film 243 1% 1/8W	24546	C4-1/8-T0-243R-F
R17	0683-5125	17	fxd comp 5.1K 5% 1/4W	01121	CB5125
R18,19	2100-0558	2	trmr 20K 10% 1-turn	28480	
R20,21	0757-0472	2	fxd film 200K 1% 1/8W	24546	C4-1/8-T0-2003-F
R22	0757-0449	2	fxd film 20K 1% 1/8W	24546	C4-1/8-T0-2002-F
R23	0683-1035	6	fxd comp 10K 5% 1/4W	01121	CB1035
R24	0683-3315	3	fxd comp 330 5% 1/4W	01121	CB3315
R25	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R26	0683-3315		fxd comp 330 5% 1/4W	01121	CB3315
R27	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R28	0683-3315		fxd comp 330 5% 1/4W	01121	CB3315
R29	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R30	0683-3915	1	fxd comp 390 5% 1/4W	01121	CB3915
R31	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R32-34	0683-1025		fxd comp 1K 5% 1/4W	01121	CB1025
R35	0689-5105	1	fxd comp 51 5% 1W	01121	GB5105
R36,37	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R38	0757-0446	2	fxd film 15K 1% 1/8W	24546	C4-1/8-T0-1502-F
R39	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R40	0698-3498	1	fxd film 8.66K 1% 1/8W	24546	C4-1/8-T0-866R-F
R41,42	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R43	0683-2015	1	fxd comp 200 5% 1/4W	01121	CB2015
R44	0757-0449		fxd film 20K 1% 1/8W	24546	C4-1/8-T0-2002-F
R45	0757-0446		fxd film 15K 1% 1/8W	24546	C4-1/8-T0-1502-F
R46-49	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125

Table 6-1. 69751A Parts List (cont.)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
R50,51	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R52-56	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R57	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R58	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
S1,2	3101-2368	2	SWITCH	28480	
U1	1826-0576	1	IC OP AMP PRCN	06665	OP-16E
U2	1826-0281	1	IC VOLTAGE REGULATOR	04713	MC79L15ACP
U3	1826-0274	1	IC VOLTAGE REGULATOR	04713	MC78L15ACP
U4	1826-0619	1	IC SMPL/HOLD	28480	
U5	1813-0098	1	IC A/D CONVERTER	8E175	ADC80AG-12
U6	1826-0528	1	IC OP AMP	27014	LF356BH
U7	1820-1199	1	IC INV TTL LS HEX	01295	SN74LS04N
U8,9	1990-0429	2	IC OPTO-ISOLATOR LED-IC GATE	28480	
U10	1990-0461	1	IC OPTO-ISOLATOR LED-IC GATE	28480	5082-4364
U11	1826-0144	1	IC VOLTAGE REGULATOR	04713	MC7805CP
U12,13	1820-1641	2	IC DRVR TTL LS BUS DRVR HEX	01295	SN74LS365AN
U14	1820-1446	1	IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS395AN
U15	1820-1433	1	IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT	01295	SN74LS164N
U16	1820-1197	1	IC GATE TTL LS NAND QUAD	01295	SN74LS00N
U17	1820-1437	2	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U18-20	1820-1544	7	IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U21	1820-1437		IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U22-24	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U25	1820-1198	1	IC GATE TTL LS NAND QUAD	01295	SN74LS03N
U26	1820-1416	1	IC SCHMITT TRIGGER TTL LS INV HEX	01295	SN74LS14N
U27,28	1820-2257	3	IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U29	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U30	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U31,32	1820-2239	2	IC DRVR TTL S BUS	27014	DP8304BN
U33	1820-2302	1	IC CONTROL CHIP	28480	

MECHANICAL PARTS

HP Part No	Qty	Description	Mfr Code
69751-80001	1	CARD EXTRACTOR	28480
1480-0059	1	..PIN ROLL (.062 IN.)	28480
69751-90003	1	MANUAL, OPERATION	28480
1200-0552	1	SOCKET-IC 40 CONTACT (U33)	28480
1200-0811	1	SOCKET-16 PIN (U5)	28480
5060-2806	1	EXTERNAL EDGE CONNECTOR ASSEMBLY	28480
9211-4189	1	SHIPPING CARTON	28480
9222-0665	1	STATIC FREE BAG	28480

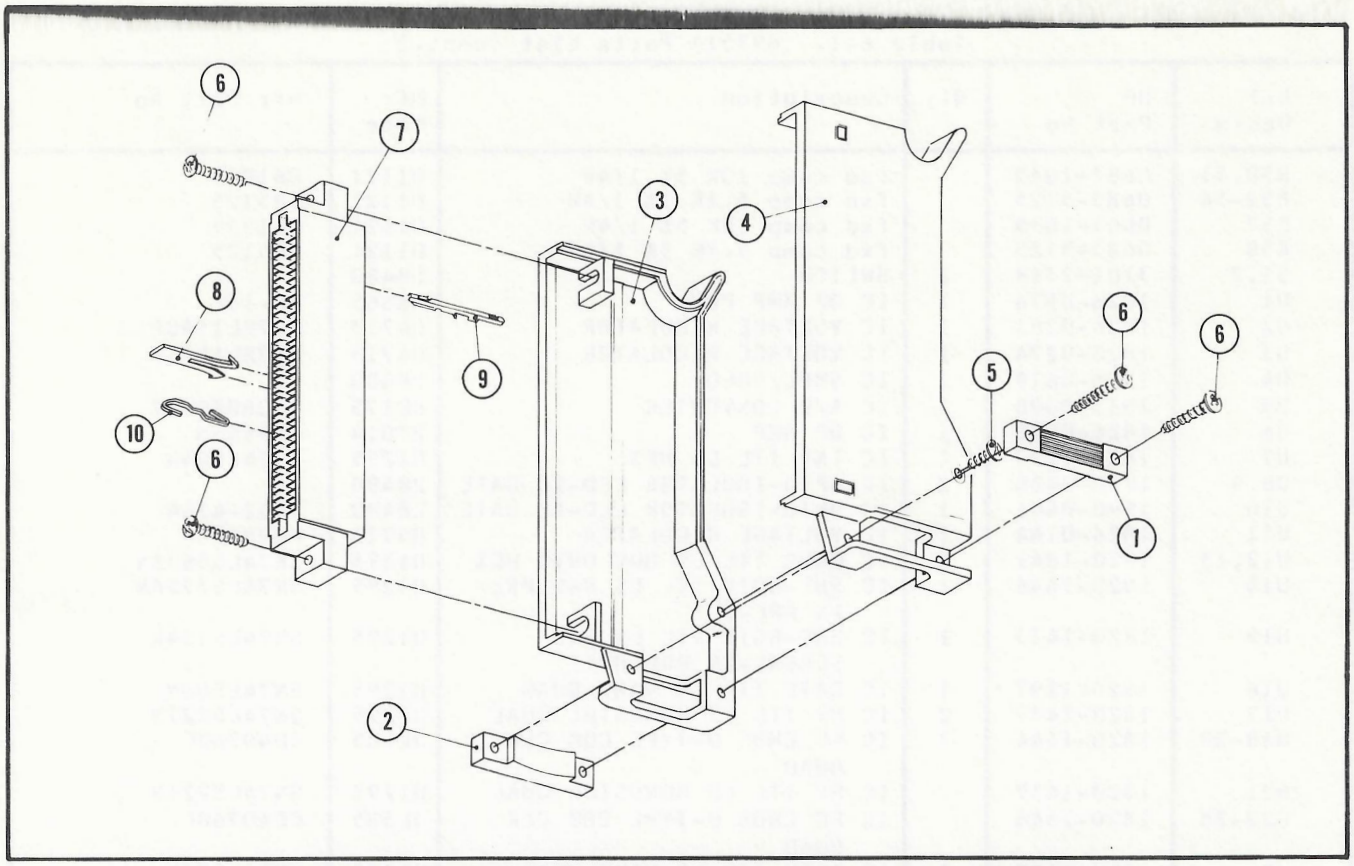


Figure 6-1. External Edge Connector Assembly, (HP P/N 5060-2806)

Table 6-2. Parts List for External Connector Assembly* (HP Part No. 5060-2806)

HP Part No	Index No	Description	Qty
1251-6307		HOOD ASSEMBLY**	
	1	**STRAIN RELIEF	
	2	**CABLE CLAMPS	
	3	**RIGHT HOOD ASSEMBLY	
	4	**LEFT HOOD ASSEMBLY	
	5	**SCREW, 7/16 INCH	
	6	**SCREWS, 11/16 INCH	
1251-6059	7	CONNECTOR PIN HOUSING	1
1251-6056	8	CONNECTOR KEY	1
1251-6183	9	SOLDER PINS, PLATED	45
1251-6380	10	SPRINGS, RETAINING	6

* CAN BE ORDERED AS MODEL 14703A, CARD EDGE CONNECTOR
** ITEM 1251-6307 CONSISTS OF INDEX ITEMS 1 THROUGH 6.

Section VII
DIAGRAMS

7-1 COMPONENT LOCATION

7-2 Figure 7-1 shows the Analog-To-Digital Converter card and identifies the various test points shown in the functional schematic diagram, Figure 7-2, and the jumper locations described in Section III.

7-3 SCHEMATIC DIAGRAM

7-4 The schematic diagram of the A/D card is given in Figure 7-2. The schematic diagram uses the ANSI Y32.14 and IEEE standard 91 for the representation of logic elements. A brief summary of this notation is given in Table 7-1.

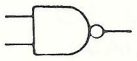
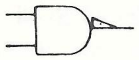
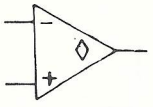
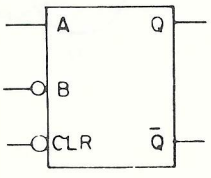
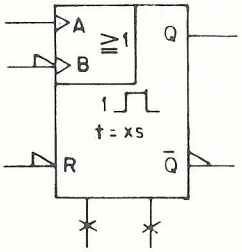
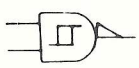
Table 7-1. Abbreviated List of ANSI Y32.14 Schematic Symbols

Definitions

High = more positive
Low = less positive

Indicator and Qualifier Symbols

≧	OR function
▱	(polarity indicator, shown outside logic symbol) Any marked input or output is active low; any unmarked input or output is active high.
⊳	(dynamic indicator) Any marked input is edge triggered, ie, active during transition between states; any unmarked input is level sensitive.
⊓	(Schmitt trigger) indicates that hysteresis exists in device.
*	(non-logic indicator) Any marked input or output does not carry logic information.
◊	open-collector or open emitter output
1⊓	monostable (one-shot) multivibrator
t= xSec	indicates pulse width (usually determined by external RC network)
G	gate input (a number following G indicates which inputs are gated)
C	control input (clock)
R	reset (clear)
S	set

OLD SYMBOL	*NEW SYMBOL*	*NOTES*
		
		Output requires external components to achieve logic state
		A positive-going transition at A or a negative-going transition at B triggers the one-shot. External timing components connect to non-logic inputs.
		Output changes state rapidly regardless of input rate of change.

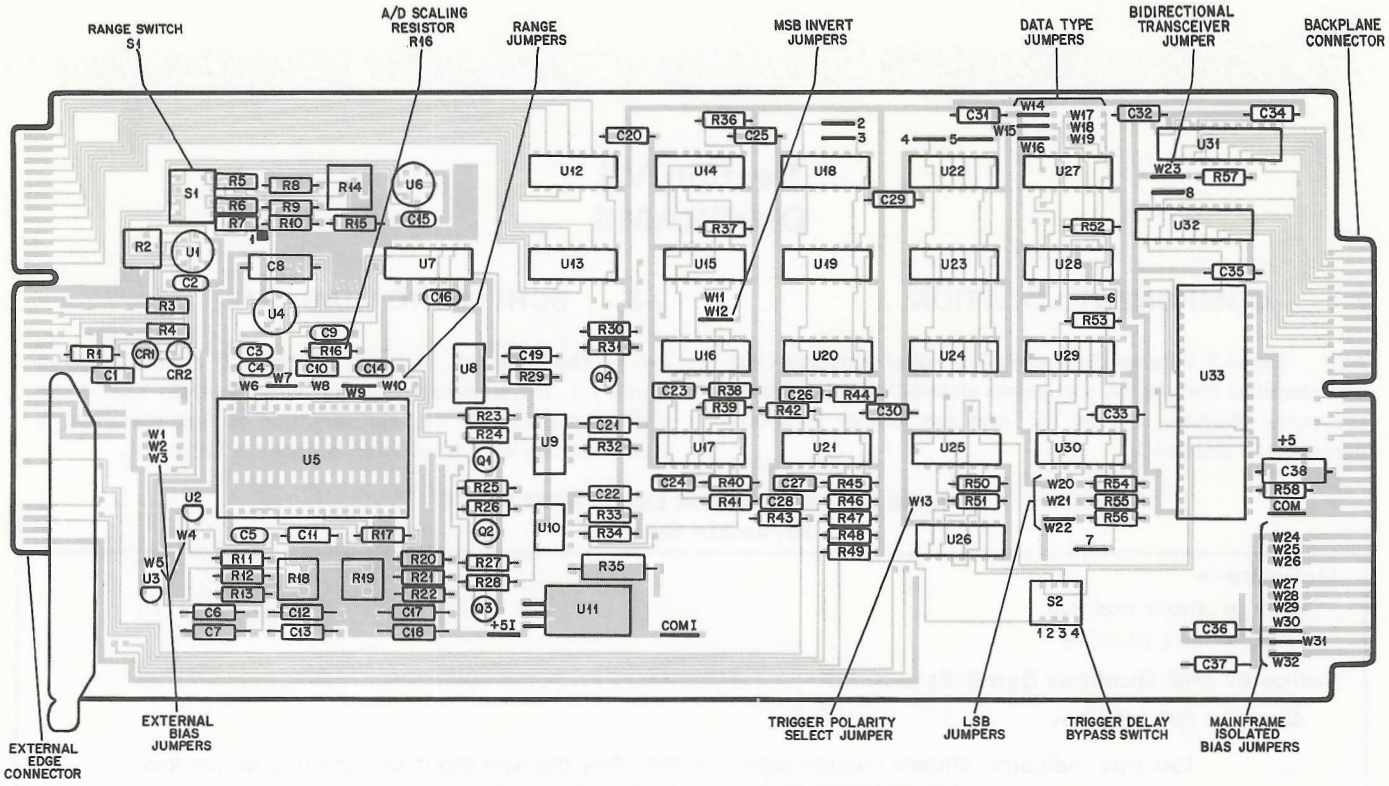


Figure 7-1. 69751A Component Location Diagram

NOTES

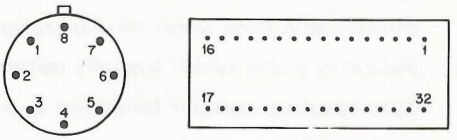
1. ALL RESISTORS ARE IN OHMS, ±5%, 1/4W UNLESS OTHERWISE INDICATED. ALL CAPACITORS ARE 50V AND IN MICROFARADS UNLESS OTHERWISE INDICATED.

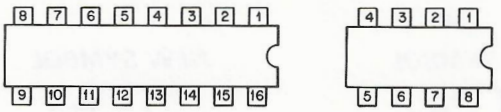
2. FOR INPUTS IN THE ±100V RANGE:
   a. CONNECT INPUT VOLTAGE TO J2-15 (÷ ATTENUATOR INPUT).
   b. CONNECT A JUMPER BETWEEN J2-17 (÷10 ATTENUATOR OUTPUT) AND J2-19 (ANALOG INPUT)
   c. THEN CLOSE THE ±10V RANGE SWITCH.

3. RANGE SWITCHES MUST BE SET TO CORRESPOND WITH ANALOG INPUT (REFER TO SECTION III OF MANUAL FOR DETAILS).

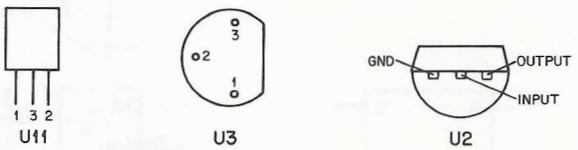
4. IF EXTERNAL +18V SUPPLY VOLTAGES ARE TO BE USED INSTEAD OF THE VOLTAGES FROM THE BACKPLANE (CONNECTOR) P1, REMOVE JUMPERS W30, W31, W32.

5. PIN LOCATIONS FOR INTEGRATED CIRCUITS ARE AS FOLLOWS:

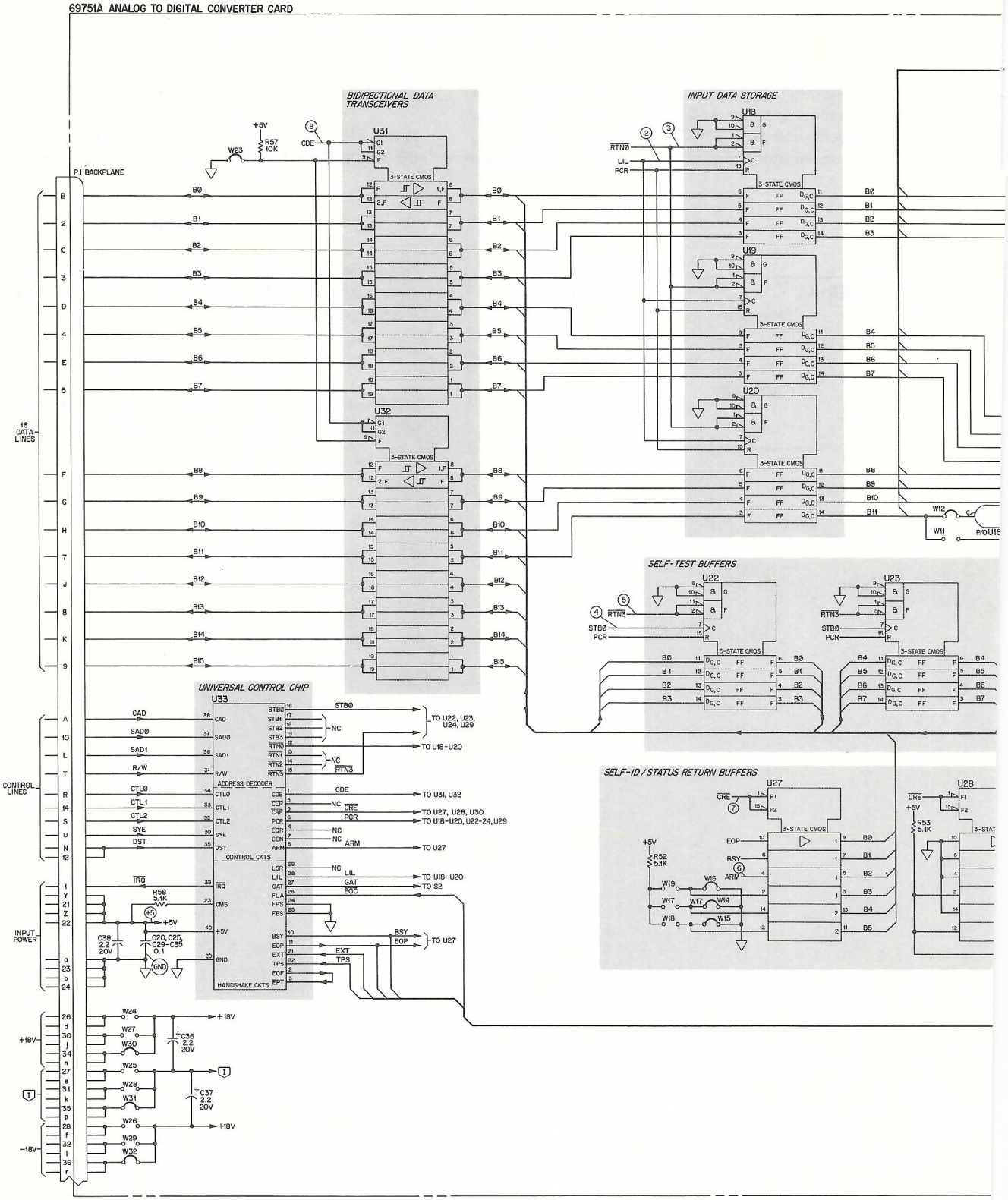




(TOP VIEWS)



(BOTTOM VIEWS)


69751A ANALOG TO DIGITAL CONVERTER CARD
BIDIRECTIONAL DATA TRANSCEIVERS
INPUT DATA STORAGE
SELF-TEST BUFFERS
SELF-ID/STATUS RETURN BUFFERS
UNIVERSAL CONTROL CHIP
P1 BACKPLANE
16 DATA LINES
CONTROL LINES
INPUT POWER
3-STATE CMOS
ADDRESS DECODER
CONTROL CKTS
HANDSHAKE CKTS
U31
U32
U33
U18
U19
U20
U22
U23
U27
U28
CDE
CRE
PCR
ARM
EOP
BSY
EXT
TPS
LIL
GAT
EOC
IRQ
CMS
CAD
SAD0
SAD1
R/W
CTL0
CTL1
CTL2
SYE
DST
LSR
FLA
FPS
FES
EDF
EPT
CLR
TO U22, U23, U24, U29
TO U18-U20
TO U31, U32
TO U27, U28, U30
TO U18-U20, U22-24, U29
TO U27
TO U18-U20
TO S2
TO U27
+5V
+18V
-18V
R57 10K
R58 5.1K
R52 5.1K
R53 5.1K
C38 2.2 20V
C20, C25, C29-C35 0.1
C36 2.2 20V
C37 2.2 20V
W23
W24
W25
W26
W27
W28
W29
W30
W31
W32
W11
W12
W14
W15
W16
W17
W18
W19

Appendix A
MANUAL BACKDATING CHANGES

A-1 This appendix describes changes that must be made to adapt this manual to earlier A/D cards. To adapt this manual to serial numbers prior to 2029A-0461, inspect the following table for your serial number and then make the appropriate changes.

SERIAL Prefix	SERIAL Number	MAKE CHANGES
2021A	0341-0460	1,2
1912A	0101-0340	2,3

CHANGE 1

In parts list and on the schematic, change capacitors C2, C3, C5, and C15 to 1μF, 50 V, HP Part No. 0160-3490, qty 4.

CHANGE 2

For proper operation of the input guard on cards with serial numbers below 2029A, connect a jumper between pins 16 and T on edge connector J2.

CHANGE 3

In parts list and on the schematic, change capacitors C2, C3, C5, and C15 to 1μF, 25 V, HP Part No. 0160-0127.

MANUAL CHANGES
Model 69751A Analog-to-Digital Converter Card
Manual HP Part No. 69751-90003

Make all corrections in the manual according to errata below, then check the following table for your card's serial number and enter any listed change(s) in the manual.

SERIAL		MAKE
Prefix	Number	CHANGES
ALL 2347A	04081-up	Errata 1

ERRATA:

In paragraph 1-13, on page 1-3, change Digital Input to A/D.

In Table 2-1, on page 2-1, the isolated bias supply for jumpers W24, 25, and 26 is Isolated Bias No. 3 (200mA).

In paragraph 2-16, on page 2-2, change 69755A Counter/Totalizer to 69775A Counter/Totalizer.

In Table 3-1, on page 3-1, change the LSB of the ±100mV range to .05mV. Add four asterisks after the .005 V entry in the LSB column. Change the ±100mV input voltage range to read: (+102.35 to -102.4mV).

In Table 3-2, on page 3-2, change the negative voltage limit of the ±5V range from -51220.0mV to -5120.0mV.

On page 4-6, under SELF-ID PARAMETERS, change CARD to CARD ID and DATA to DATA TYPE.

Correct Section V as follows:

Change 5-8 to read: "100mV Range Adjustment."

Change 5-9d to read: "Adjust potentiometer R14 for a reading of +10.000 V on DVM."

Change 5-12a to read: "Set RANGE switches on the card for ±10 V input range (only S1-4 closed)."

Add the following sentence to the end of 5-18d: "Adjust R14 for 5.000 V exactly."

Change 5-18f1 to read: "Repeat steps e1 through e3 above, except set the voltage source to precisely +10.2325 V. This provides an analog input of +5.11625 V."

Add the following sentence to the end of 5-19d: "Adjust R14 for 2.500 V exactly."

In 5-19e2, change -2.559 V to -2.559375V.

In 5-20e4, change +2.5 V to +2.5 mV.

In 5-20f2, change +10237.5V to +10237.5mV

In 5-21e4, change 1.25 V to 1.25 mV.

CHANGE 1:

The card edge connector has been changed to reduce EMI/RFI interference. When assembling the card edge connector, refer to the assembly instruction sheet (HP P/N 14703-90001) that is shipped with the connector. Disregard the assembly information in the back of this manual.

11/3/83

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