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HEWLETT PACKARD

INTERRUPT CARD
MODEL 69776A

OPERATING MANUAL
FOR SERIAL NUMBERS 1917A-00101
AND ABOVE.

For cards with serial prefixes above 1917A-00101, a manual change page may be included.

Manual Part No. 69776-90003
Microfiche Part No. 69776-90004

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Section I
GENERAL INFORMATION

1-1 SCOPE OF MANUAL

1-2 This manual covers the installation, pre-operation, and theory of operation for the Interrupt card Model 69776A. This manual does not include servicing instructions nor information on the programming of the card. Programming examples of the Interrupt card are shown in Chapter 7 of the 6942A Multiprogrammer User's Guide. Additional documents that contain general information on I/O cards are:

- 6942A Multiprogrammer User's Guide for HP 9825/35/45 Controllers (HP 06942-90003).
- 6942A Multiprogrammer User's Guide for HP 85 Controllers (HP 9826 Controllers (HP 06942-90013).
- 6942A Multiprogrammer Technical Data (HP 5952-4034).
- 6942A Multiprogrammer Installation and Assembly Level Service Manual (HP 06942-90006).

1-3 Any of these documents can be ordered directly from your local Hewlett-Packard sales office. Give the applicable HP manual part number as indicated above.

1-4 DESCRIPTION

1-5 The Interrupt card compares a programmed 16-bit reference word with an input word applied to its external edge connector and generates an interrupt when a predetermined relationship exists between them. Four interrupt modes can be programmed; the interrupt can occur when the input word becomes unequal to, equal to, greater than, or less than the reference word. One or more bits can be removed from the comparison, if desired, by sending a mask word to the card.

1-6 The reference word is written to the card's subaddress Ø in decimal form and must be an integer value between Ø and 65535. The interrupt mode is selected by writing a data value to subaddress 1. Octal data values of 1, 2, 4, or 10, respectively, select a mode in which an interrupt occurs when the input word is "not equal to", "equal to", greater than", or "less than" the reference word. A mask word written to subaddress 2 removes selected bits from or restores them to the comparison made between the input and reference words. To ease the visualization of the bits to be masked, the mask word is an octal integer between 0 and 1777777. Those mask bits set to Ø allow the corresponding bits of the input and reference words to be compared, and those set to 1 remove the corresponding bits from the comparison. At turn-on and until the value is reprogrammed, the mask register contains the value Ø, which causes all 16 bits to be included in the comparison.

1-7 Once the reference word, interrupt mode, and optional mask word have been programmed, either a programmed instruction or an External Trigger signal can be used to cycle the card, enabling it to begin a new comparison. When the comparison condition is satisfied, an armed 69776A card interrupts the microprocessor and stores the input word that caused the interrupt. A controller interrupt may or may not be generated, depending on the system operating mode and the specific instruction used.

1-8 After the card has interrupted, the word that caused the interrupt can be read back using subaddress Ø. The most recent interrupt word is always available for readback from the card. As many as 1339 interrupt words can be stored at one time in mainframe memory. These can be read back from the HP-IB extended talk address associated with the instruction that initiated the data inputs. The input word currently present at the edge connector can be read using subaddress 1 at any time. The programmed mask word can be read back using subaddress 2, and the programmed reference word can be read back using subaddress 3.

NOTE

Note that the reference word is written to subaddress Ø, but that it is read back using subaddress 3. Also note that while the data value that selects the interrupt mode is written to subaddress 1, the data read back using subaddress 1 is the word currently present at the input terminals.

1-9 To filter out noise, a digital filter on the card ignores all interrupts lasting less than 6 μs. To filter noise of longer duration, such as contact bounce, the filter delay time can be set between 5 μs and one second by changing components on the card. (Refer to Section III, paragraph 3-23.)

1-10 The Interrupt card can be used to detect alarm or error conditions in digital circuits, and if a 69771A Digtial Input/Analog Comparator card or a 69751A Analog-to-Digital Converter card is connected as a signal conditioner for the Interrupt card, it can be used to interrupt the controller when analog signals exceed or fall below programmed limits.

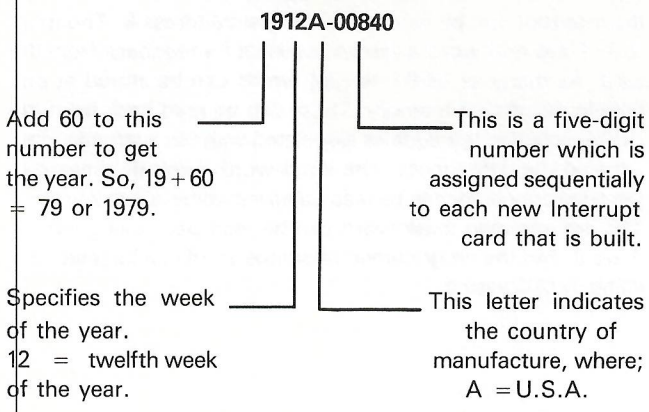
1-11 As many as 16 Interrupt cards may be used in a single mainframe.

1-12 SPECIFICATIONS

1-13 Specifications and other supplemental data for the Interrupt card are given in Table 1-1.

1-14 CARD AND MANUAL IDENTIFICATION

1-15 Hewlett-Packard I/O cards are identified by a two-part serial number, for example, 1912A-00840. This number appears on a label affixed to the component side of the circuit card. The breakdown of the serial number is explained using the example number 1912A-00840.



1-16 The first part of this serial number (year and week) indicates the last date when a significant design change was made.

1-17 Each I/O card is equipped with a handle that is marked to identify the card type (e.g. Interrupt card). The handle is located at the card's outer edge and facilitates the removal and installation of the card.

1-18 OPTIONS

1-19 To obtain additional Operating Manuals when the Interrupt card is shipped, request Option 910 when ordering the card. One additional manual will be shipped with each Option 910 ordered.

1-20 ACCESSORIES

1-21 One external connector is shipped with each I/O card. Order Model 14703A when extra connectors are required to fabricate cables for several different applications.

1-22 A deinsertion tool is available to remove the contacts from the connector. This tool can be ordered from Hewlett-Packard (HP P/N 8710-0690).

Table 1-1. Specifications and Supplemental Data

DIGITAL INPUTS:
Inputs are positive-true with 10 kΩ pull-up resistors to + volts.
A logical 1 = 2.0 V to 5.25 V
A logical 0 = 0.0 V to 0.5 V
(An additional complemented bit 15 input terminal at J2-16 makes it possible to use the card with a two's complement input word.)

DIGITAL FILTER DELAY TIME:
The card ignores all interrupts lasting less than 6 μs and responds to those lasting longer than 9 μs. Its 7.5 ±1.5 μs filter time can be varied between 5 μs and 1 second by changing one or two components on the card.

CONTROL LINES:
All output control lines at the ege connector are open collector and have these specifications:
Logic High = 3.7 V while sourcing 200 μA.
Logic Low = 0.5 V while sinking 7 mA.

All input control lines at the edge connector are applied to Schmitt trigger circuits and have these specifications:

Logic High = 2.0 V to 5.0 V (or no connection).
Logic Low = 0.0 V to 0.5 V (or short to ground).

The driving input signal must sink 1 mA in the low state.

TEMPERATURE RANGE:
From 0° to +70°C operating in the mainframe (allows 15°C internal rise in temperature when operating in the mainframe at up to +55°C ambient); from −40°C to +80°C storage.

CARD DIMENSIONS: 299.722 mm x 132.08 mm (11.8 in. x 5.2 in.)

+5 V CURRENT REQUIREMENT:
400 mA

Section II
INSTALLATION

2-1 INSPECTION

2-2 When the Interrupt card is received, inspect the card for any obvious defects that may have been incurred during shipment. Save the shipping carton and packing foam in the event that the card may have to be returned to Hewlett-Packard in the future.

2-3 Also check that the following items have been received with the card:

- I/O card connector assembly. An instruction sheet is provided with the I/O card connector assembly and shows how to assemble the connector. This information is also available in Chapter 2 of the 6942A Multiprogrammer User's Guide. The parts list in Section V of this manual lists all the parts and the corresponding Hewlett-Packard part numbers for the connector assembly.
- If applicable, a manual change sheet may be included with the manual. If a change sheet is included, check to see if the change applies to the serial number of the card you received.

2-4 AS-SHIPPED JUMPER CONNECTIONS

2-5 The Interrupt card contains various jumpers that define the values of the Data Type and LSB wake-up codes, and the logic level of the Trigger Polarity Select (TPS) line at the external edge connector. The card is shipped with jumpers set to specify the value listed below:

DATA TYPE CODE	= 3 (unsigned binary data); jumpers W3, W5, and W7 installed.
LSB VALUE	= 1 (unity); jumpers W12, W13, and W14 installed.
TRIGGER POLARITY SELECT LINE	= Logic high; jumper W1 removed.

NOTE

To change any of the jumpers mentioned, refer to Section III, Card Jumpers, for additional information.

2-6 INSTALLATION PREREQUISITES

2-7 Before installing the Interrupt card in a 6942A or 6943A chassis, consider the following prerequisite steps:

a. Determine which I/O slot will be used. An I/O card can be installed in slots 0 through 15. The card assumes the address of the slot (and unit) in which it is inserted. Also, a card in slot 0 has the highest interrupt priority, slot 1 the next highest priority, and slot 15 the lowest.

b. For the slot position selected, record the following:

1. card type.
2. card's subaddresses:

Subaddress	Read	Write
0	Reads stored input data	Loads reference register
1	Reads input data word at edge connector	Loads mode register
2	Reads mask word	
3	Reads reference word	

3. card's address, where:

CARD ADDRESS = SLOT NO. + (FRAME NO. X 100) + SUBADDRESS X 0.1)

(For example, 205.0 is the card address for a card in slot No. 5, frame number 2, referencing subaddress 0 as in a read data operation.)

2-8 Once these prerequisites have been checked, the card can be installed in the mainframe by performing the installation procedure in paragraph 2-9.

2-9 INSTALLATION PROCEDURE

2-10 To install the Interrupt card in the mainframe chassis, perform the following steps.

a. Turn off mainframe power.

CAUTION

To prevent an accidental short from damaging a card or a mainframe, always turn off Multiprogrammer power before installing or removing I/O cards.

b. Remove the rear cover of the mainframe by loosening the four quarter-turn fasteners.

c. Position the card so its handle is at the bottom, and the component side of the card is toward the right.

d. Slide the card into the desired slot position until the card just touches the backplane connector.

NOTE

A notch in the card edge and a key in the connector prevent the card from being installed upside down or in an illegal slot position.

e. With the card touching the connector, rotate the card handle downward until it engages the groove at the bottom of the I/O slot. Rotate the handle upward to insert the card into the backplane connector. (To remove a card, the handle is rotated downward.)

f. Install mainframe rear cover.

g. After the card is installed, you can proceed to make a partial test of the card by performing the functional test described in the next paragraph.

2-11 FUNCTIONAL CHECKOUT

2-12 After the card is installed, the user can run either of the two tests described in the 6942A Multiprogrammer User's Guide. These tests are:

a. The Self-Test Error Detection and Card Identifier Utility Program. This test is described in Chapter 2 of the 6942A Multiprogrammer User's Guide. This test checks the card control chip and the first rank storage register.

b. Example 7-42 in Chapter 7 of the 6942A Multiprogrammer User's Guide can be run to test the overall operation of the card. This test checks for proper response to given logic levels on the input data lines.

Section III
PRE-OPERATING INSTRUCTIONS

3-1 INTRODUCTION

3-2 The purpose of this section is to provide the user with additional card information that may be required for any of the following reasons:

- The user wishes to change the card jumpers from their "as shipped" positions to some new positions.
- The user requires additional information on the edge connector I/O signals.
- The user wishes to know what special considerations apply concerning filter delay time and the use of 2's complement arithmetic.

3-3 Since any of the above reasons affect the operation of the card, the information in this section should be read before implementing any card changes. The following topics are covered in the order mentioned.:

- Definition of all card jumpers.
- Card's External Edge Connector.
- External I/O Control Signals.
- Varying filter delay time.
- Using 2's complement input data.

3-4 CARD JUMPERS

3-5 As mentioned in Section II, the Interrupt card is shipped with certain jumpers in place. When the user wishes to change a jumper(s), the information in the following paragraphs should be referenced to find the location of the applicable jumper(s), and also, to see what other jumper arrangements are possible. The jumpers are described in the following order:

a. Bidirectional Data Transceivers.
b. Trigger Polarity Select Jumper.
c. Wake-Up Code Jumpers.
d. Flag Jumper.

3-6 Bidirectional Data Transceivers Jumper, W2

3-7 This jumper is installed at the factory and normally is never removed. This jumper establishes pin 9 of tri-state integrated circuits U25 and U43 (see Figure 6-2) at ground. With pin 9 held low, the open or isolated state of the transceivers is not used. Jumper W2 is temporarily removed during factory testing to allow the outputs of the transceiver to assume an open state for test purposes.

3-8 Trigger Polarity Select Jumper, W1

3-9 This jumper is removed prior to shipment making the Trigger Polarity Select (TPS), control line a logic high. If this jumper is installed, the TPS control line is held at a logic low level. The purpose of the Trigger Polarity Select signal is discussed in Table 3-3.

3-10 Wake-Up Code Jumpers

3-11 These jumpers determine the data type and LSB wake-up codes that are read from the card and stored in memory after power turn on. The user can override the values stored in memory by using a Set Format (SF) instruction. This is useful in applications that require a data format code or LSB value different from the values set at the factory. Any of the data types of Table 3-1 can be used. Programmed LSB values are not limited to those in Table 3-2. Any desired LSB value between 0.001 and 65.535 can be programmed. This allows the user to express programmed data in units appropriate to the process to which the card is dedicated.

3-12 If a new Data Type or LSB code will always be used, the jumpers on the card can be changed to reflect these new codes. This is more efficient than having the software constantly override the factory set values.

3-13 Data Type Code Jumpers, W3 through W8. The Interrupt card is shipped with jumpers W3, W5, and W7 installed and W4, W6, and W8 removed. The Multiprogrammer interprets these jumpers as data type code = 3, meaning as unsigned binary number. These jumpers can be changed to specify a different data type code. For example, data type 7 could be selected to program a reference word in octal form. Table 3-1 shows which jumpers must be installed and which jumpers must be removed to select other data type codes.

3-14 LSB Code Jumpers, W9 through W14. The Interrupt card is shipped with LSB Code jumpers W12, W13, and W14 installed; W9, W10, and W11 removed. These jumpers specify an LSB value of 1 (unity). Table 3-2 shows all the valid LSB values and the required jumpers.

3-15 Flag Jumper

3-16 Jumper W15 is installed at the factory and should not be removed. It is used only during factory testing of the card.

3-17 CARD'S EXTERNAL EDGE CONNECTOR

3-18 One dual 36-pin edge connector is supplied with each I/O card for interfacing field wiring to the card. The pin assignments of the I/O signals available at the card's external edge connector are shown in Figure 3-1. (The lettered pins are on the component side of the card.) Instructions for making up the mating connector and hood assembly are provided in Chapter 2 of the 6942A Multiprogrammer User's Guide.

Table 3-1. Data Type Code Jumpers

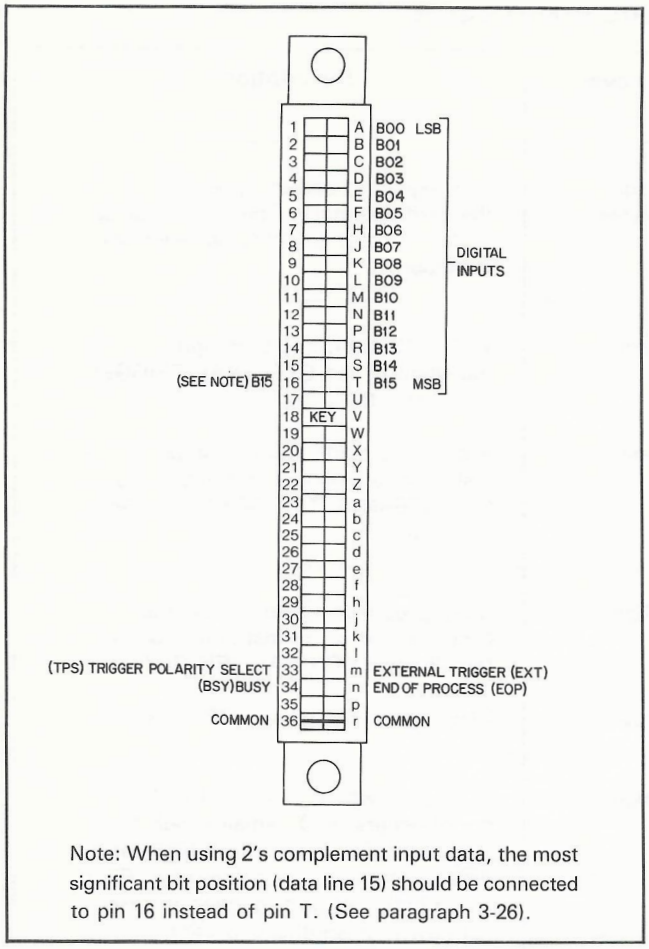
DATA TYPE CODE	DESCRIPTION	JUMPER ARRANGEMENT					
		W14	W13	W12	W11	W10	W9
1	Programmed positive or negative number is stored on card in Two's complement form.	OUT	OUT	OUT	IN	IN	IN
2	Programmed positive or negative number is stored on card IN sign-magnitude form.	OUT	OUT	IN	IN	IN	OUT
3	Programmed positive number is stored on card in unsigned binary form.	OUT	IN	OUT	IN	OUT	IN
4*	Special autorange code (used only with 69736A Timer/Pacer card)	OUT	IN	IN	IN	OUT	OUT
6	Programmed positive number is stored on card in unsigned BCD form.	IN	OUT	IN	OUT	IN	OUT
7	Programmed octal integer is stored on card in unsigned binary form.	IN	IN	OUT	OUT	OUT	IN

*When the card is shipped, its jumpers are arranged to select the starred data type when power is applied to the system.

Table 3-2. LSB Code Jumpers

CODE	LSB VALUE	JUMPER ARRANGEMENT					
		W20	W19	W18	W17	W16	W15
0	0.001	OUT	OUT	OUT	IN	IN	IN
1	0.025	OUT	OUT	IN	IN	IN	OUT
2	0.1	OUT	IN	OUT	IN	OUT	IN
3	0.5	OUT	IN	IN	IN	OUT	OUT
4	0.01	IN	OUT	OUT	OUT	IN	IN
5	0.05	IN	OUT	IN	OUT	IN	OUT
6	0.005	IN	IN	OUT	OUT	OUT	IN
7*	1.0	IN	IN	IN	OUT	OUT	OUT

*When the card is shipped, its jumpers are arranged to select the starred LSB value when power is applied to the system.



Note: When using 2's complement input data, the most significant bit position (data line 15) should be connected to pin 16 instead of pin T. (See paragraph 3-26).

Figure 3-1. Interrupt Card, External Edge Connector

3-19 DIGITAL INPUTS

3-20 As indicated in paragraph 3-13, the card is designed to accept external input words in unsigned binary form. It is also possible to use it with a two's complement input by making a slight modification to the card as described in paragraph 3-26. The programmed reference word to which the external binary input is compared can be expressed in decimal form if data type 1 or 3 is in effect for the card, or in octal form if data type 7 is in effect. These are the three data types usually used with this card. (Programming information is contained in Chapter 7 of the appropriate User's Guide.)

3-21 EXTERNAL I/O CONTROL SIGNALS (Figure 3-2)

3-22 Table 3-3 describes the control signals which interconnect between the Interrupt card and the customer's equipment. The actual electrical specifications for these signals are given in Table 1-1 of Section I.

3-23 VARYING THE FILTER DELAY TIME

3-24 To guarantee that erroneous interrupts due to the digital comparator's propagation delay are filtered out, the card's minimum filter time must be at least 5 μs. Longer filtering time may be necessary due to data settling time or contact bounce. The filter time can be varied from 5 μs to 1 second by changing one or two RC components on the card.

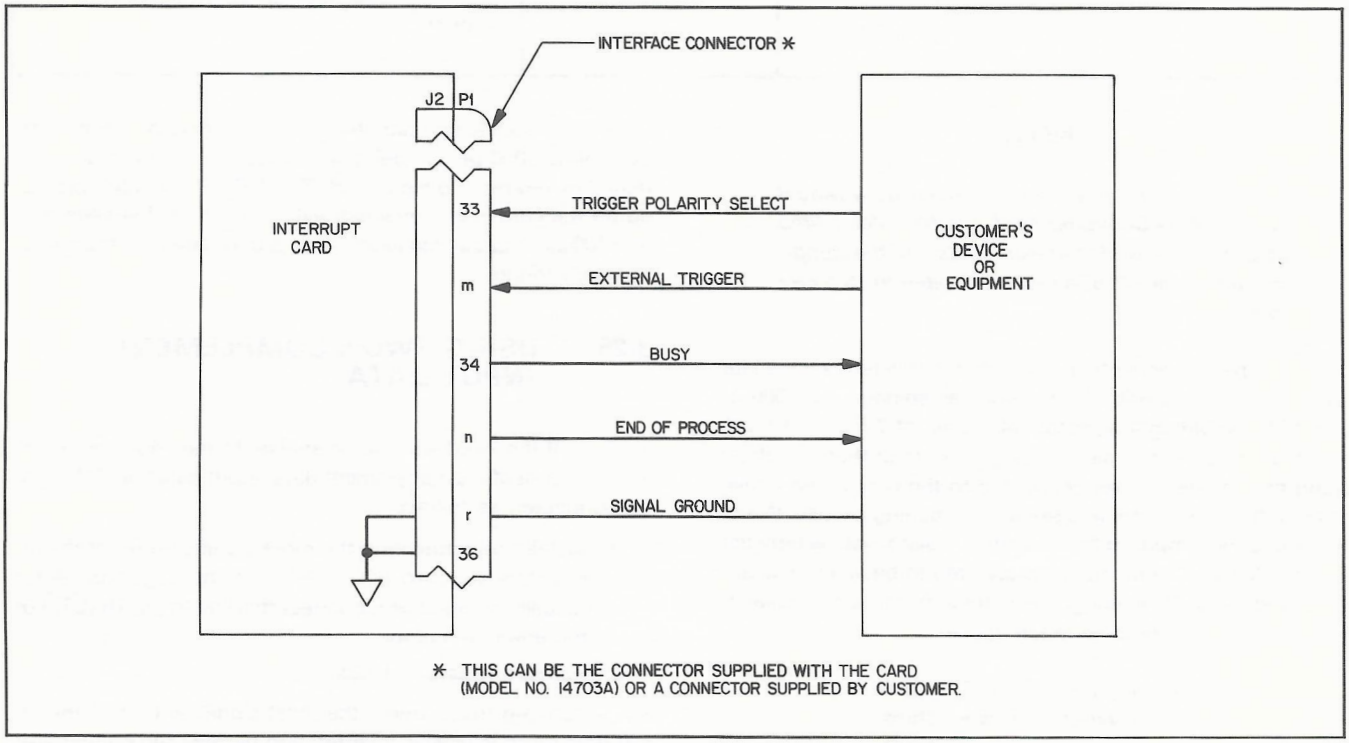


Figure 3-2. External I/O Control Signals

Table 3-3. Card's External I/O Control Signals

I/O Control Signal	Pin No.	TTL Level	Description
EXTERNAL TRIGGER also EXT (card input)	m	edge sensitive	This signal is used to cycle the card externally. The card must be cycled in order to detect an interrupt condition.
TRIGGER POLARITY SELECT also TPS (card output)	33	High	With TPS high, a low-to-high transition of the EXTERNAL TRIGGER line cycles the card.
		Low	If pin 33 is made low (or jumper W1 is installed), a high-to-low transition of the EXTERNAL TRIGGER line cycles the card.
BUSY also BSY (card output)	34	High	Busy goes high when the card is cycled either by an instruction or externally by EXTERNAL TRIGGER.
		Low	BUSY goes low when EOP goes high.
END-OF-PROCESS also EOP (card output)	n	High	Goes high when an internal FLAG signal occurs. EOP remains high for a minimum of 2 μs and stays high for a time dependent on the firmware. Pin n going high can be to trigger an external device or another I/O card.
		Low	EOP is set low by the Multiprogrammer in response to an interrupt request.

NOTE

If the interrupt card is being driven by a Model 69751A A/D Converter card, the filter delay time must be increased to at least 30 μs and the sampling rate of the 69751A must be limited to 16.5 kHz (60μs).

3-25 The components on the board that determine the filter delay are C37 and R46. Their values as shipped are 1000 pF and 15 k, providing a nominal delay time of 7.5 μs +1.5 μs). The filter delay is typically 1.5 μs greater than that calculated using the equation given below due to the propagation delay through the comparator and signal conditioning circuits. Within the restrictions imposed by (1) limiting resistor values between 5 k and 260 k, (2) limiting the delay time to between 5 μs and 1 second, and (3) limiting the minimum capacitor value to 1000 pF, the following equation applies:

td (filter delay time) = 0.45 (RC) seconds
Where: R is in Ohms,
C is in Farads,
td is in seconds.

There are actually no restrictions on the capacitor value used, but below 1000 pF the delay time must be graphically determined by referring to Figure 3-3. The 1000 pf capacitor provided on the card is a convenient value for delays between 5 μs and 100 μs. A larger capacitor is needed for delays that are substantially longer.

3-26 USING TWO's COMPLEMENT INPUT DATA

3-27 If the input word to be applied to the edge connector is in the form of 2's complement data, input data line B15 must be connected as follows:

1. Instead of connecting the most significant bit of the input data word to pin T (B15) of the edge connector (usually connection), connect this line to pin 16 ($\overline{B15}$) of the edge connector.
2. Remove resistor R1 (200 Ω).

By performing these steps, the most significant bit of the input data word is always inverted and permits the comparator to interpret the input data in an offset 2's complement format.

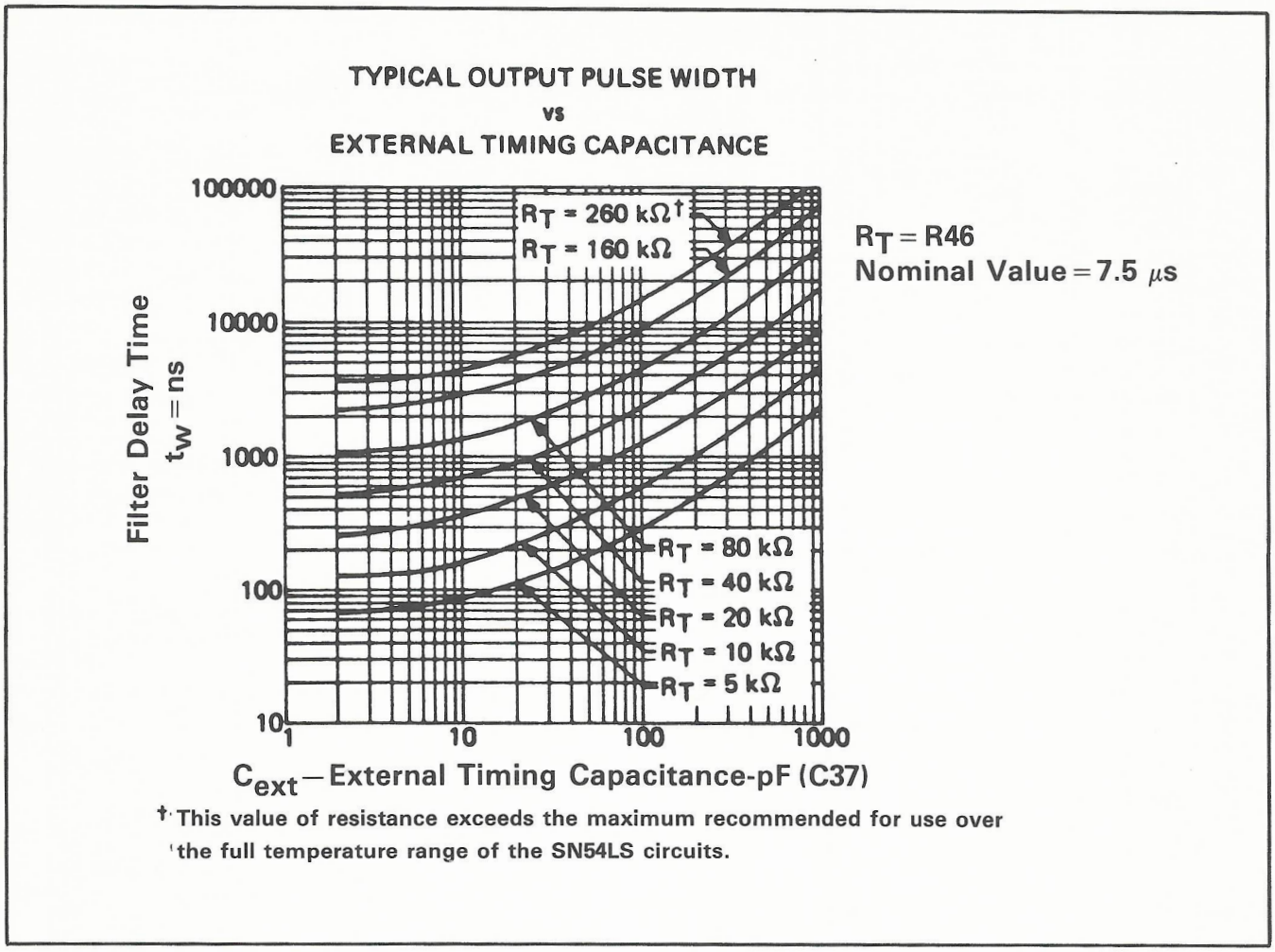


Figure 3-3. Delay Time vs. R-C Values



Section IV
THEORY OF OPERATION

4-1 INTRODUCTION

4-2 This section explains the theory of operation for the Interrupt card. The theory assumes that the reader is familiar with the instruction set and the basic operation of the 6942A Multiprogrammer. First, a brief description is given covering the basic operation and features of the card. A detailed block diagram discussion then follows. This section concludes with an example of how the card processes a set of typical instructions that might be sent to process an interrupt condition.

4-3 OVERALL OPERATION

4-4 Power Turn-On

4-5 When power is applied to the Interrupt card, the circuits on the card are first cleared. Then a self test is initiated by the Multiprogrammer to test the circuits of the Interrupt card. The self-ID, data type, size, and LSB parameters of the card are read and stored in the Multiprogrammer memory as part of the wake-up sequence.

4-6 Setting Up an Interrupt Condition

4-7 As mentioned in Section I, three registers are used to define an interrupt condition: the reference register, the mode register, and optionally, the mask register. Depending on the logical comparison to be made between the input data word and the reference word, any one or all of these registers must be programmed prior to cycling the card. Immediately after power turn-on, these registers are initialized with the following values:

a. The reference register is cleared (set to a zero value).
b. The mode register is set to the A ≠ B condition.
c. The mask register is cleared (set to a zero value) meaning that unless a different mask word is programmed, all 16-bits of the input data word are compared with all 16-bits of the reference word.

4-8 In addition, after power turn on, the 16 input data lines at the edge connector are monitored by three separate circuits: (1) an input data buffer, (2) an input data storage register, and (3) a 16-bit comparator circuit. The input data buffer always contains the data word currently appearing at the edge connector. This data word can be read at any time by a Read Value instruction referencing subaddress 1. The other two circuits also monitor the input data lines, but do not act on the input data until after the card is cycled.

4-9 Cycling the Card

4-10 Once the reference register, mode register, and mask word register are programmed for the interrupt condition, the card must be cycled to detect when the interrupt condition is met. The card can be cycled in one of two ways (See Figure 4-1):

1. Externally, by applying an External Trigger signal to the edge connector. When an EXTERNAL TRIGGER pulse is used, an additional signal called TRIGGER POLARITY SELECT determines whether cycling will occur on the low-to-high or high-to-low transition of the EXTERNAL TRIGGER pulse.
2. By the program, with a separate Cycle (CY) instruction, or with an output instruction that, in addition to loading one of the previous mentioned registers, also cycles the card. For example, a Write and Cycle (WC) instruction.

4-11 Upon cycling the card, BUSY and GATE signals are asserted. BUSY is applied to the edge connector and to the status buffer. BUSY being high indicates that the card is waiting for an interrupt condition to occur. BUSY can be monitored by inspecting bit 1 of the status word returned by a Read Status (RS) instruction. GATE going high triggers a 9 μs delay circuit. This delay time is required to allow for gate propagation delay and settling time so that erroneous interrupt conditions that might exist are not acted on simultaneously with the card being cycled.

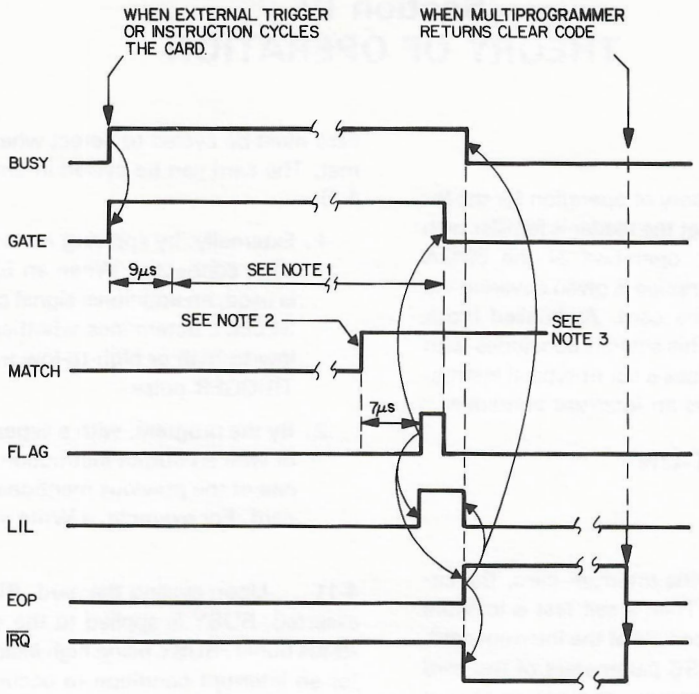
4-12 After this time delay passes, the data word appearing at the 16 input data lines is compared with the reference word. This comparison results in one of four logical conditions (comparator output lines) being true.

$$A = B$$
$$A > B$$
$$A < B$$
$$A \neq B$$

where; A is the input data word.
B is the reference data word.

4-13 Detecting the Interrupt Condition

4-14 Whichever logical condition is true is then compared with the interrupt condition speciifed by the mode register. If the result of the logical comparison from the comparator matches the logical condition specified by the mode register, a MATCH signal goes high and triggers a 7 μs filter delay circuit. This delay circuit prevents any interrupt conditions from being recognized until after the delay time passes. If the interrupt condition is still present after this delay time and the card has been cycled (gate is high), a positive going FLAG signal is generated.



NOTES:
1. During this time the card is ready to detect the interrupt condition and set FLAG.
2. MATCH goes high when an interrupt condition is detected.
3. MATCH remains high until the interrupt condition is removed or the reference register or mode register is programmed with a different value.

Figure 4-1. Card Cycling and BUSY/EOP Timing

4-15 Storing the Input Data Word

4-16 When FLAG is generated it is applied to the universal control chip on the card where internally it is used to produce a high going Load Input Latch (LIL) signal and a high going EOP signal, and also forces the GATE signal low. The effect of these signals is as follows:

a. LIL going high strobes the 16-bit input data word (just used in the comparison) into the input data storage register where it is temporarily stored.
b. EOP going high indicates that the interrupt condition has been met and that the data word is currently in the input data storage register. EOP is applied to the edge connector and also to the Self-ID/Status buffer. The program can monitor the EOP line by inspecting bit Ø of the status word returned by a Read Status (RS) instruction. EOP also clears BUSY.
c. GATE going low forces FLAG to go low.

4-17 Interrupt Request

4-18 When the End-of-Process (EOP) signal occurs, an Interrupt Request ($\overline{IRQ}$) is returned to the Multiprogrammer if the card is armed. The $\overline{IRQ}$ signal informs the Multiprogrammer that a data word meeting the interrupt condition is stored in the data register. For WF, WC and CY instructions, the card must be armed prior to the execution of the instruction if an interrupt request is to be generated. This can be done with a separate Arm Card (AC) instruction issued by the controlller.

4-19 Reading the Input Data Word

4-20 When the program detects the interrupt request signal, an input instruction (e.g. Read Value) can be issued referencing subaddress Ø to read the data word in the Input Data Storage Register. In addition, the data word in the Input Data Buffer can also be read (at subaddress Ø1) which reflects the data word at the edge connector at the moment the instruction is issued.

4-21 Restoring the Card to an Idle Condition

4-22 Some time after the interrupt occurs, the Multiprogrammer sends a clear code to the card which clears the ARM and EOP signals and the Group Address Flip-Flop (GAFF). No further interrupt conditions will be detected unless the card is again cycled. The data word at the ege connector can always be read even when the card is in the idle state.

4-23 The GAFF is internal to the Universal Control chip on the card and is set by high level instructions, such as; WC,

OS, OP, to allow multiple cards to be cycled in parallel (or simultaneously). Refer to Chapter 4 in the 6942A Multiprogrammer Users' guide for more information on cycling cards in parallel.

4-24 DETAILED BLOCK DIAGRAM DISCUSSION (Figure 4-2)

4-25 When the Interrupt card is installed in a slot position in the Multiprogrammer, 6942A, or in the Extender chassis, 6943A, the card is assigned the address of that slot position. Once installed, the card connects to the data lines, BØ-B15, to the control lines, and to the power input lines of the backplane.

4-26 The following paragraphs describe the functional circuits shown in Figure 4-2. The functional schematic in Section VI should also be referenced.

4-27 Universal Control Chip (UCC)

4-28 This control chip U49 supervises all the operations taking place on the Interrupt card. The UCC establishes the timing sequence for the various control signals used on the card.

4-29 When power is applied to the card, a PCR control signal goes high and clears all cirucits on the card. The card is then ready to process any instruction issued at the controller that addresses the card. When an instruction is issued the following input control lines set up the UCC for a particular operation:

CAD - This is the card address line which goes high to select the Interrupt card when the card is addressed in an instruction.

R/$\overline{W}$ - This is the read/write line. It is high for a read operation and is low for a write operation.

SADØ, SAD1 - These two lines supply a subaddress to the card.

CTLØ, CTL1, CTL2 - These lines supply a 3-bit control code to the UCC to indicate what operation is to be performed. Depending on the instruction issued, one or more codes are sent in succession.

4-30 The data values on the above control lines are loaded into the UCC when a data strobe (DST) pulse occurs. This data is then decoded to produce the various control signal outputs required for the indicated operation. A description of these control signals as they relate to the function being performed is included in the following paragraphs.

4-31 Tri-State Bidirectional Data Transceivers

4-32 The tri-state bidirectional transceivers control the direction of data flow to and from the card over the BØ-B15 data lines. During a write operation, control signal CDE goes low and the BØ-B15 data lines are connected to the input of the reference register, mask register, and mode register. CDE is a control signal that controls the directions of the data transceivers.

4-33 During a read operation, CDE goes high and the BØ-B15 data lines are connected to the output of the reference register return buffer, mask register return buffer, input data buffer, input data storage register, and self-ID/status buffer. Although the transceivers are tri-state logic, jumper W2 establishes pin 9 at ground (see schematic diagram) so that the isolated or open state condition is never used.

4-34 Mode Register

4-35 This register determines which logical condition must be met in order for an interrupt to occur. The octal value loaded into this register specifies the logical condition to be tested. When an output instruction is issued referencing subaddress Ø1, an STB 1 strobe pulse is generated and loads the register. The card below summarizes which logical conditions are set by the octal value stored. On power turn-on the register is set to the A ≠ B condition.

To specify the Logical Condition	Load the Mode register with the octal value
A ≠ B	1
A = B	2
A > B	4
A < B	10
none of the above	0

where; A is the input data word and
B is the reference word

4-36 Reference Register

4-37 The contents of this register is compared with the input data word applied to the edge connector. the register is cleared on power turn-on and is loaded by an STB Ø pulse when an output instruction referencing subaddress ØØ is issued.

4-38 Reference Register Return Buffer

4-39 This buffer always contains the contents of the reference register. To read the reference word, a Read Value instruction to subaddress Ø3 is used. When subaddress Ø3 is decoded by the UCC a $\overline{RTN3}$ signal connects the output of the reference register to the BØ-B15 lines.

4-40 Mask Register

4-41 The mask register is loaded with a mask word and is used in conjunction with AND gates to determine which bit positions of the input data word are to be tested. The mask register is loaded by an STB 2 strobe pulse when an output instruction is issued to subaddress Ø2. The register is cleared to zero on power turn-on. All zeroes permit all 16-bits to be used in the logical comparisons. Each bit position to be removed from the comparison must be programmed with a "1".

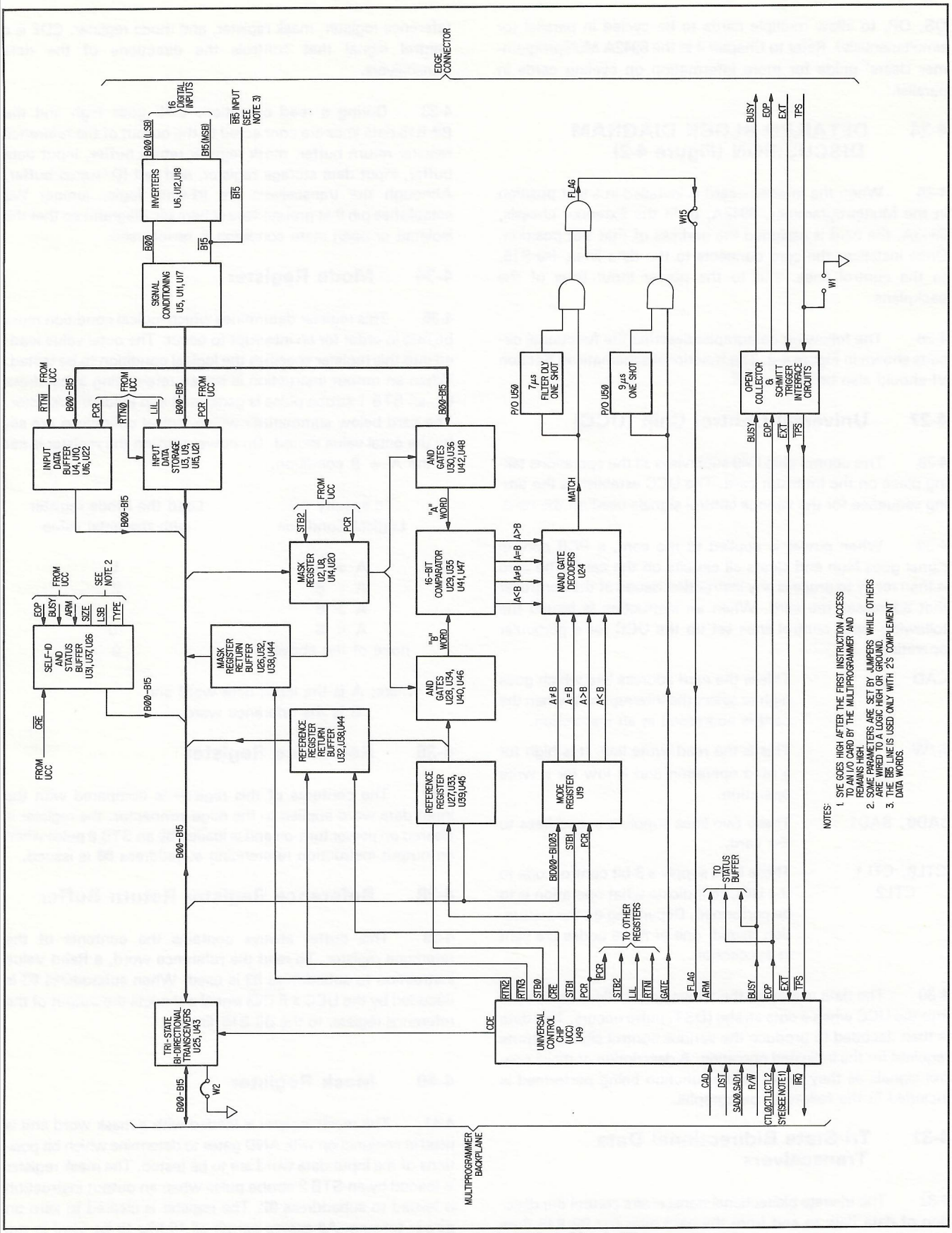


Figure 4-2. Interrupt Card, Detailed Block Diagram

4-42 Mask Register Return Buffer

4-43 This register permits the mask word in the Mask Register to be read by the Multiprogrammer. An input instruction to subaddress Ø results in an $\overline{\text{RTN2}}$ signal which places the contents of the register on the BØØ-B15 lines.

4-44 AND Gates

4-45 These gates are enabled after power turn on by all 0's in the Mask Register. A "1" programmed to any bit position in the Mask Register results in the corresponding output line going low and disabling the associated AND gate. Since the same output line is connected to both banks of AND gates, the bit positions for both reference word and input data word are disabled simultaneously.

EXAMPLE: If only the even bit positions of the input data word are to be compared with the even bit positions of the reference word, 0's would be programmed in all even bit positions of the mask word while 1's would be programmed in all odd bit positions. The bit positions having the 1's would result in the corresponding $\overline{\text{BØØ-15}}$ lines going low to disable the appropriate AND gates.

4-46 16-Bit Comparator

4-47 This circuit compares the input data word to the reference word and asserts one of three lines high depending on the result of the comparison. These lines are labeled A = B, A > B, and A < B and are connected to decoders which also receive four logical lines from the mode register.

4-48 Nand Gate Decoders

4-49 A bank of four two-input gates comprise the decoder circuit. Each NAND gate receives one of the A = B, A > B, A ≠ B, and A < B lines from the mode register. The second input receives the corresponding A = B, A > B, and A < B lines from the comparator circuit. The A = B lines from the comparator is inverted to obtain the A ≠ B input to the decoder. When the result of the logical comparison matches the logical condition specified by the mode register, one of the decoder NAND gates produces a MATCH signal. This signal triggers the 7 μs filter delay one shot circuit.

4-50 7 μs Filter Delay One Shot

4-51 This circuit is triggered by a high going MATCH signal. The purpose of this circuit is to provide a time interval during which a MATCH signal, if present, is not recognized. If MATCH signal is still present after the delay time has passed, then the logical comparison is valid and a FLAG signal is generated. The filter delay time is intended to prevent false MATCH signals due to transients or spurious signals from being recognized.

4-52 9 μs One Shot

4-53 This delay circuit is triggered when the GATE signal goes high upon cycling the card. The $\overline{\text{Q}}$ output remains low for approximately 9 μs and prevents a FLAG signal from going high should a MATCH signal be present concurrent with the card being cycled.

4-54 Input Data Buffer

4-55 This buffer is cleared initially on power turn on. The input lines to this buffer are connected directly to the edge connector via the signal conditioning circuits. The content of this buffer will be identical to the data word at the edge connector. The data word in this buffer is placed on the BØØ-B15 data lines by a $\overline{\text{RTN1}}$ signal when an input instruction is issued referencing subaddress Ø1.

4-56 Input Data Storage Register

4-57 This register is loaded with the data word at the edge connector by a Load Input Latch (LIL) signal. LIL is generated by FLAG when an interrupt condition is met after the card is cycled.

4-58 The contents of this register are placed on the BØØ-B15 lines by a $\overline{\text{RTNØ}}$ when an input instruction referencing subaddress ØØ is issued.

4-59 Signal Conditioning

4-60 Each input data line at the edge connector is connected to an RC signal shaping circuit. Invert buffers amplify the signals prior to signal conditioning. In the special case where the input data word is in 2's complement form, the MSB line is connected directly to the signal shaping circuit, bypassing the first buffer inverter.

4-61 Self-ID/Status Return Buffers

4-62 These buffers are also tri-state and their outputs are held in an open or isolated condition while the $\overline{\text{CRE}}$ control line is high. When a self-ID status operation is decoded from the control lines, $\overline{\text{CRE}}$ goes low. This connects the inputs of the self-ID/status return buffers to the BØ-B15 data lines. The self-ID/status word sent to the Multiprogrammer is shown below.

4-63 The 16-bits (BØ-B15) are read back during self-test or when a Read Status (RS) instruction is programmed. During self-test, bits B3-B14 are stored in the Multiprogrammer memory while status bits BØ-B2 are ignored. When an RS instruction is issued, status bit BØ are stored in Multiprogrammer Memory while bits B3-B125 are ignored.

4-64 The self-ID bits, B3-B15, specify the "wake-up" values of the LSB, card ID, size, and data type parameters. The values of the parameters determine how the Multiprogrammer firmware will process the data it sends to or receives from the card. Status bits, BØ-B2, are used by the Multiprogrammer to check the status of the card during operation. The status information is provided by UCC outputs, ARM, BSY, and EOP.

← SELF-ID PARAMETERS →					← STATUS →		
LSB	CARD IDENTIFICATION		SIZE	DATA	ARM	BUSY	EOP
15-13	12	7	6	5 3	2	1	0
jumpers set this field to 111 which corresponds to unity.	Hardwired to binary code of 001100 which corresponds to an ID of decimal 12.		Hardwired to binary 1 which signifies a 16-bit data word.	jumpers set this field to 010 which is incremented to 3 by the firmware (unsigned binary).	These are one bit flags where 1 = true 0 = false		

4-65 Open Collector and Schmitt Trigger Circuits

4-66 The input control lines EXT and TPS are applied to Schmitt trigger buffer inverter circuits before being applied to the UCC. Pull up resistors on both signal lines terminate these lines from the external sending device.

4-67 The output control signals BUSY and EOP are supplied to open collector AND gates with a pull-up resistor on each output line. The signal specifications for these signals are given in Table 1-1 in Section I.

4-68 PROCESSING OF AN "INTERRUPT" CONDITION

4-69 This discussion explains the processing of an interrupt condition, the instructions and the corresponding signals that occur.

a. **Setting up the Interrupt Condition.** In this example, the Interrupt card in slot 4 is addressed and the reference register and mode register are loaded with data. No mask bit is used in this example so it is assumed the mask register contains all 0's (all 16-bits used in the comparisons).

"WF,4.1,2T" (loads mode register with A = B condition).
"WF,4.0,1000T" (loads reference register with the value 1000).

b. **Arming the Card.** Next, an Arm Card instruction is issued so that when an interrupt condition is tested and is true, an interrupt request is sent to the Multiprogrammer.

"AC,4T" (sets the ARM flag internal to the UCC chip. The ARM control signal goes high).

c. **Cycling the Card.** A cycle Card instruction is issued to begin testing for logical comparisons between the reference word and (1000) and the input data word at the edge connector.

"CY,4T" (Cycles the card in slot position 4).

The Multiprogrammer sends a control code to the card to initiate a "cycle" operation. BUSY and GATE signals at the UCC go high. The 16-bit comparator circuit compares the input word with the reference word. When the input word at the edge connector becomes equal to the value 1000, a FLAG signal goes high. FLAG is applied to the UCC and results in a LIL signal loading the input word into the input data storage.

d. **End-of-Process and Interrupt Request.** When FLAG goes high it also produces a high going EOP signal. Because the card is armed, a low going IRQ signal is returned to the Multiprogrammer.

e. **Reading the Input Data Word.** Since the data word that resulted in the interrupt condition is stored in the input data storage register, the following instruction can be issued to retrieve the data word.

"RV,4.1 T"

f. **Placing Card in Idle State.** Some time after IRQ signal is sent to the Multiprogrammer, a clear code is returned to the interrupt card by the Multiprogrammer firmware to clear the ARM, EOP, IRQ flags. The interrupt card remains in the idle mode until the card is again cycled.

Section V
PARTS LIST

5-1 INTRODUCTION

5-2 This section contains information on ordering replacement parts for the Interrupt card Model 69776A. Table 5-1 lists the electrical and mechanical components of the card. Table 5-2 lists the parts comprising the external I/O connector assembly supplied with the card. Figure 5-1 illustrates how the parts in Table 5-2 are assembled.

5-3 HOW TO ORDER PARTS

5-4 You can order parts from your local Hewlett-Packard sales office. Refer to the list of sales offices at the end of this manual for the office nearest you. When ordering parts include the following information:

a. the Hewlett-Packard part number.
b. a description of the part.
c. the quantity desired.
d. the model number of the card (69776A) on which the part is used.

5-5 If you wish to order a part directly from the manufacturer, locate the manufacturer's Supply Code in Table 5-1 and use this code to find the manufacturer's address in Table 5-3.

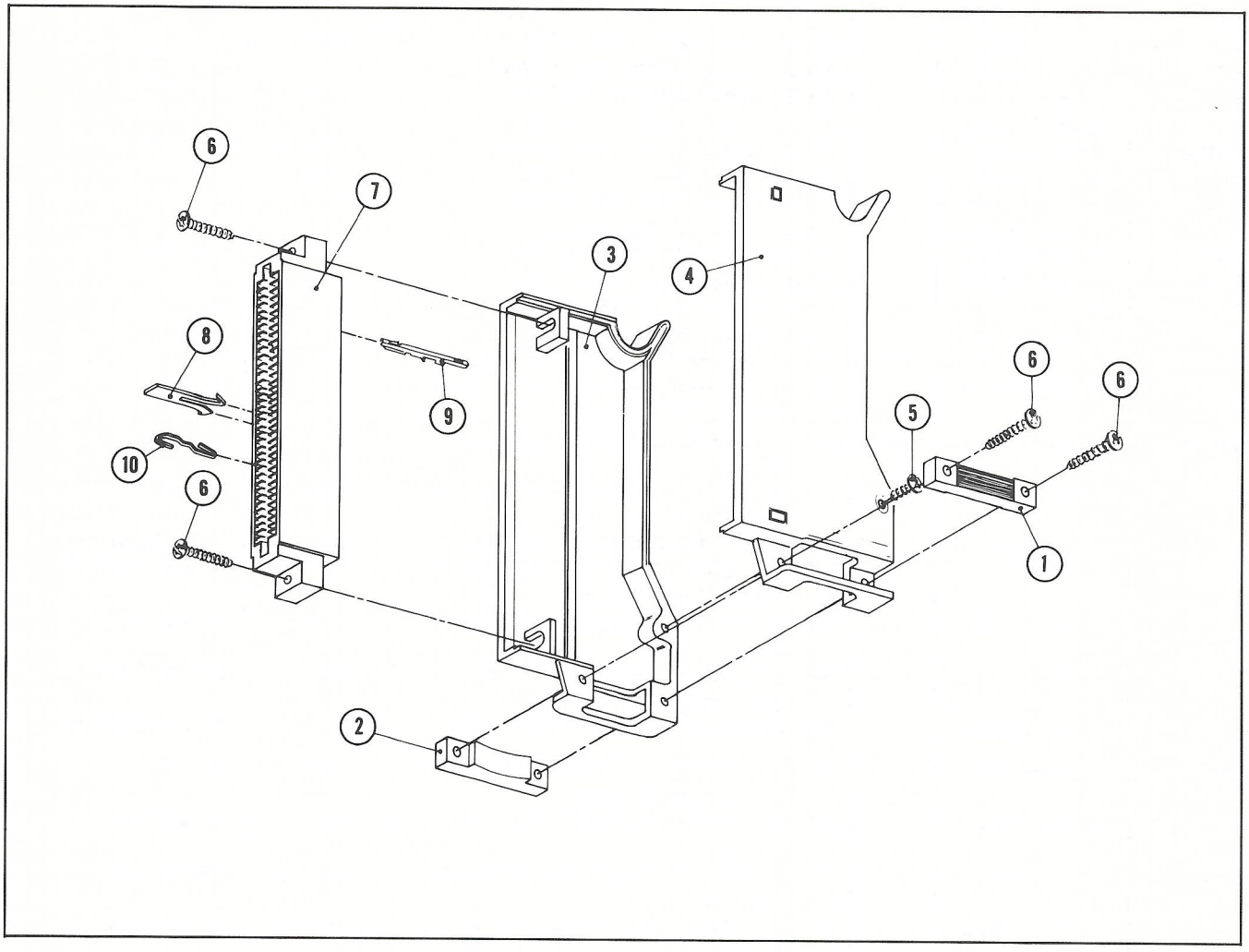


Figure 5-1. Connector Assembly. Exploded View

Table 5-1. 69776A Parts List

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
C1-8	0160-2289	18	fxd cer 2200pf +-20% 200Vdc	28480	
C9	0160-4722	19	fxd cer 0.1uf +80-20% 50Vdc	28480	
C10,11	0160-2289		fxd cer 2200pf +-20% 200Vdc	28480	
C12	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C13,14	0160-2289		fxd cer 2200pf +-20% 200Vdc	28480	
C15-18	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C19-22	0160-2289		fxd cer 2200pf +-20% 200Vdc	28480	
C23-35	0160-4722		fxd cer 0.1uf +80-20% 50Vdc	28480	
C36,37	0160-2735	2	fxd mica 1000pf +-5% 100Vdc	28480	
C38	0160-2289		fxd cer 2200pf +-20% 200Vdc	28480	
C39	0180-0291	1	fxd elect TA 1uf +-10% 35Vdc	56289	150D105X9035A2
C40	0160-2289		fxd cer 2200pf +-20% 200Vdc	28480	
R1,2	0683-2015	18	fxd comp 200 5% 1/4W	01121	CB2015
R3,4	0683-5125	28	fxd comp 5.1K 5% 1/4W	01121	CB5125
R5,6	0683-2015		fxd comp 200 5% 1/4W	01121	CB2015
R7,8	0683-1035	4	fxd comp 10K 5% 1/4W	01121	CB1035
R9,10	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R11-14	0683-2015		fxd comp 200 5% 1/4W	01121	CB2015
R15,16	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R17-20	0683-2015		fxd comp 200 5% 1/4W	01121	CB2015
R21-24	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R25-28	0683-2015		fxd comp 200 5% 1/4W	01121	CB2015
R29	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R30-44	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R45	0683-2035		fxd comp 20K 5% 1/4W	01121	CB2035
R46	0757-0446	1	fxd film 15K 1% 1/8W	24546	C4-1/8-T0-1502-F
R47,48	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
R49	0683-2015		fxd comp 200 5% 1/4W	01121	CB2015
R50	0683-1035		fxd comp 10K 5% 1/4W	01121	CB1035
R51	0683-2015		fxd comp 200 5% 1/4W	01121	CB2015
R52	0683-5125		fxd comp 5.1K 5% 1/4W	01121	CB5125
U1	1820-2257	9	IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U2	1820-2279	1	IC FF CMOS D-TYPE POS-EDGE-TRIGGERED COM	04713	MC14175BCP
U3,4	1820-1544	13	IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U5,6	1820-1416		IC SCHMITT TRIGGER TTL LS INV HEX	01295	SN74LS14N
U7	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U8	1820-2279		IC FF CMOS D-TYPE POS-EDGE-TRIGGERED COM	04713	MC14175BCP
U9,10	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U11,12	1820-1416		IC SCHMITT TRIGGER TTL LS INV HEX	01295	SN74LS14N
U13	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U14	1820-2279		IC FF CMOS D-TYPE POS-EDGE TRIGGERED COM	04713	MC14175BCP
U15,16	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U17,18	1820-1416		IC SCHMITT TRIGGER TTL LS INV HEX	01295	SN74LS14N
U19	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF

Table 5-1. 69776A Parts List (cont.)

Ref Desig	HP Part No	Qty	Description	Mfr Code	Mfr Part No
U20	1820-2279		IC FF CMOS D-TYPE POS-EDGE-TRIGGERED COM	04713	MC14175BCP
U21,22	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U23	1820-1416		IC SCHMITT TRIGGER TTL LS INV HEX	01295	SN74LS14N
U24	1820-1198		IC GATE TTL LS NAND QUAD	01295	SN74LS03N
U25	1820-2239	2	IC DRVR TTL S BUS	27014	DP8304BN
U26	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U27	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U28	1820-1486	8	IC GATE CMOS AND QUAD	3L585	CD4081BE
U29	1820-1340	4	IC COMPTR CMOS MAGTD	04713	MC14585BCP
U30	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U31,32	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U33	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U34	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U35	1820-1340		IC COMPTR CMOS MAGTD	04713	MC14585BCP
U36	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U37,38	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U39	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U40	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U41	1820-1340		IC COMPTR CMOS MAGTD	04713	MC14585BCP
U42	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U43	1820-2239		IC DRVR TTL S BUS	27014	DP8304BN
U44	1820-2257		IC BFR CMOS BUS DRVR HEX	04713	MC14503BCP
U45	1820-1544		IC FF CMOS D-TYPE COM CLK QUAD	3L585	CD4076BF
U46	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U47	1820-1340		IC COMPTR CMOS MAGTD	04713	MC14585BCP
U48	1820-1486		IC GATE CMOS AND QUAD	3L585	CD4081BE
U49	1820-2302	1	IC CONTROL CHIP	28480	
U50	1820-1423	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U51	1820-1246	1	IC GATE TTL LS AND QUAD	01295	SN74LS09N
U52	1820-1201	1	IC GATE TTL LS AND QUAD	01295	SN74LS08N
Z1,2	1810-0280	2	RESISTOR NETWORK 10K (9)	01121	210A103
Z3,4	1810-0164	2	RESISTOR NETWORK 4.7K (8)	91637	CSP09C07-472J
			MECHANICAL PARTS		
	69776-80001	1	CARD EXTRACTOR	28480	
	1480-0059	1	..PIN ROLL (.062 IN.)	28480	
	69776-90003	1	MANUAL, OPERATION AND INSTRUCTION	28480	
	1200-0552	1	SOCKET-IC 40 CONTACT (U33)	28480	
	1200-0811	1	SOCKET-16 PIN (U5)	28480	
	5060-2806	1	EXTERNAL EDGE CONNECTOR ASSEMBLY	28480	
	9211-4189	1	SHIPPING CARTON	28480	

Table 5-2. Manufacturer's Federal Supply Codes

Code	Manufacturer	Address
01121	Allen-Bradley Co.	Milwaukee, WI
01295	Texas Instruments, Inc. Semiconductor-Components Division	Dallas, TX
04713	Motorola Semiconductor Products, Inc.	Phoenix, AZ
24546	Corning Glass Works	Bradford, PA
27014	National Semiconductor Corp.	Santa Clara, CA
28480	Hewlett-Packard Co.	Palo Alto, CA
3L585	RCA Corp. Solid State Division	Somerville, NJ
56289	Sprague Electric Co.	North Adams, MA
91637	Dale Electronics	Columbus, NE

Table 5-3. Parts List For External Connector Assembly*
(HP Part No. 5060-2806)

HP Part No.	Index No.	Description	Qty
1251-6307		Hood Assembly**	
	1	**Strain Relief	
	2	**Cable Clamps	
	3	**Right Hood Assembly	
	4	**Left Hood Assembly	
	5	**Screw, 7/16 Inch	
	6	**Screws, 11/16 Inch	
1251-6059	7	Connector Pin Housing	1
1251-6056	8	Connector Key	1
1251-6183	9	Solder Pins, Plated	45
1251-6380	10	Springs, Retaining	6

* Can be ordered as Model 14703A, Card Edge Connector
** Item 1251-6307 consists of index items 1 through 6.

Section VI
DIAGRAMS

6-1 COMPONENT LOCATION

6-2 Figure 6-1 shows the location of the test points and components on the Interrupt card.

6-3 FUNCTIONAL SCHEMATIC DIAGRAM

6-4 Figure 6-2 is the schematic diagram of the Interrupt card. The schematic diagram uses the ANSI Y32.14 and the IEEE Standard, 91, for the representation of logic elements. A brief summary of this notation is given in Table 6-1.

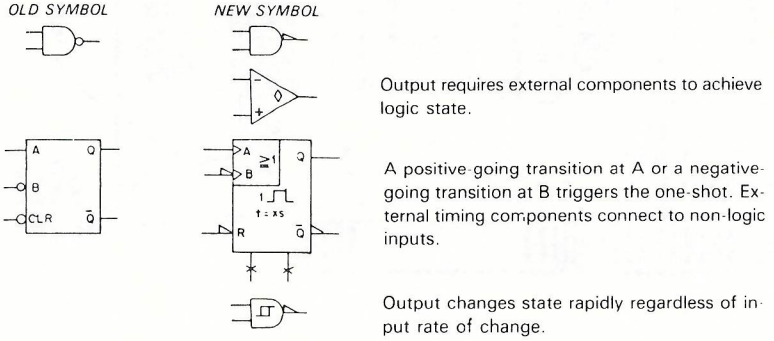
Table 6-1. Abbreviated List of ANSI Y32.14 Schematic Symbols

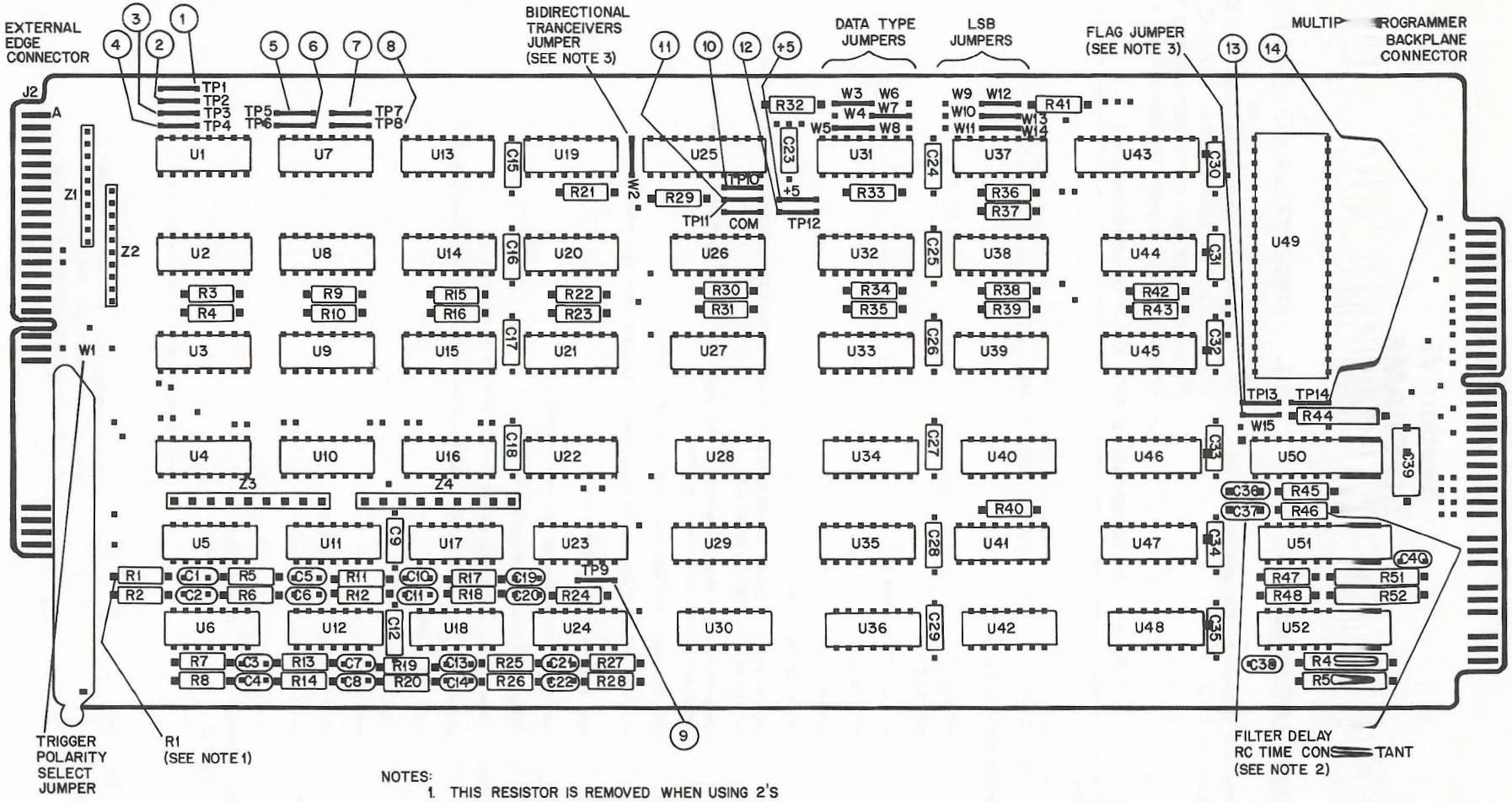
Definitions:

High = more positive
Low = less positive
True = logical "1" state
False = logical "0" state

Indicator and Qualifier Symbols

Σ	Adder
≥	OR FUNCTION
= 1	exclusive OR function
&	AND function
▽	3-state output
EN	enable Device output
	(polarity indicator, shown outside logic symbol) Any marked input or output is active low; any unmarked input or output is active high.
	(dynamic indicator) Any marked input is edge-triggered, ie, active during transition between states; any marked input is level sensitive.
	(Schmitt trigger) indicates that hysteresis exists in device.
	(non-logic indicator) Any marked input or output does not carry logic information.)
	open-collector or open emitter output
1	non-retriggerable monstable (one-shot) multivibrator
	Retriggerable monostable multivibrator
t = xSec	indicates pulse width (usually determined by external RC network)
G	gate input (a number following G indicates which inputs are gated);also, astable element
C	control input (clock)
R	reset (clear)
S	set (preset)
D	data input to storage element
▷	buffered element with extra output capacity





NOTES:

1. THIS RESISTOR IS REMOVED WHEN USING 2'S COMPLEMENT ARITHMETIC.
2. THESE R&C COMPONENTS CAN BE CHANGED TO ACHIEVE A DIFFERENT FILTER DELAY TIME.
3. USED FOR FACTORY TESTING ONLY.

Figure 6-1. Interrupt Card Component Location

NOTES:

1. The card is shipped with jumpers as shown in this schematic.
2. On IC U25, a 0.1μF capacitor, C23, is connected across pins 20 (+5 V) and pin 10 (ground). On IC U43, a 0.1 μF capacitor, C30, is connected across pins 20 (+5 V) and pin 10 (Ground).
3. The designation N.C. means "not connected."
4. Test points shown in this diagram can be found in Figure 6-1 Component Location diagram.
5. Unless otherwise specified:
   All resistors are 5%, 1/4 watt.
   All capacitors are in microfarads.
6. When the card is being used to monitor 2's complement data words applied to the edge connector, data words applied to the edge connector, remove resistor R1 and connect bit 15 of the input word to IC, U5 pin 3 instead of pin T.

Test Point Table-See Component Location Diagram

Test	Mnemonic	Signal Name
TP1	LIL	Load Input Latch
TP2	RTN0	Return 0
TP3	RTN1	Return 1
TP4	RTN2	Return 2
TP5	RTN3	Return 3
TP6	STB0	Strobe 0
TP7	STB1	Strobe 1
TP8	STB2	Strobe 2
TP9	MATCH	Match
TP10	CDE	Card Drive Enable
TP11	CRE	Control Return Enable
TP12	ARM	Arm
TP13	FLAG	Flag
TP14	FLAG	Flag

INTEGRATED CIRCUIT POWER AND GROUND PINS AND TOTAL NUMBER OF IC's USED

IC Desig.	Part Description	Total Packages	Unused Device Gates	VCC Pin No.	GND Pin No.
U1,7,13,26,31 32,37 38,44	14503B	9		16	8
U2,8,14,20	14175B	4		16	8
U3,4,9,10 15,16,19,21, 22,27,33,39, 45	14076B	13		16	8
U5,6,11,12, 17,18,23	74LS14N	7		14	7
U24	74LS03	1		14	7
U25,43	DP8304	2		20	10
U28,30,34,36 40,42,46,48	14081	8		14	7
U29,35,41,47	14585B	4		16	8
U49	Cont.Chip	1		40	20
U50	74LS123	1		16	8
U51	74LS09	1		14	7
U52	74LS08	1		14	7
Z3,Z4				9	
Z1,Z2				5	

MANUAL CHANGES
Model 69776A Interrupt Card
Manual HP Part No. 69776-90003

Make all corrections in the manual according to errata below, then check the following table for your card's serial number and enter any listed change(s) in the manual.

SERIAL		MAKE
Prefix	Number	CHANGES
ALL		Errata
2346A	01756-up	1

ERRATA:

On page 2-1, add the following information to the chart in paragraph 2-7b under Write Subaddress 2: "Loads Mask Register."

In Table 3-1, on page 3-2, move the asterisk from Data Type Code 4 to Data Type Code 3.

On page 5-3, add the following information to Table 5-1:

Static shielding bag, HP P/N 9222-0665, qty 1.
Static warning label, HP P/N 7121-0850, qty 1.

CHANGE 1:

The card edge connector has been changed to reduce EMI/RFI interference. When assembling the card edge connector, refer to the assembly instruction sheet (HP P/N 14703-90001) that is shipped with the connector. Disregard the assembly information in the back of this manual.

11/3/83

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