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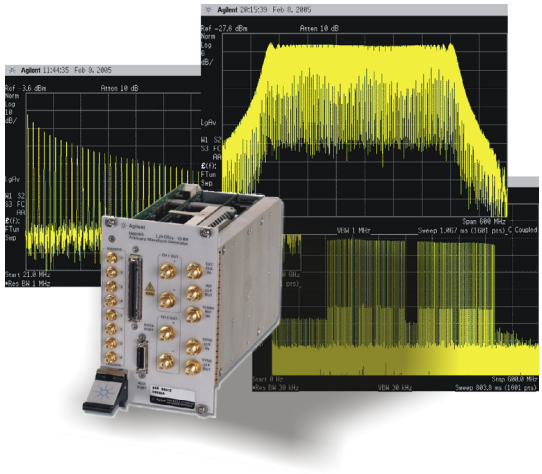
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Agilent N6030A Series
Arbitrary Waveform Generators

User's Guide



Agilent Technologies

Manufacturing Part Number: N6030-90004
Printed in USA
May 2006

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1 Introducing the N6030A Series AWGs

The N6030A Series instruments are wideband arbitrary waveform generators (AWGs) capable of creating high-resolution waveforms for radar, satellite and frequency agile communication systems. Each channel of the N6030A and N6031A AWGs operate at 1.25 GS/s and each channel of the N6032A and N6033A operate at 625 MS/s. The N6030A and N6032A feature 15 bits of vertical resolution and the N6031A and N6033A 10 bits of vertical resolution. The instruments are 4-slot 3U CompactPCI modules that offer dual differential output channels to drive both single-ended and balanced designs.

The AWGs include a complete software suite to speed waveform development and system integration supporting MATLAB®, VEE, LABVIEW, and IVI-C programmatic interfaces. In addition, the following two options are available: Dynamic Sequencing Option 300, on page 85, and Direct Digital Synthesis Option 330, on page 89

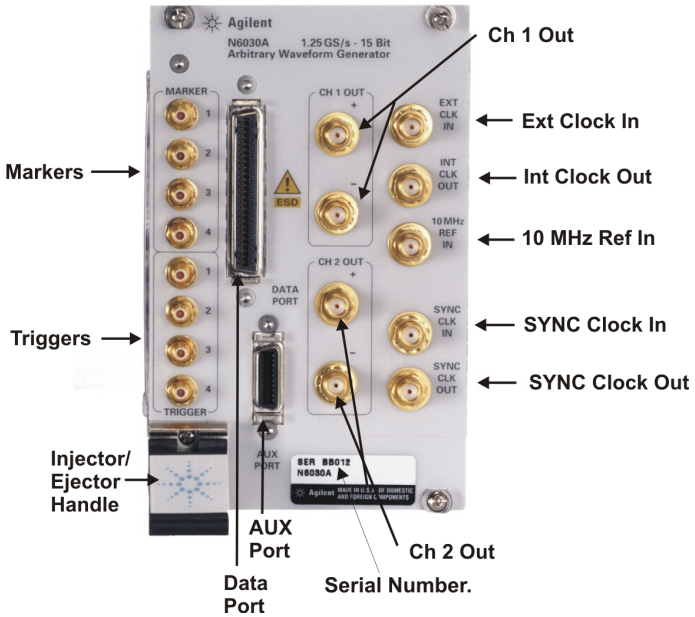
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The N6030A Series Module

Front Panel Interface



MARKER

There are four SMB female marker output connectors that can be used for triggering or system synchronization. The connectors are 3.3V TTL/CMOS 30 ohm series terminated. The output is capable of driving a 50 ohm load.

TRIGGER

There are four SMB female trigger input connectors that are used to control the waveforms in the sequencer and create event-based signal simulation. The connectors support TTL/CMOS, ECL, and PECL logic levels

Injector/Ejector Handle

This handle is used during installation and removal of the AWG module.

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CH 1/CH 2 OUT

The CH 1 OUT and CH 2 OUT positive (+) connectors are used for single-ended operation. Use both the positive (+) and negative (-) connectors for differential operation. Refer to "Signal Conditioning" on page 75 for more information.

DATA PORT

This port is currently inactive and reserved for future applications.

AUX PORT

The AUX port enables Dynamic Sequencing, Option 300.

EXT CLK IN

Use this 50 ohm SMA external clock in connector to input an external sample clock. It will accept clock rates in the range of 100 MS/s through 1.25 GS/s. Refer to "External Clock" on page 61 for more information.

NOTE An error message will appear if the clock rate does not match the hardware setting, or an external clock is not present.

INT CLK OUT

Use this 50 ohm SMA internal clock out connector to route the internal 1.25 GS/s clock to other test instruments or devices.

10MHz REF IN

Use this 50 ohm SMA 10 MHz reference in connector to input an external 10 MHz reference.

SYNC CLK IN/SYNC CLK OUT

These connectors support synchronization of multiple modules. Refer to "Multiple Module Synchronization" on page 78.

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Rear Panel



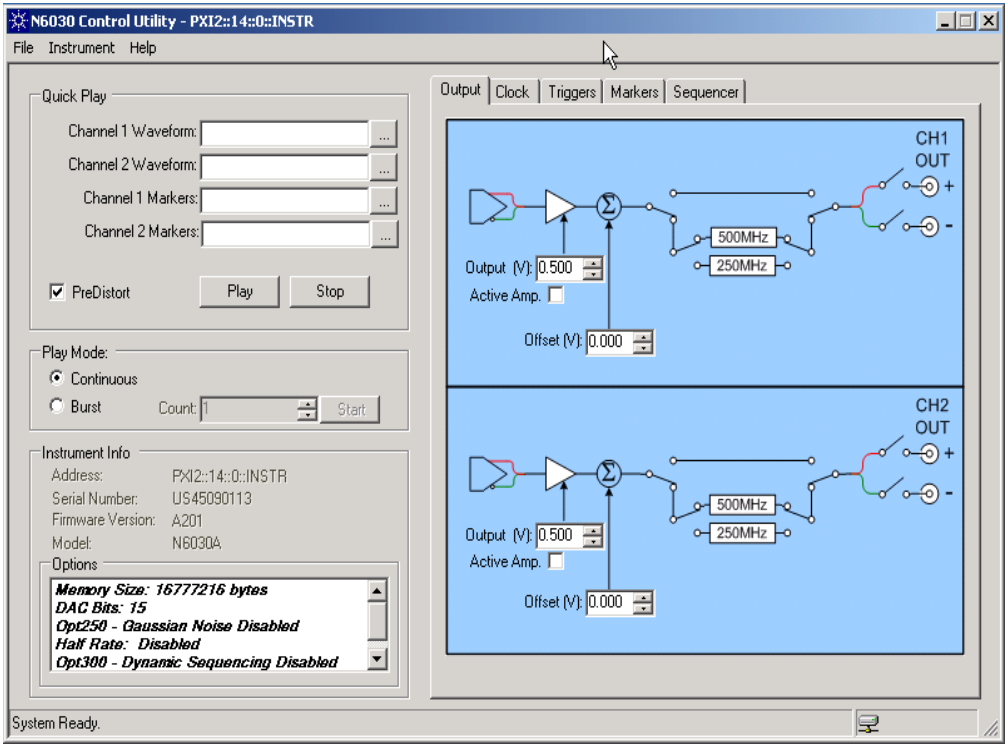
This rear panel connector is inserted into one of the peripheral slots in the backplane of the CompactPCI/PXI chassis.

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Graphical User Interface (GUI)

The tab-based graphical interaction of the GUI gives instant access to the AWG parameters, making it easy to configure signal output. Each tab is labeled with its contents, enabling quick access to all functions. Figure 1-1 displays the first level of the GUI. For more information on the GUI, refer to the N6030A Series Online Help. Access this from the application Help menu, or in Windows: **Start** > **Programs** > **Agilent** > **N6030A** > **Help**.

Figure 1-1 Graphical User Interface



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Getting Started

System Requirements

Hardware

CompactPCI compliant chassis with documentation
CompactPCI compliant embedded controller
or
MXI-4 link with related documentation
Agilent E4440A Spectrum Analyzer or equivalent (system verification)

NOTE The MXI-4 link requires a desktop computer with its documentation and an open PCI slot for the MXI-4 PCI card.

Supported Operating Systems

Windows® 2000, Service Pack 4.0 or later
Windows® XP, Service Pack 2.0 or later

Required Software

Windows.NET® Framework, Version 1.1 Redistributable Package, Service Pack 1 or later (included on the N6030A CD)
IVI Compliance Package Version 2.2 or greater, which includes the IVI Shared Components (download from www.ni.com)

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N6030A Series AWG Installation

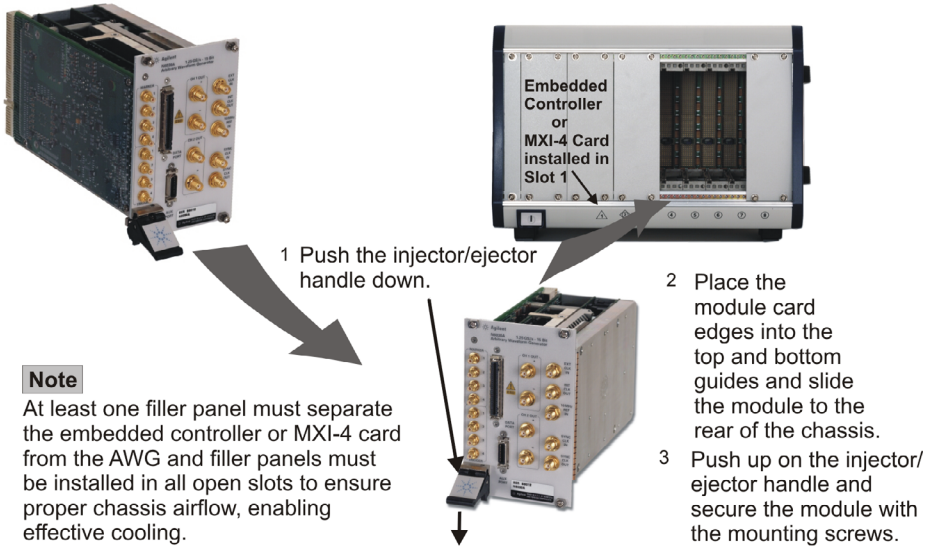
Electrostatic discharge (ESD) can damage the highly sensitive components in your instrument. ESD damage is most likely to occur as the module is being installed or when cables are connected or disconnected. Protect the circuits from ESD damage by wearing a grounding strap that provides a high resistance path to ground. Alternatively, ground yourself to discharge any static charge built-up by touching the outer shell of any grounded instrument chassis before touching the port connectors.

N6030A Series AWG in a Pre-Existing Chassis and Controller

Check the shipment:

- N6030A Series module
- N6030A Series CD
- Quick Start-Installation Guide
- N6030A Series User's Guide
- 128 MB memory stick

Follow the steps in the graphic to install the module in the chassis and then proceed to "Installing the Software" on page 20.



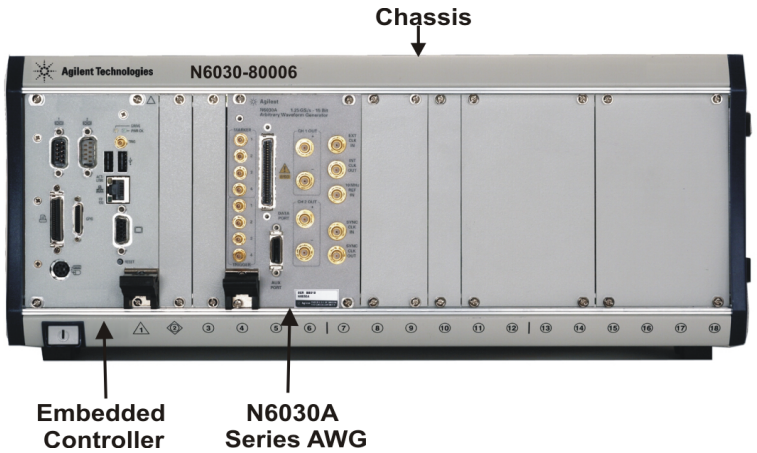
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N6030A Series AWG in a Chassis with an Embedded Controller

Check the shipment:

- chassis
- embedded controller
- N6030A Series module
- N6030A Series CD
- Quick Start-Installation Guide
- N6030A Series User's Guide
- 128 MB memory stick

This configuration is ready to use. The embedded controller, module, and all the software were installed prior to shipment



NOTE At least one filler panel must separate the controller from the AWG. and filler panels must be installed in all open slots to ensure proper chassis airflow. This enables effective cooling.

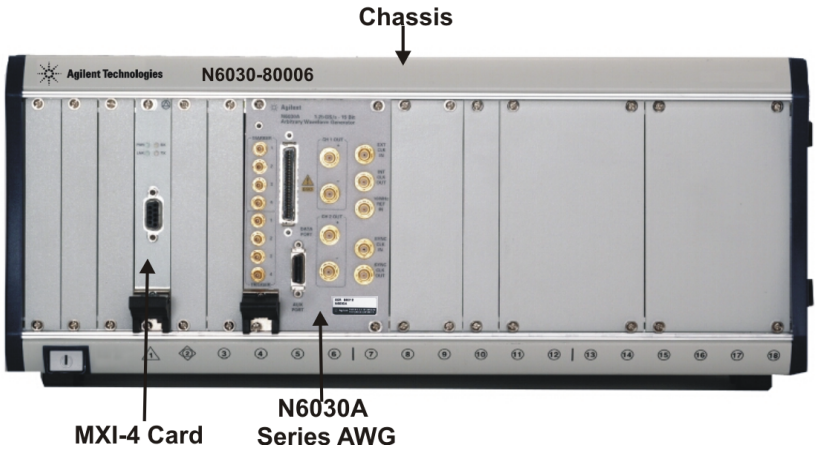
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N6030A Series AWG in a Chassis with a MXI-4 Link

1. Check the shipment.

   chassis
   NI MXI-4 card and cable
   N6030ASeries CD
   Quick Start-Installation Guide
   N6030A Series User's Guide
   NI PXI 1045 documentation
   NI PCI-8331 card (for the computer)
   NI MXI-4 documentation
   128 MB memory stick

2. This configuration ships with the N6030A Series module and MXI-4 card installed in the chassis.



NOTE At least one filler panel must separate the controller from the AWG. and filler panels must be installed in all open slots to ensure proper chassis airflow. This enables effective cooling.

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3. Turn on the PC.
4. Download the IVI Compliance Package, which contains the IVI Engine and the IVI Shared Components.
   Go to: http://www.ni.com/
   Search on **ivi compliance package version 2.2**.
   Select **IVI Compliance Package Version 2.2 for Windows 2000//NT/XP-HWDRIVER-Support-National**
   Follow the instructions for the **Download Process** at the bottom of the page.
5. Install the NI software without the MXI-4 card in the PC.
6. Install the N6030A software from the N6030A CD.
7. Shut down the PC, install the MXI-4 card and attach the cable.
8. Power on the chassis.
9. Reboot the PC.
10. Verify that Plug and Play loads the NI driver, the N6030A driver, and recognizes the MXI-4 card.

Installing the Software

Insert the N6030A Series CD into the CD drive and follow the instructions. The memory stick may also be used for this step on embedded controllers that have no CD drive.

NOTE If the install application fails to come up, navigate to the CD drive or the memory stick and double-click setup.exe.

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Verifying System Operation

System Set Up

Embedded Controller

1. Start with the controller (PC) turned off.
2. Connect the keyboard, mouse, and monitor to the controller front panel interface.
3. Connect the power cord to the chassis and turn the power on.

MXI-4 Link

1. Start with the controller (PC) turned off.
2. Connect the cable from the PCI card in the PC to the connector on the MXI-4 card installed in the chassis.
3. Connect the power cord to the chassis and turn the power on.
4. Turn the PC on.

Waveform Playback

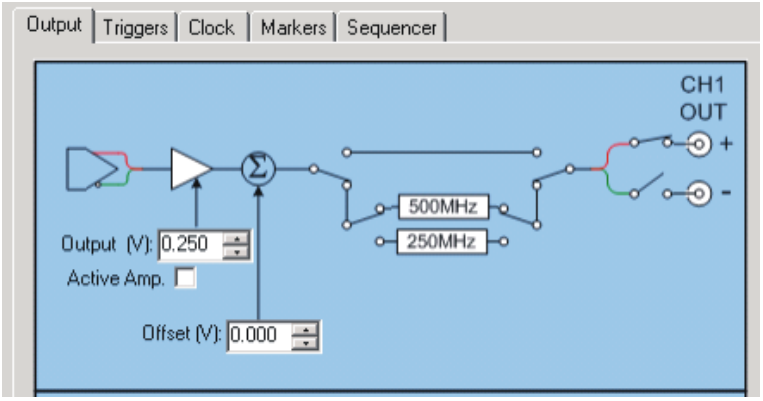
NOTE An Agilent E4440A Spectrum Analyzer or equivalent is required to view the waveforms.

1. Connect a 10 MHz reference to the AWG front panel connector. If you are using a PXI chassis, use the backplane 10 MHz reference.
2. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.
3. Open the user interface by double-clicking the **N6030A Control Utility** icon placed on the desktop during installation.

NOTE If you do not have an icon, go the **Start** > **Programs** > **Agilent** > **N6030A** and select **Control Utility** to open the user interface.

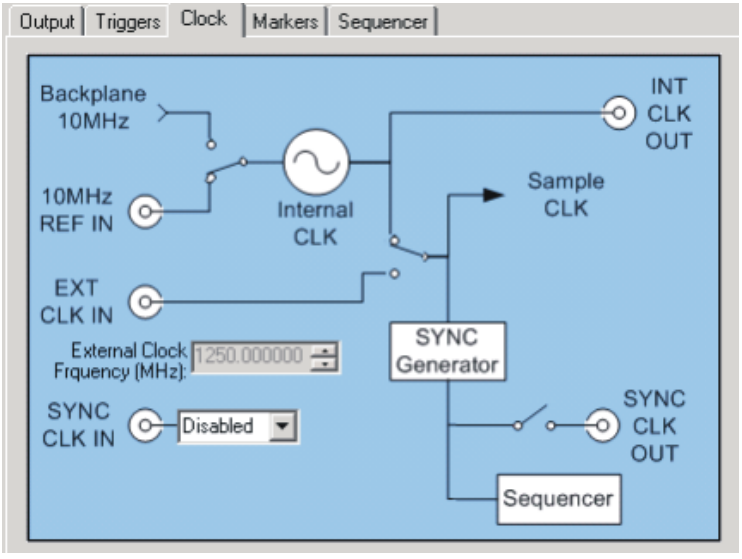
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4. In the **Output** tab, configure the signal conditioning path to include the 500MHz reconstruction filter through CH1 OUT (toggle the switches you want to connect) on channel 1 and channel 2. The connection will



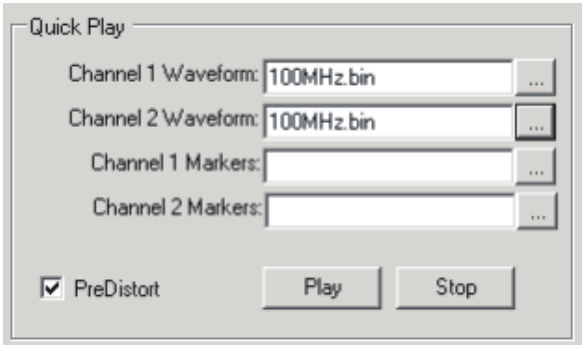
automatically enable differential mode. Click on the negative (-) node to enable single-ended mode. Notice that the Output drops to 0.250 volts.

5. Select the **Clock** tab and configure the internal clock to **10MHz REF IN**. If you are using a PXI chassis, leave the clock set to the default Backplane 10MHz.



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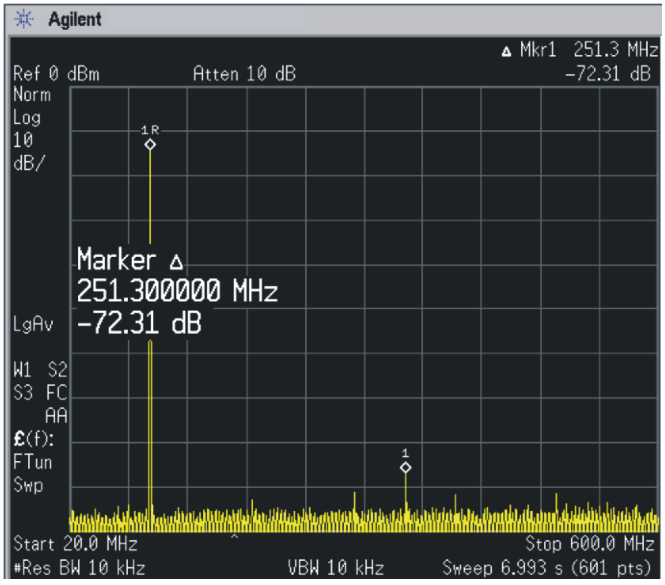
6. In the **Quick Play** section of the user interface, browse and select the **100MHz.bin** waveform file found on the memory stick for channels 1 and 2.



7. Click **Play.**

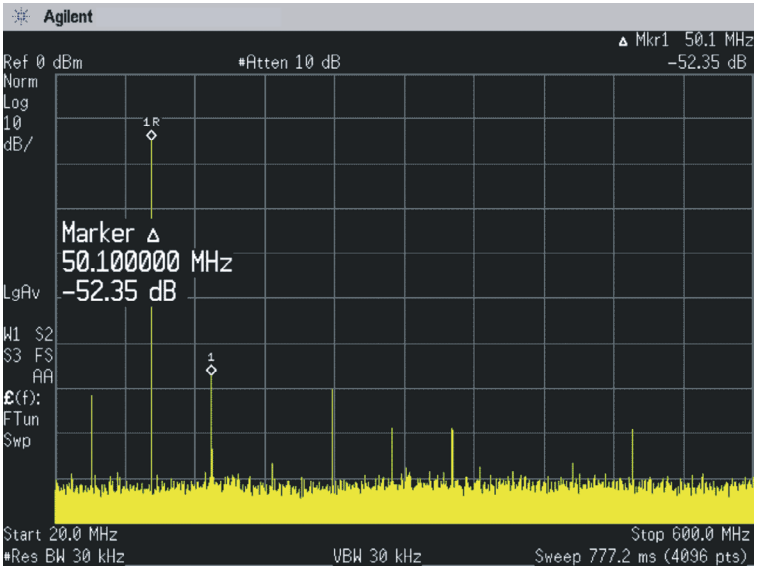
The spectrum analyzer cabled to channel 1 should display a spurious free dynamic range (SFDR) of at least −65 dBc for the N6030Aand N6032A, as shown in Figure 1-2, and a SFDR of at least −50 dBc for the N6031A and N6033A, Figure 1-3.

Figure 1-2 **N6030A and N6032A**



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Figure 1-3 N6031A and N6033A



You should also get an SFDR of at least −65 dBc for the N6030A and N6302A, and at least −50 dBc for the N6031A and N6033A when you connect channel 2 positive (+) to the spectrum analyzer RF input connector.

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Shutting Down the System

1. Close the N6030A Control Utility.
2. Shut down Windows®.
3. When Windows® is completely shut down, power off the chassis.

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Maintenance



To prevent electrical shock, disconnect the instrument and/or system from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.

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2 Basic Operation

This chapter guides you through the basic operation of the AWG. Prior to following these procedures, the N6030A Series module must be installed in a CompactPCI or PXI platform chassis and the N6030A Series software installed on the controller or PC with the installed MXI-4 PCI card. Refer to "Getting Started" on page 16 for complete instructions on how to complete these tasks.

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Using the Graphical User Interface

Generating a Single Tone Signal

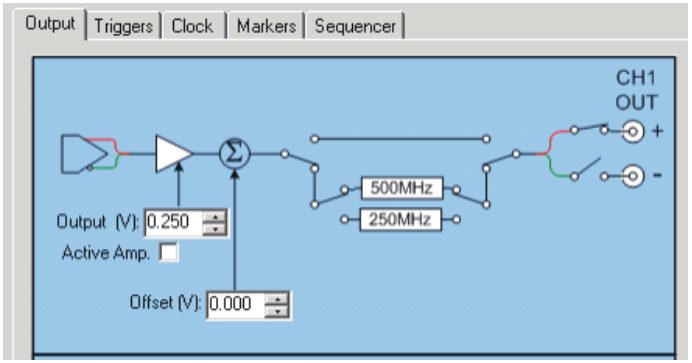
NOTE A spectrum analyzer is required to display the waveforms.

Use the following procedure as a guide to basic single-ended waveform playback with the N6030A Series AWG. All waveform parameters need to be set prior to waveform playback.

1. Connect a 10 MHz reference from the spectrum analyzer to the AWG front panel connector. If you are using a PXI chassis, use the Backplane 10MHz reference.
2. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.
3. Open the user interface by double-clicking the N6030A icon placed on the desktop during installation.

NOTE If an icon was not placed on the desktop, go to:
Start > **Programs** > **Agilent** > **N6030A** > **Control Utility**

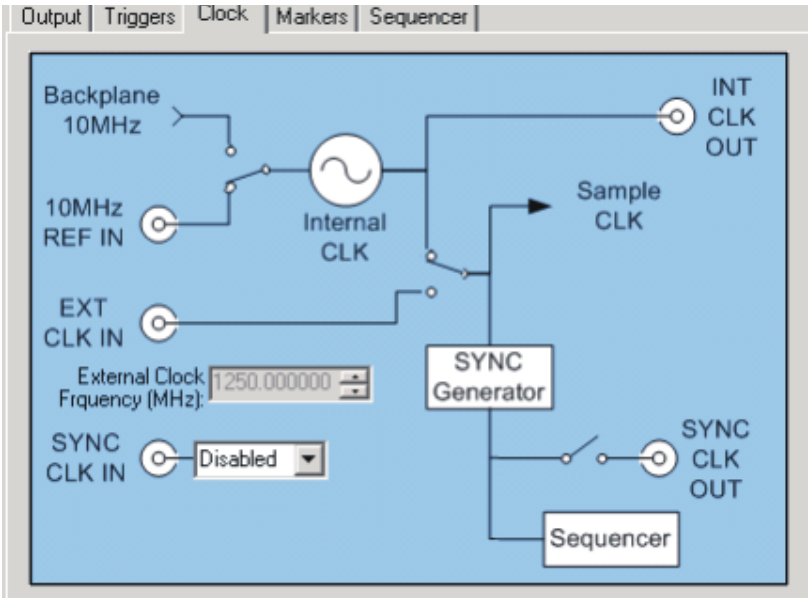
4. Select the **Output** tab and connect a single-ended signal conditioning path to CH1 OUT (+) (click on the node that you want to connect).



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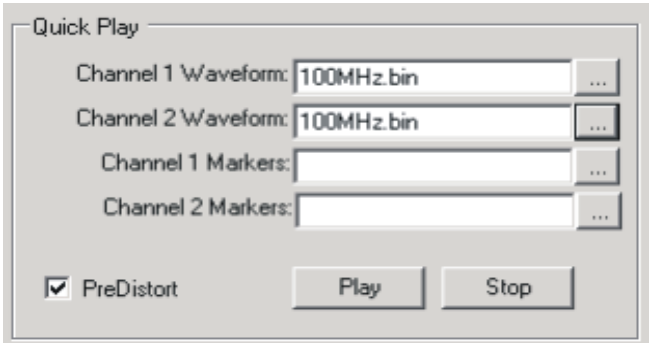
The connection will automatically enable differential mode. Click on the negative (-) node to open this path and enable single-ended mode..Notice that the default gain value was 0.500 volts. Once you select single-ended mode, the value drops to 0.250 volts. These are maximum values for the modes indicated.

5. Select the **Clock** tab and configure the **10MHz REF IN**. For this example, we utilized the 10 MHz reference from the E4440 Spectrum Analyzer in step 1. If you are using a PXI chassis, leave the clock set to the default Backplane 10MHz



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6. In the **Quick Play** section of the user interface, browse and select the desired single tone waveform file for Channel 1 Waveform. The N6030A Series accepts data formatted as 16-bit signed integers ignoring the LSB.



NOTE Different waveforms can be loaded into channel 1 and 2, but the length of the waveforms must be the same.

7. Use the default setting for the play mode and predistortion.
8. Click **Play**.

Figure 2-1 displays a 100 MHz waveform played back on the N6030A or N6032A AWG. The SFDR is greater than −70.0 dBc. Figure 2-2 displays a 100 MHz waveform played back on the N6031A or N6033A AWG. The SFDR is greater than −50.0 dBc.

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Figure 2-1 **N6030A and N6032A**

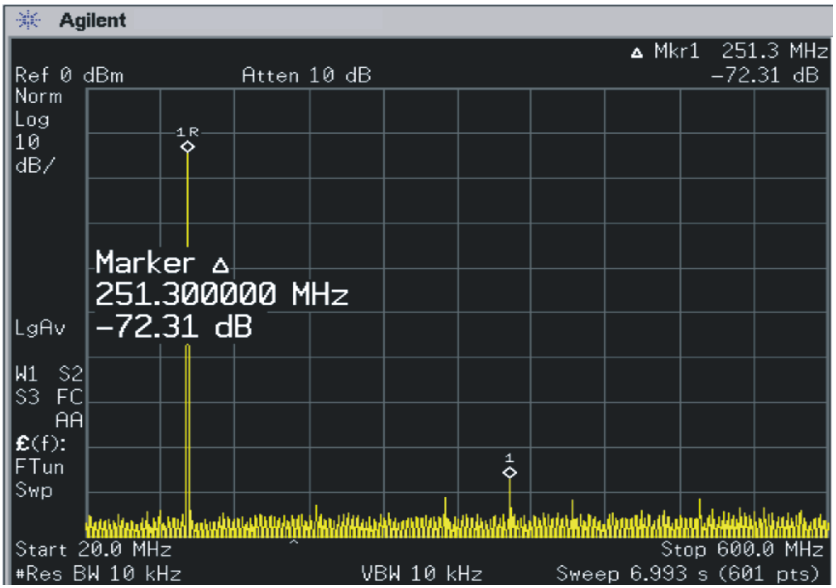
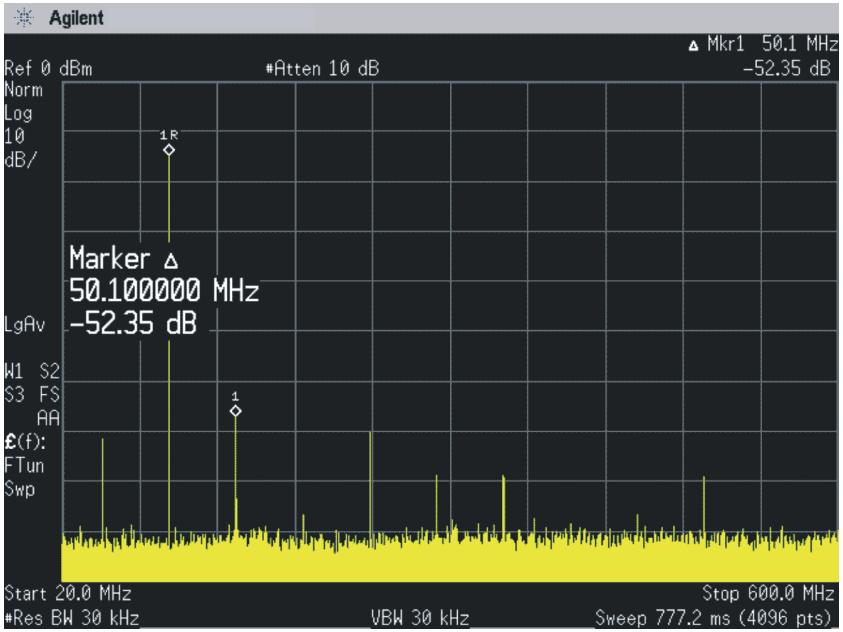


Figure 2-2 **N6031A and N6033A**



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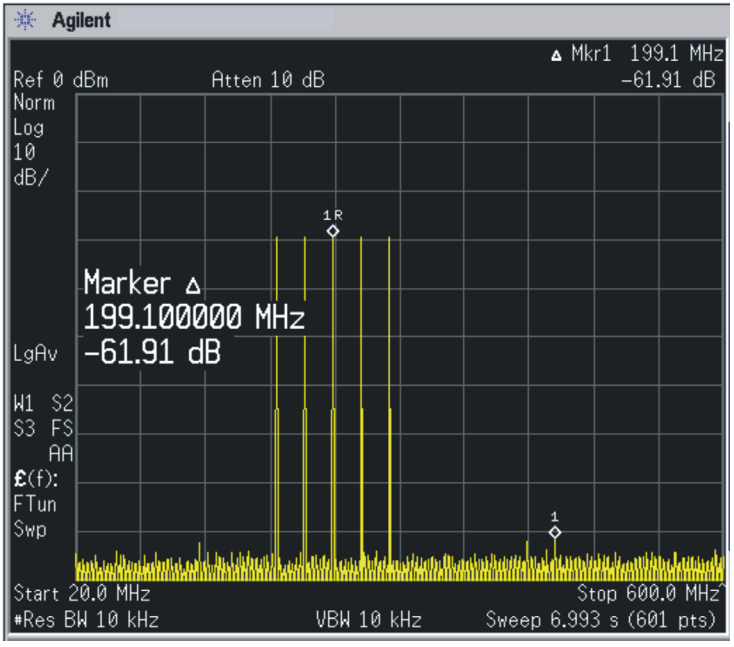
Generating a Multi-tone Signal

Follow steps 1-5 of "Generating a Single Tone Signal" on page 28 to configure the signal path and clock reference.

1. In the **Quick Play** section of the control utility, browse and select the desired multi-tone waveform for channel 1.
2. Use the default setting for play mode and predistortion.
3. Click **Play**.

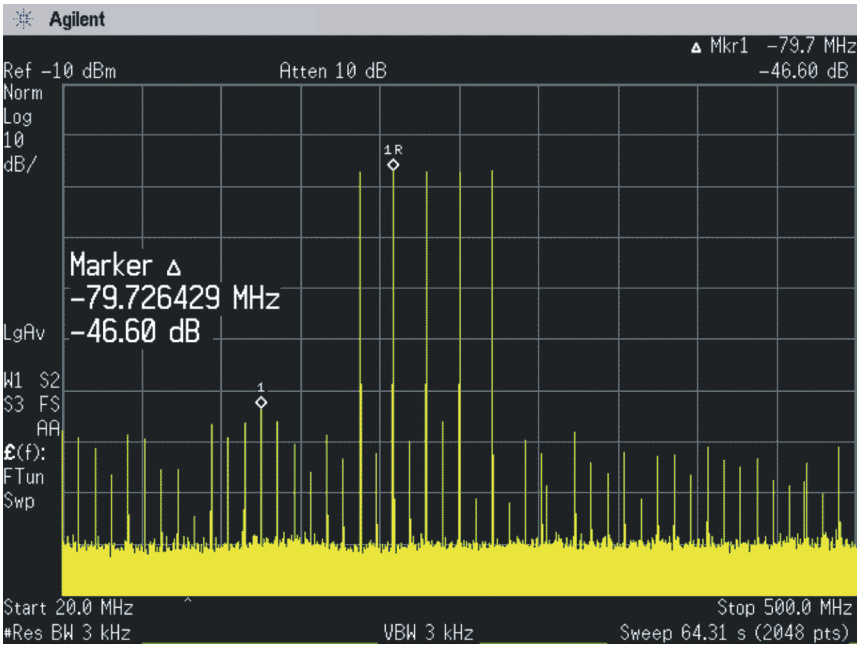
For this example, a waveform with five tones was used. The intermodulation distortion produced by the five tones played back on the N6030A and N6032A is less than 60.0 dB, Figure 2-3. The intermodulation distortion produced by the five tones played back on the N6031A and N6033A is less than 45.0 dB, Figure 2-4.

Figure 2-3 N6030A and N6032A



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Figure 2-4 **N6031A and N6033A**



Creating and Playing a Sequence

Follow steps **1-5** of "Generating a Single Tone Signal" on page 28 to configure the signal path and clock reference.

1. Select the **Sequencer** tab.
2. From the **Segment List** select **Add**. This brings up a **Segment Information** window.
3. Browse and select the **100 MHz** waveform, then click **OK**.

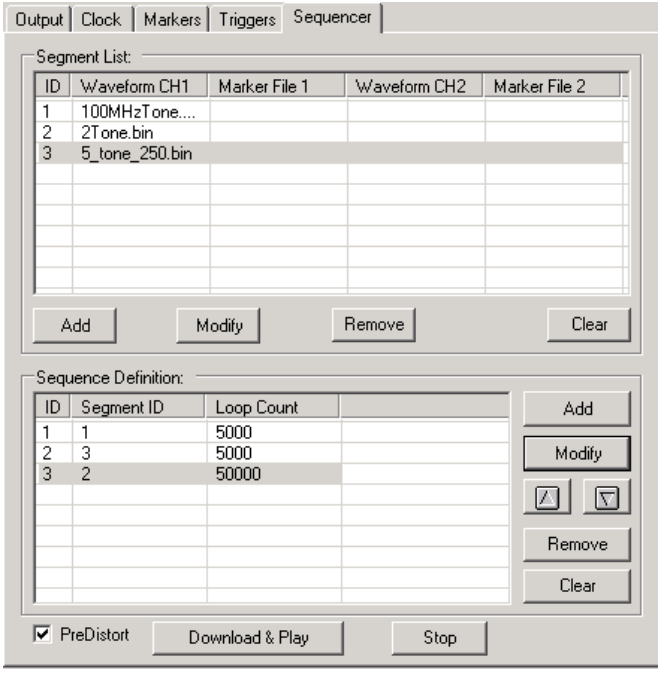
NOTE For dual channel sequencing, add the same waveform to both channel 1 and channel 2. Currently, the software does not support independent channel sequencing.

4. Repeat steps **2** and **3** twice, selecting the **2tone** and **5_tone** waveforms.

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5. In the **Segment List**, select the **100 MHz** waveform.
6. In the **Sequence Definition** area, select **Add**. This will bring up the **Enter Repetition Count** window.
7. Enter **5000** repetitions and click **OK**.
8. Repeat steps **5**, **6**, and **7** for the **2tone** and **5_tone** waveforms.
9. In the **Sequence Definition** area, select **Segment ID 2** and move it below **Segment ID 3** using the down arrow.
10. Click **Modify** and change the count to **50000**. The sequencer tab should look like Figure 2-5.

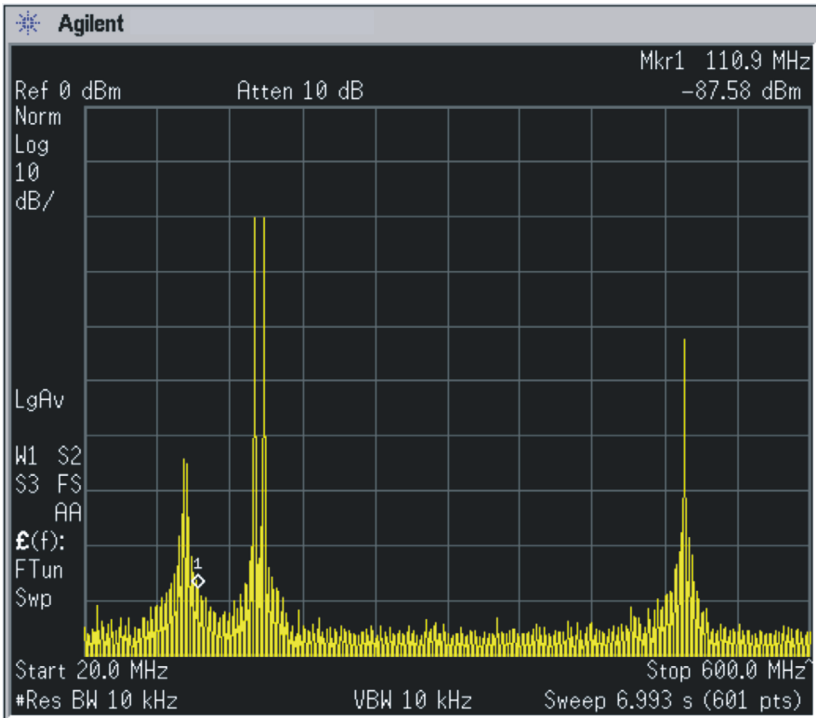
Figure 2-5 Sequencer Tab



11. Click **Download & Play**. The spectrum of the sequence should be similar to the one shown in Figure 2-6.

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Figure 2-6 Playback of a Sequence



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Synchronizing Two N6030A Series Modules

Internal Clock Synchronization Using Continuous Mode

When synchronizing two modules using the internal clock, one unit is designated as the Master and the other unit is designated as the Slave. The Master unit sources the sample clock and the sync clock signals. These signals are split and fed to the synchronized modules (the Master as well as the Slave).

The internal sample clock operates at 1.25 GHz and provides the final retiming of the analog output from each AWG. Any skew in the sample clock cable delays between the modules will result in the same skew in the analog outputs.The sample clock signal is split with a matched passive divider and the cable lengths are matched. The resulting skew is small and repeatable.

Required Equipment

N6030A Series Module

CompactPCI compliant chassis

Embedded controller or NI MXI-4 Link

Cable Kit

SMB Cable Assembly, (3 each)

SMB Adapter Tee M-M-M (1 each)

SMA Cable Assembly, 10 in (4 each

Power Divider, 11636B (2 each)

Customer Furnished Cables

SMA to BNC Cable (2 each, equal length)

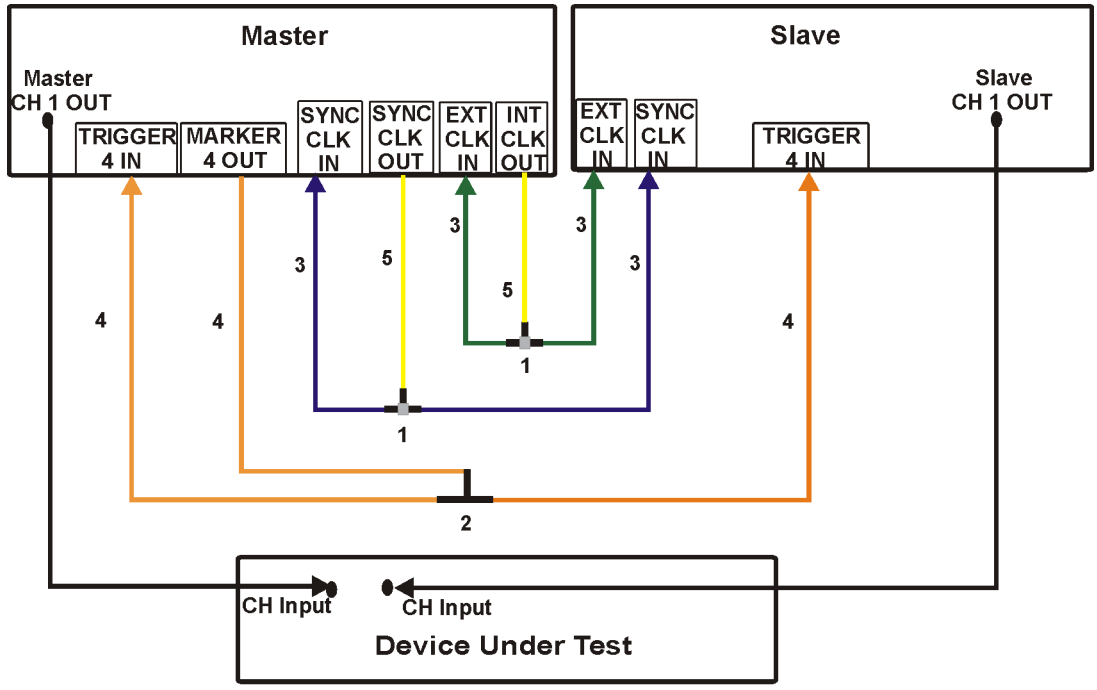
Procedure Using a Software Marker

1. Start with the system turned off.

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2. Cable the equipment as shown in Figure 2-7

Figure 2-7 Cabling for Two Module Synchronization



1 — Power divider
2 — SMB Adapter Tee
3 — SMA Cable Assembly 10 in
4 — SMB Cable Assembly
5 — Adapter

Note: The CH 1 OUT customer furnished cables from the Master and Slave modules must be of equal length.

Turn the system on.

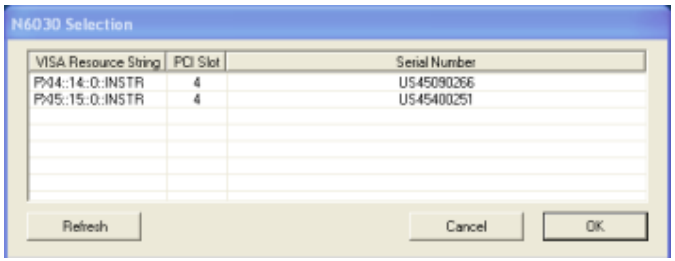
Selecting the Master Unit

1. Open an **N6030A Control Utility** session (double-click the Agilent N6030A icon on the desktop).

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2. Highlight the **Master** unit in the **N6030 Selection** window list and click **OK**.

Figure 2-8 N6030 Selection Window



3. Select the desired signal conditioning path.
4. Select the desired waveform file.
5. Select the **Clock** tab.
6. From the **SYNC CLK IN** drop-down list, select **Master**.

Notice the following changes to the graphical user interface that are automatically configured when the Master unit is assigned:

Clock Tab

the internal clock is no longer driving the sample clock

the sample clock and sync clock out are driven by the external clock in signal

the sync clock in signal communicates with the sequencer

Marker Tab

Marker 4 is assigned to a Software marker and is grayed out

Trigger Tab

Start trigger is assigned to Trigger 4 and is grayed out

Selecting the Slave Unit

1. Open an N6030A Control Utility session (double-click the Agilent N6030A icon on the desktop).

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2. Highlight the **Slave** unit in the **N6030 Selection** window list and click **OK**.
3. Select the desired signal conditioning path.
4. Select the desired waveform file.
5. Select the **Clock** tab.
6. From the **SYNC CLK IN** drop-down list, select **Slave**.

Notice the following changes to the graphical user interface that are automatically configured when the Slave unit is assigned:

Clock Tab

the internal clock is disabled

the sample clock is driven by the external clock in signal

the sync clock out is disabled

the sync clock in signal communicates with the sequencer

Trigger Tab

Start trigger is assigned to Trigger 4 and is grayed out

Initiating Synchronous Playback

1. In the **Quick Play** area of the **Slave** GUI, select **Play**. This arms the waveform playback.
2. In the Q**uick Play** area of the **Master** GUI, select **Play**. This initiates synchronous waveform playback.

NOTE You can view the output on an oscilloscope by setting Marker 1 on the Master module to Waveform Start and cabling the marker output to trigger the oscilloscope.

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Using the Programmatic Interfaces

IVI-C Driver Functionality

The IVI Foundation's class driver specification for function generators has been the model for the features in the N6030A AWG. This includes the recommended method to incorporate attributes for instrument-specific functions.

Please refer to IVI-4.3 IviFgen Class Specification and IVI-3.1 Driver Architecture Specification for more information. These can be found at:

www.ivifoundation.org/Downloads/Specifications.htm.

A set of API Functions and Attributes can be found in the N6030A Help system. Go to:

Start > **Programs** > **Agilent** > **N6030A > Help**

or from the application menu bar

Help > **N6030A Online Help**

MATLAB Interface

MATLAB is one of the programmatic interfaces supported by the N6030A Series AWG. Use the set of API functions to configure and play waveforms with the N6030A module. A complete list of the API functions can be found in the N6030A Control Utility in the Help menu. Go to:

Help > **N6030A Help** > **Programming > MATLAB API**.

To set up MATLAB for connectivity, in your MATLAB software go to:

File > Set Path > **Add with Subfolders...**

navigate to your local drive and go to:

Program Files > **Agilent** > **N6030A** > **Matlab**

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click **OK**, then **Close** the **Set Path** window.

MATLAB can now execute all of the N6030A API functions.

MATLAB Example 1, Creating and Playing a Waveform

```
% N6030 Matlab Interface, Version 1.0
% Copyright (C) 2005 Agilent Technologies, Inc.
%
% A simple example of how to create a waveform,
% open a session to % the Agilent N6030A AWG,
% play the waveform, and close the session.
% Note: the waveform must be configured before
% downloading.
% If settings are changed after downloading the
% waveform, the waveform must be re-downloaded.
% Create a waveform - a sine wave with 2000 pts
% Played at 1250 MHz, this will produce a tone
% of 1.250 MHz

numberOfSamples = 2000;
samples = 1:numberOfSamples;
ch1 = sin( 2 * samples/numberOfSamples * 2*pi);
ch2 = cos( 2 * samples/numberOfSamples * 2*pi);
waveform = [ ch1; ch2 ];

% Open a session
disp('Opening a session to the instrument');
```


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```
[ instrumentHandle, errorN, errorMsg ] =
agt_awg_open('pci','PXI*::*');

if( errorN ~= 0 )

    % An error occurred while trying to open the
session.

    disp('Could not open a session to the
instrument');

    return;

end


disp('Enabling the instrument output');

[ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle, 'outputenabled', 'true');

if( errorN ~= 0 )

    % An error occurred while trying to enable the
output.

    disp('Could not enable the instrument output');

    return;

end


disp('Setting the instrument to ARB mode');

[ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle, 'outputmode', 'arb');

if( errorN ~= 0 )

   % An error occurred while trying to set the ARB
mode.

    disp('Could not set the instrument to ARB
mode');
```


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```
    return;
end


disp('Transfering the waveform to the instrument');
[ waveformHandle, errorN, errorMsg ] =
agt_awg_storewaveform( instrumentHandle, waveform);
if( errorN ~= 0 )
   % An error occurred while trying to transfer the
waveform.
    disp('Could not transfer the waveform to the
instrument');
    return;
end


disp('Initiating playback of the waveform on the
instrument');
[ errorN, errorMsg ] = agt_awg_playwaveform(
instrumentHandle, waveformHandle );
if( errorN ~= 0 )
   % An error occurred while trying to playback the
waveform.
    disp('Could not initiate playback of the
waveform on the instrument');
    return;
end


disp('Press ENTER to close the instrument session
and conclude this example.');
```


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```
pause;


agt_awg_close( instrumentHandle );

disp('Session to the instrument closed
successfully.');
```


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MATLAB Example 2, Synchronizing Two AWG Modules

```
MATLAB Example 2, Synchronizing Two AWG Modules

% N6030 Matlab Interface, Version 1.12
% Copyright (C) 2005 Agilent Technologies, Inc.
%
% This example initiates dual module synchronized
% waveform playback.
%
% Use agt_awg_browse to identify the modules.
%
% Create a waveform - a sine wave with 2000 pts
% Played at 1250 MHz, this will produce a tone of
% 1.250 MHz
numberOfSamples = 2000;
samples = 1:numberOfSamples;
ch1 = sin( 2 * samples/numberOfSamples * 2*pi);
ch2 = cos( 2 * samples/numberOfSamples * 2*pi);
waveform = [ ch1; ch2 ];

% Try to open a session

disp('Opening a session to the instrument');

    [instrumentHandle2, errorN, errorMsg ] =
agt_awg_open('pci','PXI1::10');

        if errorN ~= 0

            disp(errorN);

            disp(errorMsg);

            disp('program stopped');

            return;

        else

            disp('ok');

        end
```


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```
    [instrumentHandle1, errorN, errorMsg ] =
agt_awg_open('pci','PXI1::15');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end

disp('Enabling the instrument output');
    [ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle1, 'outputenabled', 'true');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end

    [ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle2, 'outputenabled', 'true');
        if errorN ~= 0
            disp(errorN);
```


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```
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end


disp('Setting the instrument to ARB mode');
    [ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle1, 'outputmode', 'arb');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return;
        else
            disp('ok');
        end


    [ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle2, 'outputmode', 'arb');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
```


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```
        else
            disp('ok');
        end


disp('Setup the Master');
    [ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle1, 'syncmode', 'master');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


disp('Setup the Slave');
    [ errorN, errorMsg ] = agt_awg_setstate(
instrumentHandle2, 'syncmode', 'slave');
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('proram stopped');
            return
        else
            disp('ok');
```


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```
        end


disp('Transfering the waveform to the instrument');
    [ waveformHandle, errorN, errorMsg ] =
agt_awg_storewaveform( instrumentHandle1,
waveform);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


    [ waveformHandle, errorN, errorMsg ] =
agt_awg_storewaveform( instrumentHandle2,
waveform);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end
```


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```
disp('Initiating playback of the waveform on the
instrument');
    [ errorN, errorMsg ] = agt_awg_playwaveform(
instrumentHandle2, waveformHandle );
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end

    [ errorN, errorMsg ] = agt_awg_playwaveform(
instrumentHandle1, waveformHandle );
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end

disp('Init Generation');
    [ errorN, errorMsg ] =
agt_awg_initiategeneration(instrumentHandle2);
```


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```
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


    [ errorN, errorMsg ] =
agt_awg_initiategeneration(instrumentHandle1);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end


disp('Press ENTER to close the instrument session
and conclude this example.');
pause;
disp('Abort Generation');
    [ errorN, errorMsg ] =
agt_awg_abortgeneration(instrumentHandle2);
        if errorN ~= 0
```


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```
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end
    [ errorN, errorMsg ] =
agt_awg_abortgeneration(instrumentHandle1);
        if errorN ~= 0
            disp(errorN);
            disp(errorMsg);
            disp('program stopped');
            return
        else
            disp('ok');
        end
agt_awg_close( instrumentHandle1 );
agt_awg_close( instrumentHandle2 );


disp('Session to the instrument closed
successfully.');
/rc = AGN6030A_close(session);
return 0;
}
```


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C/C++ Example Program

```
/* Example for programming the N6030A IVI-C driver.

This will compile and link into a working .EXE
file.

For Compile: Add include path = C:\Program
Files\IVI\include,

C:\vxipnp\winnt\include

For Link: Add libpath = C:\Program
Files\IVI\Lib\msc,

Add lib = AGN6030A.lib

Opening a session with predistortion enabled
(default) creates a discrepancy for the waveform in
ch2 since predistortion is applied twice; once when
it was downloaded to ch1 and again when it is
downloaded to ch2.

You can eliminate this problem by turning off the
predistortion before downloadingnthe waveform to
ch2. An alternative is to clone the waveform to
another file name. For example, clone Wfm_ch1 to
Wfm_ch2.

*/

#include <math.h>

#include <windows.h>

#include <winbase.h>

#include <AGN6030A.h>

// #include "stdafx.h"   // if you use Microsoft
Visual
// Studio you might use this

#define WFM_LENGTH 800  //should be integer
divisible by 16
```


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```
.int main(int argc, char* argv[])

{

ViStatus rc;

ViRsrc resourceName = "PXI4::10::INSTR"; // Set
this to
// match your hardware

ViBoolean IDQuery = VI_FALSE;

ViBoolean resetDevice = VI_TRUE;

ViSession session = 0;

ViInt32 wfmHandle1;

ViInt32 wfmHandle2;

int i;

double twopi;

double if Wfm[WFM_LENGTH];

double Fsig = 500e6; // Set this to a CW frequency
// <= 500 MHz

double Fs = 1.25e9; // Sample Clock Frequency

// Initialize N6030A and setup session handle

rc = AGN6030A_init(resourceName, IDQuery,
resetDevice, &session);

if ( rc != VI_SUCCESS )

return -1;

// Setup some Channel 1 states

// Set to single-ended operation, filter on,
// 500 MHz filter selected

rc = AGN6030A_ConfigureOutputConfiguration(session,
"1", AGN6030A_VAL_CONFIGURATION_SINGLE_ENDED,

VI_TRUE, 500e6);
```


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```
if ( rc != VI_SUCCESS )

return -1;
// Set output to ON

rc = AGN6030A_ConfigureOutputEnabled(session, "1",
VI_TRUE);

if ( rc != VI_SUCCESS )

return -1;

// Do the same for Channel 2

rc = AGN6030A_ConfigureOutputConfiguration(session,
"2", AGN6030A_VAL_CONFIGURATION_SINGLE_ENDED,

VI_TRUE, 500e6);

if ( rc != VI_SUCCESS )

return -1;

rc = AGN6030A_ConfigureOutputEnabled(session, "2",
VI_TRUE);

if ( rc != VI_SUCCESS )

return -1;

// Select the Internal Sample Clock and an
//External Reference Clock

rc = AGN6030A_ConfigureSampleClock(session,
AGN6030A_VAL_CLOCK_INTERNAL, Fs);

if ( rc != VI_SUCCESS )

return -1;

// This uses the front panel 10MHz REF IN
connection.

// To use the PCI backplane clock, substitute
// AGN6030A_VAL_REF_CLOCK_PXI

rc = AGN6030A_ConfigureRefClockSource(session,
AGN6030A_VAL_REF_CLOCK_EXTERNAL);
```


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```
if ( rc != VI_SUCCESS )

return -1;

// Enable or disable built-in N6030A corrections.
// Default is enabled.  This attribute is not
available in // release 1.00.

/* rc = AGN6030A_SetAttributeViBoolean(session,
NULL, AGN6030A_ATTR_PREDISTORTION_ENABLED,

VI_TRUE);

if ( rc != VI_SUCCESS )

return -1;

*/
/ Build a sample waveform for testing.
// This produces a CW tone at Fsig Hz.

twopi = 8.0 * atan( 1.0 );

for ( i = 0; i < WFM_LENGTH; i++ )

{

ifWfm[i] = sin( twopi * (Fsig/Fs) * (double)i );

}

// Set N6030A output mode to ARB in preparation of
// downloading and playing our waveform.

rc = AGN6030A_ConfigureOutputMode(session,
AGN6030A_VAL_OUTPUT_ARB);

if ( rc != VI_SUCCESS )

return -1;

// Download the waveform to both channels 1 and 2
even if 2 // is not used.  This is a requirement of
the N6030A at
// this time and must be followed!!  To do this,
call
// the function twice and discard the second
```


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```
// waveform handle if Channel 2 is not used.

rc = AGN6030A_CreateArbWaveform(session,
WFM_LENGTH, ifWfm, &wfmHandle1);

if ( rc != VI_SUCCESS )

return -1;

rc = AGN6030A_CreateArbWaveform(session,
WFM_LENGTH, ifWfm, &wfmHandle2);

if ( rc != VI_SUCCESS )

return -1;

// Configure N6030A to play downloaded waveforms.

// Set to 250 mV gain and 0V offset.

rc = AGN6030A_ConfigureArbWaveform(session, "1",
wfmHandle1, 0.250, 0.0);

if ( rc != VI_SUCCESS )

return -1;

rc = AGN6030A_ConfigureArbWaveform(session, "2",
wfmHandle2, 0.250, 0.0);

if ( rc != VI_SUCCESS )

return -1;

// Close the open session
```


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3 Theory of Operation

The N6030A Series instruments are wideband arbitrary waveform generators (AWGs) capable of creating high-resolution waveforms for radar, satellite and frequency agile communication systems. Each channel of the N6030A and N6031A AWGs operate at 1.25 GS/s and each channel of the N6032A and N6033A operate at 625 MS/s. The N6030A and N6032A feature 15 bits of vertical resolution and the N6031A and N6033A 10 bits of vertical resolution. The instruments are 4-slot 3U CompactPCI modules that offer dual differential output channels to drive both single-ended and balanced designs.

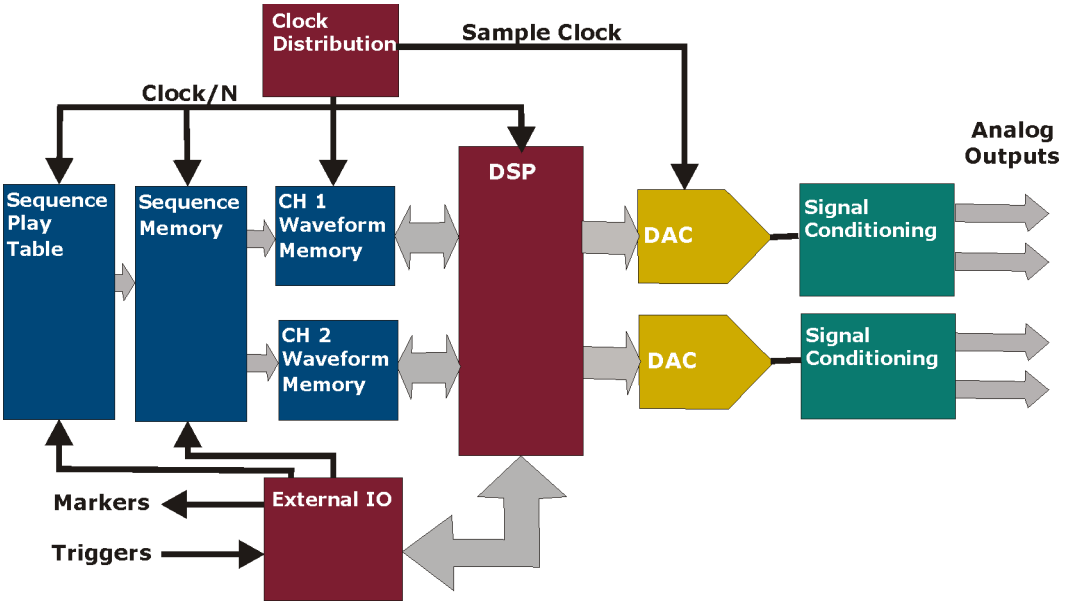
The AWGs include a complete software suite to speed waveform development and system integration supporting MATLAB®, VEE, LABVIEW, and IVI-C programmatic interfaces. In addition, the following two options are available: "Dynamic Sequencing Option 300" on page 85, and "Direct Digital Synthesis Option 330" on page 89.

N6030A Series Block Diagram 60
Clock I/O 60
Waveform Playback 61
Basic Sequencing 62
Advanced Sequencing 64
Markers 70
Triggers 72
Synchronous Triggers 73
Signal Conditioning 75
Digital Predistortion 77
Multiple Module Synchronization 78

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Theory of Operation

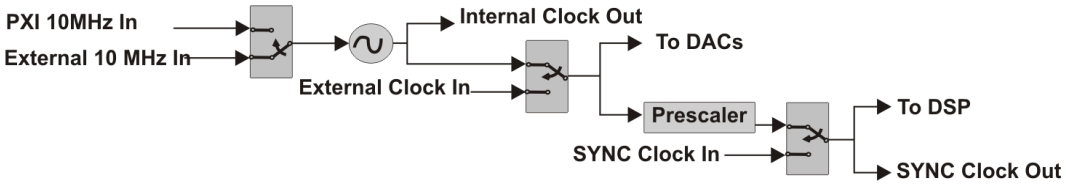
N6030A Series Block Diagram



N is the Sync clock prescaler divide ratio. Refer to Synchronous Triggers.

Clock I/O

External 10 MHz In



A 10 MHz reference is required when using the internal clock.

The Backplane 10 MHz is only available when using a PXI chassis. Compact PCI typically do not have a 10 MHz backplane reference.

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Internal Clock

The high-performance 1.25 GHz oscillator provides the internal sample clock for the module.

External Clock

An external sample clock can be input through the EXT CLK IN connector. The external sample rate must be between 100 MS/s and 1.25 GS/s. To achieve the optimal signal performance on the N6030A analog output, use an external clock with a phase noise floor below -155 dBc/Hz and a power setting of approximately 0 dBm.

NOTE An error message will appear if the clock rate does not match the hardware setting, or an external clock is not present.

Internal Clock Out

The 1.25 GS/s low noise internal sample clock is output through the INT CLK OUT connector and routed to other AWGs or test equipment.

SYNC Clock In/SYNC Clock Out

The SYNC CLOCK IN and SYNC CLOCK OUT are used for the synchronization of multiple modules. Refer to "Synchronization Using an Internal Clock" on page 78 and "Synchronization Using an External Clock" on page 79.

Waveform Playback

Waveforms

Single waveforms are played back in one of two modes:

- **Continuous**
  The waveform repeats indefinitely.
- **Burst**
  Once a trigger is received, the waveform repeats a specified number of times.

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Waveform Sequencer Function

Sequencing provides a method of waveform memory compression using a play table, sequencer memory, and waveform memory. The sequencer controls how waveforms are accessed and performs the following functions:

- determines the order of play for waveforms stored in memory
- enables the construction of long waveforms from shorter or repeated segments
- responds to external triggers
- offers several modes of segment advance
- outputs markers

Sequencer Memory

The sequencer memory contains instructions on how to play through the waveform memory. It can hold up to one million segments (waveforms with a specified loop count).

Waveform Memory

The waveform memory contains Channel 1 and Channel 2, and output marker data.

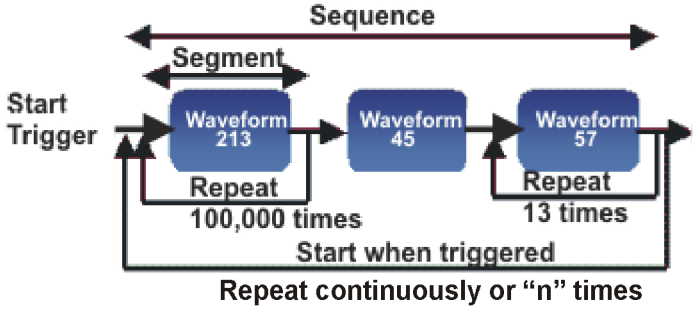
Basic Sequencing

A sequence is a sequential list of segments and may occur anywhere in the sequence memory.

The waveform playback of each channel is directly controlled by the sequencer. The sequencer supplies the memory pointers necessary to create analog signals from the digital data stored in memory. In addition, the sequencer provides the capability to create sequences made of multiple waveform segments. This is helpful when constructing long waveforms with repeating segments. A long waveform might consist of repetitive data that can be stored as single segments and repeated in the sequencer. This extends the waveform play time achievable with the available memory.

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Figure 3-1 **Sequence Example**



NOTE Basic sequencing can be done using the software Control Utility GUI or through the programatic interfaces.

The N6030A Control Utility GUI only supports basic sequencing. Advanced sequencing features can only be accessed through the programatic interfaces.

Playback

There are two playback modes for basic sequencing:

- **Continuous**
  The sequence repeats indefinitely or until an stop trigger is received.
- **Burst**
  The sequence is repeated a predefined number of times. This mode requires a start trigger.

A total of 32,768 unique waveform sequences can be defined. Segments have a minimum length of 128 samples and a granularity of 8 samples. A sequence must contain at least one segment and can have up to a maximum number of 1 million (2^{20}-8) segments. Each waveform segment is played out according to its segment definition. Each segment can be configured to repeat over 1 million times (2^{20}). After the last segment loop is executed, the entire sequence can repeat continuously or for the predefined burst count.

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Advanced Sequencing

NOTE Advanced sequencing is only available through the programatic interfaces.

Advanced sequencing enables the grouping of sequences into scenarios in a way that is similar to how segments are grouped in sequencing. With scenarios you gain more control of waveform playback.

Scenario Pointer Source

A scenario handle is written to by the host processor that addresses scenarios. The handle can be written to at any time including while a scenario is playing. A valid Start trigger or Jump trigger starts the scenario specified by the handle.

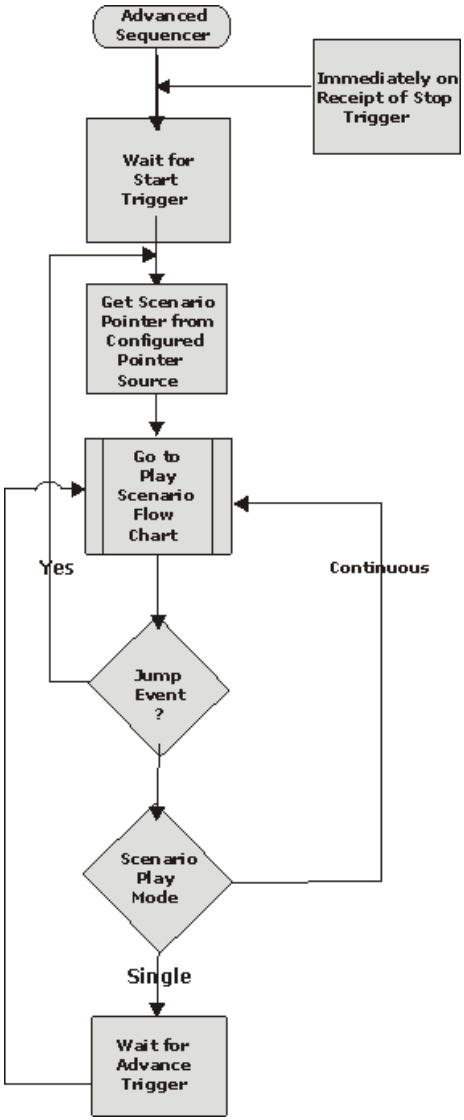
.Scenario Advance Mode

The AWG can be configured to play a scenario once or continuously after starting.

- **Single**
  The scenario plays once and then waits for an advance trigger. While waiting for a trigger, the value of the last waveform continues to play. After receiving an advance trigger, the scenario is then played again.
- **Continuous**
  The scenario repeats indefinitely until it is stopped or a scenario jump trigger is received.

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Figure 3-2 Advanced Sequencer Flow Chart



Waveform Advancement

In basic sequencing, waveforms always advance to the next waveform automatically after the specified number of repetitions. With advanced sequencing, waveforms can be configured to advance in one of four ways.

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- **Automatic**
  The waveform automatically advances to the next waveform after completing the specified number of loop repetitions.
- **Continuous**
  The waveform is played continuously until a waveform jump trigger is received. After a trigger is received, waveform playback completes before advancing to the nest segment. The waveform loop repetition count is ignored.
- **Single**
  The waveform plays once and waits at the end of the waveform playback for a trigger. The waveform is played for each trigger until the number of waveform loop repetitions is met. The next trigger will advance to the next waveform. When the waveform loop repetition count is one, a single trigger will advance to the next waveform. While waiting for a trigger, the last value of the waveform loop continues to play.
- **Repeat**
  The waveform plays repeatedly until the number of waveform loop repetitions is met, then waits for a trigger. The next trigger will advance to the next waveform.

Scenario Jump Mode

The scenario jump mode determines how the AWG responds to a scenario jump input. A scenario jump has very predictable behavior. There are three types of jump modes:

- **Immediate**
  The scenario starts or jumps immediately (with latency).
- **End of Waveform**
  The current waveform, including repeats, is completed before jumping to the new scenario.
- **End of Scenario**
  The current scenario is completed before jumping to the new scenario.

Scenario Start/Jump Trigger Source

It is possible to start a scenario, or to jump to a new scenario using one of

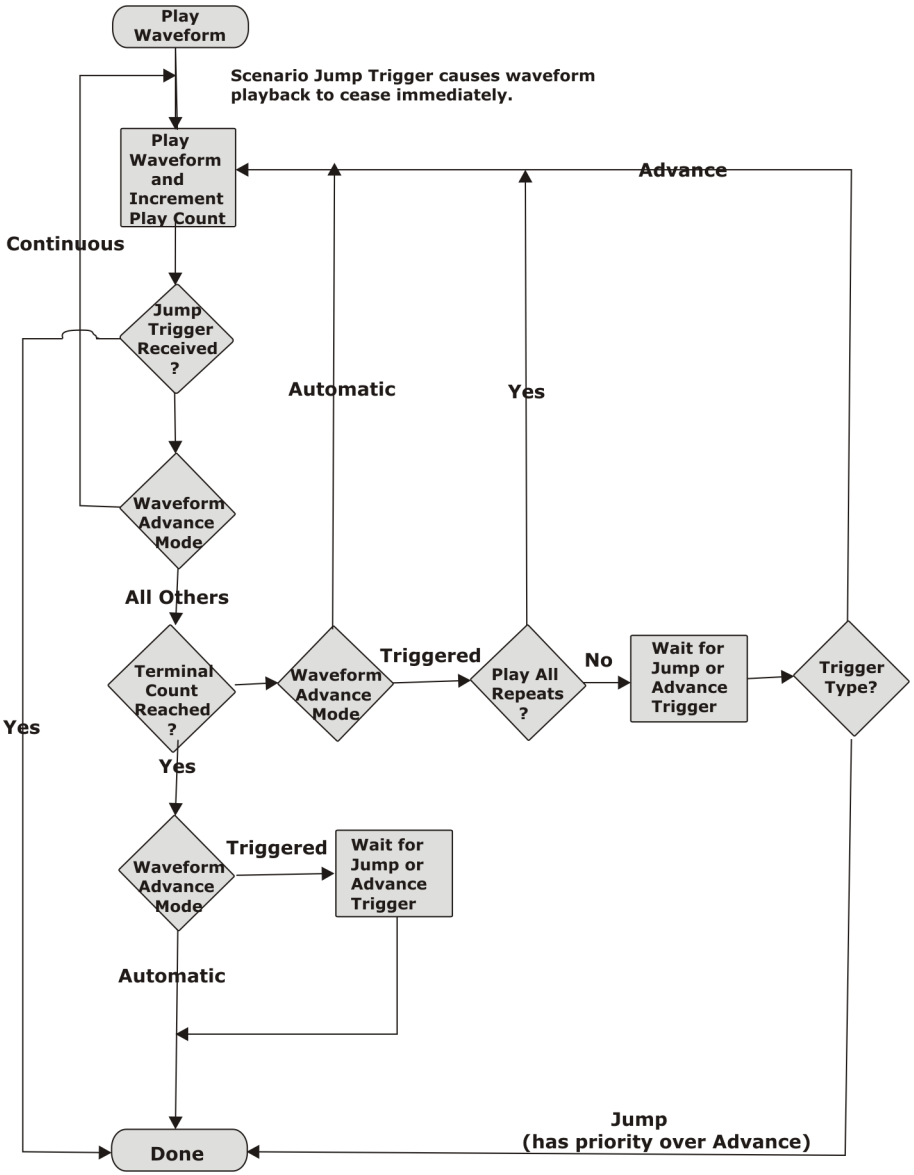
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five inputs. There are four external trigger inputs and a host trigger source. The host trigger source is a register in the play table that can be written to by the host processor. The host processor provides the user a way to start the scenario, or create a jump event. The latency for a scenario jump is established by the jump mode.

Refer to Figure 3-3, “Waveform Play Flow Chart,” on page 68, and Figure 3-4, “Scenario and Sequence Play Flow Charts,” on page 69.

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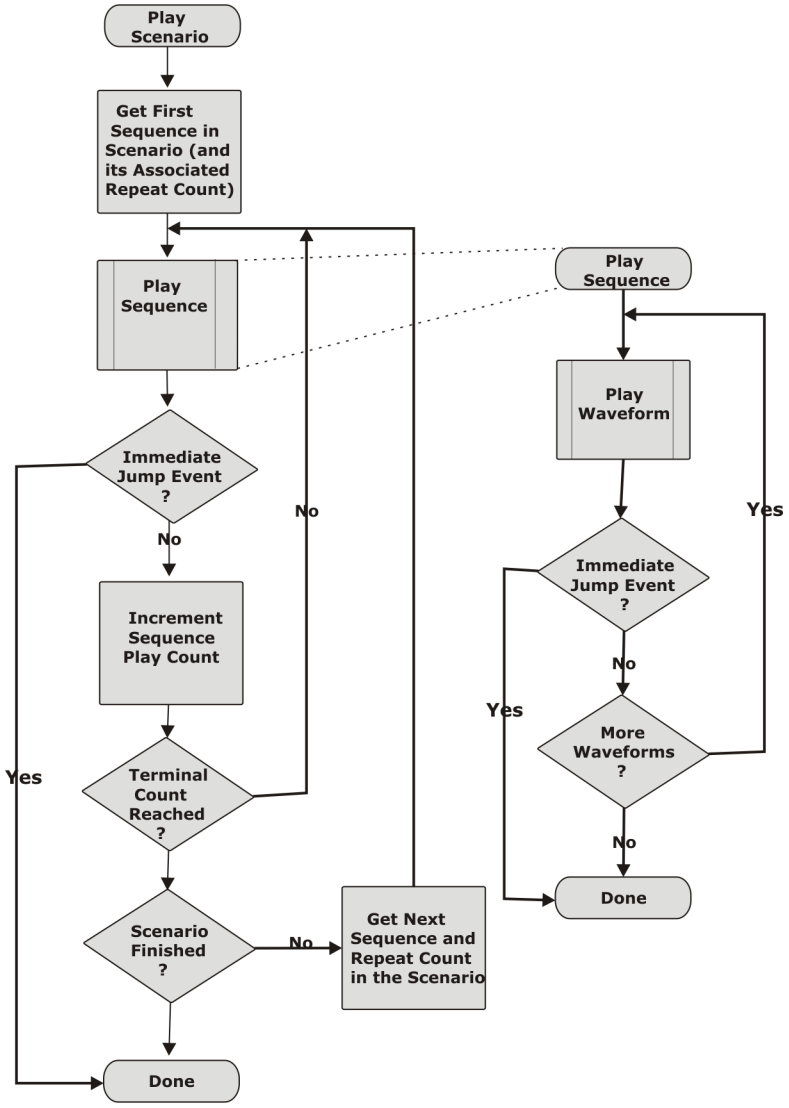
Figure 3-3 Waveform Play Flow Chart



The Jump Trigger condition is satisfied either by a waveform jump event, or by a scenario jump trigger event when the scenario jump mode is set to “End of Waveform.”

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Figure 3-4 Scenario and Sequence Play Flow Charts



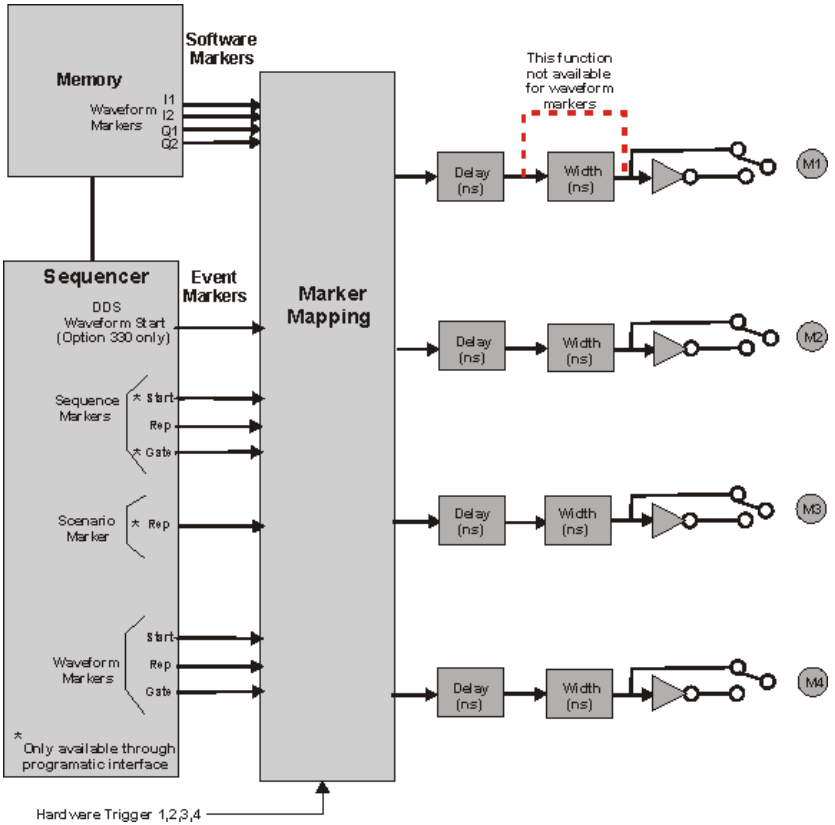
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Markers

The N6030ASeries modules provide four marker output connectors that can be used for system synchronization and triggering. The following markers can be enabled:

- Ch 1 Memory Marker 1 and Memory Marker 2
- Ch 2 Memory Marker 1 and Memory Marker 2
- Waveform Start, Repeat, and Gate
- Sequence Start, Repeat, and Gate
- Scenario Repeat
- Software
- Hardware Trigger 1-4
- DDS Waveform Start (Option 330 only)

Figure 3-5 **Marker Block Diagram**



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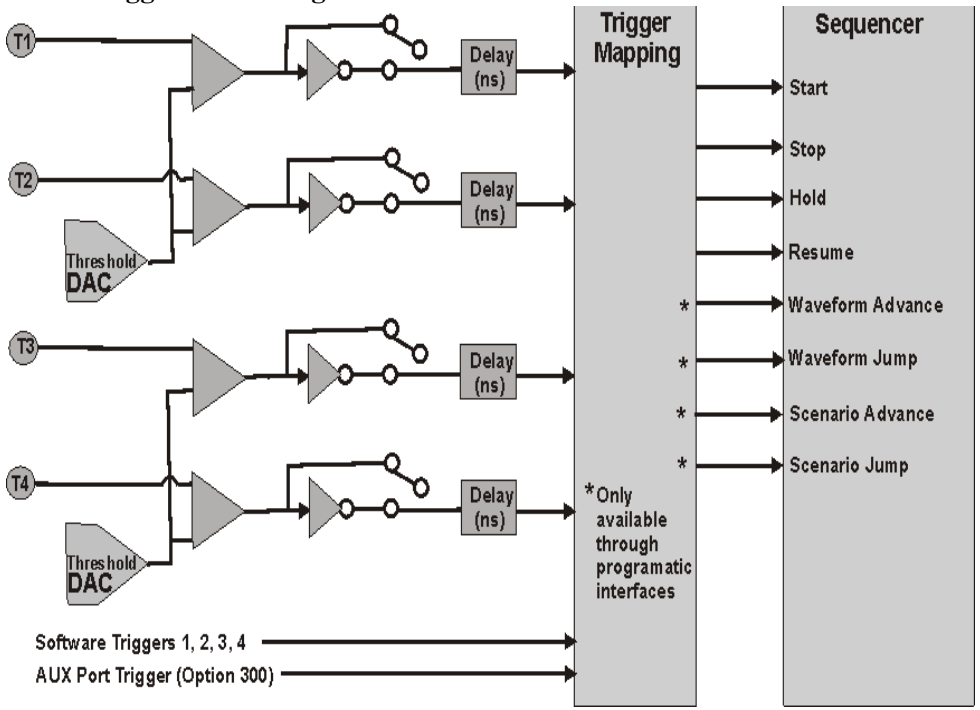
Marker outputs are aligned with the analog output of the AWG.Marker. Markers can be set in the sequencer to be at any point in the data with a positive or negative polarity. Marker widths, except those derived from waveform memory, can be set in increments of the SYNC clock (-8 to 247 clocks). The marker delay function uses the input value to calculate the delay to the nearest 1/4 SYNC clock cycle. The sequencer is capable of outputting nine markers, which can be multiplexed to the four marker outputs. The Sequence Start, Sequence Gate, and Scenario Repeat markers are only available through the programatic interfaces.

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Triggers

The N6030A Series AWGs have four trigger inputs that can be used to control waveforms in the sequencer. Hardware trigger inputs may be configured to generate events on the rising or falling SYNC clock edges, but not both at the same time. The trigger threshold can be set between -4.5 and +4.5V. Ports 1 and 2 have a common threshold, and ports 3 an 4 have a common threshold. These two common thresholds are not shared and can be set independently.

Figure 3-6 Trigger Block Diagram



Trigger delays can be set in increments of the SYNC clock (0-255 clocks).

The trigger input can be configured to initiate the following events through the software Control Utility:

- **Start**
  Starts playback at the beginning of the waveform

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- **Hold**
  Holds at the end of the waveform
- **Stop**
  Stops playback
- **Resume**
  Resumes playback at the point in the waveform that play was held or stopped

The Waveform Advance, Scenario Advance, Waveform Jump, and Scenario Jump triggers are only available through the programatic interfaces.

Synchronous Triggers

01Triggers are registered into the N6030A Series AWGs using the SYNC clock. The SYNC clock is nominally at the sample clock frequency divided by 8. However, at lower sample rates an internal variable modulus prescaler selects other binary divide ratios: 8, 4, 2, and 1. In general, the SYNC clock frequency is always in the range of 78.13 MHz to 156.25 MHz. The input clock frequency ranges and prescaler divide ratios are as specified in Table 3-1:

Table 3-1 Synchronous Triggers

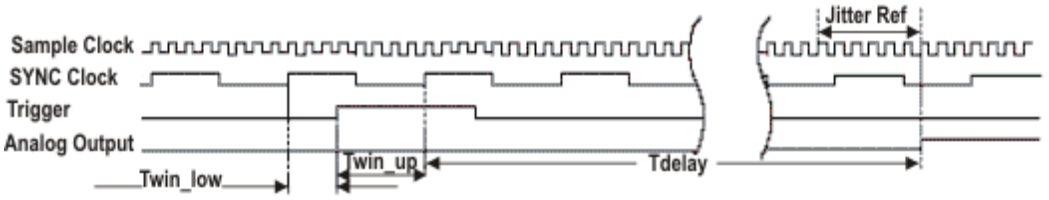
Sample Clock Frequency	SYNC Clock Prescaler Divide Ratio
625 MHz - 1.25 GHz	8
312.5 MHz – 625 MHz	4
156.25 MHz – 312.5MHz	2
100 MHz – 156.25 MHz	1

It is necessary to insure that the correct timing relationships are achieved to guarantee consistent synchronous trigger operation. The trigger input must occur within a valid window with respect to the SYNC clock. The window is specified by two times: Twin_low —the minimum trigger delay after the prior SYNC clock edge; and Twin_up — the minimum trigger setup before the next SYNC clock edge. These are specified for the trigger input relative

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to the SYNC clock output. The trigger must be a minimum of two SYNC clock cycles long. The trigger timing is specified relative to the rising edge of the SYNC clock. The analog output from the AWGs is then produced a fixed number of sample clock cycles (plus a small fixed propagation delay) after the first rising edge of the SYNC clock after the trigger goes active. Since the analog output is retimed by the sample clock, the reference for jitter measurements is the sample clock, as shown in Figure 3-7.

Figure 3-7 Synchronous Trigger Timing Diagram



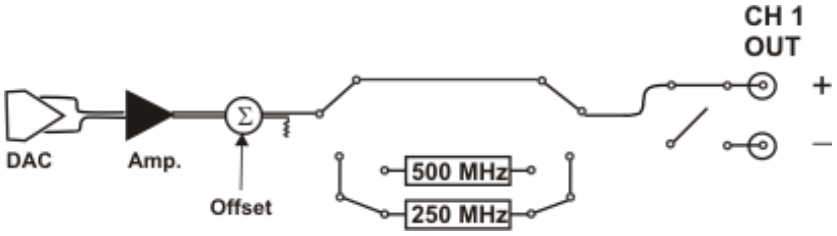
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Signal Conditioning

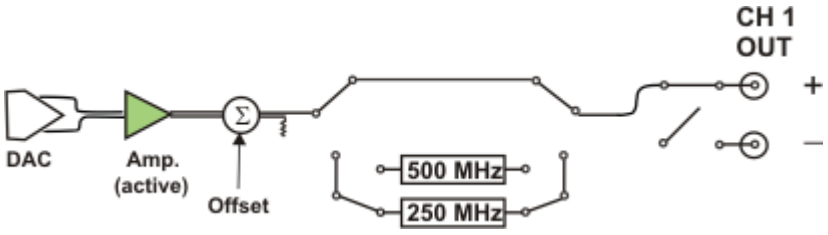
Single-Ended Mode

Single-ended mode has two modes of operation with signal output through the positive (+) port. The negative port (-) is reserved for differential mode.

Passive mode has an adjustable output level of up to 0.5Vp-p
This mode gives the greatest single-ended signal fidelity because there is a balun in the path that suppresses the second order harmonic.

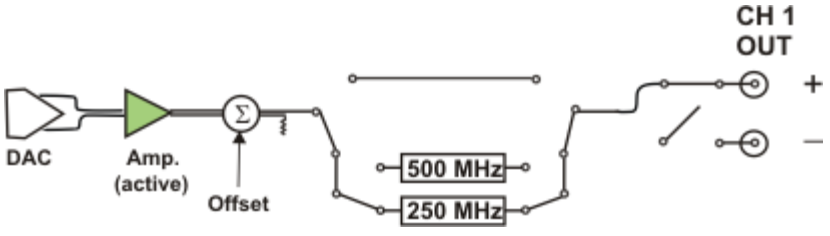


Active mode has an output level of up to 1.0Vp-p and +0.2Vp-p offset range



when the amplifier is activated
The active mode trades off signal fidelity for an increase in signal power.

There are two internal reconstruction filters, 250 MHz and 500 MHz, that can be inserted in the signal path of either mode.

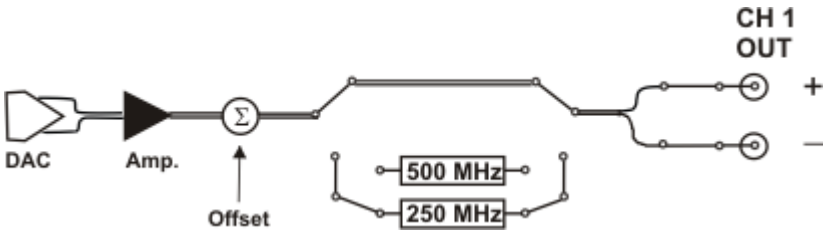


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Differential Mode

The differential mode has an output level of up to 0.5Vp-p. This mode provides exceptional signal fidelity into true differential inputs (which provide common mode rejection). A larger differential output voltage is also obtained without the use of the amplifier. To preserve signal purity, the active amplifier cannot be used in differential mode. Differential mode is not recommended when driving single-ended loads since the second order distortion is degraded. If you choose to drive single-ended loads, you must terminate the negative (-) port of the channel with a 50 ohm load.

Adjustable output voltage and offsets as well as reconstruction filters can be used in differential mode



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Digital Predistortion

The predistortion function compensates for the variation in the magnitude of the output response as a function of frequency. This variation is the result of the sin x/x (sinc) roll-off of the internal DAC and the frequency response of the reconstruction filter. The correction method uses filters to level the amplitude response and to create a linear phase response at the front panel of the AWG. This precess attenuates the signal as a function of frequency, but cannot increase the signal above the maximum output voltage. Therefore, it is necessary to attenuate the lower frequency signals. This results in a reduced output voltage and dynamic range at all frequencies, but with uniform response across the full frequency range.

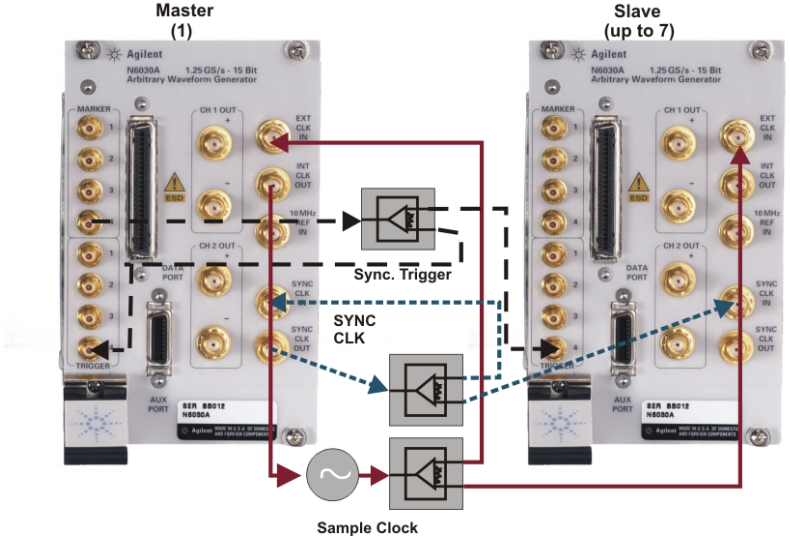
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Multiple Module Synchronization

Within each N6030A series AWG, the two channels are synchronized by design. Some systems, such as phased array radar, require more than two synchronized channels. The N6030A series AWGs are designed to support the synchronization of up to 16 channels through the use of eight AWGs. Synchronization of multiple modules can be achieved using either the internal clock or an external clock.

Synchronization Using an Internal Clock

In synchronizing multiple modules using the internal clock, one unit is designated as the Master and the other units are designated as Slave units. The Master unit sources the
following signals: Sample clock, SYNC clock, and the Sync Marker. These signals are all split and fed to each of the synchronized modules (the Master as well as the Slaves).



The internal sample clock is at 1.25 GHz. The sample clock provides the final retiming of the analog output from each AWG. Any skew in the sample clock cable delays between the multiple modules will result in the same skew in the analog outputs. Typically, the sample clock signal is split with a matched passive splitter and the cable lengths are matched to better than 5

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mm. The resulting skew is small and repeatable. If desired, the skew can be measured and calibrated (along with any phase shifts in cables on the AWG outputs) by adding fixed delay offsets to the waveforms.

The SYNC clock is used internal to the AWG to clock the internal data generator and to clock in the synchronous triggers. When using the internal clock, the SYNC clock has a frequency of 1/8th the sample clock rate (156.25 MHz). When synchronizing multiple units, the SYNC clock output must be enabled in software (in the Master) and the external SYNC clock input selected in all the modules. The SYNC clock signal is split passively and distributed with low skew. The SYNC clock output level and the input sensitivity support up to a 1 to 8 split (fan-out) using matched 50 Ohm splitters (6 dB loss per 1 to 2 splitter). There is a specific SYNC cable length that is required as a function of the sample clock frequency. Several different lengths can be used, provided they are integer multiples of one half of a SYNC clock period.

The trigger cables should all be the same length. The trigger inputs are high impedance and several inputs can be driven in parallel without matched passive splitters. The synchronous trigger timing can be determined in the same way as any synchronous trigger into the AWG. The timing is specified relative to the SYNC clock out. This is easily observed on the slave modules, where the SYNC clock out is unconnected.

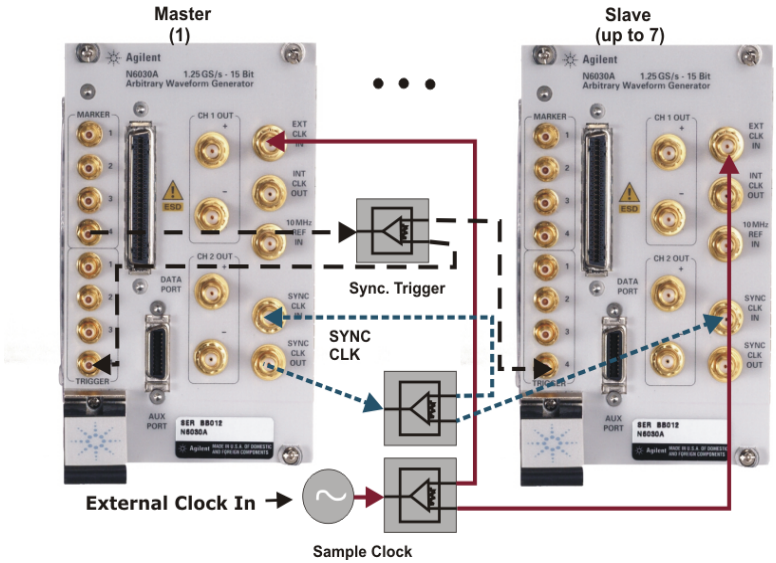
The multiple AWGs are configured to have an internal start trigger to begin play. A software start marker event is used to initiate the synchronized play. Marker 4 and Trigger 4 are used for this purpose.

Synchronization Using an External Clock

In synchronizing multiple modules using an external clock, one unit is designated as the Master and the other units are designated as Slave units. The external clock is split with low skew and distributed to all units. The Master unit sources the following signals: SYNC clock, and the Sync Marker. These signals are all split and fed to each of the synchronized

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modules (the Master as well as the Slaves)



The external Sample clock can be in the range of 625 MHz to 1.25 GHz. The Sample clock provides the final retiming of the analog output from each AWG. Any skew in the Sample clock cable delays between the multiple modules will result in the same skew in the analog outputs. Typically, the sample clock signal is split with a matched passive splitter and the cable lengths are matched to better than 5 mm. The resulting skew is small and repeatable. The skew can be measured and calibrated, along with any phase shifts in cables on the ARB outputs, by adding fixed delay offsets to the AWG waveforms. The SYNC clock is used internal to the AWG to clock the internal data generator and to clock in the synchronous triggers. When using the internal clock, the SYNC clock has a frequency of 1/8 of the sample clock rate (156.25 MHz). When synchronizing multiple units, the SYNC clock output must be enabled in software (in the Master) and the external SYNC clock input selected in all the modules. The SYNC clock signal is split passively and distributed with low skew. The SYNC clock output level and the input sensitivity support up to a 1 to 8 split (fan-out) using matched 50 Ohm splitters (6 dB loss per 1 to 2 splitter). There is a specific SYNC cable length that is required as a function of the Sample clock frequency. Several different lengths can be used, provided they are integer multiples of one half of a SYNC clock period.

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Multiple Module Synchronous Trigger Timing

Triggers are registered into the N6030A using the SYNC clock. The SYNC clock is nominally at the sample clock frequency divided by 8. However at lower sample rates an internal variable modulus prescaler selects other binary divide ratios: 8, 4, 2, and 1.

Table 3-2 SYNC Clock Frequency Ranges

Frequency Range	SYNC Clock Prescaler Divide Ratio
625 MHz-1.25 GHz	8
312.5 MHz-625 MHz	Multi-Module Synchronization
156.25 MHz-312.5 MHz	Not Supported
100 MHz-156.25 MHz	

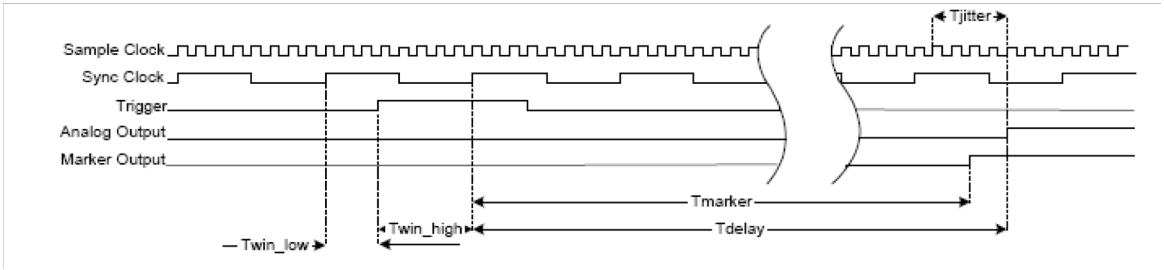
Multiple ARB synchronization is only supported in the 625 MHz – 1.25 GHz frequency range. The input clock frequency ranges and prescaler divide ratios are as specified in Table 3-2.It is necessary to insure that the correct timing relationships are achieved to guarantee consistent synchronous trigger operation. The trigger input must occur within a valid window with respect to the SYNC clock. The window is specified by two times: Twin_low -- the minimum trigger delay after the prior SYNC clock edge; and Twin_high -- the minimum trigger setup before the next SYNC clock edge. These are specified for the trigger Input relative to the SYNC clock Output. The trigger must be a minimum of two SYNC clock cycles long. The trigger timing is specified relative to the rising edge of the SYNC clock by default, as shown in Figure 3-8. To guarantee proper synchronous trigger operation with arbitrary length cables, it is possible to configure the trigger inputs to register the trigger event with respect to the falling edge of the SYNC clock, under software control. In this way there is always a setting for the trigger input timing which will operate reliably for any chosen cable. The typical specifications for the trigger window using the internal clock at 1.25 GS/s is (these values will vary at other clock frequencies):

Twin_high > 3.4 ns

Twin_low > -2.8 ns (the trigger can occur slightly before the prior SYNC clock edge)

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Figure 3-8 Multiple Module Synchronous Trigger Timing Diagram



Cable Length and Skew

The cabling requirements are as follows:

Sample Clock

Skew less than 10 mm between modules. The absolute SYNC cable length is given by the following formula as a function of the Sample clock frequency:

Equation 3-1 Sample Clock Skew Formula 1

$$Length = [(n \times 686 \times (1250MHz)/f) - 394]$$

Expressed in millimeters, where n is an arbitrary integer and f is the sample clock frequency in MHz.

It should be noted that n is the number of 1/2 SYNC clock cycles of total delay between the modules.

This can also be expressed in terms of delay:

Equation 3-2 Sample clock Skew Formula 2

$$Cabledelay = \lceil (n \times 3.29 \times (1250MHz)/f) - 1.89 \rceil$$

Expressed in nanoseconds, where n is an arbitrary integer and f is the sample clock frequency in MHz.

For the external Sample clock the formulas apply over the frequency range of 625 MHz to 1.25 GHz

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Marker and Trigger Cables

The Marker Out to Trigger In cable should be less than 305 mm (12 in). With the
1.25 GHz internal clock, the trigger is falling edge triggered.

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4 Dynamic Sequencing Option 300

The dynamic sequencing option enables you to access up to eight thousand previously stored scenarios through a 16-bit interface. This functionality gives you the ability to build custom signal scenarios to simulate dynamically changing environments.

Dynamic Sequencing 86

AUX PORT Connector 86

Signal Levels 88

Signal Descriptions 88

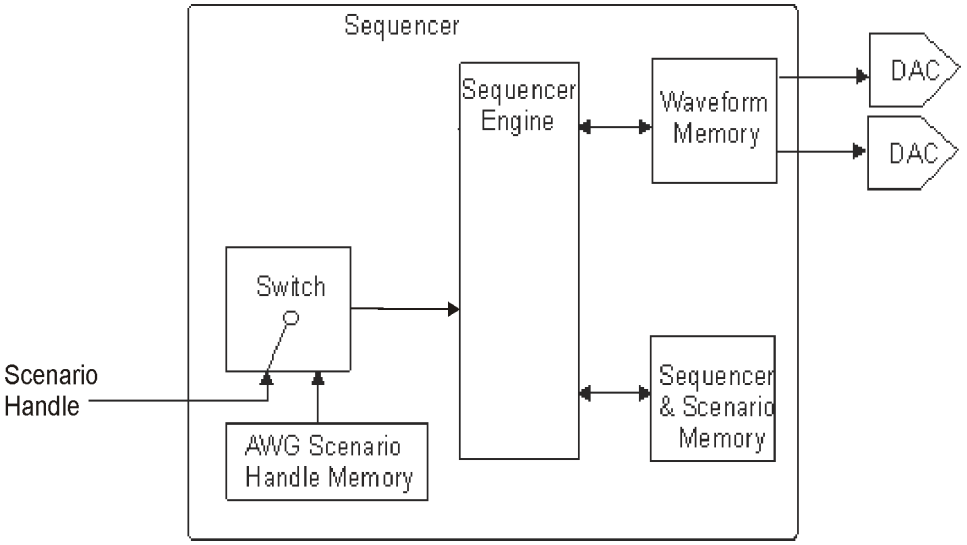
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Dynamic Sequencing

Dynamic sequencing is a mode where the AWG scenario handle memory is bypassed and scenarios are selectedfrom an external source. You must first load the data into the N6030A AWG memory, then, in real-time, provide the scenario handles through the AUX PORT input connector.

NOTE The dynamic sequencing option is only available through the programmatic interfaces since it operates in the advanced sequencing mode that is not available through the Control Utility. Refer to "Advanced Sequencing" on page 64.

Figure 4-1 Dynamic Sequencing Block Diagram



AUX PORT Connector

Description:	Receptacle, Mini D
Number of Contacts:	20
Manufacturer:	3M
Part Number:	10220-0210EC

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Figure 4-2 AUX PORT Pin Outs

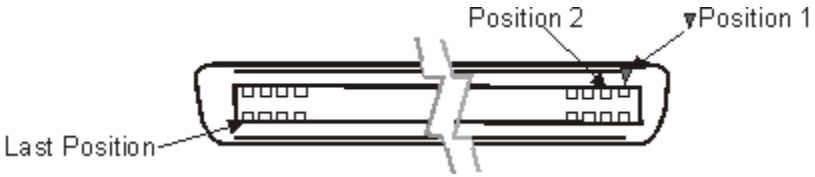


Table 4-1 Pin Assignment

Pin No.	Signal Assignment
1	Trigger
2	Ground
3	Data Valid
4	CH 1/CH 2 (Reserved, set low)
5	D0
6	D1
7	Ground
8	D2
9	D3
10	D4
11	D5
12	D6
13	D7
14	Ground
15	D8
16	D9
17	D10
18	D11
19	Ground
20	D12

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Signal Levels

All pins are configured as 2.5 V, LVCMOS inputs. The logic levels must be within the following ranges:

Low	–0.2 to +0.5 V
High	+2.0 to +2.8 V

Signal Descriptions

Data Input

The input data represents a handle to the next scenario to be played by the AWG module. Only the first 8,192 scenarios are available. The scenario handle must be divided by 2 before being written to the AUX port. For example, to play the scenario with a handle of 72, write the value 36 to the AUX port. All scenario handles are even numbers.

Data Valid

When Data Valid is asserted high, it indicates that the data present on the Data pins is valid and can be latched into the channel 1 and channel 2 next sequence register.

Trigger

Trigger input can be configured to be either rising-or falling-edge, with a programmable delay. Refer to “Triggers” on page 72.

NOTE The latency between trigger assertion and sequence playback is the same as that for the front panel trigger inputs, a resolution of one SYNC clock.

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5 Direct Digital Synthesis Option 330

The direct digital synthesis (DDS) architecture in the N6030A Series AWGs enables you to create basic waveforms in the AWG memory and then modify the behavior of the waveforms with profiles for amplitude, phase and frequency modulations.

Direct Digital Synthesis Using the Control Utility 91

- Configuring the Equipment 91
- Selecting the DDS Option 91
- Configuring the Clock 92
- Configuring the Sequencer 93
- Out of Range Input Values 96

Theory of Operation 99

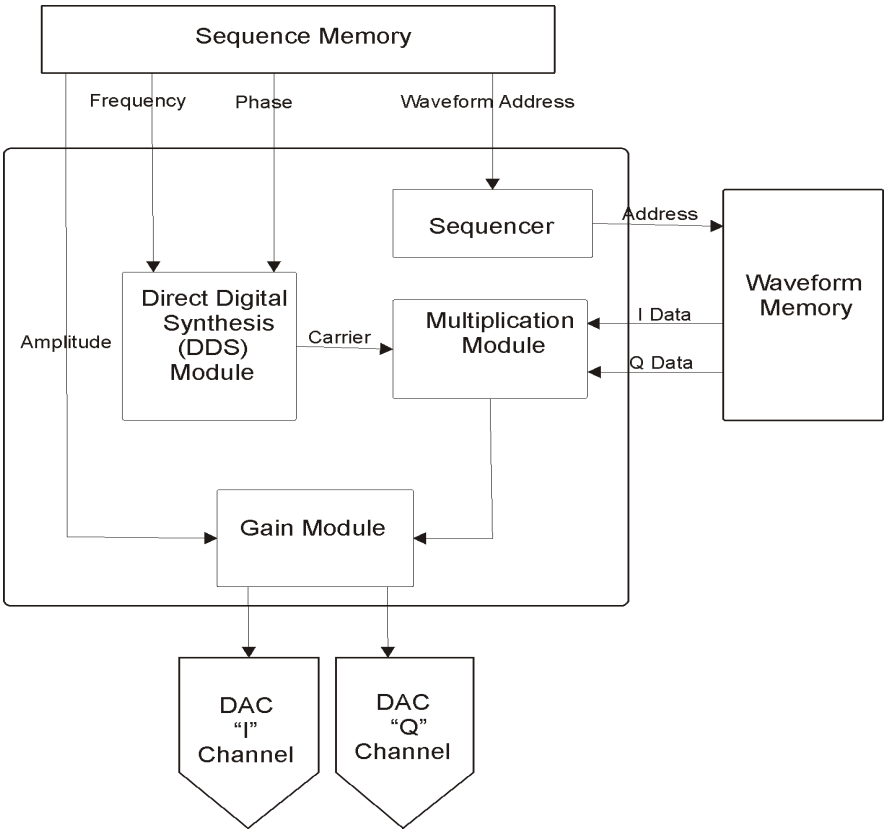
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Direct Digital Synthesis

The N6030A direct digital synthesis application can be managed through the Control Utility graphical user interface (GUI) or one of the supported programmatic interfaces. Accessing DDS through the GUI is the easiest way to view the functionality as many details are handled by the software in the background.

As an introduction, we will step through using DDS with the Control Utility. Figure 5-1 displays a high level DDS block diagram.

Figure 5-1 DDS Block Diagram



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Direct Digital Synthesis Using the Control Utility

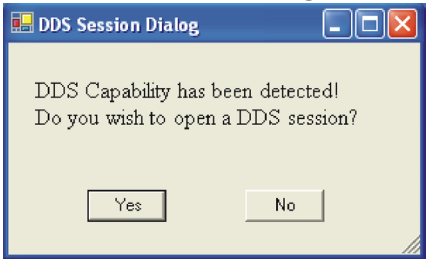
NOTE A spectrum analyzer is required to display the waveform.

Configuring the Equipment

1. Connect a 10 MHz reference from the spectrum analyzer to the AWG front panel connector. If you are using a PXI chassis, use the backplane 10MHz reference.
2. Connect the channel 1 positive (+) output to the spectrum analyzer RF input connector.

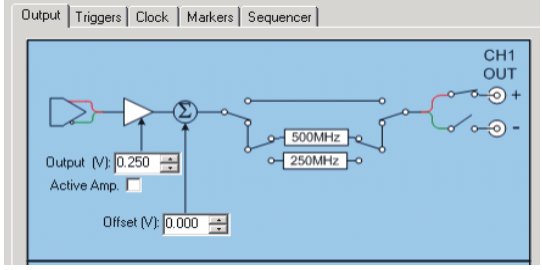
Selecting the DDS Option

1. Open the **Control Utility** by double-clicking the icon on the desktop.
2. In the **DDS Session Dialog** box, select **Yes**.



Configuring the Signal Conditioning Path

1. Select the **Output** tab and connect a single-ended signal conditioning path to CH1 OUT (+) (click on the node that you want to connect).



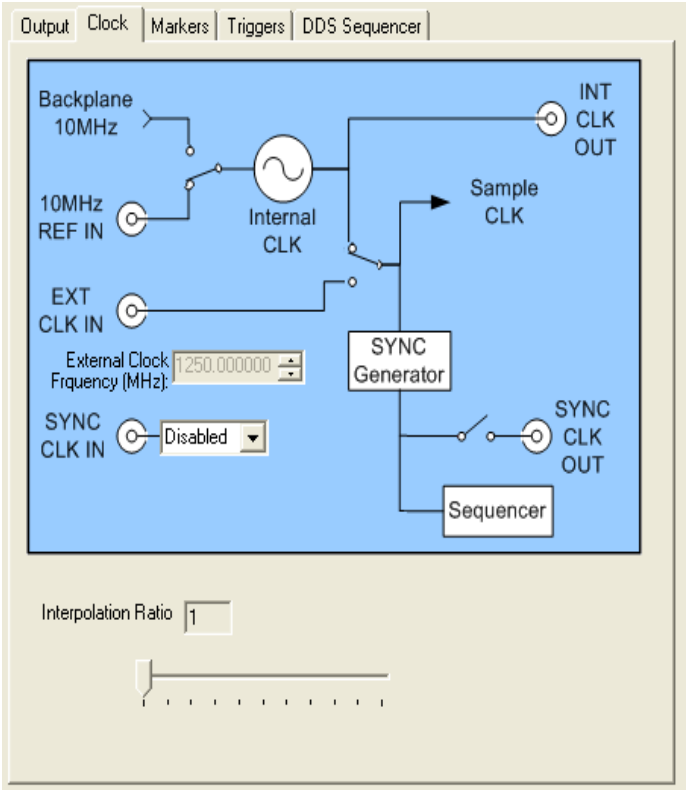
The connection will automatically enable differential mode. Click on the

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negative (-) node to open this path and enable single-ended mode.

Configuring the Clock

1. Select the **Clock** tab and configure the 10MHz REF IN. For this example, we utilized the 10 MHz reference from the E4440 Spectrum Analyzer in step 1. If you are using a PXI chassis, leave the clock set to the default Backplane 10MHz.

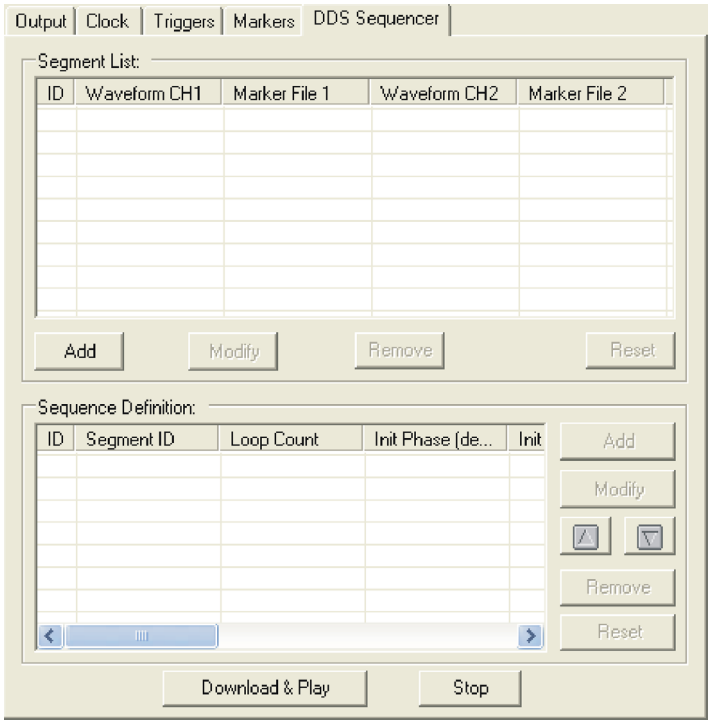


2. Use the default setting for the **Interpolation Ratio**.

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Configuring the Sequencer

1. Select the **DDS Sequencer** tab.



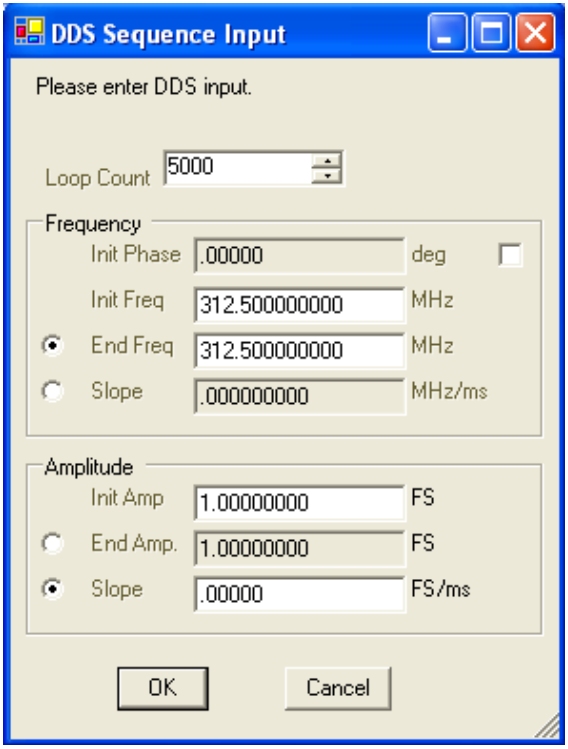
2. From the **Segment List** select **Add**. This brings up a **Segment Information** window.
3. Browse and select the **DDS_All_Ones** waveform from the **Demo Waveform DDS** folder included on the N6030A Series CD or the memory stick, then click **OK**.

NOTE For dual channel sequencing, add waveforms of the same length to both channel 1 and channel 2. Currently, the software does not support independent channel sequencing.

4. In the **Segment List**, select the **DDS_All_Ones** waveform.

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5. In the **Sequence Definition** area, select **Add**. This brings up the **DDS Sequence Input** window.
6. Enter **5000** repetitions and accept all default settings. Click **OK**.

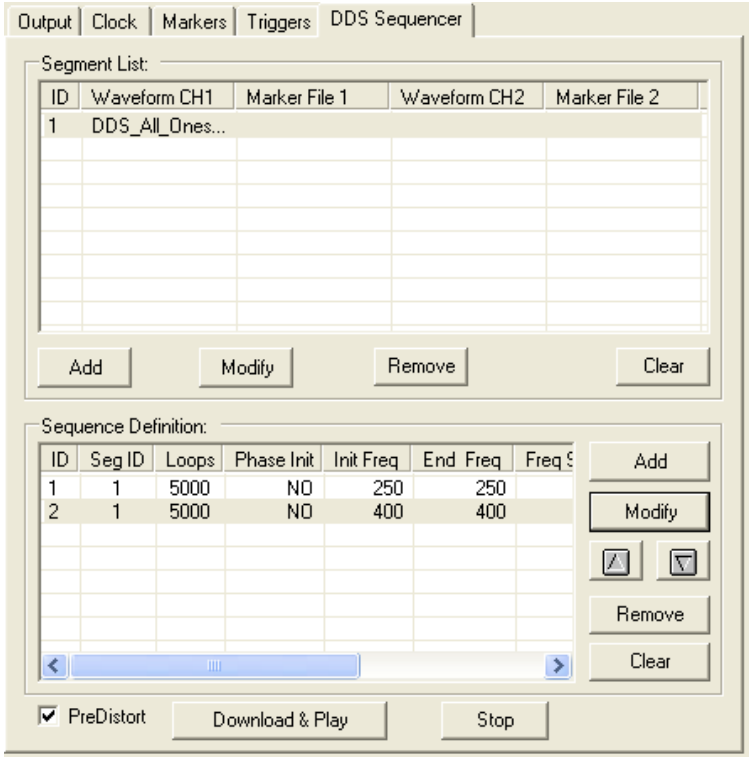


NOTE The values entered in the DDS Sequence Input window are recorded in the sequence definition area of the Sequencer tab. This enables you to review the values after the DDS Sequence Input window is closed.

7. Repeat steps **4**, **5**, and **6** using a 400 MHz Init Freq Value.
8. The sequencer tab should look like Figure 5-2.

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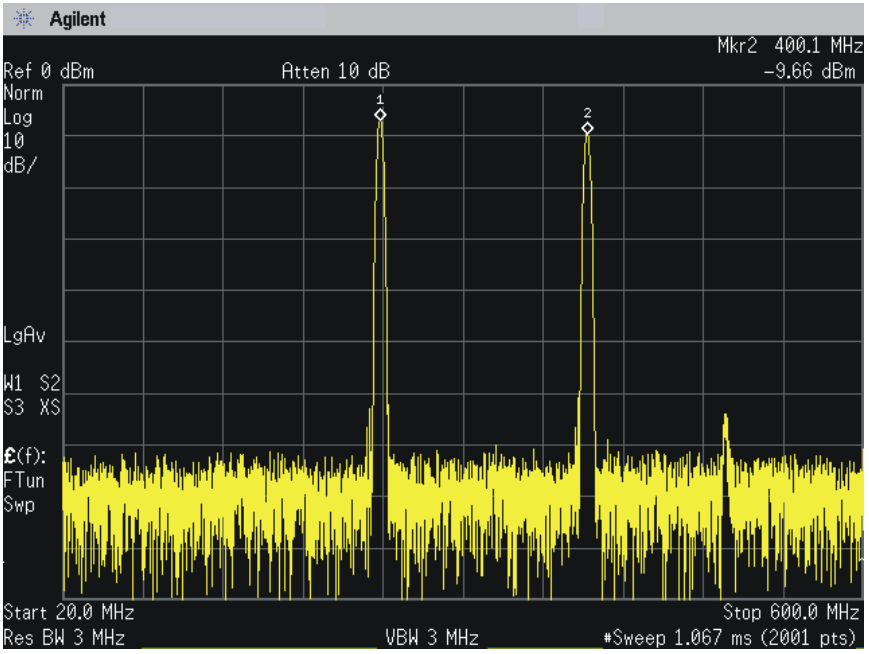
Figure 5-2 Sequencer Tab



9. Click **Download & Play**. The spectrum of the sequence should be similar to the one shown in Figure 5-3.

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Figure 5-3 Playback of a Sequence



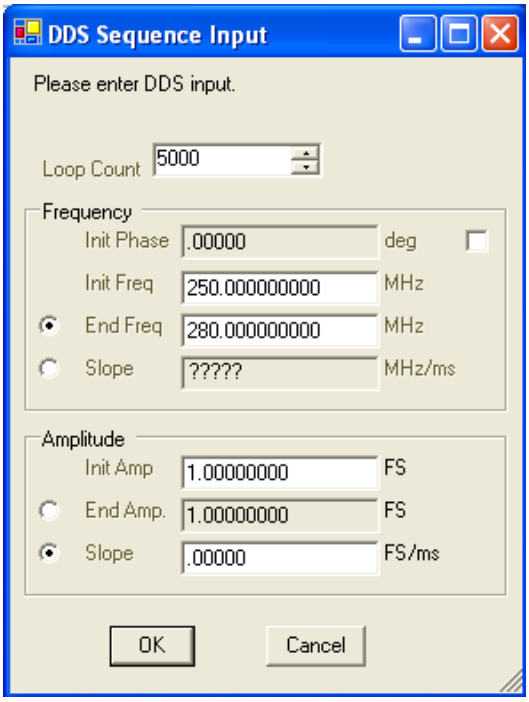
The 250 MHz carrier (marker 1) and the 400 MHz carrier (marker 2) are combined with a waveform composed of all ones.This illustrates how the DDS engine produces sine waves when a constant frequency is specified.

Out of Range Input Values

Some values may cause an 'out of range' condition. Refer to Figure 5-4.

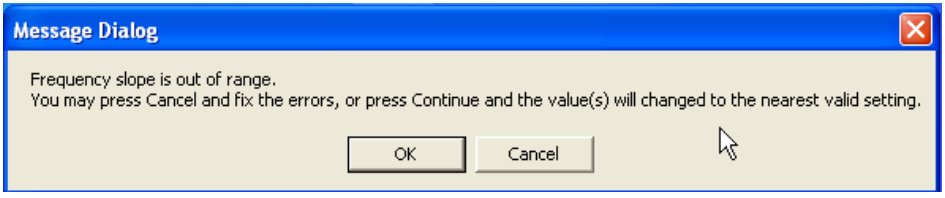
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Figure 5-4 **DDS Sequence Input Window**



Notice the question marks in the **Frequency Slope** box. This is occurs when the combination of the loop count, the initial frequency, and the end frequency cannot be calculated correctly. If you select **OK**, a message window comes up.

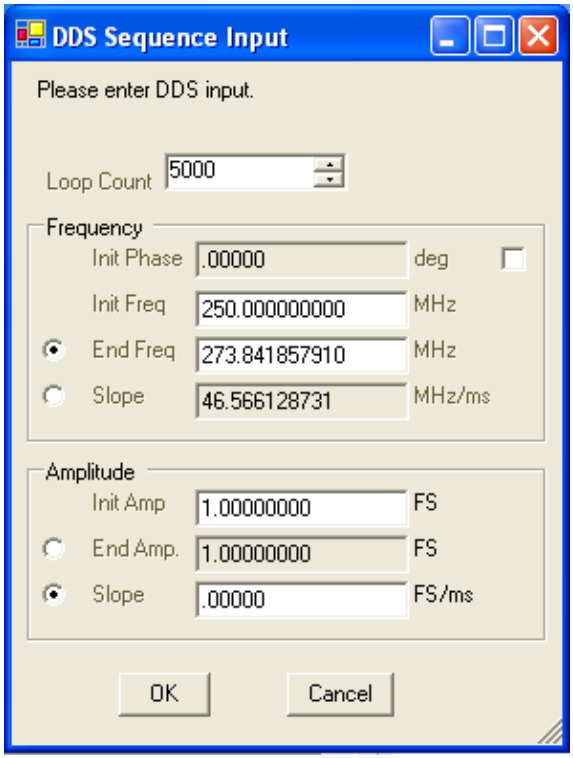
Figure 5-5 **Message Dialog**



For this example, selecting **OK** resulted in values shown in Figure 5-6.

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Figure 5-6 Calculated Valid Settings



The end frequency value was adjusted to enable the slope count.

NOTE This type of ‘out of range’ condition may also occur with amplitude settings.

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Theory of Operation

The Direct Digital Synthesis, Option 330, is a powerful tool for those customers who are using the N6030A Arbitrary Waveform Generator (AWG) to synthesize waveforms best expressed in the frequency domain. Traditionally, waveforms are expressed in the time domain, sampled, and then stored in waveform memory for eventual playback. This approach is completely generic and applicable to any describable waveform. However, many waveforms can be described as a combination of information content and simple sinusoids. For these waveforms, most of the available waveform memory gets used up storing the sinusoids, leaving little space for the information content.This is an inefficient utilization of waveform memory.

For example, in communications, the waveform can be described as a carrier (sinusoid) modulated with data (information content). Because the AWG has such high dynamic range, the modulated carrier can be generated with very good equivalent error vector magnitude (EVM) performance. But, because the carrier has to be stored in waveform memory along with the modulation, limited playback time can be achieved. Another important example of a frequency domain waveform is wideband radar chirps. Again, the waveform consists of a combination of a sinusoid and a frequency chirp profile, both of which must be traditionally stored in waveform memory, resulting in limited playback time.

To address this issue, Option 330 allows the AWG to generate the sinusoidal portion of the waveform real time, and then modulate the sinusoid with the information content stored in waveform memory (see Figure 5-7). This is done by adding a direct digital synthesizer (DDS) to the main FPGA in the AWG. The DDS implemented has a frequency resolution of 1.1369 mHz, and can synthesize sinusoids from DC to 400 MHz (using the 1.25 GHz internal clock). The DDS can be linearly ramped in frequency, with a frequency ramp rate resolution of 1.3552 Hz/s, and a maximum frequency ramp rate of 46.566 GHz/s. The frequency ramp rate can be positive or negative.

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The initial phase of the DDS can be set to a known value, with a phase resolution of 21.458 µdegrees. Alternatively, through the use of the initial phase control field, the DDS can be operated in phase continuous mode; for example, the initial phase not initialized. This is useful for applications requiring phase continuous frequency hopping. The DDS generates both sine and cosine outputs for use in the complex modulator. Refer to Figure 5-7.

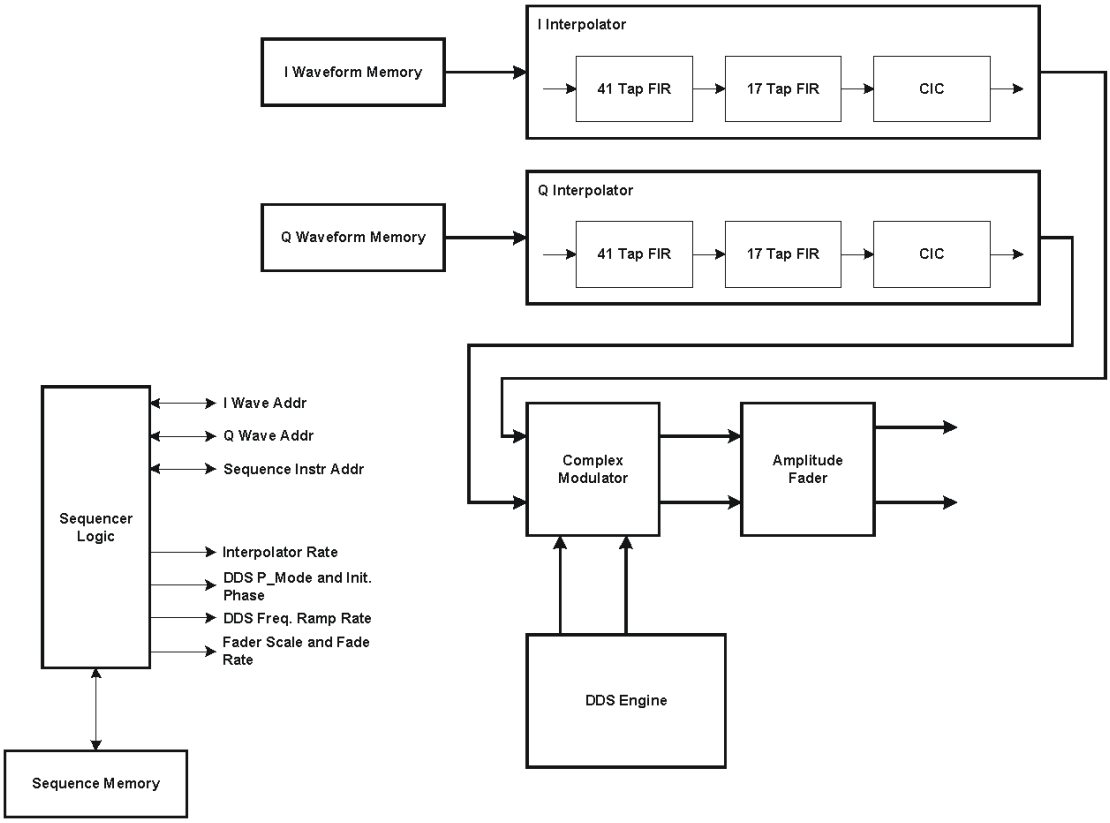
To allow waveform memory to be played back at a rate slower than the AWG sample rate, interpolation filters have been added to the main FPGA, for both channels. The interpolation filters can be configured to interpolate by integer powers of two: 2, 4, 8. . ., up to a value of 1024. Image rejection for the filters is better than 65 dBc for all interpolation rates, and flatness is compensated for automatically in software. By setting the interpolation filters to 1024, the waveform memory can be played back at a rate over a thousand times slower than the AWG sample rate. The interpolation filters can also be bypassed.

The sine and cosine outputs of the DDS, and the interpolated outputs of waveform memory are sent to a complex (or I/Q) modulator for upconversion. If the channel 1 interpolated memory is represented symbolically by “I”, and the channel 2 interpolated memory by “Q”, then the channel 1 analog output can be expressed as I*cos(wt) – Q*sin(wt). Channel 2 can be expressed as I*sin(wt) + Q*cos(wt). Each analog output represents a carrier (DDS output) I/Q modulated by data (channel 1 and 2 interpolated waveform memory). Alternatively, if both analog channels are subsequently used to drive an external I/Q modulator, they are configured to provide for upper sideband SSB conversion at the output of the external modulator.

Both internally modulated outputs can be linearly faded in amplitude within the AWG. The linear fade function occurs after the complex modulator. Amplitude fade rate resolution is set to 1.819% full scale per second, with a maximum fade rate of 62.5% full scale per nanosecond. Fade rates can be positive or negative.

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Figure 5-7 DDS



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6 Troubleshooting

The following topics are included in this chapter.

- Software 104
  - Removing the Software 104
  - Moving the Software 104
  - Updating the Software 104
- NI MXI-4 Link 105
  - If You Encounter Problems Configuring the NI MXI-4 Link 105
  - Configuring the NI MXI-4 System 106
- Contacting Agilent 112
  - Agilent on the Web 112
  - Questions or Comments on the Documentation 112

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Software

Removing the Software

If it is necessary to remove the N6030A software, go to:

Start > **Settings** > **Control Panel** > **Add/Remove Programs**

Remove **Windows Driver Package - Agilent Technologies Agilent N6030A Device Driver**.

Remove **Agilent N6030A Application Software**.

Remove **Agilent N6030A IVI-C Driver**.

You may need to restart the controller, but this will completely remove all of the N6030A files.

Moving the Software

If it becomes necessary to move the N6030A software, complete the instructions documented in Removing the Software. Then, using the N6030A CD or the memory stick, reinstall the software where it is needed.

Updating the Software

To resolve an error message you get while attempting to upgrade the N6030A series software, take the following steps in the listed order:

Go to: **Start** > **Settings** > **Control Panel**.

Double-click **Add/Remove Programs**.

Select **Windows Driver Package-Agilent Technologies Agilent N6030A Device Driver**, and select **Remove**.

Select **Agilent N6030A Arbitrary Waveform Generator**, and select **Remove**.

Reinstall the N6030A series software.

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NI MXI-4 Link

If You Encounter Problems Configuring the NI MXI-4 Link

1. Uninstall the N6030A Driver. (from Administrator mode)

   Right-click **My Computer** > **Properties** > **Hardware** > **Device Manager…**
   Expand **Agilent Technologies Test & Measurement Devices**
   Right-click on **Agilent Technologies N6030A** and select **Uninstall**

2. Uninstall the software

   Go to: **Start** > **Settings** > **Control Panel**
   Double-click **Add or Remove Programs**
   Select **Agilent N603x Software Package**, select **Remove**.
   Select **Windows Driver Package-Agilent Technologies Agilent N6030A Device Driver**, select **Remove**.
   Select **IVI Shared Components**, select **Remove**.
   Select **National Instruments Software**, select **Remove.**

3. Shut down the PC, power off the chassis, remove the cable from the MXI-4 card, and remove the MXI-4 card from the PC.

4. Re-boot the PC and make sure all the software listed above was removed. Download the IVI Compliance Package, which contains the IVI Engine and the IVI Shared Components.

5. Go to: http://www.ni.com/

   Search on **ivi compliance package version 2.2**.
   Select **IVI Compliance Package Version 2.2 for Windows 2000//NT/XP-HWDRIVER-Support-National**
   Follow the instructions for the **Download Process** at the bottom of the page.

6. Install the NI software without the MXI-4 card in the PC.

7. Install the N6030A software from the N6030A CD.

8. Shut down the PC, install the MXI-4 card and attach the cable.

9. Power on the chassis.

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10. Reboot the PC.
11. Verify that Plug&Play loads the NI driver, the N6030A driver, and recognizes the MXI-4 card.

If you are still experiencing problems, refer to Configuring the NI MXI-4 System.

Configuring the NI MXI-4 System

1. Open the **NI Measurement and Automation Explorer**.
2. An entry will appear in the tree called **IVI Drivers**.

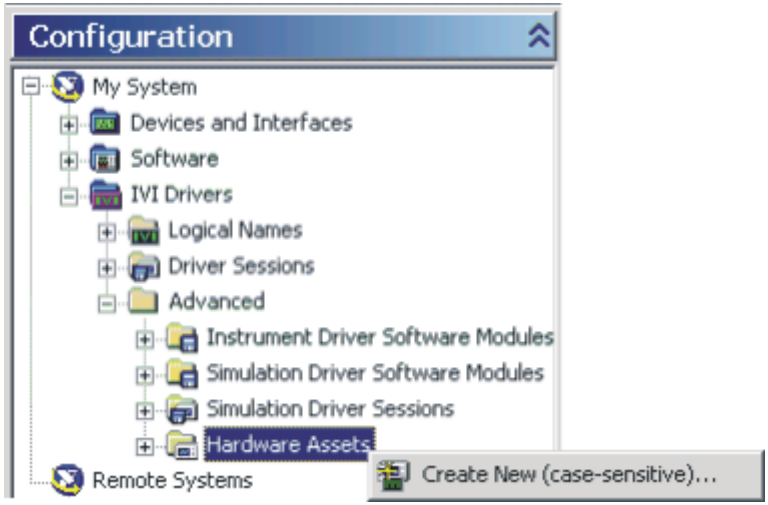


   It is important to work from the bottom of the tree and move upwards. This ensures that the inheritances are clearly established.

3. Expand **IVI Drivers**. (click the plus sign)
4. Expand the **Advanced** folder.
5. Right-click the **Hardware Assets** tab, select **Create New** and enter a

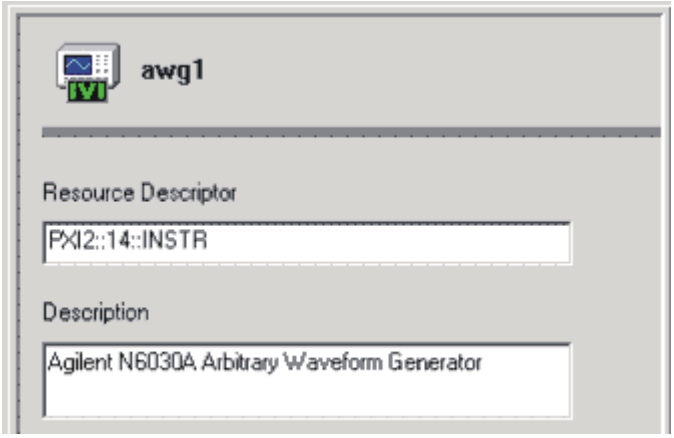
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name.In this example, awg1 was the name used.



6. Enter the N6030A address (VISA resource name) in the Resource Descriptor field and enter a description in the Description field.

   Note: The N6030A address is found on the N6030 Control Utility.

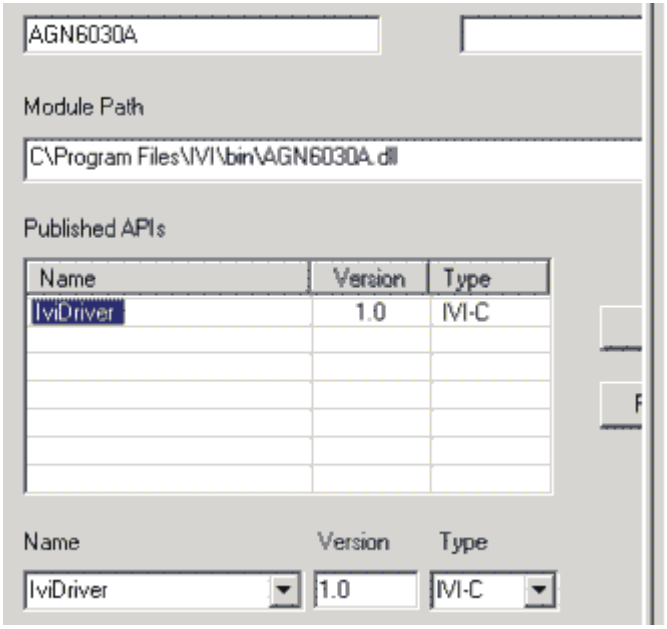


7. Select the **Instrument Driver Software Modules** tab, right-click and select Create New.

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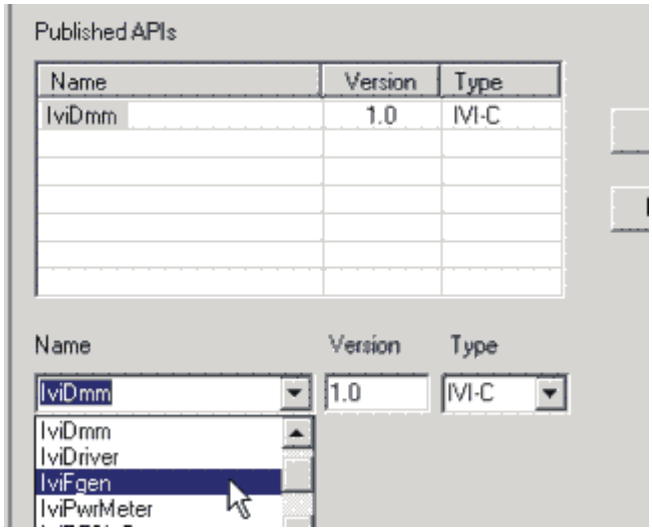
8. Rename this new entry agn6030a and enter the information in the **Prefix** and the **Module Path** fields as it is shown in the graphic.
9. In the **Published APIs** field, select **IviDriver**.

.



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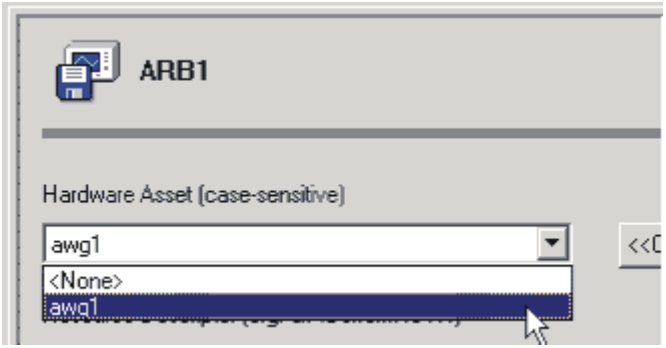
10. Expand the drop-down arrow in the **Name** field and select I**vifgen**



11. Move up in the tree, select the **Driver Sessions** tab, right-click and select **Create New**. **Rename**. ARB1 was chosen for this example.

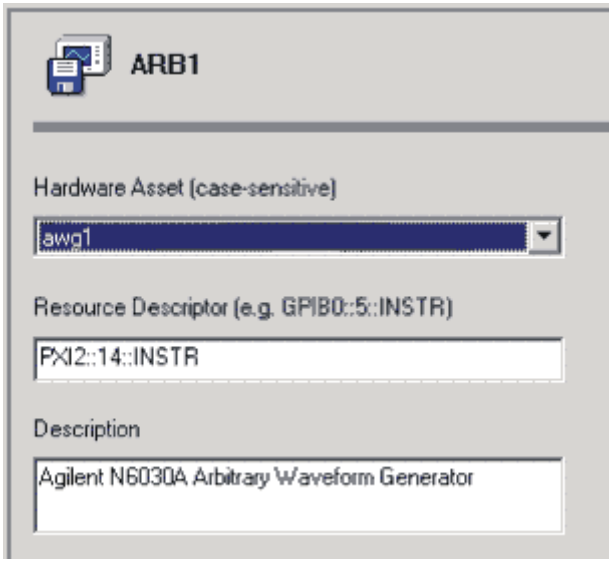
    At the bottom of this window, there are multiple tabs. Use the defaults on the **General** tab

12. At the bottom of this window, select the **Hardware** tab, expand the drop-down arrow of the **Hardware Asset** field, and select the name of the hardware you assigned in step 3.

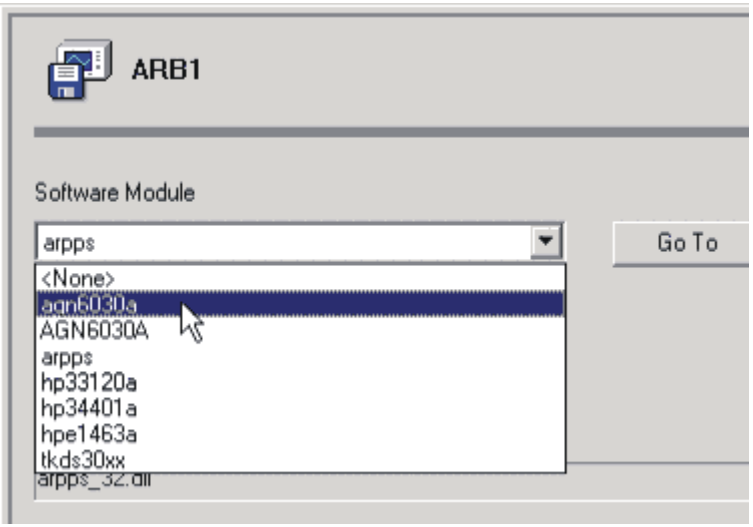


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Information will populate the fields to appear like the following graphic.

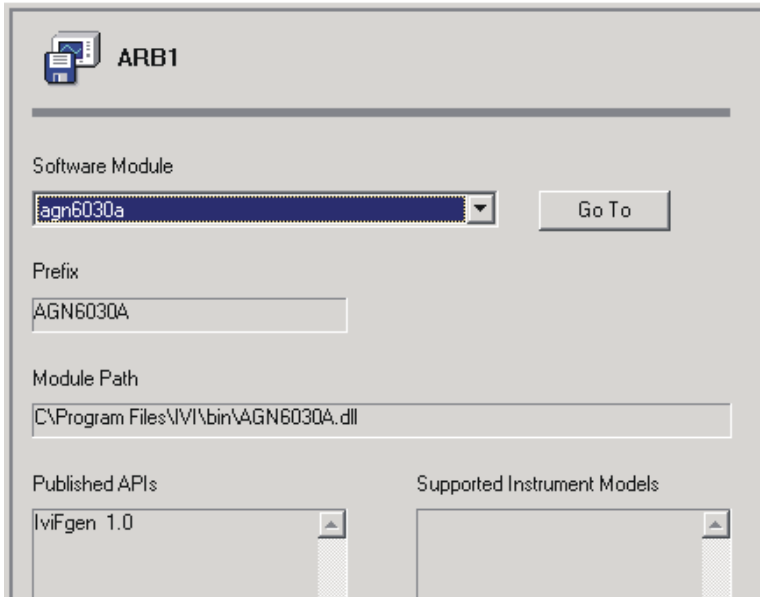


13. At the bottom of this window, select the **Software** tab, expand the **Software Module** drop-down arrow, and select the name you assigned in step 6.



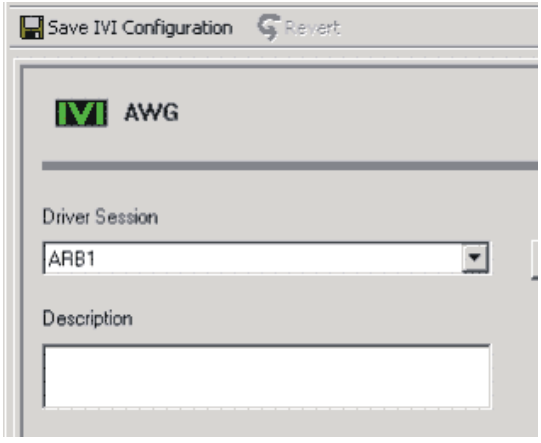
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14. Information will populate the fields to appear like the following graphic.



15. Now, move up in the tree, select the **Logical Names** tab, right-click and select **Create New**. **Rename**, AWG was chosen for this example.

16. Expand the **Driver Session** drop-down arrow and select the name given in step 9. Select Save IVI Configuration from the top of the window.



This will write all of the information to the IVI Configuration Store.

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Contacting Agilent

Agilent on the Web

You can find information about technical and professional services, product support, and equipment repair and service on the Web:

http://www.agilent.com

Click on the Test & Measurement link then click on Select a Country. Click on the Contact Us link for contact information.

Questions or Comments on the Documentation

The latest documentation can be found on our Web site, http://www.agilent.com/find/awg

We welcome any questions or comments about the documentation.

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7 Characteristics

The following topics are included in this chapter.

Technical Characteristics 114

General Characteristics 118

Declaration of Conformity 120

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Technical Characteristics

Channels

Two independent channels available as baseband or IF outputs

CH1: Single-ended and differential

CH2: Single-ended and differential

Modulation bandwidth

500MHz per channel (1 GHz IQ bandwidth)

Resolution

N6030A: 15 bits
N6032A: 15 bits

N6031A: 10 bits
N6033A: 10 bits

Output spectral purity - (CH1 and CH2)

Harmonic Distortion: 1 kHz to 500 MHz
N6030A: < –65 dBc for each channel
N6032A: < –65 dBc for each channel

N6031A: < –50 dBc for each channel
N6033A: < –50 dBc for each channel

Non-Harmonic Spurious: 1 kHz to 500 MHz
N6030A: < –65 dBc for each channel
N6031A: < –65 dBc for each channel
N6032A: < –65 dBc for each channel
N6033A: < –65 dBc for each channel

Noise floor:
N6030A: < –150 dBc/Hz across the channel bandwidth
N6031A: < –150 dBc/Hz across the channel bandwidth
N6032A: < –150 dBc/Hz across the channel bandwidth
N6033A: < –150 dBc/Hz across the channel bandwidth

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Sample clock

Internal: Fixed 1.25 GS/s

Internal clock output: +3 dBm nominal into 50 ohm load

External clock input: Tuneable 100 MS/s to 1.25 GS/s

External clock input (power): –15 to +5 dBm, 0 dBm nominal

Phase noise characteristics:

1 kHz	-95 dBc/Hz
10 kHz	-115 dBc/Hz
100 kHz	-138 dBc/Hz
1 MHz	-150 dBc/Hz
Noise Floor	-150 dBc/Hz

Accuracy:
Same as 10 MHz timebase input

Frequency reference

Input drive level: +2 to +12 dBm into 50 ohms (+2 dBm nominal)

Waveform length

8 MS per channel (16 MS with option 016)
Minimum waveform length: 128 samples
Waveform granularity: 8 samples

Segments

From 1 to 32,768 unique segments can be defined consisting of waveform start and stop address, repetitions and marker enable flags.

Sequences

Up to 16,384 total unique waveform segments can be combined with separate loop counts to form a sequence.

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External triggers

Number of inputs:	5 each (4 SMB female front-panel connectors plus one software trigger over PCI backplane from host processor)
Trigger polarity:	Negative/positive
Trigger impedance:	2k ohms
Maximum input level:	4.3V
Input sensitivity:	250 mV
Trigger threshold:	-4.5 to + 4.5 V
Trigger timing resolution:	Clock/8 (6.4 ns at full rate)
Trigger uncertainty:	< 50 ps
Minimum trigger width:	12.8 ns at full clock rate
Trigger delay:	resolution of 1 SYNC clock

External markers

Markers can be defined for each waveform segment.

Number of outputs:	4 each SMB female
Marker polarity:	Negative, positive
Output type:	3.3V CMOS with 30 ohm series termination
Marker low level:	100 mV nominal (high impedance load)
Marker high level:	3.2V nominal (high impedance load)
Marker timing resolution:	Clock/8 (6.4 ns at full rate)
Marker delay:	resolution of 1 sample clock
Marker width:	resolution of 1 SYNC clock

Module synchronization

Hardware supports synchronization of multiple modules with future software enhancements.

Sync clock output level: 800 mV p-p 50 ohm output impedance, AC coupled
Sync clock input level: 100 mV p-p into 50 ohms AC coupled

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Analog output

Output connector: SMA female
Output impedance: ~50 ohms

Analog output levels

The following output levels are specified into 50 ohms:

	Single-Ended	Differential
Passive Mode	0.5Vp-p	1Vp-p
Active Mode	1Vp-p with +/-0.2Vp-p	N/A

Uncorrected passband flatness: +/- 1 dB DC - 200 MHz; +/- 3.5 dB DC - 500 MHz (with 1.25 GHz clock)
Uncorrected passband group delay: +/- 500 ps DC - 200 MHz; +/- 1 ns DC - 500 MHz (with 1.25 GHz clock)

Reconstruction filters

500 MHz and 250 MHz realized as 7-pole elliptical filters plus thru-line output

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General Characteristics

Power

Supply	Typical Operation (Watts)
+3.3 VDC	11.2
+5 VDC	22
+12 VDC	5
-12 VDC	5
Total Power	43.2

Environmental

Samples of this product have been type tested in accordance with the Agilent Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation, and End-use; those stresses include but are not limited to temperature, humidity, shock vibration, altitude, and power line conditions. Test methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

Operating temperature:	0 to +55 degrees C
Storage temperature:	-20 to +70 degrees C
Relative Humidity:	
Type tested:	10 to 90% at 40 degrees C (non-condensing)
Altitude:	0 to 2000m (6500 ft) above sea level

Safety

Designed for compliance to IEC 61010-1:2001

EMC

Meets the conducted and radiated emissions and immunity requirements of IEC 61326:2002 when tested with EMC shielded filler panels (Agilent P/N N6030-80007, kit of 6) separating the controller and the N6030A module, and in all open slots. The RFI gaskets must be oriented to the right.

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Weight

1.14 kg (2.5 lb)

Security

All user data stored in volatile memory

Dimensions

3U, 4 slot CompactPCI module: 8.1 x 13 x 21.6 cm (3.2 x 5.1 x 8.5 inches)

Recommended calibration cycle

12 months

ISO compliance

This modular instrument is manufactured in an ISO-9001 registered facility in concurrence with Agilent Technologies, Inc. commitment to quality.

Options (N6030A, N6031A, N6032A, N6033A)

N6030A-016: Waveform memory expansion to 16 MS per channel
N6030A-300 Dynamic Sequencing
N6030A-330 Direct Digital Synthesis (DDS)

N6030A-500: PXI 18-slot chassis

N6030A-501: PXI embedded controller, P4

N6030A-502: PXI MXI-4 kit (includes PC and chassis PCI cards)

N6030A-503: Shielded PXI chassis filler kit to cover 17 slots

N6030A-504: 17-inch flat panel monitor

N6030A-505: PS2 keyboard and mouse

N6030A-506: Rack mount kit for PXI chassis

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Declaration of Conformity

The Declaration of Conformity (DOC) is on file. If a copy is required, please contact an Agilent Sales Representative or the closest Agilent Sales Office. Alternately, contact Agilent at:

http://www.agilent.com/find/assist

The N6030A Series AWGs share the same hardware covered by this DOC.

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