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Model V635

8-channel, 100 kHz Frequency Counter

User's Manual

August 10, 1998

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About This Manual

Organization

Chapter 1, ***Introduction***, gives you a brief overview of the Model V635, lists items you need to get started, and explains how to safely unpack your module.

Chapter 2, ***Installation and Configuration***, explains how to configure the V635 and correctly insert it into a C-size VXIbus mainframe.

Chapter 3, ***Understanding the V635***, describes the performance of the V635.

Chapter 4, ***Configuration and Operational Registers***, explains how to access and control the V635.

Chapter 5, ***Programming Information***, gives you example setup procedures for preparing the V635 to acquire frequency counts.

The ***Appendices*** provide additional information that may be helpful in learning more about KineticSystems and its products, and in quickly reaching us.

Glossary

Following is a glossary of some of the terms and conventions used throughout this manual:

*****	An indicator that a register bit contains low-true data. For example, writing a **"0"** to a bit labeled Enable* would cause a function to be enabled.
A16 Space	The first 64 kbytes of address space, accessible with 16-bit addressing. The configuration registers of VXI devices occupy 64-byte blocks of this address space. The Logical Address of a device determines which 64-block block is associated with that device.
A32 Space	The 4 Gbyte address space, accessible with 32-bit addressing. A module can request a block of this address space via information contained in its *Configuration* registers. *Operational* registers, if present, reside in this space.
Configuration Registers	Setup registers located in **A16** space. Some are mandatory; some are optional.
D16	A single 16-bit data transfer.
D16 BLK	A block transfer of 16-bit words.
D32	A single 32-bit data transfer. Not all Slot-0 controllers support **D32**.

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D32 BLK	A block transfer of 32-bit words. Not all Slot-0 controllers support **D32** BLK.
Device	One of 255 devices that a VXIbus system can support. The term is often used interchangeably with "module." The distinction is that a VXIbus module can consist of more than one device.
Dynamic Addressing	The VXIbus addressing mode in which the address of a device is stored in a write-able register. See also Static Addressing.
hexadecimal	A base-16 number. The suffix, "h," indicates that a number is hexadecimal. For example, 1Ah = 26_{10}; FFh = 255_{10}; 1000h = 4096_{10}.
Logical Address	A VXIbus module's unique address. A VXIbus system has 254 logical addresses that are available. **"0"** is the address of the Slot-0 controller. **"255"** specifies that dynamic addressing be used to address that module.
Observation Window	The time selected to sample the input signal and internal clock to determine the input frequency.
Operational Registers	Setup and data-transfer registers that are located in A32 address space.
Period Counter	The counter that counts the number of periods of the input signal during an observation window.
RAM	Random Access Memory. RAM refers to a memory block that has direct addressable access, as opposed to sequential access.
Resource Manager	Software that sets logical addresses and optimally configures Operational register addresses and memory-block addresses in a system. The manufacturer of the Slot-0 controller provides this software, often referred to as "RESMAN."
Static Addressing	The VXIbus addressing mode in which the address of a device is stored in a switch register. See also Dynamic Addressing.
Tick Counter	The counter that counts the number of clock periods (ticks) that relate to the input period counts during an observation window.

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Chapter 1: Introduction

About the V635

Features

- Options available with four or eight frequency counter channels
- Frequency range from 0.06 Hz to 100 kHz
- Differential and TTL inputs provided
- Differential input range ordering options: ±20 mV or ±100 mV, highest sensitivity
- Programmable AC/DC differential inputs
- Programmable observation window: 1 ms to 1.024 s
- Precision time base (±1 ppm, 10°C to 50°C)

Applications

- Monitoring shaft encoders and other devices to measure RPM from shafts on automotive and aircraft engines
- Monitoring flow meters
- General-purpose frequency counting

General Description

The V635 is a single-width, C-size, register-based, VXIbus module with four or eight frequency measurement channels. This counter module can be used to monitor a variety of pulse sources. Moreover, its unique circuitry allows the monitoring of a wide range of frequencies without changing any module settings. TTL inputs are provided as well as differential input circuits with filtering and hysteresis to provide high noise immunity. The switching threshold is programmable, and the input voltage should be at least twice the threshold voltage for noise immunity. AC or DC coupling of the differential inputs is programmable on a per-channel basis.

The V635 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A32/A16, D32/D16 data transfers.

Ordering Information

Model V635-AA11	4-channel, 100 kHz Frequency Counter, ±20 - 200 mV to ±20 V Range
Model V635-AA21	8-channel, 100 kHz Frequency Counter, ±20 - 200 mV to ±20 V Range
Model V635-AB11	4-channel, 100 kHz Frequency Counter, ±100 - 1000 mV to ±20 V Range
Model V635-AB21	8-channel, 100 kHz Frequency Counter, ±100 - 1000 mV to ±20 V Range

Related products

Model 5930-Z1A	9-contact "D" Connector with Sockets
Model 5931-Z1D	15-contact "D" Connector with Sockets
Model 5934-Z1A	25-contact "D" Connector with Sockets

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Getting Started

To set up and use your V635 VXIbus module, you will need most or all of the following:

- The V635 Counter module and this User Manual
- Your VXIbus system with its Resource Manager and high-level test and/or application software

Unpacking the V635

The V635 comes in an anti-static bag to avoid electrostatic damage. Electrostatic discharge to the module can damage components on it. Please take the following precautions when unpacking the module:

- Ground yourself with a grounding strap or by touching a grounded object.
- Touch the anti-static package to a metal part of your VXIbus chassis before removing the module from the package.
- Remove the module from the package and inspect the module for damage.
- Do not install the module into the VXIbus chassis until you are satisfied that the module exhibits no obvious mechanical damage and is configured to conform to the desiring operating environment. The next chapter describes installation and configuration.

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Chapter 2: Installation and Configuration

Setting the Logical Address Switches

A VXI system can have as many as 255 devices, with each having a unique number in the range from 0 to 254. Eight bits represent the number, which is the Logical Address of the device.

VXIbus defines two concepts of addressing: "static" and "dynamic." All VXIbus devices *must* allow static addressing, in which the address is determined by the setting of a switch register. VXIbus devices may, but are not required to, support dynamic addressing. In dynamic addressing, the Logical Address is stored in a software-addressable register. For reasons discussed in Chapter 4, all KineticSystems VXIbus devices support dynamic as well as static addressing.

Before installing the V635 in the VXIbus chassis, you must set the switch register to an appropriate value. If you wish to employ static addressing you must make sure you set the switch register to a unique value other than 0 or 255. It is a good idea to note module addresses in an accessible log, because if you replace a module, it is very important that the new module have the same address as the replaced one.

If your system employs dynamic addressing, which delegates the task of assigning device addresses to the Resource Manager software, then make sure the address switch is set to 255 (all **"1"**s).

Figure 2-1. V635 Logical Address Switch Locations

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Selecting the Analog Input Termination

The analog input path for each of the eight channels has the switch-selectable option of unterminated or terminated. For most applications, the unterminated selection (the factory-set default) will be chosen. A 100-ohm termination can also be selected for each of these paths for use with RS-422, RS-485 or similar differential transmitters. If this module is the only (or last) receiver node on an RS-422 or an RS-485 path, the 100-ohm termination should be switched IN (terminated).

Figure 2-2. V635 Channel Termination Switch Locations

Module Insertion

Before inserting your VXIbus module into the chassis, make sure that the chassis is plugged into electrical power but *not turned on.* The power cord provides a ground connection for the mainframe and protects the equipment and you from electrical harm.

In a VXI system, the Bus Grant and IACK signals are received and transmitted by each of the modules. These signals must be jumpered around any vacant slots in the mainframe. Most current mainframes, including our V194 and V195, contain jumperless backplanes, where the Bus Grant and IACK signals are automatically jumpered when a slot is empty.

If your mainframe does not contain a jumperless backplane, you must position certain jumpers correctly on the chassis backplane to assure that the V635 acknowledges interrupts properly. Remove the Interrupt Acknowledge (IACK) jumper from the slot selected for the V635 and install daisy-chain jumpers in any empty slots between the V635 and the Slot 0 Controller.

You can now insert the V635 into the chassis. Slowly push it in until its plug connectors are resting against the backplane connectors. Then, using evenly distributed pressure, press the module straight in until it seats in the slot and the module front panel is even with the chassis front panel. Tighten the top and bottom screws. *You may now safely apply power to the V635.*

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Module Configuration

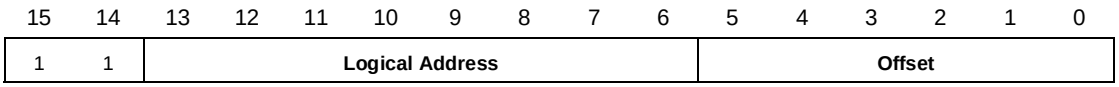
Setting the VXI Logical Address

You, or your software, must perform two types of module configuration. The first has to do with VXIbus-related items and involves communication with V635 *configuration* registers. The second deals with setting parameters related to module operation and involves communication with V635 *operational* registers.

VXIbus-related configuration includes setting the logical address, specifying the amount of memory space required, specifying where in memory the V635 registers and memory blocks are located, and setting interrupt levels.

When you configure the V635 for operation, you must select parameters such as the observation window period, internal clock rate, input signal type and analog input sensitivity.

VXIbus devices occupy system memory space. The configuration registers for each VXIbus device have 64 bytes of memory space in the upper 16 kbytes of the 64-kbyte **A16** memory space. Whether you set the 8-bit Logical Address statically in the switch register or dynamically in the Logical Address register, those eight bits determines the base address of the 64-byte block of memory as follows:



Each 64-byte block contains several registers that supply information about the module, such as the manufacturer, the module identifier (i.e., "207h"), its class (register-based or message-based), serial number, and the amount of memory space it requires.

In addition to **A16** addressing, a VXIbus device can also support **A24** or **A32** addressing. The V635 supports both A16 and A32 addressing.

The operational registers are all in **A32** space. To access them, one must first write a proper offset value to the Offset register in **A16** space. Refer to Chapter 5 for details relating to the *configuration* and *operational* registers.

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Chapter 3: Understanding the V635

Overview

The V635 is a single-width, C-size, register-based, VXIbus module with four or eight frequency measurement channels. This counter module can be used to monitor a variety of pulse sources. Moreover, its unique circuitry allows the monitoring of a wide range of frequencies without changing any module settings. TTL inputs are provided as well as differential analog input circuits with filtering and hysteresis to provide high noise immunity. Figure 3.1 is a block diagram showing one channel of the module.

Figure 3-1 V635 simplified block diagram showing one channel

Basic Circuit Operation

The module provides for two types of signal sources, analog and TTL. The analog input paths are differential for high noise immunity. These inputs can be unterminated (high impedance) or terminated with 100 ohms, selected by an on-board switch. The analog input coupling can be DC (the normal setting for most applications) or AC (with a series capacitor in each leg of the input path). The analog path also includes a gain control and a high-frequency noise filter. Both are programmable. The gain control sets the input switching threshold, while the filter provides a 3 dB rolloff at 50 kHz. The selection of analog or TTL input is programmable on a per-channel basis.

The internal clock for the module is driven from a 10 MHz clock having a 1 ppm accuracy from 10° C to 50° C. The internal clock can be set to 1 MHz or 10 MHz under program control. The 10 MHz clock provides an order of magnitude increase in counting resolution over the 1 MHz clock and is the general choice. The only disadvantage of the 10 MHz clock is that it causes a faster rollover of the tick count and limits the lowest frequency to be measured to 0.6 Hz, compared to 0.06 Hz when the 1 MHz clock is used.

All input channels on the module are monitored over a single user-selectable period, called the *observation window*. This window period is programmable from 1 millisecond to 1.024 seconds, in increments of 1 millisecond. The basic resolution of the measurement is ±1 clock period. Making the observation window period longer will generally increase the counting accuracy because the measurement period will be longer compared with the period of one cycle of the internal clock. The window period would be shortened to provide faster updates on an input signal whose frequency is changing.

At the end of each window period, 24 bits of data, containing the count from the internal clock, as well as 18 bits, containing the number of whole periods observed, are stored in the Tick Count register and the Period Count register for that channel. If the period of the input pulse stream is longer than the window

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period, the window remains "open" until one whole period of the input signal is observed. This "elastic" observation window that allows the module to count over a wide range of frequencies. The V635 can operate in a single-scan or in a continuous mode. If the module is operating in continuous mode (the normal selection), these registers can be read by software at any time, with the data from the latest observation being read. The frequency can be calculated by host computer software using the following formula:

Frequency = clock rate x whole input periods/internal clock counts

The clock rate is 1 MHz or 10 MHz, the whole input periods are represented by the Period Count data for that channel, and the internal clock counts are represented by the Tick Count data for that channel. For example, a period count of 500, a clock rate of 10 MHz and a tick count of 100,000 will result in the following:

50,000 Hz = 10,000,000 x 500/100,000

Count Acquisition

Figure 3-2 shows a typical timing sequence for one observation period. In this example the clock is set to 10 MHz, the observation window is set to 10 milliseconds and the input signal being measured is 490 Hz. The input period counter and the tick counter are simultaneously enabled on the first low-to-high transition of the input signal after the observation window edge, and counting of the input signal and clock ticks commence. Counting stops at the first low-to-high transition of the input signal after the next observation window edge. The input count = 5, and the tick count = 102,040. The frequency calculation is:

490.0039 Hz = 10,000,000 x 5/102,040

The clock resolution of ±1 count could result in readings from 489.999 to 490.0087 Hz.

Figure 3-2 The timing sequence for a 490 Hz input signal and 10 millisecond observation window

In the previous example the actual observation period approximated the observation window period. Figure 3-3 shows another timing example. In this case the input frequency is 20 Hz, with the observation window remaining at 10 milliseconds and the clock at 10 MHz. Since the actual observation period starts and ends at the first input low-to-high transition after a window edge, the counting spans multiple observation window periods. For this example the input count = 1, and the tick count = 500,000. The frequency calculation is:

20 Hz = 10,000,000 x 1/500,000

The clock resolution of ±1 count could result in readings from 19.9996 to 20.00004 Hz. Note that this is a better counting accuracy than the previous example because the *actual* counting period is 50 milliseconds, even though the observation window is set to 10 milliseconds. As the input frequency decreases, the actual observation period increases until the frequency causes tick counter overflow (0.6 Hz for a 10 MHz

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clock or 0.06 Hz for a 1 MHz clock).

Figure 3-3 The timing sequence for a 20 Hz input signal and 10 millisecond observation window

Counting Accuracy

The clock rate for the module is programmable to provide a tick rate of 1 MHz or 10 MHz with a clock accuracy of ±1 ppm or ±0.0001%. The counting accuracy depends on the time base accuracy as well as the monitoring resolution. The longer the observation window, the higher the accuracy. The overall accuracy is determined by the following formula:

Accuracy (%) = (100 x (1 - (1 - clock accuracy/100) x (1- 1/(clock rate x observation period)))

With a clock rate of 10 MHz and an observation period of 10 milliseconds (0.01 s), the accuracy is:

0.00110 % = 100 x (1 - (1 - 0.0001/100) x (1 - 1/(10,000,000 x .01)))

Excluding any inaccuracy (jitter) in the signal itself, Table 3-1 indicates the accuracy obtained for various clock rates and observation periods.

Observation Period (ms)	Accuracy (%) (1 MHz Clock)	Accuracy (%) (10 MHz Clock)
1	0.1001	0.01010
10	0.0101	0.00110
100	0.0011	0.00020
1000	0.0002	0.00011

Table 3-1 Overall accuracy for various observation periods and clock rates

Input Paths

The analog input path associated with each channel contains a differential input for high noise immunity. Each path has the switch-selectable option of unterminated or terminated. For most applications, the unterminated selection (the factory-set default) will be chosen. A 100-ohm termination can also be selected for each of these paths for use with RS-422, RS-485 or similar differential transmitters. If this module is the only (or last) receiver node on an RS-422 or an RS-485 path, the 100-ohm termination should be switched IN.

The analog input circuit is shown in Figure 3-4. The input circuit consists of a 47 kohm series resistor in each leg, diode clamps to ±10 volts and a pair of one-megohm resistors to ground. Also, AC coupling can

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be program selected by adding a pair of 1 microfarad capacitors in series with the inputs. This circuit drives a programmable instrumentation amplifier. The diode clamps protect the input circuit and "clip" the input signal peaks with an absolute value greater than +10 or -10 volts. The 1 megohm input impedance decreases to 47 kohm for voltages above ±10 volts. A 100 ohm resistor can provide termination for RS-422 or RS-485 differential paths. All of the analog inputs can be disconnected from the input connector and connected to a common "health check" bus. A known frequency source can be connected to the health check input to verify module operation.

Figure 3-4 A detailed view of the analog differential input circuit

Table 3-2 shows the recommended input ranges and associated input thresholds for the two V635 options. To provide a safety margin, the actual switching threshold is approximately 30% of the input range minimums shown in the table (±60 mV for the *±200 mV to 20 V* range, for example). The input threshold tolerance is ±5%. The Input Range from this table should be used as a guide for setting the internal gain. A gain value higher than needed will result in a lower switching threshold and poorer noise immunity. A gain that is too low could cause input pulses to be missed. If a V635 analog channel is used as an RS-422 or RS-485 receiver, the gain should be selected to the ±200 mV to 20 V range. The gain is selectable on a per-channel basis.

Internal Gain	V635-AAyz Input Range	V635-AAyz Threshold	V635-AByz Input Range	V635-AByz Threshold
1	±200 mV to 20 V	±60 mV	±1 V to 20 V	±300 mV
2	±100 mV to 20 V	±30 mV	±500 mV to 20 V	±150 mV
5	±40 mV to 20 V	±12 mV	±200 mV to 20 V	±60 mV
10	±20 mV to 20 V	±6 mV	±100 mV to 20 V	±30 mV

Table 3-2 Recommended input ranges and switching thresholds

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For maximum noise immunity, the instrumentation amplifier drives an operational amplifier that is configured for differential hysteresis. This means that, once the signal reaches the positive switching threshold (+60 mV, for example), it must reach the negative switching threshold (-60 mV, for example), before the output will switch again. This is shown in Figure 3-5. Note that the higher voltage threshold in (a) causes the circuit to ignore the unwanted zero-crossing, while the lower threshold voltage in (b) produces spurious results. Therefore, we recommend the highest threshold setting that gives sufficient voltage margin. The recommended settings for various voltage ranges are shown in Table 3-2.

Figure 3-5 The effect of threshold voltage setting with a signal having multiple transitions

AC Input Considerations

DC coupling is appropriate for most applications. However, if the input signal on a channel has a sufficient DC offset that there is little or no zero crossing margin, then that channel can be programmed for AC coupling. With AC coupling the input signal will "float" to a value to provide an equal integrated voltage verses time above and below zero. It will not be centered around zero if the signal is very asymmetric. Also, AC coupling increases the effective threshold voltage at very low frequencies. This is shown in Table 3-3. For example, the actual threshold voltage will be about 128% of the DC threshold voltage at 0.2 Hz for input signals approximating a sine wave.

Frequency (Hz)	Threshold Multiplier
.05	3.34
0.1	1.88
0.2	1.28
0.5	1.05
1.0	1.01
>1.0	1.00

Table 3-3 Decrease in input sensitivity at very low frequencies with AC coupling

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Input Connections

The recommended input connections for one channel are shown in Figure 3-6. The connections from a typical ground-connected transducer to a differential analog input are shown in (a), while connections from an RS-422 or RS-485 transmitter are shown in (b). Note that the shield is connected to ground at *both* ends. This reduces noise pickup and does not create a "bad" ground loop because shield is not a signal-carrying conductor. For more information on ground loops, refer to the *Data Acquisition Handbook*, by J. W. Tippie, found on the Internet at **http://www.kscorp.com/www/tech_rep/pdf/cal.pdf**. There can be one cable shield per channel or a single overall shield for the entire cable. Figure 3-9 (c) shows the recommended connections for a TTL input. Note that each TTL input is terminated with a 220Ω/330Ω termination within the V635. This requires a minimum of 23 mA current sinking capability on the external driver.

Figure 3-6 Recommended connections for the analog and TTL channel input paths

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Communicating with the Module

The module is arranged to provide efficient access to the count information. As indicated earlier, there are two register interfaces for the count data from each channel, the *Period Count* register and the *Tick Count* register. These registers are implemented in fast static RAM and appear as an array of sixteen 32-bit words to the VXIbus interface (eight words for the 4-channel versions of the module).

When the module is operating in continuous mode, this memory array represents the current value of the data for all channels, and reading this data can be totally asynchronous from the acquisition of the data. This operation is gapless (The count period for observation *n+1* begins at the same clock tick as the count period for observation *n* ends.) When the count information from a channel is acquired, that information is deposited in the RAM memory. Since this memory is dual-ported (written with the count information and read from VXIbus), it is protected from conflicts. If data is being written, and a VXIbus read operation is requested, the VXI handshake response is delayed until the internal write operation is complete. Also, if a VXI read operation from the memory is in progress, writing to the memory is delayed until the VXI operation is completed. This also guarantees that the period count and the tick count are from the same observation period.

Five Operational Registers in **A32** space are used to configure the various programmable options in the module. For more details, refer to Chapter 4. These read/write registers are:

- *Setup*—includes bits to clear the Operational Registers, enable the insertion of a "health check" signal, select single or continuous mode, select the clock rate, and set the observation window period for the entire module.
- *Filter Select*—inserts or removes a 50 kHz lowpass filter on a per-channel basis..
- *Coupling Select*—chooses AC or DC coupling on a per-channel basis.
- *TTL Input Select*—chooses the TTL or differential analog paths for inputs on a per-channel basis.
- *Gain Select*—chooses from four gain options, thereby setting the input threshold for the differential inputs, on a per-channel basis.

Two additional **A32** registers are related to the count status for the various channels. They are:

- *Clear Count Status*—contains bits to clear the Stale Data and Overflow bits in the *Count Status* register. This is a write-only register.
- *Count Status*—contains bits related to stale data and tick counter overflow for the various channels. This is a read-only register.

Stale data is defined as data that has not been updated since it was previously read. Therefore a Stale Data bit is set when a channel is read and cleared when the counter data is written to the RAM memory for that channel. A tick counter overflow occurs when the input frequency is sufficiently low (below 0.6 Hz with a 10 MHz clock or below 0.06 Hz with a 1 MHz clock). An Overflow bit remains set until cleared by a bit in the *Clear Count Status register* or by a module clear operation. Both stale data and counter overflow can occur in a system that is operating normally. You can use the data from the *Count Status* register to meet your particular requirements.

If you wish to store the stale data and overflow information along with the period and tick counts for the input channels, the most time-efficient sequence would be a **D32** block-read operation, starting with the *Count Status* register, followed by the *Period Count* and *Tick Count* registers. These registers are at contiguous addresses. Refer to Chapter 4 for more information.

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V635 Specifications

Item	Specifications
Inputs	
Number of input channels	8
Type	Differential and TTL
Differential inputs:	
Coupling	AC or DC, per-channel programmable
Input impedance (switchable)	1 MΩ /100 Ω (DC coupling), >10 MΩ /100 Ω (AC coupling)
Input range (per-channel programmable)	V635-AA21: ±20, 40, 100, 200 mV to ±20 V (all ranges) V635-AB21: ±100, 200, 500, 1000 mV to ±20 V (all ranges) (Max further limited to ±5 V with the 100 Ω termination active)
Switching threshold	30% of input range minimums as shown above (typical)
Hysterisis	After a positive-going signal passes the positive threshold, the signal must pass the negative-going threshold to cause switching.
Input protection	47kΩ series resistors followed by ±10 V diode clamps
Common-mode input voltage	±10 V MAX (operating)
Maximum safe input voltage	±50 V, continuous (AC or DC coupling)
Frequency measurement range	0.06 Hz to 50 kHz (1 MHz clock) 0.6 Hz to 50 kHz (10 MHz clock)
Filtering	
Filter type	Single-pole, low-pass RC type, programmable (filter in/out)
-3 dB cutoff frequency (f_c)	50 kHz
Time Base	
Clock rate	1 MHz or 10 MHz, programmable
Stability	±1 ppm, +10°C to +50°C
Observation Window	From 1 ms to 1.024 s, in 1 ms increments
Counter Sizes	
Time base counter	16,777,215 (24 bits)
Input pulse counter	262,140 (18 bits)
Input Connector Types	25P "D" (analog), 15P "D" (TTL), 9P "D" (Health Check)
Power Requirements	
+5 V	
+24 V	
-24 V	
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Table 3-4 Specifications

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Front Panel

LEDs

Active

Illuminated when the module is enabled to acquire data (a single scan is in progress or the module is in continuous scanning mode).

Add Rec

Illuminated when the module is being accessed.

Int Src

Illuminated as long as the V635 has an interrupt pending.

Connectors

Analog In

This 25-contact "D" connector with pins provides the differential analog input paths for the eight channels.

TTL In

This 15-contact "D" connector with pins provides the TTL input paths for the eight channels.

Health In

This 9-contact "D" connector with pins provides the "health check" input path for the differential input channels.

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Front-panel Connector Pinout

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Chapter 4: Configuration and Operational Registers

Address Space

VXIbus uses the VMEbus protocol for data transfer and therefore supports 32-bit addressing to access I/O slave devices. 32-bit addressing provides direct access to memory space of four Gigabytes.

Slave devices such as VXIbus data acquisition modules exist for a variety of purposes and can be simple or very complex. Communication between host and slave can require access to several registers in one device or access to many Mbytes of memory in another. ("Devices" and "modules" are terms often used interchangeably. The distinction is that more than one VXIbus device *can* reside in a VXIbus module. However, there is generally one device per module.)

To minimize the amount of address-decoding hardware needed, simpler slave devices use addressing modes that fully decode only 16 or 24 address lines rather than 32. Therefore, there are three defined addressing modes…**A16**, **A24** and **A32**…having address spaces of 64 kbytes, 16 Mbytes and 4 Gbytes, respectively.

All VXIbus devices have registers located within 64-byte blocks in **A16** address space and therefore support **A16** addressing. Devices requiring no more than 64 bytes of address space need only support **A16** addressing. Devices needing more than the 64 bytes to accommodate additional registers or blocks of memory *must* also support **A24** or **A32** addressing, but not both.

VXIbus devices that use **A24** or **A32** addressing modes are required to have four registers in **A16** space for parameter definition. One such parameter is Required Memory, which uses four bits (*m*) to specify the size of the memory in **A24** or **A32** space required by the device. A device *may not* use more than one-half of the memory space, and it *should not* use more than one-fourth. Table 5-1 shows the relationship between the four-bit parameter, *m*, and the memory required by the device. Note that *m = 0* defines the case for maximum usage, i.e., half of the memory space. Required Memory is specified in bits 15 – 12 in the Device Type register at offset 02h.

m	Required Memory				*m*	Required Memory			
	A24		A32			A24		A32	
0	8	Mbytes	2	Gbytes	**8**	32	kbytes	8	Mbytes
1	4	"	1	"	**9**	16	"	4	"
2	2	"	512	Mbytes	**10**	8	"	2	"
3	1	"	256	"	**11**	4	"	1	"
4	512	kbytes	128	"	**12**	2	"	512	kbytes
5	256	"	64	"	**13**	1	"	256	"
6	128	"	32	"	**14**	512	bytes	128	"
7	64	"	16	"	**15**	256	"	64	"

Table 5-1. Relationship between the "*m*" Parameter and Required Memory

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One of the four registers is the Offset register, which is needed only for devices using **A24** or **A32** address space. This 16-bit read/write register defines the base address of the device's **A24** or **A32** operational registers. The *m+1* most significant bits of the Offset register provide the values of the *m+1* most significant bits of the device's **A24** or **A32** register addresses, where *m* is as defined in Table 5-1 above.

Static and Dynamic Configuration

A VXIbus system can have up to 255 devices. Therefore, eight bits define the device address, which is called the "Logical Address." The Logical Address can be "static" or "dynamic." A static address resides in an 8-bit switch register; a dynamic address resides in a write-only register. Setting the switch register to 255 (all **"1"**s) causes dynamic addressing to be enabled. Any other setting enables static addressing, in which case the value held in the switch register is the Logical Address.

With the Logical Address set to 255, a device responds to accesses at address 255 only when the MODID line is asserted as a qualifier by the Slot-0 controller. After a new Logical Address is written to the device, the device responds to the new address independent of the state of the MODID line.

For data acquisition and control applications, dynamic configuration is an important concept. A system often contains more than one module of a given type, and it can be easy, and sometimes desirable, to swap positions of two modules after removing them from the mainframe. If dynamic configuration is not employed, one must make sure that the switch register is correctly set when inserting or re-inserting a device. Dynamic configuration greatly simplifies system setup, since the software can assure that the devices are located in the desired slots. Dynamic configuration also allows a system's Resource Manager to configure memory usage optimally in a system.

Communication Protocol

VXIbus allows communication over the backplane by either register-based or message-based protocols. With register-based protocol, the communication is via an 8-, 16- or 32-bit parallel path directly to I/O registers within the modules. With message-based protocol, an ASCII interpreter is included on each module, and the binary representations of ASCII characters are transmitted over the backplane. The advantage of message-based protocol is that English-like commands and responses can be used.

High-performance data acquisition and control modules are usually register-based because the data throughput is usually several orders of magnitude greater than with message-based devices. All Kinetic-Systems VXIbus devices are register-based.

Register Addressing

The user assigns each device in a VXIbus system a unique number between 1 and 254. This 8-bit number, called the Logical Address, defines the base address for the VXIbus device registers located on the module. Each device has a 64-byte block of memory reserved for these registers. The memory blocks, called configuration space, are located in the upper 16 kbytes of the 64-kbyte **A16** address space.

Every device has at least three configuration registers: ID / Logical Address, Device Type, and Status / Control. Modules using **A24** or **A32** addressing must also have an Offset register. The rest of the 64-byte block can contain registers or memory appropriate for the operation of the specific device.

A device's Logical Address occupies bits 13 - 6 of the register address. Bits 15 and 14 of the address are

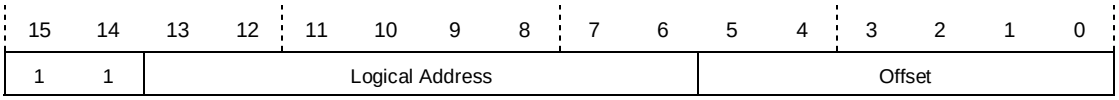
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both **"1**'s,**"** and the base address of the register block is therefore:

***V**40h+C000h**

where *V* is the Logical Address of the device and C000h is the starting address of the top 16-kbyte block.

The address of a specific register is the base address plus an offset address. The offset is bits 5 - 0 of the register address and ranges from 00h to 3Eh.



The V635 also uses *operational* registers in **A32 space; therefore,** it is an "Extended" register-based device.

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Required Configuration Registers

The four required VXIbus registers are ID / Logical Address, Device Type, Status / Control, and Offset. You can access these registers by **D16** transfers only.

ID Register *00h*

This read-only register returns 5F29h.

Fields are Device Classification, Addressing Mode and Manufacturer ID.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	1
	Class = Extended		**Addressing Mode = A32**		**KineticSystems' Manufacturer ID = F29h (3881)**											

Device Classification *Bits 15 and 14*

00 Memory device

01 Extended device

10 Message-based device

11 Register-based device

The V635 is an *Extended device.*

Addressing Mode *Bits 13 and 12*

00 **A24**

01 A32

10 Reserved

11 **A16**

The V635 uses *A32 addressing.*

Manufacturer ID *Bits 11 through 0*

KineticSystems' Manufacturer ID is *3881*, which corresponds to F29h.

Logical Address Register *00h*

This write-only register holds the Logical Address. In systems using Dynamic Configuration, the system Resource Manager uses this register to set the Logical Address of the device.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	Not Used								Logical Address							

Logical Address *Bits 7 through 0*

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Device Type Register 02h

This read-only register contains the Required Memory and Model Code for the V635. It returns F635h.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	0	1	1	0	0	0	1	1	0	1	0	1
	Required Memory (*m*)								**Model Code = 635h**							

Required Memory Bits 15 – 12

A value of **Fh** is returned (*m* = 15 decimal), indicating that the V635 is allocated 64 kbytes in **D32** space.

Model Code Bits 11 – 0

The model code for the V635 is 635h.

Status Register 04h

This read-only register provides binary information about the status of the V635.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	A32 Active	MODID*	Not Used										Ready	Passed	Sysfail Inhibit	Soft Reset

A32 Active Bit 15

"**1**" in this field indicates that the **A32** registers of the V635 can be accessed. This bit reflects the state of the Control register's **A32** Enable bit.

MODID* Bit 14

"**1**" in this field indicates that the V635 is *not* selected via the P2 MODID line. A "**0**" indicates that the device is selected by a high state on the P2 MODID line. The Resource Manager uses this bit to configure the V635 dynamically.

Ready Bit 3

"**1**" in this field indicates that the registers have been successfully initialized. The V635 is ready for access.

Passed Bit 2

"**1**" in this field indicates that the device self-test has passed. A "**0**" indicates that the V635 has failed—or is currently executing—its self-test.

Sysfail Inhibit Bit 1

"**1**" in this field indicates that the V635 is disabled from driving the SYSFAIL* line. This bit reflects the state of the Sysfail Inhibit line in the Control register.

Soft Reset Bit 0

"**1**" in this field indicates that the V635 is in a reset state. While in this state, the V635 will allow access

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only to its Configuration registers.

Control Register *04h*

This write-only register causes execution of specific actions by the V635.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	A32 Enable	Not Used													Sysfail Inhibit	Soft Reset

A32 Enable *Bit 15*

Setting this bit to "**1**" enables access of the **A32** registers of the V635.

Sysfail Inhibit *Bit 1*

Setting this bit to "**1**" disables the V635 from driving the SYSFAIL* line.

Soft Reset *Bit 0*

Setting this bit to "**1**" forces the V635 into a reset state.

Offset Register *06h*

This read/write register determines and reports the device base address in **A32** memory space.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Base Address in A32 memory space								0	0	0	0	0	0	0	0

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Additional Configuration Registers

Additional configuration registers are:

- Attribute register
- Serial Number High & Low registers
- Version Number register
- Interrupt Status register
- Interrupt Control register
- Subclass register, and
- Suffix High & Low registers.

Note that you can access these registers by **D16** transfers only.

Attribute Register *08h*

This read-only register provides low-true information about the V635's interrupt handling capabilities. A read of this register returns FFFAh.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
	Reserved													**Interrupt Capability***	**Interrupt Handler Control***	**Interrupt Status Reporting***

Reserved *Bits 15 - 3*

These bits are reserved for future use and return **"1"**s when read.

*Interrupt Capability** *Bit 2*

"**0**" signifies that the V635 is capable of generating interrupts.

*Interrupt Handler Control** *Bit 1*

"**1**" indicates that the V635 is *not* capable of Interrupt Handler Control.

*Interrupt Status Reporting** *Bit 0*

"**0**" indicates that the V635 has Interrupt Status Reporting capability.

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Serial Number Register *0Ah, 0Ch*

The read-only Serial Number registers (high and low words) store the 32-bit hexadecimal value of the V635's decimal serial number.

0Ah

	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Read-only	SN7	SN6	SN5	SN4

High word

0Ch

	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Read-only	SN3	SN2	SN1	SN0

Low word

Version Number Register *0Eh*

This read-only register gives the hardware and firmware revision numbers of the module.

	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Read-only	Firmware Version	Firmware Revision	Hardware Version	Hardware Revision

Firmware Version ***Bits 15 - 12***

Firmware Revision ***Bits 11 - 8***

Hardware Version ***Bits 7 - 4***

Hardware Revision ***Bits 3 - 0***

Each field is a four-bit integer indicating the version or revision number.

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Interrupt Status Register *1Ah*

This read-only register provides information about the state of the Overflow interrupt source. It can be used for polling of interrupts. Interrupt bits are cleared by a read of this register or by an interrupt-acknowledge cycle.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	0	0	0	0	0	0	Ovrflw	Logical Address							

Interrupt Source *Bit 8*

A "**1**" in this bit location indicates that one of the Overflow bits in the Stale-data/overflow register has been set and can cause an interrupt. The actual Overflow bits are cleared by the Clear Stale-data/overflow register. These registers are at **1Ch** and **14h**, respectively, in **A32** Operational Register space.

Logical Address *Bits 7 - 0*

During a read operation, these bits return all "1's." During an interrupt acknowledge cycle, these bits return the V635's Logical Address.

Interrupt Control Register *1Ch*

The read/write register contains mask bits for the interrupt source, a bit for disabling interrupts and three bits that determine interrupt level. All of the bits in this register are set to **"1"** on the assertion of SYSRESET or if the *Soft Reset* bit in the Status/Control register is written with a **"1."**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	1	1	1	1	1	1	1	Ovrflw	EN*	1	Interrupt Req. Level			1	1	1

Interrupt Mask Bit *Bit 8*

Writing a "**1**" to this bit *prevents* the Overflow interrupt source from generating an interrupt request. Writing a **"0"** enables an interrupt source to generate an interrupt request.

Interrupt Enable *Bit 7*

Writing a "**1**" to this bit disables interrupt generation. Writing a **"0"** enables interrupt generation.

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Interrupt Request Level ***Bits 5 - 3***

These bits determine the interrupt request level.

Bits 5	Bits 4	Bits 3	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

Table 5-3. Interrupt Request Levels

Not Used ***Bits 2 – 0***

Bits 2 – 0 are not used and return **"1"**s when read.

Subclass Register *1Eh*

This read-only register provides information about the Subclass of the VXIbus device.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	Extended Device	**Extended Register-based Device**														

Bit 15 indicates that the V635 is a VXIbus-defined Extended Device.

Bits 14 through 0 indicate that the V635 is an Extended Register-based Device.

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Suffix Register *20h, 22h*

The Suffix read-only register (high and low words) hold the ASCII codes for the four characters of the V635's suffix. The suffix defines the optional characteristics of the module.

20h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	1	0	0	0	0	0	1	0	1	0	0	0	0	x	x

ASCII code for A = 41h (1st character) **ASCII code for A or B = 41h or 42h (2nd character)**

22h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	0	1	1	0	0	x	x	0	0	1	1	0	0	x	x

ASCII code for 1 or 2 = 31h or 32h (3rd character) **ASCII code for 1, 2, etc. = 31h, 32h, etc. (4th character)**

The suffix options for the V635 are:

1st character: **"A"** for all options

2nd character: Input Range

"A" indicates an input range from ±20 mV.

"B" indicates an input range from ±100 mV.

3rd character: Number of Channels

"1" indicates a module with 4 input channels.

"2" indicates a module with 8 input channels.

4th character: Revision level

The number, **"1," "2,"** etc., gives the module revision level.

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Operational Registers in A32 Space

The following operational registers are in **A32** space beginning at a starting address specified by the Offset register in **A16** configuration space. The hexadecimal addresses shown are the offset from the starting address. You can access these registers by **D16** or **D32** transfers. Any register bit that is shown as **"0"** is always read as **"0"** regardless of the data that is written to it. *For the 4-channel versions of this module, only the bits representing Channels 1 to 4 are used.*

Setup Register *00h*

This read/write register selects the primary setup parameters for the module.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/write	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	Clear Reg	Health Enable	Exec Single	Cont Scan	Tick Clock	Observation Window Select (1 to 1024 ms)									

For **D16** transfers, Bits 15-0 are accessed at **02h**.

Clear Reg *Bit 14*

Set this bit to **"1"** to clear all of the A32 Operational registers in the module, including the Setup register, but excluding the Period Count and Tick Count registers. This bit is also cleared by this operation. If the *Clear Reg* bit set to **"1,"** SYSRESET is asserted or if the *Soft Reset* bit in the Status/Control configuration register is written with a **"1,"** the module is placed in the following state:

- The differential inputs are connected to the input connector, not the "health check" input.
- The module is set to Single Scan mode.
- The internal clock is set to 10 MHz.
- The Observation Window is set to 1 millisecond.
- The 50 kHz low-pass filters are OUT (inactive).
- The differential input coupling is DC for all channels.
- The differential input channels are enabled.
- The internal gain is set to **1** for all channels (*±200 mV to 20 V* for a V635-AAyz or *±1 V to 20 V* for a V635-AByz module).
- The Stale Data and Overflow bits are cleared in the *Count Status* register.

Health Enable *Bit 13*

Set this bit to **"1"** to disconnect the differential inputs for all of the channels from the input connector and to connect these inputs to the external "health check" signal. This allows the use of a precision frequency source to check the counting integrity of the module. Set this bit to **"0"** to connect the differential inputs to their respective input paths for normal operation of the module. The TTL input paths are not affected by this selection.

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Exec Single *Bit 12*

Set this bit to **"1"** to initiate a single scan of all the channels. Once all channels have been scanned, this bit is cleared to **"0."** The scan of any channel will not begin until an input transition has occurred after a window "edge." For this bit to perform any action, **Bit 11** must be set to **"0,"** indicating that *Single Scan* mode has been selected.

Cont Scan *Bit 11*

Set this bit to **"1"** to place the module in *Continuous Scan* mode. In this mode, the count information for each of the channels is updated automatically at a rate set by Observation Window Select, **Bits 9-0**, or by the input frequency of a particular channel if one period of that signal is longer than one observation window period. Set this bit to **"0"** to place the module in *Single Scan* mode, with a scan initiated by setting **Bit 12** to **"1."**

Tick Clock *Bit 10*

Set this bit to **"1"** to select a 1 MHz internal clock, to **"0"** to select a 10 MHz internal clock. The advantage of the 10 MHz clock is that it provides a ten-fold increase in resolution, thereby increasing counting accuracy. Its only disadvantage is that the lower counting limit is 0.6 Hz, compared with 0.06 Hz for a 1 MHz internal clock.

Observation Window Select *Bits 9-0*

Use the Observation Window Select bits to set the period of the observation window with **Bit 9** as the MSB and **Bit 0** as the LSB.. The valid range for this clock is 1 to 1024 milliseconds *in increments of 1 millisecond*. The decimal representation of the bit selection is given by the formula:

Observation Window Select = Desired window clock period in milliseconds - 1

Therefore the range of the selection for 1 to 1024 ms is 0 to 1023 decimal (000h to 3FFh). Some of the more common selection periods are shown in Table 4-1.

Period (ms)	Selection (Hex)	Period (ms)	Selection (Hex)
1	000	50	031
2	001	100	063
5	004	200	0C7
10	009	500	1F3
20	013	1000	3E7

Table 4-1 Selection values for common Observation Window periods

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Filter Select Register *04h*

This read/write register enables and disables the low-pass filters for the differential-input signal paths.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/write	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1
									Filter Select							

For **D16** transfers, Bits 15-0 are accessed at **06h**.

Ch x Filter Select *Bits 7-0*

Set these bits to **"1"** to enable the low-pass filters for differential input channel 8 through channel 1, respectively. Set these bits to **"0"** to disable the filters on the associated channels. Each single-pole passive filter provides a voltage attenuation of about 3 dB (approximately 30% attenuation) at 50,000 Hz. These filters improve the immunity to high-frequency noise. They should be enabled on any channel where the expected input frequency for the associated channel will not exceed 50,000 Hz, and they should be disabled if the input frequency will exceed 50,000 Hz. Note that these filters do not affect the TTL input paths.

Coupling Select Register *08h*

This read/write register selects AC or DC coupling for the differential-input signal paths.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/write	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1
									AC Coupling Select							

For **D16** transfers, Bits 15-0 are accessed at **0Ah**.

Ch x AC Coupling Select *Bits 7-0*

Set these bits to **"1"** to select AC coupling for differential input channel 8 through channel 1, respectively. Set these bits to **"0"** to select DC coupling on the associated channels. When AC coupling is selected on any channel, a 1 microfarad non-polarized capacitor is placed in series with each leg of the differential input with a 1 megohm load to ground. DC coupling should generally be used unless there is a substantial DC offset on the input signal.

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TTL Input Select Register *0Ch*

This read/write register selects the TTL-input or the differential-input signal paths.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/write	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1
									TTL Input Select							

For **D16** transfers, Bits 15-0 are accessed at **0Eh**.

Ch x TTL Input Select *Bits 7-0*

Set these bits to **"1"** to enable the TTL input paths for Channels 8 through 1, respectively. Set these bits to **"0"** to enable the differential input paths.

Gain Select Register *10h*

This read/write register the signal gain for the differential-input signal paths.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read/write	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Ch 8 Gain		Ch 7 Gain		Ch 6 Gain		Ch 5 Gain		Ch 4 Gain		Ch 3 Gain		Ch 2 Gain		Ch 1 Gain	

For **D16** transfers, Bits 15-0 are accessed at **12h**.

Ch x Gain Select *Bits 7-0*

These two-bit fields select the internal gain of the differential input paths for Channels 8 through 1, respectively. Table 4-2 indicates the input signal range for each gain setting:

Gain Selection Bit Pattern	Internal Gain	V635-AAyz Input Range	V635-AByz Input Range
00	1	±200 mV to 20 V	±1 V to 20 V
01	2	±100 mV to 20 V	±500 mV to 20 V
10	5	±40 mV to 20 V	±200 mV to 20 V
11	10	±20 mV to 20 V	±100 mV to 20 V

Table 4-2 Input ranges for various internal gain settings

To provide a safety margin, the actual switching threshold is approximately 30% of the input range minimums shown above (±60 mV for the *±200 mV to 20 V* range, for example). The Input Range from this table should be used as a guide for setting the internal gain. A gain value higher than needed will result in a lower switching threshold and poorer noise immunity. A gain that is too low could cause input pulses to

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be missed. If a V635 analog channel is used as an RS-422 or RS-485 receiver, the gain should be selected to the ±200 mV to 20 V range.

Clear Count Status Register 14h

This write-only register selectively clears the corresponding bits in the Count Status register.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write-only	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1
	Clear Stale Bit								Clear Overflow Bit							

For **D16** transfers, Bits 15-0 are accessed at **16h**.

Ch x Clear Stale Bit Bits 15-8

Set these bits to **"1"** to provide a selective clear of the corresponding Stale Data bits in the Count Status register. These bits then clear themselves. Setting any of these bits to **"0"** has no effect on the corresponding Count Status register bits. *These bits are provided for factory test purposes.*

Ch x Clear Overflow Bit Bits 7-0

Set these bits to **"1"** to clear the corresponding Overflow bits in the Count Status register. These bits then clear themselves. Setting any of these bits to **"0"** has no effect on the corresponding Count Status register bits.

Count Status Register 1Ch

This read-only register contains the status of stale data and tick counter overflow.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read-only	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1
	Stale Data								Overflow							

For **D16** transfers, Bits 15-0 are accessed at **1Eh**.

Ch x Stale Data Bits 15-8

Any of these bits are set to **"1"** under the following conditions:

- Data for that channel has been read (an access to the *Period Count* and/or to the *Tick Count* register for that channel).
- In *Single Scan* mode: That channel has not been updated yet.

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Any of these bits are set to "**0**" under the following conditions:

- The count information for that channel has been updated with fresh data.
- Writing a "**1**" into the associated bit location in the *Clear Count Status* register. This is primarily for factory test purposes.

Ch x Overflow ***Bits 7-0***

When any one of these bits is **"1"** it indicates that the time base tick counter for the corresponding channel *has* overflowed since the last time this bit was cleared. When any one of these bits is **"0"** it indicates that the time base tick counter for the corresponding channel *has not* overflowed since the last time this bit was cleared.

Period Count Registers *20h (Channel 1)*

These read-only registers contain the number of input signal periods counted in the observation window.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read-only	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Period Count (Bits 17-16)	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Period Count (Bits 15-0)															

For **D16** transfers, Bits 31-16 are accessed at **20h**, and Bits 15-0 are accessed at **22h**.

Period Count ***Bits 17-0***

There are eight Period Count registers, one for each input channel. The associated counters are 18 bits in length. Each of these registers contains the current value for the number of periods of the input signal counted in the actual observation period. The maximum count stored is 262,143 decimal (3FFFFh). Refer to Table 4-3 below for the offset addresses of the Period Count registers for all channels.

Tick Count Registers *24h (Channel 1)*

These read-only registers contain the number of time base periods counted in the observation window.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read-only	0	0	0	0	0	0	0	0	Tick Count (Bits 23-16)							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tick Count (Bits 15-0)															

For **D16** transfers, Bits 31-16 are accessed at **24h**, and Bits 15-0 are accessed at **26h**.

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Tick Count ***Bits 23-0***

There are eight Tick Count registers, one for each input channel. The associated counters are 24 bits in length. Each of these registers contains the current value for the number of periods (ticks) of the time-base clock counted in the actual observation period. The maximum count stored is 16,777,215 decimal (FFFFFFh). Refer to the following table for the offset addresses of the Tick Count registers. If an observation results in a period count overflow, all bits in the *Period Count* and *Tick Count* registers set to **"0."** Since the frequency calculation includes the division of the period count by the tick count, the *Tick Count* register should be checked to determine that it is not zero before the calculation is performed.

Period Count and Tick Count Register Address Map

The following table indicates the **D32** offset addresses for the eight Period Count registers and the eight Tick Count registers (Only Channels 1-4 are used with the 4-channel versions of this module.). The values in parenthesis represent the offset addresses (upper word, lower word) for **D16** transfers.

Input Channel	Period Count	Tick Count
1	20h (20h, 22h)	24h (24h, 26h)
2	28h (28h, 2Ah)	2Ch (2Ch, 2Eh)
3	30h (30h, 32h)	34h (34h, 36h)
4	38h (38h, 3Ah)	3Ch (3Ch, 3Eh)
5	40h (40h, 42h)	44h (44h, 46h)
6	48h (48h, 4Ah)	4Ch (4Ch, 4Eh)
7	50h (50h, 52h)	54h (54h, 56h)
8	58h (58h, 5Ah)	5Ch (5Ch, 5Eh)

Table 4-3 Period Count and Tick Count address map

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Chapter 5: Programming Information

An example procedure to set up the module and acquire count information

This example sets up the V635 then reads the module for period count and tick count data. The setup conditions are:

- Continuous scan
- 10 MHz clock
- 100 ms observation window
- 50 kHz filters IN for all channels
- DC coupling
- Differential input
- Operating range = ±100 mV to 20 V operating range (V635-AAyz): *Internal gain = 2*

Module Setup
Get the base address for the V635 Operational registers, which are all in A32 space. Read the Offset register at 06h (**A16** space) to get the **A32** offset. Logical shift the result 16 places to the left to get the V635 base address.
*The registers that follow are all in A32 space. This sequence assumes **D32** transfers.* **Clear the operational registers.** Write 4000h to the *Setup* register at 00h.
Set Continuous Scan and 10 MHz Clock; set the Observation Window to 100 ms. Write 0863h to the *Setup* register at 00h.
Set the 50 kHz filters IN for all channels. Write 00FFh to the *Filter Select* register at 04h.
Select DC coupling for all channels. Write 0000h to the *Coupling Select* register at 08h.
Select differential inputs for all channels. Write 0000h to the *Coupling Select* register at 0Ch.
Select an internal gain of 2 for all channels. Write 5555h to the *Gain Select* register at 10h.

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Read Period and Tick Count Data
*The registers that follow are all in A32 space. This sequence assumes **D32** transfers. The data can be read as a contiguous block.*
Read the Count Status data. Read the *Count Status* register at 1Ch.
Read the Period Count data for Channel 1. Read the *Period Count* register at 20h.
Read the Tick Count data for Channel 1. Read the *Tick Count* register at 24h.
Read the data for the remaining channels that are in use. Read the *Period Count* and *Tick Count* registers for the remaining channels.
Continue scanning. If in a scanning environment, repeat the above sequence at the periodic rate of the scan.

Calculate Frequency
This sequence involves the reading of host computer memory. It can be performed as the count data is read, or it can be executed on archived data.
Determine if the Tick Count data for channel *n* is zero or nonzero. If the Tick Count data for Channel *n* is *zero*, store a frequency of **0 Hz** (decimal) and proceed to the next channel. If *nonzero*, perform the next step.
Calculate the frequency for Channel *n*. The frequency is calculated by the following formula: . **Frequency (Hz) = Clock Rate (Hz) x Period Count/Tick Count**
Repeat the above for other channels.

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Appendix: About KineticSystems

KineticSystems Corporation designs, produces and markets high-performance data acquisition and control systems to a broad range of customers in aerospace, defense, automotive, scientific and other industrial markets.

The Leader in the Delivery of High-performance CAMAC-based Products

The company was founded in 1970 to develop and manufacture interface modules and associated products based on the international CAMAC standard. CAMAC, an acronym for Computer Automated Measurement and Control, is a set of specifications developed by a committee of the government-sponsored research laboratories (the NIM Committee). The committee's goal was to provide standardized modular building blocks for configuring a wide range of data acquisition and control systems. CAMAC, the first open-system real-time input/output (I/O) specification, later was accepted as a standard by the Institute of Electrical and Electronic Engineers (IEEE STD 583). We soon became the recognized leader in delivering high-performance CAMAC-based products. We have retained that leadership position.

Innovation with the CAMAC Serial Highway

As the need for large distributed data acquisition and control systems grew, the NIM Committee produced specifications for the CAMAC Serial Highway to allow communication between a host computer and CAMAC I/O chassis over some distance. In 1975, we delivered the first CAMAC Serial Highway computer interface. We soon were recognized as the leader in the delivery of Serial Highway system components. Serial Highway innovations included a block-mode protocol that increased data throughput by a factor of 10 and fiber-optic highway interfaces that allow the CAMAC chassis to be separated by up to 2 kilometers at full data rate. We continue to be an innovator in the field of high-performance data acquisition.

H•TMS, a Turn-key Testing Solution, Added to Our Product Range

In 1991, we purchased the H•TMS (High-performance Test Management System) product line. H•TMS is a modular set of microprocessor-based hardware and software components that delivers functions usually found in several instruments and a computer. H•TMS increases testing productivity and provides solutions to key problems encountered by test engineers and managers. The addition of this product line provides the answer for customers who need a turnkey testing solution.

A Major Player in VXIbus, a Rapidly Growing Interface Standard

VXIbus is a standard (now IEEE STD 1155) developed by the major instrumentation manufacturers to allow customers to move from chassis-type instruments to computer-interfaced modular building blocks. In 1992 we embraced the relatively new VXIbus standard. Using our extensive CAMAC experience, we soon produced 35 VXI modules for data acquisition and control. As the VXI market has grown to several hundred million dollars, we continue our innovations with additional high-performance products. This includes the development of a set of products called the Grand Interconnect™. These products allow VXI chassis to be distributed on a fiber-optic highway. CAMAC and mixed VXI/CAMAC chassis are also supported. We are an active member of the VXI *plug&play* Systems Alliance, an organization that promotes standards that make VXI easier to configure and to use.

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KineticSystems Today

Our headquarters and factory facilities in Lockport, Illinois, have grown to 70,000 square feet. We also have an operation in Englewood, Colorado, and six domestic sales offices, including the Lockport facility. We have distributors in 17 other countries. VXI, CAMAC and H•TMS continue to be our major product lines.

Today, an increasing number of customers are demanding the delivery of data acquisition and control solutions, not just products. For many years we have provided software drivers for our products to make them easier to use. We have an active program to develop VXI *plug&play* instrument drivers for our range of VXI modules. We have developed a high-performance software application program called Reality®. Distributed VXI and/or CAMAC systems can be configured using this software. By using UNIX workstations and powerful I/O control computers, a high I/O performance can be achieved that is not available with any other general-purpose software package. Additionally, to achieve more complete solutions, we provide integration services.

KineticSystems is ideally suited to meet customers' needs as we approach the twenty-first century. We have extensive experience in the design, manufacture and delivery of high-performance data acquisition products and systems. Even though the demand for standards-based products has only recently become a high priority, we have the experience with such products since 1970.

Ways to contact us:



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KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems are prepaid by the purchaser, while charges for returning the repaired product to the purchaser, if located in the United States, are paid by KineticSystems. Return shipments are made by UPS, where available, unless the purchaser requests a premium method of shipment at his expense. The selected carrier is not the agent of KineticSystems, and KineticSystems assumes no liability relating to the services provided by the carrier.

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Products are not accepted for credit or exchange without prior written approval. If it is necessary to return a product for repair replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center before shipping the product to KineticSystems.

Please take the following steps if you are having a problem and feel you may need to return a product for service:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include with the product a description of the problem and the name of the technical contact person at your facility.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Corporation

Repair Service Center

900 North State Street

Lockport, IL 60441

Telephone: (815) 838-0005

Fax: (815) 838-4424

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Feedback

The purpose of this manual is to provide you with the information you need to make the V635 as easy as possible to understand and use. It is very important that the information is accurate, understandable and accessible. To help us continue to make this manual as "user friendly" as possible, we hope you will fill out this form and Fax it back to us at (815) 838 0095. Or mail a copy to Ruth McCluskey, KineticSytems Corporation, 900 N. State, Lockport, IL 60441. Your input is very valuable.

Please rate each of the following.

The information in this manual is:

	Yes									**No**
Accurate	10	9	8	7	6	5	4	3	2	1
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Easy to find	10	9	8	7	6	5	4	3	2	1
Well organized	10	9	8	7	6	5	4	3	2	1
Sufficient	10	9	8	7	6	5	4	3	2	1

We would appreciate receiving any thoughts you have about how we can improve this user's manual:

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