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Model V120

FOXI VXI Slot-0 Controller

User's Manual

February 16, 2001

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Model V120
UNPACKING AND INSTALLATION

The Model V120 is shipped in an anti-static bag within a Styrofoam packing container. Carefully remove the module from its anti-static bag and prepare to set the various options to conform to the operating environment.

Logical Address Switches

The V120 is a Slot 0 capable device. It is shipped from the factory configured for Slot 0 operation with its Logical Address Switches statically configured for Logical Address 0. If the V120 is to operate as the Slot 0 device, then its Logical Address must be set for Logical Address 0. If it is not, these switches must be set for Logical Address 1 to 255. Logical Address 255 can be shared by multiple devices in a system that supports Dynamic Configuration. If a non-Slot 0 V120 is to be used in a system that does not support Dynamic Configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating the eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to Figure 1.)

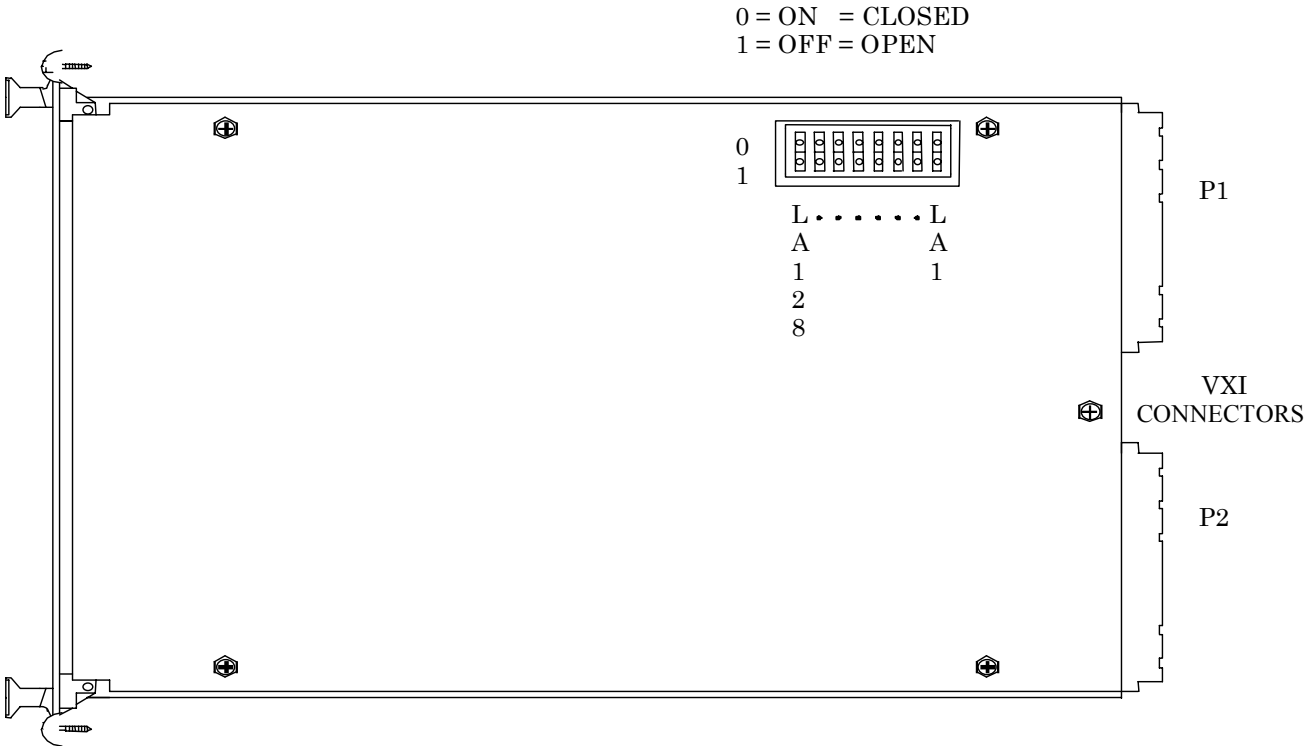


Figure - 1 V120 Logical Address Switches

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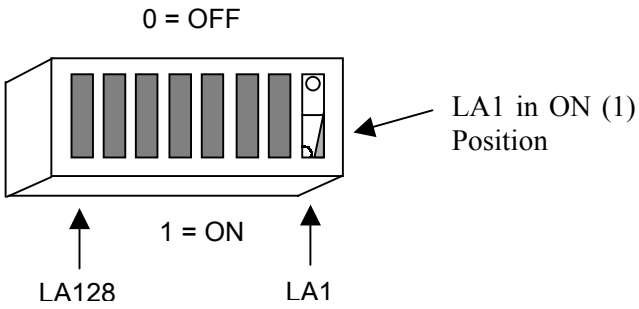


Figure 2 - V120 Switch Locations

These switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value. A switch pushed down on the OPEN side is ON (1). For a Logical Address of zero, all switches should be pushed down on the closed (top as viewed in Figure 1) side.

The Logical Address is used to define the A16 base address of the V120's VXIbus defined configuration registers. Further explanation on calculating this base address can be found in the section on VXIbus Configuration Registers.

Module Insertion

The V120 is a C-sized, single width VXIbus module. This module is shipped from the factory configured for Slot 0 operation. Installing a Slot 0 configured V120 in any other slot (other than Slot 0) can result in damage to it and other components in the system. Refer to the section on V120 Slot 0 Configuration for more information.

At KineticSystems, static precautions are observed from production, test, and packaging of the module. This includes using static proof mats and wrist straps. Please observe these same precautions when unpacking and installing the module whenever possible.

CAUTION: To guard against electrostatic discharge if no wrist straps are available, touch the anti-static bag to a metal part of the VXI chassis before removing the V120.

The Model V120 is shipped in an anti-static bag within a Styrofoam packing container.

The VXIbus backplane must be properly configured before inserting a module and applying power. The Bus Grant and Interrupt Acknowledge daisy chain jumpers should be installed in any unoccupied slot.

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FRONT PANEL INFORMATION

This section describes the connectors, status LEDs, etc., that appear on the front panel and their functions.

Node Address Switch

The Node Address Switch establishes the V120's highway node address. This switch contains two digits in hexadecimal format. Each slave on the highway must have a unique node address, ranging from 1 (01_{16}) to 127 ($7F_{16}$). Node address 0 (00_{16}) is reserved and should not be used.

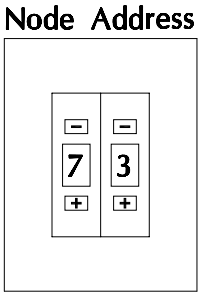


Figure 3 - V120 Node Address Switch

Figure 3 shows the node address switch set to a value of 73_{16} (115). Notice the most significant digit is on the left and the least is on the right.

LEDs

The V120 has eight LEDs located on the front panel to display status information. All LEDs are one-shot extended. Table 1 lists each LED and defines when they are active (lighted).

Table 1. - Status LED Definitions

LED Mnemonic (Color)	Description
Failed (R)	Failed- Onboard DSP is executing or has failed its self-test.
Add Rec (G)	Address Recognized - Transfer to V120's Configuration Registers was successful.
Dmd (R)	Demand - A demand message has been placed in the Demand FIFO.
Sync (G)	Synchronization - Indicates valid highway activity or synchronization message.
Hwy Add Rec (G)	Highway Address Recognized - V120 recognizes that it is the addressed node.
Error (R)	Error - A parity error has occurred on the highway.

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The V120 has a set of front panel connectors used for clocks and triggers. The V120 has four SMB connectors.

SMB Connector Option

All V120-Axxx options have front panel mounted SMBs. Table 2 describes the function of each.

Table 2. - SMB Connector Descriptions

Mnemonic	Description
Clk I/O	10 MHz system clock - Can be configured with straps for input or output.
Trig I/O	Trigger Input/Output - Configured with straps to route a TTL Trigger Line in/ out.
Trig Out B	Internal Trigger Output B signal - See Internal Register description.
Trig Out A	Internal Trigger Output A signal - See Internal Register description.

Each of these signals appears on the center pin of the SMB connector. The shell of these connectors is connected to module ground.

Fiberoptic

The V120's two front panel ST type connectors serve as the input and output for the fiberoptic highway. The connector labeled Hwy In is the highway input. This input should be connected to the highway output connector of the driver or another slave. Conversely, the Hwy Out is the output connector and should be connected to a driver or slave highway input connector. Fiberoptic highway connections should be made using 62.5/100µm fiberoptic cables.

VXIBUS CONNECTORS

The V120 is a C-sized VXIbus module and uses both the P1 and P2 connectors. Tables 3 and 4 list the connections made.

VXI*bus* Connectors P1, P2 Pinouts

Table 3. - VXI*bus* P1 Connector

Pin Number	ROWa Signal Mnemonic	ROWb Signal Mnemonic	ROWc Signal Mnemonic	Pin Number
1	D00	BBSY*	D08	1
2	D01	BCLR*	D09	2
3	D02	ACFAIL*	D10	3
4	D03	BG0IN*	D11	4
5	D04	BG0OUT*	D12	5

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Pin Number	ROWa Signal Mnemonic	ROWb Signal Mnemonic	ROWc Signal Mnemonic	Pin Number
6	D05	BG1IN*	D13	6
7	D06	BG1OUT*	D14	7
8	D07	BG2IN*	D15	8
9	GND	BG2OUT*	GND	9
10	SYSCLK	BG3IN*	SYSFAIL*	10
11	GND	BG3OUT*	BERR*	11
12	DS1*	BR0*	SYSRESET*	12
13	DS0*	BR1*	LWORD*	13
14	WRITE*	BR2*	AM5	14
15	GND	BR3*	A23	15
16	DTACK*	AM0	A22	16
17	GND*	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	SERCLK (1)	A17	21
22	IACKOUT*	SERDAT* (1)	A16	22
23	AM4	GND	A15	23
24	A07	IRQ7*	A14	24
25	A06	IRQ6*	A13	25
26	A05	IRQ5*	A12	26
27	A04	IRQ4*	A11	27
28	A03	IRQ3*	A10	28
29	A02	IRQ2*	A09	29
30	A01	IRQ1*	A08	30
31	-12 V	+5 V STDBY	+12 V	31
32	+5 V	+5 V	+5 V	32

Table 4. - VXI*bus* P2 Connector

Pin Number	ROWa Signal Mnemonic	ROWb Signal Mnemonic	ROWc Signal Mnemonic	Pin Number
1	ECLTRG0	+5 V	CLK10+	1
2	-2 V	GND	CLK10-	2
3	ECLTRIG1	RSV1	GND	3
4	GND	A24	-5.2 V	4
5	LBUSA00	A25	LBUSC00	5
6	LBUSA01	A26	LBUSC01	6
7	-5.2 V	A27	GND	7

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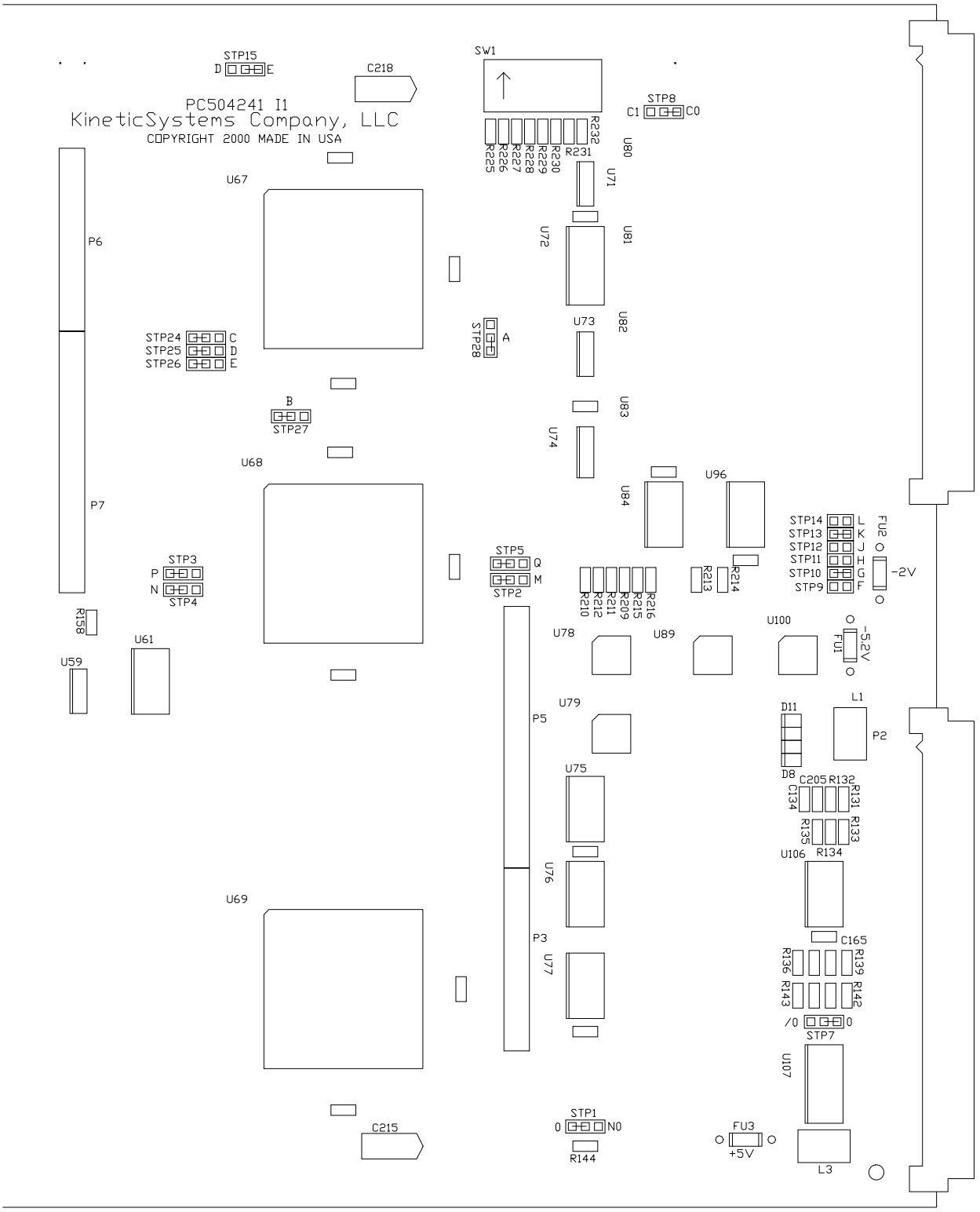
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Pin Number	ROWa Signal Mnemonic	ROWb Signal Mnemonic	ROWc Signal Mnemonic	Pin Number
8	LBUSA02	A28	LBUSC02	8
9	LBUSA03	A29	LBUSC03	9
10	GND	A30	GND	10
11	LBUSA04	A31	LBUSC04	11
12	LBUSA05	GND	LBUSC05	12
13	-5.2 V	+5 V	-2 V	13
14	LBUSA06	D16	LBUSC06	14
15	LBUSA07	D17	LBUSC07	15
16	GND	D18	GND	16
17	LBUSA08	D19	LBUSC08	17
18	LBUSA09	D20	LBUSC09	18
19	-5.2 V	D21	-5.2 V	19
20	LBUSA10	D22	LBUSC10	20
21	LBUSA11	D23	LBUSC11	21
22	GND	GND	GND	22
23	TTLTRG0*	D24	TTLTRG1*	23
24	TTLTRG2*	D25	TTLTRG3*	24
25	+5 V	D26	GND	25
26	TTLTRG4*	D27	TTLTRG5*	26
27	TTLTRG6*	D28	TTLTRG7*	27
28	GND	D29	GND	28
29	RSV2	D30	RSV3	29
30	MODID	D31	GND	30
31	GND	GND	+24 V	31
32	SUMBUS	+5 V	-24 V	32

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Model V120

Figure - 4 V120 Strapping View 1



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STRAPPING INFORMATION

The V120 is factory configured as shown in Figure 4.

Figure 4 shows the factory-configured positions for straps A-E and STP 1,8. The configuration is as follows:

1.) V120 is a Slot 0 device.
2.) V120 is an Interrupt Handler.
3.) Bus Request Level is set to 3.
4.) Backplane CLK 10 signal is an output on front panel Clk I/O.
5.) Positions 1 through 8 on SW1 are pushed down on top (set to zeros) so V120 is at Logical Address zero.

Figure 4 shows the factory configured strapping for the TTL Trigger Line and CLK 10 selections. This configuration allows the V120 to do the following.

1.) V120 drives backplane Clk10+/-.
2.) TTL Trigger Line 0 is routed to front panel Trig I/O as an output.
3.) V120 has pull-up enabled for Slot 0 MODID line.

Figure 4 shows the factory-configured positions for the SYSRESET and emulator straps. This configuration allows the V120 to drive the backplane SYSRESET signal.

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Table 5. - Strap Configuration

Label	Reference Designator	Function
A	STP28	* Arbiter Enable
B	STP27	* Interrupt Handler
C	STP24	* Slot 0
D	STP25	Bus Request Level
E	STP26	
F	STP9	* CLK10 +/-
G	STP10	
H	STP11	
J	STP12	
K	STP13	
L	STP14	
M	STP2	TTL Trigger Line
N	STP4	
P	STP3	
Q	STP5	TTL Trigger I/O
/0 0	STP7	* Slot 0 MODID Line Resistor
N0 0	STP1	V120 MODID Line
CI C0	STP8	CLK10 I/O
D E	STP15	* SYSRESET (System Reset Enable)

Strap Descriptions

V120 Strap Descriptions	
Arbiter Enable	Enables V120 to function as the bus arbiter deciding which requester is granted control of the data bus.
Interrupt Handler	Enables V120 to be an Interrupt Handler.
Slot 0	Enables the V120 to be a Slot 0 device.

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V120 Strap Descriptions	
Bus Request Level	Specifies the bus request level the V120 will use when requesting the data bus.
CLK10 +/-	Configures routing for CLK10 +/- to P2 connector.
TTL Trigger Line	Specifies the TTL trigger line to be used in conjunction with the front panel Trigger I/O.
TTL Trigger I/O	Determines the direction of the front panel Trigger I/O.
Slot 0 MODID	Enables pull-up resistor connected to V120 MODID line when used as a Slot 0 device.
V120 MODID Line	Used for testing purposes only. Should remain in the factory-configured position to connect the MODID line to the MODID resistor.
CLK 10 I/O	Configures front panel CLK10 signal as an input or an output.
SYSRESET	Allows an onboard reset signal to be routed to *SYSRESET signal on backplane.

VXIbus Slot 0 Configuration

The V120 is shipped from the factory configured for Slot 0 operation. If is to be installed in any other slot, is must be properly configured before installation.



Warning: If the V120 is configured for Slot 0 operation, installation in any other slot may result in damage to the V120, the Slot 0 device, and the VXIbus backplane.

A VXIbus Slot 0 device functions as the VMEbus System Controller. The System Controller is the VMEbus Arbiter for the data transfer bus. The controller also provides both the 16-MHz system clock (SYSCLK) and system reset (SYSRESET). The Slot 0 Device must also implement a MODID register to monitor and control the VXIbus MODID lines.

VXIbus Slot 0 Configuration

The V120 is shipped from the factory configured for Slot 0 operation. If is to be installed in any other slot, is must be properly configured before installation.



Warning: If the V120 is configured for Slot 0 operation, installation in any other slot may result in damage to the V120, the Slot 0 device, and the VXIbus backplane.

A VXIbus Slot 0 device functions as the VMEbus System Controller. The System Controller is the VMEbus Arbiter for the data transfer bus. The controller also provides both the 16-MHz system clock (SYSCLK) and system reset (SYSRESET). The Slot 0 Device must also implement a MODID register to monitor and control the VXIbus MODID lines.

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V120 Slot 0 Configuration

To configure the V120 for Slot 0 operation,

1. Strap A (STP28) in down position - V120 is bus arbiter.
2. Strap C (STP24) in left position - V120 is Slot 0 device.
3. Strap D E (STP15) in right position - V120 drives *SYSRESET.
4. Strap /0 0 (STP7) in right position - Enable Slot 0 MODID pull-up resistor.

To configure the V120 for Non-Slot 0 operation,

1. Strap A (STP28) in up position - V120 is not the bus arbiter.
2. Strap C (STP24) in right position - V120 is not a Slot 0 device.
3. Strap D E (STP15) in left position - V120 does not drive *SYSRESET.
4. Strap /0 0 (STP7) in left position - Disable Slot 0 MODID pull-up resistor.

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Bus Request Level

Straps D and E (STP25 and STP26, respectively) are used to specify the VMEbus Request Level the V120 uses. Table 8 shows how these straps determine the request level.

Table 6. - Bus Request Level Selections

Strap Position		Bus Request Level
Strap D (BR1)	Strap E (BR0)	
Left	Left	Request Level 3
Left	Right	Request Level 2
Right	Left	Request Level 1
Right	Right	Request Level 0

Interrupt Handler

The Interrupt Handler feature may be defeated by means of a strap on the V120. The default configuration is to have the Interrupt Handler enabled - Strap B in the left position. If the Interrupt Handler needs to be disabled, Strap B must be placed in the right position.

TTL Trigger I/0

The V120 can be configured to route the front panel Trigger I/O to a selected TTL Trigger line or take a selected TTL Trigger Line and route it to the front panel Trigger I/O. Straps M,N, and P are used to select a particular TTL Trigger Line. Strap Q is used to specify the direction of the TTL Trigger Line. When Strap Q is in the left position, the selected TTL Trigger Line is routed out to the front panel Trigger I/O signal. Conversely, the Strap Q in the right position allows the front panel Trigger I/O to source a trigger on the selected line. Table 7 shows how combinations of Straps M, N, and P select the TTL Trigger Line to be used. The left position of these straps is interpreted as a logical 0 and the right as a 1.

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Table 7. - I/O TTL Trigger Line Selections

STRAP POSITIONS			TTL TRIGGER LINE
M (TTL2)	P (TTL1)	N (TTL0)	
Left	Left	Left	7
Left	Left	Right	6
Left	Right	Left	5
Left	Right	Right	4
Right	Left	Left	3
Right	Left	Right	2
Right	Right	Left	1
Right	Right	Right	0

CLK10 Source

As the Slot 0 device, the V120 must supply the VXIbus defined differential ECL CLK10 source. This signal may originate from an onboard 10MHz source or from the front panel CLK10 I/O signal. Straps F through L are used to determine if the V120 supplies CLK10 and the if the source is from the onboard source or front panel CLK10 I/O signal. Only two shorting straps are supplied for strap locations F through L. When one of these straps is placed in location F, G, or H, the other strap must be in position J, K, or L, respectively. Table 10 defines the only valid combinations that may be used to configure straps F through L. If the front panel CLK10 I/O signal is used as the source, the CI-CO strap must be in the CI (left) position. If the front panel signal is not used as the CLK10 source, the CI-CO strap may be placed in the CO (right) position. This configuration allows the VXIbus CLK10 signal to appear as an output on the V120's front panel CLK10 I/O signal, regardless of which slot the V120 is installed.

Table 8. - CLK10 Configurations

Straps Installed in	Function
F and J	V120 is source for VXIbus CLK10 from front panel CLK10 I/O signal.
G and K	V120 is source for VXIbus CLK10 from onboard 10Mhz source.
H and L	V120 is not the source for VXIbus CLK10.

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PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXI*bus* Configuration Registers, the V120 implements those required for extended register-based devices. The V120 does not contain any registers located in A24 or A32 address space.

Access to the Configuration Registers for all VXI*bus* modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

A16 Base Address

The bit pattern for the A16 base address is shown below:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A 15	A 14	A 13	A 12	A 11	A 10	A 09	A 08	A 07	A 06	A 05	A 04	A 03	A 02	A 01	
1	1	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1	0	0	0	0	0	0

Bits 15 through 1 correspond to the VME address lines A15-A01.

Bits 15 and 14 are set to one (VXI defined).

Bits 13 through 6 are user selectable via the Logical Address switches and the ID/Logical Address register.

Bits 5 through zero are set to zero to indicate a block of 64 bytes.

VXIbus Configuration Registers

Configuration Registers are required by the VXI*bus* specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V120 are offset from the base address. **Note: the V120 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the VMEbus cycle.** Table 1 shows the applicable Configuration Registers present in the V120, their offset from the base (Logical) address, and their Read/Write capabilities.

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Table 9. - Configuration Registers Configuration (A16)Space

A16	Write/Read	Register Name
00_{16}	Write/Read	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Write/Read	Status/Control Register
06_{16}	N/A	Reserved
08_{16}	Write/Read *	Attribute / MODID Register *
$0A_{16}$	Read Only	Serial Number High Register
$0C_{16}$	Read Only	Serial Number Low Register
$0E_{16}$	Read Only	Version Number Register
10_{16} - 19_{16}	Read Only	Reserved Registers
$1A_{16}$	Read Only	Interrupt Status Register
$1C_{16}$	Write/Read	Interrupt Control Register
$1E_{16}$	Read Only	Subclass Register
20_{16}	Read Only	Suffix Register High
22_{16}	Read Only	Suffix Register Low
24_{16} - $3F_{16}$	N/A	Reserved

* If the V120 is configured as a Slot0 Controller, the register at offset 08_{16} is the write/read MODID register. For non-Slot0 configurations, the register at offset 08_{16} is the read-only Attribute register.

ID/Logical Address Register (Offset 00_{16})

The ID/Logical Address Register, which is located at offset 00_{16} from the logical base address, serves two functions, depending on the direction of the VME transfer. When executing a read operation to this register, the data returned indicates the Device Class, the Address Space requirements outside of A16 space, and the Manufacturer's Identification. A write operation to this register is only executed during a dynamic configuration sequence. During the configuration sequence, the Resource Manager assigns a logical address to the V120 by writing the logical address into the lower 8-bits of this register. The format and bit assignments for this ID/Logical Address register are shown in the following diagram. Since this register has write-only and read-only bits, two bit patterns are shown.

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	0	0	1	0	1	0	0	1

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Bit(s)	Mnemonic	Meaning
15,14	Device Class	This is an Extended Register Based device.
13,12	Address Space	The V120 does not require A24/A32 addressment space.
11-0	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

On Write transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used								LA 128	LA 64	LA 32	LA 16	LA 08	LA 04	LA 02	LA 01

For Write transfers to offset 00_{16} of the V120, bits 15 through 08 are not used. A write to these bits has no effect on the V120. In Dynamically Configured Systems (i.e., the Logical Address switches were set to a value of 255), bits 07 through 00 are written with the new Logical Address value. This write operation is typically executed by a Resource Manager.

Device Type Register (Offset 02_{16})

The Device Type Register is a read-only register located at an offset of 02_{16} from the logical base address. This register contains the Model Code of the V120. Since the V120 is an A16-only device, the entire 16 bits of this register are used for the Model Code.

Model Codes for VXI Slot 0 devices must be in the range of 00_{16} to FF_{16}. Model Codes for VXI non-Slot0 devices must be in the range of 100_{16} to $FFFF_{16}$. When the V120 is configured for non-Slot 0 functionality, the Model Code returned when reading this register is 160_{16}. To follow the VXI specification for Model Codes, the 100_{16} bit is set to zero when the V120 is configured for Slot 0 operation.

V120 Model Codes: 120_{16} for non-Slot 0 Operation
020_{16} for Slot 0 Operation

The following diagram shows the bit pattern of the Device Type Register for both Slot0 and non-Slot0 configurations.

For Slot0 configurations:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

For non-Slot0 configurations:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0

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Status/Control Register (Offset 04_{16})

The Status/Control Register, which is located at an offset of 04_{16} from the logical base address, contains write-only, read-only, and write/read bits. The following describes the bits for write and read operations.

This bit pattern shows the register layout for read accesses to the Status/Control Register.

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MODID*	1	1	1	1	1	1	1	1	1	1	Ready	Pass	SYSINB	Soft Reset

Bit(s)	Mnemonic	Meaning
15	Not Used	This bit is not used and should be written as a zero.
14	MODID*	This bit is set to a one if the module is not selected with the MODID line on the VXI P2 connector. A zero indicates that the device is selected by a high state on the P2 MODID line.
13-4	Not Used	These bits are not used and read as ones
3	Ready	READY is a read-only bit that is set to a one indicating successful completion of register initialization.
2	Pass	Pass is a read-only bit that is set to a one after the V120 has completed its power-on self-test without any errors. If errors occur, this bit is set to a zero and the SYSFAIL signal is asserted.
1	SYS INB	Reading this bit as a one indicates that the V120 may not drive the SYSFAIL* line.
0	Soft Reset	This write/read bit is used to reset the V120. Reading this bit as a one indicates that the V120 is currently in the RESET state. Setting this bit to a zero removes the V120 from the RESET state.

This bit pattern shows the register layout for write accesses to the Status/Control Register.

On Write transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used														SYSINB	Soft Reset

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Bit(s)	Mnemonic	Meaning
15-2	Not Used	These bits are not used for write operations.
1	SYS INB	SYSFAIL INHIBIT is a write-only bit that is set to a one to inhibit the V120 from asserting the VXI SYSFAIL* signal.
0	Soft Reset	This write/read bit used to reset the V120. Reading this bit as a one indicates that the V120 is currently in the RESET state. Setting this bit to a zero removes the V120 from the RESET state.

Attribute Register (Offset 08_{16})

The Attribute Register is located at an offset of 08_{16} from the logical base address. This register is only available when the V120 is configured as a non-Slot0 device. When the V120 is configured for Slot 0 operation, the Attribute Register is replaced with the MODID (Module Identification) Register. Refer to the MODID Register section of this manual for additional information.

The Attribute Register is a read-only register that contains information regarding the interrupt capabilities of the V120.

The format of the Attribute Register is shown in the following diagram.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	IR*	IH*	IS*

Bit(s)	Mnemonic	Meaning
15-3	Not Used	These bits are not used and read as ones.
2	IR*	The V120 has interrupter control capabilities and returns this bit set to zero.
1	IH*	The V120 has interrupt handling capabilities and returns this bit set to zero.
0	IS*	The V120 has interrupt status capabilities and returns this bit set to zero.

MODID Register (Offset 08_{16})

The MODID Register is located at an offset of 08_{16} from the logical base address. This register is only available when the V120 is configured as a Slot0 device. When the V120 is configured for non-Slot0 operation, the MODID Register is replaced with the Attribute Register. Refer to the Attribute Register section of this manual for additional information.

The MODID Register is a write/read register used to control the MODID geographic addressing lines on the VXI P2 connector. Each of the 13 slots in the VXI chassis have an individual line that can be asserted and monitored through the MODID Register. Before any MODID lines can be asserted by the V120, the Output Enable bit (bit 13) of the register must be set to a one. When the outputs are enabled, setting a MODID bit location to a one asserts the associated MODID signal.

The data read from the MODID bits in this register do not necessarily reflect the state of the bits that were written to this register. Instead, a read of this register returns the actual state of each MODID line.

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The following diagram shows the bit pattern for the MODID Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	MODID Enable	MID 12	MID 11	MID 10	MID 9	MID 8	MID 7	MID 6	MID 5	MID 4	MID 3	MID 2	MID 1	MID 0

Bit(s)	Mnemonic	Meaning
15,14	Not Used	These bits are not used and read as ones.
13	MODID Enable	OUTPUT ENABLE is a write/read bit used to enable or disable the V120 from driving the MODID signals. Setting this bit to a one enables the drivers and a zero disables them.
12-0	MID12-0	MODULE ID 12 through 0 are write/read bits used to assert and monitor the MODID signals. Writing a bit with a one will assert (as indicated by a high state) the corresponding slot's MODID line.

Serial Number High Register (Offset $0A_{16}$)

The Serial Number High Register, which is located at an offset of $0A_{16}$ from the logical base address, is used in combination with the Serial Number Low Register to define the serial number of the V120 module. These registers are read-only and a write operation to these registers have no effect.

The format of the Serial Number High Register is shown in the following diagram.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 31	SN 30	SN 29	SN 28	SN 27	SN 26	SN 25	SN 24	SN 23	SN 22	SN 21	SN 20	SN 19	SN 18	SN 17	SN 16

Bit(s)	Mnemonic	Meaning
15-0	SN31-16	SERIAL NUMBERS 31 through 16 are read-only bits that represent the upper 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN15-SN00 in the Serial Number Low register.

Serial Number Low Register (Offset $0C_{16}$)

The Serial Number Low Register, which is located at an offset of $0C_{16}$ from the logical base address, is used in combination with the Serial Number High Register to define the serial number of the V120 module. These registers are read-only and a write operation to these registers has no effect.

The format of the Serial Number Low Register is shown in the following diagram.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 9	SN 8	SN 7	SN 6	SN 5	SN 4	SN 3	SN 2	SN 1	SN 0

Bit(s)	**Mnemonic**	**Meaning**
15-0	SN15-0	SERIAL NUMBERS 15 through 0 are read-only bits that represent the upper 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN31-SN16 in the Serial Number Low register.

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Version Number Register (Offset $0E_{16}$)

The Version Number Register, which is located at an offset of $0E_{16}$ from the logical base address, is a read-only register that reflects the current revision level of the hardware and firmware residing on the V120. All write operations to this register are ignored.

The following shows the bit layout of the Version Number Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Firmware Version				Firmware Revision				Hardware Version				Hardware Revision			

Bit(s)	Mnemonic	Meaning
15-12	Firmware Version	These bits reflect the module's firmware main revision level.
11-8	Firmware Revision	These bits reflect the module's firmware revision number.
7-4	Hardware Version	These bits reflect the module's firmware main revision number.
3-0	Hardware Revision	These bits reflect the module's firmware revision number.

Interrupt Status Register (Offset $1A_{16}$)

The Interrupt Status Register is a 16-bit read-only register located at an offset of $1A_{16}$ from the logical base address. This register is enabled onto the VMEbus during interrupt acknowledge cycles. The register contains the logical address of the V120 in the lower-bits of the register and the upper 8-bits indicate the cause/status of the interrupt. The V120 itself cannot generate an interrupt. This register is shown here for completeness only.

The format of the Interrupt Status Register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1
Interrupt Cause/Status								Device Logical Address							

Bit(s)	Mnemonic	Meaning
15-8	Cause/Status	These bits are always returned as zeros.
7-0	LA128-LA1	These bits return the current logical address of the V120.

Interrupt Control Register (Offset $1C_{16}$)

The Interrupt Control Register, which is located at offset $1C_{16}$ from the logical base address, is a write/read register used to configure the V120 for interrupt generation. The Interrupt Request Level and

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Interrupt Enable bit are located in this register. The V120 version of the slot0 controller does not generate interrupts on VXI. Therefore, no interrupts should be enabled in this register.

The format and description of the bits in the Interrupt Control Register are shown in the following diagram.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used				FP TGB	FP TGA	ECL 1	ECL 0	TTL 7	TTL 6	TTL 5	TTL 4	TTL 3	TTL 2	TTL 1	TTL 0

Bit(s)	**Mnemonic**	**Meaning**
15-8	Not Used	These bits are not used and read as ones..
7	IREN*	INTERRUPT REQUEST ENABLE is a write/read bit used to enable/disable the generation of an interrupt by the V120. Setting this bit to a zero enables the V120 to interrupt and a one disables all interrupts.
6	Not Used	This bit is not used and read as a one.
5-3	IRQS3-IRQS1	INTERRUPT REQUEST SELECT 3 through 1 are write/read bits used to select the desired Interrupt Request Level that the V120 asserts when an interrupt is sourced. The following shows the Interrupt Request Level selections.
2-0	Not Used	These bits are not used and read as ones.

IRQS3	IRQS2	IRQS1	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	IRQ0

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Subclass Register (Offset $1E_{16}$)

The Subclass Register, which is located at an offset of $1E_{16}$ from the logical base address, is a read-only register that indicates the subclass of the V120. The V120 is an Extended Register Based Device as the following pattern indicates.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS PAS	RSV D	RSVD	DMD OFL	DMS CLR	DMD PND	DMD ENA	RSV D	INT DEN	RSV D	DLY ENA	BST ENA	RSV D	SYS FAL	RD SFL	SYS RST

Suffix High Register (Offset 20_{16})

The Suffix High register, which is located at an offset of 20_{16} from the logical base address, is a read-only register used in combination with the Suffix Low Register to determine the module model number suffix. The Suffix High Register contains the first two ASCII characters of the suffix and the Suffix Low Register contains the second two characters. The suffix shown is for the V120-A11 module.

The format and bit assignments for the Suffix High Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1

This read only register contains the first two ACSII characters of the module's suffix ("A" = 4141_{16}).

Suffix Low Register (Offset 22_{16})

The Suffix Low register, which is located at an offset of 22_{16} from the logical base address, is a read-only register used in combination with the Suffix High Register to determine the module model number suffix. The Suffix Low Register contains the last two ASCII characters of the suffix and the Suffix High Register contains the first two characters. The suffix shown is for the V120-A11 module.

The format and bit assignments for the Suffix Low Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1

This read only register contains the last two ACSII characters of the module's suffix ("11" = 3131_{31}).

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V120 Internal Register Description

All accesses to the V120 internal registers must be 32-bit accesses, even if the register is less than 32-bits in width. Table 10 shows the address allocations of the various internal registers on the V120.

Table 10. - Internal Registers

Address Location (Base 16)	Access Capabilities	Register Name
00	Write/Read	Control/Status Register (CSR)
04	Write Only	Burst Count Register (BCT)
08	Write Only	Delay Count Register (DCT)
0C	Read Only	Total Transfer Count Register (TTCR)
10	N/U	Reserved
14	Read Only	Demand FIFO Register (DFR)
18	Write Only	Interrupt Handler Mask Register (IHMSK)
1C	N/U	Reserved
20	Write Only	Trigger Source Register (TSR)
24	Write Only	Broadcast Trigger Mask (BTMSK)
28-2C	N/U	Reserved

Control/Status Register (CSR) (00_{16})

The Control/Status Register (CSR) is located at address 00_{16}. This write/read register is used to control and monitor various operations within the V120.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS PAS	RSV D	RSVD	DMD OFL	DMS CLR	DMD PND	DMD ENA	RSV D	INT DEN	RSV D	DLY ENA	BST ENA	RSV D	SYS FAL	RD SFL	SYS RST

Bit(s)	Mnemonic	Meaning
15	STS PAS	The Self-Test Passed is a read-only bit is set to a one when the self-
14:13	RSVD	These bits are reserved and must be set to 0.
12	DMD OFL	Demand Overflow is a read-only bit that is set to a one when the

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Bit(s)	Mnemonic	Meaning
		Demand FIFO is full and a subsequent demand is received. This bit is cleared on power-up and by a write to the CSR with the DMD CLR (Demand Clear) bit set to a one.
11	DMD CLR	Demand Clear is a write-only bit that is used to clear the contents of the Demand FIFO and to clear the Demand Overflow (DMD OFL) bit once it is set.
10	DMD PND	Demand Pending is a read-only bit that is set to a one as long as a demand is stored in the Demand FIFO. This bit is cleared as long as no demands are present, after power-up, and after a write to the CSR with the DMD CLR bit set to a one.
9	DMD ENA	Demand Enable is a write/read bit which is used to enable/disable the generation of highway demand messages when the Demand FIFO contains data.
8	RSVD	This bit is reserved and must be set to 0.
7	INTDEN	Interrupt Demand Enable is a write/read bit used to enable or disable the storage of a demand entry in the Demand FIFO when a VXI interrupt occurs. Setting this bit to a one enables the demand and a zero disables it.
6	RSVD	This bit is reserved and must be set to 0.
5	DLY ENA	Delay Enable is a write/read bit used to enable/disable the programmable delay associated with the receipt of broadcast trigger messages. Setting this bit to a zero disables the delay and a one enables it.
4	BST ENA	Burst Enable is a write/read bit used to enable/disable burst mode transfers on the VXI bus. Setting this bit to a one enables a DMA burst transfer of up to 256 transfers without relinquishing control of the VXI bus. Setting this bit to a zero disables this feature.
3	RSVD	This bit is reserved and must be set to 0.
2	SYS FAL	SYSFAIL is a write/read bit used to control the VXI bus SYSFAIL signal. Setting this bit to a one asserts the signal, and unasserted when the bit is set to zero.
1	RD SFL	Read SYSFAIL is a read-only bit that reflects the current state of the VXI bus SYSFAIL signal.
0	SYS RST	System Reset is a write-only bit, which is used to source the VXI bus SYSRESET signal. Setting this bit to a one asserts the SYSRESET signal. This bit is not latched.

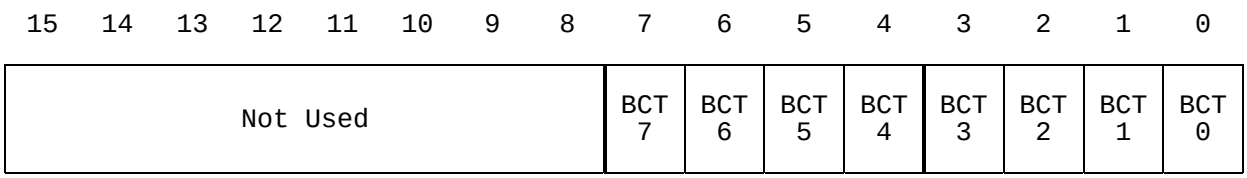
Burst Count Register (BCT) (04_{16})

The Burst Count Register (BCT) is a write-only register located at address 04_{16}. This register is used to specify the maximum number of transfers the V120 may execute on the VXI bus without relinquishing control of the VXI bus. This specification allows for up to 256 transfers without re-negotiation. To enable burst transfers, the BST ENA bit in the Control/Status Register must be set to a one prior to DMA operations.

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The following diagram shows the bit pattern for the Burst Count Register.



Bit(s)	Mnemonic	Meaning
15-8	Not Used	These bits are not used.
7-0	BCT7-0	Burst Count 7 through 0 specifies the number of DMA transfers the V120 may execute before relinquishing control of the VXIbus during a DMA operation.

Delay Count Register (DCT) (08_{16})

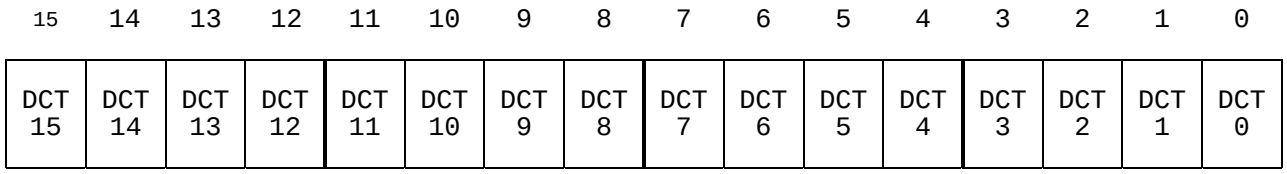
The Delay Count Register is a write-only register located at address 08_{16} within the V120. This register is used to specify a delay count associated with the receipt of a Broadcast Trigger command from the Interconnect Highway. Once the trigger command is received from the highway, the delay counter starts counting down until it underflows. When the count is exhausted, the content of the Broadcast Trigger Register is used to source the corresponding signals. The delay count is enabled with the DLY ENA bit in the Control/Status Register. If the delay is not enabled in the CSR, the contents of the Broadcast Trigger Register are used immediately to source the corresponding signals.

The delay count specification is the number of 200 nanoseconds intervals to wait before sourcing the broadcast trigger data. This allows for a delay specification in the range of 200 nanoseconds to 13.1 milliseconds in 200 nanosecond increments.

There is a minimum delay time within the V120 before the broadcast trigger data is sourced. This time is 500 nanoseconds. Therefore, to calculate the time from receipt of the Broadcast Trigger message until the actual broadcast, data source is as follows:

Time = (500 nanoseconds) + (Delay Count X 200 nanoseconds)

The following diagram shows the bit pattern for the Delay Count Register.



Bit(s)	Mnemonic	Meaning
15-0	DCT15-0	Delay Count 15 through 0 specify the amount of time to wait after receiving a Broadcast Trigger message until the Broadcast Trigger Mask Register data is sourced. This specification is the number of 200 nanosecond increments.

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Total Transfer Count Register (TTCR) ($0C_{16}$)

The Total Transfer Count Register is a read-only register located at address $0C_{16}$ within the V120. This register is used to verify the number of valid transfers that have occurred during a requested operation. If an error occurs during a requested operation, this register may then be read to determine the actual number of valid transfers before the error occurred. This value is the two's complement of number of words remaining to be transferred. This may then be subtracted from the original value to determine the valid transfer count.

The TTCR is originally loaded with the transfer count value that is received from the command message. As DMA transfers occur, this counter is incremented and DMA operations continue until the TTCR is exhausted.

The following diagram shows the bit pattern for the Total Transfer Count Register (TTCR).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCR 31	TCR 30	TCR 29	TCR 28	TCR 27	TCR 26	TCR 25	TCT 24	TCR 23	TCR 22	TCR 21	TDR 20	TCR 19	TCR 18	TCR 17	TCR 16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCR 15	TCR 14	TCR 13	TCR 12	TCR 11	TCR 10	TCR 9	TCR 8	TCR 7	TCR 6	TCR 5	TCR 4	TCR 3	TCR 2	TCR 1	TCR 0

Bit(s)	Mnemonic	Meaning
31-0	TCR31-0	Total Transfer Count 31 through 0 specify the total number of transfers remaining to be performed by the V120. This data is in two's complement format.

Demand FIFO Register (DFR) (14_{16})

The Demand FIFO Register is a read-only register located at address 14_{16} in the V120. This register is a FIFO capable of "holding" 2048 demand entries. These entries are generated by VXI interrupts. If the INT DEN bit in the Control/Status Register (CSR) is enabled, each interrupt event on the VXI bus is stored in the Demand FIFO.

Demand entries are stored in the FIFO until they are either read by the host computer or sent out onto the Interconnect Highway as Demand messages. If the DMD ENA bit in the CSR is set to zero the V120 does not generate any demand messages, but continues to store demand events as they occur.

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As long as there is at least one demand stored in the Demand FIFO, the DMD PND bit in the CSR is set to a one. If the Demand FIFO contains 2048 and one additional demand occurs, the data is not stored and the DMD OFL bit in the CSR is set. The Demand Overflow bits (DMD OFL) is not reset when the FIFO becomes less than full. A write operation to the CSR with the DMD CLR bit set to a one clears the FIFO and the overflow condition.

When a demand source is entered from an interrupt source, the data that is written into the FIFO is the actual interrupt request level. For example, data = 1 corresponds to interrupt request level 1; data = 6 corresponds to interrupt request level 6. Data from 1 to 7 represents demand sources generated from VXI interrupts.

The following diagram shows the bit pattern for the Demand FIFO Register.



Bit(s)	Mnemonic	Meaning
15-4	Not Used	These bits are not used.
3-0	DSC3-0	Demand Source 3 through 0 reflect the source of the demand. The following chart shows the valid demand sources and the corresponding data values

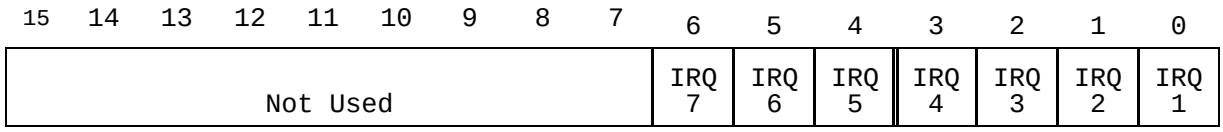
DSC 3	DSC 2	DSC 1	DSC 0	Demand Source
0	0	0	0	Reserved
0	0	0	1	Interrupt Request Level 1
0	0	1	0	Interrupt Request Level 2
0	0	1	1	Interrupt Request Level 3
0	1	0	0	Interrupt Request Level 4
0	1	0	1	Interrupt Request Level 5
0	1	1	0	Interrupt Request Level 6
0	1	1	1	Interrupt Request Level 7
1	0	0	0	Reserved

Interrupt Handler Mask Register (IHMSK) (18_{16})

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The Interrupt Handler Mask Register is a write-only register located at internal address 18_{16}. This register is used to indivi interrupt request lines will be monitored by the V120.



Bit(s)	Mnemonic	Meaning
6-0	IRQ7-1	The IRQ7 through IRQ1 bits are set to A1 to select which interrupt request lines IRQ7 through IRQ1 will be monitored for interrupt handling by the V120.

Interrupt Handler Mask Register (IHMSK) (18_{16})

The Interrupt Handler Mask Register is a write-only register located at internal address 18_{16}. This register i interrupt request lines will be monitored by the V120.

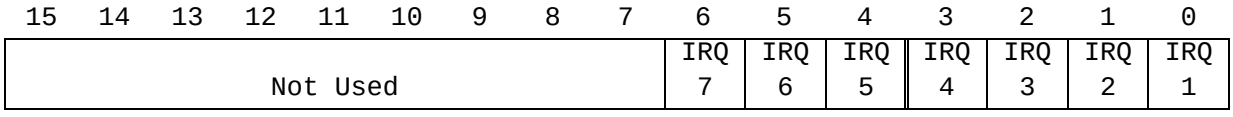
Bit(s)	Mnemonic	Meaning
6-0	IRQ7-1	The IRQ7 through IRQ1 bits are set to A1 to select which interrupt request lines IRQ7 through IRQ1 will be monitored for interrupt handling by the V120.

Trigger Source Register (TSRC) (20_{16})

The Trigger Source Register is a write-only register located at internal address 20_{16}.
This register is used to source any of the following signals:

1.) VXI TTL Trigger lines 0 through 7.
2.) VXI ECL Trigger lines 0 and 1.
3.) Front Panel Trigger Out B and A.

A 200 nanosecond pulse is applied to each signal when its corresponding bit in the Trigger Source Register is written to a one. The following diagram shows the bit pattern for the Trigger Source Register.



Bit(s)	Mnemonic	Meaning
15-12	Not Used	These bits are not used.

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Bit(s)	Mnemonic	Meaning
11	FP TGB	Front Panel Trigger Out B is set to a one to source the front panel trigger out B.
10	FP TGA	Front Panel Trigger Out A is set to a one to source the front panel trigger out A.
9-8	ECL1-0	The ECL1 and ECL0 bits are set to a one to source a trigger on the VXI trigger lines ECL1 and ECL0.
7-0	TTL7-0	The TTL7 through TTL0 bits are set to a 1 to assert the VXI trigger lines TTL7 through TTL0.

Broadcast Trigger Mask Register (BTMSK) (24_{16})

The Broadcast Trigger Mask Register is a write-only register that is located at internal address 24_{16} on the V120. This register is used to specify the signal to be sourced when a Broadcast Trigger message is received by the V120.

A Grand Interconnect host may issue a Broadcast Trigger message that informs all chassis connected to the highway to assert the data contained in the Broadcast Trigger Mask Register. On the V120, this data contains VXI TTL/ECL triggers and the two front panel triggers.

Associated with the Broadcast Trigger mechanism is the Delay Timer. The Delay Timer, if enabled, causes the V120 to delay the assertion of the Broadcast Trigger Mask Register until a predetermined interval of time elapses. The delay data is loaded in the Delay Count Register.

The following diagram shows the bit pattern for the Broadcast Trigger Mask Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used				FP TGB	FP TGA	ECL 1	ECL 0	TTL 7	TTL 6	TTL 5	TTL 4	TTL 3	TTL 2	TTL 1	TTL 0

Bit(s)	Mnemonic	Meaning
15-12	Not Used	These bits are not used.
11	FP TGB	Front Panel Trigger Out B is set to a one to source the front panel trigger out B.
10	FP TGA	Front Panel Trigger Out A is set to a one to source the front panel trigger out A.
9-8	ECL1-0	The ECL1 and ECL0 bits are set to a one to source a trigger on the VXI trigger lines ECL1 and ECL0.
7-0	TTL7-0	The TTL7 through TTL0 bits are set to a 1 to assert the VXI trigger lines TTL7 through TTL0.

Demand Messages

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The purpose of Demand Messages is to have a mechanism to inform the host of certain conditions.

The V120 can generate demand messages originating from a VME interrupt. Refer to the description of the Demand FIFO Register (DFR) and the Control Status Register (CSR) for further information.

Demands may be handled in two ways. One method of managing demands is by simply polling the Demand Pending (DMD PND) bit in the Control Status Register and reading the Demand FIFO. The second is to enable a pending demand to generate a highway message. When handled this way, it is not necessary to constantly read the Control Status register to determine if further action should be taken. The V120 can also insert these demand messages in the data stream. This allows demands to be seen at the host during large block transfers.

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APPENDIX

ID/Logical Address Register (Offset 00_{16})

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	0	0	1	0	1	0	0	1

On Write transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used								LA 128	LA 64	LA 32	LA 16	LA 08	LA 04	LA 02	LA 01

Device Type Register (Offset 02_{16})

For Slot0 configurations:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

For non-Slot0 configurations:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0

Status/Control Register (Offset 04_{16})

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MOD ID *	1	1	1	1	1	1	1	1	1	1	Ready	Pass	SYS INB	Soft Reset

On Write transactions:

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used														SYS INB	Soft Reset

Attribute Register (Offset 08_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	IR*	IH*	IS*

MODID Register (Offset 08_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	MODID Enable	MID 12	MID 11	MID 10	MID 9	MID 8	MID 7	MID 6	MID 5	MID 4	MID 3	MID 2	MID 1	MID 0

Serial Number High Register (Offset $0A_{16}$)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 31	SN 30	SN 29	SN 28	SN 27	SN 26	SN 25	SN 24	SN 23	SN 22	SN 21	SN 20	SN 19	SN 18	SN 17	SN 16

Serial Number Low Register (Offset $0C_{16}$)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 9	SN 8	SN 7	SN 6	SN 5	SN 4	SN 3	SN 2	SN 1	SN 0

Version Number Register (Offset $0E_{16}$)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Firmware Version	Firmware Revision	Hardware Version	Hardware Revision

Interrupt Status Register (Offset $1A_{16}$)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	IR EN*	1	IRQ S3	IRQ S2	IRQ S1	1	1	1

Subclass Register (Offset $1E_{16}$)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS PAS	RSV D	RSVD	DMD OFL	DMS CLR	DMD PND	DMD ENA	RSV D	INT DEN	RSV D	DLY ENA	BST ENA	RSV D	SYS FAL	RD SFL	SYS RST

Suffix High Register (Offset 20_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1

Suffix Low Register (Offset 22_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1

Control/Status Register (CSR) (00_{16})

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STS PAS	RSV D	RSVD	DMD OFL	DMS CLR	DMD PND	DMD ENA	RSV D	INT DEN	RSV D	DLY ENA	BST ENA	RSV D	SYS FAL	RD SFL	SYS RST

Burst Count Register (BCT) (04_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used								BCT 7	BCT 6	BCT 5	BCT 4	BCT 3	BCT 2	BCT 1	BCT 0

Delay Count Register (DCT) (08_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCT 15	DCT 14	DCT 13	DCT 12	DCT 11	DCT 10	DCT 9	DCT 8	DCT 7	DCT 6	DCT 5	DCT 4	DCT 3	DCT 2	DCT 1	DCT 0

Total Transfer Count Register (TTCR) ($0C_{16}$)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCR 31	TCR 30	TCR 29	TCR 28	TCR 27	TCR 26	TCR 25	TCT 24	TCR 23	TCR 22	TCR 21	TDR 20	TCR 19	TCR 18	TCR 17	TCR 16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCR 15	TCR 14	TCR 13	TCR 12	TCR 11	TCR 10	TCR 9	TCR 8	TCR 7	TCR 6	TCR 5	TCR 4	TCR 3	TCR 2	TCR 1	TCR 0

Demand FIFO Register (DFR) (14_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Not Used	DSC 3	DSC 2	DSC 1	DSC 0

Interrupt Handler Mask Register (IHMSK) (18_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used									IRQ 7	IRQ 6	IRQ 5	IRQ 4	IRQ 3	IRQ 2	IRQ 1

Trigger Source Register (TSRC) (20_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used				FP TGB	FP TGA	ECL 1	ECL 0	TTL 7	TTL 6	TTL 5	TTL 4	TTL 3	TTL 2	TTL 1	TTL 0

Broadcast Trigger Mask Register (BTMSK) (24_{16})

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used				FP TGB	FP TGA	ECL 1	ECL 0	TTL 7	TTL 6	TTL 5	TTL 4	TTL 3	TTL 2	TTL 1	TTL 0

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