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Model V387-ZA11

128-Channel, Discrete I/O

Instruction Manual

July, 2003

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128 -channel Discrete Input/Output

V387

GENERAL DESCRIPTION

The V387 is a single-width, C-size VXIbus module that contains up to 128 channels of discrete input and/or output. The module is configurable on a 32-channel basis through four interchangeable mezzanine cards, which are available in an assortment of I/O options.

Three different mezzanine card types can be used. For bidirectional transfers, a non-isolated TTL version is available. Five isolated voltage options (TTL, 12VDC, 24VDC, 48VDC, and 120VAC), configured for either input or output signaling, are also available. Input isolation is achieved by using LED/photo-transistor optical isolators. Each option has 16 circuits with identical input voltage ratings, and the switching threshold is approximately ½ the rated input voltage. Each circuit draws more than five, but less than 15 milliamperes. The logic convention is such that a contact closure (voltage present) is interpreted as a logical “1”. Each input is conditioned by filtering after the optical isolator. The filter time constant is programmable from 4 microseconds to over a second in 64 steps.

Output-only cards are available, with output circuits composed of reed relays, optical isolators, isolated ac switches, or single-pole, double-throw (Form "C") contacts. Each output card is a 16-channel circuit.

Input/output data is controlled in a 16-bit basis. Double buffering of I/O data allows the module to simultaneously sample or update all inputs or outputs, respectively. These actions are programmable for each card an may be initiated by selecting either a trigger line or one of four external sources. The module may be used with or without external handshake circuitry. The logical sense of the external handshake signals is programmable for each mezzanine card. The logical sense of each I/O word can also be set under program control. Pattern recognition capabilities are programmable in 16-bit increments. A pre-written data pattern, and a corresponding "enable" mask, are compared with the incoming data on a continuing basis. A change-of-state indicator is also updated on a continuing basis. Either function (pattern recognition or change-of-state) can be used to generate a VXIbus trigger or an interrupt. The selection of interrupt level and/or trigger line is made under program control.

An extensive Self-test is automatically performed on power-up. It can also be initiated by software. Module functionality as well as the I/O capability of each data byte is tested. A Pass/Fail status as well as problem source are indicated.

The V387 supports both static and dynamic configuration capabilities. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A32/A16, D16/D32 data transfers.

FEATURES

- **128 channel I/O capability in 32-channel increments**
- **Double buffered I/O data**
- **Pluggable mezzanine cards with various I/O options**
- **Trigger generation or interrupt on pattern recognition or change-of-state detection**
- **Programmable contact bounce suppression on inputs**
- **Variety of I/O strobe or handshake options**
- **Register-based**
- **Self-test capability**

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SPECIFICATIONS

Number of Channels	128 (maximum)
Bidirectional I/O	
Number of channels per circuit	32 TTL level signals
I/O lines overvoltage protected and TTL pull-ups provided	
Input current draw	greater than five, less than 10 milliamperes
Input switching threshold	
"0" Level	1.5 volts maximum
"1" Level	3.5 volts minimum
Output switching threshold	
"0" Level	0.7 volts maximum
"1" Level	2.0 volts minimum
Low-level output current	-24 milliamperes, maximum
High-level output current	10 milliamperes, maximum
Input-Only Circuits	
Number of channels per circuit	16 two-wire, floating inputs
Input signal options	5, 12, 24, or 48 volts DC; 120 volts AC; Contact closure (See ORDERING INFORMATION)
Input isolation	500 volts
Input current draw	greater than five, less than 15 milliamperes
Switching threshold	approximately ½ rated input
Input filter time constant	programmable from 4 microseconds to 480 seconds in 64 steps
Output-Only Circuits	
Number of channels per circuit	16
Reed Relay option	
Maximum open-circuit voltage	100 volts DC
Maximum current	0.5 amperes
Maximum switched load	10 volt-amperes
Life expectancy	5×10^6 operations (with proper contact protection)
Contact Resistance	200 mΩ, minimum
Operate time	330 microseconds, maximum
Release time	150 microseconds, typical
Insulation resistance	100 MΩ, minimum
Output polarity	Either
Contact bounce	3 milliseconds
Optical Isolator option	
Maximum open-circuit voltage	30 volts
Maximum ON current	10 milliamperes
ON voltage drop	1 volt
OFF current	Less than one microampere
Output polarity	Collector positive, with respect to Emitter
AC Switch option	
Zero voltage turn-on	10 volts, peak
Maximum open-circuit voltage	250 VRMS (400 VPeak)
Maximum ON current	1 ampere, 47 to 70 hertz
Minimum ON current	0.01 amperes
ON voltage drop	1.6 VRMS, maximum (at rated current)
Turn-on time (60 Hertz)	8.3 milliseconds, maximum
Turn-off time (60 Hertz)	8.4 milliseconds, maximum
Form "C" Relay option	
Maximum open-circuit voltage	500 VDC/130 VAC
Maximum current	1 ampere, switched or carry
Maximum switched load	50 volt-amperes
Life expectancy	5×10^9 operations (with proper contact protection)
Contact Resistance	100 mΩ, max; stable to within ±10% over life
Operate time	2.3 milliseconds, typical
Release time	1.5 milliseconds, maximum
Breakdown voltage	500 volts peak

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Insulation resistance	100 MΩ, minimum

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Connector Type	** TBD **
Mating Connector	KineticSystems Model ** TBD **
Power Requirements	
+5 volts	** TBD **
+24 volts	** TBD **
Environmental and Mechanical	
Temperature Range	
Operational	0 to +50°C
Storage	-25°C to +75°C
Relative Humidity	0 to 85%, non-condensing to 40°C
Cooling Requirements	10 cubic feet per minute
Dimensions	340mm X 233.35mm X 30.48mm (C-sized VXIbus)
Front Panel Potential	Chassis Ground

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ORDERING INFORMATION

Model V387-ZA11	128-Channel Discrete Input / Output Base Board
Model P300-300A	16-Channel Isolated Input Mezzanine Card 5VDC
Model P300-301A	16-Channel Isolated Input Mezzanine Card 12VDC
Model P300-302A	16-Channel Isolated Input Mezzanine Card 24VDC
Model P300-303A	16-Channel Isolated Input Mezzanine Card 48VDC
Model P300-304A	16-Channel Isolated Input Mezzanine Card 120VAC
Model P300-341A	16-Channel Isolated Output Mezzanine Card
Model P300-342A	16-Channel Reed Relay Output Mezzanine Card
Model P300-343A	16-Channel Form "C" Relay Output Mezzanine Card
Model P300-344A	16-Channel AC Switch Mezzanine Card
Model P300-380A	32-Channel TTL Input / Output Mezzanine Card
Model P500-387A	Local Bus Data / Frame Source Mezzanine Card
Model P501-387A	Local Bus Data Sink Mezzanine Card

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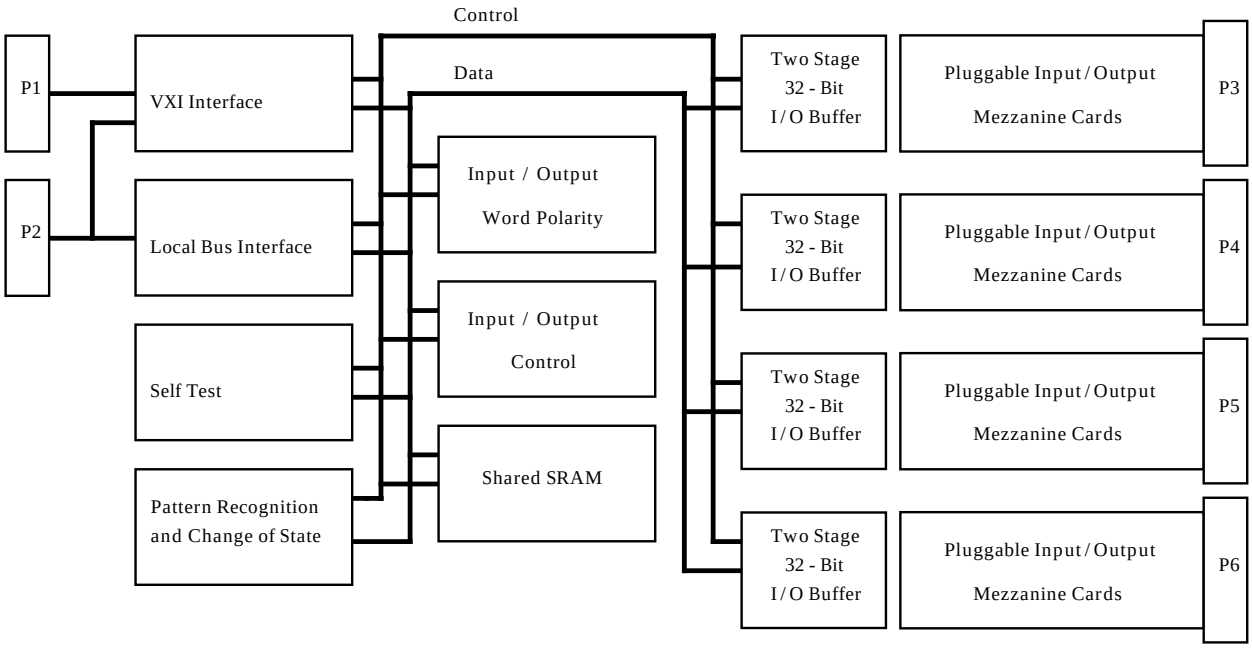


FIGURE 1 - V387 BLOCK DIAGRAM

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Getting Started

This manual is organized into four sections:

- The *Introduction* section describes the capabilities of the V387.
- The *Unpacking and Installation* section explains how to install the V387 into a VXI chassis.
- The *Programming Information* section explains how to access and control the V387. The first half of the section explains the use of the Configuration Registers. These general purpose registers are standard registers defined by VXI which are used to identify the module and control interrupts. The second half of the section explains the use of the Operational Registers. The registers are specific for operation and control of the V387. These registers are used to control pattern matching, TTL trigger lines, I/O data, etc.
- The *Appendix* provides additional information about specific I/O mezzanine cards.

The following is a list of some of the terms used throughout this manual:

A16 Space: As described in the VXI specification, this mnemonic is used to describe the first 64 kilobytes of address space. Every VXI module is automatically allocated a 64 byte block of this address space (also known as Configuration Registers). The exact location is determined by the logical address of the module.

A32 Space: As described in the VXI specification, this mnemonic is used to describe the 4 Gigabyte block of address space provided. Any module can request a block of this address space from information contained in its Configuration Registers. This memory block is also called the Operational Registers.

Configuration Registers: See A16 Space.

D16: As described in the VXI specification, this mnemonic is used to describe a single 16-bit data transfer.

D32: As described in the VXI specification, this mnemonic is used to describe a single 32-bit data transfer. This mode is not supported by all Slot-0 controllers. Check the owners manual for the Slot-0 before attempting this type of transfer.

I/O Word: This term is used to designate which of the eight 16-bit input/output words is being referenced. I/O Word numbers range from 0 to 7 and represent channels 1 to 128 in 16-channel groups. See Table 7.

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Logical Address: Every VXI module is given a unique logical address. There are a total of 256 logical addresses with 0 reserved for the Slot-0 controller.

Operational Registers: See A32 Space.

Rank 1 Buffer: First level of double-buffered input circuit (or last stage of output circuit).

Rank 2 Buffer: Second level of double-buffered input circuit (or first stage of output circuit).

Resource Manager: Also referred to as Resman. This software is made available by the manufacturer of the Slot-0 controller and is used to set logical addresses and Operational Registers of all the modules in the system.

Sample Clock: Clock signifying the start of a data frame for use in Local Bus transfers. The sample clock is generated by the Local Bus Master.

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Model V387-ZA11

INTRODUCTION

The V387 module is a versatile, user configurable Input / Output device that contains up to 128 channels of discrete I / O. The V387 is configured through the use of modular, interchangeable mezzanine cards. There are four slots on the V387, each capable of handling 32 channels of discrete I / O. There are three types of I / O cards available: isolated input, output, and bidirectional. The logical convention is such that a contact closure or voltage present is interpreted as a logical "1". An additional socket is provided for an optional Digi-bus™ input or output interface.

There are two kinds of non-isolated cards for bidirectional transfers, a 32-channel single-ended TTL version, and a 16-channel differential version (RS-422 signal levels).

There are seven isolated input versions, 5Vdc, 12Vdc, 16Vdc, 24Vdc, 28Vdc, 48Vdc, and 120Vac. Each isolated input card has 16 channels. Switching threshold is approximately one-half the rated voltage. Each input has filtering for contact bounce suppression. The filter time constant is programmable from 5µs to 1s in 64 steps.

There are four 16-channel output cards. The output circuit are composed of reed relays, optical isolators, isolated AC switches, or SPDT (Form "C") contacts.

I / O data is double buffered, allowing the module to simultaneously sample or update all inputs or outputs, respectively. The device can be triggered from an external source, from the V387 itself, or from the VXI*bus*. The logical sense of the I / O data is user selectable. Pattern recognition compares incoming data to a pre-written data pattern and data mask on a continuous basis. A change-of-state indicator is also updated on a continuous basis. Either function can be used to generate a VXI*bus* trigger or an interrupt.

The V387 is a single-width, C-size, register-based, VXI*bus* module which takes advantage of many of the features of the VXI standard. The VXI C-size specification, while it uses the same bus specification as VME, provides some significant system level enhancements. These include the definition of 8 TTL and 2 ECL trigger lines, a 10MHz ECL clock for system timing, module ID line for geographic addressing and module identification, an analog summing bus, and a 12-line daisy-chained Local Bus. These portions of the VXI standard provide a solid basis for a comprehensive systems level approach.

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VXI Trigger Lines

Eight of the pins on the P2 connector of the VXI*bus* are defined as TTL trigger lines. These open collector lines provide a wired-OR function that is suited to their use in communicating event information between modules.

A practical concept in using these lines is that of event sources and event sinks. Any one of several modules may generate an event on a specific trigger line, and one or more modules may be programmed to respond to this event, including the module which is the source of the event.

Examples of V387 event sources are change of state detection, pattern match detection, and front-panel external trigger inputs. Examples of event sinks are transient capture triggers to initiate the capture and local storage of a data segment, and sample clocks to synchronize sampling of input signals or the output of DAC or digital data.

System Configuration Validation

One of the issues, particularly in larger systems, is ensuring that the proper modules with the proper options are installed and configured in the system. This is especially important when the current system configuration cannot be validated because of system size or physical access to areas in a distributed system. Verifying proper installation can be particularly frustrating when modules of the same type or model number can be configured with a number of internal options. Unfortunately, this is an increasingly common practice because of the high densities that can be achieved today and the relatively large card size of VXI. A related issue is the capability to identify and trace the history of specific modules within a larger system.

The VXI standard requires (or in some cases, suggests) that certain register conventions be followed. These register conventions partially address these issues. Standardized registers include the manufacturer ID assigned by the VXI Consortium, a device-type or model identifier, a serial number, and a version number or revision number for hardware and firmware.

An extension of this concept provides a module option identifier as well as some amount of user-writeable EEPROM. The EEPROM provides the capability to record in nonvolatile memory any option, calibration, or other module-specific information that may be important to system operation and/or maintenance. Since these registers are accessible by software, it is possible to develop software to verify system configuration at startup, as well as track modules for maintenance purposes.

Private Digital Path, Digi-bus

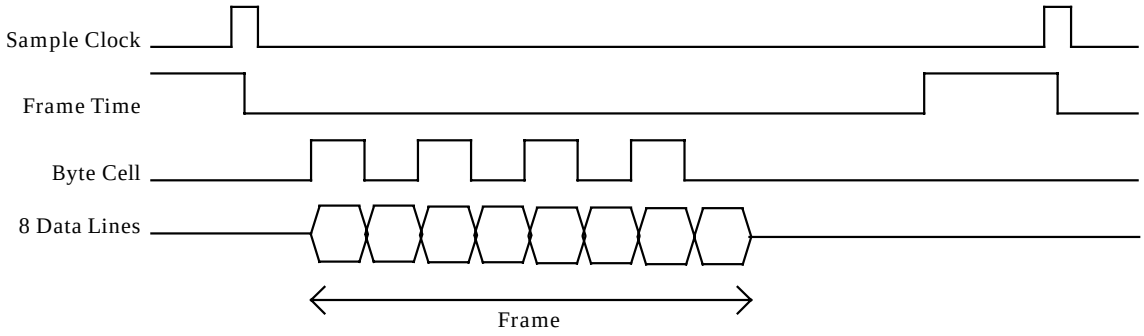
The VXI Local Bus provides 12 user-defined lines that are daisy-chained to adjacent modules. For digital signals, these lines provide a simple way to implement private data paths between system components that follow natural data flow, such as between an ADC and a digital signal processor

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(DSP) and / or a large block of memory. In many applications, there is a requirement to perform FFTs, digital filtering, and signal averaging. Other applications include a need to store huge amounts of data.

The VXI Local Bus provides a convenient mechanism to implement a private digital bus (Digi-bus) for moving synchronous data between modular elements of the system. By using a private synchronous bus as opposed to the main VXI backplane bus, issues regarding bus contention and latency are avoided.

The Digi-bus is propagated from slot to slot by appropriate modules. Transfers of "frames" of data are synchronous with the clock line used to drive the Digital-In modules. The right-most "source" module is designated as the master. The master provides the time base for a frame of data as well as control and termination for the bus. One fixed length frame of data is generated for each tick of the designated clock. Frame length is determined at configuration time by software consistent with the source module capabilities and configuration. The clock "tick" serves as the beginning of a new frame. In a multi-source configuration each source module is configured by software to generate a selected number of data items per clock tick at a selected location in the frame. Each data source has pre-assigned locations within a frame to place data, and data sinks can extract data from known locations within a frame. In effect, each module is assigned a "time slot" for transferring its data. The Digi-bus supports multiple data sources as well as multiple data sinks. The left-most sink also terminates the bus.



Since a particular sink module may only require selected data from a frame or, in some cases, only every Nth sample, a data selection scheme must be provided. Digi-bus implements a simple bit map of the frame that selects data based on position within a frame.

The Digi-bus supports transfer rates up to 10 Mbytes / second (10MHz) with bus timing controlled by the designated bus master. The right-most (source) module serves as bus master and provides all necessary timing and control as well as termination. The left-most (sink) module also provides bus termination. Data flow is generally from right to left. The VXI Slot-0 controller is defined by the standard to be in the left-most slot. Since the Slot-0 is either a computer in its own right (smart controller) or connected to a computer, the possibility of passing digital Local Bus data directly to the

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Slot-0 should not be precluded. In fact, Digi-bus options are available for KineticSystems Slot-0, the V160.

The unit of data on the Digi-bus is the 16-bit word. Data sources with more than 16-bit resolution are handled by a double word. When transferring data in the double word format, the first word is the least significant 16-bits followed by the most significant 16-bits.

V387 Data Register Organization

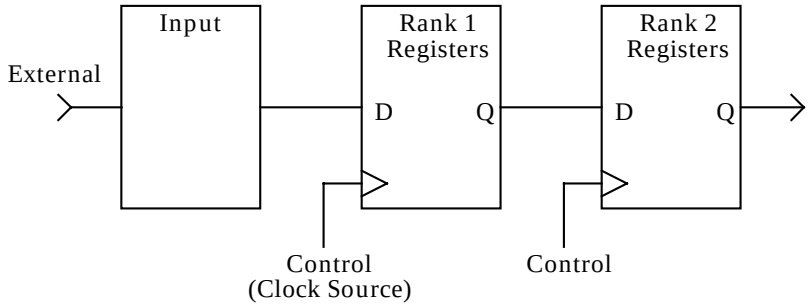
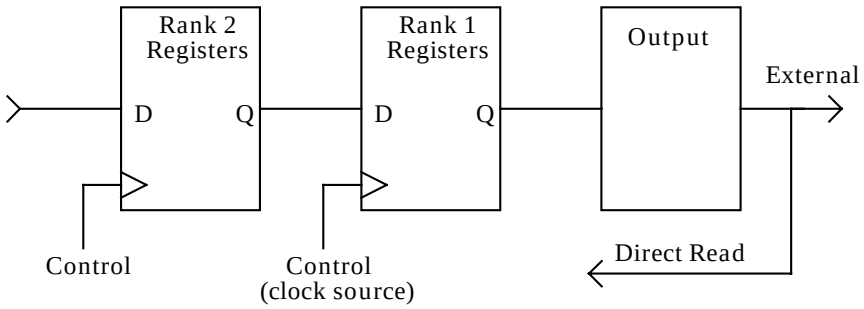


Figure 2. Input Data Register Diagram

There are three data registers on the V387. Consider the input circuit shown in figure 2. The Rank 1 and Rank 2 data registers act to double buffer the I/O, while the Direct Input Read register reads the input or output directly. Reading the Direct Input Read Register passes the present state of the inputs through Ranks 1 and 2, overwriting both registers. Rank 1 can store either the state of the inputs from the last read of the Direct Input Read Register, or the state of the inputs when last clocked by the selected clock source for the I/O card being used. Reading Rank 1 data overwrites Rank 2 data. Rank 2 stores the last data read, either from the Rank 1 Register or the Direct Input Read Register.

The register arrangement for an output-configured circuit is shown in figure 3. Reading the Direct Input Read Register for an output circuit yields the present state of the outputs, and does not affect the data stored in the Rank 1 and Rank 2 output registers. Writing data to Rank 2 stores the data in Rank 2. When strobed by the clock selected by the Clock Source Register, the data in Rank 2 then moves into the Rank 1 register. Writing to Rank 1 immediately overwrites the Rank 2 and Rank 1 registers and updates the outputs.



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Figure 3. Output Data Register Diagram

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Handshaking Organization

The Handshake Registers control the handshaking protocol for the bi-directional TTL card and the differential TTL card, allowing the V387 to communicate with external peripheral devices. These cards support three handshake signals not implemented on input- or output-only cards, the signals DATA STROBE OUT, ACKNOWLEDGE IN, and ERROR IN. Handshaking can be enabled or disabled through register control. With handshaking enabled, the DATA STROBE OUT line is asserted at the beginning of an I/O transfer. For the transfer to occur, the ACKNOWLEDGE IN line must be asserted by the external device. The ERROR IN line may also be asserted instead of the ACKNOWLEDGE IN line and the transfer will be aborted. Handshaking is used in both read and write cycles. With handshaking enabled for the card and no external ACKNOWLEDGE IN or ERROR IN signal received, transfers to the card's I/O locations will be aborted when the controller times-out the bus cycle. The maximum time the external device has to respond with an acknowledge or error signal is determined by the maximum bus cycle time of the controller. With handshaking disabled, an internal auto-acknowledge signal is generated to complete the I/O transfer.

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UNPACKING AND INSTALLATION

At KineticSystems, static precautions are observed from production, test and packaging of the module. This includes using static-proof mats and wrist straps. Please observe these same precautions when unpacking and installing the module whenever possible.

The Model V387 is shipped in an anti-static bag within a Styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the options to conform to the operating environment.

Logical Address Switches

The V387 represents one of the 255 devices permitted in a VXI*bus* system (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the module is set for a Logical Address of 255 then the V387 will be dynamically configured by the Resource Manager. If the V387 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. It is therefore the user's responsibility to ensure that no two modules are set to the same address. The Logical Address is set by manipulating eight rocker switches located under the access hole in the module's right-side ground shield (Refer to Figure 4).

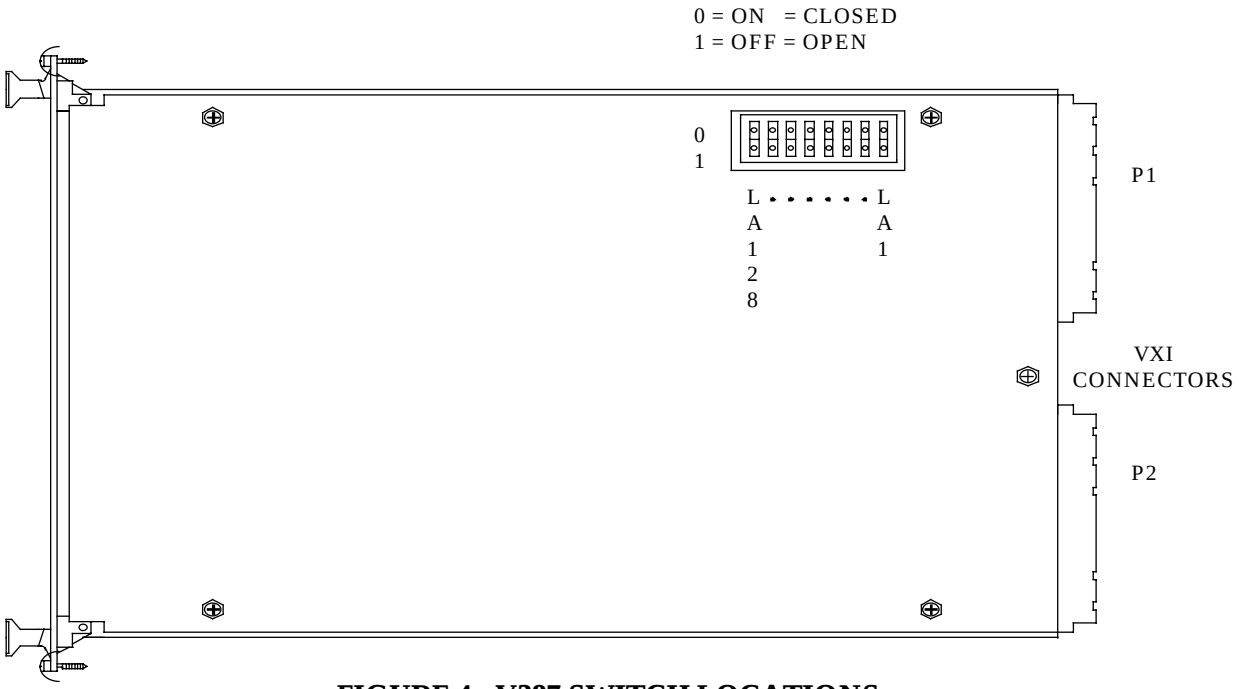


FIGURE 4 - V387 SWITCH LOCATIONS

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The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the A16 base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1	0	0	0	0	0	0

Bits 15 and 14 are set to one (VXI defined).
Bits 13 through 6 are user selectable via the address switches LA128-LA1.
Bits 5 through zero are set to "0" to indicate a block of 64 bytes.

For more information on switch settings, see "Programming Information"

Module Insertion

The V387 is a C-sized, single width VXI*bus* module. It requires 4.6 amps of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-sized VXI*bus* mainframe.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE OR USE AN AUTOCONFIGURING BACKPLANE

To insure proper interrupt acknowledge cycles from the V387 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V387 and the Slot 0 Controller.

Front Panel Information

LEDs

Add Rec — This LED turns on when V387's registers are being accessed (Address Received).

Failed — This LED turns on when the V387 has failed or is executing its self-test.

Connectors

The V387 has four fifty-position SCSI-II type pin connectors on the front panel. Each connector, P3-P6, corresponds to a mezzanine card, C3-C6, respectively. Refer to each optional cards' description for the correct pinout assignments.

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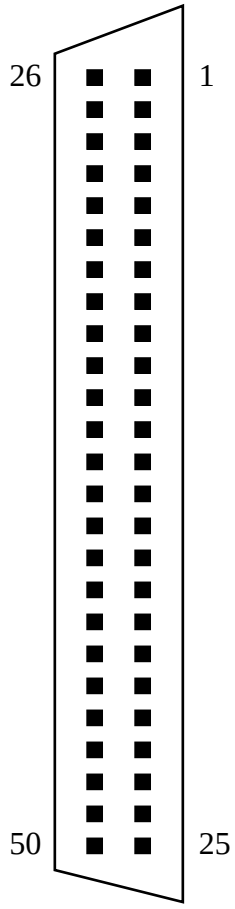


FIGURE 5 - 50-POSITION SCSI-II PLUG

The connector pictured above is an example of the connectors used on the V387. The connector is shown with the pinout and position as indicated if viewed from the front panel.

Strap Options

All straps on the V387 are for testing purposes only. They should remain in their factory configured position for proper operation.

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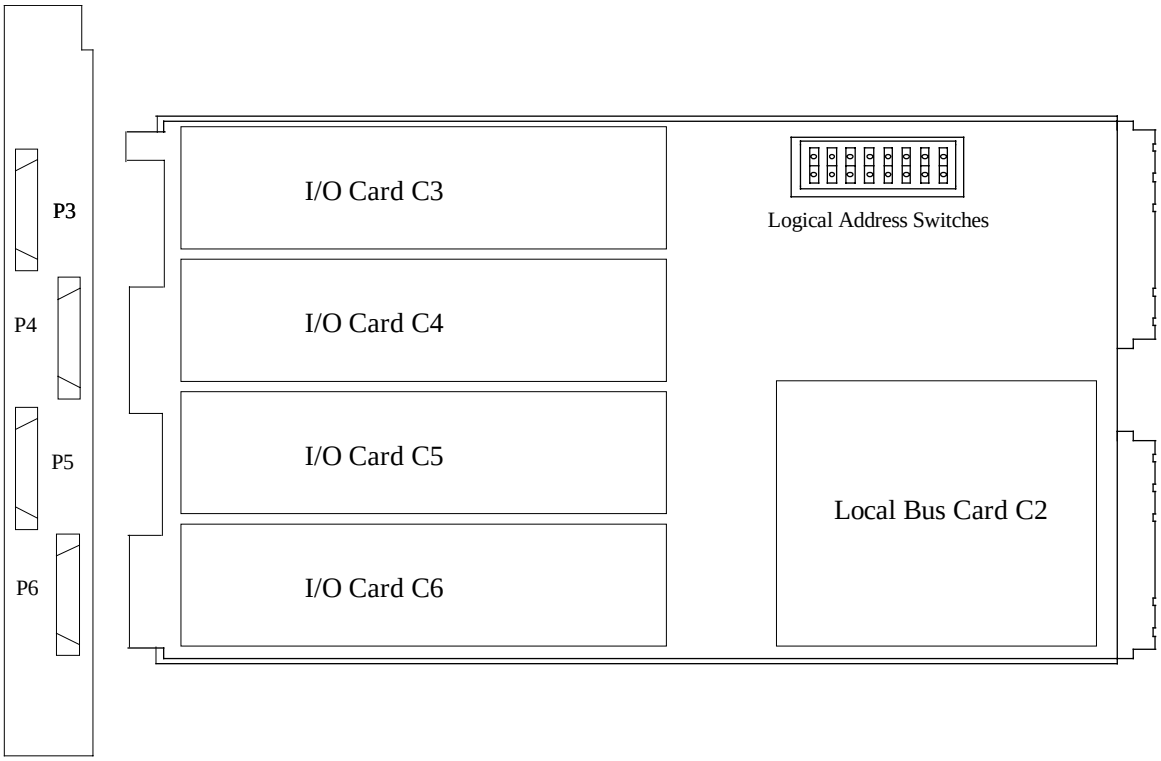


FIGURE 6 - V387 CARD OUTLINES

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Mezzanine Card Front Panel Pinouts
Table 1. Isolated Input Cards

P300-300 16-Channel Isolated Input (5VDC) Pinout
P300-301 16-Channel Isolated Input (12VDC) Pinout
P300-302 16-Channel Isolated Input (24VDC) Pinout
P300-303 16-Channel Isolated Input (48VDC) Pinout
P300-304 16-Channel Isolated Input (120VAC) Pinout

Pin Number	Function	Pin Number	Function
1	Channel 1 Signal	26	Channel 1 Return
2	Channel 2 Signal	27	Channel 2 Return
3	Channel 3 Signal	28	Channel 3 Return
4	Channel 4 Signal	29	Channel 4 Return
5	Channel 5 Signal	30	Channel 5 Return
6	Channel 6 Signal	31	Channel 6 Return
7	Channel 7 Signal	32	Channel 7 Return
8	Channel 8 Signal	33	Channel 8 Return
9	Channel 9 Signal	34	Channel 9 Return
10	Channel 10 Signal	35	Channel 10 Return
11	Channel 11 Signal	36	Channel 11 Return
12	Channel 12 Signal	37	Channel 12 Return
13	Channel 13 Signal	38	Channel 13 Return
14	Channel 14 Signal	39	Channel 14 Return
15	Channel 15 Signal	40	Channel 15 Return
16	Channel 16 Signal	41	Channel 16 Return
17	No Connection	42	No Connection
18	No Connection	43	No Connection
19	No Connection	44	No Connection
20	Data Strobe In	45	Data Strobe In Rtn
21	No Connection	46	No Connection
22	No Connection	47	No Connection
23	No Connection	48	No Connection
24	No Connection	49	No Connection
25	No Connection	50	No Connection

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Table 2. Isolated Output Cards

P300-341 16-Channel Isolated Output Pinout P300-342 16-Channel Reed Relay Output Pinout P300-344 16-Channel AC Switch Output Pinout			
Pin Number	Function	Pin Number	Function
1	Channel 1 Signal	26	Channel 1 Return
2	Channel 2 Signal	27	Channel 2 Return
3	Channel 3 Signal	28	Channel 3 Return
4	Channel 4 Signal	29	Channel 4 Return
5	Channel 5 Signal	30	Channel 5 Return
6	Channel 6 Signal	31	Channel 6 Return
7	Channel 7 Signal	32	Channel 7 Return
8	Channel 8 Signal	33	Channel 8 Return
9	Channel 9 Signal	34	Channel 9 Return
10	Channel 10 Signal	35	Channel 10 Return
11	Channel 11 Signal	36	Channel 11 Return
12	Channel 12 Signal	37	Channel 12 Return
13	Channel 13 Signal	38	Channel 13 Return
14	Channel 14 Signal	39	Channel 14 Return
15	Channel 15 Signal	40	Channel 15 Return
16	Channel 16 Signal	41	Channel 16 Return
17	No Connection	42	No Connection
18	No Connection	43	No Connection
19	No Connection	44	No Connection
20	No Connection	45	No Connection
21	No Connection	46	No Connection
22	No Connection	47	No Connection
23	No Connection	48	No Connection
24	No Connection	49	No Connection
25	No Connection	50	No Connection

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Table 3. Relay Output Card

P300-343 16-Channel Form "C" Relay Output Pinout			
Pin Number	Function	Pin Number	Function
1	Channel 1 Signal	26	Channel 1 N.C.
2	Channel 2 Signal	27	Channel 3 Signal
3	Channel 3 N.C.	28	Channel 4 Signal
4	Channel 5 Signal	29	Channel 5 N.C.
5	Channel 6 Signal	30	Channel 7 Signal
6	Channel 7 N.C.	31	Channel 8 Signal
7	Channel 9 Signal	32	Channel 9 N.C.
8	Channel 10 Signal	33	Channel 11 Signal
9	Channel 11 N.C.	34	Channel 12 Signal
10	Channel 13 Signal	35	Channel 13 N.C.
11	Channel 14 Signal	36	Channel 15 Signal
12	Channel 15 N.C.	37	Channel 16 Signal
13	No Connection	38	Channel 1 N.O.
14	Channel 2 N.C.	39	Channel 2 N.O.
15	Channel 3 N.0.	40	Channel 4 N.C.
16	Channel 4 N.O.	41	Channel 5 N.O.
17	Channel 6 N.C.	42	Channel 6 N.O.
18	Channel 7 N.O.	43	Channel 8 N.C.
19	Channel 8 N.O.	44	Channel 9 N.O.
20	Channel 10 N.C.	45	Channel 10 N.O.
21	Channel 11 N.O.	46	Channel 12 N.C.
22	Channel 12 N.O.	47	Channel 13 N.O.
23	Channel 14 N.C.	48	Channel 14 N.O.
24	Channel 15 N.O.	49	Channel 16 N.C.
25	Channel 16 N.O.	50	No Connection

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Table 4. Bi-directional TTL Card

P300-380 32-Channel Bi-directional TTL Card Pinout			
Pin Number	Function	Pin Number	Function
1	Data Bit 1	26	Data Bit 2
2	Data Bit 3	27	Data Bit 4
3	Data Bit 5	28	Data Bit 6
4	Data Bit 7	29	Data Bit 8
5	Data Bit 9	30	Data Bit 10
6	Data Bit 11	31	Data Bit 12
7	Data Bit 13	32	Data Bit 14
8	Data Bit 15	33	Data Bit 16
9	Data Bit 17	34	Data Bit 18
10	Data Bit 19	35	Data Bit 20
11	Data Bit 21	36	Data Bit 22
12	Data Bit 23	37	Data Bit 24
13	Data Bit 25	38	Data Bit 26
14	Data Bit 27	39	Data Bit 28
15	Data Bit 29	40	Data Bit 30
16	Data Bit 31	41	Data Bit 32
17	Acknowledge In	42	Error In
18	Data Strobe Out	43	Data Strobe In
19	Ground	44	Ground
20	Ground	45	Ground
21	Ground	46	Ground
22	Ground	47	Ground
23	Ground	48	Ground
24	Ground	49	Ground
25	Ground	50	Ground

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Table 5. Differential Card

P300-382A 16-Channel Differential I/O Card Pinout			
Pin Number	Function	Pin Number	Function
1	+ Data Bit 1	26	- Data Bit 1
2	+ Data Bit 2	27	- Data Bit 2
3	+ Data Bit 3	28	- Data Bit 3
4	+ Data Bit 4	29	- Data Bit 4
5	+ Data Bit 5	30	- Data Bit 5
6	+ Data Bit 6	31	- Data Bit 6
7	+ Data Bit 7	32	- Data Bit 7
8	+ Data Bit 8	33	- Data Bit 8
9	+ Data Bit 9	34	- Data Bit 9
10	+ Data Bit 10	35	- Data Bit 10
11	+ Data Bit 11	36	- Data Bit 11
12	+ Data Bit 12	37	- Data Bit 12
13	+ Data Bit 13	38	- Data Bit 13
14	+ Data Bit 14	39	- Data Bit 14
15	+ Data Bit 15	40	- Data Bit 15
16	+ Data Bit 16	41	- Data Bit 16
17	+ Acknowledge In	42	- Acknowledge In
18	+ Error In	43	- Error In
19	+ Data Strobe In	44	- Data Strobe In
20	+ Data Strobe Out	45	- Data Strobe Out
21	Ground	46	Ground
22	Ground	47	Ground
23	Ground	48	Ground
24	Ground	49	Ground
25	Ground	50	Ground

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PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

The V387 is classified according to the VXI specification as an extended register-based device, which means it has registers that occupy A16 and A32 space. The V387 contains Configuration Registers as required for VXI extended register based devices. The V387 also contains a set of Operational Registers to monitor and control the functional aspects of the device.

The Configuration Registers are located in A16 space and include the standard registers as well as additional general purpose registers. From these registers, information about the specific module can be read, the base address for the A32 registers can be controlled, and the interrupt level can be set. For example, by reading certain registers in A16 space, the following information about this module can be found just by knowing the module's logical address:

Manufacturer:	KineticSystems
Module Type:	V387
Base Card Option:	ZA11
Serial Number:	20
Firmware Version:	1.0
Hardware Version:	1.0

In general, any configuration register can be accessed by simply knowing the module's logical address (set by the logical address switches) and the register's offset. The configuration registers are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The logical address switch settings or the contents of the Logical Address Register (see below) are mapped into address lines A6 through A13, establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$. A complete list of the A16 registers and corresponding address offsets is available in the next section. The general formula for obtaining the A16 address of a register is:

$$A16_Address = C000_{16} + (Logical_Address \cdot 40_{16}) + Offset$$

VXIbus Configuration Registers

Configuration Registers are required by the VXI*bus* specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V387 are offset from the base address. **Note: the V387 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 6 shows the applicable Configuration Registers present in the V387, their offset from the base (Logical) address, and their Read / Write capabilities.

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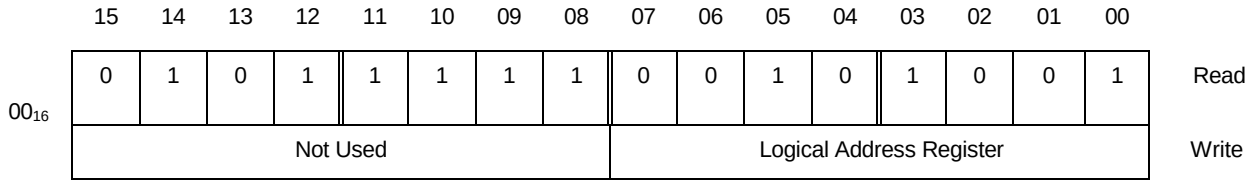
Table 6. Configuration Registers - A16 Space

A16 Offset	Read/Write Capability	Register Name
00_{16}	Mixed	ID / Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Mixed	Status / Control Register
06_{16}	Read / Write	Offset Register
08_{16}	Read Only	Attribute Register
$0A_{16}$	Read Only	Serial Number High Register
$0C_{16}$	Read Only	Serial Number Low Register
$0E_{16}$	Read Only	Version Number Register
10_{16} - 19_{16}	Read Only	Reserved Registers
$1A_{16}$	Read Only	Interrupt Status Register
$1C_{16}$	Mixed	Interrupt Control Register
$1E_{16}$	Read Only	Subclass Register
20_{16}	Read Only	Suffix Register High
22_{16}	Read Only	Suffix Register Low
24_{16} - $3F_{16}$	Read / Write	User Defined Registers

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ID/Logical Address Register

The format and bit assignments for the ID / Logical Address register are as follows:



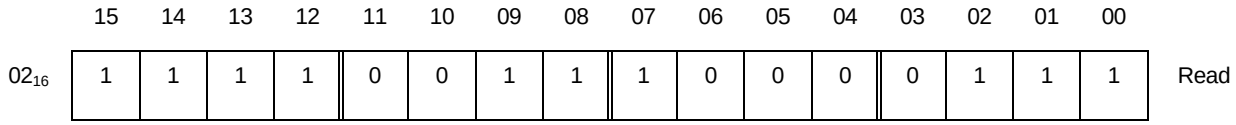
On READ transactions the module returns $5F29_{16}$:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is an Extended Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16 / A32 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits fifteen through eight are not used. A write to these bits has no effect on the V387. In Dynamically configured systems (i.e. the Logical Address switches set to a value of 255), bits seven through zero are written with the new Logical Address value obtained from the resource manager.

Device Type Register

The format and bit assignments for the Device Type register are as follows:



On READ transactions the module returns $F387_{16}$:

Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	The V387 requires 64k bytes of additional memory space. (This is the minimum number of bytes that may be requested in A32 space.)
11 - 0	Model Code	Identifies this device as Model V387 (387_{16}).

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Status/Control Register

The format and bit assignments for the Status / Control register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A32 ENA	MODID *	1	1	1	1	1	1	1	1	1	1	RDY	PASS	SYS INB	RST	Read
	A32 ENA	Not Used													SYS INB	RST	Write

Bit(s)	Mnemonic	Meaning
15	A32 Enable (A32 ENA)	This bit is written with a "1" to enable A32 addressing and reset (to "0") to disable A32 addressing. **This bit must be set to "1" to allow access to the module's Operational Registers**. Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*
14	MODID*	This read only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13 - 04	Not used.	These bits will return all "1s" when read. Ignored when written.
03	Ready (RDY)	A "1" indicates the successful completion of register initialization.
02	Passed	A "0" indicates that the V387 has failed or is executing its (PASS) self-test.
01	Sysfail Inb. (SYS INB)	Writing a "1" to this bit disables the device from driving the SYSFAIL* line. Reads of this bit indicate its current state.
00	Reset (RST)	Writing a "1" to this bit forces the device into the Soft Reset condition. While in the Soft Reset state, the module will only allow access to its Configuration Registers. Writing a "0" to this bit will then force the module to begin executing its Self Test. This bit must be cleared along with the Passed and Ready bits set before any access to the Operational Registers is allowed.

Offset Register

The format and bit assignments for the Offset register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	Read/ Write

After SYSRESET* and prior to self-test, all bits are set to "0". Otherwise a write defines the base address of the device's operational registers.

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Attribute Register

The format and bit assignments for the Attribute Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	Not Used / Read as ones													0	1	0	Read

On READ transactions the module returns $FFFA_{16}$

Bit(s)	Mnemonic	Meaning
15 - 03	Not used	A write to these bits has no effect. A read of these bits will return all "1s".
02	Intr Control	A zero indicates that the V387 has Interrupt Control capability.
01	Intr Handler	A one indicates that the V387 does not have Interrupt Handler capabilities.
00	Intr Status	A zero indicates that the V387 does have an Interrupt Status register.

Serial Number High Register

The format and bit assignments for the Serial Number High Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$0A_{16}$	SN31	SN30	SN29	SN28	SN27	SN26	SN25	SN24	SN23	SN22	SN21	SN20	SN19	SN18	SN17	SN16	Read

This read only register contains the upper code of the module's serial number.

Serial Number Low Register

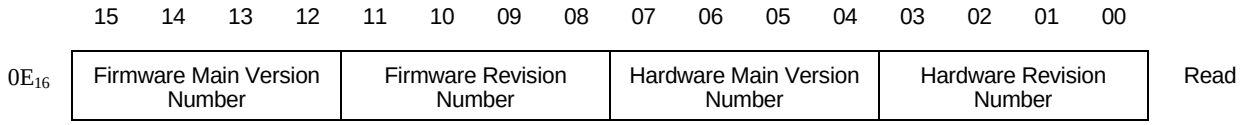
The format and bit assignments for the Serial Number Low Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$0C_{16}$	SN15	SN14	SN13	SN12	SN11	SN10	SN09	SN08	SN07	SN06	SN05	SN04	SN03	SN02	SN01	SN0	Read

This read only register contains the lower code of the module's serial number.

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Version Number Register
The format and bit assignments for the Version Number Register are as follows:

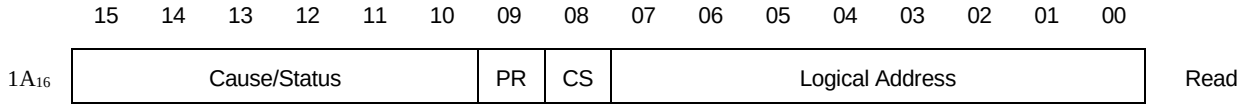


On READ transactions the module will return the revision level of its hardware and firmware:

Bit(s)	Mnemonic	Example
15 - 12	Firmware Main Version Number	1_{16}
11 - 08	Firmware Revision Number	0_{16}
07 - 04	Hardware Main Version Number	1_{16}
03 - 00	Hardware Revision Number	0_{16}

Address locations 10_{16} - 19_{16} are reserved

Interrupt Status Register
The format and bit assignments for the Interrupt Status Register are as follows:



A read of this register will clear the status bit(s) which generated the interrupt.

Bit(s)	Mnemonic	Meaning
15 - 08	Cause / Status	A “1” in bit eight (PR) indicates that a pattern recognition has occurred. A “1” in bit nine (CS) indicates that a change of state has occurred. All other bits should be read as “0s”
07 - 00	Logical Address	Logical address of the device.

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Interrupt Control Register

The format and bit assignments for the Interrupt Control Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1C_{16}$	1	1	1	1	1	1	IM1	IM0	IREN *	1	IRL2	IRL1	IRL0	1	1	1	Read
	Not Used						IM1	IM0	IREN *	Not Used	IRL2	IRL1	IRL0	Not Used			Write

Bit(s)	Mnemonic	Meaning
15 - 10	Not Used	Read back as “1s”.
09 - 08	Interrupt Mask Bits (IM1-IM0)	Read / Write bits where a “1” disables the interrupt associated with the corresponding bit.
	(IM1)	Masks a change of state interrupt.
	(IM0)	Masks a pattern recognition interrupt.
07	IR ENA* (IR EN *)	A “1” in this bit disables all interrupt generation.
06	Not Used	Read back as “1”.
05 - 03	Interrupter IRQ Line* (IRL2-IRL0)	These bits determine the interrupt priority level of interrupts generated by the V387 by selecting which interrupt request line to assert. 111 - disconnected 110 - IRQ1 ↓ 000 - IRQ7
02 - 00	Not Used	Read back as “1s”.

Interrupts generated by the V387 for Change of State and Pattern Recognition both use the interrupt IRQ line selected by IRL2-0.

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Subclass Register
The format and bit assignments for the Subclass Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	Read

On READ transactions the module returns $FFFE_{16}$:

Bit(s)	Meaning
15	VXIbus extended device
14 - 0	$7FFE_{16}$ - Extended Register Based Device

Suffix Register High
The format and bit assignments for the Suffix Register High are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
20_{16}	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1	Read

This read only register contains the upper code of the module's suffix (ZA = $5A41_{16}$).

Suffix Register Low
The format and bit assignments for the Suffix Register Low are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
22_{16}	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	Read

This read only register contains the upper code of the module's suffix (11 = 3131_{16}).

24_{16}-$3F_{16}$ User Defined Registers

These Read/Write registers are contained in non-volatile EEPROM and may be used to store user defined data. Allow 10 milliseconds for writes to these registers.

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Operational Registers

The operational registers are the channels through which the various functions of the V387 are controlled. These registers also hold the input and output data patterns. For compatibility with other KineticSystems VXI*bus* modules in this series, these registers are positioned in VMEbus Extended Address (A32) space. The base address for these registers is defined by the contents of the Offset register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A32 Enable bit (bit 15) must be set in the Status / Control Register (see Configuration Registers). **Note: The V387 will only respond to these addresses if the Extended Address Modifier Codes ($0F - 0D_{16}$ or $0B - 09_{16}$) are set for the bus cycles. These include the Extended Supervisory/Non-Privileged Block Transfer, Program Access, and Data Access Address Modifier codes.**

Of the 64k bytes requested by the setting of the Device Type Register in the Configuration Register set, only 552 bytes are used (64kbytes is the minimum number of bytes that may be requested through the Device Type register in A32 space). Table 8 shows the applicable Operational Registers present in the V387, their offset from the base A32 address, and their Read / Write capabilities.

The V387 supports both D16 (16-bit short word) and D32 (32-bit longword) transfers to its Operational Registers. The data for each I / O channel is represented in memory as shown below.

D16 transfer:

Short Word Data Bits	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Short Word Offset $X2_{16}$	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1
Short Word Offset $X0_{16}$	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17

D32 transfer:

Long Word Data Bits	D31	D30	D29	D28	D27	...	...	D04	D03	D02	D01	D00
Long Word Offset $X0_{16}$	CH 32	CH 31	CH 30	CH 29	CH 28	...	...	CH 5	CH 4	CH 3	CH 2	CH 1

Channel 1 data is accessed through the least significant bit of either a 16-bit short word transfer to offset $X2_{16}$ or a 32-bit long word transfer to $X0_{16}$. Similarly, Channel 16 data is the least significant bit during a 16-bit short word transfer to offset $X0_{16}$ or data bit 16 during a 32-bit longword transfer to $X0_{16}$. Table 7 illustrates the mapping of channels from memory to their respective mezzanine cards and out the front panel connector. The term I / O Word is used to designate which of the eight 16-bit input / output words is being referenced. This term will be used frequently to differentiate between the channel registers when defining the various control functions. Note that I / O Word 00 corresponds to channels 17-32, and I / O Word 01 corresponds to channels 01-16, etc.

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Model V387-ZA11

As shown in table 7, the channels are arranged in 16 channel groups, two per mezzanine card. If a mezzanine card only uses 16 channels, then the upper channels are not used by the V387. For example, with a 16-channel card in the first slot (C3) and a 16-channel card in the second slot (C4), channels 17-32 and 49-64 are not used. Reads and writes, in that case, should use I/O words 01 and 03 only.

To calculate the A32 address of a register, the A32 offset (as defined in the Offset Register in the Configuration Registers) is added to the Channel Offset along with the Operational Register offset.

A 31	A 30	A 29	...	A 18	A 17	A 16	A 15	A 14	A 13	A 12	A 11	A 10	A 09	A 08	A 07	A 06	A 05	A 04	A 03	A 02	A 01	A 00
Offset Register 15-0							Always zeros.							Operational Offset					Channel Offset			

For instance, the Offset Register contains 1000_{16} and the Mask Register for Channels 1-16 is to be written. The address for the desired register is 10000072_{16}. To write to the Mask Register for Channels 32-17, the address would be 10000070_{16}.

Table 7. Channel and I/O Word Definitions

Channel Number	Channel Offset	Front Panel Connector	Mezzanine Card	I/O Word
CH32-CH17	$X0_{16}$	P3	C3	00
CH16-CH01	$X2_{16}$	P3	C3	01
CH64-CH49	$X4_{16}$	P4	C4	02
CH48-CH33	$X6_{16}$	P4	C4	03
CH96-CH81	$X8_{16}$	P5	C5	04
CH80-CH65	XA_{16}	P5	C5	05
CH128-CH113	XC_{16}	P6	C6	06
CH112-CH96	XE_{16}	P6	C6	07

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Table 8. Operational Registers- Extended Address (A32) Space

A32 Offset	Read/Write Capability	Register Name
00_{16}	Read Only	Mezzanine Card ID Register
02_{16}	Read / Write	Strobe Disable Register
04_{16}	Read / Write	Debounce Configuration Register 1
06_{16}	Read / Write	Debounce Configuration Register 2
08_{16}	Read / Write	Bi-directional Configuration Register
$0A_{16}$	Read / Write	Pattern Recognition Enable Register
$0C_{16}$	Read / Write	Change of State Enable Register
$0E_{16}$	Read / Write	Trigger Line Selection Register
10_{16}	Read / Write	I / O Word Polarity Register
12_{16}	Read / Write	Handshake Polarity Register
14_{16}	Read / Write	Handshake Enable Register
16_{16}	Read / Write	Clock Source Register
18_{16}- $1A_{16}$	Read Only	Self-test Results Registers
$1C_{16}$- $1E_{16}$		Reserved
20_{16} - $2E_{16}$	Read / Write	Rank 1 I / O Data Registers
30_{16} - $3E_{16}$	Read / Write	Pattern Registers
40_{16} - $4E_{16}$	Read / Write	Change of State Results Registers
50_{16} - $5E_{16}$	Read Only	Direct Input Read Registers
60_{16} - $6E_{16}$	Read / Write	Rank 2 I / O Data Registers
70_{16} - $7E_{16}$	Read / Write	Mask Registers
80_{16} -$17E_{16}$†	Read / Write	Local Bus Sink Reception Bits Registers
100_{16}*	Read / Write	Local Bus Source Frame Control Register
102_{16}*	Read / Write	Local Bus Source Start Address
104_{16}*	Read / Write	Local Bus Source Word Select Low
106_{16}*	Read / Write	Local Bus Source Word Select High
$10A_{16}$*	Read / Write	Local Bus Source Enable Data / Frame Skip
$10C_{16}$-$18E_{16}$*		Reserved
180_{16}†	Write	Local Bus Sink Enable / Frame Skip

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A32 Offset	Read/Write Capability	Register Name
182_{16}†	Write	Local Bus Sink Word Select Low
184_{16}†	Write	Local Bus Sink Word Select High
$18E_{16}$- $FFFE_{16}$	Not Used	Reserved

* Implemented on P500-387 Local Bus Data Output option only.
† Implemented on P501-387 Local Bus Data Input option only.

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Mezzanine Card ID Register

The format and bit assignments for the Mezzanine Card ID Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Mezzanine Card 6 ID				Mezzanine Card 5 ID				Mezzanine Card 4 ID				Mezzanine Card 3 ID				Read

This register contains four 4-bit codes that identify each card as an input with debounce, presence of card, etc. and are defined as follows:

Card ID Bit Number	Meaning
03	A "1" indicates that the programmable debounce is supported on this card.
02	A "0" indicates that a card is installed in this slot.
01-00	These two bits define which type of card is installed:

Bit Pattern	Meaning
11	Input Only
10	Reserved
01	Output Only
00	Bi-directional

Strobe Disable Register

The format and bit assignments for the Strobe Disable Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	Not Used								SD 7	SD 6	SD 5	SD 4	SD 3	SD 2	SD 1	SD 0	Read/ Write

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
07 - 00	Strobe Disable	Setting these bits disables the movement of the corresponding data word in Rank 1 and Rank 2 I/O registers by disabling the clock source to the I/O registers. This prevents the external event (as specified in the Clock Source Register) from altering the data in the Rank 1 and Rank 2 I/O registers. With Strobe Disable set, reads to the Direct Input Read Registers will return the last value latched into the Rank 2 Registers. This register is cleared on any reset.

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On READ transactions bits fifteen through zero return the last value written.

Debounce Time Configuration Register 1

The format and bit assignments for the Debounce Time Configuration Register 1 are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	Not Used		C6 5	C6 4	C6 3	C6 2	C6 1	C6 0	Not Used		C5 5	C5 4	C5 3	C5 2	C5 1	C5 0	Read/ Write

This register contains the debounce suppression time constants for I/O cards five and six. The bit values for the constants are defined in table 9. Debounce suppression is not supported for output cards or the differential card. Reading the Mezzanine Card ID register will indicate if the I/O cards support debounce suppression. Writing to one of the Debounce Time Configuration Registers whose slot contains an output card or differential card will not affect the I/O.

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
13 - 08	Control (C6 5-0)	Control the debounce time for I/O card six (as defined in Table 4). These bits are cleared on any reset.
05 - 00	Control (C5 5-0)	Control the debounce time for I/O card five (as defined in Table 4). These bits are cleared on any reset.

On READ transactions bits fifteen through zero return the last value written.

Debounce Time Configuration Register 2

The format and bit assignments for the Debounce Time Configuration Register 2 are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	Not Used		C4 5	C4 4	C4 3	C4 2	C4 1	C4 0	Not Used		C3 5	C3 4	C3 3	C3 2	C3 1	C3 0	Read/ Write

Same as Debounce Time Configuration Register 1 except for I/O cards three and four.

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
13 - 08	Control (C4 5-0)	Control the debounce time for I/O card four (as defined in Table 4). These bits are cleared on any reset.
05 - 00	Control (C3 5-0)	Control the debounce time for I/O card three (as defined in Table 4). These bits are cleared on any reset.

On READ transactions bits fifteen through zero return the last value written.

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Table 9. Debounce Time Control

Set Control		Bit 3	0	0	0	0	1	1	1	1
		Bit 4	0	0	1	1	0	0	1	1
Bit 0	Bit 1	Bit 5 / Bit 2	0	1	0	1	0	1	0	1
0	0	0	5	50	500	5K	50k	500K	5M	50M
0	0	1	50	500	5k	50k	500k	5M	50M	500M
0	1	0	10	100	1k	10k	100k	1M	10M	100M
0	1	1	15	150	1.5k	15k	150k	1.5M	15M	150M
1	0	0	20	200	2k	20k	200k	2M	20M	200M
1	0	1	25	250	2.5k	25k	250k	2.5M	25M	250M
1	1	0	30	300	3k	30k	300k	3M	30M	300M
1	1	1	60	600	6k	60k	600k	6M	60M	600M

Note: The times given above are all in microseconds.

Bi-directional Configuration Register

The format and bit assignments for the Bi-directional Configuration Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	Mode	Not Used							I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Read/ Write

This register contains the data direction information for the mezzanine cards installed. For Bi-directional I/O cards, writing to this register controls the data direction in 16-channel groups. For input- or output-only cards, the register indicates the card type. The MODE bit enables or disables Auto-Update mode. In Auto-Update Mode with a bi-directional mezzanine card installed, writing to the card's I/O location automatically configures it as an output. Reading from that location automatically configures it as an input. The channels are configured as each operation is performed. On READ transactions bits fifteen through zero return the last value written.

Bit(s)	Mnemonic	Meaning
15	Mode bit (MODE)	When the Mode bit is set to "1" (disabling Auto-Update mode), bits seven through zero define the input/output status of the corresponding I/O Word for bi-directional I/O cards. When this bit is set low, Auto-Update mode is enabled. the MODE bit is set to "1" on reset.
07 - 00	I/O Bits	A "0" configures I/O Word as an output. A "1" configures the corresponding I/O Word (I/O7-I/O0) as an input. These bits are configured appropriately on any reset depending on the type of I/O card that is located in the corresponding slot. Bi-directional cards will be configured as outputs. Refer to Table 7 for I/O Word designations.

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Pattern Recognition Enable Register

The format and bit assignments for the Pattern Recognition Enable Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$0A_{16}$	GO	Not Used							PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	Read/ Write

This register is the main control of the pattern recognition function. It enables/disables pattern recognition on a 16-channel basis. To do pattern matching for less than 16 channels, set the Mask register accordingly. Related registers are the Trigger Line Selection Register, Interrupt Control Register (in the Configuration Registers), Pattern Registers, and Mask Registers

On WRITE transactions:

Bit(s)	Mnemonic:	Meaning:
15	GO bit (GO)	Writing a "1" starts the pattern recognition process. Setting this bit, along with at least one of the Pattern Enable bits, starts a mechanism which scans the Rank 2 input registers. These registers are compared with the corresponding Pattern register and bits are selectively masked (ignored) by bits in the corresponding Mask register. Once the Rank 2 data (with the Mask applied) matches the Pattern data, a given *TTL Trigger Line and/or an Interrupt Request may be asserted. At this point the GO bit must again be written with a "1" to restart the pattern recognition scan process.
07 - 00	Pattern Enable Bits (PE7-PE0)	"1" enables and "0" disables pattern recognition on the corresponding I/O word. A "0" written to a bit eliminates the need to specify a pattern or mask for that I/O Word. Refer to Table 7 for I/O Word channel assignments.

On READ transactions bits fifteen through zero return the last value written.

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Change of State Enable Register

The format and bit assignments for the Change of State Enable Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$0C_{16}$	GO	Not Used							CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0	Read/ Write

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
15	GO bit (GO)	A "1" starts change of state detection. Setting this bit, along with at least one of the Check Enable bits, starts a mechanism to compare the Rank 1 and Rank 2 input registers. In this situation, a last state value is held in the Rank 2 input register and the present state of the inputs is held in the Rank 1 input register. The registers are compared and any change of state is logged into the Change of State Results Registers. If any change of state is detected, a *TTL Trigger Line and/or Interrupt Request is asserted and detection is halted. Ranks 1 and 2 will contain the present state (changed) value. To restart the process, the GO bit must be re-written with a "1".
07 - 00	Check Enable (CE7-CE0)	A "1" enables and "0" disables Change of State check on the corresponding I/O Word. Writing a "0" allows an I/O location to be ignored when testing of a change of state. In this circumstance, the Change of State Results Register for this I/O Word will not be altered. Refer to Table 7 for I/O Word channel assignments.

On READ transactions bits fifteen through zero return the last value written.

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Trigger Line Selection Register

The format and bit assignments for the Trigger Line Selection Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
OE_{16}	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Read/ Write

The Trigger Line Selection Register allows the V387 to generate VXI trigger signals when a Pattern Recognition or Change of State event has occurred. Any combination of the eight TTL trigger lines may be selected. Those selected will all be asserted on the event, there is no correlation to I/O Word or channel number.

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
15 - 08	Pattern Trigger Bits (PT7-PT0)	"1" - enables trigger generation on the corresponding TTL-Trigger lines if a pattern recognition occurs. PT7 ⇒ TTL Trigger Line 7 PT0 ⇒ TTL Trigger Line 0
07 - 00	Change Trigger Bits (CT7-CT0)	"1" - enables trigger generation on the corresponding TTL-Trigger lines if a change of state occurs. CT7 ⇒ TTL Trigger Line 7 CT0 ⇒ TTL Trigger Line 0

Once a pattern recognition or change of state has occurred, a write to this register with any data pattern will de-assert all trigger lines.

On READ transactions bits fifteen through zero return the last value written.

Word Polarity Register

The format and bit assignments for the Word Polarity Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
10_{16}	Not Used								WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0	Read/ Write

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
07 - 00	Word Polarity (WP7-WP0)	Each bit determines the polarity of each I/O Word. A "1" inverts polarity of a byte during a transfer to or from an I/O location. All bits are set to "0" after any reset condition. In this mode, data written or read as a "1" is taken to be high-true or ON.

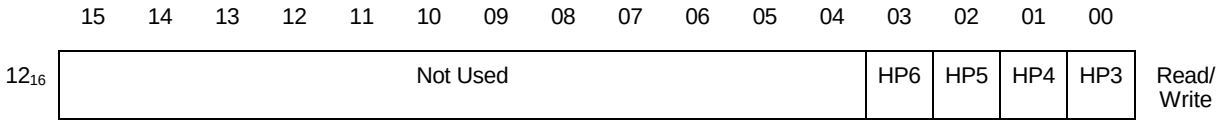
Note: When reading data written to the Rank 1 output register through the Direct Input Read Registers, the data pattern read back will be the same as what was written.

On READ transactions bits fifteen through zero return the last value written.

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Handshake Polarity Register

The format and bit assignments for the Handshake Polarity Register are as follows:



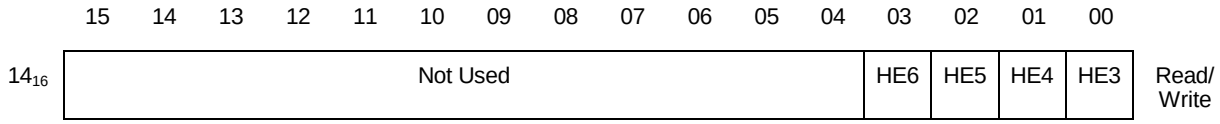
On WRITE transactions:

Bit(s)	Mnemonic	Meaning
03 - 00	Handshake Polarity (HP6-HP3)	Each bit determines the polarity of the handshake signals to the corresponding mezzanine card."0" indicates active low, "1" indicates active high. These bits are cleared after any reset. In this state, the polarity of all handshake signals is ON = low true = 0 volts and the acknowledge line(s) must be asserted low to complete the I/O transfer.

On READ transactions bits fifteen through zero return the last value written.

Handshake Enable Register

The format and bit assignments for the Handshake Enable Register are as follows:



On WRITE transactions:

Bit(s)	Mnemonic	Meaning
03 - 00	Handshake Enable (HE6-HE3)	A "1" enables a mechanism which requires an external acknowledge when the I/O location for the corresponding mezzanine card is accessed from VXI. A "0" in these locations disables this mechanism.

On READ transactions bits fifteen through zero return the last value written.

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Clock Source Register

The format and bit assignments for the Clock Source Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
16_{16}	Clock Source Card 6				Clock Source Card 5				Clock Source Card 4				Clock Source Card 3				Read/ Write

On WRITE transactions:

This register contains four 4-bit codes that specify the clock source for the corresponding mezzanine card. The codes are defined in the following table:

Strobe Source	Code Value(s)
*Internal : (for Pattern Matching and Change of State only)	0_{16}
*ECL Trigger Lines(2) *ECL Trigger Line 0 = 1_{16} *ECL Trigger Line 1 = 2_{16}	$1\text{-}2_{16}$
Local Bus Sample Clock	3_{16}
*External Strobe Source(4) *Data Strobe In from Card 3 = 4_{16} ↓ *Data Strobe In from Card 6 = 7_{16}	$4\text{-}7_{16}$
*TTL Trigger Lines(8) *TTL Trigger Line 0 = 8_{16} ↓ *TTL Trigger Line 7 = F_{16}	$8\text{-}F_{16}$

All clock sources are negative edge triggered with the exception of the Local Bus Sample Clock. The External Strobe Sources are available on Input and Bidirectional I/O cards only (as DATA STROBE IN). These external sources are routed from the appropriate front panel connector. The voltage level and isolation/protection of these external signals will match that of the input channels. External Strobe Sources must have a minimum pulse width of 50 nanoseconds and must not exceed the maximum analog bandwidth of that I/O card. (See the specifications for the various I/O cards). The internal clock source (*Internal) should be used during Pattern Recognition and Change of State Detection if no other source is available to signal when the inputs should be sampled.

On READ transactions bits fifteen through zero return the last value written.

Self-test Results Registers (18_{16}-$1A_{16}$)

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The format and bit assignments for the Self-test Results Registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
18_{16}	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	1	Read/ Write
$1A_{16}$	0	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	Read/ Write

These read / write registers return the results of the on-board diagnostic test which is executed during any Reset condition. Before normal operation can be expected, this register should contain 50415353_{16} (PASS - passed self-test ASCII). Otherwise, these registers will contain the following bit patterns:

Bit(s)	Meaning
15 - 08	8-bit code for self-test failure reason.
07 - 00	8-bit code for source of problem.

$1C_{16}$ - $1E_{16}$ Reserved

Rank 1 I/O Data Registers

The format and channel assignments for the Rank 1 I / O Data Registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
20_{16}	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	Read/ Write
22_{16}	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	Read/ Write
24_{16}	CH 64	CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56	CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	Read/ Write
26_{16}	CH 48	CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40	CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	Read/ Write
28_{16}	CH 96	CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88	CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	Read/ Write
$2A_{16}$	CH 80	CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72	CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	Read/ Write
$2C_{16}$	CH 128	CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120	CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	Read/ Write
$2E_{16}$	CH 112	CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104	CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	Read/ Write

The table above shows the relative position of each channel in memory. Channel 1 (Data Bit 00) is positioned as the least significant bit location of offset 22_{16}. These registers contain the I / O data that was clocked in (or out) by the source specified in the Clock Source Register. They may also contain input data from a Direct Input Read, or data written directly to this register. A read or write to these locations will overwrite the Rank 2 input or output registers, respectively.

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Pattern Registers

The format and channel assignments for the Pattern Registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
30_{16}	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	Read/ Write
32_{16}	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	Read/ Write
34_{16}	CH 64	CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56	CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	Read/ Write
36_{16}	CH 48	CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40	CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	Read/ Write
38_{16}	CH 96	CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88	CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	Read/ Write
$3A_{16}$	CH 80	CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72	CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	Read/ Write
$3C_{16}$	CH 128	CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120	CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	Read/ Write
$3E_{16}$	CH 112	CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104	CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	Read/ Write

These registers contain the pattern that is compared with its corresponding I/O bit during a pattern recognition operation. See Pattern Recognition Enable Register for more information.

Change of State Result Registers

The format and channel assignments for the Change of State Results registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
40_{16}	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	Read/ Write
42_{16}	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	Read/ Write
44_{16}	CH 64	CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56	CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	Read/ Write
46_{16}	CH 48	CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40	CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	Read/ Write
48_{16}	CH 96	CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88	CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	Read/ Write
$4A_{16}$	CH 80	CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72	CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	Read/ Write
$4C_{16}$	CH 128	CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120	CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	Read/ Write
$4E_{16}$	CH 112	CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104	CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	Read/ Write

This register contains change of state results when active. The values of these registers will not be updated if Change of State is not enabled for the corresponding I/O location. The Mask Register does not affect Change of State detection.

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Direct Input Read Registers

The format and channel assignments for the Direct Input Read registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
50_{16}	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	Read
52_{16}	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	Read
54_{16}	CH 64	CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56	CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	Read
56_{16}	CH 48	CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40	CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	Read
58_{16}	CH 96	CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88	CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	Read
$5A_{16}$	CH 80	CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72	CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	Read
$5C_{16}$	CH 128	CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120	CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	Read
$5E_{16}$	CH 112	CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104	CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	Read

These read only registers contain the data for a direct input read. These registers are used to read back the value written to a location configured as an output, and also to read the current state of a location configured as an input. A read of these registers will overwrite the values in the corresponding Rank 1 and Rank 2 input registers in an input configured circuit. Reading back output values does not overwrite Rank 1 and Rank 2 data in an output configured circuit.

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Rank 2 I/O Data Registers

The format and channel assignments for the Rank 2 I/O Data registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
60_{16}	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	Read/ Write
62_{16}	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	Read/ Write
64_{16}	CH 64	CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56	CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	Read/ Write
66_{16}	CH 48	CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40	CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	Read/ Write
68_{16}	CH 96	CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88	CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	Read/ Write
$6A_{16}$	CH 80	CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72	CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	Read/ Write
$6C_{16}$	CH 128	CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120	CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	Read/ Write
$6E_{16}$	CH 112	CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104	CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	Read/ Write

On READ (input) transactions:

These registers hold the last state of the inputs read from the Rank 1 or Direct input registers.

On WRITE (output) transactions:

These registers may be filled with the desired data that will appear at the outputs after the next external clock event.

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Mask Registers

The format and bit assignments for the Mask registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
70_{16}	CH 32	CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24	CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	Read/ Write
72_{16}	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	Read/ Write
74_{16}	CH 64	CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56	CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	Read/ Write
76_{16}	CH 48	CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40	CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	Read/ Write
78_{16}	CH 96	CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88	CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	Read/ Write
$7A_{16}$	CH 80	CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72	CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	Read/ Write
$7C_{16}$	CH 128	CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120	CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	Read/ Write
$7E_{16}$	CH 112	CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104	CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	Read/ Write

These registers allow the corresponding I/O channel bit to disregarded during a pattern recognition operation. Masking has no effect on the Change of State Register. A “1” written to the appropriate bit provides a “Don’t Care” condition as an I/O bit is compared to its pattern bit. The bits are set to “0” on reset.

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Local Bus Registers

The following registers are implemented on the appropriate local bus mezzanine card.

Local Bus Sink Reception Bit Registers 80_{16} - $17E_{16}$

The format and bit assignments for the Sink Reception Bit registers are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
80_{16}	00F	00E	00D	00C	00B	00A	009	008	007	006	005	004	003	002	001	000	Read/ Write
82_{16}	01F	01E	01D	01C	01B	01A	019	018	017	016	015	014	013	012	011	010	Read/ Write
84_{16}	02F															020	Read/ Write
	•															•	
	• • • • • • • • •															• • • • • • • • •	
	•															•	
$17A_{16}$	•															•	
$17C_{16}$	•															•	
$17E_{16}$	7FF	7FE	7FD	7FC	7FB	7FA	7F9	7F8	7F7	7F6	7F5	7F4	7F3	7F2	7F1	7F0	Read/ Write

Note: All above values in hex.

These read / write registers contain 2048 bits which enable(1) or disable(0) the reception of the corresponding cell in a given frame. The bit labeled 000_{16} corresponds to first cell, 001_{16} is the second cell, etc. This selects which samples are kept and which are discarded in a given frame.

These registers may only be read or written after the Enable Capture (ENA CAP) bit of the Local Bus Sink Enable / Sample Skip Register is written with a “0”.

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Local Bus Source Frame Control Register

The format and bit assignments for the Local Bus Frame Control Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
100_{16}	STB ENA	Not used	TTL 2	TTL 1	TTL 0	SF10	SF9	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0	Read/ Write

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
15	Strobe Enable (STB ENA)	"1" enables this module to source a sample clock (frame clock) onto the local bus. This allows the module to control local bus transfers. This sample clock will be a direct representation of the TTL Trigger line that is selected by bits 13-11 of this register.
14	Not Used	This bit is not used.
13-11	Trigger Selection (TTL2-TTL0)	Selects which TTL Trigger line is to be used as a Sample Clock. Data = 0 ⇒ TTL Trigger Line 0. Data = 7 ⇒ TTL Trigger Line 7.
10-00	$SF_{10} - SF_0$	Data = 0 ⇒ 1 cell per frame. Data = $7FF_{16}$ ⇒ 2048 cells per frame.

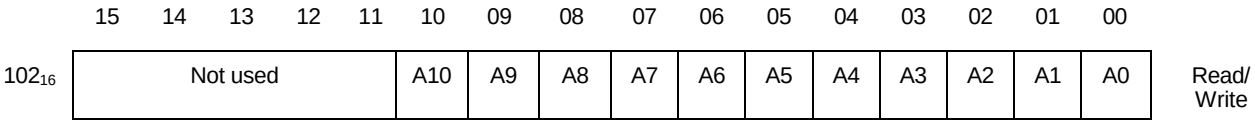
Note: Transfers to the module's Operational Registers will result in a bus error if the V387 is currently involved with activities on the Local Bus lines. Once a valid transfer to the module's operational registers has begun all data transfers over the Local Bus will be ignored by the V387.

On READ transactions bits fifteen through zero return the last value written.

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Local Bus Source Start Address

The format and bit assignments for the Local Bus Source Start Address are as follows:



On WRITE transactions:

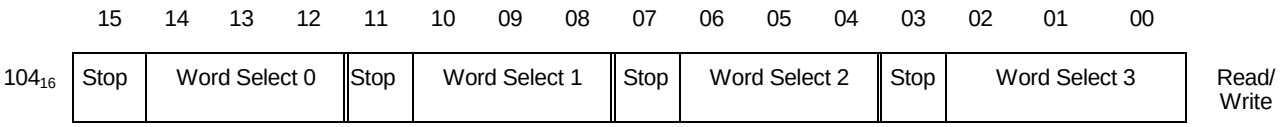
Bit(s)	Mnemonic	Meaning
15-11	Not used	These bits are not used.
10 - 00	A10-A0	Define the start address in the frame from which the V387 will begin to source data onto the local bus (000_{16} - $7FF_{16}$).

If a single V387 is used, the address should be set to 000_{16}. If multiple V387s are used as sources, the start addresses of the additional V387s should be set to start where the previous V387 stopped sourcing data. For example, if the Local Bus Source Word Select Registers (see below) of the first V387 were set to place 5 I/O Words on the bus, the first V387 should have a start address of 000_{16} and the second V387 should have a start address of 005_{16}.

On READ transactions bits fifteen through zero return the last value written.

Local Bus Source Word Select Low

The format and bit assignments for the Local Bus Source Word Select Low are as follows:



This read / write register holds the first four 3-bit addresses (000 - 111) for the 16-bit I/O Words (see Table 7 for additional information on I/O Word channel assignments) to be placed onto the local bus in the designated slot. The I/O words are read from the Rank 1 Register. With the clock source set to Local Bus Sample Clock (3_{16}) the Rank 1 Register will be updated at the start of the frame and will hold the input value until the start of the next frame.

The 16-bit data words corresponding to the selected I/O Words are addressed with the lower three bits. The I/O words are placed onto the bus until the Stop bit in one of the four-bit slots is set, making the value of the 4-bit code greater or equal to 8_{16}. For example, a one in bit 11 will stop the transfer after one transfer of a 16-bit word has been completed. With "0s" in bits 15, 11, 7 and a "1" in bit 3, three transfers of 16-bit words will be completed. Combined with the start address, this allows 16-bit words to be placed onto the bus at any time within the frame and in any order. With the Local Bus Source Word Select High Register, a maximum of eight 16-bit data words can be written to the Local Bus in a single frame by a single V387.

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Local Bus Source Word Select High

The format and bit assignments for the Local Bus Source Word Select High are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
106_{16}	Stop	Word Select 4			Stop	Word Select 5			Stop	Word Select 6			Stop	Word Select 7			Read/ Write

This read / write register holds last four 4-bit addresses for the 16-bit words to be placed onto the local bus in the designated slot. Its operation is similar to the Local Bus Source Word Select Low register. Please see table 7 for additional information in I / O word channel assignments.

108_{16} Reserved

Local Bus Source Enable Data / Frame Skip

The format and bit assignments for the Local Bus Source Enable Data / Frame Skip register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$10A_{16}$	GO	Not used							S7	S6	S5	S4	S3	S2	S1	S0	Read/ Write

This register holds the GO bit (bit 15) that must be written with a "1" in order for the V387 to begin sourcing data onto the Local Bus. It also determines the number of frames between the sourcing of data words on the local bus.

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
15	GO	This bit must be written with a "1" in order for the V387 to begin sourcing data onto the Local Bus. This bit is cleared to "0" on any reset.
14 - 08	Not used	These bits are not used.
07 - 00	S7-S0	Defines the number of frames that will be skipped before the V387 will source another data set onto the Local Bus. S7-S0 = 00_{16} ⇒ Source on every frame. S7-S0 = 01_{16} ⇒ Source on every other frame. . . . S7-S0 = FF_{16} ⇒ Source on every 255th frame.

On READ transactions bits fifteen through zero return the last value written.

$10C\text{-}10E_{16}$ Reserved

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Local Bus Sink Enable/Frame Skip

The format and bit assignments for the Local Bus Sink Enable / Sample Skip register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
180_{16}	ENA CAP	Not used							SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Write

On WRITE transactions:

Bit(s)	Mnemonic	Meaning
15	Enable Capture (ENA CAP)	Must be set to "1" to allow acceptance of data from the local bus. Setting this bit disables access to the Local Bus Sink Reception Bit Registers.
14-08	Not used	These bits are not used.
07 - 00	SC7 - SC0	Specifies the frame count interval. If this value is 00_{16} the V387 stores data on every frame. If this value is 01_{16} it stores on every other frame, etc. following the cell pattern written to the Local Bus Sink Reception Bit Registers

Note: When ENA CAP(bit 15) of this register is set to "1", transfers to the module's Operational Registers will result in a Bus Error if the V387 is currently involved with activities on the Local Bus lines. Once a valid transfer to the module's Operational Registers has begun, all data transfers to the V387 over the Local Bus lines will be ignored, until the transfer to the Operational Registers is complete.

Local Bus Sink Word Select Low

The format and bit assignments for the Local Bus Sink Word Select Low register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
182_{16}	Not used	Word Select 3			Not used	Word Select 2			Not used	Word Select 1			Not used	Word Select 0			Write

This register holds eight 3-bit addresses of daughter cards that will be updated with the 16-bit words taken off the local bus in the designated slot. Bits 15, 11, 7, and 3 are not used by the V387 and should be "0s". The corresponding 16-bit words of I / O data are addressed with the lower three bits. This, along with the sink reception bits and / or the previous sink register allow 16-bit words to be taken off the bus:

1) starting or stopping at any time in the frame,

2) placed at any I / O location (in any order),

3) while storing each frame, every other frame, etc.

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Please refer to table 7 for additional information on I/O Word channel assignments.

Local Bus Sink Word Select High

The format and bit assignments for the Local Bus Sink Word Select High register are as follows:

	15	14 13 12	11	10 09 08	07	06 05 04	03	02 01 00	
184_{16}	Not used	Word Select 7	Not used	Word Select 6	Not used	Word Select 5	Not used	Word Select 4	Write

This register holds last four 3-bit addresses for the 16-bit words to be taken off the local bus in the designated slot. Its operation is similar to the Local Bus Sink Word Select Low register. Please refer to table 7 for additional information on I/O Word channel assignments.

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V387 Example: Setup V387 to source data onto Digi-bus on VXI trigger

This example shows the registers that should be written in order to configure the V387 as an input device that will source all I/O words onto the Digi-bus with the assertion of VXI TTL trigger line 0. The V387 should have input or bi-directional mezzanine cards installed, as well as the Digi-bus source card.

1. Read Configuration Register 0x06 (A16 space) for A32 offset.
2. Write Bi-directional Configuration Register (A32 offset 0x08) with 0x80FF to disable auto update and configure TTL bits as inputs.
3. Write Pattern Recognition Enable Register (A32 offset 0x0A) with 0x0 to disable pattern recognition.
4. Write I/O Word Polarity Register (A32 offset 0x10) with 0x0 to set polarity of input words to high-true.
5. Write Clock Source Register (A32 offset 0x16) with 0x3333 to set the Mezzanine Card Clock source to the local bus sample clock for all cards.
6. Write Local Bus Frame Control Register (A32 offset 0x100) with 0x8007 to set strobe enable bit, setup 8 cells of data and select TTL Trigger line 0 as the Sample Clock.
7. Write Local Bus Enable Data Source Register (A32 offset 0x10A) with 0x0 to set the GO bit to 0, so the Digi-bus is not being sourced.
8. Write Local Bus Source Start Address Register (A32 offset 0x102) with 0x0 to set the start address to 0 because V387 is the only source in this example.
9. Write Local Bus Source Word Select Low Register (A32 offset 0x104) with 0x1032 so data comes across as 1, 2, 3, 4.
10. Write Local Bus Source Word Select High Register (A32 offset 0x106) with 0x5476 so the rest of the data comes across as 5, 6, 7, 8.
11. Write Local Bus Source Sample Skip Register (A32 offset 0x108) with 0x0 to get every Digi-bus sample.
12. Write Local Bus Enable Data Source Register (A32 offset 0x10A) with 0x8000 to write the GO bit which enables Digi-bus data sourcing.

Now toggling TTL trigger line 0 will latch input data for all I/O words and then source to the local bus.

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DESCRIPTION OF OPTIONAL CARDS

Input Card Options

Model P300-300A	16-Channel Isolated Input 5VDC
Model P300-301A	16-Channel Isolated Input 12VDC
Model P300-302A	16-Channel Isolated Input 24VDC
Model P300-303A	16-Channel Isolated Input 48VDC
Model P300-304A	16-Channel Isolated Input 120VAC
Model P300-305A	16-Channel Isolated Input 16VDC
Model P300-306A	16-Channel Isolated Input 28VDC

These seven isolated voltage options (TTL, 12VDC, 16VDC, 24VDC, 28VDC, 48VDC, and 120VAC), are configured for input signaling. Input isolation (500 volts peak) is achieved by using LED / photo-transistor optical isolators. Each option has 16 circuits with identical input voltage ratings, and the switching threshold is approximately ½ the rated input voltage. Each circuit draws more than five, but less than 10 milliamperes. The logic convention is such that a contact closure (voltage present) is interpreted as a logical "1". Each input is conditioned by filtering after the optical isolator. The filter time constant is programmable from 5.33 microseconds to over 1 second in 64 steps.

Input data is controlled on a 16-bit basis. Double buffering of data allows the module to simultaneously sample all inputs. These actions are programmable for each card and may be initiated by selecting either a trigger line or one of four external sources.

Inputs are continuously filtered according to the time constant specified in the Debounce Configuration Registers. READ operations of the appropriate Operational Registers can supply various levels of data. For example, one of these mezzanine cards is located in position C3. The Bi-directional Configuration Register should have its Mode bit set (bit 15 should be cleared to "1") and bit 00 should be set to "1" (configured as input). Then, the Debounce Time Configuration Register 2 (bits 05-00) should be configured to allow the desired level of contact bounce suppression. By clearing bits 05-00, the minimum time constant (5.33 microseconds) is selected. Now, READ operations at the proper locations provide the following data (see Figure 7):

Offset	Register Name	Action
62_{16}	Rank 2 Register, Lower Byte	Retains data of last read to Rank 1.
22_{16}	Rank 1 Register, Lower Byte	Returns the latched value in the Rank 1 buffer.
52_{16}	Direct Input Read Register Lower Byte	Returns the present state of the inputs.

The sense of the input words can be inverted by setting the bits in the Word Polarity Register.

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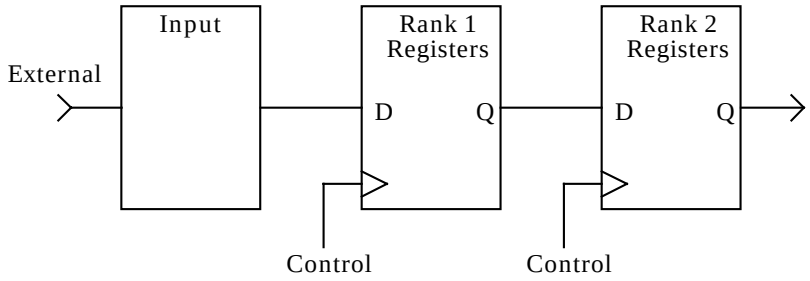


Figure 7. Simplified Input Circuit

By reading the inputs directly (offset 52_{16} in above example), the data returned is the input (D) to the Rank 1 buffer. When Rank 1 is read (offset 22_{16} in above example), the data returned will be the value that was latched after the last transition of the clock source, and the input (D) to the Rank 2 buffer. As Rank 2 is read, the value returned will be the output (Q) of the Rank 2 buffer. Notice also, both the true and complemented forms of any input register are available. This selection is made by choosing either low true by writing a "1" to the Word Polarity Register at the appropriate bit location, or high true by writing a "0".

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Output Card Options

Model P300-341A	16-Channel Isolated Output
Model P300-342A	16-Channel Reed Relay Output
Model P300-343A	16-Channel Form "C" Relay Output
Model P300-344A	16-Channel AC Switch

Output-only cards are available with output circuits composed of reed relays, optical isolators, isolated AC switches, or single-pole, double-throw (Form "C") contacts. Each output card is a 16-channel circuit.

Output data is controlled in a 16-bit basis. Double buffering of I/O data allows the module to simultaneously sample or update all outputs. These actions are programmable for each card and may be initiated by selecting either a trigger line or one of four external sources. The logical sense of each output word can also be set under program control.

WRITE operations of the appropriate Operational Registers can update the outputs in several ways. For instance, one of these output mezzanine cards is located in position C3. The Bi-directional Configuration Register should have its Mode bit cleared to “0” or bit 01 should be set to “0”. The clock source register bits 03-00 should also be used to select the event that causes the Rank 1 and Rank 2 registers to latch data intended for the outputs. Now, WRITE operations at the proper locations provide the following data:

Offset	Register Name	Action
62_{16}	Rank 2 Register, Lower Byte	Latches a next state value into the Rank 2 output buffer.
22_{16}	Rank 1 Register, Lower Byte	Immediately updates the outputs through the Rank 1 buffer. Overwrites Rank 2 buffer (Same data in both buffers).

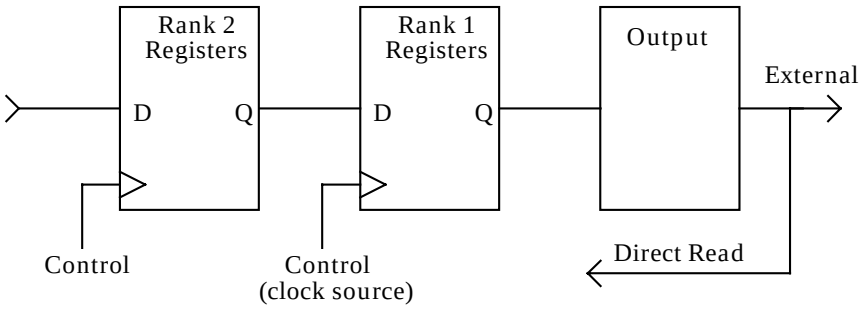


Figure 8. Simplified Output Circuit

Writes to the Rank 1 Registers always update the outputs. Writing to the Rank 2 holds the data in the Rank 2 Registers until the next transition of the clock source, at which point the data is latched into the Rank 1 Registers and the outputs are updated. Both the true and complemented forms of the Rank 1 output are available to the output circuits by choosing either low true (“1”) or high true (“0”) data in the Word Polarity Register.

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Bi-Directional Options

Model P300-380A 32-Channel TTL Input/Output

The P300-380 combines all the read and write capabilities of both the input and output circuits described before. All I/O lines have open-collector output drivers with TTL pull-ups and overvoltage protection. On power-up, all channels are set to be inputs. A strap on each card determines the initial state of the channels after power-up. The initial state of the outputs is set low at the factory, but can be modified to +5V by moving the strap.

Model P300-382A 16-Channel Differential Input/Output

The P300-382A has all the read and write capabilities of the 32-channel TTL I/O card except there are 16 channels of differential signals conforming to the RS-422 signal levels. The termination resistors are socketed, and can be changed depending on the system configuration. Termination resistors are initially 50Ω in series with each leg and 100Ω across the differential path is the initial arrangement. Programmable debounce is not supported on this card. On power-up, all channels are initially set to be inputs.

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Digi-bus Options

Model P500-387A Local Bus Data / Frame Source

This mezzanine card may occupy position C2 on the V387. This card provides the necessary circuitry for the V387 to control, as well as source data onto the VXIbus Local Bus Lines.

Model P501-387A Local Bus Data Sink

This mezzanine card may occupy position C2 on the V387. This card provides the necessary circuitry for the V387 to capture off the VXIbus Local Bus Lines. It provides the capability of selecting a subset of data from the Digi-bus on a channel-by-channel (word) basis as well as selecting every Nth frame. Frame selection is determined on a frame count basis ranging from selecting every frame to every 255th frame.

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APPENDIX B: V387 Board Drawings

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This block diagram is correct only for the AC card, and is incorrect for the DC cards.

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