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User Manual

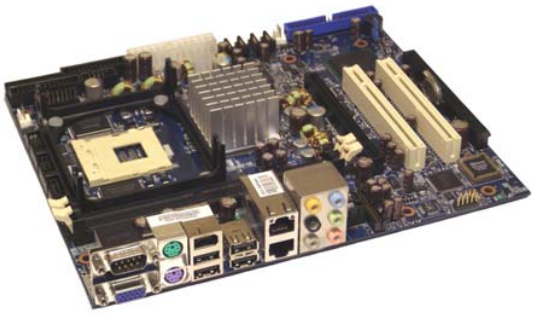
for the Motherboards:



986LCD-M/mITX



986LCD-M/mITX BGA



986LCD-M/Flex



986LCD-M/ATXE



986LCD-M/ATXP

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Document revision history.

Revision	Date	By	Comment
Q	April 22nd 2008	MLA	Removed note that WOL only on ETH1. 3.3V tolerance increased.
P	Feb. 28th 2008	MLA	Battery load information added. Added "Resume On PME#"
O	Jan. 10th 2008	MLA	Deleted remaining Floppy controller info in BIOS description. Added LED color info for ETHER2/3. ETHER1 removed from ATXE picture. Chp. 5: ATXPWR corrected and ATX+12V added. Revised TV-Out and MacroVision licencing text.
N	Oct. 18th, 2007	MLA	Correction to printer connector chapt. 4.8 and in "Onboard connectors" and in note for ETHER2/3 connector. Included warning in Installation procedure.
M	Sep. 28th, 2007	MLA	In "Component Main Data" ACPI 2.0 changed to ACPI 3.0. BIOS setting "Plug and Play" default corrected to "No". Setting "Quiet Boot" has added option "Black Screen" and "White Screen" and setting "Long Splash" is added. Settings "Auto Adjust Boot Priority" and "Removable Devices 1st" are replaced by "Default init boot order". COM port description added +/-12V.
L	Sep. 6th, 2007	MLA	Added Supervisor Password protection diagram and more details. Added info to "Video Function Configuration". Core Duo L2400 added. XP Embedded "possible limitation" removed.
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G - J	Jun. 1st, 2007	MLA	*(Text removed in revision O of this document)*
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A	Dec. 5th 2006	MLA	*(Text removed in revision L of this document)*
0	July 6, 2006	PJA	First preliminary manual version.

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- CPU Board
  1. Type.
  2. Part-number.
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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1. Introduction

This manual describes the 986LCD-M/Flex, 986LCD-M/ATXP, 986LCD-M/ATXE and 986LCD-M/mITX boards made by KONTRON Technology A/S. The boards will also be denoted 986LCD family if no differentiation is required.

All boards are to be used with the Intel® Core™Duo, Intel® Core™ 2 Duo, Intel® Core™Solo and Celeron® M Processors. These belong to the Intel Yonah and Merom processor families.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the 986LCD Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 3 before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus. Except for the CMOS Clear jumper, no jumper configuration is required.

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2. Installation procedure

2.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has CPU, DDR DRAM and Cooler mounted. In this case Step 2-4 can be skipped.

1. Turn off the power supply.



Warning: Do not use Power Supply without 3.3V monitoring watchdog, which is standard feature in ATX Power Supplies.
Running the board without 3.3V connected will damage the board after a few minutes.

2. Insert the DDR2 DIMM 240pin DRAM module(s). **Important**: If only one module is used then use Slot 0. Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR2 DIMM modules contact your Distributor or FAE (list under preparation).
   DDR2-667 DIMM 240pin DRAM modules (PC5400) are supported.

3. Install the processor. The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. Intel® Core™Duo, Intel® Core™ 2 Duo, Intel® Core™Solo and Celeron® M Processors are supported, refer to supported processor overview for details.

4. Use heat paste or adhesive pads between CPU and cooler and connect the Fan electrically to the FAN_CPU (J21) connector.

5. Insert all external cables for hard disk, keyboard etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to flat panel support. To achieve UDMA-66/100 performance on the IDE interface, 80poled UDMA cables **must** be used. When using bootable SATA disk, then connect to SATA0 or SATA2 or select in BIOS “ATA/IDE Configuration” = Enhanced.

6. Connect power supply to the board by the ATX/ BTXPWR and 4-pin ATX connectors. For board to operate connection of both the ATX/BTX and 4-pin ATX (12V) connectors are required.

7. Turn on the power on the ATX/ BTX power supply.

8. The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A “normally open” switch can be connected via the FRONTPNL connector.

9. Enter the BIOS setup by pressing the “DEL” key during boot up. Refer to the Software Manual (under preparation) for details on BIOS setup.
   Enter Advanced Menu / CPU Configuration / Intel SpeedStep Tech. and set this option to “Maximum Performance”.

Note: To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.



Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

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2.2 Requirement according to EN60950

Users of 986LCD boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

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3. System specification

3.1 Component main data

The table below summarises the features of the 986LCD-M/mITX, 986LCD-M/Flex, 986LCD-M/ATXP and 986LCD-M/ATXE embedded motherboards.

Form factor	986LCD-M/mITX: mini ITX (170.18millimeters by 170.18millimeters) 986LCD-M/Flex: Flex-ATX (190,50millimeters by 228,60millimeters) 986LCD-M/ATXP: ATX (190,50millimeters by 304,00millimeters) 986LCD-M/ATXE: ATX (190,50millimeters by 304,00millimeters)
Processor	• Support for Intel® Core™Duo, Intel® Core™ 2 Duo, Intel® Core™Solo and Celeron® M Processors in 478pin Micro-FCPGA package with up to 667MHz system bus and 1/2/4MB internal cache. • Yonah (65 nanometer) and Merom (65 nanometer) family processors.
Memory	• 2 pcs DDR2 DIMM 240pin DRAM sockets. • Support for DDR 400/533/667 (PC3200/PC4200/PC5300) • Support system memory from 256MB up to 3GB (2+1GB type Samsung PC5300U-M378T5663AZ3-CE6 + PC5300U_M378T2953CZ3-CE6). • ECC not supported
Chipset	Intel 945GM Chipset consisting of: • Intel® 82945G Graphics and Memory Controller Hub (GMCH) • Intel® ICH7R I/O Controller Hub (ICH7R) • 8 Mbit Firmware Hub (FWH)
Video	• Intel® Integrated Graphics Engine (Generation 3.5) • Intel® Graphics Media Accellerator 950 (Intel® GMA 950) • Dynamic Video Memory Technology (DVMT) 3.0, 160MB/224MB when using SDRAM 256MB/512MB min. (System memory is allocated when it is needed dynamically). • Analog Display Support CRT, 400-MHz integrated RAMDAC with support for analogue monitors up to 2048x1536 at 75 Hz • Single or dual channel 18bit LVDS panel support (OpenLDI/ SPWG) up to UXGA (1600x1200) panel resolution. Interlaced Display output support. **NOTE**: Support of 24bit OpenLDI/ SPWG panels are not officially supported by Intel®, but is supported by the 986LCD series boards by Kontron. Kontron intends to continue to provide 24bit OpenLDI/ SPWG panel support even if Intel® withdraws this from the chipset. • TV-Out option, NTSC/ PAL, three integrated 10-bit DACs, Macrovision support. **IMPORTANT:** If the TV-Out option is available then you must make agreement with Macrovision (http://www.macrovision.com/) about lincence fee. Only Macrovision (not Kontron) can determine the actual licence fee which depends on the application. • Serial Digital Video Out (SDVO) ports (2 channels) for additional CRT, LVDS panel, DVI, TV-Out and/or HDMI support via Advanced Digital Display 2 (ADD2) cards or Media Expansion Cards. Dual independent pipe support, Mirror and Dual independent display support. Dual Monitor support with combinations of LVDS interface, SDVO port, CRT and TV-Out.
Audio	Audio, 7.1 and 7.2 Channel High Definition Audio Codec using the Realtek ALC882 codec • Line-out • Line-in • Surround output: SIDE, LFE, CEN, BACK and FRONT • Microphone: MIC1 • CDROM in • SPDIF Interface Onboard speaker

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I/O Control	Winbond W83627THF LPC Bus I/O Controller
Peripheral interfaces	• Four USB 2.0 ports on I/O area • Four USB 2.0 ports on internal pinrows • One IEEE1394a Firewire port on I/O area (IEEE1394a-2000 OHCI controller) • One IEEE1394a Firewire port on internal pinrow (IEEE1394a-2000 OHCI controller) • Four Serial ports (RS232) • One Parallel port, SPP/EPP/ECP • Four Serial ATA 300 IDE interfaces • Two Parallel ATA IDE interfaces with UDMA 33, ATA-66/100 support • PS/2 keyboard and mouse ports
LAN Support	• 986LCD-M/mITX: 3x 10/100/1000Mbits/s LAN using Realtek RTL8111B controllers • 986LCD-M/Flex: 2x 10/100/1000Mbits/s LAN using Realtek RTL8111B controllers • 986LCD-M/ATXP: 3x 10/100/1000Mbits/s LAN using Realtek RTL8111B controllers • 986LCD-M/ATXE: 2x 10/100/1000Mbits/s LAN using Realtek RTL8111B controllers • PXE netboot supported. Wake On LAN (WOL) supported.
BIOS	• Kontron Technology / AMI BIOS (core version) • Support for Advanced Configuration and Power Interface (ACPI 3.0), Plug and Play o Suspend To Ram o Suspend To Disk o Intel Speed Step • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • RAID Support (RAID modes 0, 1, 5 and 10) (for Linux O/S only RAID 0 and 1)
Expansion Capabilities	• PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.3) o 986LCD-M/mITX: 1 slot PCI 2.3, 32 bits, 33 MHz, 5V compliant o 986LCD-M/Flex: 2 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant o 986LCD-M/ATXP: 6 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant o 986LCD-M/ATXE: 5 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant • PCI-Express bus routed to PCI Express slot(s) (PCI Express 1.0a) o 986LCD-M/mITX: 1 slot PCI-Express x16 o 986LCD-M/Flex: 1 slot PCI-Express x16, 1 slot PCI-Express x4 o 986LCD-M/ATXP: 1 slot PCI-Express x16 o 986LCD-M/ATXE: 1 slot PCI-Express x16, 1 slot PCI-Express x4 • Mini PCI-Express routed to mini PCI-Express connector Support for Mini PCI-Express modules with no components on backside. o 986LCD-M/mITX: 1 slot mini PCI-Express x1 o 986LCD-M/Flex: None o 986LCD-M/ATXP: 1 slot mini PCI-Express x1 o 986LCD-M/ATXE: None • SMBus routed to FEATURE, PCI slot, PCI Express and mini-PCI Express connectors • LPC Bus routed to TPM connector • DDC Bus routed to LVDS and CRT connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_CPU, FAN_SYS and FEATURE • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 7ºC) • Voltage monitoring • Intrusion detect input SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• Win2000 • WinXP • Win2003 • WinXP Embedded • WinCE.net (limitations may apply) • Linux: Feodora Core 5, Suse 10.01 (limitations may apply)

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Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 (986LCD-M/ATXP approval pending) **Theoretical MTBF:** 160.000/91.000 hours @ 40/60ºCCalculation based on Telcordia SR-332 method. **Restriction of Hazardeous Substances (RoHS):** All boards in the 986LCD-M family are RoHS compliant. **Capacitor utilization:** No Tantal capacitors used. Only Japanese brand Aluminium capacitors rated for 100ºC is used.
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Toshiba / Part-number CR2032. Expected minimum 5 years retention varies depending on temperature, actual application on/off rate and variation within chipset and other components. Approximately current draw is 2.2µA (no PSU connected). **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

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3.2 Processor support table.

The 986LCD-M/mITX, /Flex, /ATXP and /ATXE are designed to support the PGA (478 pins) processors:

Intel® Core™ 2 Duo Mobile Processor, Merom 65 nm process, FSB 667MHz with 4 MB L2 cache
Intel® Core™ Duo Processor, Yonah 65 nm process, FSB 667MHz with 2 MB L2 cache
Intel® Core™ Solo Processor, Yonah 65 nm process, FSB 667MHz with 2 MB L2 cache
Celeron® M Processor, Yonah 65 nm process, FSB 533MHz with 1 MB L2 cache

Processor Brand	Clock Speed	Processor Number	sSpec no.	Thermal Guideline	Embedded
Intel® Core™ 2 Duo, 65nm, 4 MB L2	2.33 GHz	T7600	SL9SD	34.0 W	No
	2.16 GHz	**T7400**	**SL9SE**	**34.0 W**	**Yes**
	2.00 GHz	T7200	SL9SF	34.0 W	No
	1.83 GHz	T5600	SL9SG	34.0 W	No
	1.66 GHz	T5500	SL9SH	34.0 W	No
Intel® Core™ Duo, 65nm, 2 MB L2	2.16 GHz	T2600	SL8VN	31.0 W	No
	2.00 GHz	**T2500**	**SL8VP**	**31.0 W**	**Yes**
	1.83 GHz	T2400	SL8VQ	31.0 W	No
	1.66 GHz	T2300	SL8VR	31.0 W	No
Intel® Core™ Solo, 65nm, 2 MB L2	1.83 GHz	T1400	SL92V	27.0 W	No
	1.66 GHz	T1300	SL8VY	27.0 W	No
Celeron® M, 65nm, 1 MB L2	**1.86 GHz**	**440**	**SL9KW**	**27.0W**	**Yes**
	1.60 GHz	420	SL8VZ	27.0W	No
	1.73 GHz	430	SL92F	27.0 W	No
	1.46 GHz	410	SL8W2	27.0 W	No
986LCD-M/mITX(BGA) w Core Duo	**1.66 GHz**	**L2400**	**SL8VW**	**15W**	**Yes**
986LCD-M/mITX(BGA) w Celeron M 1MB L2	1.06 GHz	-	-	5.5W	-

3.3 System Memory support

The 986LCD-M boards have two onboard DDR2 DIMM sockets and support the following memory features:

- 1.8V (only) 240-pin DDR2 SDRAM DIMMs with gold-plated contacts
- Supports Single- / Dual channel DDR2 SDRAM
- Supports 256 Mbit, 512 Mbit and 1 Gbit technologies for x8 and x16 width devices.
- Maximum of 3 Gbytes (2GB + 1GB) based on Samsung PC5300U-M378T5663AZ3-CE6 + PC5300U_M378T2953CZ3-CE6).
- Supports 400 MHz (PC3200) , 533 MHz (PC4200), and 667 MHz (PC5400) DDR2 devices
- 64-bit data interface (ECC not supported)

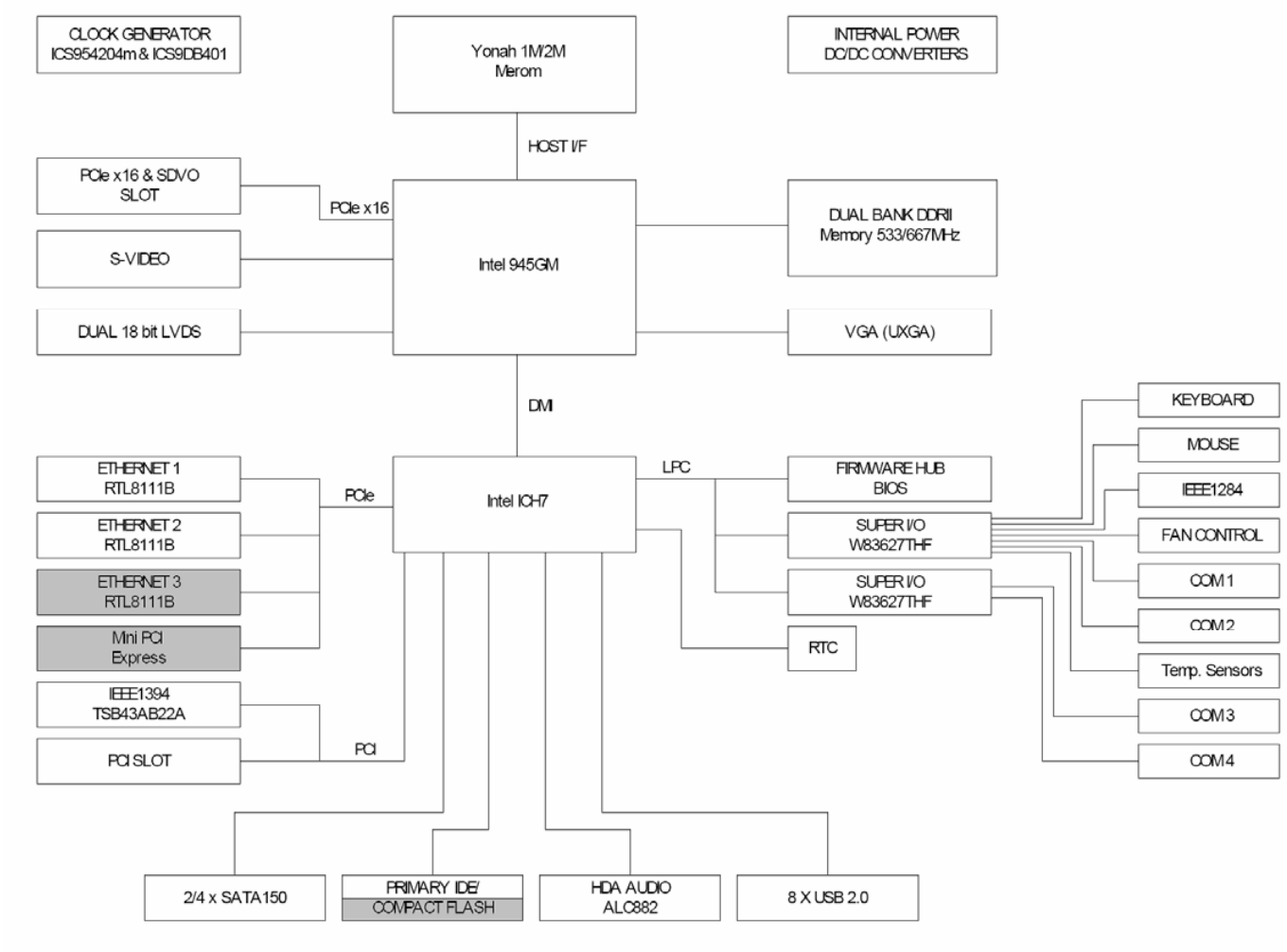
The installed DDR2 SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

Important: If only one module is used then use Slot 0.

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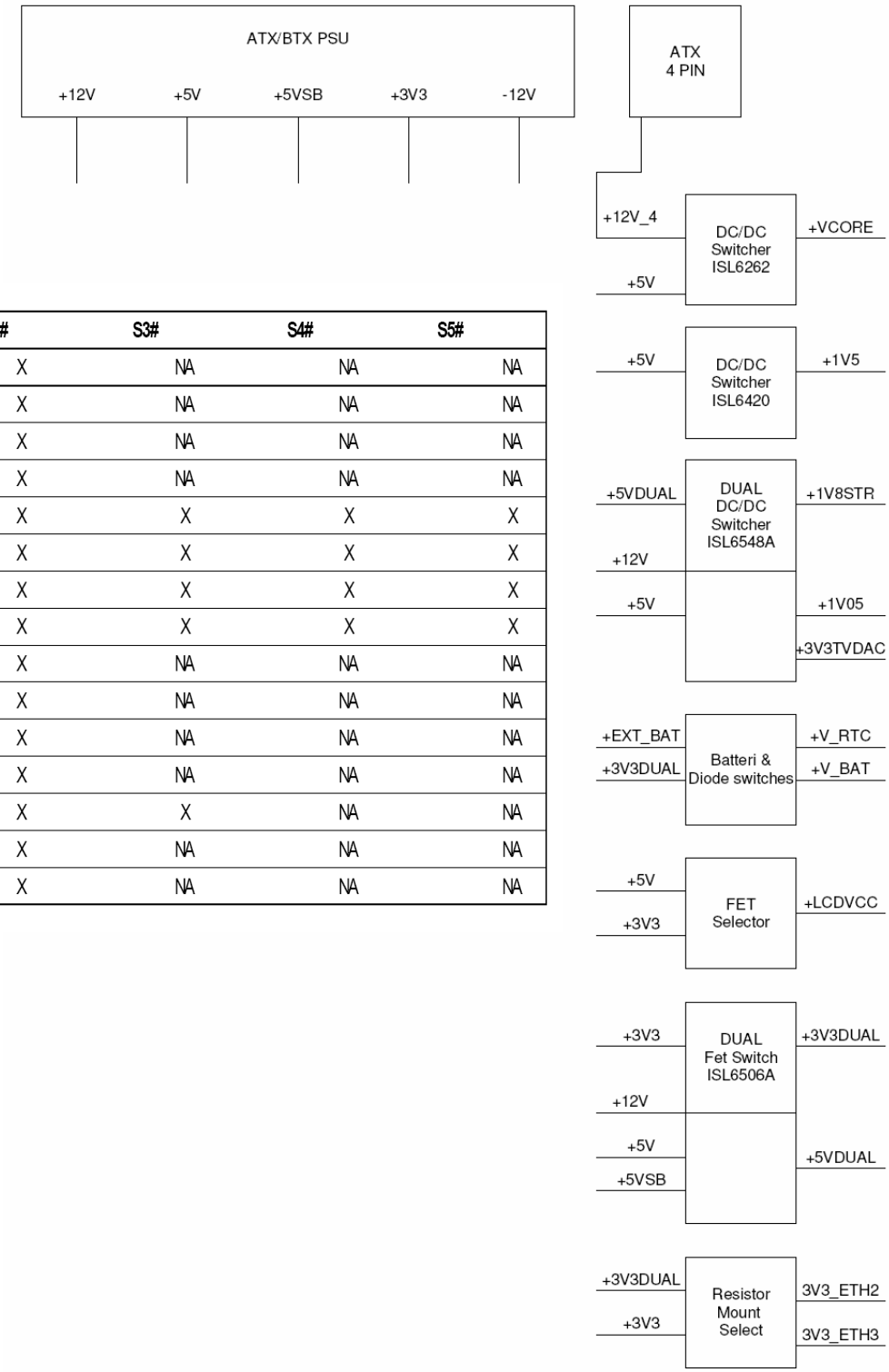
3.4 System overview

The block diagram below shows the architecture and main components of the 986LCD boards. The two key components on the board are the Intel® 945GM and Intel® ICH7R Embedded Chipsets.
Components shown shaded are optional depending on board type (986LCD-M/mITX, /Flex, /ATXP or /ATXE) and variants of the board.



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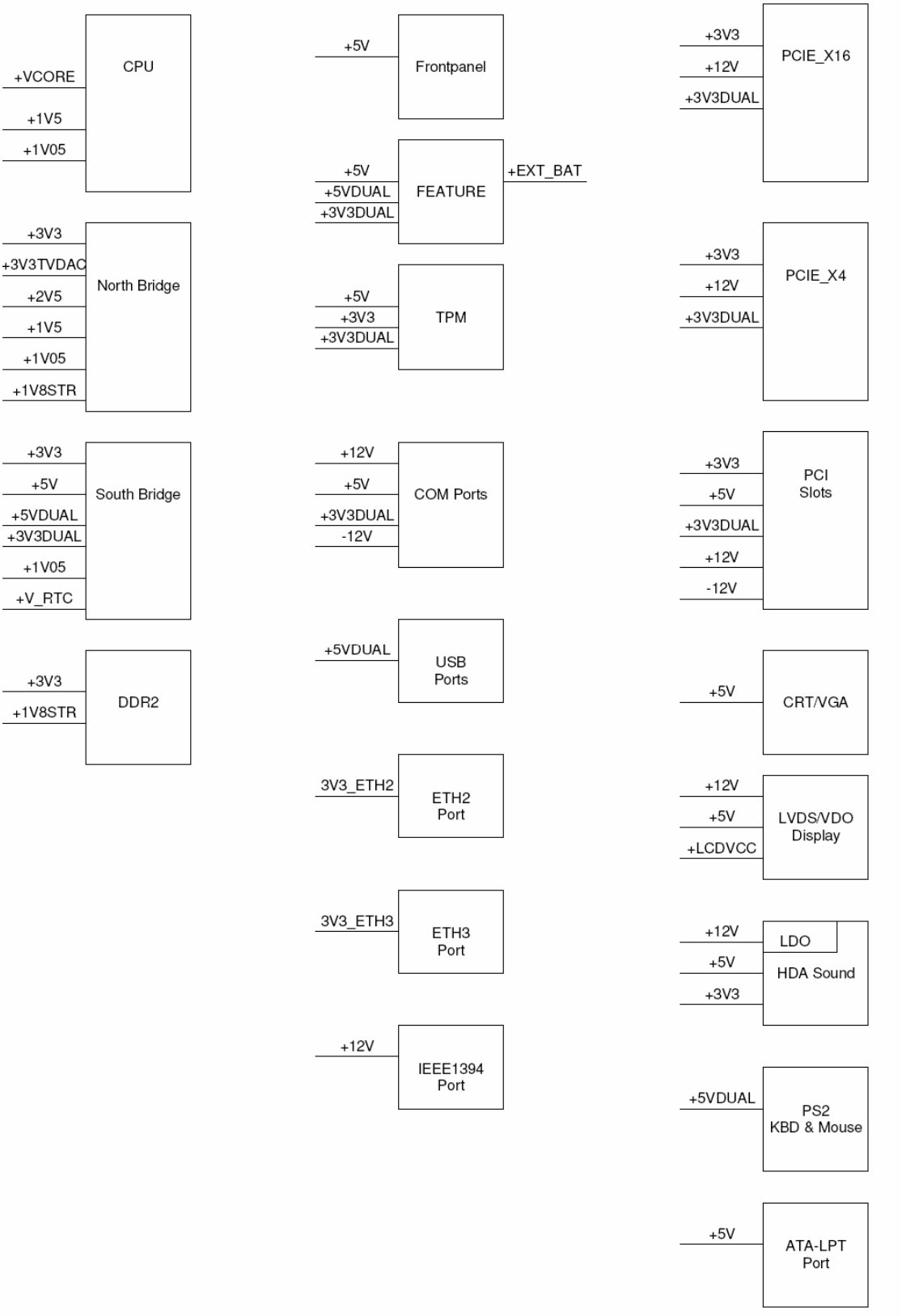
3.5 986LCD-M Power Distribution & Power State Map



POWER NET/STATE	S0#	S3#	S4#	S5#
+3V3	X	NA	NA	NA
+5V	X	NA	NA	NA
+12V	X	NA	NA	NA
-12V	X	NA	NA	NA
+5VSB	X	X	X	X
+3V3SB	X	X	X	X
+3V3DUAL	X	X	X	X
+5VDUAL	X	X	X	X
+1V05	X	NA	NA	NA
+VCORE	X	NA	NA	NA
+1V5	X	NA	NA	NA
+3V3TVDAC	X	NA	NA	NA
+1V8STR	X	X	NA	NA
+0V9STR	X	NA	NA	NA
+2V5	X	NA	NA	NA

(continues)

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3.6 Power Consumption

In order to ensure safe operation of the board, the ATX power supply must monitor the supply voltage and shut down if the supplies are out of range – refer to the hardware manual for actual power specification.

The 986LCD-M board is powered through the ATX connector and the additional 12V separate supply for CPU as specified in the ATX specification; besides this the power supplied to the board must be within the ATX specification.

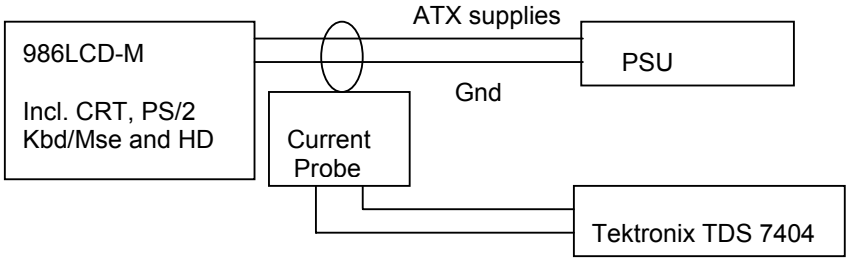
The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
Vcc3	3.135V	3.465V	Should be ±5% for compliance with the ATX specification
Vcc	4.75V	5.25V	Should be ±5% for compliance with the ATX specification
+12V	11.4V	12.6V	Should be ±5% for compliance with the ATX specification
–12V	–13.2V	–10.8V	Should be ±10% for compliance with the ATX specification
-5V	-5,50V	-4.5V	Not required for the 986LCD-M/mITX board
5VSB	4.75V	–5.25V	Should be ±5% for compliance with the ATX specification

Test system configuration

The following items are used in the test setup:

1. 986LCD-M board equipped with CPU, RAM and 12V active cooler if required
2. ATX PSU
3. CRT, PS/2 keyboard & mouse and HD
4. Tektronix TDS 7404, P6345 probes
5. Fluke Current Probe 80i-100S AC/DC



Note: The Power consumption of CRT, Fan and HD is not included.

Test results:

The power consumption of the 986LCD-M Board is measured under:

1- DOS, idle, mean
2- WindowsXP, Running 3DMARK & CPU BURN, mean
3- WindowsXP, Running 3DMARK & CPU BURN, peak
4- S1, mean
5- S3, mean
6- S4, mean
7- Inrush, peak

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986LCD-M/mITX with Core Duo (T2500) & 1GB DDR2 Ram test results:

Test	Supply	Current draw	Power consumption
DOS, Idle, mean	+12V	0.88A	10.56W
	+5V	1.48A	7.4W
	+3V3	1.22A	4.03W
	-12V	0.05A	0.6W
	5VSB	0A	0W
		Total	22.59W
WinXP, 3DMARK2000 & CPUBURN, mean	+12V	2.34A	28.08W
	+5V	1.73A	8.65W
	+3V3	1.22A	4.03W
	-12V	0.05A	0.6W
	5VSB	0A	0W
		Total	41.36W
WinXP, 3DMARK2000 & CPUBURN, peak	+12V	2.67A	32.04W
	+5V	2.48A	12.4W
	+3V3	1.28A	4.22W
	-12V	0.08A	0.96W
	5VSB	0A	0W
		Total	49.62W
S1, mean	+12V	0.83A	9.96W
	+5V	1.17A	5.85W
	+3V3	1.21A	3.99W
	-12V	0.03A	0.36W
	5VSB	0A	0W
		Total	20.16W
S3, mean	+12V	0A	0W
	+5V	0A	0W
	+3V3	0A	0W
	-12V	0.03A	0.36W
	5VSB	0.64A	3.68W
		Total	4.04W
S4, mean	+12V	0A	0W
	+5V	0A	0W
	+3V3	0A	0W
	+-12V	0A	0W
	5VSB	0.64A	3.2W
		Total	3.2W
Inrush, peak	+12V	5.08A	
	+5V	2.48A	
	+3V3	3.52A	
	-12V	0.3A	
	5VSB	2.92A	

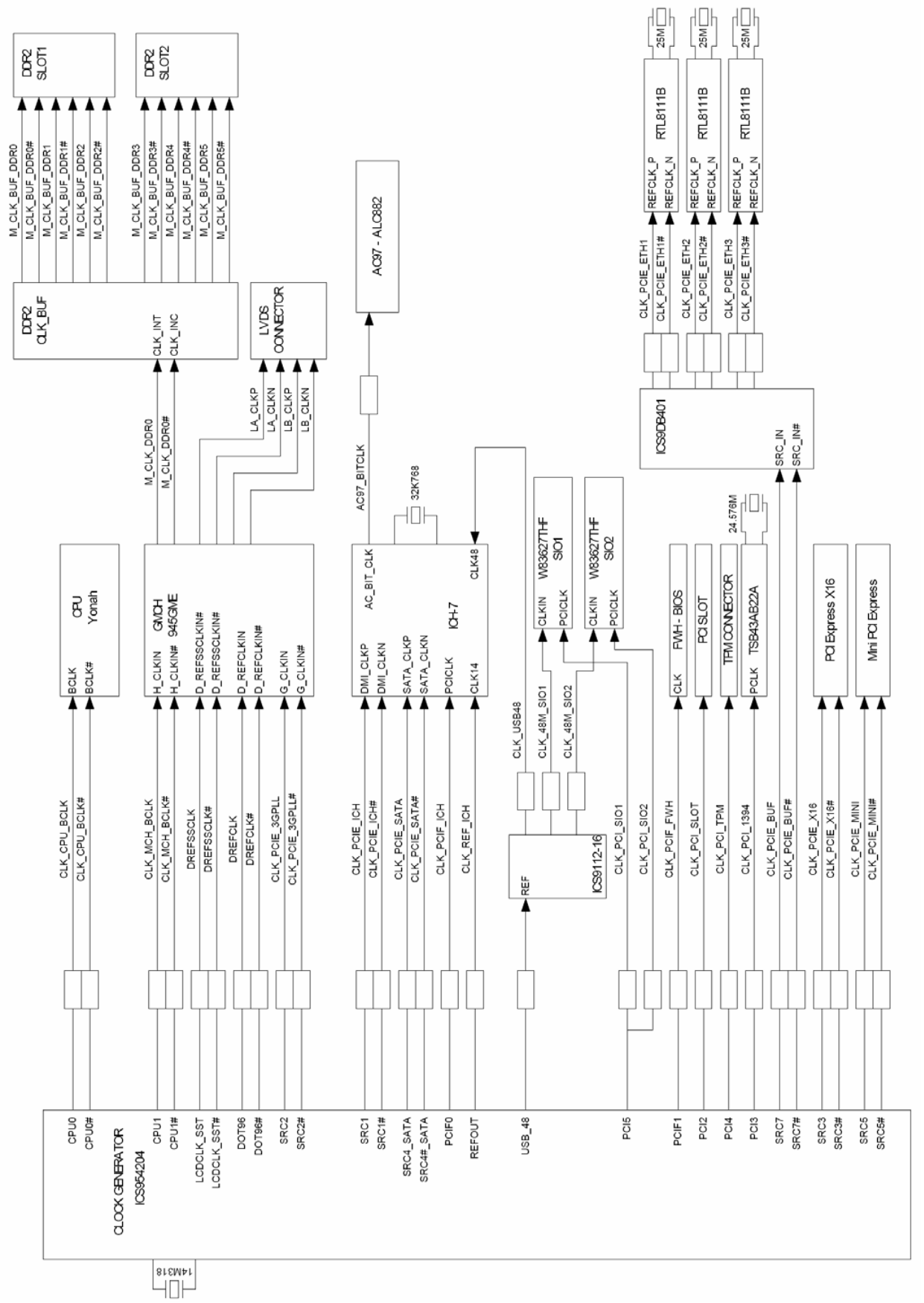
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986LCD-M/mITX with w/1.06GHz Celeron M 512MB test results:

Test	Supply	Current draw	Power consumption
DOS, Idle, mean	+12V	0.36A	4.32W
	+5V	1.37A	6.85W
	+3V3	1.31A	4.323W
	-12V	0A	0W
	5VSB	0A	0W
		Total	15.493W
WinXP, 3DMARK2000 & CPUBURN, mean	+12V	0.4A	4.8W
	+5V	1.47A	7.35W
	+3V3	1.54A	5.08W
	-12V	0A	0W
	5VSB	0A	0W
		Total	17.232W
WinXP, 3DMARK2000 & CPUBURN, peak	+12V	0.61A	7.32W
	+5V	2.1A	10.5W
	+3V3	1.64A	5.41W
	-12V	0A	0W
	5VSB	0A	0W
		Total	23.232W
S1, mean	+12V	0.25A	3W
	+5V	1.05A	5.25W
	+3V3	0.75A	2.48W
	-12V	0A	0W
	5VSB	0A	0W
		Total	10.73W
S3, mean	+12V	0A	0W
	+5V	0A	0W
	+3V3	0A	0W
	-12V	0A	0W
	5VSB	0.18A	0.9W
		Total	0.9W
S4, mean	+12V	0A	0W
	+5V	0A	0W
	+3V3	0A	0W
	+-12V	0A	0W
	5VSB	0.18A	0.9W
		Total	0.9W
Inrush, peak	+12V	1.54A	
	+5V	1.02A	
	+3V3	1.2A	
	-12V	0.09A	
	5VSB	3.5A	

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3.7 986LCD-M Clock Distribution



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4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

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The connector definitions follow the following notation:

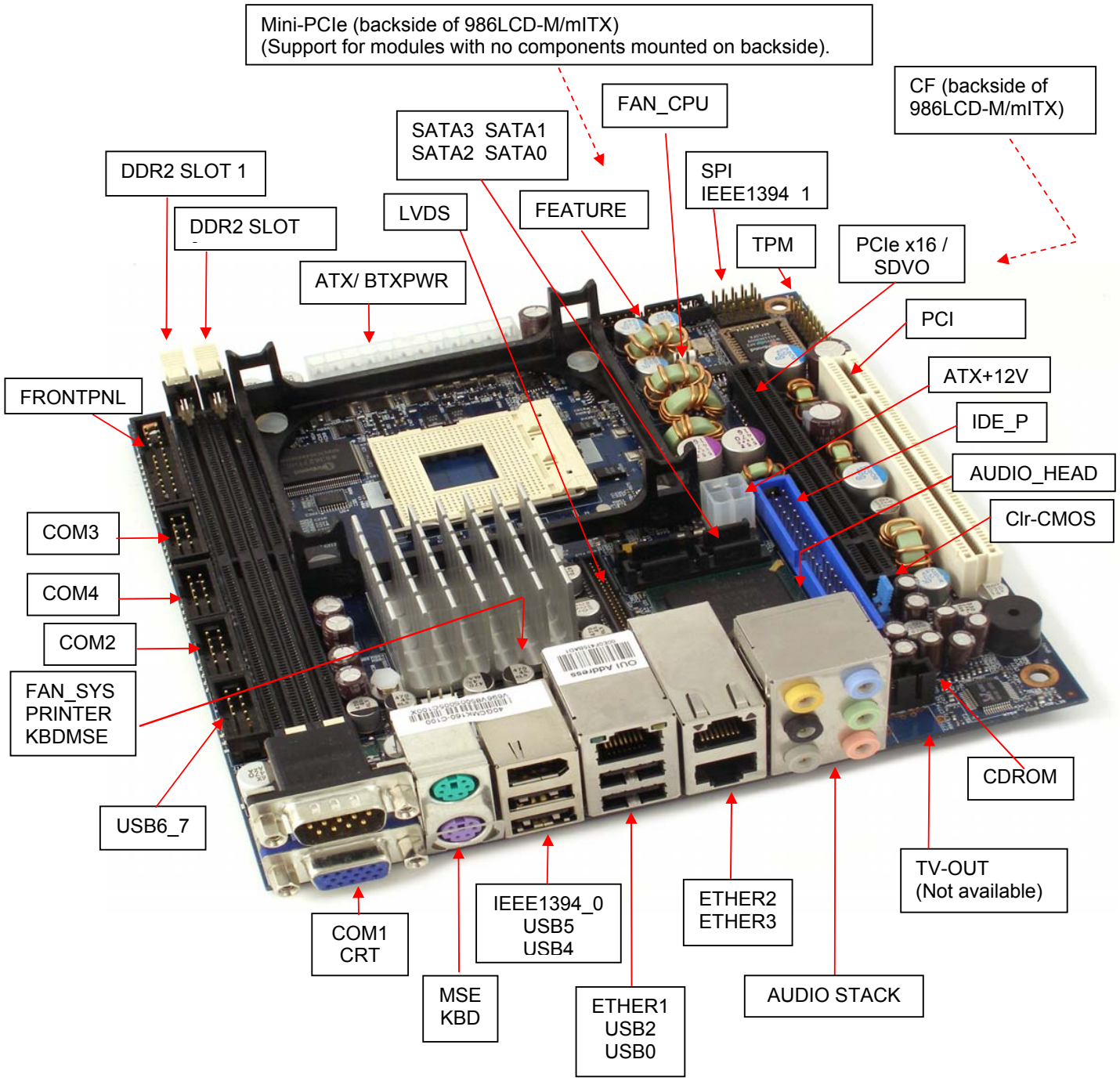
Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

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4.1 Connector layout

4.1.1 986LCD-M/mITX



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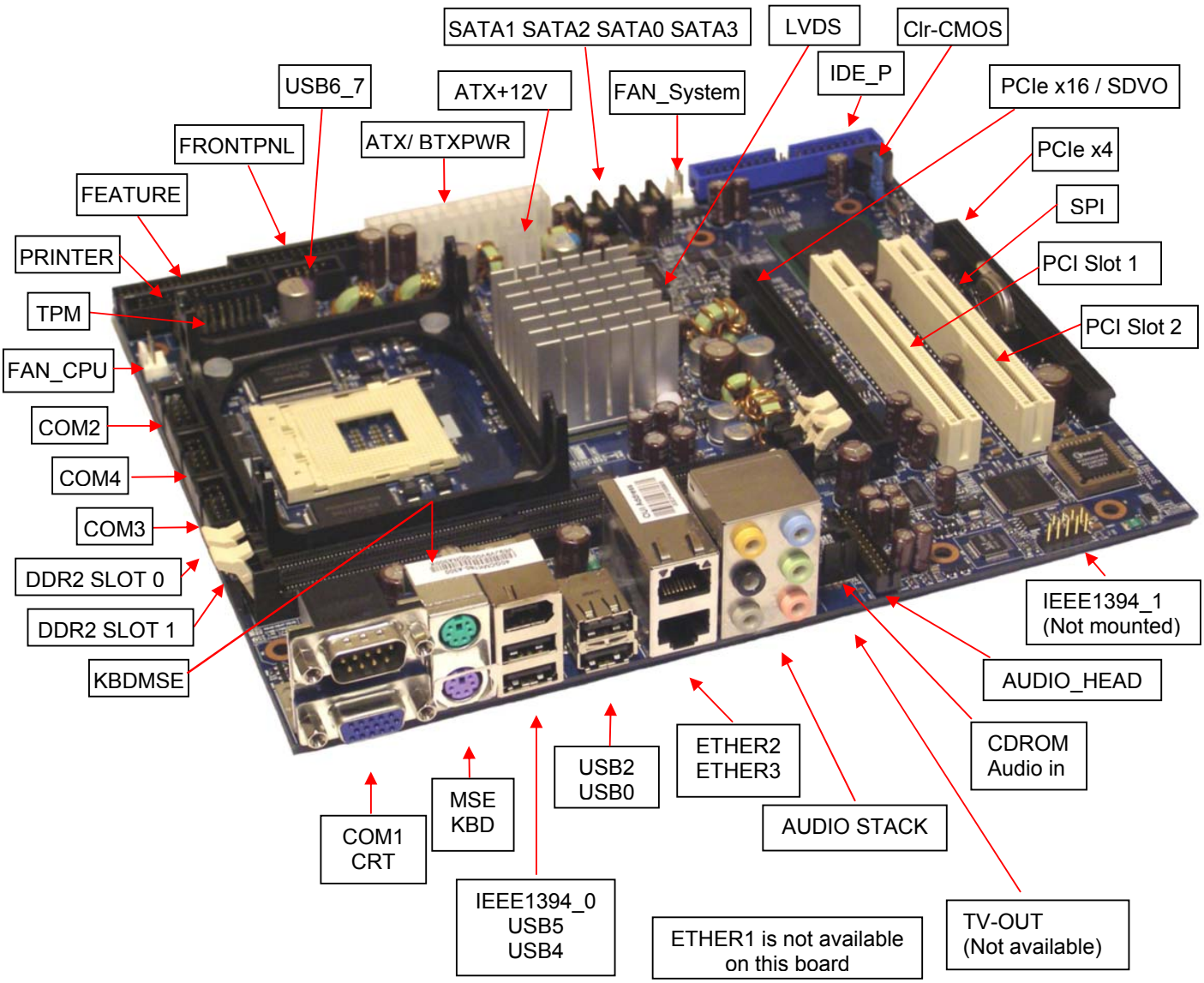
986LCD-M/mITX BGA

Same connectors available as on the standard 986LCD-M/mITX, except that CPU socket is replaced with BGA version of CPU. (Passive cooler included).



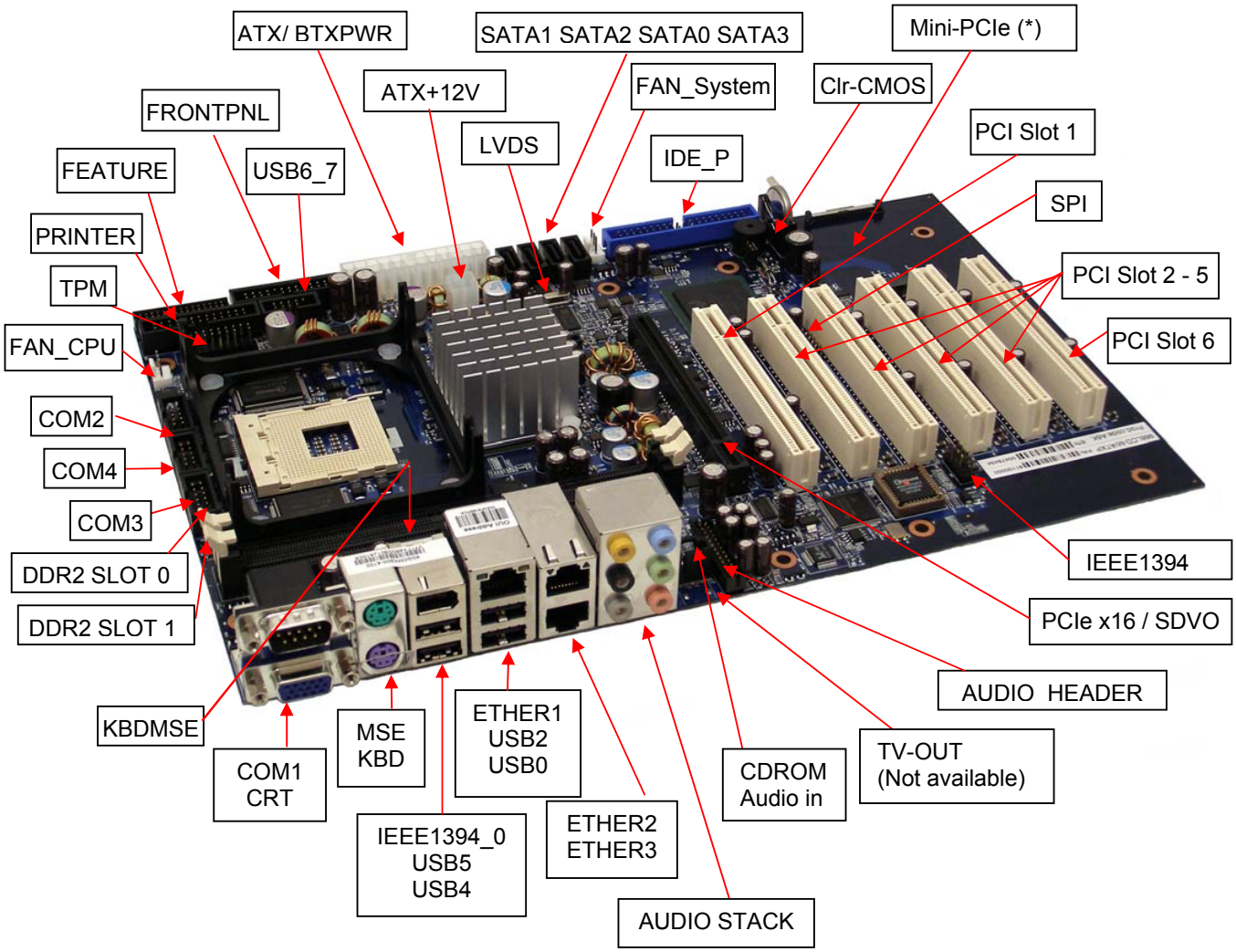
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4.1.2 986LCD-M/Flex



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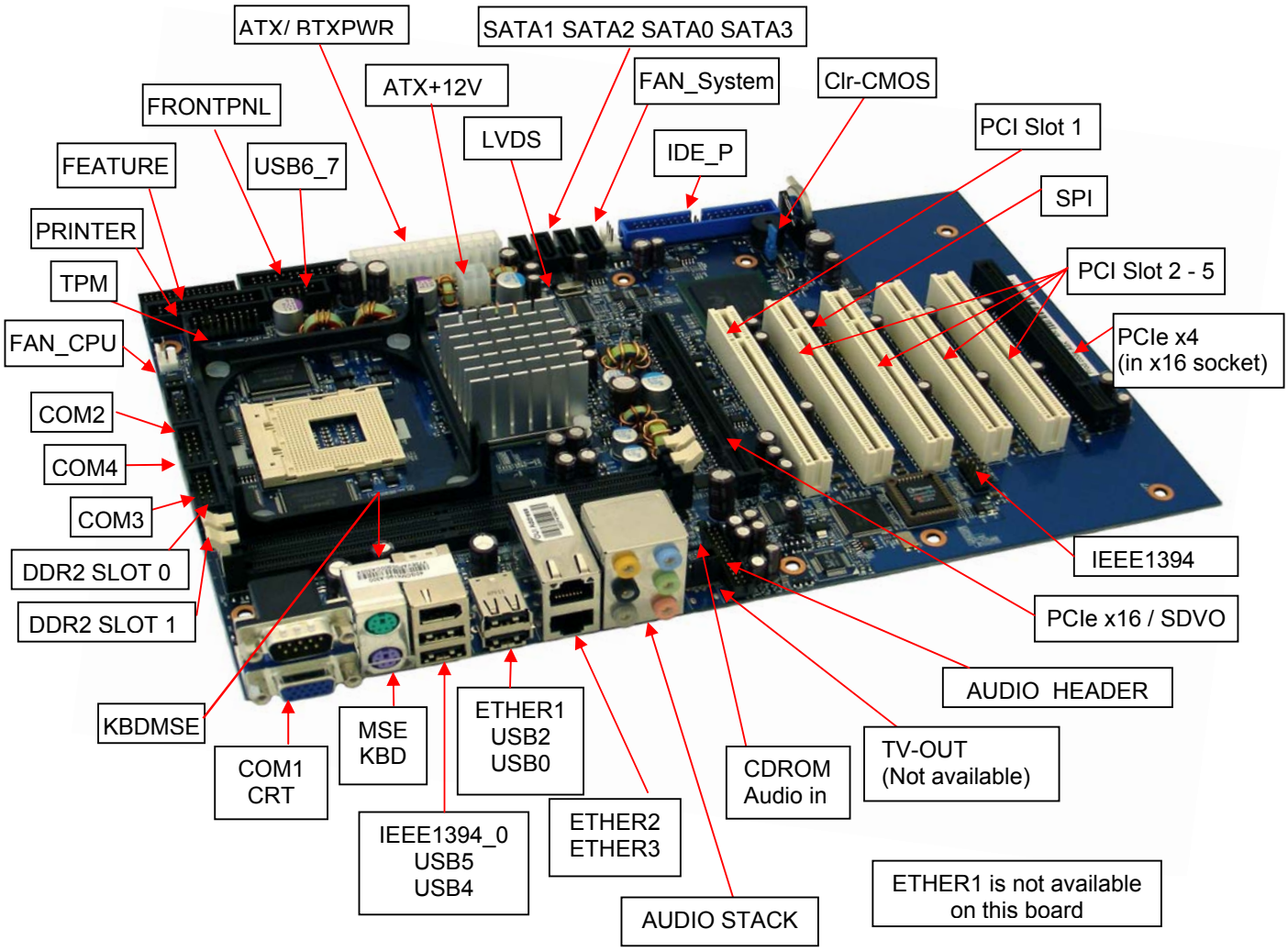
4.1.3 986LCD-M/ATXP



* Support for Mini PCI-Express modules with no components mounted on backside.

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4.1.4 986LCD-M/ATXE



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4.2 Power Connector (ATXPWR)

The 986LCD-M boards are designed to be supplied from a standard ATX or BTX power supply.

ATX/ BTX Power Connector:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	3V3	12	24	GND	PWR	-	-	
			PWR	+12V	11	23	5V	PWR			
			PWR	+12V	10	22	5V	PWR			
	-	-	PWR	SB5V	9	21	5V	PWR	-	-	
	-	-	I	P_OK	8	20	-5V	PWR	-	-	1
	-	-	PWR	GND	7	19	GND	PWR	-	-	
	-	-	PWR	5V	6	18	GND	PWR	-	-	
	-	-	PWR	GND	5	17	GND	PWR	-	-	
	-	-	PWR	5V	4	16	PSON#	OC	-	-	
	-	-	PWR	GND	3	15	GND	PWR	-	-	
	-	-	PWR	3V3	2	14	-12V	PWR	-	-	
	-	-	PWR	3V3	1	13	3V3	PWR	-	-	

Note 1: -5V supply is not used onboard.
Note 2: Use of BTX supply not required for operation, but may be required to drive high-power PCI Express x16 Add cards.

ATX+12V Power Connector:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	GND	1	3	+12V	PWR	-	-	1
1			PWR	GND	2	4	+12V	PWR			1

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of the 986LCD-M boards.

See chapter “Power Consumption” regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification).

Control signal description:

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply with the 986LCD-M boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the 986LCD-M boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

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4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from 5V_STB when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOC	TBD	4K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOC	TBD	4K7	
			-	NC	6 5	KBDCLK	IOC	TBD	4K7	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOC	TBD	4K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 Keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	4K7	
2	KBDDAT	IOC	TBD	4K7	
3	MSCLK	IOC	TBD	4K7	
4	MSDAT	IOC	TBD	4K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

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4.4 Display Connectors

The 986LCD-M board family provides onboard two basic types of interfaces to a display: Analog CRT interface and a digital interface typically used with flat panels. The digital interface to flat panels can be achieved through the onboard LVDS dual channel interface and/or the SDVO port available on the PCI Express connector.

4.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		ANA-GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		ANA-GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	2K2	
						8		ANA-GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		DIG-GND	PWR	-	-	
	-	-	PWR	DIG-GND	5		15	DDCCLK	IO	TBD	2K2	

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.

Signal Description - CRT Connector:

Signal	Description
HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

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4.4.2 TV-Out (Optional)

Optionally the 986LCD-M board include TV-Out connector with support for Component, S-Video and Composite Output interfaces and NTSC/ PAL output format.
The Intel® 945GM chipset include Macrovision support.

IMPORTANT: If the TV-Out option is available then you must make agreement with Macrovision (http://www.macrovision.com/) about lincence fee. Only Macrovision (not Kontron) can determine the actual licence fee which depends on the application.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
						GND				
				TVDACC		TVDACB				
					4 7 3					
					2 6 5 1					
				GND		GND				
				GND		TVDACA				

Signal	Description
TVDACA	TVDAC Channel A output supports: Composite: CVBS signal Component: Chrominance (Pb) analog signal
TVDACB	TVDAC Channel B output supports: S-Video: Luminance analog signal Component: Luminance (Y) analog signal
TVDACC	TVDAC Channel C output supports: S-Video: Chrominance analog signal Component: Chrominance (Pr) analog signal

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4.4.3 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	Pin		Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
4K7Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	4K7Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
Note 1	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	Note 1
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
Note 1	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	Note 1
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Note 1: Support of 24bit OpenLDI/ SPWG panels is not officially supported by Intel®, but is supported by the 986LCD series boards by Kontron. Kontron intends to continue to provide 24bit OpenLDI/ SPWG panel support even if Intel® withdraws this from the chipset, by an external converter module.

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0..B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock
DDC DATA	DDC Channel Data

Note 1) Windows API (version Hwmon_KTAPI ver 4.5 or newer) is available to operate the BKLTCTL signal. Some Inverters has a limited voltage range 0- 2.5V for this signal: If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise to the BKLTCTL signal resulting in making the lvds transmision fail (corrupted picture on the display). By adding 1K Ohm resistor in series with this signal and mounted in the Inverter end of the cable kit the noise is limited and picture is stabil.

Note 2) If the Backlight Enable is required to be active high then make the BIOS Chipset setting: Backlight Signal Inversion = Enabled.

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4.5 PCI-Express Connectors

4.5.1 PCI-Express x16/ SDVO connector

The 986LCD-M boards supports one 16-lane (x16) PCI Express port for external PCI Express based graphics boards or ADD2 devices.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[15] / SDVOB_RED	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[15] / SDVOB_RED#	B15	A15	GND		
		GND	B16	A16	PEG_RXP[15] / SDVO_TVCLKIN		
		SDVO_CTRLCLK	B17	A17	PEG_RXN[15] / SDVO_TVCLKIN#		
		GND	B18	A18	GND		
		PEG_TXP[14] / SDVOB_GREEN	B19	A19	NC		
		PEG_TXN[14] / SDVOB_GREEN#	B20	A20	GND		
		GND	B21	A21	PEG_RXP[14] / SDVOB_INT		
		GND	B22	A22	PEG_RXN[14] / SDVOB_INT#		
		PEG_TXP[13] / SDVOB_BLUE	B23	A23	GND		
		PEG_TXN[13] / SDVOB_BLUE#	B24	A24	GND		
		GND	B25	A25	PEG_RXP[13] / SDVO_FLDSTALL		
		GND	B26	A26	PEG_RXN[13] / SDVO_FLDSTALL#		
		PEG_TXP[12] / SDVOB_CLKP	B27	A27	GND		
		PEG_TXN[12] / SDVOB_CLKN	B28	A28	GND		
		GND	B29	A29	PEG_RXP[12]		
		NC	B30	A30	PEG_RXN[12]		
		SDVO_CTRLDATA	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[11] / SDVOC_RED	B33	A33	NC		
		PEG_TXN[11] / SDVOC_RED#	B34	A34	GND		
		GND	B35	A35	PEG_RXP[11]		
		GND	B36	A36	PEG_RXN[11]		
		PEG_TXP[10] / SDVOC_GREEN	B37	A37	GND		
		PEG_TXN[10] / SDVOC_GREEN#	B38	A38	GND		
		GND	B39	A39	PEG_RXP[10] / SDVOC_INT		
		GND	B40	A40	PEG_RXN[10] / SDVOC_INT#		
		PEG_TXP[9] / SDVOC_BLUE	B41	A41	GND		
		PEG_TXN[9] / SDVOC_BLUE#	B42	A42	GND		
		GND	B43	A43	PEG_RXP[9]		
		GND	B44	A44	PEG_RXN[9]		
		PEG_TXP[8] / SDVOC_CLKN	B45	A45	GND		
		PEG_TXN[8] / SDVOC_CLKP	B46	A46	GND		
		GND	B47	A47	PEG_RXP[8]		
		PRSNT#2	B48	A48	PEG_RXN[8]		
		GND	B49	A49	GND		
		PEG_TXP[7]	B50	A50	NC		
		PEG_TXN[7]	B51	A51	GND		
		GND	B52	A52	PEG_RXP[7]		
		GND	B53	A53	PEG_RXN[7]		
		PEG_TXP[6]	B54	A54	GND		
		PEG_TXN[6]	B55	A55	GND		
		GND	B56	A56	PEG_RXP[6]		
		GND	B57	A57	PEG_RXN[6]		
		PEG_TXP[5]	B58	A58	GND		
		PEG_TXN[5]	B59	A59	GND		

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		GND	B60	A60	PEG_RXP[5]		
		GND	B61	A61	PEG_RXN[5]		
		PEG_TXP[4]	B62	A62	GND		
		PEG_TXN[4]	B63	A63	GND		
		GND	B64	A64	PEG_RXP[4]		
		GND	B65	A65	PEG_RXN[4]		
		PEG_TXP[3]	B66	A66	GND		
		PEG_TXN[3]	B67	A67	GND		
		GND	B68	A68	PEG_RXP[3]		
		GND	B69	A69	PEG_RXN[3]		
		PEG_TXP[2]	B70	A70	GND		
		PEG_TXN[2]	B71	A71	GND		
		GND	B72	A72	PEG_RXP[2]		
		GND	B73	A73	PEG_RXN[2]		
		PEG_TXP[1]	B74	A74	GND		
		PEG_TXN[1]	B75	A75	GND		
		GND	B76	A76	PEG_RXP[1]		
		GND	B77	A77	PEG_RXN[1]		
		PEG_TXP[0]	B78	A78	GND		
		PEG_TXN[0]	B79	A79	GND		
		GND	B80	A80	PEG_RXP[0]		
		NC	B81	A81	PEG_RXN[0]		
		NC	B82	A82	GND		

4.5.2 PCI-Express x4 in a x16 connector

The 986LCD-M/Flex and the 986LCD-M/ATXE boards supports one 4-lane PCI Express (x16) port.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	NC		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x4 CLK		
		PCIE_TXP[1]	B14	A14	PCIE_x4 CLK#		
		PCIE_TXN[1]	B15	A15	GND		
		GND	B16	A16	PCIE_RXP[1]		
		NC	B17	A17	PCIE_RXN[1]		
		GND	B18	A18	GND		
		PCIE_TXP[2]	B19	A19	NC		
		PCIE_TXN[2]	B20	A20	GND		
		GND	B21	A21	PCIE_RXP[2]		
		GND	B22	A22	PCIE_RXN[2]		
		PCIE_TXP[3]	B23	A23	GND		
		PCIE_TXN[3]	B24	A24	GND		
		GND	B25	A25	PCIE_RXP[3]		
		GND	B26	A26	PCIE_RXN[3]		
		PCIE_TXP[4]	B27	A27	GND		
		PCIE_TXN[4]	B28	A28	GND		
		GND	B29	A29	PCIE_RXP[4]		
		NC	B30	A30	PCIE_RXN[4]		
		NC	B31	A31	GND		
		GND	B32	A32	NC		
		NC	B33	A33	NC		
		NC	B34	A34	GND		
		GND	B35	A35	NC		
		GND	B36	A36	NC		
		NC	B37	A37	GND		
		NC	B38	A38	GND		
		GND	B39	A39	NC		

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		GND	B40	A40	NC		
		NC	B41	A41	GND		
		NC	B42	A42	GND		
		GND	B43	A43	NC		
		GND	B44	A44	NC		
		NC	B45	A45	GND		
		NC	B46	A46	GND		
		GND	B47	A47	NC		
		NC	B48	A48	NC		
		GND	B49	A49	GND		
		NC	B50	A50	NC		
		NC	B51	A51	GND		
		GND	B52	A52	NC		
		GND	B53	A53	NC		
		NC	B54	A54	GND		
		NC	B55	A55	GND		
		GND	B56	A56	NC		
		GND	B57	A57	NC		
		NC	B58	A58	GND		
		NC	B59	A59	GND		
		GND	B60	A60	NC		
		GND	B61	A61	NC		
		NC	B62	A62	GND		
		NC	B63	A63	GND		
		GND	B64	A64	NC		
		GND	B65	A65	NC		
		NC	B66	A66	GND		
		NC	B67	A67	GND		
		GND	B68	A68	NC		
		GND	B69	A69	NC		
		NC	B70	A70	GND		
		NC	B71	A71	GND		
		GND	B72	A72	NC		
		GND	B73	A73	NC		
		NC	B74	A74	GND		
		NC	B75	A75	GND		
		GND	B76	A76	NC		
		GND	B77	A77	NC		
		NC	B78	A78	GND		
		NC	B79	A79	GND		
		GND	B80	A80	NC		
		NC	B81	A81	NC		
		NC	B82	A82	GND		

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4.5.3 miniPCI-Express connector

The 986LCD-M/mITX and the 986LCD-M/ATXP supports one miniPCI Express port.

Note	Type	Signal	PIN		Signal	Type	Note
		WAKE#	1	2	+3V3		
		NC	3	4	GND		
		NC	5	6	+1.5V		
		NC	7	8	NC		
		GND	9	10	NC		
		PCIE_mini CLK#	11	12	NC		
		PCIE_mini CLK	13	14	NC		
		GND	15	16	NC		
		NC	17	18	GND		
		NC	19	20	W_Disable		
		GND	21	22	RST#		
		PCIE_RXN	23	24	GND		
		PCIE_RXP	25	26	GND		
		GND	27	28	+1.5V		
		GND	29	30	SMB_CLK		
		PCIE_TXN	31	32	SMB_DATA		
		PCIE_TXP	33	34	GND		
		GND	35	36	NC		
		NC	37	38	NC		
		NC	39	40	GND		
		NC	41	42	NC		
		NC	43	44	NC		
		NC	45	46	NC		
		NC	47	48	+1.5V		
		NC	49	50	GND		
		NC	51	52	+3V3		

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4.6 Parallel ATA harddisk interface

One parallel primary ATA harddisk controller is available on the board.
Standard 3½" harddisks or CD-ROM drives may be attached to the primary controller board by means of the 40 pin IDC connectors, IDE_P.
The primary controller is shared between the IDE_P connector and the backside Compact Flash connector (986LCD-M/mITX only). In case CF is utilized, only one IDE device is supported on the IDE_P connector.
The harddisk controllers support Bus master IDE, ultra DMA 33/66/100 MHz and standard operation modes.

The signals used for the harddisk interface are the following:

Signal	Description
PDA2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCS1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
D15..8	High part of data bus.
D7..0	Low part of data bus.
IOR#	I/O Read.
IOW#	I/O Write.
IORDY#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESET#	Reset signal to the hard disk. The signal is similar to RSTDRV in the PC-AT bus.
HDIRQ	Interrupt line from hard disk. Routed by the SiS630 chipset to PC-AT bus interrupt.
CBLID	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQ	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACK#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACT#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].
The pinout of the connectors are defined in the following sections.

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4.6.1 IDE Hard Disk Connector (IDE_P)

This connector can be used for connection of two primary IDE drives. If Compact Flash connector (986LCD-M/mITX only) is utilized, only one IDE device is supported.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESET#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQ	21	22	GND	PWR	-	-	
	-	TBD	O	IOW#	23	24	GND	PWR	-	-	
	-	TBD	O	IOR#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDY	27	28	GND	PWR	-	-	
	-	-	O	DDACK#	29	30	GND	PWR	-	-	
	8K2	-	I	HDIRQ	31	32	NC	-	-	-	
	-	TBD	O	PDA1	33	34	CBLID#	I	-		
	-	TBD	O	PDA0	35	36	PDA2	O	TBD	-	
	-	TBD	O	HDCS1#	37	38	HDCS3#	O	TBD	-	
	-	-	I	HDACT#	39	40	GND	PWR	-	-	

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4.6.2 CF Connector (CF)

This connector is mounted on the backside of the 986LCD-M/mITX only. If a Compact Flash Disk is used, only one IDE device is supported on the IDE_P connector. The CF socket support DMA/UDMA CF modules.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	TBD	IO	DA3	2	1	GND	PWR	-	-	1
	-	TBD	IO	DA5	4	3	DA4	IO	TBD	-	
	-	TBD	IO	DA7	6	5	DA6	IO	TBD	-	
	-	-	PWR	GND	8	7	HDCS1#	O	TBD	-	
	-	-	PWR	GND	10	9	GND	PWR	-	-	
	-	-	PWR	GND	12	11	GND	PWR	-	-	
	-	-	PWR	GND	14	13	5V	PWR	-	-	
	-	-	PWR	GND	16	15	GND	PWR	-	-	
	-	-	O	PDA2	18	17	GND	PWR	-	-	
	-	-	O	PDA0	20	19	PDA1	O	-	-	
	-	TBD	IO	DA1	22	21	DA0	IO	TBD	-	
	-	-	-	NC	24	23	DA2	IO	TBD	-	
	-	-	-	NC	26	25	NC	-	-	-	
	-	TBD	IO	DA12	28	27	DA11	IO	TBD	-	
	-	TBD	IO	DA14	30	29	DA13	IO	TBD	-	
	-	TBD	O	HDCS3#	32	31	DA15	IO	TBD	-	
	-	TBD	O	IOR#	34	33	NC	I			
	-	-	PWR	5V	36	35	IOW#	O	TBD	-	
	-	-	PWR	5V	38	37	IRQ	I	-	8K2	
				NC	40	39	GND	PWR	-	-	
	4K7	-	I	IORDYB#	42	41	RESET#			-	
	-	-	O	DDACK#	44	43	DDRQ	I	-	-	
	-	-	I	CBLID#	46	45	HDACT#				
	-	TBD	IO	DA9	48	47	DA8	IO	TBD	-	
1	-	-	PWR	GND	50	49	DA10	IO	TBD	-	2

Note 1: Pin is longer than average length of the other pins.
Note 2: Pin is shorter than average length of the other pins.

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4.7 Serial ATA harddisk interface

The 986LCD-M boards have an intergrated SATA Host controller that supports independent DMA operation on four ports and data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0, 1, 5 and 10 (Linux O/S only support for RAID 0 and 1).

4.7.1 SATA Hard Disk Connector (SATA0, SATA1, SATA2, SATA3)

SATA:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

"*" specifies 0, 1, 2, and 3 depending on SATA port.
All of the above signals are compliant to [4].

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4.8 Printer Port Connector (PRINTER).

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3	4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5	6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7	8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9	10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11	12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13	14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15	16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17	18	GND	PWR	-	-	
	2K2	-	I	ACK#	19	20	GND	PWR	-	-	
	2K2	-	I	BUSY	21	22	GND	PWR	-	-	
	2K2	-	I	PE	23	24	GND	PWR	-	-	
	2K2	-	I	SLCT	25	26	GND	PWR	-	-	

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus. The bus are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Input indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

Connecting the cable kit 821026 “Cable LPT 2mm 250mm” to the mITX or the 821031 “Cable LPT 2.54mm 250mm” implements the standard DB-25 interface:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1	14	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	2	15	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	3	16	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	4	17	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	5	18	GND	PWR	-	-	
	2K2	24/24	IO	PD4	6	19	GND	PWR	-	-	
	2K2	24/24	IO	PD5	7	20	GND	PWR	-	-	
	2K2	24/24	IO	PD6	8	21	GND	PWR	-	-	
	2K2	24/24	IO	PD7	9	22	GND	PWR	-	-	
	2K2	-	I	ACK#	10	23	GND	PWR	-	-	
	2K2	-	I	BUSY	11	24	GND	PWR	-	-	
	2K2	-	I	PE	12	25	GND	PWR	-	-	
	2K2	-	I	SLCT	13						

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4.9 Serial Ports

Four RS232 serial ports are available on the 986LCD-M boards

The typical interpretation of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the device. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the device that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that data set is ready to establish a communication link.
RTS	Request To Send, indicates to the device that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.9.1 Com1 (Port1) DB9 Connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5	9	RI	I	-	/5K	
	-		AO*	DTR	4	8	CTS	AI*	-	/5K	
	-		AO*	TxD	3	7	RTS	AO*		-	
	/5K	-	AI*	RxD	2	6	DSR	AI*	-	/5K	
	/5K	-	AI*	DCD	1						

* = +/-12V signals.

4.9.2 Com2, Com3 & Com4 Pin Header Connectors.

The pinout of Serial ports Com2, Com3 and Com4 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	AI*	DCD	1	2	DSR	AI*	-		
		-	AI*	RxD	3	4	RTS	AO*		-	
	-		AO*	TxD	5	6	CTS	AI*	-		
	-		AO*	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

* = +/-12V signals.

Note 1: 5V supply is shared with supply pins in Com2/Com3/Com4 headers. The common fuse is 1.1A.

If the DB9 adapter (ribbon cable) is used, the DB9 pinout will be identical to the pinout of Serial Com1.

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4.10 Ethernet connectors.

The 986LCD-M/mITX and 986LCD-M/ATXP boards supports 3 channels of 10/100/1000Mb Ethernet RTL8111B LAN controllers.
The 986LCD-M/Flex and 986LCD-M/ATXE boards supports 2 channels of 10/100/1000Mb Ethernet RTL8111B LAN controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[0]-	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]-	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDI[2]-	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDI[3]-	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

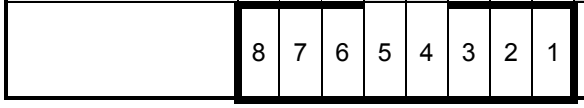
Note: MDI = Media Dependent Interface.

4.10.1 Ethernet connector 1 (ETHER1)

Ethernet connector 1 is mounted together with USB Ports 0 and 2.
(Not available on 986LCD-M/Flex and 986LCD-M/ATXE).

The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2-				
MDI1-				
MDI2+				
MDI3+				
MDI3-				



On top of Ethernet1 connector there is a Green LED (to the left) turning on when a 100MHz connection is made and it is flashing when 100MHz traffic is ongoing. The Yellow LED (to the right) turns on when a 1GHz connection is made and it is flashing when traffic is ongoing.

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4.10.2 Ethernet connector 2/3 (ETHER2/3)

The two Ethernet channels in ETHER2/3 are supported by two discrete Ethernet controllers (RTL8111B) connected to the onboard PCI bus.

The pinout of the RJ45's connector are as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2-				
MDI1-				
MDI2+				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			
	1 2 3 4 5 6 7 8			
MDI0+				
MDI0-				
MDI1+				
MDI2-				
MDI1-				
MDI2+				
MDI3+				
MDI3-				

Note: The connector has two LEDs which indicates connection and traffic status. Green/Yellow means 100MHz/1GHz and flasing when traffic is ongoing. The left LED is status for the ETHER3 (buttom port) and the right LED is for ETHER2. More than one type of connector is approved for this application. Please notice that it is possible that the shape of the LED might vary depending on actual type of connector.

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4.11 Firewire/ IEEE-1394 connectors.

The 986LCD-M boards supports two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200M bits/s, and 400M bits/s.

4.11.1 IEEE1394 Connector (IEEE1394_0)

The pinout of the Firewire / IEEE1394 connector IEEE1394_0 (stacked together with USB Ports 4 and 5) is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN
				TPA0+	
				TPB0+	
				GND	
					10 12 14
					9 11 13
1				+12V	
				TPB0-	
				TPA0-	

Note 1: The 12V supply for the IEEE1394_0 devices is on-board fused with a 1.5A reset-able fuse.

Signal	Description
TPA0+ TPA0–	Differential signal pair A
TPB0+ TPB0–	Differential signal pair B
+12V	+12V supply

4.11.2 IEEE1394 Connector (IEEE1394_1)

The IEEE1394_1 is not mounted on the 986LCD-M/Flex.

The pinout of the Firewire / IEEE1394 connector IEEE1394_1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				TPA1+	1	2	TPA1-				
				GND	3	4	GND				
				TPB1+	5	6	TPB1-				
1				+12V	7	8	+12V				1
				KEY	9	10	GND				

Note 1: The 12V supply for the IEEE1394_1 devices is on-board fused with a 1.5A reset-able fuse.

Signal	Description
TPA1+ TPA1–	Differential signal pair A
TPB1+ TPB1–	Differential signal pair B
+12V	+12V supply

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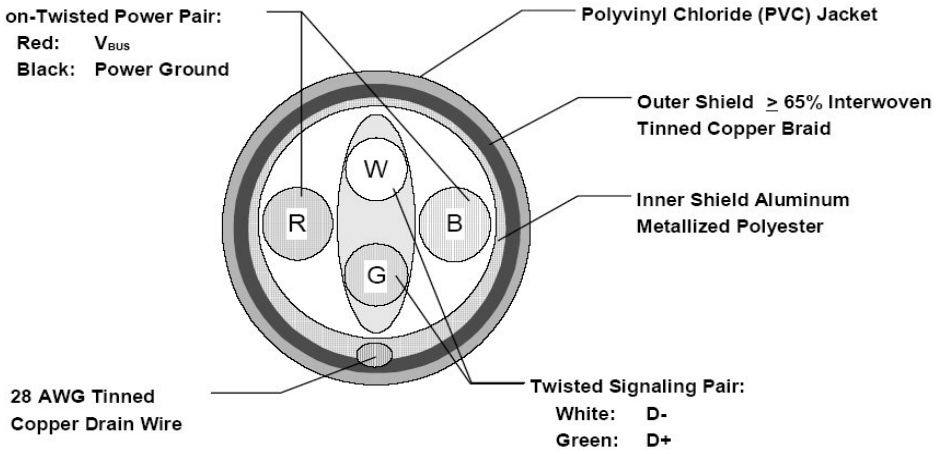
4.12 USB Connector (USB)

The 986LCD-M boards contains an Enhanced Host Controller Interface (EHCI) host controller that supports USB 2.0 allowing data transfers up to 480Mb/s. The 986LCD-M boards also contains four Universal Host Controller Interface (UHCI Revision 1.1) controllers that support USB full-speed and low-speed signaling. The 986LCD-M boards supports a total of eight USB 2.0 ports. All eight ports are high-speed, full-speed, and low-speed capable and USB Legacy mode is supported.

Over-current detection on all eight USB ports is supported.

USB Port 0 and 2 are supplied on the combined ETHER1, USB0, USB2 connector. USB Ports 1 and 3 are supplied on the FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.
USB Port 4 and 5 are supplied on the combined IEEE1394_0, USB4, USB5 connector.
USB Port 6 and 7 are supplied on the internal USB6, USB7 pinrow.

Note: It is recommended to use only High-/Full-Speed USB cable, specified in USB2.0 standard:



4.12.1 USB Connector 0/2 (USB0/2)

USB Ports 0 and 2 are mounted together with ETHER1 ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB2+ USB2-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

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4.12.2 USB Connector 4/5 (USB4/5)

USB Ports 4 and 5 are mounted together with IEEE1394_0 port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.12.3 USB Connector 6/7 (USB6_7)

The pinout of the USB connector USB6_7 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1	2	5V/SB5V	PWR	-		1
		-	IO	USB6-	3	4	USB7-	IO		-	
	-		IO	USB6+	5	6	USB7+	IO	-		
	-		PWR	GND	7	8	GND	PWR	-		
	-	-		KEY	9	10	NC		-	-	

Signal	Description
USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

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4.13 Audio Connector

4.13.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector. Below is shown audio stack configuration when configured for 8-channel audio.

Note	Type	Signal			Signal	Type	Note
		CEN-OUT	TIP	TIP	LINE1-IN-L	IA	1
		LFE-OUT	RING	RING	LINE1-IN-R	IA	1
		GND	SLEEVE	SLEEVE	GND	PWR	
		REAR-OUT-L	TIP	TIP	FRONT-OUT-L	OA	
		REAR-OUT-R	RING	RING	FRONT-OUT-R	OA	
		GND	SLEEVE	SLEEVE	GND	PWR	
		SIDE-OUT-L	TIP	TIP	MIC1-L	IA	1
		SIDE-OUT-R	RING	RING	MIC1-R	IA	1
		GND	SLEEVE	SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.

Signal descriptions

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	

Audio 2, 4, 6, or 8-channel configuration

Port	2-channel	4-channel	6-channel	8-channel
Light Blue	Line in	Line in	Line in	Line in
Lime	Line out	Front speaker out	Front speaker out	Front speaker out
Pink	Mic in	Mic in	Mic in	Mic in
Gray	-	-	-	Side speaker out
Black	-	Rear speaker out	Rear speaker out	Rear speaker out
Yellow Orange	-	-	Center/ Subwoofer	Center/ Subwoofer

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4.13.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

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4.13.3 AUDIO Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
				LFE-OUT	1	2	CEN-OUT				
				AAGND	3	4	AAGND				
				FRONT-OUT-L	5	6	FRONT-OUT-R				
				AAGND	7	8	AAGND				
				REAR-OUT-L	9	10	REAR-OUT-R				
				SIDE-OUT-L	11	12	SIDE-OUT-R				
				AAGND	13	14	AAGND				
				MIC1-L	15	16	MIC1-R				
				AAGND	17	18	AAGND				
				LINE1-IN-L	19	20	LINE1-IN-R				
				NC	21	22	AAGND				
	-	-	PWR	GND	23	24	SPDIF-IN				
				SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

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4.14 Fan connectors , FAN_CPU and FAN_SYS.

The **FAN_CPU** is used for connection of the active cooler for the CPU.

The **FAN_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.

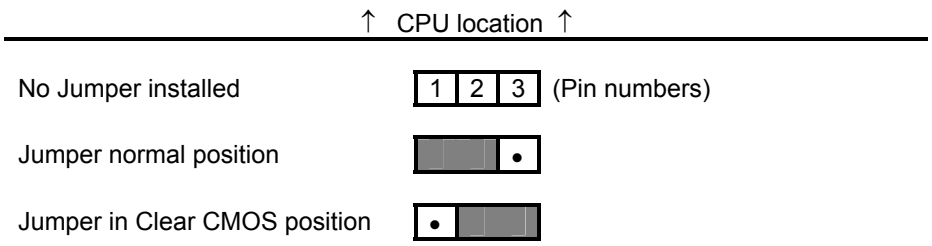
PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	SENSE	PWR	-	4K7	
2	12V	PWR	-	-	
3	GND	PWR	-	-	

Signal description:

Signal	Description
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 800 mA can be supplied from this pin.
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.

4.15 The Clear CMOS Jumper, Clr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.



To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

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4.16 TPM connector (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	LPC IRQ#				

4.17 SPI connector (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				SPI_CLK	1	2	SB3V3				
	10K/			SPI_CS	3	4	BOOT0				
	10K/			SPI_ARB	5	6	BOOT1				
	10K/			SPI_MOSI	7	8	NC				
	10K/			SPI_MISO	9	10	GND				

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4.18 Front Panel connector (FRONTPNL).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
				USB13_5V	1	2	USB13_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	NC	9	10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	LINE2-IN-R	-	-	-	
				AGND	21	22	AGND				
1				MIC2-L	23	24	MIC2-R				1

Note 1: Unsupported inputs, leave these inputs unconnected.

Signal	Description
USB13_5V	+5V supply for the USB devices on USB Port 1 and 3 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connectorfladkabel or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. Pull low to reset the board.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R are unsupported. Leave these terminals unconnected.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

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4.19 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	243K/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I			
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
3	2K7/	/12mA	IOT	GPIO0	11	12	GPIO1	IOT	/12mA	2K7/	3
3	2K7/	/12mA	IOT	GPIO2	13	14	GPIO3	IOT	/12mA	2K7/	3
4	2K7/	/12mA	IOT	GPIO4	15	16	GPIO5	IOT	/12mA	2K7/	4
4	2K7/	/12mA	IOT	GPIO6	17	18	GPIO7	IOT	/12mA	2K7/	4
	-	-	PWR	GND	19	20	FAN3OUT				
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Note 1: Pull-up to +5V. Note 2: Pull-up to RTC-Voltage. Note 3: Pull-up to +5VDual (+5V or +5VSB). Note 4: Pull-up to +5VSB.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
SB3V3	Standby 3.3V. Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND (etc. pin 10). The external battery is protected against charging and can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KONTRON API (Application Programming Interface) available for Win98, WinXP and Win2000.
FAN3OUT	FAN 3 speed control OUTput. This analogue voltage output signal can be used to control the Fan's speed. The output has 16 values in the range from 0 – 5V. For more information please look into the datasheet for the Winbond I/O controller W83627.
FAN3IN	FAN3 Input. 0V to +5V amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin23 (Temp3-In). Further a resistor 30K/1% shall be connected between pin 23 and pin 24 (Vref). Precision +/- 7ºC.
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

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4.20 PCI Slot

4.20.1 PCI Slot Connector

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

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4.20.2 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(continues)

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ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

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4.20.3 PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
986LCD-M/mITX	1	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
986LCD-M/FLEX	1	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
	2	AD18	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
986LCD-M/ATXP	1	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
	2	AD18	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	3	AD19	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F
	4	AD20	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G
	5	AD21	INT_PIRQ#D	INT_PIRQ#C	INT_PIRQ#B	INT_PIRQ#A
	6	AD22	INT_PIRQ#C	INT_PIRQ#B	INT_PIRQ#A	INT_PIRQ#D
986LCD-M/ATXE	1	AD17	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
	2	AD18	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	3	AD19	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F
	4	AD20	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G
	5	AD21	INT_PIRQ#D	INT_PIRQ#C	INT_PIRQ#B	INT_PIRQ#A

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E. 820982 PCI Riser shall be plugged into Slot #1.

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5. Onboard Connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_SYS, FAN_CPU	Molex	22-23-2031	AMP	1375820-3
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA0-3	Molex	67491-0020	Molex	67489-8005
			Kontron	KT 821035 (cable kit)
ATXPWR	Molex	44206-0002	Molex	39-01-2205
			Molex	39-01-2245
ATX+12V	Foxconn	HM2502E	Molex	39-01-2045
COM2	Foxconn	HL20051	Molex	90635-1103
COM3			Kontron	KT 821016 (cable kit)
COM4			Kontron	KT 821017 (cable kit)
IEEE1394_0 IEEE1394_1	Foxconn	HC11051-P9	Kontron	KT 821040 (cable kit)
USB6_7	Foxconn	HC11051-P9	Kontron	KT 821401 (cable kit)
PRINTER for	Foxconn	HS55137	Molex	51110-2651
mITX			Kontron	KT 821026 (cable kit)
PRINTER for	Foxconn	HL2213F	Molex	90635-1263
Flex/ATXP/ATXE			Kontron	KT 821031 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
FRONTPNL	Foxconn	HL20121	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)
IDE_P	Foxconn	HL20201-UD2	Kontron	KT 821018 (cable kit)
			Kontron	KT 821013 (cable kit)
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1
			Kontron	KT 821515 (cable kit)
			Kontron	KT 821155 (cable kit)

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6. System Ressources

6.1 Memory map

Address range (hex)		Size	Description
00000000	0009FFFF	655360	System board
000A0000	000BFFFF	131072	Mobile Intel 945GM Express Chipset Family
000A0000	000BFFFF	131072	PCI bus
000C0000	000CFFFF	65536	System board
000D0000	000DFFFF	65536	PCI bus
000E0000	000FFFFF	131072	System board
00100000	3F7FFFFF	1064304640	System board
3F800000	FFFFFFFF	3229614080	PCI bus
D0000000	DFFFFFFF	268435456	Mobile Intel 945GM Express Chipset Family
E0000000	E3FFFFFF	67108864	Motherboards resources
FEC00000	FEC00FFF	4096	Motherboards resources
FED13000	FED19FFF	28672	System board
FED1C000	FED1FFFF	16384	Motherboards resources
FED20000	FED8FFFF	458752	Motherboards resources
FEE00000	FEE00FFF	4096	Motherboards resources
FF400000	FF4FFFFF	1048576	Intel 82801G PCI Express Root Port
FF4FF000	FF4FFFFF	4096	Realtek RTL8111 PCI-E Gigabit Ethernet NIC
FF500000	FF5FFFFF	1048576	Intel 82801G PCI Express Root Port
FF5FF000	FF5FFFFF	4096	Realtek RTL8111 PCI-E Gigabit Ethernet NIC
FF600000	FF6FFFFF	1048576	Intel 82801G PCI Express Root Port
FF6FF000	FF6FFFFF	4096	Realtek RTL8111 PCI-E Gigabit Ethernet NIC
FF7C8000	FF7CBFFF	4096	Texas Inst. OHCI Compliant IEEE 1394 Host Controller
FF7CF800	FF7CFFFF	2048	Texas Inst. OHCI Compliant IEEE 1394 Host Controller
FF980000	FF9FFFFF	524288	Mobile Intel 945GM Express Chipset Family
FFA37800	FFA37BFF	1024	Intel 82801GR/GH SATA RAID Controller
FFA37C00	FFA37FFF	1024	Intel 82801G USB2 Enhanced Host Controller
FFA38000	FFA3BFFF	16384	Microsoft UAA Bus Driver for High Definition Audio
FFA40000	FFA7FFFF	262144	Mobile Intel 945GM Express Chipset Family
FFA80000	FFAFFFFF	524288	Mobile Intel 945GM Express Chipset Family
FFB00000	FFBFFFFF	1048576	Intel 82802 Firmware Hub Device
FFC00000	FFEFFFFF	3145728	Motherboard resources
FFF00000	FFFFFFFF	1048576	Intel 82802 Firmware Hub Device

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6.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
0	0	0	8086h	27A0h		ICH7	Host bridge
0	2	0	8086h	27A2h		945GME	VGA controller
0	2	1	8086h	27A6h		945GME	Display controller
0	27	0	8086h	27D8h		ICH7	
0	28	0	8086h	27D0h		ICH7	Pci to Pci bridge
0	28	1	8086h	27D2h		ICH7	Pci to Pci bridge
0	28	2	8086h	27D4h		ICH7	Pci to Pci bridge
0	29	0	8086h	27C8h		ICH7	USB
0	29	1	8086h	27C9h		ICH7	USB
0	29	2	8086h	27CAh		ICH7	USB
0	29	3	8086h	27CBh		ICH7	USB
0	29	7	8086h	27CCh		ICH7	USB
0	30	0	8086h	244Eh		ICH7	Pci to Pci bridge
0	31	0	8086h	27B8h		ICH7	ISA Bridge
0	31	1	8086h	27DFh		ICH7	IDE Controller
0	31	2	8086h	27C3/27C0		ICH7	RAID/IDE Controller
0	31	3	8086h	27DAh		ICH7	SMBus
1	0	0	10ECh	8168h		RTL8111	Ethernet
2	0	0	10ECh	8168h		RTL8111	Ethernet
3	0	0	10ECh	8168h		RTL8111	Ethernet
4	0	0	104Ch	8023h	AD16	TSB43AB22	FireWire
4	1	0	-	-	AD17	-	PCI slot #1
*	-	-	-	-	-	-	PCI-E slot #1
*	-	-	-	-	-	-	Mini PCI-E slot #1

When a PCI-E or Mini PCI-E card is used it could change the BUS number on other PCI-E and PCI devices like RTL8111 and FireWire.
Note: All PCI slots for the 986LCD-M boards supports PCI BUS Mastering.

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6.3 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Serial Port C	May be used by onboard Serial Port D	May be used by onboard FireWire controller	May be used by onboard Parallel Port	May be used by onboard Floppy disk Controller	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used by primary harddisk controller	May be used by secondary harddisk controller	May be used for SATA RAID controller	May be used for onboard Sound System	May be used for PCI Express Root Port	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard Ethernet controller 3	May be used by onboard VGA Controller	May be used by onboard SMBus Controller	Available on PCI slots as IRQA-IRQD depending on selections in the BIOS	Notes
NMI	•																										
IRQ0		•																									
IRQ1			•																								
IRQ2				•																							
IRQ3						•																				•	1, 2
IRQ4					•																					•	1, 2
IRQ5																										•	1, 2
IRQ6																									•	•	1, 2
IRQ7										•																•	1, 2
IRQ8												•															
IRQ9																										•	1, 2
IRQ10								•																		•	1, 2
IRQ11							•																			•	1, 2
IRQ12													•													•	1
IRQ13														•													
IRQ14															•											•	1
IRQ15																•										•	1
IRQ16									•									•	•	•	•			•			3
IRQ17																			•			•					3
IRQ18																			•	•			•				3
IRQ19																	•			•							3
IRQ20																											3
IRQ21																											3
IRQ22																											3
IRQ23																				•							3
IRQ24																											3
IRQ25																											3
IRQ26																											3

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ16 to IRQ26 are APIC interrupts

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6.4 I/O Map

Address (hex)	Size	Description
0020- 0021	1	Programmable interrupt controller
0040- 0043	4	System Timer
0060- 0060	1	Standard keyboard
0061- 0061	1	System speaker
0064- 0064	1	Standard keyboard
0070- 0071	2	System CMOS/Real time clock
0170- 01F7	8	Secondary Parallel ATA IDE Channel
01F0- 01F7	8	Primary Parallel ATA IDE Channel
02E8- 02EF	8	Comport 4
02F8- 02FF	8	Comport 2 / IRDA
0376- 0376	1	Secondary IDE Channel
0378- 037F	8	Printer Port
03B0- 03BB	12	945GM VGA Controller
03C0- 03DF	32	945GM VGA Controller
03E8- 03EF	8	Comport 3
03F6- 03F6	1	Primary IDE Channel
03F8- 03FF	8	Comport 1
0400- 041F	32	SMBus Controller
A000- AFFF	4096	PCI Express Root Port
A800- A8FF	256	RTL8111 PCI-E Gigabit Ethernet NIC
B000- BFFF	4096	PCI Express Root Port
B800- B8FF	256	RTL8111 PCI-E Gigabit Ethernet NIC
C000- CFFF	4096	PCI Express Root Port
C800- C8FF	256	RTL8111 PCI-E Gigabit Ethernet NIC
D800- D81F	32	Intel 82801G ICH7 USB Universal Host Controller
D880- D89F	32	Intel 82801G ICH7 USB Universal Host Controller
DC00- DC1F	32	Intel 82801G ICH7 USB Universal Host Controller
E000- E01F	32	Intel 82801G ICH7 USB Universal Host Controller
E080- E08F	16	Intel 82801GR/GH Serial ATA Storage Controller
E400- E403	4	Intel 82801GR/GH Serial ATA Storage Controller
E480- E487	8	Intel 82801GR/GH Serial ATA Storage Controller
E800- E803	4	Intel 82801GR/GH Serial ATA Storage Controller
E880- E887	8	Intel 82801GR/GH Serial ATA Storage Controller
EC00- EC07	8	945GM VGA Controller
FFA0- FFAF	16	Intel 82801G ICH7 Ultra ATA Storage Controllers

Notes: This is the IO map after a standard Windows XP SP2 installation

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6.5 DMA Channel Usage

DMA Channel Number	Data Width	System Ressources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

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7. Overview of BIOS features

This Manual section details specific BIOS features for the 986LCD-M boards.
The 986LCD-M boards are based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

7.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

The 886LCD-M Boards supports reading certain MIF specific details by the Windows API. Refer to the API section in this manual for details.

7.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

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8. BIOS Configuration / Setup

8.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the 986LCD-M board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar look like this:

```
                              BIOS SETUP UTILITY
      Main     Advanced     PCIPnP     Boot     Security     Chipset     Exit
```

The available keys for the Menu screens are as:

Function Key	Description
<←> or <→>	Select Screen
<↑> or <↓>	Select Item
<+> or <->	Change Field
<Tab>	Select Field
<F1>	General Help
<F10>	Save and Exit
<Esc>	Exits the Menu

Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in bold, but please notice that when Failsafe Defaults are loaded a few of the options, marked with "*", are now the default option.

8.2 Main Menu

```
                              BIOS SETUP UTILITY
      Main     Advanced     PCIPnP     Boot     Security     Chipset     Exit
  System Overview                                          Use [ENTER], [TAB] or
                                                           [SHIFT-TAB] to select
  AMIBIOS                                                  a field.
  ID        : 986LCD27
  Build Date: 02/05/08                                     Use [+] or [-] to
  PCB ID    : 01                                           configure system Time.
  Serial #  : 00426007
  Part   #  : 67110000

  Processor
  Type      : Genuine Intel(R) CPU T2500 @
  Speed     : 2000MHz                                      <-   Select Screen
  Count     : 1                                            ||   Select Item
                                                           +-   Change Field
  System Memory                                            Tab  Select Field
  Size      : 504MB                                        F1   General Help
                                                           F10  Save and Exit
  System Time                    [10:18:15]                ESC  Exit
  System Date                    [Tue 05/31/2007]
          V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.
```

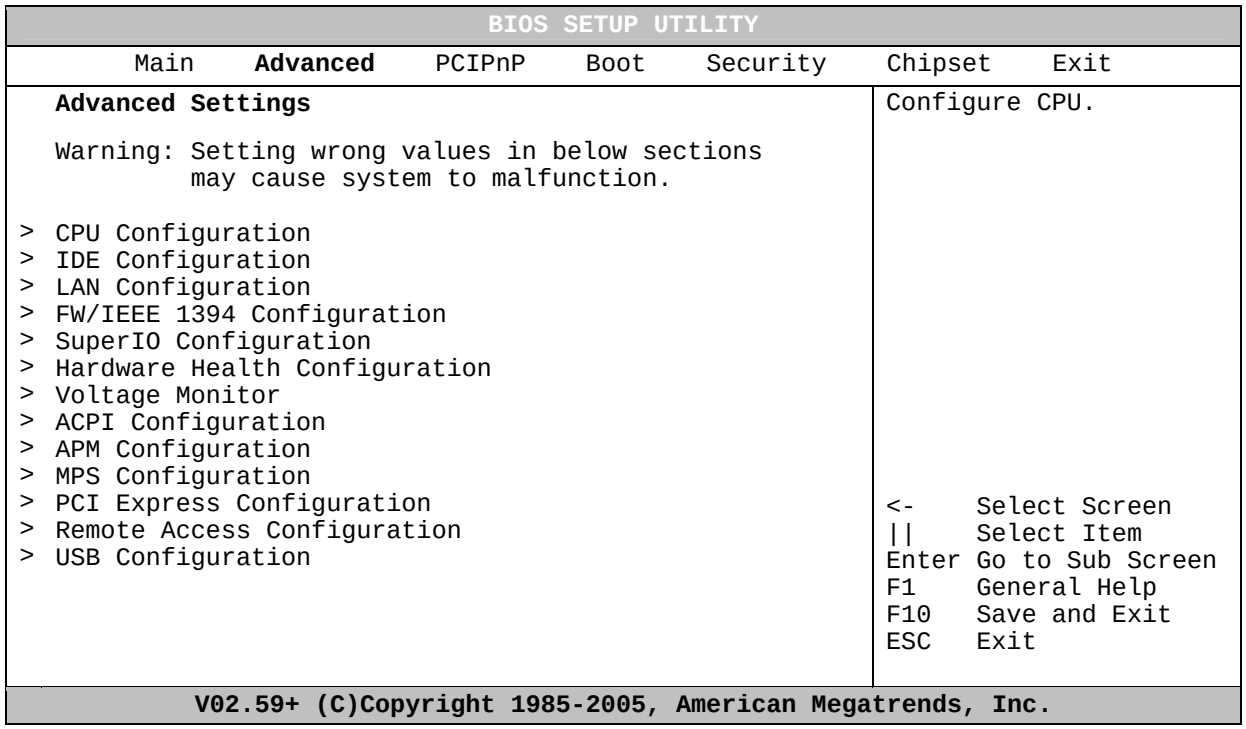
Main Menu Selections

You can make the following selections. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.

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8.3 Advanced Menu



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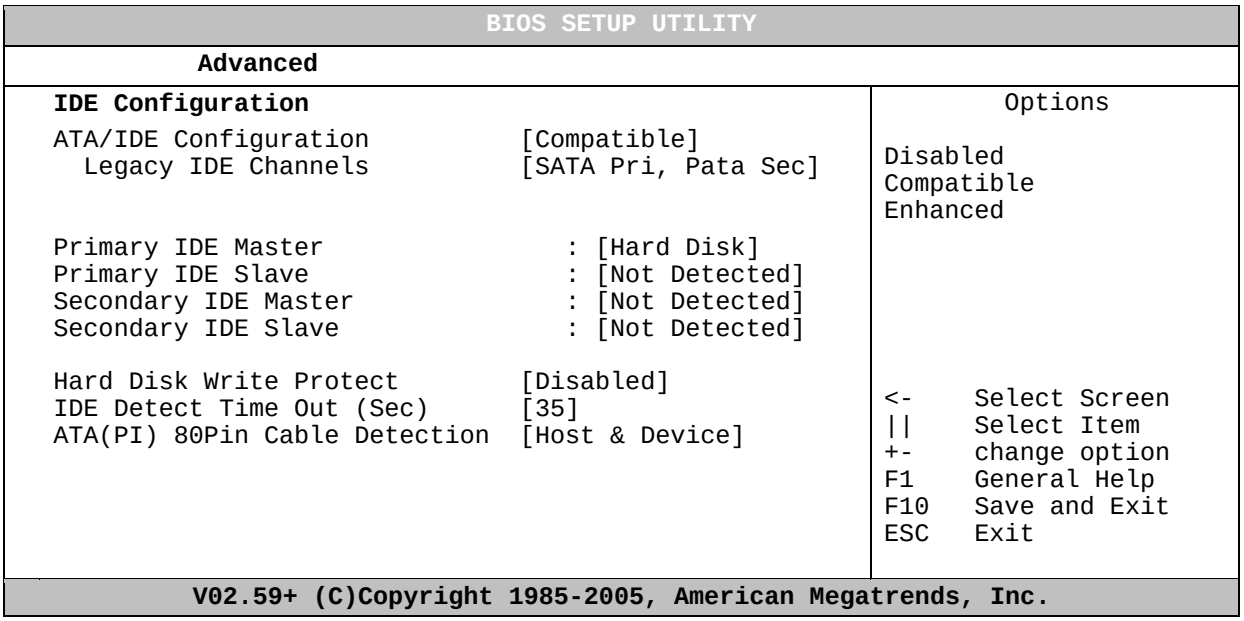
8.3.1 Advanced settings – CPU Configuration

```
                        BIOS SETUP UTILITY
                              Advanced
  Configure advanced CPU settings                  | Maximum: CPU Speed is
  Module Version –13.04                            | set to maximum.
                                                   | Minimum: CPU Speed is
  Manufacturer: Intel                              | set to minimum.
  Brand String: Genuine Intel(R) CPU        T2500  | Automatic: CPU speed
  Frequency   : 2.00GMHz                           | controlled by
  FSB Speed   : 667MHz                             | Operating system.
                                                   | Disabled: Default CPU
  Cache L1    : 64 KB                              | speed.
  Cache L2    : 2048 KB
  Execute Disable Bit             [Enabled]        | <-    Select Screen
  Vanderpool Technology:          [Enabled]        | ||    Select Item
  Intel(R) SpeedStep(tm) tech.    [Automatic]      | +-    Change Option
                                                   | F1    General Help
                                                   | F10   Save and Exit
                                                   | ESC   Exit
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```

Feature	Options	Description
Execute Disabled Bit	**Enabled** Disabled	When disabled, force the XD feature flag to always return 0.
Vanderpool Technology:	**Enabled** Disabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. Need a full reset to change its state.
Intel™ SpeedStep™ tech.	Maximum Speed Minimum Speed **Automatic** Disabled *	Select the operation mode of the CPU. To ensure full performance of the CPU, use the Maximum Speed setting. When Disabled (Failsafe Default) the CPU speed will be same as Minimum Speed. (In order to verify the effect of the setting a reboot must be carried out).

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8.3.2 Advanced settings – IDE Configuration



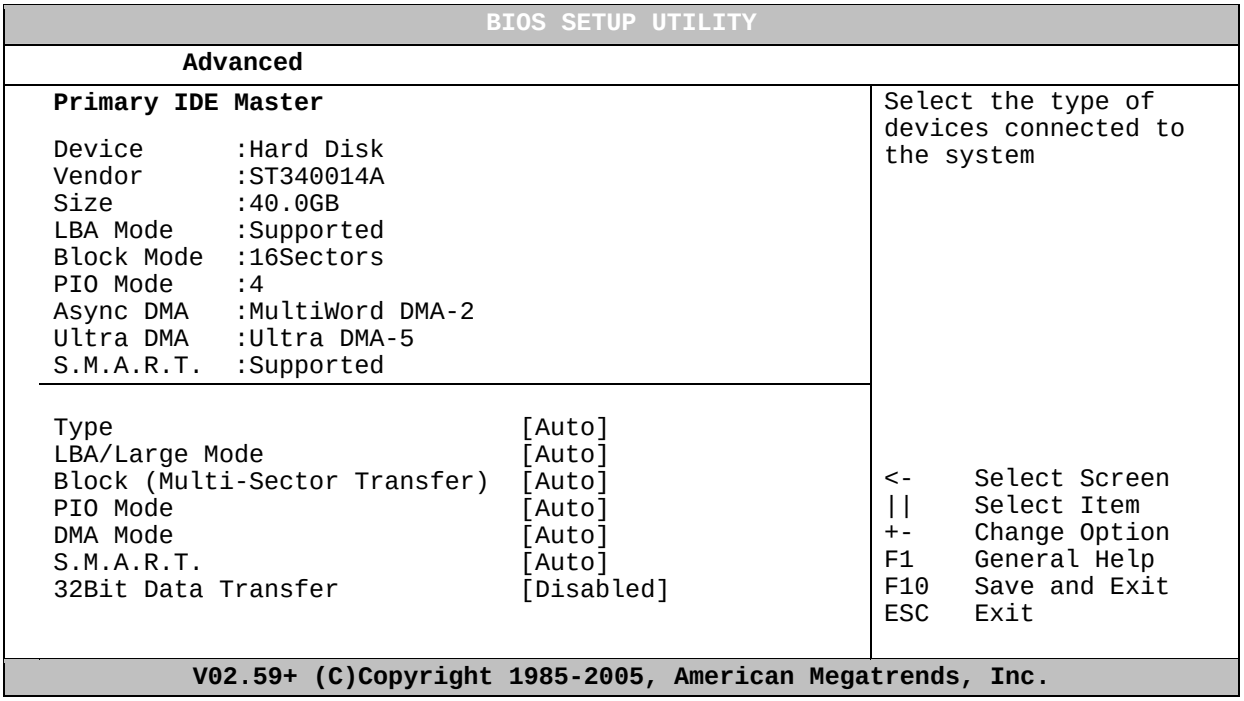
Feature	Options	Description
ATA/IDE Configuration	Disable **Compatible** Enhanced	Disable, Compatible (SATA0 and SATA2 bootable) Enhanced (all SATA ports bootable)

Feature	Options	Description
Legacy IDE Channels	SATA Only PATA Pri, SATA Sec **SATA Pri, PATA Sec** PATA Only	

When P-ATA only mode is selected:

Feature	Options	Description
Configure S-ATA as	**Disabled** RAID	Note: Install the driver via USB-Floppy connected to USB port 2 (lower connector)

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Feature	Options	Description
Type	Not Installed **Auto** CDROM ARMD	Select the type of device installed
LBA/Large Mode	Disabled **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled **Auto**	Select if the device should run in Block mode
PIO Mode	**Auto** 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	**Auto**, SWDMA0, SWDMA1, SWDMA2, MWDMA0, MWDMA1, MWDMA2, UDMA0, UDMA1, UDMA2, UDMA3, UDMA4, UDMA5	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Note: To use UDMA Mode 2, 3, 4 and 5 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).**
S.M.A.R.T.	**Auto** Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	**Disabled** Enabled	Select if the Device should be using 32Bit data Transfer

(continues)

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Feature	Options	Description
Hard Disk Write Protect	**Disable** Enabled	Enable write protection on HDDs, only works when it is accessed through the BIOS
IDE Detect Time Out (Sec)	0, 5, 10, 15, 20, 25, 30, **35**	Select the time out value when the BIOS is detecting ATA/ATAPI Devices
ATA(PI) 80Pin Cable Detection	**Host & Device** Host Device	Select the mechanism for detecting 80Pin ATA (PI) Cable

8.3.3 Advanced settings – LAN Configuration

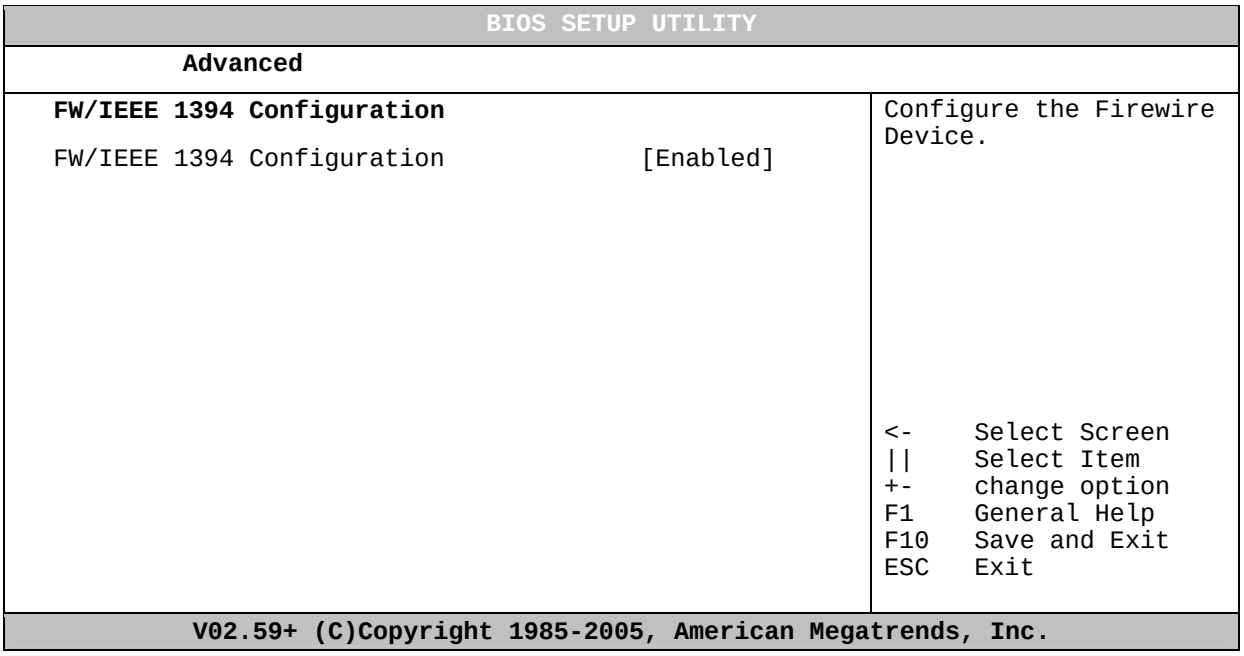
```
                        BIOS SETUP UTILITY
                              Advanced
  LAN Configuration                                  Control of Ethernet
                                                     Devices and RPL/PXE
  ETH1 Configuration                 [Enabled]       boot
    MAC Address                      :00E0F4000001
  ETH2 Configuration  (Upper)        [Enabled]
    MAC Address                      :00E0F4000002
  ETH3 Configuration  (Lower)        [Enabled]
    MAC Address                      :00E0F4000003

                                                     <-    Select Screen
                                                     ||    Select Item
                                                     +-    change option
                                                     F1    General Help
                                                     F10   Save and Exit
                                                     ESC   Exit
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```

Feature	Options	Description
ETH1 Configuration	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH2 Configuration	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH3 Configuration	Disabled **Enabled** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom

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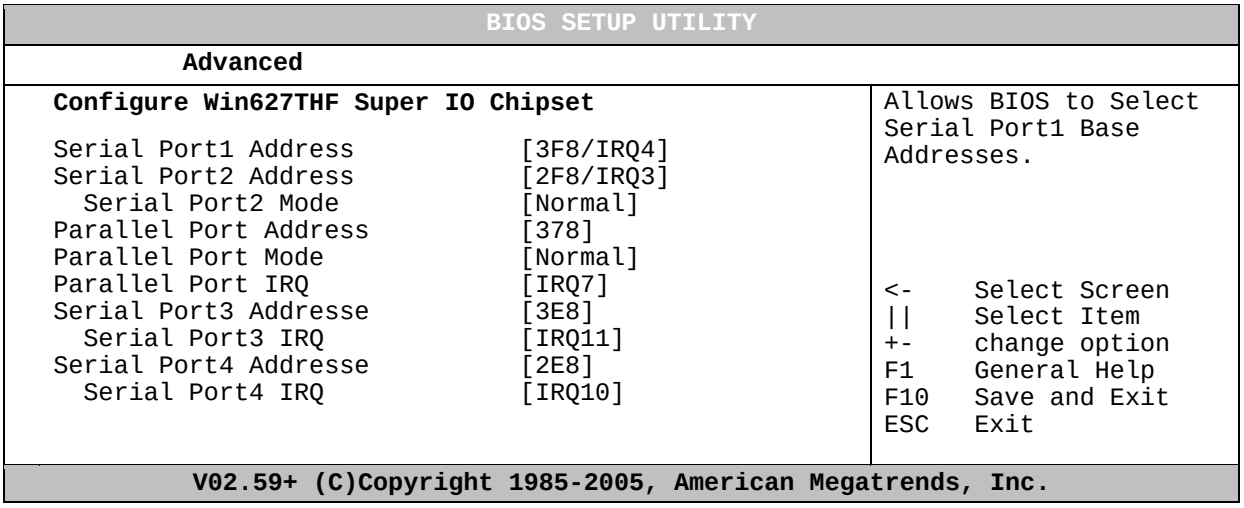
8.3.4 FW/IEEE 1394 Configuration



Feature	Options	Description
FW/IEEE 1394 Configuration	Disabled **Enabled**	Configure the Firewire Device.

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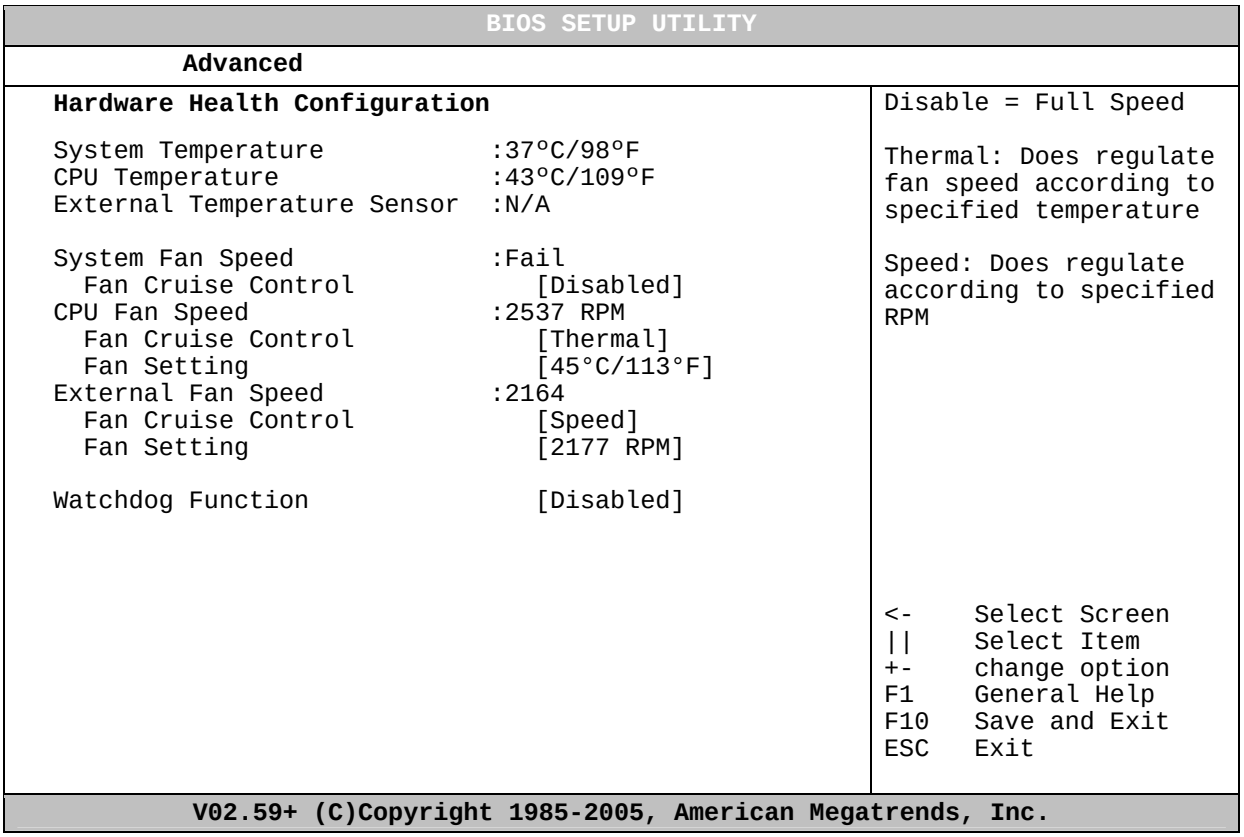
8.3.5 Advanced settings – Super IO Configuration



Feature	Options	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Address	Disabled 3F8/IRQ4 **2F8/IRQ3** 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Mode	**Normal**, IRDA, ASK IR	Select Mode for Serial Port2
Parallel Port Address	Disabled ***** **378** 278 3BC	Select the I/O address for the LPT.
Parallel Port Mode	**Normal**, Bi-Directional, ECP, EPP, ECP & EPP	Allow BIOS to select the mode that the parallel port will operate in.
EPP Version	**1.9** 1.7	Setup with version of EPP you want to run on the parallel port
ECP Mode DMA Channel	DMA0, DMA1, **DMA3**	Select a DMA channel
Parallel Port IRQ	IRQ5, **IRQ7**	Select a IRQ
Serial Port3 Address	Disabled 3F8 2F8 **3E8** 2E8	Select the BASE I/O address (The available options depends on the setup for the the other Serial Ports).
Serial Port3 IRQ	IRQ3, IRQ4 IRQ10, **IRQ11**	Allows BIOS to select Serial Port 3 IRQ
Serial Port4 Address	Disabled 3F8 2F8 3E8 **2E8**	Select the BASE I/O address (The available options depends on the setup for the the other Serial Ports).
Serial Port4 IRQ	IRQ3, IRQ4 **IRQ10,** IRQ11	Allows BIOS to select Serial Port 4 IRQ

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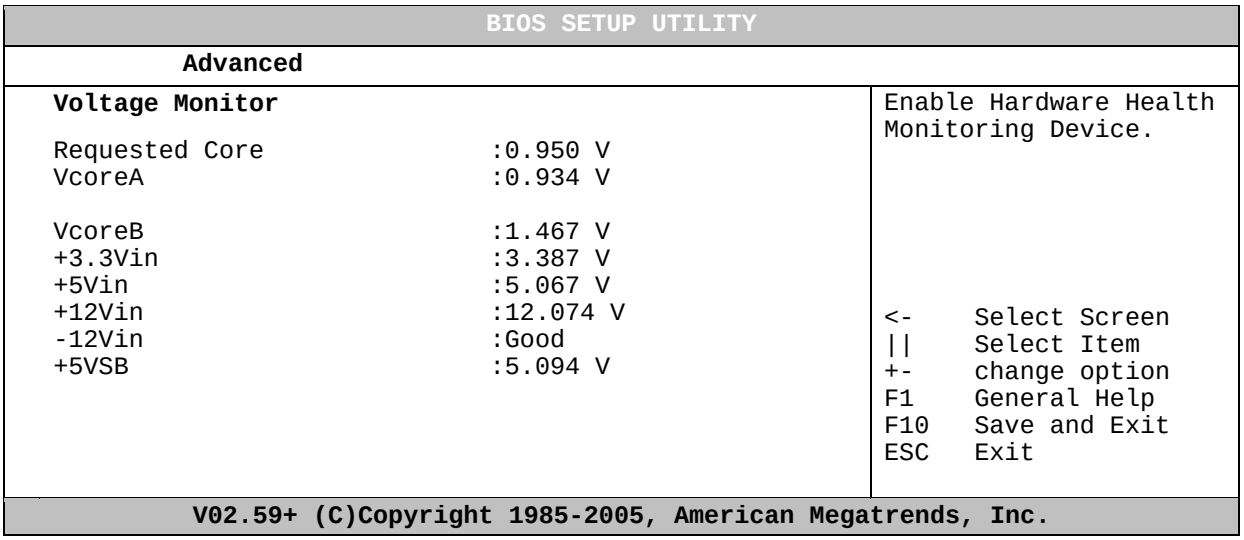
8.3.6 Advanced settings – Hardware Health Configuration



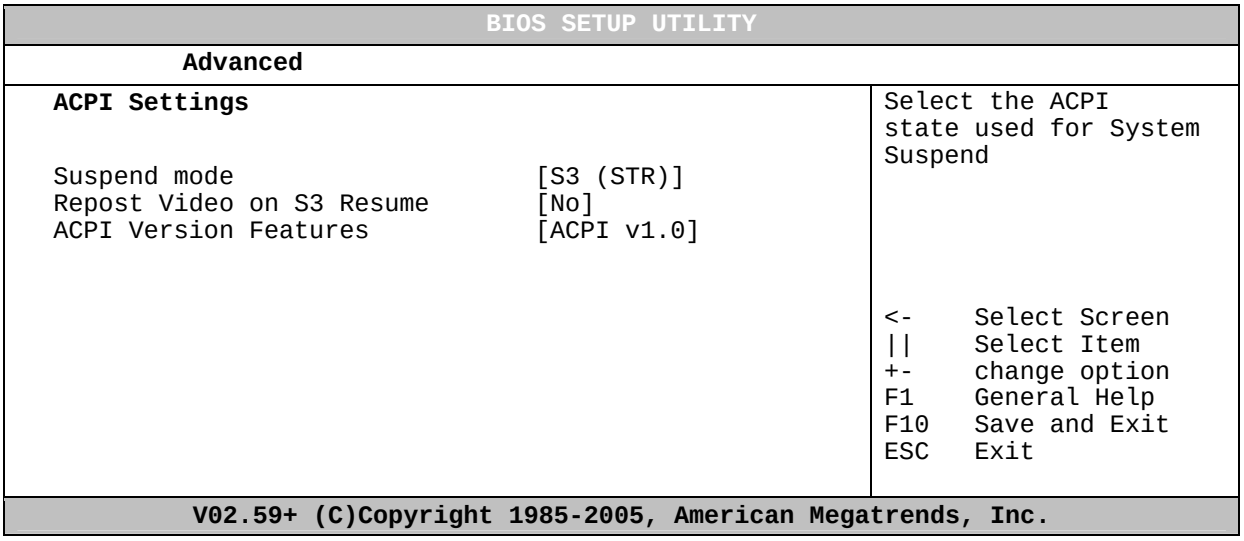
Feature	Options	Description
Fan Cruise Control	**Disabled** Thermal Speed	Select how the Fan shall operate. When set to Thermal, the Fan will start to run at the CPU die temperature set below. When set to Speed, the Fan will run at the Fixed speed set below.
Fan Settings	1406-5625 RPM, 30°-75°C	The fan can operate in Thermal mode or in a fixed fan speed mode
Watchdog	**Disabled,** 15 seconds, 30 seconds, 1 minute, 2 minutes, 5 minutes, 10 minutes	To be service via API.

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8.3.7 Advanced settings – Voltage Monitor



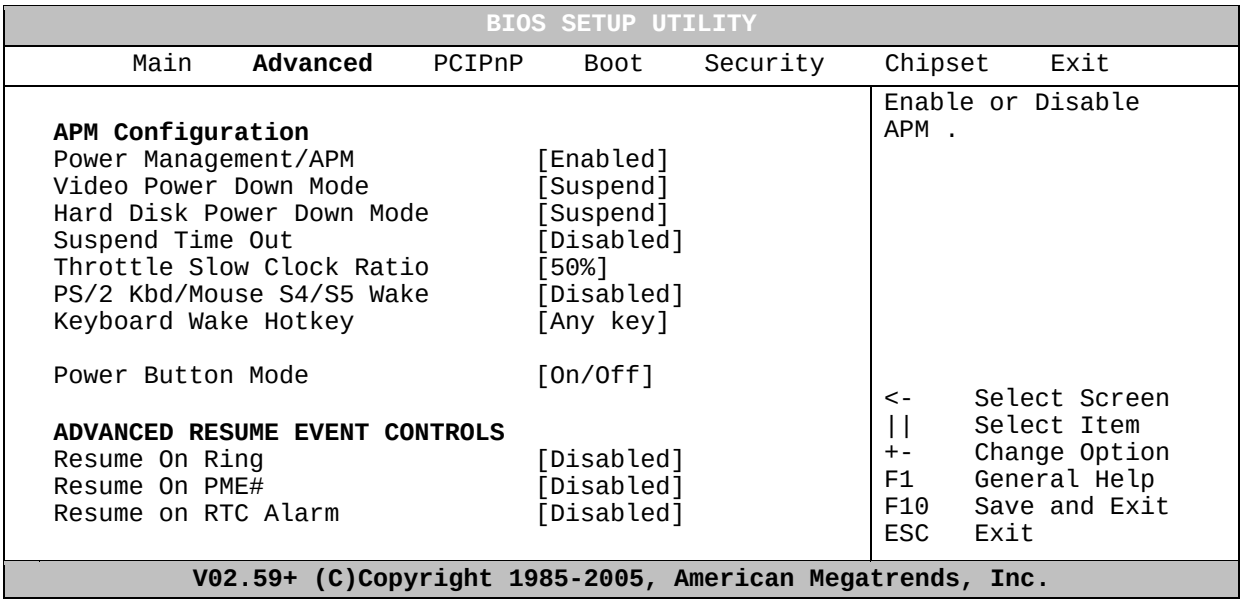
8.3.8 Advanced settings – ACPI Configuration



Feature	Options	Description
Suspend mode	S1 (POS) ***** **S3 (STR)** Auto	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	**No** Yes	Determine whether to invoke VGA BIOS post on S3/STR resume.
ACPI Version Features	**ACPI v1.0** ACPI v2.0 ACPI v3.0	Enable RSDP pointers to 64-bit Fixed System Description Tables. Different ACPI version has some addition.

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8.3.9 Advanced settings – APM Configuration



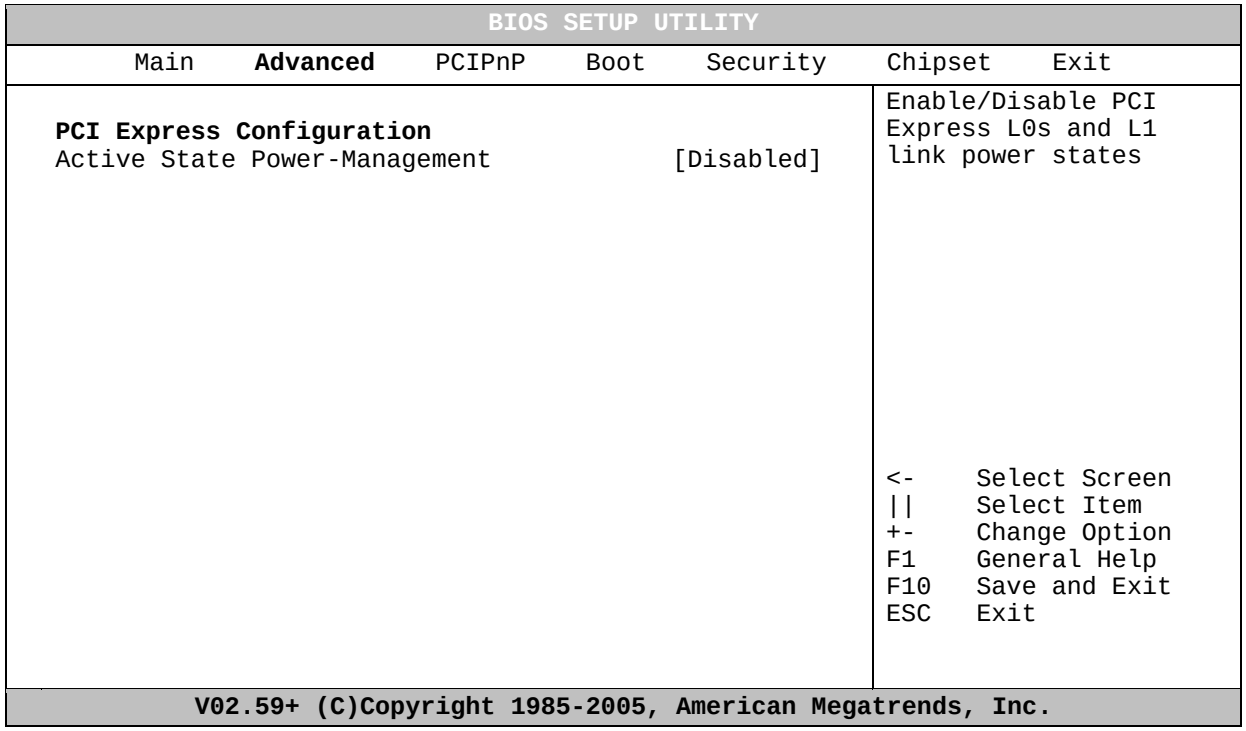
Feature	Options	Description
Power Management/APM	Disabled **Enabled**	Enable or disable APM.
Video Power Down Mode	**Suspend** Disabled *****	Power Down video in Suspend or Standby Mode
Hard Disk Power Down Mode	**Suspend** Disabled *****	Power Down Hard Disk in Suspend or Standby Mode
Suspend Time Out	**Disabled**, 1 Min, 2 Min, 4 Min, 8 Min, 10 Min, 20 Min, 30 Min, 40 Min, 50 Min, 60 Min	Go into Suspend in the specified Time.
Throttle Slow Clock Ratio	12.5%,25%,37.5%,**50%** 62.5%,75%,87.5%	Select the Duty Cycle in Throttle mode.
PS/2 Kbd/Mouse S4/S5 Wake	**Disabled** Enabled	Enabled: System can be waked from S4 or S5. Disabled: PS2 Kbd/Mse can still wake system from S3.
Keyboard Wake Hotkey	**Any Key** “SPACE” “ENTER” “Sleep button”	Any Key “SPACE” “ENTER” “Sleep button”
Power Button Mode	**ON/OFF** Suspend	Go into On/Off of Suspend when Power button is pressed.
Resume On Ring	**Disabled** Enabled	Disabled/Enable RI to generate a wake event.
Resume On PME#	**Disabled** Enabled	Disabled/Enable PME to generate a wake event. See note below.
Resume On RTC Alarm	**Disabled** Enabled	Disabled/Enable RTC to generate a wake event.
RTC Alarm Date (Days)	**15**	Key In “+” / “-“ to select.
RTC Alarm Time	**12:30:30**	Use [ENTER], [TAB] or [SHIFT-TAB] to select a field. Use [+] or [-] to configure system Time.

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Note on “Resume On PME#” (When using PCI LAN WOL function):

BIOS version must be 986LCD27 or higher. The LAN card must have a Standby Voltage input to make it possible to implement WOL. Very often such cards have a 3 pin connector and one of the pins is the Standby Voltage. This voltage can be taken directly from the ATX power supply or from the Font Panel connector pin 1 (or pin 2) or from the Feature connector pin 6.

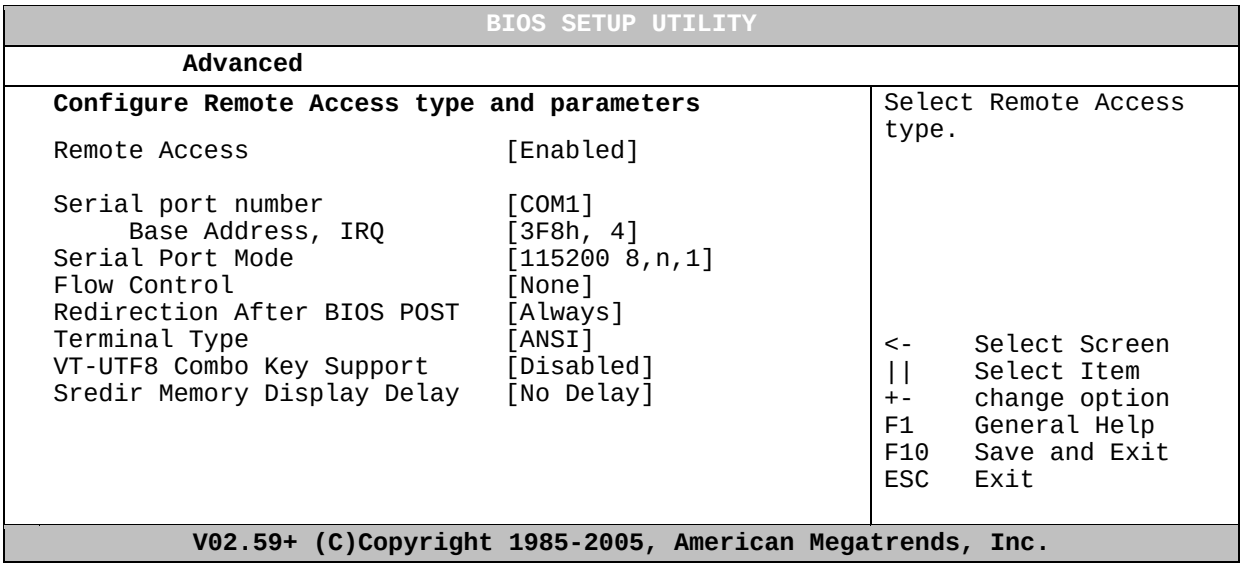
8.3.10 PCI Express Configuration



Feature	Options	Description
Active state Power-Management	**Disabled** Enable	Enable/Disable PCI Express L0s and L1 link power states

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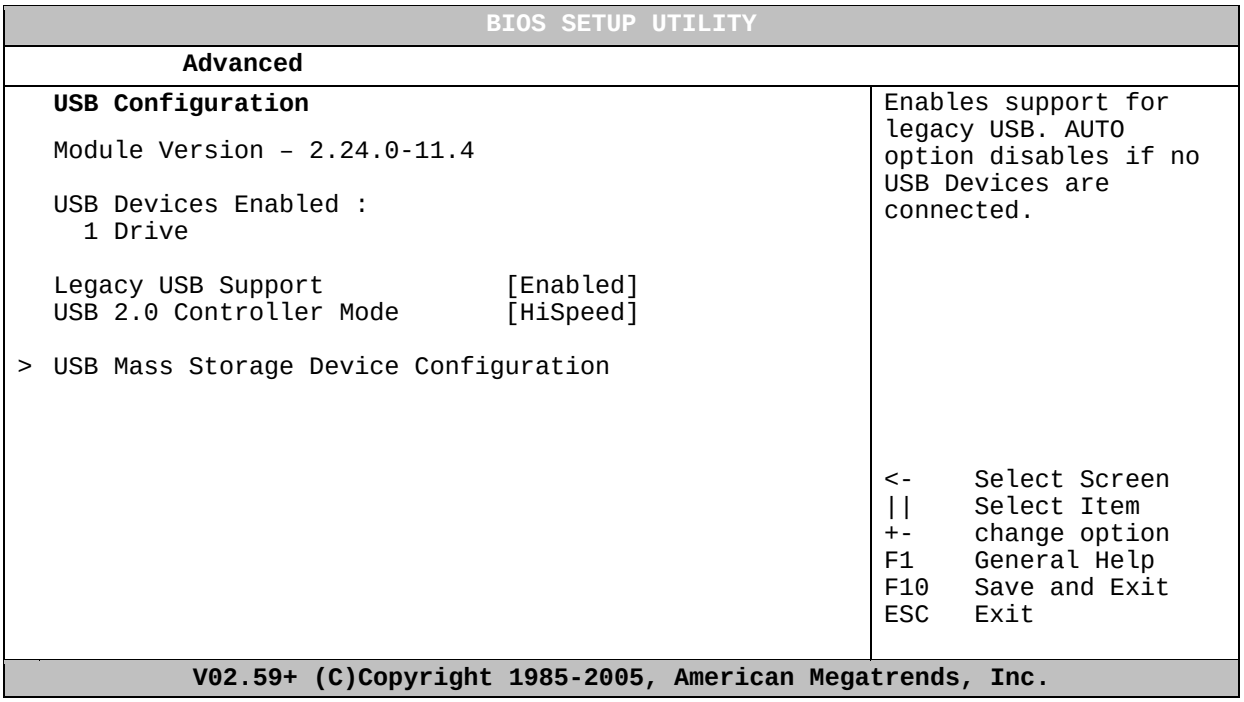
8.3.11 Advanced settings – Remote Access Configuration



Feature	Options	Description
Remote Access	**Disabled** Enabled	Allows you to see the screen over the comport interface, in a terminal window
Serial port number	**COM1** COM2	Setup which comport that should be used for communication
Serial Port Mode	**115200 8 n** 1 57600 8 n 1 38400 8 n 1 19200 8 n 1 9600 8 n 1	Select the serial port speed
Flow Control	**None** Hardware Software	Select Flow Control for serial port
Redirection After BIOS POST	Disabled Boot Loader **Always**	How long shall the BIOS send the picture over the serial port
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	Disabled **Enabled**	Setup VT-UTF8 Combo Key
Sredir Memory Display Delay	**No Delay** Delay 1 sec Delay 2 sec Delay 4 sec	Gives the delay in seconds to display memory information.

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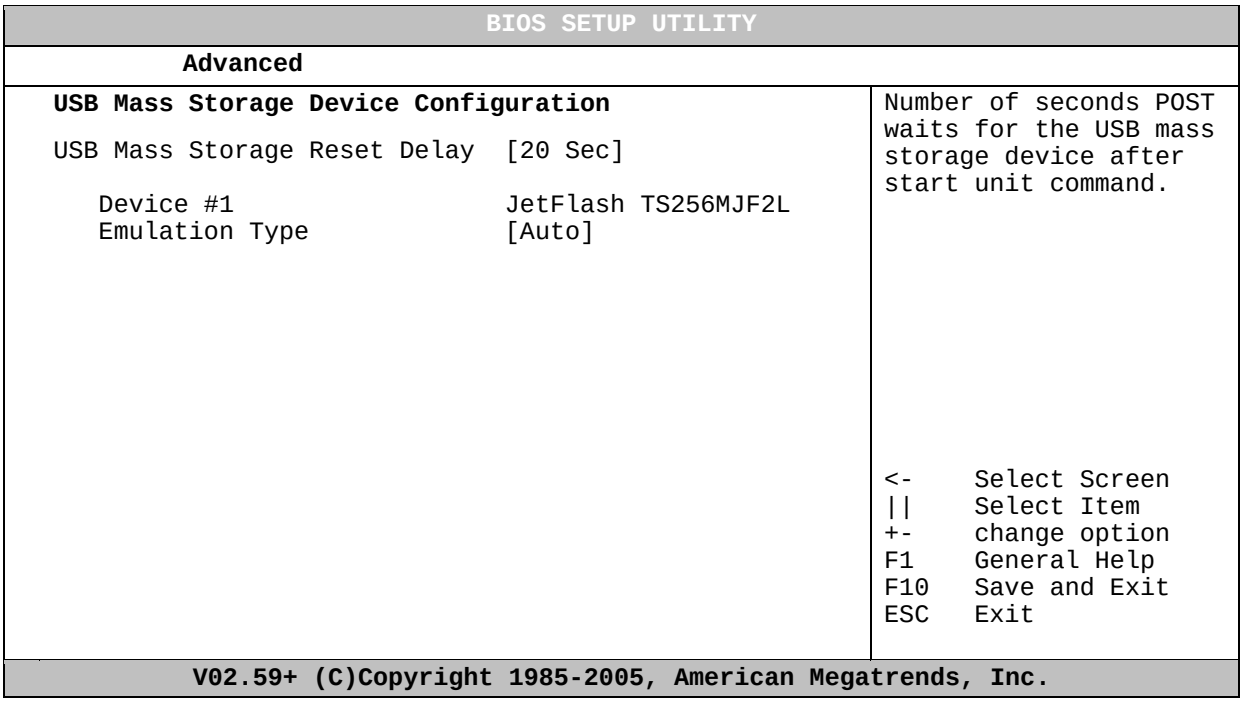
8.3.12 Advanced settings – USB Configuration



Feature	Options	Description
Legacy USB Support	Disabled **Enabled** Auto	Support for legacy USB Keyboard
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configure the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). Note: This feature is not available when Failsafe Defaults are loaded, because USB2.0 controller is disabled as default.

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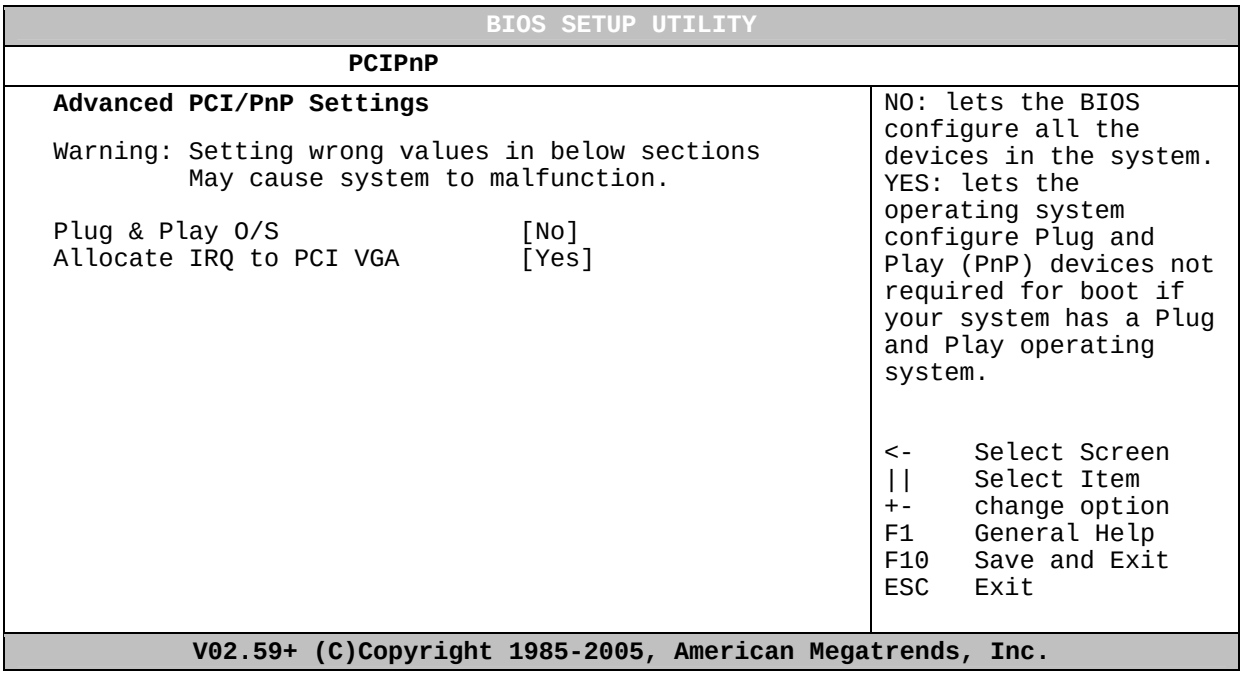
8.3.13 Advanced settings – USB Mass Storage Device Configuration



Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec **20 Sec** 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

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8.4 PCIPnP Menu



Feature	Options	Description
Plug & Play O/S	**No** Yes	NO: lets the BIOS configure all the devices in the system. YES: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.
Allocate IRQ to PCI VGA	**Yes** No	YES: Assigns IRQ to PCI VGA card if card request IRQ. NO: Does not assign IRQ to PCI VGA card even if card request an IRQ.

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8.5 Boot Menu

```
                              BIOS SETUP UTILITY
       Main     Advanced     PCIPnP     Boot     Security     Chipset     Exit
  Boot Settings                                          Configure Settings
                                                         during System Boot.
> Boot Settings Configuration

> Boot Device Priority


                                                         <-    Select Screen
                                                         ||    Select Item
                                                         Enter Go to Sub Screen
                                                         F1    General Help
                                                         F10   Save and Exit
                                                         ESC   Exit
                  V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.
```

8.5.1 Boot – Boot Settings Configuration

```
                              BIOS SETUP UTILITY
                                      Boot
  Boot Settings                                          Allows BIOS to skip
                                                         certain tests while
                                                         booting. This will
  Quick Boot                    [Enabled]                decrease the time
  Quiet Boot                    [Disabled]               needed to boot the
     Long Splash                [Disabled]               system.
  AddOn ROM Display Mode        [Force BIOS]
  Bootup Num-Lock               [On]
  PS/2 Mouse Support            [Auto]                   <-    Select Screen
  Wait for 'F1' If Error        [Enabled]                ||    Select Item
  Hit 'DEL' Message Display     [Enabled]                Enter Go to Sub Screen
  Interrupt 19 Capture          [Disabled]               F1    General Help
  Default init boot order       [Yes]                    F10   Save and Exit
  Force boot Device             [Disabled]               ESC   Exit
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```

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Feature	Options	Description
Quick Boot	**Enabled** Disabled	Allows BIOS to skip certain test while booting in order to decrease boot time.
Quiet Boot	**Disabled** Enabled Black Screen White Screen	Disabled: Displays normal POST messages. Enabled: Displays OEM Logo. Black Screen: Displays black picture (noting). White Screen: Display white picture.
Long Splash	**Disabled** WinXP ™ Vista ™	(Long Splash only available if Quiet Boot). WinXP ™: Boot logo until WinXP boots. Vista ™: Boot logo until Vista boots.
AddOn ROM Display Mode	**Force BIOS** Keep current	Set display mode for Option ROM.
Bootup Num-Lock	Off **On**	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	Select support for PS/2 Mouse.
Wait for 'F1' If Error (see note)	Disabled **Enabled**	Wait for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled **Enabled**	Displays "Press DEL to run Setup" in POST.
Interrupt 19 Capture	**Disabled** Enabled	Allows option ROMs to trap interrupt 19.
Default init boot order	**0->4->3->5->2->1** 0->4->3->5->1->2 1->2->3->5->0->4 3->5->1->2->0->4 3->0->4->1->2->5 2->1->0->4->3->5 2->0->4->3->1->5 2->1->0->4->2->5	The numbers in the sequence means: 0 = "Removables" 1 = "Hard Disk" 2 = "ATAPI CDROM" 3 = "BEV/onboard LAN" 4 = "USB" 5 = "External LAN"
Force boot Device	**Disabled** Primary IDE Master Primary IDE Slave Secondari IDE Master Secondary IDE Slave Third IDE Master Third IDE Slave Network	Does overwrite current boot setting. Device must be in the boot priority menu though. If the device fails to boot, the system will not try other devices.

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Note: List of errors:

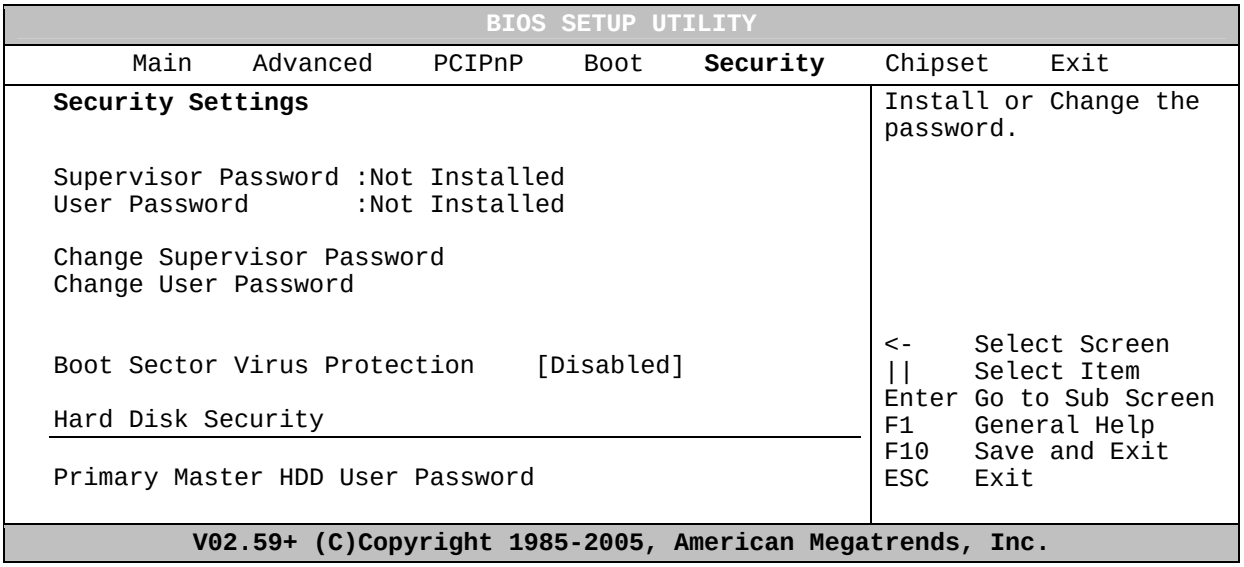
<INS> Pressed	Primary Master Hard Disk Error	PCI I/O conflict
Timer Error	S.M.A.R.T HDD Error	PCI ROM conflict
Interrupt Controller-1 error	Cache Memory Error	PCI IRQ conflict
Keyboard/Interface Error	DMA Controller Error	PCI IRQ routing table error
Halt on Invalid Time/Date	Resource Conflict	
NVRAM Bad	Static Resource Conflict	

8.5.2 Boot – Boot Device Priority

BIOS SETUP UTILITY	
Boot	
Boot Device Priority 1st Boot Device [ESS-ST380811AS]	Specifies the boot sequence from the available devices. A device enclosed in paranthesis has been disabled in the corresponding type menu. <- Select Screen || Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
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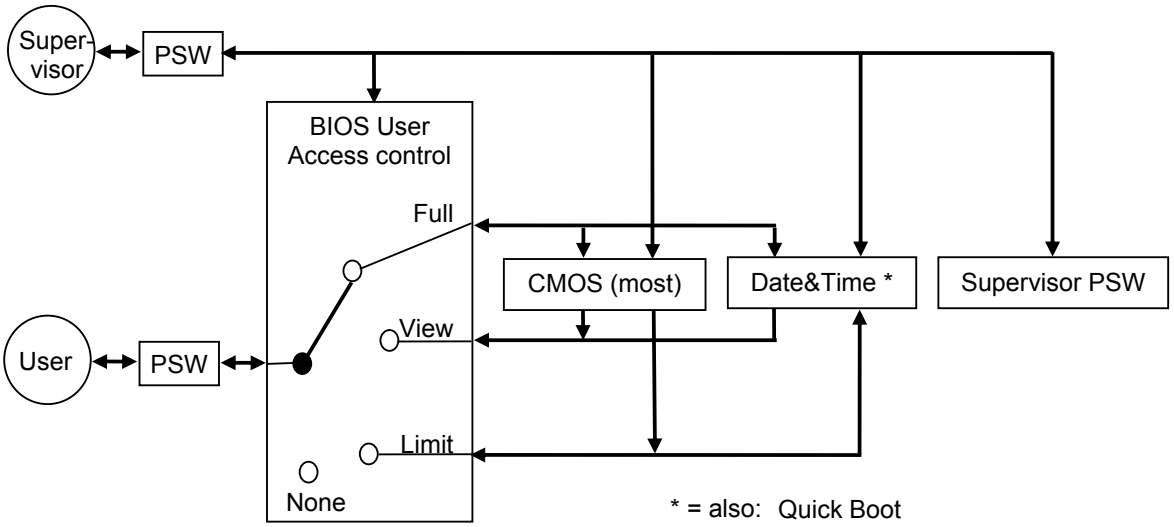
8.6 Security Menu



Feature	Options	Description
Change Supervisor Password	Password	When not cleared the advanced Supervisor Password protection system is enabled (see below diagram). Hereafter setting can only be accessed when entering BIOS as Supervisor.
User Access Level	**Full Access** View Only Limited No Access	Only visible if Supervisor Password is installed. Full Access: User can change all BIOS settings. View Only: User can only read BIOS settings. Limited: User can only read settings except: Date & Time, Quick Boot, Quiet Boot, Repost Video on S3 Resume, Active State Power-Management and Remote Access. No Access: User can not enter BIOS, but if Password Check = Always then User password will allow boot.
Change User Password	Password	Change the User Password
Password Check	**Setup** Always	Only visible if Password is installed. Setup: Protects only BIOS settings. Always: Protects both BIOS settings and Boot.
Boot Sector Virus Protection	Enabled **Disabled**	Will write protect the MBR when the BIOS is used to access the harddrive
HDD Password	Password	Locks the HDD with a password, the user needs to type the password on power on

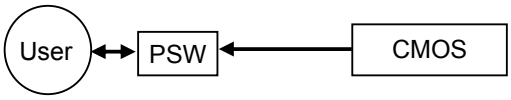
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Supervisor Password protection (setup Supervisor before User)



* = also: Quick Boot
Quiet Boot
Repost Video on S3 Resume
Active State Power-Management
Remote Access.

User Password protection only (no Supervisor Password used)



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8.7 Chipset Menu

```
                              BIOS SETUP UTILITY
       Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit
  Advanced Chipset Settings                          Configures North
                                                     Bridge features.
  Warning: Setting wrong values in below sections
           may cause system to malfunction.

> North Bridge Configuration
> South Bridge Configuration                        <-    Select Screen
                                                    ||    Select Item
                                                    Enter Go to Sub Screen
                                                    F1    General Help
                                                    F10   Save and Exit
                                                    ESC   Exit
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```

8.7.1 Advanced Chipset Settings – North Bridge Chipset Configuration

```
                              BIOS SETUP UTILITY
                                                              Chipset
  North Bridge Adapter Priority Configuration

  Boots Graphics Adapter Priority    [PEG/ PCI]
  Internal Graphics Mode Select      [Enabled, 8MB]

  PEG Port Configuration
    PEG Port                         [Auto]
    PEG Force x1                     [Disabled]

> Video Function Configuration                     <-    Select Screen
                                                   ||    Select Item
                                                   Enter Go to Sub Screen
                                                   F1    General Help
                                                   F10   Save and Exit
                                                   ESC   Exit
                  V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.
```

Feature	Options	Description
Boots Graphics Adapter Priority	IGD PCI/IGD PCI/PEG PEG/IGD **PEG/PCI**	Select which graphics controller to use as the primary boot device.
Internal Graphics Mode Select	Disabled Enabled, 1MB **Enabled, 8MB**	Select the amount of system memory used by the Internal graphics device
PEG Port	**Auto** Disabled	
PEG Force x1	Enabled **Disabled**	

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8.7.2 Advanced Chipset Settings – Video Function Configuration

```
                        BIOS SETUP UTILITY
                                                          Chipset
  Video Function Configuration

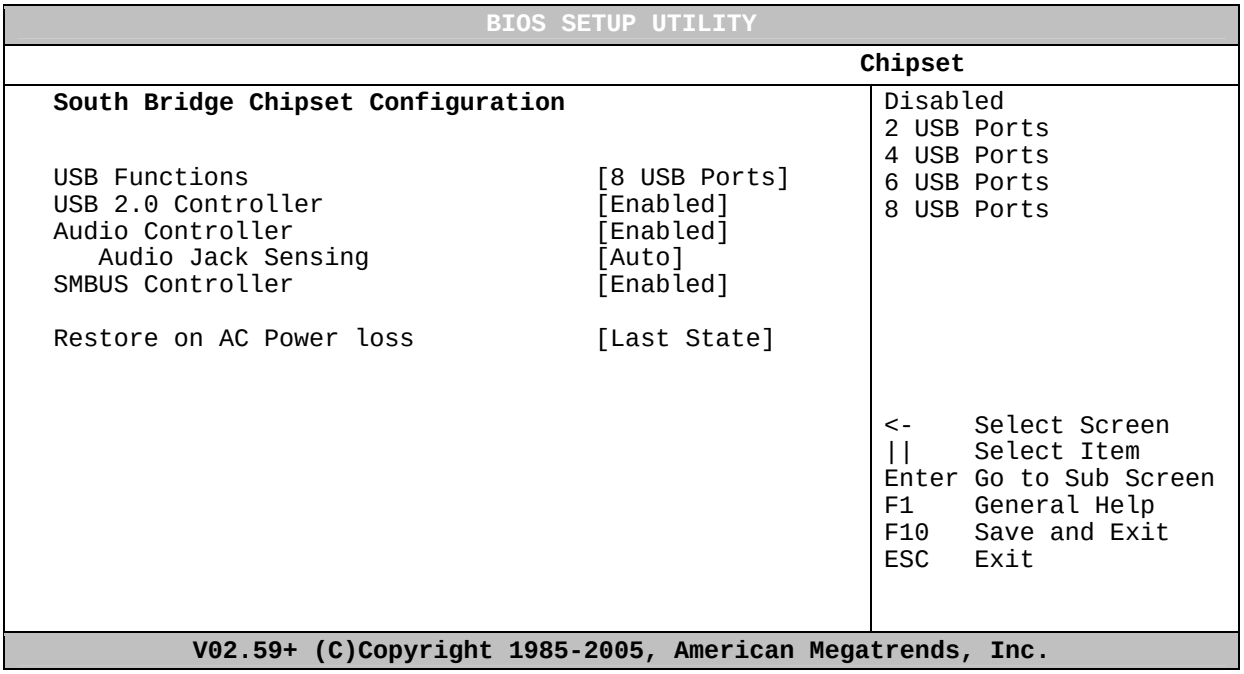
  DVMT Mode Select                  [DVMT Mode]           Fixed Mode
    DVMT/ Fixed Memory              [128MB]               DVMT Mode
                                                          Combo Mode
  Boot Type:                        [CRT]
  Backlight Signal Inversion        [Disabled]
  LCDVCC Voltage                    [3.3V]

                                                          <-    Select Screen
  LVDS                              [None]                ||    Select Item
  SDVO                              [N/A]                 Enter Go to Sub Screen
                                                          F1    General Help
                                                          F10   Save and Exit
                                                          ESC   Exit
                    V02.59+ (C)Copyright 1985-2005, American Megatrends, Inc.
```

Feature	Options	Description
DVMT Mode Select	Fixed Mode **DVMT Mode** Combo Mode	Setup Video memory mode
DVMT/ Fixed Memory	64MB **128MB** Maximum DVMT	
Boot Type	VBIOS Default **CRT** LFP CRT+LFP EFP TV CRT+EFP CRT+TV EFP+EFP2 EFP+TV CRT+CRT2	VBIOS: Automatic detection. CRT: Boot on CRT (onboard VGA CRT) LFP: Boot on Local Flat Panel (onboard LVDS) CRT+LFP: Boot on CRT and on LFP EFP: Boot on External Flat Panel (ADD2-card) TV: Boot on TV (only available on some boards) CRT+EFT: Boot on CRT and on EFP CRT+TV: Boot on CRT and TV EFP+EFP2: Not supported EFP+TV: Not supported CRT+CRT2: Boot on CRT and CRT2 (ADD2-CRT)
LCDVCC Voltage	**3.3V** 5V	Select LCDVCC voltage for LVDS connector output
LVDS	(see description ->)	Select Resolution, Manufacturer and Type no. for the actual LVDS display.
SDVO	N/A (see description ->) DVI-D DVI-I CRT	N/A: No ADD2 card detected -> ADD2-LVDS card: select display type. DVI-D: ADD2-DVI card installed DVI-I: Not supported CRT: ADD2-CRT card installed

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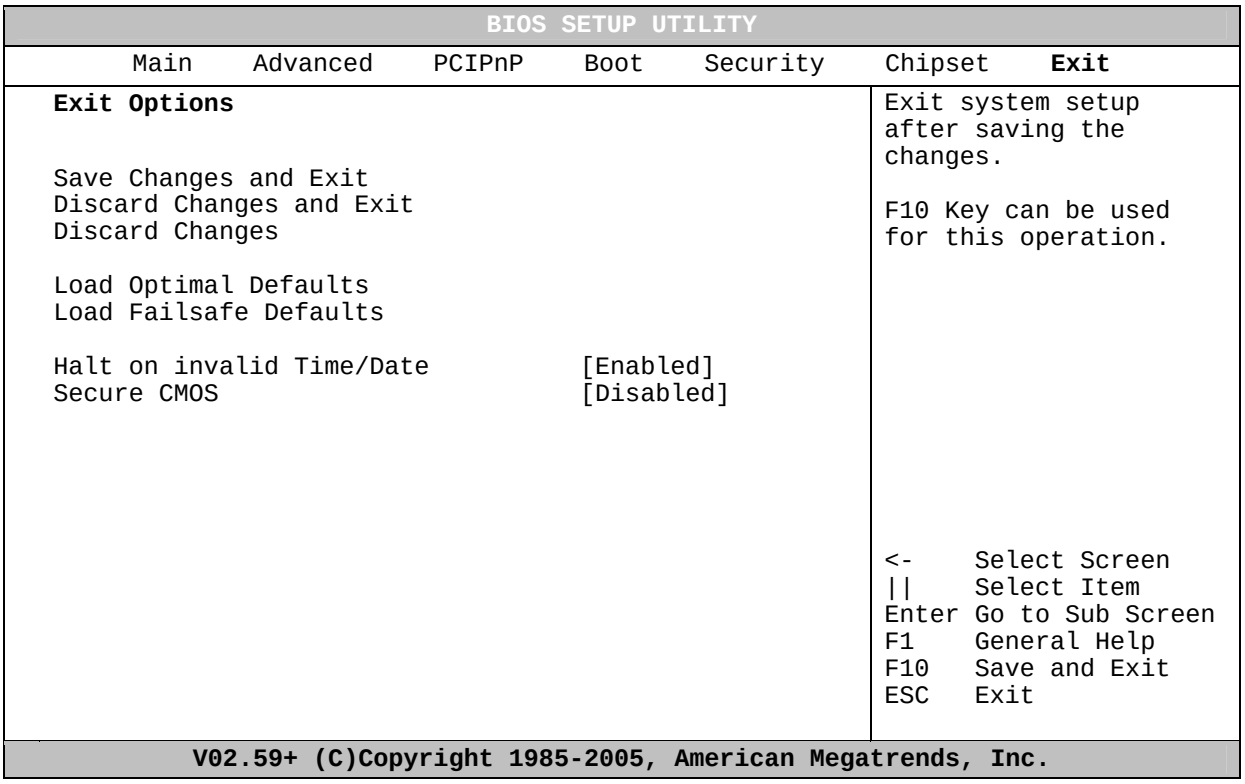
8.7.3 Advanced Chipset Settings – SouthBridge Configuration



Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports **8 USB Ports**	
USB 2.0 Controller	**Enabled** Disabled *****	
Audio Controller	**Enabled** Disabled	
Audio Jack Sensing	**Auto** Disabled	Auto: The insertion of audio jacks are auto determined. Disabled: Driver assumes that all jacks are inserted (usefull when using Audio pinrow).
SMBUS Controller	**Enabled** Disabled	
Restore on AC Power loss	Power Off Power On **Last State**	

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8.8 Exit Menu



Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	**Enabled** Disabled	
Secure CMOS	Enabled **Disabled**	Enable will store current CMOS in non volatile ram. This will maintain the settings even if battery is failing.

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8.9 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

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9. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on the 986LCD-M Driver CD or they can be downloaded from the homepage www.kontron.com

Note: When installing/using ADD cards like ADD-DVI or ADD-LVDS it's possible that the OS start up without any connected display(s) active. If you are able to pass the "Log On to Windows" etc. by entering the password etc. without actually see the picture on the display and If the Hot Keys have not been disabled in the Extreme Graphic driver then the following key combinations you can select a connected display:

<Ctrl><Alt><F1> enables the CRT (on board)
<Ctrl><Alt><F3> enables the LVDS (on board)
<Ctrl><Alt><F4> enables display conneted to the ADD card.

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10. Warranty

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   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
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   E. Any other causes which does not relate to a product defect.
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