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AM4010

Single Mid and Full-size AMC Module based on the Intel® Core™ Duo Processor and the Intel® Core™ 2 Duo Processor with the Intel® 3100 Chipset

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User Guide

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Table of Contents

Revision History ..... *ii*
Imprint ..... *ii*
Disclaimer ..... *ii*
Table of Contents ..... *iii*
List of Tables ..... *vii*
List of Figures ..... *ix*
Proprietary Note ..... *xi*
Trademarks ..... *xi*
Environmental Protection Statement ..... *xi*
Explanation of Symbols ..... *xii*
For Your Safety ..... *xiii*
High Voltage Safety Instructions ..... *xiii*
Special Handling and Unpacking Instructions ..... *xiii*
General Instructions on Usage ..... *xiv*
Two Year Warranty ..... *xv*

1. Introduction ..... 1 - 3
1.1 AdvancedTCA System Overview ..... 1 - 3
1.2 Board Overview ..... 1 - 4
1.2.1 Board Introduction ..... 1 - 4
1.2.2 Board-Specific Information ..... 1 - 5
1.3 System Relevant Information ..... 1 - 6
1.4 Board Diagrams ..... 1 - 6
1.4.1 Functional Block Diagram ..... 1 - 6
1.4.2 Front Panel ..... 1 - 8
1.4.3 Board Layouts ..... 1 - 9
1.5 Technical Specification ..... 1 - 10
1.6 Kontron Software Support ..... 1 - 14
1.7 Standards ..... 1 - 15
1.8 Related Publications ..... 1 - 16

2. Functional Description ..... 2 - 3
2.1 CPU, Memory and Chipset ..... 2 - 3

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2.1.1 CPU ....2 - 3
2.1.2 Memory ....2 - 4
2.1.3 Intel® 3100 Chipset ....2 - 4
2.2 Peripherals ....2 - 4
2.2.1 Timer ....2 - 4
2.2.2 Watchdog Timer ....2 - 5
2.2.3 Battery ....2 - 5
2.2.4 Power Monitor and Reset Generation ....2 - 5
2.2.5 FLASH Memory ....2 - 5
2.3 Board Interfaces ....2 - 6
2.3.1 Front Panel LEDs ....2 - 6
2.3.2 General Purpose DIP Switch ....2 - 9
2.3.3 Debug Interface ....2 - 9
2.3.4 USB Host Interface ....2 - 10
2.3.5 Serial Ports ....2 - 10
2.3.6 Gigabit Ethernet Interfaces ....2 - 11
2.3.7 Serial ATA Interface ....2 - 12
2.4 AMC Interconnection ....2 - 13
2.4.1 Fabric Interface ....2 - 13
2.4.2 Synchronization Clock Interface ....2 - 15
2.4.3 System Management Interface ....2 - 15
2.4.4 JTAG Interface ....2 - 15
2.4.5 Module Power Interface ....2 - 15
2.4.6 Pinout of AMC Card-edge Connector J1 ....2 - 16
2.5 Module Management ....2 - 20
2.5.1 Module Management Controller ....2 - 20

3. Installation ....3 - 3

3.1 Safety Requirements ....3 - 3
3.2 AM4010 Hot Swap Insertion Procedures ....3 - 4
3.3 AM4010 Hot Swap Extraction Procedures ....3 - 5
3.4 Software Installation ....3 - 5

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4. Configuration ..... 4 - 3

4.1 DIP Switch Configuration ..... 4 - 3
4.1.1 User-Specific LED Configuration (BIOS POST Code) ..... 4 - 4
4.1.2 BIOS Firmware Hub Flash Configuration ..... 4 - 4
4.1.3 Boot Order Configuration ..... 4 - 4
4.1.4 Clear BIOS CMOS Configuration ..... 4 - 4
4.2 Interrupts ..... 4 - 5
4.3 Memory Map ..... 4 - 6
4.3.1 I/O Address Map ..... 4 - 6
4.4 AM4010-Specific Registers ..... 4 - 6
4.4.1 BIOS Configuration Register ..... 4 - 7
4.4.2 MMC I/O Status Register ..... 4 - 7
4.4.3 Watchdog Timer Control Register ..... 4 - 8
4.4.4 AMC Geographic Addressing Register ..... 4 - 10
4.4.5 Board and Logic Revision Register ..... 4 - 10
4.4.6 Reset Status Register ..... 4 - 11
4.4.7 Host I/O Status Register ..... 4 - 12
4.4.8 Host I/O Configuration Register ..... 4 - 12
4.4.9 Board ID Register ..... 4 - 12
4.4.10 Board Interrupt Configuration Register ..... 4 - 13
4.4.11 Hot Swap Status Register ..... 4 - 13
4.4.12 User-Specific LED Configuration Register ..... 4 - 14
4.4.13 User-Specific LED Control Register ..... 4 - 16
4.4.14 Serial Over LAN Configuration Register ..... 4 - 17
4.4.15 Delay Timer Control and Status Register ..... 4 - 18
4.4.16 MMC Configuration Register ..... 4 - 19
4.4.17 IPMI Keyboard Control Style Interface ..... 4 - 19

5. Power Considerations ..... 5 - 3

5.1 AM4010 Voltage Ranges ..... 5 - 3
5.2 Carrier Power Requirements ..... 5 - 3
5.2.1 Payload Power ..... 5 - 3
5.2.2 Payload and MMC Voltage Ramp ..... 5 - 4

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5.2.3 Module Management Power Consumption .....5 - 4
5.3 Payload Power Consumption of the AM4010 .....5 - 4
5.4 IPMI FRU Payload Power Consumption .....5 - 6
5.5 Payload Start-Up Current of the AM4010 .....5 - 6

6. Thermal Considerations .....6 - 3
6.1 Thermal Monitoring .....6 - 3
6.1.1 Placement of the Temperature Sensors .....6 - 4
6.1.2 Board Thermal Monitoring .....6 - 5
6.1.3 Processor Thermal Monitoring .....6 - 5
6.1.4 Chipset Thermal Monitor Feature .....6 - 7
6.2 System Airflow .....6 - 8
6.2.1 Forced Airflow in MicroTCA Systems .....6 - 8
6.2.2 Airflow Impedance .....6 - 10
6.2.3 Airflow Paths .....6 - 11

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List of Tables

1-1 System Relevant Information ..... 1 - 6
1-2 AM4010 Main Specifications ..... 1 - 10
1-3 Standards ..... 1 - 15
1-4 Related Publications ..... 1 - 16
2-1 Module Management LED Function ..... 2 - 7
2-2 User-Specific LED Function ..... 2 - 8
2-3 POST Code Example ..... 2 - 9
2-4 DIP Switch Functions ..... 2 - 9
2-5 USB Connector J2 Pinout ..... 2 - 10
2-6 Serial Con. J4 (COM1) Pinout ..... 2 - 10
2-7 Gigabit Ethernet Connector J3 Pinout Based on the Implementation .... 2 - 12
2-8 Pinout of AMC Edge Connector J1 ..... 2 - 16
2-9 Reserved Pins Description ..... 2 - 19
2-10 Extended Options Region Pins Description ..... 2 - 19
2-11 JTAG Pins Description ..... 2 - 19
2-12 Processor and Chipset Supervision ..... 2 - 21
2-13 AMC-Specific Signals ..... 2 - 21
2-14 Onboard Power Supply Supervision ..... 2 - 21
2-15 Temperature Signals ..... 2 - 22
4-1 DIP Switch Functions ..... 4 - 3
4-2 User-Specific LED Configuration (BIOS POST Code) ..... 4 - 4
4-3 BIOS Firmware Hub Flash Configuration ..... 4 - 4
4-4 BIOS Boot Order Configuration ..... 4 - 4
4-5 BIOS CMOS Configuration ..... 4 - 4
4-6 Interrupt Setting ..... 4 - 5
4-7 I/O Address Map ..... 4 - 6
4-8 BIOS Configuration Register ..... 4 - 7
4-9 MMC I/O Status Register ..... 4 - 7
4-10 Watchdog Timer Control Register ..... 4 - 9
4-11 AMC Geographic Addressing Register ..... 4 - 10
4-12 Board and Logic Revision Register ..... 4 - 10
4-13 Reset Status Register ..... 4 - 11

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4-14 Host I/O Status Register ..... 4 - 12
4-15 Host I/O Configuration Register ..... 4 - 12
4-16 Board ID Register ..... 4 - 12
4-17 Board Interrupt Configuration Register ..... 4 - 13
4-18 Hot Swap Status Register ..... 4 - 13
4-19 User-Specific LED Configuration Register ..... 4 - 14
4-20 User-Specific LED Control Register ..... 4 - 16
4-21 Serial over LAN Configuration Register ..... 4 - 17
4-22 Delay Timer Control and Status Register ..... 4 - 18
4-23 MMC Configuration Register ..... 4 - 19
5-1 DC Operational Input Voltage Ranges ..... 5 - 3
5-2 Payload Power Consumption: AM4010 with Core™ Duo, 1.2 GHz ..... 5 - 5
5-3 Payload Power Consumption: AM4010 with Core™ Duo, 1.66 GHz ..... 5 - 5
5-4 Payload Power Consumption: AM4010 with Core™ 2 Duo, 1.5 GHz ..... 5 - 5
5-5 IPMI FRU Payload Power Consumption of the AM4010 ..... 5 - 6
5-6 Payload Start-Up Current of the AM4010 ..... 5 - 6
6-1 Pressure Drop vs. Airflow Data ..... 6 - 10
6-2 Deviation of the Airflow Rate on a Mid-Size AM4010 ..... 6 - 11
6-3 Deviation of the Airflow Rate on a Full-Size AM4010 ..... 6 - 12

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Figures

1-1 AM4010 Functional Block Diagram ..... 1 - 7
1-2 AM4010 Front Panel Versions ..... 1 - 8
1-3 AM4010 Board Layout (Top View) ..... 1 - 9
1-4 AM4010 Board Layout (Bottom View) ..... 1 - 9
2-1 Front Panel LEDs ..... 2 - 6
2-2 USB Connector J2 ..... 2 - 10
2-3 Serial Con. J4 (COM1) ..... 2 - 10
2-4 Gigabit Ethernet Connector J3 ..... 2 - 12
2-5 AM4010 Port Mapping ..... 2 - 14
4-1 DIP Switch ..... 4 - 3
6-1 Board Temperature Sensor Placement (AM4010 Bottom View) ..... 6 - 4
6-2 Processor Temperature Sensor Placement (AM4010 Top View) ..... 6 - 4
6-3 Temperature vs. Airspeed Graph of a Mid-Size AM4010 ..... 6 - 8
6-4 Temperature vs. Airspeed Graph of a Full-Size AM4010 ..... 6 - 9
6-5 Mid-Size and Full-Size AM4010 Impedance Curves ..... 6 - 10
6-6 Thermal Zones of the Mid-Size AM4010 Module ..... 6 - 11
6-7 Thermal Zones of the Full-Size AM4010 Module ..... 6 - 12

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Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note ...

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High Voltage Safety Instructions



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Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Warning!



This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

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It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 AdvancedTCA System Overview

The Advanced Mezzanine Card (AMC) described in this manual operates with the Advanced Telecommunications Computing Architecture (AdvancedTCA® or ATCA) and the Micro Telecommunications Computing Architecture (MicroTCA or µTCA) defined by the *PCI Industrial Computer Manufacturers Group (PICMG).* The main advantages of AdvancedTCA include high throughput, multi-protocol support, high-power capability, hot swappability, high scalability, and integrated system management. For further information regarding the AdvancedTCA/MicroTCA standards and their use, please consult the complete AdvancedTCA specification or visit the *PICMG* web site.

The Kontron AMC cards can be integrated not only on Kontron ATCA carrier boards or MicroTCA backplanes, but also on a variety of AMC-supporting ATCA and proprietary carrier boards and backplanes providing them with superior processing power and maximum design options. To learn more about the outstanding features and advantages of Kontron ATCA carrier boards, please contact Kontron or visit the Kontron web site.

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1.2 Board Overview

1.2.1 Board Introduction

The AM4010 is a highly integrated CPU board implemented as a Single Mid-size or Full-size Advanced Mezzanine Card (AMC) Module. The design is based on the Intel® Core™ Duo and the Intel® Core™ 2 Duo processors combined with the Intel® 3100 server-class chipset.

The board is capable of supporting the Intel® Core™ Duo and the Intel® Core™ 2 Duo processor versions in 65 nm technology with 64 kB L1 and up to 4 MB L2 cache in a 479 µFCBGA package with frequencies ranging from 1.2 GHz up to 1.66 GHz providing up to 667 MHz front side bus (FSB) speed. The processor and the memory are soldered on the AM4010 which results in higher Mean Time Between Failures (MTBF) and a significant improvement in cooling.

The Intel® Core™ Duo and the Intel® Core™ 2 Duo are low-power dual-core processors supporting Intel's Virtualization Technology (VT). The Intel® Core™ Duo consists of two cores and up to 2 MB L2 cache shared by both cores. The Intel® Core™ 2 Duo consists of two cores, up to 4 MB L2 cache shared by both cores, Intel® Extended Memory 64 Technology (Intel® EM64T), and enhanced address range for up to 64 GB memory. The Intel® Core™ Duo and the Intel® Core™ 2 Duo processors deliver optimized power-efficient computing and outstanding dual-core performance with low power consumption.

The board includes up to 2 GB registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running at 400 MHz. Two dual Gigabit Ethernet controllers each utilizing a x4 lane PCI Express interconnection to the Intel® 3100 chipset ensure maximum data throughput between processor and memory. The AM4010 further provides up to 4 GB Flash memory via an onboard USB 2.0 NAND Flash Controller.

The AM4010 has full hot swap capability, which enables the board to be replaced, monitored and controlled without having to shut down the ATCA carrier board or the MicroTCA system. A dedicated Module Management Controller (MMC) is used to manage the board and support a defined subset of Intelligent Platform Management Interface (IPMI) commands and PICMG (ATCA/AMC) command extensions, which enables operators to detect and eliminate faults faster at module level. This includes monitoring several onboard temperature conditions, board voltages and the power supply status, managing hot swap operations, rebooting the board, etc. All in all, IPMI enhances the board's availability and reliability while reducing the operating costs and the mean-time-to-repair.

As a "headless" AMC design (no onboard graphics controller), the AM4010 supports one USB 2.0 host interface to the front, one standard RS232 COM port, one optional Gigabit Ethernet port and a variety of high-speed interconnect topologies to the system, such as Dual Gigabit SerDes connection and Dual Serial ATA storage interface in the Common Options Region, x4 PCI Express and optional Dual Gigabit Ethernet SerDes connection in the Fat Pipes Region, and Dual Serial ATA storage interface, Debug port and Serial port in the Extended Options Region.

Optimized for high-performance, packet-based telecom systems, the AM4010 is targeted towards, but not limited to the telecom market application such as radio network controllers, media streaming, traffic processing, database management and routing. The AM4010 also fits into all applications situated in industrial environments, including I/O intensive applications. The careful design and the selection of high temperature resistant components ensure a high product availability. This, together with a high level of scalability, reliability, and stability, make this state-of-the-art product a perfect core technology for long-life embedded applications.

The board is offered with the generic Linux Board Support Package which supports various Linux distributions including the Carrier Grade Linux (CGL) operating system. Please contact Kontron for further information concerning the operation of the AM4010 with other operating systems.

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1.2.2 Board-Specific Information

Due to the outstanding features of the AM4010, such as superior processing power and flexible interconnect topologies, this AMC board provides a highly scalable solution not only for a wide range of telecom and data network applications, but also for several highly integrated industrial environment applications with solid mechanical interfacing.

Some of the AM4010's outstanding features are:

- Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
- Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
- Intel® Core™ 2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache
- Intel® 3100 chipset
- Up to 2 GB DDR2 SDRAM memory with ECC running at 400 MHz (PC3200)
- AMC interconnection
  - Dual Gigabit SerDes connection in the Common Options Region
  - Dual SATA storage interface in the Common Options Region
  - x4 PCI Express in the Fat Pipes Region (operates as a root complex controller only)
  - Dual Gigabit SerDes connection in the Fat Pipes Region (optional)
  - Dual SATA storage interface in the Extended Options Region
  - Serial port in the Extended Options Region
  - Debug port in the Extended Options Region
  - PCI Express clock reference input, FCLKA
- Full hot swap support
- One dual Gigabit Ethernet controller, 82571EB, connected to the Common Options Region
- One dual Gigabit Ethernet controller, 82571EB, connected to the Fat Pipes Region, or one single Gigabit Ethernet controller, 82572EI, connected to Front I/O
- USB 2.0 Flash Controller for up to 4 GB NAND Flash memory
- One USB 2.0 host port on Front I/O
- One Serial port on Front I/O (RS232)
- One Gigabit Ethernet port on Front I/O (optional)
- Two redundant FWH Flash chips for BIOS (2 x 1 MB)
- Dedicated IPMI Module Management Controller with redundant Firmware Flash (2 x 512 kB)
- Watchdog Timer
- JTAG interface for debugging and manufacturing
- Four bicolor Debug LEDs
- Standard temperature range: -5°C to + 55°C
- Thermal management
- Passive heat sink solution
- Single Mid-size and Full-size AMC module
- Designed to be compliant with the following specifications:
  - PICMG AMC.0, Advanced Mezzanine Card Specification R2.0
  - PICMG AMC.1, PCI Express and Advanced Switching R1.0
  - PICMG AMC.2, Gigabit Ethernet R1.0
  - PICMG AMC.3, Storage Interfaces R1.0
  - PICMG MTCA.0 Micro Telecommunications Computing Architecture R1.0
  - IPMI - Intelligent Platform Management Interface Specification, v2.0, R1.0
- AMI BIOS

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1.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the AM4010.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION

Hardware Requirements	The AM4010 can be installed on any AMC-supporting carrier board or MicroTCA backplane with the following AMC Card-edge connector port mapping:
	• Common Options Region ports 0-1
	  • Two Gigabit Ethernet SerDes ports
	• Common Options Region ports 2-3
	  • Two Serial ATA 150 ports
	• Fat Pipes Region ports 4-7
	  • One x4 PCI Express interface
	• Fat Pipes Region ports 8-9
	  • Two Gigabit Ethernet SerDes ports (optional)
	• Extended Options Region ports 12-13
	  • Two Serial ATA 150 ports
	• Extended Options Region port 14
	  • One Debug port
	• Extended Options Region port 15
	  • One Serial port
	• Clock
	  • PCI Express clock reference input, FCLKA
	For further information on the AMC interconnection, refer to section 2.4, “AMC Interconnection”.

PCI Express Configuration	The AM4010 only supports the PCI Express root complex configuration; non-transparent bridge functionality is not supported.
Operating Systems	The AM4010 is offered with the generic Linux Board Support Package which supports various Linux distributions including the Carrier Grade Linux (CGL) operating system. Please contact Kontron for further information concerning the operation of the AM4010 with other operating systems.

1.4 Board Diagrams

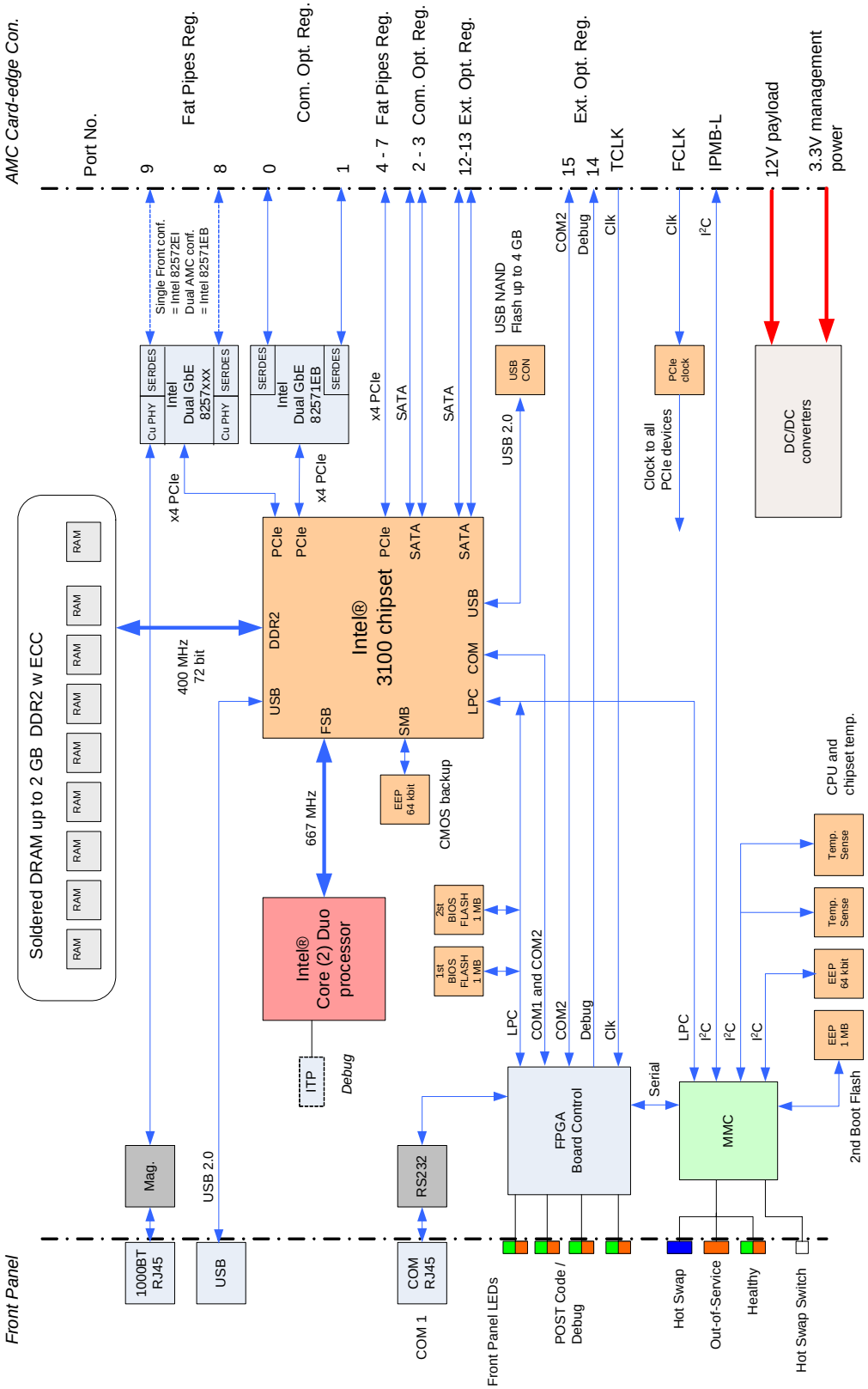
The following diagrams provide additional information concerning board functionality and component layout.

1.4.1 Functional Block Diagram

The following figure shows the block diagram of the AM4010.

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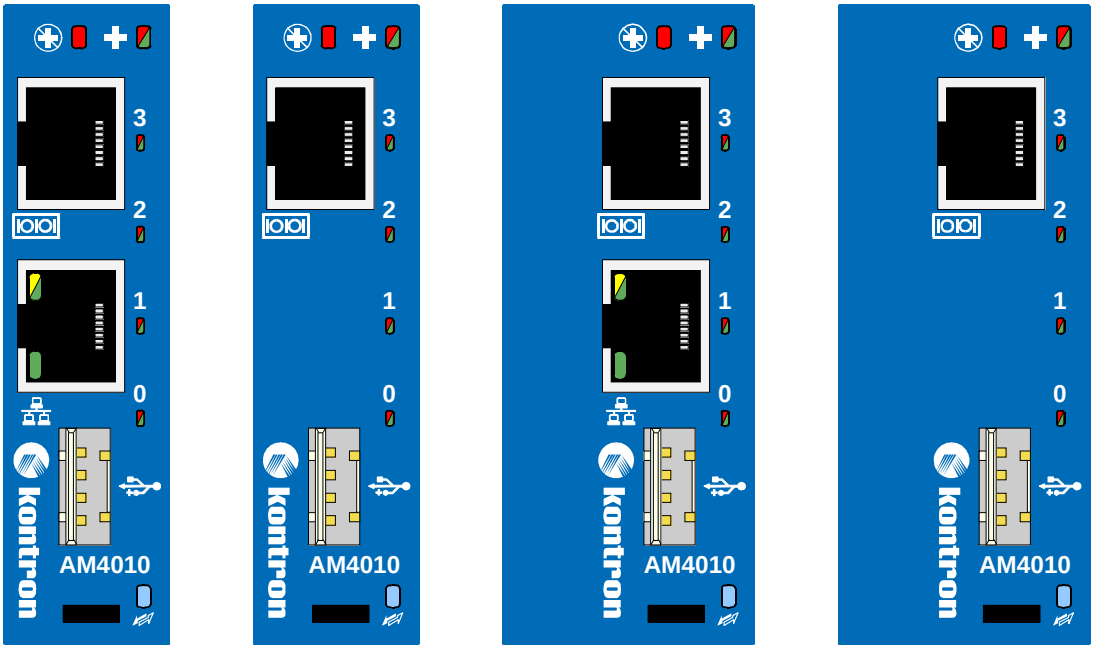
Figure 1-1: AM4010 Functional Block Diagram



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1.4.2 Front Panel

Figure 1-2: AM4010 Front Panel Versions



Mid-size front panel with GbE | Mid-size front panel without GbE | Full-size front panel with GbE | Full-size front panel without GbE

Module Management LEDs

- LED1 (red): Out-of-Service LED
- LED2 (red/green/amber): Health LED
- HS LED (blue): The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are *off*, *short blink*, *long blink*, and *on*.

User-Specific LEDs

- 3 • ULED3 (red/green/amber): AMC Eth. port A link signal status or BIOS POST code LED
- 2 • ULED2 (red/green/amber): AMC Eth. port B link signal status or BIOS POST code LED
- 1 • ULED1 (red/green/amber): Freely configurable or BIOS POST code LED
- 0 • ULED0 (red/green/amber): Freely configurable or BIOS POST code LED

Connectors

- Serial Connector
- Gigabit Ethernet Connector
- USB Connector

For further information on the LEDs used on the AM4010, refer to section 2.3.1, “Front Panel LEDs”.

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1.4.3 Board Layouts

Figure 1-3: AM4010 Board Layout (Top View)

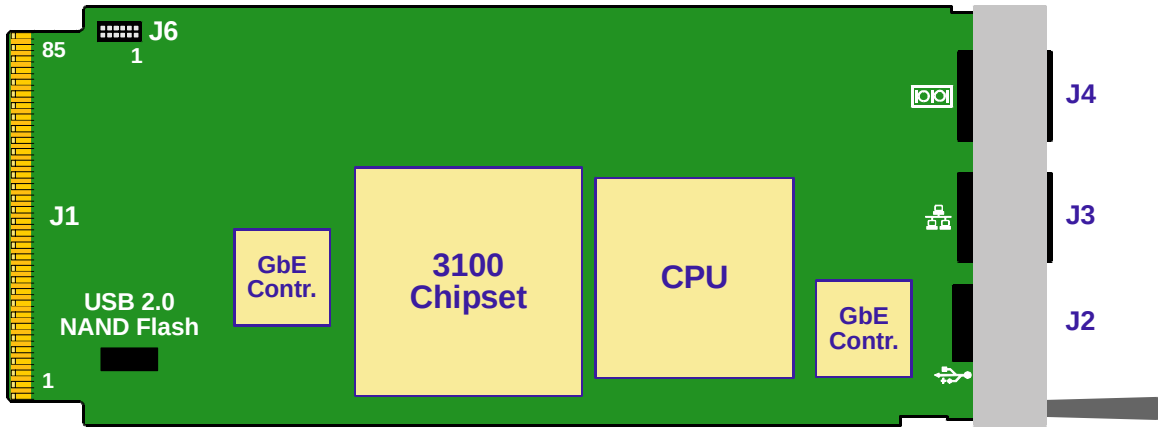
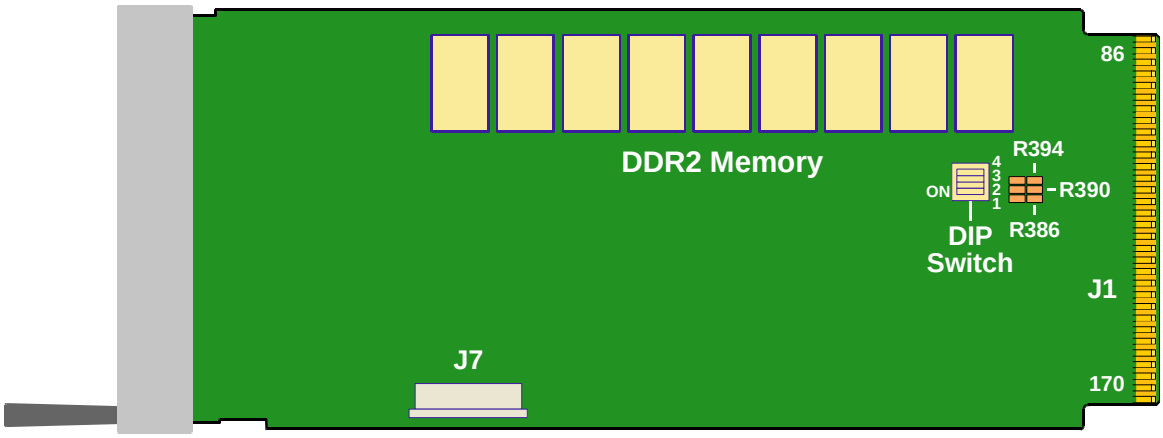


Figure 1-4: AM4010 Board Layout (Bottom View)



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1.5 Technical Specification

Table 1-2: AM4010 Main Specifications

AM4010		SPECIFICATIONS
Processor and Memory	CPU	The AM4010 supports the following microprocessors: • Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache • Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache • Intel® Core™ 2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache All microprocessors are provided in a 479 µFCBGA packaging. Please contact Kontron for further information concerning the suitability of other Intel processors for use with the AM4010.

	Memory	Main Memory:
		• Up to 2 GB registered DDR2 SDRAM memory with ECC running at 400 MHz (PC3200)
		Cache structure:
		• 64 kB L1 on-die full speed processor cache
		  • 32 kB for instruction cache
		  • 32 kB for data cache
		• Up to 4 MB L2 on-die full speed processor cache
		FLASH Memory:
		• Two redundant Firmware Hub (FWH) Flash chips (2 x 1 MB) controlled by the MMC
		Mass Storage Device:
		• Up to 4 GB NAND Flash via an onboard USB 2.0 Flash Controller
		Serial EEPROM with 64 kbit

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Table 1-2: AM4010 Main Specifications (Continued)

AM4010		SPECIFICATIONS

Chipset	Intel® 3100	Intel® 3100 chipset:
		• Support for a single Intel® Core™ Duo or Core™ 2 Duo processor
		• 64-bit AGTL/AGTL+ based System Bus interface at up to 667 MHz
		• System Memory interface with optimized support for DDR2 SDRAM memory at 400 MHz with ECC
		• Three x4 PCI Express ports
		• RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features:
		  • Memory error detection and reporting of 1- and 2-bit errors including correction of 1-bit failures
		  • Integrated Memory Scrub Engine, which logs any uncorrectable memory errors
		  • Support for automatic read retry on uncorrectable errors
		  • Memory sparing allows for one memory bank per channel to be held in reserve and brought on-line if another memory bank in the channel becomes defective (only supported with 1 GB and 2 GB main memory configuration)
		• Six-Channel SATA 150 interface (only four channels are used)
		• USB 2.0 host interface with up to four USB ports available (only two USB 2.0 ports are used on the AM4010)
		• Firmware Hub (FWH) interface support
		• Low Pin Count (LPC) interface
		• PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations (not used on the AM4010)
		• Power management logic support
		• Enhanced DMA controller, interrupt controller, and timer functions
		  • System Management Bus (SMBus) compatible with most I²C™ devices
		• Two 16550-compatible Serial ports (COM)

Onboard Controllers	Gigabit Ethernet	• Intel® 82571EB Dual Gigabit Ethernet PCI Express bus controller connected to the Common Options Region • Intel® 82571EB Dual Gigabit Ethernet PCI Express bus controller connected to the Fat Pipes Region or Intel® 82572EI Single Gigabit Ethernet PCI Express bus controller connected to Front I/O The Gigabit Ethernet controllers are provided with advanced management features such as serial redirection over LAN.

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Table 1-2: AM4010 Main Specifications (Continued)

AM4010		SPECIFICATIONS
AMC Interconnection	Gigabit Ethernet	Common Options Region ports 0-1 • Two Gigabit Ethernet SerDes ports Fat Pipes Region ports 8-9 • Two Gigabit Ethernet SerDes ports (optional)
	Serial ATA	Common Options Region ports 2-3 • Two Serial ATA 150 ports Extended Options Region ports 12-13 • Two Serial ATA 150 ports
	PCI Express	Fat Pipes Region ports 4-7 • One x4 PCI Express interface operating as a root complex controller only
	Debug Interface	Extended Options Region port 14 • One Debug port
	Serial Interface	Extended Options Region port 15 • One Serial port
	Clock Input	Clocks • PCI express clock reference input (FCLKA)
Connectors	Front Panel Connectors	• One USB 2.0 port on 4-pin connector • One Serial port (COM1) with RS232-signal level on RJ45 connector • One Gigabit Ethernet port on RJ45 connector (optional)
	AMC Card-edge Connector	• One 170-pin AMC Card-edge connector
Switches	DIP Switch	One DIP switch consisting of four switches for board configuration
LEDs	Module Management LEDs	• LED1 (red): Out-of-Service LED • LED2 (red/green/amber): Health LED • HS LED (blue): The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are *off*, *short blink*, *long blink*, and *on*.
	User-Specific LEDs	• ULED3 (red/green): AMC Ethernet port A link signal status or BIOS POST code LED. • ULED2 (red/green): AMC Ethernet port B link signal status or BIOS POST code LED. • ULED1 (red/green): Freely configurable or BIOS POST code LED • ULED0 (red/green): Freely configurable or BIOS POST code LED

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Table 1-2: AM4010 Main Specifications (Continued)

AM4010		SPECIFICATIONS
Timer	Watchdog Timer	• Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 256 s in 12 steps • Serves for generating IRQ, NMI, or hardware reset
	System Timer	• The Intel® 3100 chipset contains three 8254-style counters which have fixed uses • In addition to the three 8254-style counters, the Intel® 3100 chipset includes three individual high-precision event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register. • Hardware delay timer for short reliable delay times
IPMI	Module Management Controller	• Renesas H8 microcontroller with 40 kB RAM and redundant 512 kB Firmware Flash with automatic roll-back strategy • The MMC carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations • The MMC is accessible via a local IPMB (IPMB-L) and two host Keyboard Style Interfaces (KCS)
	Hot Swap	The AM4010 has full hot swap capability.
	Thermal Management	CPU and board overtemperature protection is provided by: • Four temperature sensors for monitoring the board temperature • Six processor sensors • One chipset sensor • Specially designed heat sinks
General	Power Consumption	For further information, refer to Chapter 5, “Power Considerations”.
	Temperature Range	Operational: -5°C to +55°C Storage: -40°C to +70°C
	Mechanical	Single Module: • Mid-size version • Full-size version
	Dimensions	Mid-size: 181.5 mm x 73.5 mm x 18.96 mm Full-size: 181.5 mm x 73.5 mm x 28.95 mm
	Board Weight	Mid-size: 262 grams (with heat sink) Full-size: 323 grams (with heat sink)
	JTAG	Two JTAG interfaces: • One processor JTAG interface routed to the onboard debug connector for debugging purposes • One onboard JTAG interface connected to the AMC Card-edge connector for debugging and manufacturing purposes

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Table 1-2: AM4010 Main Specifications (Continued)

AM4010		SPECIFICATIONS
Software	Software BIOS	AMI BIOS with 1 MB of Flash memory and having the following features: • Serial console redirection via the Serial port or LAN • QuickBoot • QuietBoot • BootBlock • LAN boot capability for diskless systems (standard PXE boot) • Boot from USB device (floppy, CD-ROM, hard disk, memory stick) • BIOS support for USB keyboards • Plug and Play capability • BIOS parameters are saved in the EEPROM • Board serial number is saved within the EEPROM • ACPI
	Software IPMI	Module Management Controller Firmware providing the following features: • The MMC is accessible via IPMB-L and two KCS interfaces with interrupt support • The MMC Firmware can be updated in field through all supported interfaces using the Kontron FirmWare Upgrade Manager (FWUM) • Two MMC Flash banks with automatic roll-back capability in case of an upgrade Firmware failure • Board supervision and control extensions such as board reset, power and Firmware Hub Flash control, and boot order configuration
	Operating Systems	The AM4010 is offered with the generic Linux Board Support Package which supports various Linux distributions including the Carrier Grade Linux (CGL) operating system. Please contact Kontron for further information concerning the operation of the AM4010 with other operating systems.

1.6 Kontron Software Support

Kontron is one of the few AdvancedTCA and CompactPCI vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *Kontron* is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with *Kontron* can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

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1.7 Standards

The *Kontron* AMC boards comply with the requirements of the following standards.

Table 1-3: Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3 EN300386	--
	Immission	EN55024 EN61000-6-2 EN300386	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental and Health Aspects	Vibration (sinusoidal)	IEC60068-2-6	5-150 [Hz] / 1 [g] / 1 [oct/min] 10 [cycles/axis] 3 [directions: x,y,z]
	Vibration (sinusoidal, transportation)	IEC60068-2-6	2-50 [Hz] / 1 [g] / 0.1 [oct/min] 50-500 [Hz] / 3 [g] / 0.25 [oct/min] 10 [cycles/axis] 3 [directions: x,y,z]
	Shock (operating)	IEC60068-2-27	4 [g] 22 [ms] 3 [shocks per direction] 5 [s] recovery time 6 [directions, ±x, ±y, ±z]
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment

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1.8 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
ATCA	PICMG® 3.0 AdvancedTCA Base Specification R2.0, March 18, 2005
MicroTCA	PICMG® MTCA.0 Micro Telecommunications Computing Architecture R1.0, July 6, 2006
AMC	PICMG® AMC.0, Advanced Mezzanine Card Specification R2.0 PICMG® AMC.1, PCI Express and Advanced Switching R1.0 PICMG® AMC.2, Gigabit Ethernet R1.0 PICMG® AMC.3, Storage Interfaces R1.0
IPMI	IPMI - Intelligent Platform Management Interface Specification, v2.0 Document Revision 1.0, February 12, 2004 IPMI - Platform Management FRU Information Storage Definition, V1.0 Document Revision 1.1, September 27, 1999
PCI Express	PCI Express Base Specification Revision 1.0a
Serial ATA	Serial ATA 2.5 Specification

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The AM4010 supports the latest Intel® Core™ Duoand Intel® Core™ 2 Duo processor family up to speeds of 1.66 GHz with up to 667 MHz FSB, such as:

- Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
- Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
- Intel® Core™ 2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache

The Intel® Core™ Duo consists of two cores and up to 2 MB L2 cache shared by both cores. The Intel® Core™ 2 Duo consists of two cores, up to 4 MB L2 cache shared by both cores, Intel® Extended Memory 64 Technology (Intel® EM64T), and enhanced address range for up to 64 GB memory. The Intel® Core™ Duo and the Intel® Core™ 2 Duo processors deliver optimized power-efficient computing and outstanding dual-core performance with low power consumption.

The Intel® Core™ Duo and the Intel® Core™ 2 Duo support the latest Intel's Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions, such as performing system upgrades and maintenance without interrupting the system or the application, keeping software loads and virus attacks separate, combining multiple servers in one system, etc. With processor and I/O enhancements to Intel's various platforms, Intel Virtualization Technology improves the performance and robustness of today's software-only virtual machine solutions.

Furthermore, the Intel® Core™ Duo and the Intel® Core™ 2 Duo processors also support the Intel® SpeedStep® technology which enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. The frequency for the processor may also be selected in the BIOS or via the operating system.

The following list sets out some of the key features of the Intel® Core™ Duo and the Intel® Core™ 2 Duo processors:

- Outstanding dual-core performance with low power consumption
- Support of Intel's Virtualization Technology (Vanderpool)
- Support of Intel Architecture with Dynamic Execution
- On-die, primary 32 kB instruction cache and 32 kB write-back data cache
- On-die, L1 and L2 cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 3 (SSE3)
- Up to 667 MHz, Source-Synchronous Front Side Bus (FSB)
- Advanced Power Management features including Enhanced Intel® SpeedStep® technology
- Intel® Extended Memory 64 Technology for 64-bit computing (only with Intel® Core™ 2 Duo)

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2.1.2 Memory

The AM4010 supports a single-channel (72-bit), registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running at 400 MHz (PC3200). The available memory configuration can be either 1 GB or 2 GB.

There are several Reliability, Availability, Serviceability, Usability, and Manageability (RASUM) features available for the memory interface:

- Memory error detection and reporting of 1 and 2 bit errors and correction of 1 bit failures
- Integrated Memory Scrub Engine, the scrub engine logs any uncorrectable memory error
- Support for automatic read retry on uncorrectable errors
- Memory sparing allows for one memory bank per channel to be held in reserve and brought on-line if another memory bank in the channel becomes defective.

2.1.3 Intel® 3100 Chipset

The AM4010 is equipped with the Intel® 3100 chipset which combines server-class memory and I/O controller hub functions into a single component with the following features:

- CPU interface up to 667 MHz FSB
- Single-channel registered DDR2 SDRAM system memory interface with ECC
- Three x4 PCI Express interfaces
- Six-Channel Serial ATA 150 interfaces (only four channels are used)
- USB 2.0 host interface with up to four USB ports available (only two USB 2.0 ports are used on the AM4010)
- Firmware Hub interface support
- Low Pin Count interface
- PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations (not used on the AM4010)
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- System Management Bus (SMBus) compatible with most I²C™ devices
- RTC controller
- Two 16550-compatible Serial ports (COM)

2.2 Peripherals

The following standard peripherals are available on the AM4010 board:

2.2.1 Timer

The AM4010 is equipped with the following timers:

- Real-Time Clock
  The Intel® 3100 chipset integrates a MC146818A compatible real-time clock with 256 Byte CMOS RAM. The AM4010 does not include a dedicated 3V lithium battery power source for RTC backup. Alternatively, the RTC can be powered from the management power. But, if the power is switched off, the RTC will lose its data. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.
- Counter/Timer
  Three 8254-style counter/timers are included on the AM4010 as defined for the PC/AT.
- Three High Precision Event Timers (HPET)

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The 3100 chipset includes three High Precision Event Timers (HPET) that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.

- Hardware delay timer for short reliable delay times

2.2.2 Watchdog Timer

The AM4010 provides a Watchdog Timer that is programmable for a timeout period ranging from 125 ms to 256 s in 12 steps. Failure to trigger the Watchdog Timer in time results in a system reset, an interrupt, or NMI. In the dual-stage mode, a combination of both NMI, and reset if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog Timer generated the reset.

2.2.3 Battery

The AM4010 does not provide a battery. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.

2.2.4 Power Monitor and Reset Generation

All onboard voltages on the AM4010 are supervised, which guarantees controlled power-up of the board. This is done by activating a stable power-up reset signals after the threshold voltages have been passed.

2.2.5 FLASH Memory

There are three Flash devices available as described below, two for the BIOS and one for the USB 2.0 NAND Flash Controller.

2.2.5.1 BIOS FLASH (Firmware Hub)

The AM4010 provides two redundant Firmware Hub Flash chips (2 x 1 MB). The fail-over mechanism for the BIOS recovery can be controlled via the MMC controller or the DIP switch.

If one Firmware Hub Flash is corrupted, the MMC can enable the second Firmware Hub Flash and boot the system again.

The Firmware Hub Flash includes a hardware write protection option, which can be configured via the BIOS. If write protection is enabled, the Firmware Hub Flash cannot be written to.

2.2.5.2 USB 2.0 NAND Flash Controller

The AM4010 supports up to 4 GB of NAND Flash in combination with a dedicated USB 2.0 NAND Flash module, which is connected to the USB 2.0 port of the Intel® 3100 chipset.

The USB NAND Flash module is a USB 2.0 based NAND Flash drive with a built-in full hard-disk emulation and a high data transfer rate (sustained read rate with up to 25 MB/sec and sustained write rate with up to 20 MB/sec). It is optimized for embedded systems providing high-performance, reliability and security.

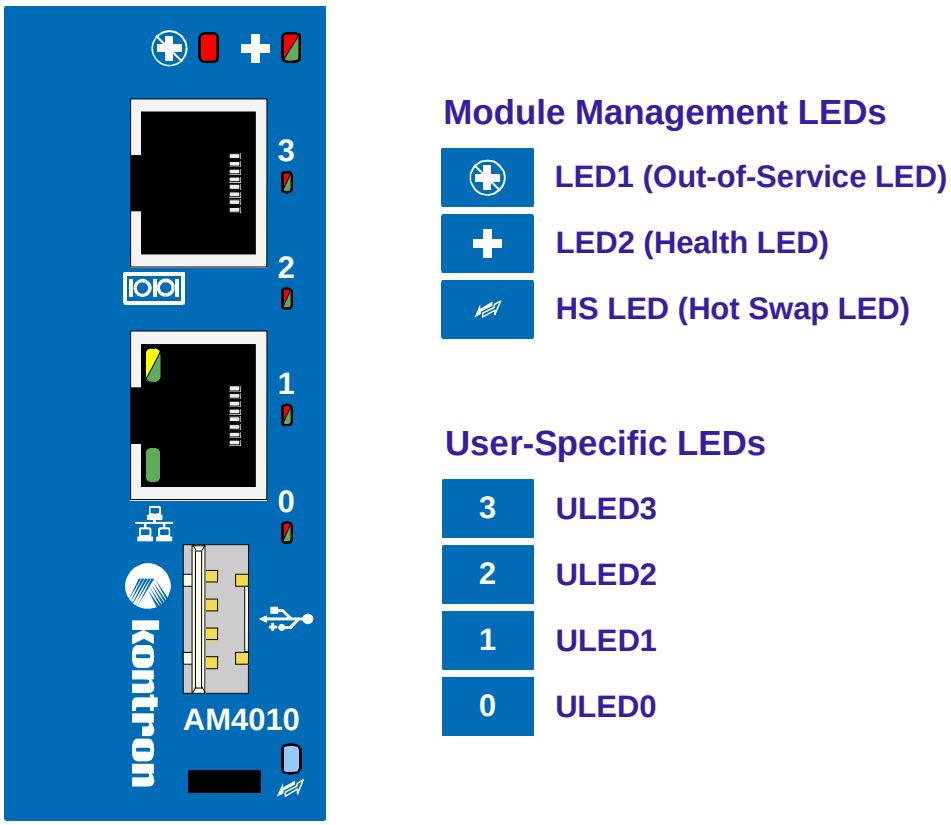
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2.3 Board Interfaces

2.3.1 Front Panel LEDs

The AM4010 is equipped with three Module Management LEDs and four User-Specific LEDs. The User-Specific LEDs can be configured via two onboard registers (see section 4.4.12, “User-Specific LED Configuration Register”).

Figure 2-1: Front Panel LEDs



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Table 2-1: Module Management LED Function

MODULE MANAGEMENT LED	COLOR	NORMAL MODE	OVERRIDE MODE state selectable by user or carrier, depending on PICMG LED command	DEBUG MODE state selectable by IPMI OEM command
LED1	red	Off = default	Depends on carrier or user	--
		On = MMC in reset state (the MMC does not operate)		
		Blinking = MMC upgrade		

LED2	red	--	Depends on carrier or user	4 time slots:
				• 1st time slot: amber
				  • One Serial port
				  • Heartbeat
				• 2nd time slot: green
				  • On = IPMB-L active
				  • Off = IPMB-L not active
				• 3rd time slot: green
				  • On = KCI interface active
				  • Off = KCI interface not active
				• 4th time slot: green
				  • On = Message waiting for SMS/MMS
				  • Off = Message not waiting for SMS/MMS

	green	On = default (IPMI sensor aggregation)		
	amber	On = fail (IPMI sensor aggregation)		
HS LED	blue	On = ready for hot swap Blinking = how swap in progress	By carrier: • On • Off • Slow/Fast Blinking By user: • Only lamp test	--

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Table 2-2: User-Specific LED Function

USER-SPECIFIC LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING BIOS POST (if POST code config. is enabled)	DEFAULT FUNCTION AFTER BOOT-UP
ULED3	red	When lit up during boot-up, it indicates a power failure.	--	processor overtemperature above 125 °C (blinking) and processor overtemperature above 100 °C
	green	--	BIOS POST bit 3 and bit 7	AMC Ethernet port A link signal status
ULED2	red	When lit up during boot-up, it indicates a clock failure	--	processor overtemperature above 125 °C (blinking) and chipset overtemperature above 105 °C
	green	--	BIOS POST bit 2 and bit 6	AMC Ethernet port B link signal status
ULED1	red	When lit up during boot-up, it indicates a hardware reset.	--	processor overtemperature above 125 °C (blinking)
	green	--	BIOS POST bit 1 and bit 5	freely configurable (host or MMC)*
	red+green	--	--	freely configurable (host or MMC)*
ULED0	red	When lit up during boot-up, it indicates a BIOS boot failure	--	processor overtemperature above 125 °C (blinking)
	green	--	BIOS POST bit 0 and bit 4	freely configurable (host or MMC)*
	red+green	When lit up during boot-up, it indicates a BIOS boot failure	--	freely configurable (host or MMC)*

* Fur further information on the freely configurable LEDs, refer to section 4.4.12, “User-Specific LED Configuration Register”.

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How to Read the 8-Bit POST Code

Due to the fact that only 4 bits are available and 8 bits must be displayed, the User-Specific LEDs are multiplexed.

The following is an example of the User-Specific LEDs' operation if BIOS POST configuration is enabled (see also Table 2-2, "User-Specific LED Function").

Table 2-3: POST Code Example

STATE	USER-SPECIFIC LEDs
0	All User-Specific LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0



Note ...

Under normal operating conditions, the User-Specific LEDs should not remain lit during boot-up. They are intended to be used only for debug purposes. In the event that a User-Specific LED lights up during boot-up and the AM4010 does not boot, please contact the Kontron's Technical Support.

If all User-Specific LEDs flash red on and off at regular intervals, they indicate that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Once activated, the overtemperature event remains latched until a cold restart of the AM4010 is undertaken (all power off and then on again).

2.3.2 General Purpose DIP Switch

The AM4010 is equipped with a general purpose 4-bit DIP switch which enables the user to configure the AM4010 according to his individual needs.

The following table indicates the functions of the four switches integrated in the DIP switch.

Table 2-4: DIP Switch Functions

SWITCH	FUNCTION
1	POST code display during bootup
2	BIOS Firmware Hub configuration
3	Set the default boot order configuration
4	Clearing BIOS CMOS parameters

For further information on the DIP switch configuration, refer to section 4.1, "DIP Switch Configuration".

2.3.3 Debug Interface

The AM4010 provides several onboard options for hardware and software debugging, such as:

- Four bicolor debug LEDs for signaling hardware failures and BIOS POST code
- An optional ITP700 (processor JTAG) connector J9 is included to facilitate debug and BIOS software development.

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2.3.4 USB Host Interface

The AM4010 supports one high-speed, full-speed, and low-speed capable USB 2.0 host port on the front I/O via the 4-pin USB connector, J2. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s.

The following figure and table provide pinout information on the USB port connector, J2.

Figure 2-2: USB Connector J2

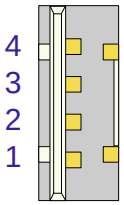


Table 2-5: USB Connector J2 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--



Note ...

The AM4010 host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.3.5 Serial Ports

The AM4010 provides two Serial ports, COM 1 and COM2, both fully compatible with the 16550 controller.

The COM1 interface includes a complete set of handshaking signals. Data transfer rates up to 115.2 kB/s are supported. COM1 is available on the front panel as a serial RS232, 8-pin, RJ45, connector J4.

The COM2 interface includes only receive and transmit signals. Data transfer rates up to 115.2 kB/s are supported. COM2 is available on the AMC port 15 in the Extended Options Region of the AMC Card-edge Connector as TTL 3.3 V signal level.

The following figure and table provide pinout information on the serial port connector J4.

Figure 2-3: Serial Con. J4 (COM1)

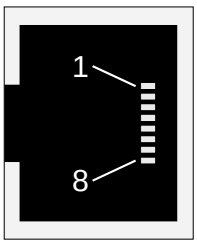


Table 2-6: Serial Con. J4 (COM1) Pinout

PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data send ready	I
8	CTS	Clear to send	I

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2.3.6 Gigabit Ethernet Interfaces

The AM4010 supports up to four Gigabit Ethernet interfaces using either the Intel 82571EB dual Gigabit Ethernet controller or the Intel 82572EI single Gigabit Ethernet controller. Two Gigabit Ethernet configurations are available on the AM4010:

- **Configuration with three Gigabit Ethernet interfaces**
  In this configuration one Gigabit Ethernet copper port (1000BASE-TX) is connected to the RJ45 front panel connector and two Gigabit Ethernet SerDes ports are routed to the AMC ports 0-1 in the Common Options Region of the AMC Card-edge Connector.
  This configuration is based on one Intel 82572EI controller (1000BASE-TX) and one Intel 82571EB controller.
- **Configuration with four Gigabit Ethernet interfaces**
  In this configuration two Gigabit Ethernet SerDes ports are routed to the AMC ports 0-1 in the Common Options Region of the AMC Card-edge Connector and two additional Gigabit Ethernet SerDes ports are routed to the AMC ports 8-9 in the Fat Pipes Region of the AMC Card-edge Connector.
  This configuration is based on two Intel 82571EB controllers.

The Intel® 82571EB Dual Gigabit Ethernet Controller and the Intel® 82572EI single Gigabit Ethernet controller are optimized to deliver high performance data throughput with the lowest power consumption. The controller's architecture includes a large packet buffer (48 kB per port) which maintains superior performance. The Ethernet controllers are directly connected to the Intel® 3100 chipset using two x4 PCI Express ports.

An additional management feature provided by the controller is serial-over-LAN redirection via the PCI Express interface. In the serial-over-LAN redirection, the 82571EB/82572EI looks like a regular serial controller (COM) and the BIOS can send all serial packets to the remote console over LAN. The Boot from LAN feature is supported. The 82571EB supports IPMI-over-LAN as well. For information on IPMI, refer to the AM4010-IPMI, MMC User Manual software manual provided with the software and documentation CD.

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2.3.6.1 Gigabit Ethernet Connector

The Ethernet connector is realized as RJ45 connector. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

The J3 connector supplies the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Figure 2-4: Gigabit Ethernet Connector J3

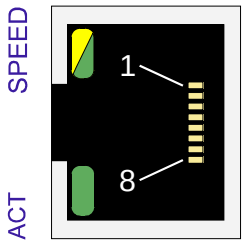


Table 2-7: Gigabit Ethernet Connector J3 Pinout Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

SPEED (green/yellow): This LED lights up to indicate a successful 100Base-TX or 1000BASE-T connection. When green it indicates a 100Base-TX connection and when yellow it indicates a 1000Base-T connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.

2.3.7 Serial ATA Interface

The AM4010 provides up to four SATA 1.0a interfaces running at 1.5 Gbit/s. All four ports are logically connected to the Intel® 3100 chipset. Two SATA ports are connected to the AMC ports 2-3 in the Common Options Region of the AMC Card-edge Connector. The other two SATA ports are connected to the AMC ports 12-13 in the Extended Options Region of the AMC Card-edge Connector.

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2.4 AMC Interconnection

The AM4010 communicates with the carrier board or the MicroTCA backplane via the AMC Card-edge Connector, which is a serial interface optimized for high-speed interconnects. The AMC Card-edge Connector supports a variety of fabric topologies divided into five functional groups:

- Fabric interface
- Synchronization clock interface
- System management interface
- JTAG interface
- Module power interface

The following sections provide detailed information on these interfaces.

2.4.1 Fabric Interface

The Fabric interface is the real communication path and comprises 20 high-speed ports providing point-to-point connectivity for module-to-carrier and module-to-module implementations. The high-speed ports are separated in three logical regions as follows:

- Common Options Region
- Fat Pipes Region
- Extended Options Region

The AM4010 Port Mapping is described below and illustrated in figure 2-5.

- Common Options Region
  - Ports 0-1: two redundant Gigabit Ethernet SerDes ports
  - Ports 2-3: two Serial ATA 150 ports
- Fat Pipes Region
  - Ports 4-7: one x4 PCI Express interface operating as a root-complex only
  - Ports 8-9: two redundant Gigabit Ethernet SerDes ports (optional)
- Extended Options Region
  - Ports 12-13: two Serial ATA 150 ports
  - Port 14: one Debug port
  - Port 15: one Serial port

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Figure 2-5: AM4010 Port Mapping

	Port No.	AMC Standard Port Mapping	AM4010 Port Mapping
Basic Connector	TCLKA	Clocks	System Tick (optional)
	TCLKB		not used
	FCLKA		PCI Express Reference Clock
	0	Common Options Region	GbE-A
	1		GbE-B
	2		SATA-A
	3		SATA-B
	4	Fat Pipes Region	x4 PCI Express
	5		
	6		
	7		
Extended Connector	8	Fat Pipes Region	GbE-C (optional)
	9		GbE-D (optional)
	10		not used
	11		
	12	Extended Options Region	SATA-C
	13		SATA-D
	14		Debug
	15		Serial (COM2)
	TCLKC/D		not used
	17		
	18		
	19		
	20		

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2.4.2 Synchronization Clock Interface

On the AM4010, two PCI Express reference clock configurations are supported in accordance with the PCI Express Base Specification Revision 1.0a. One configuration uses two separate 100 MHz reference clocks, one on the AM4010 and one on the carrier. The other configuration uses one common clock source for both the AM4010 and the carrier. If the common clock source is used, the AM4010 uses the AMC clock interface FCLKA (see Figure 2-5, “AM4010 Port Mapping”). In this event, the carrier must provide the common reference clock (100 MHz) on the FCLKA pins.



Note ...

Clock spectrum modulation in the BIOS setup can be used only in the common clock configuration. If clock spectrum configuration is enabled, all onboard devices are operating in clock spectrum mode.

2.4.3 System Management Interface

The system management interface is a port from the module to the carrier via the Local Intelligent Platform Management Bus (IPMB-L). The Module Management Controller uses this port for the communication with the carrier Intelligent Platform Management Controller (IPMC). The IPMB-L is a multi-master I^2C bus.

2.4.4 JTAG Interface

JTAG support is provided on the AMC edge connector. The JTAG interface is supported for vendor product test and logic update.

On the AM4010, the FPGA JTAG port is connected to the AMC JTAG port.

2.4.5 Module Power Interface

The module power interface provides the management power (MP) and payload power (PWR). These two supply voltages must have power-good indicators so that the system management can detect boot sequence events and nominal operating conditions.

The AM4010 operates with payload power in the range of 10.8 V to 13.2 V, and with management power of 3.3 V ± 5%.

The board supports removal and insertion in a powered slot as required by AMC.0.

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2.4.6 Pinout of AMC Card-edge Connector J1

The AMC edge connector is a high-speed serial interface and supports 170 pins. The following table provides the pinout of the AMC edge connector J1. The shaded table cells indicate signals that are not used on the AM4010

Table 2-8: Pinout of AMC Edge Connector J1

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
1	GND	Logic Ground	-	170	GND	Logic Ground	-
2	PWR	Payload Power	Carrier	169	TDI	JTAG Test Data Input	Carrier
3	PS1#	Presence 1	AMC	168	TDO	JTAG Test Data Output	AMC
4	MP	Management Power	Carrier	167	TRST#	JTAG Test Reset Input	Carrier
5	GA0	Geographic Address 0	Carrier	166	TMS	JTAG Test Mode Select In	Carrier
6	RSV	Reserved (Optional PCIe Reset Output)	AMC	165	TCK	JTAG Test Clock Input	Carrier
7	GND	Logic Ground	-	164	GND	Logic Ground	-
8	RSV	Reserved	-	163	Tx20+	Not Connected	AMC
9	PWR	Payload Power	Carrier	162	Tx20-	Not Connected	AMC
10	GND	Logic Ground	-	161	GND	Logic Ground	-
11	Tx0+	GbE-A Transmitter +	AMC	160	Rx20+	Not Connected	Carrier
12	Tx0-	GbE-A Transmitter -	AMC	159	Rx20-	Not Connected	Carrier
13	GND	Logic Ground	-	158	GND	Logic Ground	-
14	Rx0+	GbE-A Receiver +	Carrier	157	Tx19+	Not Connected	AMC
15	Rx0-	GbE-A Receiver	Carrier	156	Tx19-	Not Connected	AMC
16	GND	Logic Ground	-	155	GND	Logic Ground	-
17	GA1	Geographic Address 1	Carrier	154	Rx19+	Not Connected	Carrier
18	PWR	Payload Power	Carrier	153	Rx19-	Not Connected	Carrier
19	GND	Logic Ground	-	152	GND	Logic Ground	-
20	Tx1+	GbE-B Transmitter +	AMC	151	Tx18+	Not Connected	AMC
21	Tx1-	GbE-B Transmitter -	AMC	150	Tx18-	Not Connected	AMC
22	GND	Logic Ground	-	149	GND	Logic Ground	-
23	Rx1+	GbE-B Receiver +	Carrier	148	Rx18+	Not Connected	Carrier
24	Rx1-	GbE-B Receiver -	Carrier	147	Rx18-	Not Connected	Carrier
25	GND	Logic Ground	-	146	GND	Logic Ground	-
26	GA2	Geographic Address 2	Carrier	145	Tx17+	Not Connected	AMC
27	PWR	Payload Power	Carrier	144	Tx17-	Not Connected	AMC
28	GND	Logic Ground	-	143	GND	Logic Ground	-

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Table 2-8: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
29	Tx2+	SATA-A Transmitter +	AMC	142	Rx17+	Not Connected	Carrier
30	Tx2-	SATA-A Transmitter -	AMC	141	Rx17-	Not Connected	Carrier
31	GND	Logic Ground	-	140	GND	Logic Ground	-
32	Rx2+	SATA-A Receiver +	Carrier	139	TCLKD+	Not Connected	AMC
33	Rx2-	SATA-A Receiver -	Carrier	138	TCLKD-	Not Connected	AMC
34	GND	Logic Ground	-	137	GND	Logic Ground	-
35	Tx3+	SATA-B Transmitter +	AMC	136	TCLKC+	Not Connected	Carrier
36	Tx3-	SATA-B Transmitter -	AMC	135	TCLKC-	Not Connected	Carrier
37	GND	Logic Ground	-	134	GND	Logic Ground	-
38	Rx3+	SATA-B Receiver +	Carrier	133	Tx15+	Not Connected	AMC
39	Rx3-	SATA-B Receiver -	Carrier	132	Tx15-	Not Connected	AMC
40	GND	Logic Ground	-	131	GND	Logic Ground	-
41	ENABLE#	AMC Enable	Carrier	130	Rx15+	Serial Port Receive	Carrier
42	PWR	Payload Power	Carrier	129	Rx15-	Serial Port Transmit	AMC
43	GND	Logic Ground	-	128	GND	Logic Ground	-
44	Tx4+	PCIe-0 Transmitter +	AMC	127	Tx14+	Debug serial data output	AMC
45	Tx4-	PCIe-0 Transmitter -	AMC	126	Tx14-	Debug serial clock output	AMC
46	GND	Logic Ground	-	125	GND	Logic Ground	-
47	Rx4+	PCIe-0 Receiver +	Carrier	124	Rx14+	Not Connected	Carrier
48	Rx4-	PCIe-0 Receiver -	Carrier	123	Rx14-	Not Connected	Carrier
49	GND	Logic Ground	-	122	GND	Logic Ground	-
50	Tx5+	PCIe-1 Transmitter +	AMC	121	Tx13+	SATA-D Transmitter +	AMC
51	Tx5-	PCIe-1 Transmitter -	AMC	120	Tx13-	SATA-D Transmitter -	AMC
52	GND	Logic Ground	-	119	GND	Logic Ground	-
53	Rx5+	PCIe-1 Receiver +	Carrier	118	Rx13+	SATA-D Receiver +	Carrier
54	Rx5-	PCIe-1 Receiver -	Carrier	117	Rx13-	SATA-D Receiver -	Carrier
55	GND	Logic Ground	-	116	GND	Logic Ground	-
56	SCL_L	IPMB-L Clock	IPMI Agent	115	Tx12+	SATA-C Transmitter +	AMC
57	PWR	Payload Power	Carrier	114	Tx12-	SATA-C Transmitter -	AMC
58	GND	Logic Ground	-	113	GND	Logic Ground	-
59	Tx6+	PCIe-2 Transmitter +	AMC	112	Rx12+	SATA-C Receiver +	Carrier

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Table 2-8: Pinout of AMC Edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
60	Tx6-	PCIe-2 Transmitter -	AMC	111	Rx12-	SATA-C Receiver -	Carrier
61	GND	Logic Ground	-	110	GND	Logic Ground	-
62	Rx6+	PCIe-2 Receiver +	Carrier	109	Tx11+	Not Connected	AMC
63	Rx6-	PCIe-2 Receiver -	Carrier	108	Tx11-	Not Connected	AMC
64	GND	Logic Ground	-	107	GND	Logic Ground	-
65	Tx7+	PCIe-3 Transmitter +	AMC	106	Rx11+	Not Connected	Carrier
66	Tx7-	PCIe-3 Transmitter -	AMC	105	Rx11-	Not Connected	Carrier
67	GND	Logic Ground	-	104	GND	Logic Ground	-
68	Rx7+	PCIe-3 Receiver +	Carrier	103	Tx10+	Not Connected	AMC
69	Rx7-	PCIe-3 Receiver -	Carrier	102	Tx10-	Not Connected	AMC
70	GND	Logic Ground	-	101	GND	Logic Ground	-
71	SDA_L	IPMB-L Data	IPMI Agent	100	Rx10+	Not Connected	Carrier
72	PWR	Payload Power	Carrier	99	Rx10-	Not Connected	Carrier
73	GND	Logic Ground	-	98	GND	Logic Ground	-
74	TCLKA+	Telecom Clock A+ (optional)	Carrier	97	Tx9+	GbE-D Transmitter +	AMC
75	TCLKA-	Telecom Clock A- (optional)	Carrier	96	Tx9-	GbE-D Transmitter -	AMC
76	GND	Logic Ground	-	95	GND	Logic Ground	-
77	TCLKB+	Not Connected	AMC	94	Rx9+	GbE-D Receiver +	Carrier
78	TCLKB-	Not Connected	AMC	93	Rx9-	GbE-D Receiver -	Carrier
79	GND	Logic Ground	-	92	GND	Logic Ground	-
80	FCLKA+	PCIe Reference Clock +	Carrier	91	Tx8+	GbE-C Transmitter +	AMC
81	FCLKA-	PCIe Reference Clock -	Carrier	90	Tx8-	GbE-C Transmitter -	AMC
82	GND	Logic Ground	-	89	GND	Logic Ground	-
83	PS0#	Presence 0	Carrier	88	Rx8+	GbE-C Receiver +	Carrier
84	PWR	Payload Power	Carrier	87	Rx8-	GbE-C Receiver -	Carrier
85	GND	Logic Ground	-	86	GND	Logic Ground	-



Warning!

When handling the board, take care not to touch the gold conductive fingers of the AMC Card-edge connector.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

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The following table lists the reserved pins, which must not be connected to external circuitry.

Table 2-9: Reserved Pins Description

AMC PIN	AMC PORT	FUNCTION	I/O	SIGNALING VOLTAGE
6	--	Optional PCI Express reset output	O	3.3V TTL level
8	--	Reserved input for general purpose	I	3.3V TTL level



Warning!

The reserved pins listed above are reserved for optional use and must not be connected to external circuitry.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

The following table lists the Extended Options Regions pins:

Table 2-10: Extended Options Region Pins Description

AMC PIN	AMC PORT	FUNCTION	I/O	SIGNALING VOLTAGE
130	15	Rx serial port (COM2)	I	3.3V TTL level
129	15	Tx serial port (COM2)	O	3.3V TTL level
127	14	Debug serial data output	O	3.3V TTL level
126	14	Debug serial clock output	O	3.3V TTL level



Note ...

The Extended Options Region pins listed above are not differential signals. They have 3.3V TTL signaling voltage.

The following table lists the JTAG pins:

Table 2-11: JTAG Pins Description

AMC PIN	SIGNAL	FUNCTION	I/O	SIGNALING VOLTAGE
169	TDI	JTAG Test Data Input	I	3.3V TTL level
168	TDO	JTAG Test Data Output	O	3.3V TTL level
167	TRST#	JTAG Test Reset Input	I	3.3V TTL level
166	TMS	JTAG Test Mode Select In	I	3.3V TTL level
165	TCK	JTAG Test Clock Input	I	3.3V TTL level



Note ...

The JTAG pins are connected to the onboard FPGA logic and can be used to update the onboard logic. For further information, contact Kontron's Technical Support.

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2.5 Module Management

A dedicated Module Management Controller (MMC) on the AM4010 manages the module and supports a defined subset of IPMI commands and sensors. For information on IPMI, refer to the AM4010-IPMI, MMC User Manual software manual provided with the software and documentation CD.

2.5.1 Module Management Controller

The Module Management Controller is based on the 16-bit H8 microcontroller with two redundant 512 kB Flash blocks and 40 kB RAM. The two redundant 512 kB Flash blocks provide an automatic roll-back strategy to the backup copy, for example, if a Firmware upgrade is interrupted or corrupted. In addition to the code Flash, the field replacement unit (FRU) inventory information is stored in the nonvolatile memory on the EEPROM. It is possible to store up to 4 KB within the FRU inventory information.

The processor communicates with the MMC using the Keyboard Controller Style (KCS) interface. The base address of the LPC KCS interface is 0xCA2 - 0xCA3 and 0xCA4 - 0xCA5. Furthermore, the MMC is able to communicate directly with the FPGA via the I²C interface. This can be used to read the POST codes and configure the BIOS default boot parameters.

The MMC is used to manage the AM4010, for example, it monitors several onboard temperature conditions, board voltages and the power supply status, manages hot swap LEDs and operations, reboots the board, etc. Additionally, the MMC can intervene in the operating status of the system by reading temperature values, shutting down systems, generating alarm signals if fault conditions occur. These fault conditions are simultaneously logged in nonvolatile memory for analysis and for fault recovery.

To provide a reliable system, the AM4010 includes six temperature sensors distributed over the complete board to measure onboard temperature values and regulate the board's power consumption. The AM4010 uses the following temperature sensors:

- Inlet board temperature sensor near the AMC Card-edge connector (Inlet AMC Sensor)
- Outlet board temperature sensor near the AMC Card-edge connector (Outlet AMC Sensor)
- Inlet board temperature sensor near the processor (Inlet Processor Sensor)
- Outlet board temperature sensor near the processor (Outlet Processor Sensor)
- Intel® Core™ Duo and Intel® Core™ 2 Duo processor die temperature sensor
- Intel® 3100 chipset die temperature sensor

The MMC also includes an integrated Watchdog to protect against CPU lockups. This enhances the board's characteristics and improves the system's reliability.

The MMC Firmware is designed and specially made for AMC environments, and is compliant with the PICMG 3.0 and IPMI v2.0 rev 1.0 specifications.

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2.5.1.1 MMC Signals Implemented on the AM4010

The MMC implements several signals to monitor and control the different board functions. The following tables indicate the signals implemented on the AM4010.

Table 2-12: Processor and Chipset Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
PCI reset	Status of PCI reset signal	Monitor reset status
Board reset	Reset the complete board	Control reset circuit
S3 Sleep state	Status of chipset sleep state	Monitor sleep state
Processor NMI	Status of processor NMI	Monitor NMI
Processor SMI	Status of processor SMI	Monitor SMI
FWH Flash control	FWH Flash fail-over control	Control FWHs
Post Code	BIOS POST code information	Monitor BIOS
Boot order	Configure BIOS boot order	Configure boot

Table 2-13: AMC-Specific Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
GA[0:2]	Geographic address	Monitor and control
Hot swap LED	Hot swap LED	Control LED
Hot swap switch	Status of hot swap switch	Monitor switch
User-Specific LED	Basic feedback about failures	Control User-Specific LED
Gigabit Ethernet A/B	Gigabit Ethernet link status	Monitor link status
Gigabit Ethernet C/D	Gigabit Ethernet link status	Monitor link status

Table 2-14: Onboard Power Supply Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
AMC power enable	Control AMC board supply	Control power supply
Onboard power supply	Status of various onboard supply voltages	Monitor power good signals
Processor power supply	Status of processor supply voltage	Monitor power good
Voltage 0.9 V	DDR termination supply (1%)	Monitor voltage
Voltage 1.5 V	Board 1.5 V supply (1%)	Monitor voltage
Voltage 1.8 V	Board 1.8 V supply (1%)	Monitor voltage
Voltage 3.3 V	Board 3.3 V supply (1%	Monitor voltage
Voltage 5 V	Board 5 V supply (1%)	Monitor voltage
Voltage AMC 3.3 V	AMC management power 3.3 V (1%)	Monitor voltage
Voltage AMC 12 V	AMC payload power 12 V (1%)	Monitor voltage

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Table 2-15: Temperature Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
Processor temperature	Processor die temperature	Monitor temperature
Intel® 3100 chipset temperature	Intel® 3100 chipset die temperature	Monitor temperature
Inlet AMC sensor temperature	Inlet board temperature sensor near the AMC Card-edge connector	Monitor temperature
Outlet AMC sensor temperature	Outlet board temperature sensor near the AMC Card-edge connector	Monitor temperature
Inlet processor temperature	Inlet board temperature sensor near the processor	Monitor temperature
Outlet processor temperature	Outlet board temperature sensor near the processor	Monitor temperature
Processor over temperature	Indicates a catastrophic cooling failure processor temperature > 125°C	Monitor processor overtemperature signal
Processor internal thermal monitor	Status of internal thermal monitor	Monitor processor hot signal

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Chapter 3

Installation

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3. Installation

The AM4010 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AM4010. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



ESD Equipment!

This AMC board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Warning!



This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

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3.2 AM4010 Hot Swap Insertion Procedures

The AM4010 is designed for hot swap operation. Hot swapping allows the coordinated insertion and extraction of modules without disrupting other operational elements within the system. This allows for identified faulty elements to be removed and replaced without taking the carrier card out of service that will typically be hosting others modules.

The following procedures are applicable when inserting the AM4010 in a running system.

1. Ensure that the safety requirements indicated section 3.1 are observed.



Warning!

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installation. For information regarding the configuration of the AM4010 refer to Chapter 4.



Warning!

Care must be taken when applying the procedures below to ensure that neither the AM4010 nor other carrier boards are physically damaged by the application of these procedures.

3. To install the AM4010 perform the following:
   1. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the AMC Card-edge connector located on the carrier or backplane.
   2. Connect all external interfacing cables to the board as required.
   3. Using the handle on the front panel, engage the board with the carrier or backplane. When the handle is locked, the board is engaged and the following steps occur:
      1. The BLUE HS LED turns on.
         If the carrier recognizes that the AM4010 is fully seated, the carrier then enables the management power for the AM4010 and the BLUE HS LED turns on.
      2. Long blinks of the BLUE HS LED
         If the carrier IPMI controller detects the AM4010, it sends a command to the AM4010 to perform long blinks of the BLUE HS LED.
      3. The BLUE HS LED turns off.
         The Intelligent Platform Management Controller on the carrier reads the Module Current Requirements record and the AMC Point-to-Point Connectivity record. If the Module FRU information is valid and the carrier can provide the necessary payload power, the BLUE HS LED will be turned off. If the module FRU information is invalid or the carrier cannot provide the necessary payload power, the insertion process is stopped and the BLUE HS LED keeps blinking. Should this problem occur, please contact Kontron's Technical Support.
      4. Short blinks of the Module Management LEDs and the User-Specific LEDs
         The carrier enables the payload power for the AM4010, and the Module Management LEDs and the User-Specific LEDs emit a short blink.
   4. Ensure that the board and all required interfacing cables are properly secured.
4. The AM4010 is now ready for operation. For operation of the AM4010, refer to appropriate AM4010-specific software, application, and system documentation.

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3.3 AM4010 Hot Swap Extraction Procedures

To extract the board proceed as follows:

1. Ensure that the safety requirements indicated in section 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!
2. Pull the handle on the AM4010's front panel initiating the deactivation. This changes the state of the handle to open. Now, the following steps occur:
    1. Short blinks of the BLUE HS LED
        - When the carrier IPMI controller receives the handle opened event, the carrier sends a command to the MMC with a request to perform short blinks of the BLUE HS LED. This indicates to the operator that the AM4010 is waiting to be deactivated.
        - Now the AM4010 waits for a permission from higher level management (Shelf Manager or System Manager) to proceed with its deactivation.
        - Once the AM4010 receives the permission to continue the deactivation, all used ports are disabled.
        - The Intelligent Platform Management Controller on the Carrier disables the AM4010's Payload Power.
    2. The BLUE HS LED turns on
       Now the AM4010 is ready to be safely extracted.
3. Disconnect any interfacing cables that may be connected to the AM4010.
4. Pull the AM4010 out of the slot. Now the carrier disables the management power for the AM4010.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

3.4 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to the appropriate OS software documentation for installation.



Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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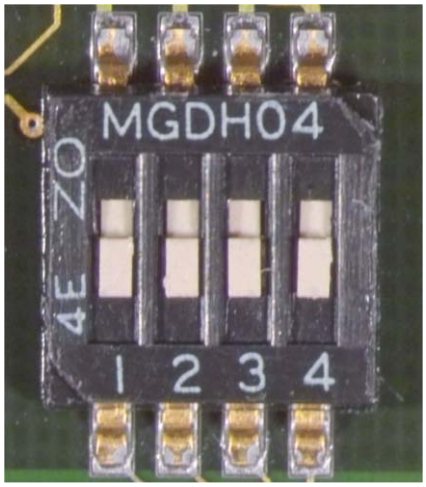
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4. Configuration

4.1 DIP Switch Configuration

The DIP switch consists of four switches for board configuration: switch 1 for BIOS POST code display configuration during boot-up, switch 2 for BIOS Firmware Hub Flash configuration, switch 3 for boot order configuration, and switch 4 for clearing the BIOS CMOS parameters.

Figure 4-1: DIP Switch



The following table indicates the functions of the four switches integrated in the DIP switch.

Table 4-1: DIP Switch Functions

SWITCH	FUNCTION
1	BIOS POST code configuration during boot-up
2	BIOS Firmware Hub configuration
3	Set the default boot order configuration
4	Clearing BIOS CMOS parameters

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4.1.1 User-Specific LED Configuration (BIOS POST Code)

The User-Specific LEDs are available for either general application use or indicating the BIOS POST code during boot-up. When BIOS POST code is selected, the User-Specific LEDs indicate BIOS POST code during boot-up.

Table 4-2: User-Specific LED Configuration (BIOS POST Code)

SWITCH 1	DESCRIPTION
OFF	*Enable BIOS POST Code during boot-up*
ON	Disable BIOS POST Code during boot-up

The default setting is indicated by using italic bold.

4.1.2 BIOS Firmware Hub Flash Configuration

BIOS Firmware Hub Flash configuration means that there are two chips for the BIOS on the AM4010 board. One chip is intended to provide a backup in the event that the other gets corrupted. If the primary BIOS is corrupted due to physical damage or a faulty Flash upgrade, either the Module Management Controller or the DIP switch can select the 2nd Flash, and the system can boot from it.

Table 4-3: BIOS Firmware Hub Flash Configuration

SWITCH 2	DESCRIPTION
OFF	*Normal boot from the primary BIOS FWH Flash*
ON	Boot from the secondary BIOS FWH Flash

The default setting is indicated by using italic bold.

4.1.3 Boot Order Configuration

Switch 3 enables the user to set the BIOS boot order. For further information on the boot order configuration, refer to section 4.4.1, “BIOS Configuration Register”.

Table 4-4: BIOS Boot Order Configuration

SWITCH 3	DESCRIPTION
OFF	*Boot order configured by the MMC*
ON	Default BIOS boot order configuration

The default setting is indicated by using italic bold.

4.1.4 Clear BIOS CMOS Configuration

Switch 4 enables the user to clear the BIOS CMOS parameters.

Table 4-5: BIOS CMOS Configuration

SWITCH 4	DESCRIPTION
OFF	*Standard BIOS CMOS parameters*
ON	Clear BIOS CMOS parameters

The default setting is indicated by using italic bold.

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4.2 Interrupts

The AM4010 board uses the standard AT IRQ routing (8259 controller). This interrupt routing is the default configurations, but it can be modified via the BIOS settings.

Table 4-6: Interrupt Setting

IRQ	PRIORITY	STANDARD FUNCTION
IRQ0	1	System Timer
IRQ1	2	Free (Keyboard Controller)
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	COM2
IRQ4	12	COM1
IRQ5	13	Watchdog
IRQ6	14	Free (Floppy Disk Controller)
IRQ7	15	Module Management Controller
IRQ8	3	System Real Time Clock
IRQ9	4	ACPI
IRQ10	5	Free
IRQ11	6	Free
IRQ12	7	Free
IRQ13	8	Coprocessor error
IRQ14	9	Free
IRQ15	10	Free
NMI		Watchdog

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4.3 Memory Map

The AM4010 board uses the standard AT ISA memory map.

4.3.1 I/O Address Map

The following table sets out the AM4010-specific I/O registers. The blue shaded table cells indicate MMC-specific registers.

Table 4-7: I/O Address Map

ADDRESS	DEVICE
0x080 - 0x81	BIOS POST Code
0x84	Debug POST Code
0x280	BIOS Configuration Register
0x281	MMC I/O Status Register
0x282	Watchdog Timer Control Register
0x283	AMC Geographic Addressing Register
0x284	Board and Logic Revision Register
0x285	Reset Status Register
0x286	Host I/O Status Register
0x287	Host I/O Configuration Register
0x288	Board ID Register
0x289	Board Interrupt Configuration Register
0x28A	Hot Swap Status Register
0x28B	User-Specific LED Configuration Register
0x28D	User-Specific LED Control Register
0x28E	Serial over LAN Configuration Register
0x28F	Delay Timer Control and Status Register
0x29C	MMC Configuration Register
0xCA2 - 0xCA3	IPMI SMS KCS interface
0xCA4 - 0xCA5	IPMI MSM KCS interface

4.4 AM4010-Specific Registers

The following registers are special registers which the AM4010 uses to watch the onboard hardware special features and the AMC control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.



Note ...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

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4.4.1 BIOS Configuration Register

The BIOS Configuration Register is used to configure a number of BIOS settings. The register is read only and can be configured only by the Module Management Controller.

Table 4-8: BIOS Configuration Register

REGISTER NAME		BIOS CONFIGURATION REGISTER		
ADDRESS		0x280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WPFWH	FWH write protection 0 = FWH write protection is disabled 1 = FWH write protection is enabled	0	
6-5	Res.	Reserved	00	R
4-3	BCON	BIOS configuration	00	R
2-0	BBOCON	BIOS boot order configuration 000 = Default BIOS boot order configuration If the DIP switch 3 is on, the default BIOS boot order configuration is selected	0	R

4.4.2 MMC I/O Status Register

The MMC I/O Status Register describes the MMC control signals. The register is read only and can be configured only by the Module Management Controller.

Table 4-9: MMC I/O Status Register

REGISTER NAME		MMC I/O STATUS REGISTER		
ADDRESS		0x281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	MFSEL	MMC Firmware Hub selection 0 = Select second FWH boot device 1 = Default FWH boot device is active	1	R
6	MCOVT	MMC chipset overtemperature 0 = Chipset temperature is above 105°C 1 = Normal operating	1	R
5	MEOR	MMC AMC Extended Options Region configuration 0 = AMC Extended Options Region is disabled 1 = AMC Extended Options Region is enabled With this bit the COM2 port and the debug port of the AMC Extended Options Region can be configured.	1	R
4	MFP89	MMC AMC Fat Pipes ports 8-9 configuration (GbE SerDes) 0 = AMC Fat Pipes ports 8-9 is disabled 1 = AMC Fat Pipes ports 8-9 is enabled With this bit the AMC Fat Pipes ports 8-9 can be configured.	1	R
3-1	Res.	Reserved	111	R
0	PEXC	PCI Express reference clock (100 MHz) configuration 0 = Reference clock from AMC Card-edge connector (FCLKA) 1 = Local reference clock used	1	R

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4.4.3 Watchdog Timer Control Register

The AM4010 has one Watchdog Timer provided with a programmable timeout ranging from 125 ms to 256 s. Failure to strobe the Watchdog Timer within a set time period results in a system reset, NMI or an interrupt. The NMI and interrupt mode can be configured via the board interrupt configuration register (0x289).

There are four possible modes of operation involving the Watchdog Timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register (0x282) must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational Watchdog Timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. To be effective, the hard reset must not be masked or otherwise negated. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

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Table 4-10: Watchdog Timer Control Register

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER		
ADDRESS		0x282		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog timer expired status bit 0 = Watchdog Timer has not expired 1 = Watchdog Timer has expired. Writing a '1' to this bit resets it to 0.	0	R
6-5	WMD	Watchdog Mode 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable/Watchdog trigger control bit: 0 = Watchdog Timer has not been enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog Timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog Timer is enabled, it will indicate a '1'. 1 = Watchdog Timer is enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3-0	WTM	Watchdog timeout settings 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = reserved 1101 = reserved 1110 = reserved 1111 = reserved The nominal timeout period is 5% longer than the above-stated values.	0000	R/W

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4.4.4 AMC Geographic Addressing Register

This register holds the AMC geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the AM4010.

Table 4-11: AMC Geographic Addressing Register

REGISTER NAME		AMC GEOGRAPHIC ADDRESSING REGISTER		
ADDRESS		0x283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-5	Res.	Reserved	000	R
4-0	GA	AMC geographic address	N/A	R



Note ...

The AMC geographic addressing register is set to the default values by power-on reset, not by PCI reset.

4.4.5 Board and Logic Revision Register

The Board and Logic Revision Register signals to the software when differences in the hardware require different handling by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each changed in hardware as development continues.

Table 4-12: Board and Logic Revision Register

REGISTER NAME		BOARD AND LOGIC REVISION REGISTER		
ADDRESS		0x284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	HWR	Board revision	N/A	R
3-0	LR	Logic revision	N/A	R

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4.4.6 Reset Status Register

The reset status register is used to determine the reset source.

Table 4-13: Reset Status Register

REGISTER NAME		RESET STATUS REGISTER		
ADDRESS		0x285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PHRST	Power-on host reset detection 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears this bit.	N/A	R/W
6-4	Res.	Reserved	N/A	R
3	MRST	MMC reset the host processor 0 = System reset generated by power-on reset 1 = System reset generated by MMC Writing a '1' to this bit clears the bit.	0	R/W
2-1	Res.	Reserved	00	R
0	WRST	Watchdog timer reset the host processor 0 = System reset generated by power-on reset 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W

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4.4.7 Host I/O Status Register

The Host I/O Status Register describes the onboard and AMC control signals.

Table 4-14: Host I/O Status Register

REGISTER NAME		HOST I/O STATUS REGISTER		
ADDRESS		0x286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-6	Res.	Reserved	00	R
5-4	FBSTA	Firmware Hub boot status 00 = Boot from FWH0 01 = Boot from FWH1 10 = Boot from LPC FWH	00	R
3-0	DIPS	DIP Switch configuration	1111	R

4.4.8 Host I/O Configuration Register

The Host I/O Configuration Register holds a series of bits defining the onboard configuration.

Table 4-15: Host I/O Configuration Register

REGISTER NAME		HOST I/O CONFIGURATION REGISTER		
ADDRESS		0x287		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-6	Res.	Reserved	0	R
5	FSEL	Firmware Hub selection 0 = Default FWH boot device is active 1 = Select second FWH boot device	0	R/W
4-0	Res.	Reserved	00000	R

4.4.9 Board ID Register

This register describes the hardware and the board index. The content of this register is unique for each Kontron AMC board.

Table 4-16: Board ID Register

REGISTER NAME		BOARD I/D REGISTER		
ADDRESS		0x288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-0	BID	Board identification 0xA2 = AM4010	0xA2	R/W

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4.4.10 Board Interrupt Configuration Register

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing for the Watchdog. If the Watchdog Timer fails, it can generate two independent hardware events: NMI and IRQ5 interrupt.

Table 4-17: Board Interrupt Configuration Register

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER		
ADDRESS		0x289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-2	Res.	Reserved	000000	R
1-0	WIRQ	Watchdog interrupt configuration 00 = Disabled 01 = IRQ5 10 = Reserved 11 = NMI	00	R/W

4.4.11 Hot Swap Status Register

The hot swap status register describes the AMC hot swap handle status.

Table 4-18: Hot Swap Status Register

REGISTER NAME		HOT SWAP STATUS REGISTER		
ADDRESS		0x28A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res.	Reserved	0	R
6	HSH	AMC hot swap handle status 0 = AMC hot swap handle in closed position 1 = AMC hot swap handle in open position	N/A	R
5-0	Res.	Reserved	000000	R

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4.4.12 User-Specific LED Configuration Register

The User-Specific LED Configuration Register holds a series of bits defining the onboard configuration for the front panel User-Specific LEDs.

Table 4-19: User-Specific LED Configuration Register

REGISTER NAME		USER-SPEDIFIC LED CONFIGURATION REGISTER		
ADDRESS		0x28B		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	Res.	Reserved	0000	R
3-0	ULCON	User-Specific LED Configuration 0000 = POST [1] 0001 = MODE A [2] 0010 = MODE B [3] 0011 = MODE C [4] 0100 - 1101 = Reserved 1110 = DIAG [5] *This is the default mode after POST.* 1111 = TEST [6]	0000	R/W

Regardless of the selected configuration, the User-Specific LEDs are used to signal a number of fatal onboard hardware errors, such as:

ULED0: BIOS boot fail (red)
ULED1: Hardware reset (red)
ULED2: Clock fail (red)
ULED3: Power fail (red)

[1] In BIOS POST mode (default), the User-Specific LEDs build a binary vector to display BIOS POST code during the pre-boot phase. In doing so, the higher 4-bit nibble of the 8-bit BIOS POST code is displayed followed by the lower nibble followed by a pause. BIOS POST code is displayed in general in green color.

ULED0: POST bit 0 and bit 4 (green)
ULED1: POST bit 1 and bit 5 (green)
ULED2: POST bit 2 and bit 6 (green)
ULED3: POST bit 3 and bit 7 (green)

For further information on reading the 8-Bit BIOS POST Code, refer to section 2.3.1, “Front Panel LEDs”.

[2] Configured for MODE A, the User-Specific LEDs are dedicated to functions as follows:

ULED0: User-Specific LED 0, controlled by HOST (red/green)
ULED1: User-Specific LED 1, controlled by HOST (red/green)
ULED2: Ethernet Link Status of AMC channel B (green)
ULED3: Ethernet Link Status of AMC channel A (green)

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[3] Configured for MODE B, the User-Specific LEDs are dedicated to functions as follows:

ULED0: User-Specific LED 0, controlled by MMC (red/green)
ULED1: User-Specific LED 1, controlled by MMC (red/green)
ULED2: Ethernet Link Status of AMC channel B (green)
ULED3: Ethernet Link Status of AMC channel A (green)

[4] Configured for MODE C, the User-Specific LEDs are dedicated to functions as follows:

ULED0: Ethernet Link Status of AMC channel D (green)
ULED1: Ethernet Link Status of AMC channel C (green)
ULED2: Ethernet Link Status of AMC channel B (green)
ULED3: Ethernet Link Status of AMC channel A (green)

[5] Configured for DIAG, the User-Specific LEDs are dedicated to functions as follows:

ULED0: Watchdog Timer running (green), Watchdog Timer Timeout (red+green)
ULED1: SATA channels active (green)
ULED2: Ethernet Link Status of AMC channel B (green)
ULED3: Ethernet Link Status of AMC channel A (green)

[6] Configured for TEST, the User-Specific LEDs are dedicated to functions as follows:

ULED0: User-Specific LED 0 (red/green)
ULED1: User-Specific LED 0 (red/green)
ULED2: User-Specific LED 0 (red/green)
ULED3: User-Specific LED 0 (red/green)

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4.4.13 User-Specific LED Control Register

The User-Specific LED Control Register enables the user to switch on and off the front panel User-Specific LEDs.

Table 4-20: User-Specific LED Control Register

REGISTER NAME		USER-SPECIFIC LED CONTROL REGISTER		
ADDRESS		0x28D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	ULCMD	User-Specific LED command: 0000 = Get User-Specific LED 0 0001 = Get User-Specific LED 1 0010 - 0111 = Reserved 1000 = Set User-Specific LED 0 1001 = Set User-Specific LED 1 1010 - 1111 = Reserved	0	R/W
3-0	ULCOL	User-Specific LED color: 0000 = off 0001 = green 0010 = red 0011 = red+green 0100 = reserved 0101 = green, slow blinking 0110 = red, slow blinking 0111 = red+green, slow blinking 1000 = reserved 1001 = green, fast blinking 1010 = red, fast blinking 1011 = red+green, fast blinking		



Note ...

This register can only be used if the User-Specific LEDs indicated in the “User-Specific LED Configuration Register” (Table 4-19) are configured in Mode A.

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4.4.14 Serial Over LAN Configuration Register

Via the Serial Over LAN configuration Register the MMC can configure a number of SOL settings. This register is read only and can be configured only by the MMC.

Table 4-21: Serial over LAN Configuration Register

REGISTER NAME		SERIAL OVER LAN CONFIGURATION REGISTER		
ADDRESS		0x28E		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	SCOM	Host COM1 port configuration for Serial over LAN	0000	R
3-0	SOLC	Serial over LAN configuration 0000 = 82571EB emulated serial port is used 0001 = MMC using host COM1 port for Serial Over LAN If the MMC is using the host COM1 port for Serial Over LAN, both bits (SCOM and SOLC) must be set to '1'.	0000	R

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4.4.15 Delay Timer Control and Status Register

The Delay Timer enables the user to realize short, reliable delay times. It runs by default and does not start again on its own. It can be restarted at anytime by writing anything else then a ’0’ to the delay timer control/status register. The hardware delay timer provides a set of outputs for defined elapsed time periods. The timer outputs reflected in the delay timer control/status register are set consecutively and remain set until the next restart is triggered again.

Table 4-22: Delay Timer Control and Status Register

REGISTER NAME		DELAY TIMER CONTROL/STATUS REGISTER		
ADDRESS		0x28F		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-0	DTC	Delay Timer Control The hardware delay timer is operated via one simple 8-bit control/status register. During normal operation, each of the 8 bits reflects a timer output which means defined elapsed time period after the last restart according to the following bit mapping: DTC[7:0] Value Accuracy Bit 7: 1 ms < + 0.04% Bit 6: 500 µs < + 0.08% Bit 5: 250 µs < + 0.16% Bit 4: 100 µs < + 0.4% Bit 3: 50 µs < + 0.8% Bit 2: 10 µs < + 4% Bit 1: 5 µs < + 8% Bit 0: 1 µs < + 40%	0x00	R/W

Since the timer width and thus the availability of outputs varies over different implementations, it is necessary to be able to determine the timer capability. Therefore, writing a ’0’ to the delay timer control/status register followed by reading indicates the timer capability (not the timer outputs). For example, writing 0x00 and then reading 0xFF results in a 8-bit wide timer register. This status register mode can be switched off to normal timer operation by writing anything else then a ’0’ to this register.

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4.4.16 MMC Configuration Register

The MMC Configuration Register holds a series of bits defining the host COM port routing and the MMC Serial port configuration.

Table 4-23: MMC Configuration Register

REGISTER NAME		MMC CONFIGURATION REGISTER		
ADDRESS		0x29C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	MPGC	MMC program request 0 = No action 1 = Request MMC to program internal Flash from external Flash	0	R/W
6	MPGU	MMC enforce User Program Mode request 0 = No action 1 = Set MMC in User Program Mode (this bit is ignored if MMC is in local programming mode)	0	R/W
5-4	Res.	Reserved	00	R
3	MCOMT	MMC Serial port configuration for debugging purposes 0 = MMC Serial port is connected to the COM front panel RJ45 connector (only for debugging purposes) 1 = MMC Serial port is isolated	1	R
2	MSCI	MMC Serial port configuration for Firmware update 0 = Host COM2 port is disable 1 = Host COM2 port is connected to MMC Serial port (this bit is ignored if the MCOMT signal is 0)	0	R/W
1	MRST	MMC reset function 0 = MMC controller is running 1 = MMC controller is in reset state	0	R/W
0	MPGM	MMC program mode; select the Firmware update mode 0 = Normal operating mode 1 = Set MMC in Firmware update mode	0	R/W

4.4.17 IPMI Keyboard Control Style Interface

The host processor communicates with the MMC using two Keyboard Control Style interfaces, which are defined in the IPMI specification. One interface is for the System Management Software (SMS) used within an operating system, and one for the System Management Mode (SMM) used only by the BIOS.

The KCS interface for the system management software is on the I/O location 0xCA2 and 0xCA3, and configured as regular ISA interrupt.

The KCS interface for the system management mode is on the I/O location 0xCA4 and 0XCA5, and configured as SMI interrupt.

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Chapter 5

Power Considerations

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5. Power Considerations

5.1 AM4010 Voltage Ranges

The AM4010 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The AM4010 requires two power sources, the module management power for the MMC (nominal: 3.3V DC) and a single payload power (nominal: 12V DC) for the module components.

The following table specifies the ranges for the different input power voltages within which the board is functional. The AM4010 is not guaranteed to function if the board is not operated within the operating range.

Table 5-1: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	OPERATING RANGE
Payload Power (nominal: 12V DC)	10.0 V min. to 14.0 V max.	10.8 V min. to 13.2 V max.
Module Management Power (nominal: 3.3V DC)	2.97 V min. to 3.63 V. max. (±10%)	3.135 V min. to 3.465 V max. (±5%)



Warning!

The AM4010 must not be operated beyond the absolute range indicated in the table above. Failure to comply with the above may result in damage to the board.

5.2 Carrier Power Requirements

5.2.1 Payload Power

Payload power is the power provided to the module from the carrier or the backplane for the main function of the module. The payload power voltage should be selected at the higher end of the specified voltage range. The continuous current limit value is based on the power limit of 60 W per module at the minimum supply value. The maximum current value for the payload power is derived from a 25% derating of the connector pins, which allow a total of 6.0 A (0.75 A per pin; 8 pins).

The payload power voltage shall be at least 10.8 V and not more than 13.2 V at the module contacts during normal conditions under all loads (see Table 5-1, “DC Operational Input Voltage Ranges”). The bandwidth-limited periodic noise due to switching power supplies or any other source shall not exceed 200 mV peak to peak.

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5.2.2 Payload and MMC Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the AM4010:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.

The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.2.3 Module Management Power Consumption

The module management power is used only for the Module Management Controller (MMC), which has a very low power consumption. The management power voltage measured on the AMC at the connector shall be 3.3 V ± 5% and the maximum current is 100 mA (see Table 5-1, “DC Operational Input Voltage Ranges”).

5.3 Payload Power Consumption of the AM4010

The goal of this description is to provide a method to calculate the payload power consumption for the AM4010 board with different configurations and applications. The processor, the chipset and the memory dissipate the majority of the payload power.

The payload power consumption tables below list the voltage and power specifications for the AM4010 board using Intel® Core™ Duo and the Intel® Core™ 2 Duo processors. The values were measured using an AMC carrier with two power supplies: one for the AM4010 module, and the other for the hard disk and the peripheral devices.

The operating systems used were DOS and Linux. All measurements were conducted at a temperature of 25°C with a nominal payload power of 12 V and with the following interfaces connected:

- Front Gigabit Ethernet
- Front Serial Port
- Front USB (keyboard and mouse)

All AMC fabric interfaces were active during the measurements.

The module management power is below 0.3 W and it was therefore not considered for these measurements. The measured values varied, because the power consumption was dependent on processor activity.



Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 10%.

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The payload power consumption was measured using the following processors:

- Intel® Core™ Duo processor U2500 (ULV), 1.2 GHz, 533 MHz FSB, 2 MB L2 cache
- Intel® Core™ Duo processor L2400 (LV), 1.66 GHz, 667 MHz FSB, 2 MB L2 cache
- Intel® Core™ 2 Duo processor L7400 (LV), 1.5 GHz, 667 MHz FSB, 4 MB L2 cache

with the following operating systems and test software:

- DOS
  With this operating system only one processor core was active. This operating system has no power management support and provides a very simple method to verify the measured power consumption values.
- Linux, IDLE Mode
  With these operating systems both processor cores were in IDLE state.
- Linux, Intel® Thermal Analysis Tool (TAT) at 75% (real application)
  The power consumption values measured using the Intel® Thermal Analysis Tool operating at 75% correspond to 100% CPU usage of both processor cores and are equivalent to the values of a maximum user application environment.

  If the Intel® Thermal Analysis Tool (TAT) is operated at 75%, the power dissipated by the processor corresponds to the maximum Thermal Design Power (TDP) as specified in the respective datasheets for the Intel® Core Duo and the Intel® Core 2 Duo processors.
- Linux, Intel® Thermal Analysis Tool (TAT) at 100% (no real application)
  The power consumption values measured using the Intel® Thermal Analysis Tool operating at 100% do not represent the power consumption of a real application. However, the processor may also generate short power load pulses during normal operation. For this reason, the power supplies must be able to deliver the amount of power required by the AM4010 as indicated in the tables below.

Table 5-2: Payload Power Consumption: AM4010 with Core™ Duo, 1.2 GHz

MEMORY CONFIG.	DOS	LINUX IDLE MODE	LINUX 75% INTEL® TAT	LINUX 100% INTEL® TAT
1 GB / 2 GB	22 W	18 W	25 W	27 W

Table 5-3: Payload Power Consumption: AM4010 with Core™ Duo, 1.66 GHz

MEMORY CONFIG.	DOS	LINUX IDLE MODE	LINUX 75% INTEL® TAT	LINUX 100% INTEL® TAT
1 GB / 2 GB	27 W	22 W	34 W	38 W

Table 5-4: Payload Power Consumption: AM4010 with Core™ 2 Duo, 1.5 GHz

MEMORY CONFIG.	DOS	LINUX IDLE MODE	LINUX 75% INTEL® TAT	LINUX 100% INTEL® TAT
1 GB / 2 GB	27 W	22 W	36 W	40 W



Note ...

The power consumption values measured using the Intel® Thermal Analysis Tool operated at 100% cannot be reached in normal software applications.

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5.4 IPMI FRU Payload Power Consumption

The following tables indicate the IPMI FRU payload power consumption.

Table 5-5: IPMI FRU Payload Power Consumption of the AM4010

MEMORY CONFIGURATION	INTEL® Core™ Duo 1.2 GHz	INTEL® Core™ Duo 1.66 GHz	INTEL® Core™ 2 Duo 1.5 GHz
1 GB / 2 GB	2.1 A (25.2 W)	2.9 A (34.8 W)	3 A (36 W)

5.5 Payload Start-Up Current of the AM4010

The following tables indicate the payload start-up current of the AM4010 during the first 2-3 seconds after the payload power has been applied. The payload power consumption of the AM4010 during operation is indicated in Tables 5-2 to 5-4.

Table 5-6: Payload Start-Up Current of the AM4010

MEMORY CONFIGURATION	INTEL® Core™ Duo 1.2 GHz	INTEL® Core™ Duo 1.66 GHz	INTEL® Core™ 2 Duo 1.5 GHz
1 GB / 2 GB	1.3 A	1.4 A	1.7 A

For further information on the start-up current, contact Kontron's Technical Support.

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Chapter 6

Thermal Considerations

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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing AM4010 applications.

6.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AM4010, all onboard components must remain within the maximum temperature specifications. The most critical components on the AM4010 are the processor and the chipset. Operating the AM4010 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the BIOS and the Module Management Controller support several temperature monitoring and control features.

The AM4010 includes six temperature sensors that are accessible via the Module Management Controller. They are distributed over the complete board to measure the onboard temperature values and regulate the board's power consumption.

The AM4010 uses the following temperature sensors:

- Inlet board temperature sensor near the AMC Card-edge connector (Inlet AMC Sensor)
- Outlet board temperature sensor near the AMC Card-edge connector (Outlet AMC Sensor)
- Inlet board temperature sensor near the processor (Inlet Processor Sensor)
- Outlet board temperature sensor near the processor (Outlet Processor Sensor)
- Thermal Diode Sensor on the Intel® Core™ Duo / Intel® Core™ 2 Duo processor
- Thermal Diode Sensor on the Intel® 3100 chipset

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6.1.1 Placement of the Temperature Sensors

Figure 6-1: Board Temperature Sensor Placement (AM4010 Bottom View)

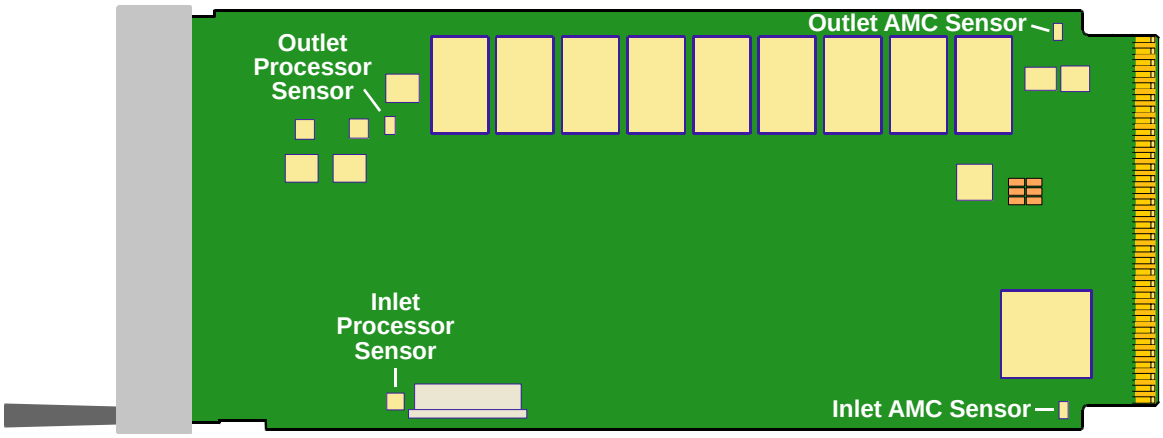
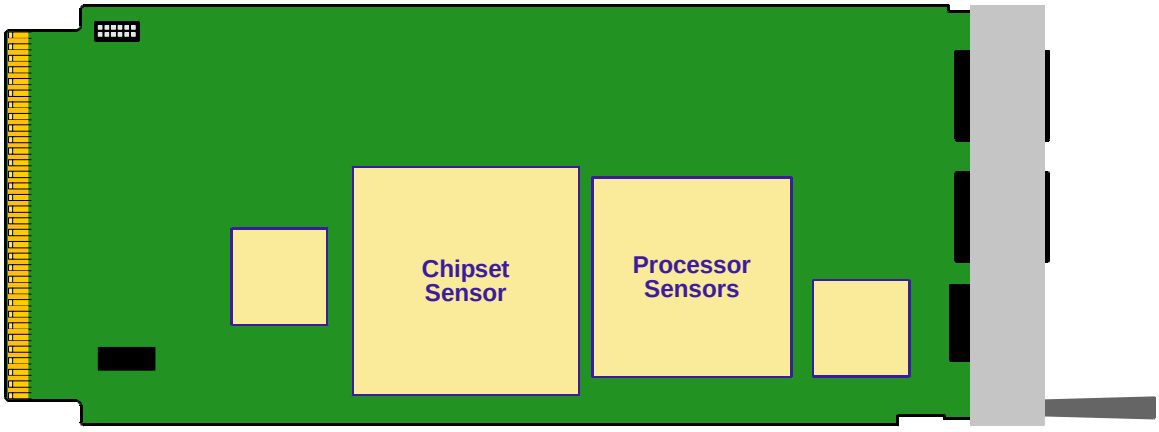


Figure 6-2: Processor Temperature Sensor Placement (AM4010 Top View)



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6.1.2 Board Thermal Monitoring

The AM4010 includes four board temperature sensors distributed over the complete board to measure the board temperature and regulate the board's power consumption (see Figure 6-1). The board temperature sensors accessible via the Module Management Controller.

The AM4010 uses the following board temperature sensors:

- Inlet board temperature sensor near the AMC Card-edge connector (Inlet AMC Sensor)
- Outlet board temperature sensor near the AMC Card-edge connector (Outlet AMC Sensor)
- Inlet board temperature sensor near the processor (Inlet Processor Sensor)
- Outlet board temperature sensor near the processor (Outlet Processor Sensor)

6.1.3 Processor Thermal Monitoring

The Intel® Core™ Duo / Core™ 2 Duo processor includes the following on-die temperature sensors:

- Two Digital Thermal Sensors (DTS)
- Thermal Diode Sensor
- Thermal Monitor 1 (TM1) Sensor
- Thermal Monitor 2 (TM2) Sensor
- Catastrophic Cooling Failure Sensor

Via the Thermal Diode Sensor, the Module Management Controller can measure the processor die temperature. Via the Digital Thermal Sensor (DTS), the BIOS or the application software can measure the processor die temperature.

The Thermal Monitor 1 (TM1) Sensor, the Thermal Monitor 2 (TM2) Sensor, and the Catastrophic Cooling Failure Sensor are not accessible. They serve for protecting the processor from overheating. These sensors are integrated in the processor and work without any interoperability of the Module Management Controller, the BIOS or the software application. Enabling the thermal control circuit in the BIOS allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

The maximum die temperatures for all processor types is as follows:

- Intel® Core™ Duo: all versions: 100 °C
- Intel® Core™ 2 Duo: all versions: 100 °C

6.1.3.1 Digital Thermal Sensor (DTS)

The processor includes two on-die Digital Thermal Sensors (DTS) that can be read via an internal register of the processor (no I/O interface). The Digital Thermal Sensors provide the preferred method of reading the processor die temperature since they are located much closer to the hottest portions of the die and can thus more accurately track the die temperature. The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating temperature (100 °C).

The values measured at the Digital Thermal Sensors (DTS) may not correspond to the values measured at the Thermal Diode Sensor since the Thermal Diode Sensor is located elsewhere on processor die.

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6.1.3.2 Thermal Diode Sensor

The processor includes one Thermal Diode Sensor used by the Module Management Controller to measure the processor die temperature.

6.1.3.3 Thermal Monitor 1 (TM1)

The Thermal Monitor 1 (TM1) Sensor controls the processor temperature and power consumption by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature.

When TM1 is enabled and a high temperature situation exists, the processor frequency is reduced and the event is reported via an external signal to the Module Management Controller. Once the temperature has dropped below the maximum operating temperature, the Thermal Control Circuit goes inactive.

The temperature at which TM1 activates the Thermal Control Circuit is neither user-configurable nor software-visible.

TM1 does not require any additional hardware, software drivers, or interrupt handling routines. This function can be enabled and disabled in the BIOS.



Note ...

When the ULED3 on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 100°C.

6.1.3.4 Thermal Monitor 2 (TM2)

The Thermal Monitor 2 (TM2) Sensor controls the processor temperature and power consumption by activating the Intel® Speedstep® function when the processor silicon reaches its maximum operating temperature.

When TM2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel® SpeedStep® Technology transition to a lower operating point and reports the event via an external signal to the Module Management Controller. In this case, the processor reduces its operating frequency and processor core voltage. This combination of reduced frequency and core voltage results in a reduction of the processor power consumption. If the processor temperature drops below the critical temperature level, the processor will make an Enhanced Intel® SpeedStep® Technology transition to the last requested operating point.

The temperature at which TM2 activates the Intel® Speedstep® function is neither user-configurable nor software-visible.

TM2 does not require any additional hardware, software drivers, or interrupt handling routines. This function can be enabled and disabled in the BIOS.



Note ...

When the ULED3 on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 100°C.

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6.1.3.5 Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating. The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 125°C. Once activated, the event remains latched until the AM4010 undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the BIOS. It is always enabled to ensure that the processor is protected in any event.



Note ...

When all ULEDs on the front panel are blinking red, it indicates that the processor die temperature is above 125°C.

6.1.4 Chipset Thermal Monitor Feature

The Intel® 3100 chipset includes one on-die Thermal Diode Sensor used by the Module Management Controller to measure the chipset die temperature.

The maximum chipset case temperature is as follows:

- Intel® 3100 chipset: 105 °C



Note ...

When the ULED2 on the front panel is lit red after boot-up, it indicates that the chipset case temperature is above 105°C.

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6.2 System Airflow

The AM4010 is equipped with a specifically designed heat sink to ensure the best possible basis for operational stability and long-term reliability. Coupled together with system chassis, which provide variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

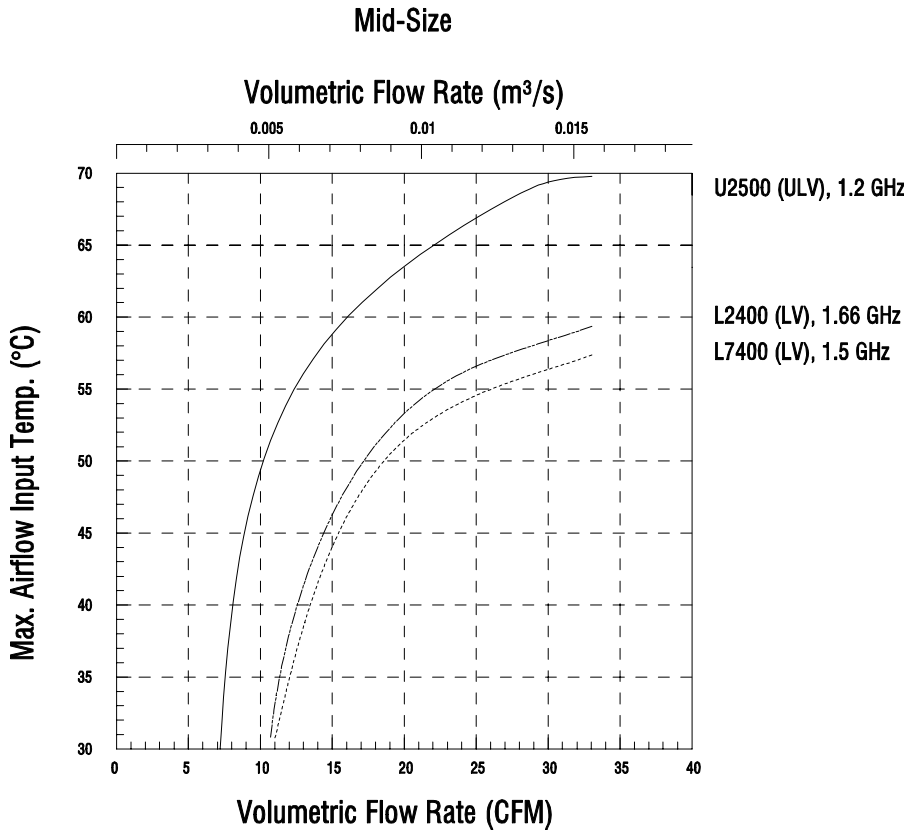
The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, it has been specifically designed to efficiently support forced airflow concepts as found in modern AMC carriers and MicroTCA systems.

6.2.1 Forced Airflow in MicroTCA Systems

When developing applications using the AM4010, the system integrator must be aware of the overall system thermal requirements. The MicroTCA systems must satisfy these thermal requirements.

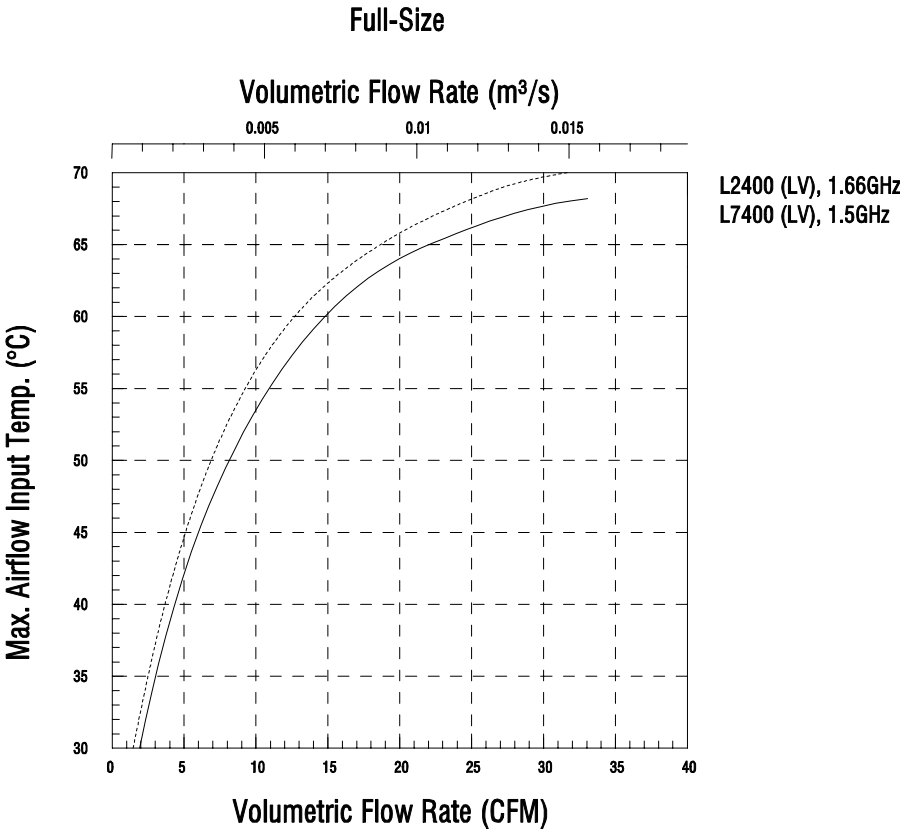
The following figures illustrate the temperature vs. airspeed graphs of a Mid-size and a Full-size AM4010 mounted in a MicroTCA system designed for Single Modules. The measurements were made using the Intel® Thermal Analysis Tool (TAT) operating at 75% which corresponds to 100% CPU usage of both processor cores. These measurements are equivalent to the values of a maximum user application environment.

Figure 6-3: Temperature vs. Airspeed Graph of a Mid-Size AM4010



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Figure 6-4: Temperature vs. Airspeed Graph of a Full-Size AM4010





Note ...

The maximum airflow input temperature was measured at the bottom of the board just before the air flowed over the board.

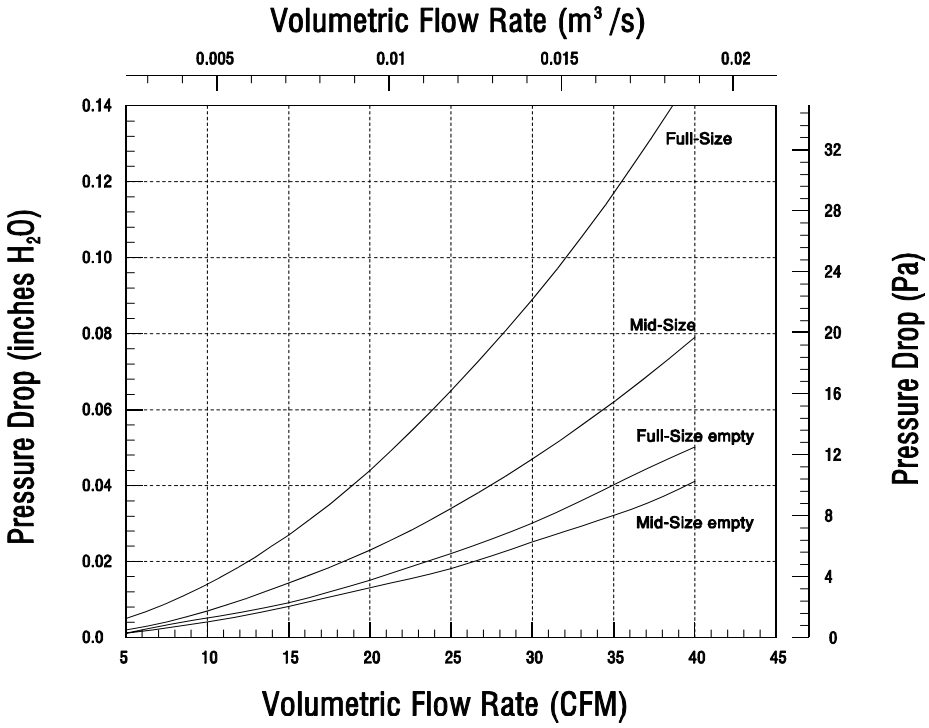
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6.2.2 Airflow Impedance

In order to determine the cooling requirements of the AM4010, the airflow impedance of a Mid-size and a Full-size AM4010 module has been determined via simulation. No card guides or struts have been used for the simulations because the resulting airflow impedance depends on individual configuration of the AMC carrier or MicroTCA system.

The following figure shows the impedance curves of a Mid-size and a Full-size AM4010 module.

Figure 6-5: Mid-Size and Full-Size AM4010 Impedance Curves



The following table indicates the pressure drop at 10, 20, 30, and 40 CFM volumetric flow rates.

Table 6-1: Pressure Drop vs. Airflow Data

VOLUMETRIC FLOW RATE [CFM]	PRESSURE DROP [inches H2O]			
	MID-SIZE	MID-SIZE EMPTY	FULL-SIZE	FULL-SIZE EMPTY
10	0.007	0.004	0.014	0.005
20	0.023	0.013	0.044	0.015
30	0.047	0.025	0.089	0.030
40	0.079	0.041	0.149	0.050

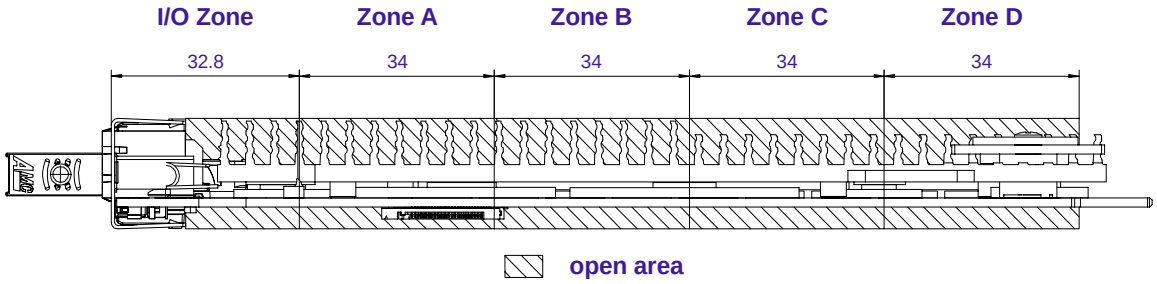
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6.2.3 Airflow Paths

The area between the front panel and the AMC Card-edge connector is divided into five zones, one I/O zone and four uniform thermal zones, A, B, C, and D. The PICMG AMC.0 Specification states that the uniformity of the airflow paths' resistance should provide an impedance on the A, B, C, and D zones that is within ± 25% of the average value of the four thermal zones.

The following figure shows the thermal zones of a Mid-size AM4010.

Figure 6-6: Thermal Zones of the Mid-Size AM4010 Module



The following table indicates the deviation of the airflow rate on a Mid-size AM4010 module.

Table 6-2: Deviation of the Airflow Rate on a Mid-Size AM4010

VOLUMETRIC FLOW RATE [CFM]	DEVIATION OF THE AIRFLOW RATE			
	ZONE A	ZONE B	ZONE C	ZONE D
10	1.42%	-0.85%	-1.42%	1.99%
20	2.14%	-0.71%	-1.00%	2.43%
30	2.10%	-0.57%	-0.95%	2.48%
40	1.93%	-0.64%	-0.79%	2.08%

Note ...

The Mid-size AM4010 module has an airflow rate deviation of max. ± 2.5% of the average value of the four thermal zones (max. ± 25% is allowed).

Positive deviation means increased airflow.

Negative deviation means decreased airflow.

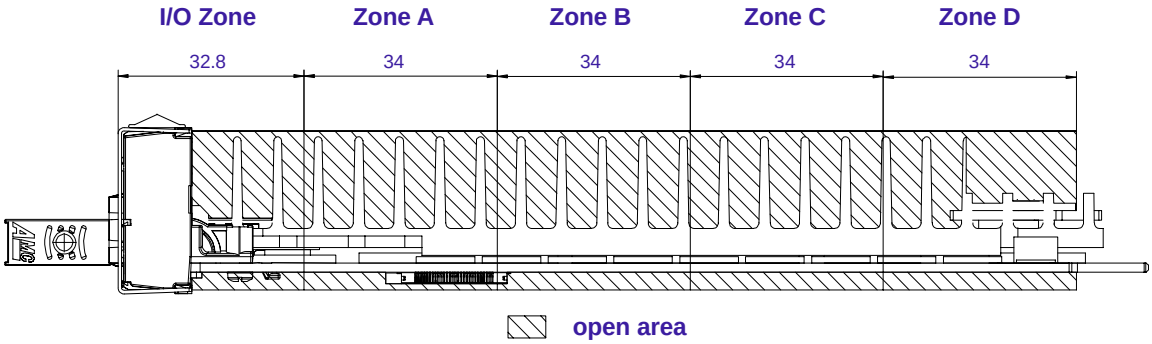
Note ...

The Mid-size AM4010 module provides an open area of 44%. According to the PICMG AMC.0 Specification, an open area of 20 to 70% perpendicular to the airflow path is recommended.

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The following figure shows the thermal zones of a Full-size AM4010.

Figure 6-7: Thermal Zones of the Full-Size AM4010 Module



The following table indicates the deviation of the airflow rate on a Full-size AM4010 module.

Table 6-3: Deviation of the Airflow Rate on a Full-Size AM4010

VOLUMETRIC FLOW RATE [CFM]	DEVIATION OF THE AIRFLOW RATE			
	ZONE B	ZONE D	ZONE C	ZONE D
10	4.0%	-2.86%	-2.86%	1.71%
20	4.0%	-2.29%	-2.86%	1.14%
30	3.82%	-2.29%	-2.64%	1.15%
40	3.87%	-1.87%	-2.44%	0.43%

Note ...

The Full-size AM4010 module has an airflow rate deviation of max. ± 4% of the average value of the four thermal zones (max. ± 25% is allowed).

Positive deviation means increased airflow.

Negative deviation means decreased airflow.

Note ...

The Full-size AM4010 module provides an open area of 47%. According to the PICMG AMC.0 Specification, an open area of 20 to 70% perpendicular to the airflow path is recommended.

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