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»Kontron User's Guide«

AM4904



Document Revision 1.2

Document ID: SK-MAN-AM4904 1036-1597

Issue Date: April 2011

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Revision History

Rev. Index	Brief Description of Changes	Date of Issue
0.1	Initial Issue	3 July, 2009
0.2	Included PCIe and sRIO variants, minor edits	16 September, 2009
1.0	Major edits in all chapters	14 July, 2010
1.1	Minor edits in all chapters	6 April, 2011
1.2	Minor edits in chapter 3 „Operating the Unit“	14 April, 2011

Customer Service

Contact Information:

Kontron Canada, Inc.
4555 Ambroise-Lafortune
Boisbriand, Québec, Canada
J7H 0A4
Tel: (450) 437-5682
(800) 354-4223
Fax: (450) 437-8053
E-mail: support@ca.kontron.com

Kontron Modular Computer GMBH
Sudetenstrasse 7
87600 Kaufbeuren
Germany
+49 (0) 8341 803 333
+49 (0) 8341 803 339
support-kom@kontron.com

Visit our site at:www.kontron.com

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Kontron reserves the right to make changes without notice in product or component design as warranted by evolution in user needs or progress in engineering or manufacturing technology. Changes that affect the operation of the unit will be documented in the next revision of this user's guide.

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

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Before you Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisory Conventions" section for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.
- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support

WARNING



High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.



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When Working Inside a Computer

Before taking covers off a computer, perform the following steps:

- Turn off the computer and any peripherals.
- Disconnect the computer and peripherals from power sources or subsystems to prevent electric shock or system board damage. This does not apply to when hot-swapping parts.
- Disconnect telephone or telecommunications lines from the computer.

In addition, take note of these safety guidelines when appropriate:

- To help avoid possible damage to system boards, wait five seconds after turning off the computer before removing a component, removing a system board, or disconnecting a peripheral device from the computer.
- When you disconnect a cable, pull on its connector or on its strain-relief loop, not on the cable itself. Some cables have a connector with locking tabs. If you are disconnecting this type of cable, press in on the locking tabs before disconnecting the cable. As you pull connectors apart, keep them evenly aligned to avoid bending any connector pins. Also, before connecting a cable, make sure both connectors are correctly oriented and aligned.

CAUTION



Do not attempt to service the system yourself, except as explained in this user's guide. Follow installation and troubleshooting instructions closely.



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Advisory Conventions

CAUTION



This symbol and title indicate potential damage to hardware and tells you how to avoid the problem.



CAUTION

Electric Shock



This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.



WARNING



This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



ESD Sensitive Device



This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions”.

Note...



This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

CE Conformity



This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Regulatory Compliance Statements” in this manual.

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Safety Instructions

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

WARNING



All operations on this device must be carried out by sufficiently skilled personnel only.



WARNING



Do not connect a switch port to a telephone line.



WARNING



For installation in a Hot-Plug system, observe the safety instructions specific to the system. Read the relevant documentation.



CAUTION

Electric Shock



High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.



Caution, Laser Light!



Laser light from fiber-optic transmission cables and components can damage your eyes. The laser components plugged into the switch are Class 1 laser components. Class 1 laser is considered incapable of producing damaging radiation levels during normal operation or maintenance.

To avoid damaging your eyes and to continue safe operation in case of abnormal circumstances:

- Never look directly into the outlets of fiber-optic transmission components or fiber-optic cables with unprotected eyes.
- Never allow fiber-optic transmission path to operate until all the connections have been made.
- Always fit protective plugs to any unused ports of the switch.

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Special Handling and Unpacking Instructions



ESD Sensitive Device

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing mezzanines, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

Powering up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting without any other I/O peripherals attached, including AMC adapters.

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Make sure your system provides the minimum DC voltages required at the board's slot, especially if DC power is carried by cables.

If you are still not able to get your board running, contact our Technical Support for assistance.

Storing the Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron AG and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

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Regulatory Compliance Statements

FCC Compliance Statement for Class B Devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING



This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.



Safety Certification

All Kontron equipment meets or exceeds safety requirements based on the IEC/EN/UL/CSA 60950-1 family of standards entitled, "Safety of information technology equipment." All components are chosen to reduce fire hazards and provide insulation and protection where necessary. Testing and reports when required are performed under the international IECEE CB Scheme. Please consult the "Kontron Safety Conformity Policy Guide" for more information.

CE Certification

The product described in this user's guide was tested in a representative system and is found to be compliant with the CE marking requirements. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

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Kontron AG grants the original purchaser of Kontron's products a *TWO YEAR LIMITED HARDWARE WARRANTY* as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron AG.

Kontron AG warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron Modular Computers GmbH or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1 Introduction

1.1 MicroTCA™ System Overview

The MicroTCA™ Carrier Hub (MCH) described in this manual is based on the Micro Telecommunications Computing Architecture (MicroTCA™ or µTCA™) defined by the PCI Industrial Computer Manufacturers Group (PICMG®). The main advantages of MicroTCA™ include high throughput, multi-protocol support, hot swappability, high scalability, and integrated system management. For further information regarding the MicroTCA™ standard and its use, please consult the complete Micro Telecommunications Computing Architecture Base Specification.

The Kontron MCH cards can be integrated into MicroTCA™ backplanes providing them with superior processing power and maximum design options. To learn more about the outstanding features and advantages of Kontron MicroTCA™ systems, please contact Kontron or visit the Kontron web site.

1.2 Product Overview

A MicroTCA Carrier Hub (MCH) is the central management and data switching device in a MicroTCA system. The mandatory and optional functionality is defined in the MicroTCA specification MicroTCA.0, issued by the PICMG.

The design of the MCH is flexible and scalable enough to fulfil the requirements of both, telecom and non-telecom systems. The basic functionality of an MCH is to deliver switching and hub functionality for the various system fabrics as defined in the AMC.x standards such as Gigabit Ethernet, 10 GbE, PCI Express, Serial Attached SCSI (SAS) and Serial RapidIO (sRIO).

The MCH is available in four different versions based on the same technology:

- AM4904-Base
- AM4904-PCIe
- AM4904-sRIO
- AM4910

This user guide covers the AM4904 family. For information on the AM4910, please refer to appropriate manual.

1.3 Optional Accessories

The following parts are not included with the AM4904 and have to be obtained separately.

- Serial adapter cable (Order No. 1016-6698, see chapter 2.6.6)
- sRIO DensiShield cable or adapter (see chapter 2.6.9)

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1.4 Technical Specifications

1.4.1 General

- Mechanical: Single, Full-size AMC form factor
- Dimensions: 180.6 mm x 73.5 mm
  - Board Weight:
  - AM4904-Base: 350 grams max.
  - AM4904-PCIe: 400 grams max.
  - AM4904-sRIO: 400 grams max.

1.4.2 ATCA LEDs

- LED0 (blue): Ready for Hot Swap
- LED1 (red/green/yellow): Out of Service LED
- LED2 (green/amber/red): Healthy LED

1.4.3 Operating Voltages

- Management: 3.3V+/-0.33V
- Payload: 10VDC to 14VDC

1.4.4 Operation Power

- Management: 500mW max.
- Payload:
  - AM4904-Base: 26.0W max.
  - AM4904-PCIe: 40.0W max.
  - AM4904-sRIO: 35.0W max.

1.4.5 Temperature

This board is designed for operation from 0 °C to 55°C inlet air temperature.

- Normal Operating: +5 °C to +40 °C
- Short-Term Operating: -5 °C to +55 °C

1.4.6 Humidity

The board is designed to meet IEC 60068-2-78

- Operating: 5%-93% (non-condensing) at 40°C
- Non-Operating: 5%-95% (non-condensing) at 40°C

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1.4.7 Altitude

The board is designed to meet the following requirements according Belcore GR-63, Section 4.1.3:

- Operating: 4000 m (13123 ft), may require additional cooling above 1800m (5905ft)
- Non-Operating: 15000 m (49212 ft)

1.4.8 Vibration

The product is designed to meet the following requirements:

- Operating
  - 5Hz to 200Hz 0.2G, 5mm/s
  - 5HZ to 100Hz: 0.1G @ 0.1 Octave/minute
  - 5Hz to 100Hz: 1G @ 0.1 Octave/minute
  - 0.02 m^2/s^3 ASD, 5-10Hz + 12dB/oct, 10-50Hz 0dB/oct, 50-100Hz - 12dB/oct (random)
- Non-Operating
  - 5Hz to 200Hz 2G, 5mm/s
  - 0.02 m^2/s^3 ASD, 5-10Hz + 12dB/oct, 10-50Hz 0dB/oct, 50-100Hz - 12dB/oct (random)
  - 5Hz to 20Hz: 0.01g^2/Hz (random)
  - 20Hz to 200Hz: -3dB/octave (random)

1.4.9 Shock

The product is designed to meet the following requirements:

- Operating: 3G/11 ms
- Non-Operating: 18G, 6ms

1.4.10 Safety

CB report to IEC 60950-1, complies with EN/CSA/UL 60950-1.

1.4.11 Electromagnetic Compatibility

The product is designed to meet or exceed the following specifications/requirements (assuming an adequate carrier/chassis):

- FCC 47 CFR Part 15, (USA)
- EMC Directive 89/336/EEC (Europe)
- EN55022 (Europe)
- EN55024 (Europe)
- CISPR22
- CISPR24
- VCCI (Voluntary Japan Electromagnetic Compatibility requirement)

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- EN 300 386, Electro-Magnetic Compatibility (EMC) Requirements for Public Telecommunication Network Equipment; Electromagnetic Compatibility (EMC) Requirements
- Telcordia GR-1089

1.4.12 MTBF

- MTBF is min.: AM4904-Base:170,000h@40°C
- AM4904-sRIO: 148,000h@40°C
- AM4904-PCIe: 160,000h@40°C

Calculations are based on Bellcore/Telcordia SR-332, Issue 1.

1.5 Standards Compliance

This product is compatible to the following standards:

- AMC.0 R2.0 Advanced Mezzanine Card Base Specification
- AMC.1 R1.0 PCI Express (only AM4904-PCIe)
- AMC.2 R1.0 AMC Gigabit Ethernet
  - AMC.2 Type 4 E2
  - AMC.2 Type 5 E2
- AMC.4 R0.4 SerialRapidIO (only AM4904-sRIO)
- mTCA.0 R1.0
- IPMI v1.5
- IEEE 802.3

The AM4904 is RoHS compliant.

1.6 Related Publications

The following publications contain information relating to this product.

Table 1-1: Related Publications

PRODUCT	PUBLICATION
MicroTCA™	PICMG® MTCA.0 Micro Telecommunications Computing Architecture R1.0, July 6,2006
AMC	PICMG® AMC.0, Advanced Mezzanine Card Specification R1.0
IPMI	IPMI - Intelligent Platform Management Interface Specification, v1.5
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142

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Chapter 2

Functional Description

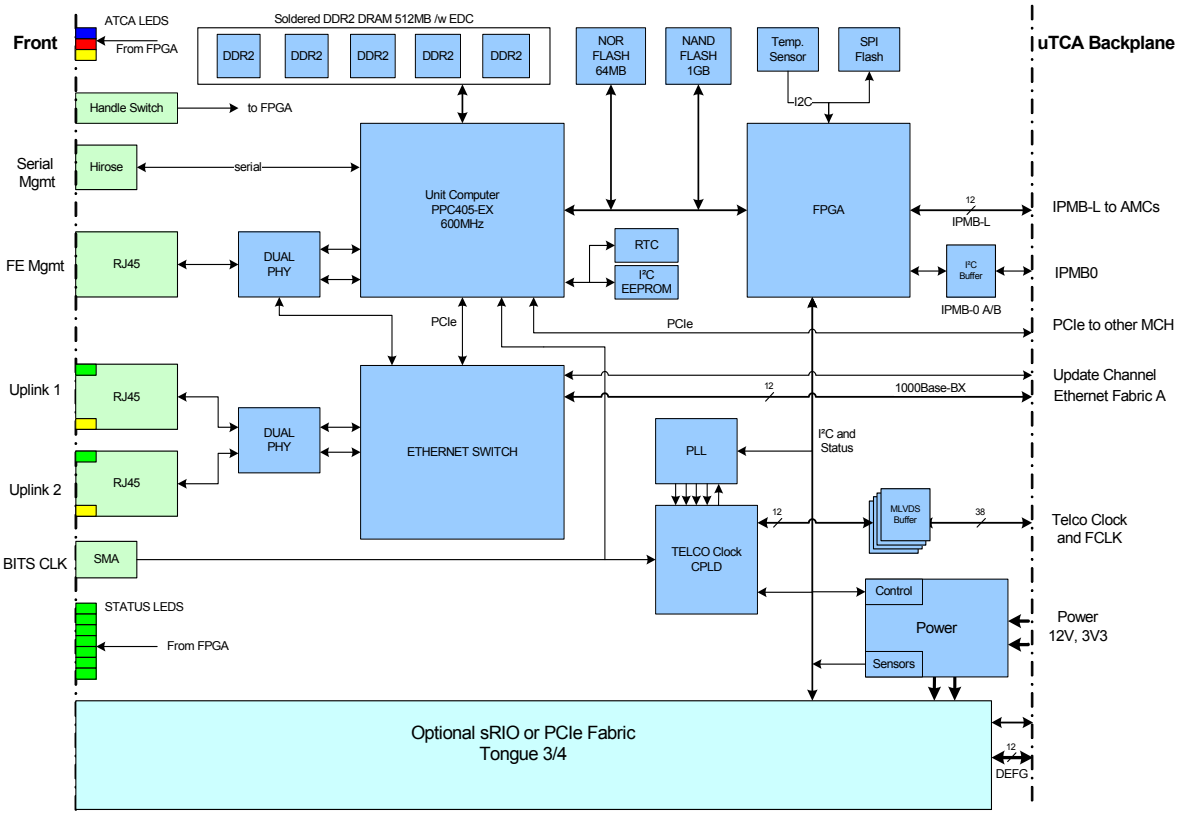
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2 Functional Description

This chapter describes the board specific items of the AM4904 MicroTCA Carrier Hub.

2.1 Block Diagrams

Figure 2-1: AM4904 Functional Block Diagram



The AM4904-Base consists of a MicroTCA Carrier Management Controller (MCMC), a managed switch and a clocking subsystem which are detailed in this chapter. The AM4904-PCIe and AM4904-sRIO variants have an additional fabric switch, see “PCI Express / Serial RapidIO Switch” on page 21.

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2.2 MicroTCA Carrier Management Controller

The AM4904 supports a processor unit which can operate as only MCMC or as MCMC/CM Software. These two modes are described in this section.

The MCMC operates with the following building blocks which are detailed below:

- Unit computer PowerPC 405EX
- DDR2 Memory
- NOR Flash
- NAND Flash
- Dual GE PHY
- FPGA
- I2C EEPROM
- Real Time Clock (RTC)
- Serial Management
- FE Management

2.2.1 Unit Computer PowerPC 405EX

One of the main components of the MCMC is the PowerPC 405EX. The following list sets out the key features of the PPC 405EX:

- PowerPC 405EX runs at 600MHZ core frequency without security feature (option -N)
- UART 1 to Front, RX, TX
- SPI to FPGA (reserved for optional FPGA update procedure)
- DDR2 SDRAM controller operates at 200MHz/400Mbps with ECC
- PCIe Port 0 lane 0 connects to Ethernet Switch
- PCIe Port 1 lane 0 connects to other MCH via XOVER0/2
- Dual Ethernet MAC operates in RGMII mode and connects to Front Management port and On-Board Switch
- EBC interface connects to FPGA and NOR/NAND Flash
- 1 PPS reference pulse input (GPIO) and timer reference clock input (TMRCLK) from either RTC or Telco PLL via FPGA

The PPC 405EX unit computer does not only implement the MCMC functionality but also hosts the GbE switch management and controls the clocking subsystem.

2.2.2 DDR2 Memory

Five DDR2 Memory modules work with the PowerPC 405EX. The key features of this Memory modules are:

- 512MB, 1024MB or 2048MB DDR2 Memory support with ECC (512MB is the standard memory size)
- 400Mbps double data rate with CAS latency of 2, 2.5 and 3

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2.2.3 NOR Flash

The NOR Flash holds Firmware, Firmware Configuration, SPD data and FRU data. The NOR FLASH could also be used for limited Logging Tracing.

- Up to 128MB NOR Flash
- Two Firmware images

2.2.4 NAND Flash

The NAND FLASH is used for high volume storage (TFTP Server applications) with high frequency read. The NAND FLASH could also be used for limited Logging Tracing.

- Up to 4GB with dual-chip select
- High Frequency Read, High Volume Storage, NAND with wear-leveling
- 1024MB standard memory size

2.2.5 Dual GE PHY

- Dual 10/100/1000Base-T Ethernet Transceiver
- Port 1 operates in RGMII to 10/100/1000Base-T mode and connects to front low profile RJ45 with integrated magnetics
- Port 2 operates in RGMII to Fiber (SerDes) mode and connects to local Switch Fabric
- Dual PHY distributes 125MHz to PPC405EX GMCRefClk

2.2.6 FPGA

The FPGA is also a main component of the MCMC and has many functions. It has the ability to be upgraded in the field. The key features of the FPGA are listed below:

- Update configuration FLASH via EBC register Interface
- FPGA Dual Image support
- 16Bit/100 MHz EBC interface to PowerPC 405EX
- 12x IPMB-L to AMC inclusive I2C Pull-Up register control
- 1x IPMB-L Cross-Over to MCH inclusive I2C Pull-Up register control
- 2x IPMB0 + Buffer Control inclusive I2C Pull-Up register control, dual slave address support
- 1x FRU Data I2C Backplane
- 3x I2C to Tongue 1, Tongue 2 and Tongue 3
- MCH-MCH interlink via XOVER1
    - Request for takeover
    - Heartbeat
    - Present
    - Isolate request
    - Switch-over request

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- RTC input/output
- LED Bus receiver
- LED distribution
- Board Option Register / Strappings (8bit)
- Watchdog
- Reset Distribution
- Slot address/Site-ID decoding

2.2.7 I2C EEPROM

The I2C EEPROM holds PowerPC 405EX configuration data. The size of the I2C EEPROM is minimum 128bit (16 Byte EEPROM bootstrap configuration content. It has a write protection by FPGA and is programmable via JTAG.

2.2.8 Real Time Clock (RTC)

The real time clock is used on the MCMC to keep accurate time. The clock has an integrated micro crystal oscillator. The oscillator's frequency is 32.768 KHz. The back-up capacity of the RTC is up to 2 weeks.

2.2.9 Serial Interface

The PowerPC 405EX is connected to the front plate of the board via a multichannel RS232 Line Transceiver. The serial RS232 interface supports the TX# and RX# signals as well as the RTS, DTR, CTS and DSR signals and operates with up to 115.2kB/s.

2.2.10 FE Management

The front panel provides a direct 10/100/1000 Base-T Ethernet connection (RJ45) to the PPC 405EX for out-of-band management and debugging purposes.

2.2.11 Board Sensors

Sensors for voltage or temperature monitoring and various others for pass/fail type signal monitoring are provided.

Every sensor is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensors identification such as sensor type, sensor name, sensor unit. SDRs also contain the configuration of a specific sensor such as thresholds, hysteresis, event generation capabilities, etc. that specify the sensor's behavior. Some fields of the sensor SDR are configurable through IPMI v1.5 command and are set to a built-in initial value.

The sensor ID is the number which identifies the sensor e.g. when using the IPMI command "Get Sensor Reading". Please note that 'ipmitool' accepts sensor IDs in decimal (e.g. '10') or hexadecimal (e.g. '0xa') notation.

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Module sensors that have been implemented are listed in the sensor list below.

Table 2-1: Sensor List AM4904-Base

Sensor ID	SENSOR Name	Sensor Type Code	Description
0	Kontron CM	MC Device Loc.	Only readable as CM
1	Kontron MCMC	MC Device Loc.	Only readable as MCMC
2	Kontron MCMC	FRU Device Loc.	Only readable as CM
3	Specified by Telco Alarm module	FRU Device Loc.	Only readable as CM and when Telco alarm module is detected
4	Health Error	24h (Platform Alert)	The sensor is an aggregation of analog sensors and shows the healthy state of the module. If the sensor is asserted the Health LED lit on amber.
5	Board Reset	CFh (OEM Kontron Reset)	Generates an event when CPU is released from reset. The reset type and reset source is encode in the event data
6	FW Ver Change	2Bh (Version Change)	Generates an event when firmware changed occurred.
7	FRU0 Reconfig	12h (System Event)	Generates when the changes configura-tion,
8	SEL State	10h (Event Logging Dis-able)	Generates an event for SEL fill state
9	ModuleHotSwap	F2h (Module Hot Swap)	Refer to AMC.0 specification.
10	IPMB0 Link State	F1h (PICMG Physical IPMB-0)	see PICMG 3.0R2.0 section 3.8.4.2 for event trigger and sensor definition
11	PLL Status	D5h OEM (PLL Status)	Generates an event when PLL status changes. The sensor only returns valid values when payload is activated.
12	IPMI Watchdog	23h (Watchdog 2)	Generates event when IPMI watchdog bites. For closer information refer to IPMI v1.5 specification.
13	T1_0x90_Temp	01h (Temperature)	For thresholds, see “Sensor Thresholds” on page 14
14	T1_0x40_V_3V3	02h (Voltage)	
15	T1_0x40_Temp	01h (Temperature)	
16	T1_0x40_V_12V	02h (Voltage)	
17	T1_0x48_V_1V8	02h (Voltage)	
18	T1_0x48_Temp	01h (Temperature)	
19	T1_0x4C_V_1V25	02h (Voltage)	
20	T1_0x4C_Temp	01h (Temperature)	
21	T2_0x54_V_1V8	02h (Voltage)	
22	T2_0x54_Temp	01h (Temperature)	
23	T2_0x5C_V_1V2	02h (Voltage)	
24	T2_0x5C_Temp	01h (Temperature)	

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Table 2-2: Sensor List AM4904-PCIe

Sensor ID	SENSOR Name	Sensor Type Code	Description
0	Kontron CM	MC Device Loc.	Only readable as CM
1	Kontron MCMC	MC Device Loc.	Only readable as MCMC
2	Kontron MCMC	FRU Device Loc.	Only readable as CM
3	Specified by Telco Alarm module	FRU Device Loc.	Only readable as CM and when Telco alarm module is detected
4	Health Error	24h (Platform Alert)	The sensor is an aggregation of analog sensors and shows the healthy state of the module. If the sensor is asserted the Health LED lit on amber.
5	Board Reset	CFh (OEM Kontron Reset)	Generates an event when CPU is released from reset. The reset type and reset source is encode in the event data
6	FW Ver Change	2Bh (Version Change)	Generates an event when firmware changed occurred.
7	FRU0 Reconfig	12h (System Event)	Generates when the changes configura-tion,
8	SEL State	10h (Event Logging Dis-able)	Generates an event for SEL fill state
9	ModuleHotSwap	F2h (Module Hot Swap)	Refer to AMC.0 specification.
10	IPMB0 Link State	F1h (PICMG Physical IPMB-0)	see PICMG 3.0R2.0 section 3.8.4.2 for event trigger and sensor definition
11	PLL Status	D5h OEM (PLL Status)	Generates an event when PLL status changes. The sensor only returns valid values when payload is activated.
12	IPMI Watchdog	23h (Watchdog 2)	Generates event when IPMI watchdog bites. For closer information refer to IPMI v1.5 specification.
13	T1_0x90_Temp	01h (Temperature)	For thresholds, see “Sensor Thresholds” on page 14
14	T1_0x40_V_3V3	02h (Voltage)	
15	T1_0x40_Temp	01h (Temperature)	
16	T1_0x40_V_12V	02h (Voltage)	
17	T1_0x48_V_1V8	02h (Voltage)	
18	T1_0x48_Temp	01h (Temperature)	
19	T1_0x4C_V_1V25	02h (Voltage)	
20	T1_0x4C_Temp	01h (Temperature)	
21	T2_0x54_V_1V8	02h (Voltage)	
22	T2_0x54_Temp	01h (Temperature)	
23	T2_0x5C_V_1V2	02h (Voltage)	
24	T2_0x5C_Temp	01h (Temperature)	
25	T3_0x48_V_1V0	02h (Voltage)	
26	T3_0x48_Temp	01h (Temperature)	

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Table 2-3: Sensor List AM4904-sRIO

Sensor ID	SENSOR Name	Sensor Type Code	Description
0	Kontron CM	MC Device Loc.	Only readable as CM
1	Kontron MCMC	MC Device Loc.	Only readable as MCMC
2	Kontron MCMC	FRU Device Loc.	Only readable as CM
3	Specified by Telco Alarm module	FRU Device Loc.	Only readable as CM and when Telco alarm module is detected
4	Health Error	24h (Platform Alert)	The sensor is an aggregation of analog sensors and shows the healthy state of the module. If the sensor is asserted the Health LED lit on amber.
5	Board Reset	CFh (OEM Kontron Reset)	Generates an event when CPU is released from reset. The reset type and reset source is encode in the event data
6	FW Ver Change	2Bh (Version Change)	Generates an event when firmware changed occurred.
7	FRU0 Reconfig	12h (System Event)	Generates when the changes configura-tion,
8	SEL State	10h (Event Logging Dis-able)	Generates an event for SEL fill state
9	ModuleHotSwap	F2h (Module Hot Swap)	Refer to AMC.0 specification.
10	IPMB0 Link State	F1h (PICMG Physical IPMB-0)	see PICMG 3.0R2.0 section 3.8.4.2 for event trigger and sensor definition
11	PLL Status	D5h OEM (PLL Status)	Generates an event when PLL status changes. The sensor only returns valid values when payload is activated.
12	IPMI Watchdog	23h (Watchdog 2)	Generates event when IPMI watchdog bites. For closer information refer to IPMI v1.5 specification.
13	T1_0x90_Temp	01h (Temperature)	For thresholds, see “Sensor Thresholds” on page 14
14	T1_0x40_V_3V3	02h (Voltage)	
15	T1_0x40_Temp	01h (Temperature)	
16	T1_0x40_V_12V	02h (Voltage)	
17	T1_0x48_V_1V8	02h (Voltage)	
18	T1_0x48_Temp	01h (Temperature)	
19	T1_0x4C_V_1V25	02h (Voltage)	
20	T1_0x4C_Temp	01h (Temperature)	
21	T2_0x54_V_1V8	02h (Voltage)	
22	T2_0x54_Temp	01h (Temperature)	
23	T2_0x5C_V_1V2	02h (Voltage)	
24	T2_0x5C_Temp	01h (Temperature)	
25	T3_0x48_V_1V2	02h (Voltage)	
26	T3_0x48_Temp	01h (Temperature)	

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2.2.11.1 Sensor Thresholds

Following tables show sensor thresholds for temperature and voltage sensors.

Table 2-4: AM4904 Temperature Sensor Thresholds [°C]

SENSOR Number / ID string	Upper non critical	Upper critical	Upper non recoverable
13 / T1_0x90_Temp	45	60	70
15 / T1_0x40_Temp	115	125	135
18 / T1_0x48_Temp	115	125	135
20 / T1_0x4C_Temp	115	125	135
22 / T2_0x54_Temp	115	125	135
24 / T2_0x5C_Temp	115	125	135
26 / T3_0x48_Temp (AM4904-PCIe and AM4904-sRIO only)	115	125	135

Table 2-5: AM4904 Voltage Sensor Thresholds

SENSOR Number / ID string	Lower critical	Nominal	Upper critical
14 / T1_0x40_V_3V3	3.13	3.30	3.46
16 / T1_0x40_V_12V	9.96	12.00	13.98
17 / T1_0x48_V_1V8	1.70	1.80	1.90
19 / T1_0x4C_V_1V25	1.20	1.25	1.30
21 / T2_0x54_V_1V8	1.70	1.80	1.90
23 / T2_0x5C_V_1V2	1.15	1.20	1.26
25 / T3_0x48_V_1V0 (AM4904-PCIe only)	0.84	1.00	1.15
25 / T3_0x48_V_1V2 (AM4904-sRIO only)	1.15	1.20	1.26

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2.2.11.2 Supported Sensor Type Codes and Event offsets

Table 2-6: Sensor Type Codes and Event offsets

Sensor Type Code	Event type code/event offsets
24h (platform alarm)	03h (discrete)
CFh (Kontron OEM Reset)	03h (discrete) Offset 0: Event Data2: Reset Type 0 – Unknown 1 – Cold Reset 2 – Warm Reset Event Data3: Reset Source 0 – IPMI Watchdog 1 – IPMI command 2 – not used 3 – not used 4 – not used 5 – Power up 6 – PPC watchdog 7 – not used 8 – Software Initiated 9 – Setup / XOVER FFh - unknown
2Bh (Version Change)	See IPMI 2.0
12h (System Event)	6Fh (Sensor Specific) Offset 0: Sensor population changed (insertion or extraction of a module)
10h (Event Logging Disabled)	6Fh (Sensor Specific) Offset 2: Log Area Reset/cleared Offset 4: Log Area full Offset 5: Log Area almost full (75%)
F2h (PICMG Module Hotswap)	See AMC.0 R2.0 standard
F1h (PICMG Physical Link state)	See PICMG 3.0 standard
D5h (Kontron OEM PLL Status)	6Fh (Sensor Specific) Offset 0: PLL locked to primary reference clock (assertion) Offset 1: PLL locked to secondary reference clock (assertion) Offset 2: PLL in holdover mode (assertion) Offset 3: PLL in free-run mode (assertion) Offset 4: PLL primary reference clock line failure (assertion/de-assertion) Offset 5: PLL secondary reference clock line failure (assertion/de-assertion)
23h (IPMI watchdog)	See IPMI 1.5
24h (platform alarm)	03h (discrete)

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2.3 Managed Ethernet Switch

The managed ethernet switch is a multilayer Gigabit Ethernet silicon which is controlled by a switching application running on the unit computer. Below, the switch and the switching application are described in more detail.

2.3.1 Fabric [A] Switch

The Ethernet infrastructure on the MCH is a highly integrated solution, combining all the functions of a high-speed switch system. The switch silicon provides 16 GbEthernet ports. Each GbE port can be configured in SGMII or SerDes mode. The ports 0/1 to 0/12 are connected to the appropriate AMC slot in a MicroTCA compliant chassis. Port 0/13 is connected to the redundant MCH. Port 0/14 is used for the connection to the CPU PowerPC 405EX. Two ports (0/15 and 0/16) are connected with the dual Phy and they represent two uplink ports at the MCH faceplate.

The switch is connected to the uplinks on the front plate of the board through a dual 10/100/1000Base-T Ethernet transceiver. Uplink Ports 1 and 2 operate in SGMII to 10/100/1000Base-T mode and connect to front dual RJ45 with integrated magnetics.

The physical ports of the switch are mapped as shown in the following table.

Table 2-7: FASTPATH AM4904 Switch Port Mapping

FASTPATH unit/port	Backplane Port Map	Speed
0/1	AMC FA1	1 GbE
0/2	AMC FA2	1 GbE
0/3	AMC FA3	1 GbE
0/4	AMC FA4	1 GbE
0/5	AMC FA5	1 GbE
0/6	AMC FA6	1 GbE
0/7	AMC FA7	1 GbE
0/8	AMC FA8	1 GbE
0/9	AMC FA9	1 GbE
0/10	AMC FA10	1 GbE
0/11	AMC FA11	1 GbE
0/12	AMC FA12	1 GbE
0/13	AMC FUA	1 GbE
0/14	Unit Computer	1 GbE
0/15	Uplink GbE 1	10/100/1000 MB
0/16	Uplink GbE 2	10/100/1000 MB

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2.3.2 Switch Management Software

The switch management application is based on Broadcom FASTPATH. It is running as a Linux application on the main CPU. It coexists with the MCMC/CM application as well as customer software.

For additional information of system configuration refer to "*AM4904/AM4910 CLI Reference Manual*".

2.3.2.1 Supported Management RFCs

- RFC 826 - ARP
- RFC 854 - Telnet
- RFC 855 - Telnet Option
- RFC 1155 - SMI v1
- RFC 1157 - SNMP
- RFC 1212 - Concise MIB Definitions
- RFC 1901 - Community based SNMP v2
- RFC 2246 - The TLS Protocol, Version 1.0
- RFC 2271 - SNMP Framework MIB
- RFC 2295 - Transparent Content Negotiation
- RFC 2296 - Remote Variant Selection; RSVA/1.0 State Management "cookies"
- RFC 2346 - AES Ciphersuites for Transport Layer Security
- RFC 2576 - Coexistence between SNMP v1,v2 & v3
- RFC 2578 - SMI v2
- RFC 2579 - Textual Conventions for SMI v2
- RFC 2580 - Conformance statements for SMI v2
- RFC 3410 - Introduction and Applicability Statements for Internet Standard Management Framework
- RFC 3411 - An Architecture for Describing SNMP Management Frameworks
- RFC 3412 - Message Processing and Dispatching (December 2002)
- RFC 3413 - SNMP Applications (December 2002)
- RFC 3414 - User-based Security Model (December 2002)
- RFC 3415 - View-based Access Control Model (December 2002)
- RFC 3416 - Version 2 of SNMP Protocol Operations (December 2002)
- RFC 3417 - Transport Mappings (December 2002)
- RFC 3418 - MIB for the Simple Network Management Protocol.
- RFC 3635 - Definition of Managed Objects for Ethernet-like Interface Types
- SSL 3.0 & TLS 1.0
- SSH 1.5 & 2.0
- Draft-ietf-secsh-transport-16 - SSH Transport Layer Protocol
- Draft-ietf-secsh-userauth-17 - SSH Authentication Protocol
- DRAFT-ietf-secsh-connect-17 - SSH Connection Protocol

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- Draft-ietf-secsh-architecture-14 - SSH Protocol Architecture
- Draft-ietf-secsh-publickeyfile-03 - SECSH Public Key File Format
- Draft-ietf-secsh-dh-group-exchange-04 - Diffie-Hellman Group exchange for the SSH Transport Layer Protocol
- Configurable Management VLAN ID
- Industry Standard CLI

2.3.2.2 Supported Switching RFCs

- IEEE 802.3ac - VLAN Tagging
- IEEE 802.3ad - Link Aggregation with Static LAG and LACP support
- IEEE 802.1S - Multiple Spanning Tree
- IEEE 802.1W - Rapid Spanning Tree
- IEEE 802.1D - Spanning Tree
- GARP
- GVRP - Dynamic VLAN Registration
- GMRP - Dynamic L2 Multicast Registration
- IEEE 802.1Q - Virtual LANs with Port Based VLANs
- IEEE 802.1v - Protocol based VLANs
- IEEE 802.1p - Ethernet Priority with User Provisioning & Mapping
- IEEE 802.1X - Port Authentication
- IEEE 802.3x - Flow Control
- IGMP Snooping
- Port Mirroring
- Broadcast Storm Recovery
- Static MAC Filtering
- Double VLAN / vMAN Tagging
- Jumbo Frames
- IPv6 Classification APIs
- XMODEM
- RFC 768 - UDP
- RFC 783 - TFTP
- RFC 791 - IP
- RFC 792 - ICMP
- RFC 793 - TCP
- RFC 951 - BOOTP
- RFC 1321 - Message Digest Algorithm (MD5)
- RFC 1534 - Interoperation between BOOTP and DHCP

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- RFC 2030 - Simple Network Time Protocol (SNTP) Version 4 for IPv4, IPv6 and OSI
- RFC 2131 - DHCP Client
- RFC 2131 - DHCP Server
- RFC 2132 - DHCP Options and BOOTP Vendor Extensions
- RFC 2865 - RADIUS Client
- RFC 2866 - RADIUS Accounting
- RFC 2868 - RADIUS Attributes for Tunnel Protocol Support
- RFC 2869 - RADIUS Extensions
- rfc2869bis - RADIUS support for EAP
- RFC 3176 - InMon Corporation's sFlow: A Method for Monitoring Traffic in Switched and Routed Networks
- RFC 3396 - Encoding Long Option in the Dynamic Host Configuration Protocol (DHCPv4)
- RFC 3580 - 802.1X RADIUS Usage Guidelines
- Draft-ietf-magma-snoop-11.txt - Considerations for IGMP and MLD Snooping Switches

2.3.2.3 Supported QoS

- Bandwidth Policing (Min and Max; per port/per VLAN)
- Committed Information Rate (CIR)
- Maximum Burst Rate (MBR)
- Per Port (Interface)
- Per VLAN
- Filtering (L3/L4 Access Lists)
- IP Classification - 6 Tuple Classification
- RFC 2474 - DiffServ Definition
- RFC 2475 - DiffServ Architecture
- RFC 2597 - Assured Forwarding PHB
- RFC 3246 - An Expedited Forwarding PHB
- RFC 3260 - New Terminology and Clarifications for DiffServ

Additionally the software supports the following MIBs.

2.3.2.4 Supported Enterprise MIB

- Support for all managed objects not contained in standards based MIBs

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2.3.2.5 Supported Switching Package MIBs

- RFC 1213 - MIB-II
- RFC 1493 - Bridge MIB: Definitions of Managed Objects for Bridges (dot1d)
- RFC 1643 – Definitions of managed objects for the Ethernet-like interface types
- RFC 2233 - The Interfaces Group MIB using SMI v2
- RFC 2618 - RADIUS Authentication Client MIB
- RFC 2620 - RADIUS Accounting MIB
- RFC 2674 - VLAN & Ethernet Priority MIB: The Bridge MIB Extension module for managing Priority and Multicast Filtering, defined by IEEE 802.1D-1998.
- RFC 2674 - Q-BRIDGE-MIB: The VLAN Bridge MIB module for managing Virtual Bridged Local Area Networks
- RFC 2737 – Entity MIB version 2
- RFC 2819 - RMON Groups 1,2,3 & 9
- RFC 2863 – Interfaces Group MIB
- RFC 3291 - Textual Conventions for Internet Network Addresses
- RFC 3635 - Etherlike-MIB: Definitions of Managed Objects for the Ethernet-like Interface Types
- IANA-ifType-MIB
- IEEE 802.1X MIB (IEEE8021-PAE-MIB)
- IEEE 802.3AD MIB (IEEE8021-AD-MIB)
- IEEE 802.1AB – LLDP MIB
- ANSI/TIA 1057 – LLDP-MED MIB
- RADIUS-ACC-CLIENT-MIB: RADIUS Accounting Client MIB
- RADIUS-AUTH-CLIENT-MIB: RADIUS Authentication Client MIB

2.3.2.6 Supported QoS Package MIBs

- RFC 3289 - DIFFSERV-MIB: Management Information Base for the Differentiated Services Architecture
- RFC 3289 - DIFFSERV-DCSP-TC MIB: Management Information Base for the Textual Conventions used in DIFFSERV-MIB

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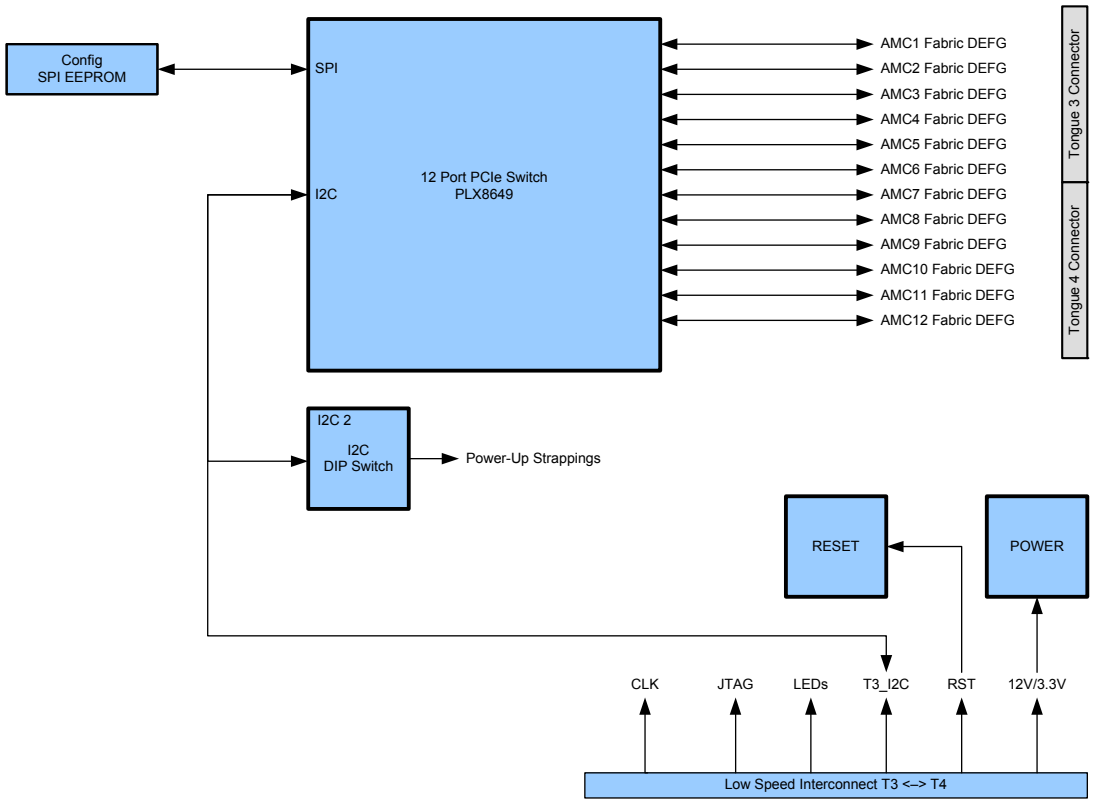
2.3.2.7 Supported SNMP MIBs

- RFC 1907 - SNMPv2-MIB: The MIB module for SNMPv2 entities
- SNMP-COMMUNITY-MIB: This MIB module defines objects to help support coexistence between SNMPv1, SNMPv2 and SNMPv3
- SNMP-FRAMEWORK-MIB: The SNMP Management Architecture MIB
- SNMP-MPD-MIB: The MIB for Message Processing and Dispatching
- SNMP-NOTIFICATION-MIB: The Notification MIB Module
- SNMP-TARGET-MIB: The Target MIB Module
- SNMP-USER-BASED-SM-MIB: The management information definitions for the SNMP User-based Security Model
- SNMP-VIEW-BASED-ACM-MIB: The management information definitions for the View-based Access Control Model for SNMP

2.4 PCI Express / Serial RapidIO Switch

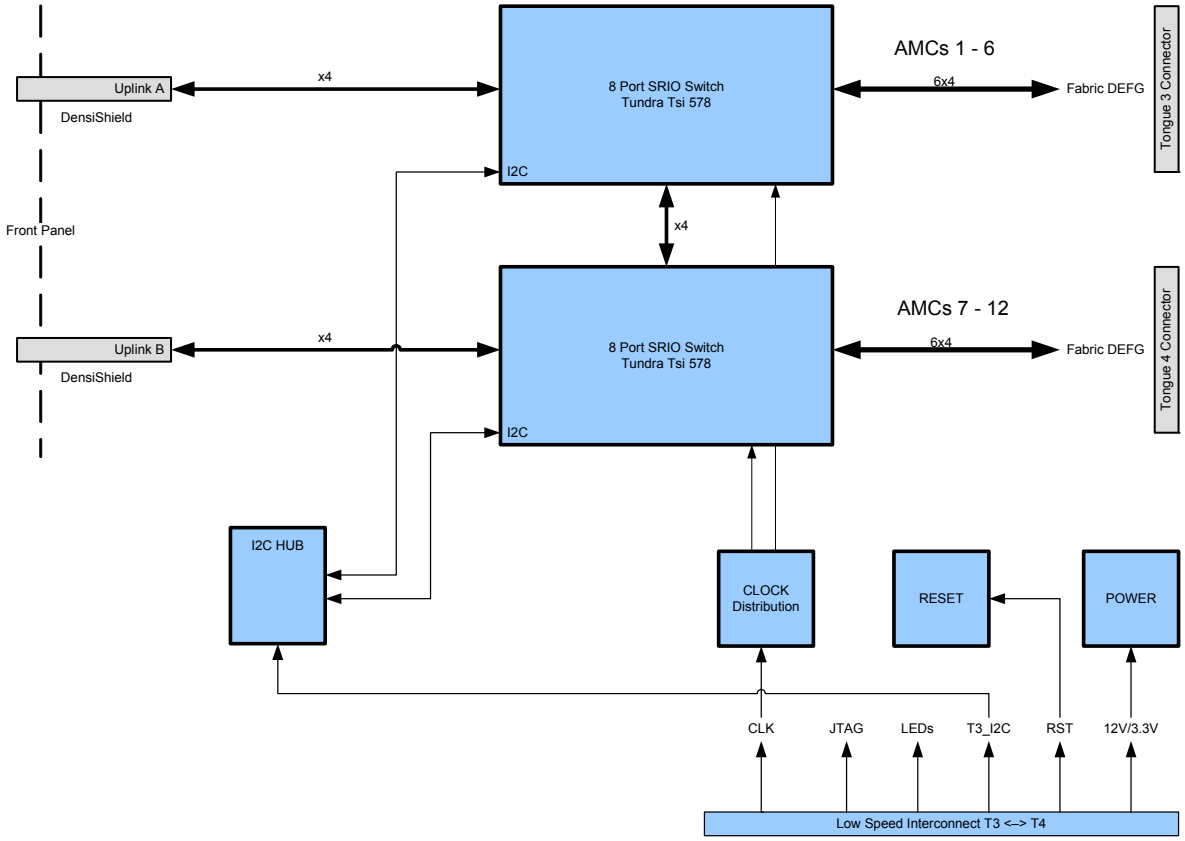
The following figures show block diagrams of the sRIO and the PCIe fabrics. For information about PCIe configuration, see “Configuring PCI Express” on page 62, for information about sRIO configuration, see “Configuring sRIO” on page 64.

Figure 2-2: PCIe fabric



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Figure 2-3: sRIO fabric



The physical ports of the fabric switch are mapped as shown in the following tables.

Table 2-8: AM4904-PCIe Switch Port Mapping

Switch Station	Switch Station Port	Switch Port	Lanes	Port Mapping
0	0	0	0-3	AMC Fabric DEFG 1
		1	4-7	AMC Fabric DEFG 2
		2	8-11	AMC Fabric DEFG 3
		3	12-15	AMC Fabric DEFG 4
5	20	20	16-19	AMC Fabric DEFG 5
		21	20-23	AMC Fabric DEFG 6
		22	28-31	AMC Fabric DEFG 7
		23	24-27	AMC Fabric DEFG 8
4	16	16	32-35	AMC Fabric DEFG 9
		17	36-39	AMC Fabric DEFG 10
		18	40-43	AMC Fabric DEFG 11
		19	44-47	AMC Fabric DEFG 12

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Table 2-9: AM4904-sRIO Switch Port Mapping

sRIO Switch Unit #	Port #	Port Mapping	Speed (Default)
0	P0	SW interlink	3.125Gbps
	P2	AMC Fabric DEFG 6	3.125Gbps
	P4	AMC Fabric DEFG 4	3.125Gbps
	P6	AMC Fabric DEFG 1	3.125Gbps
	P8	Uplink S1 (P0)	3.125Gbps
	P10	AMC Fabric DEFG 5	3.125Gbps
	P12	AMC Fabric DEFG 3	3.125Gbps
	P14	AMC Fabric DEFG 2	3.125Gbps
1	P0	SW interlink	3.125Gbps
	P2	AMC Fabric DEFG 12	3.125Gbps
	P4	AMC Fabric DEFG 10	3.125Gbps
	P6	AMC Fabric DEFG 8	3.125Gbps
	P8	Uplink S2 (P1)	3.125Gbps
	P10	AMC Fabric DEFG 11	3.125Gbps
	P12	AMC Fabric DEFG 9	3.125Gbps
	P14	AMC Fabric DEFG 7	3.125Gbps

2.5 Clocking

The clock distribution module is part of the board and shares the CPU PowerPC 405EX and its peripherals with the Carrier Management Controller functionality. In addition the clock distribution module has its own features which are the PCIe Clock distribution and the Telco Clock Distribution.

2.5.1 PCIe Clock Distribution

- 100MHz PCIe GEN2 generator with SSC support
- 100MHz HCS GEN2 clock signal to tongue 3
- 100MHz HCS clock signal to local device (optional)
- CLK3-[12:1]_P/N HCS outputs to AMC[12:1]

2.5.2 Telco Clock Distribution

- CLK1-[12:1]_M-LVDS input/outputs to/from AMCs
- CLK2-[12:1]_M-LVDS inputs/outputs to/from AMCs
- CLK1_RX_M-LVDS input from other MCH
- CLK1_TX_M-LVDS output to other MCH
- CLK3_RX_M-LVDS input from other MCH
- CLK3_TX_M-LVDS output to other MCH

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- Zarlink ZL30143 SyncE 10GE/GE/SONET/SDH G.8262/Stratum 3 System Synchronizer/Sets PLL
- Stratum 3 Accuracy
  - Long Term Accuracy (20 years): ±4.6 ppm
  - Short Term Stability (24 hours): ±0.37 ppm
  - Frequency Drift Rate: ±4.63x10e-13
- SONET/SDH/PDH System Timing Module
  - Input references from BITS input, other MCH or AMC
    - 1 PPS
    - 2 KHz
    - 8 KHz, and multiple of 8 kHz up to 77.76MHz
    - 1.544 MHz
    - 2.048 MHz
    - 8.192 MHz
    - 16.384 MHz
    - 19.44 MHz
    - 25 MHz
    - 62.5 MHz
    - 125 MHz
    - 155.52 MHz
    - 10 MHz
  - Input reference monitoring for frequency and phase irregularities
  - Output frequencies 8kHz, 1.544MHz, 2.048MHz, 19.44MHz and multiples of 8kHz up to 100MHz
  - Hardware quality level of GR-1244 Stratum 3
  - Module supports free-run, hold-over and phase-locked
  - Meets jitter, wander, holdover and other performance specifications detailed in Telecordia GR-253-CORE (SONET) or ITU-T G.813 (SDH)
  - The input voltage range is from 0V to 5V with a minimum input level of 300mVpp. The input is AC coupled
  - The SMA input is terminated with 50 Ohm
- Synchronous Ethernet System Timing Module
  - Synchronizes to 25MHz, recovered clock from local front-uplink Ethernet PHYs
  - Transmits 25MHZ to local PHYs and switch silicon reference clock
  - G.8262

2.6 Board Interfaces

The AM4904 has following front panel interfaces:

- 10/100Base-T Management Port with LEDs
- Serial RS232 Interface
- BITS Clock Input (CLK)
- Dual 10/100/1000Base-T Uplink (GbE1, GbE2) with LEDs

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- Module Management LEDs (Out-Of-Service, Health, Hot Swap)
- AMC Status LEDs (AMC)
- Other MCH Status LED (other MCH)
- Synchronisation Clock LEDs (Lock, Hold, Free)
- Power Module and Cooling Unit Status LEDs (PM1/2, CU1/2)
- Module Handle

Figure 2-4: AM4904-Base Front Panel LEDs and Interfaces

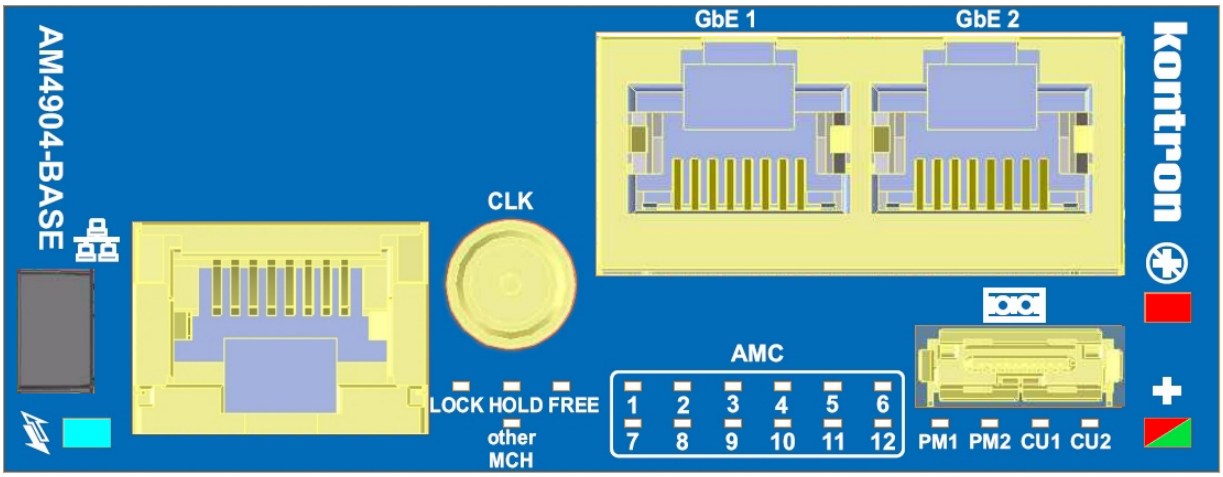
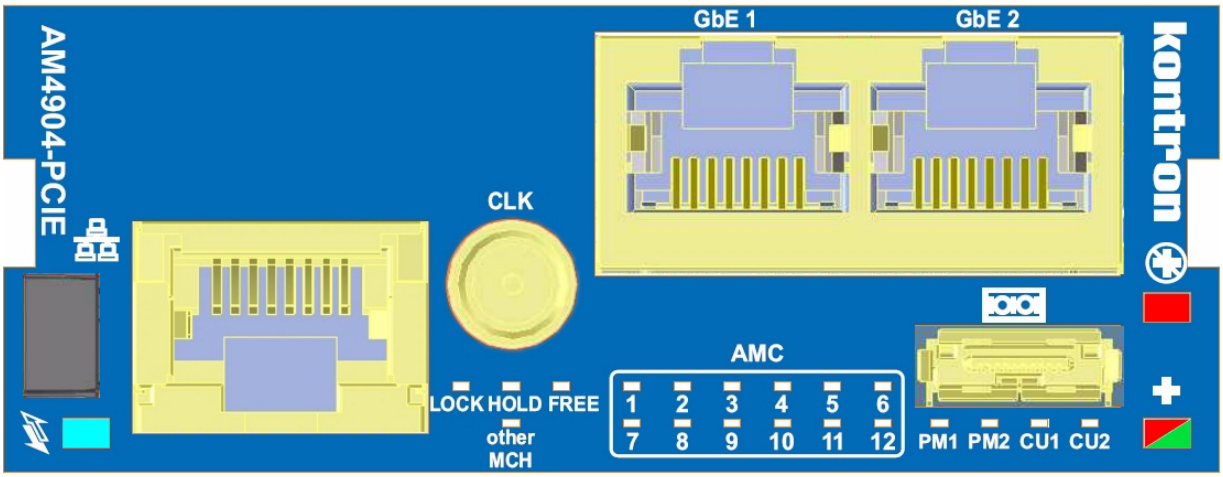
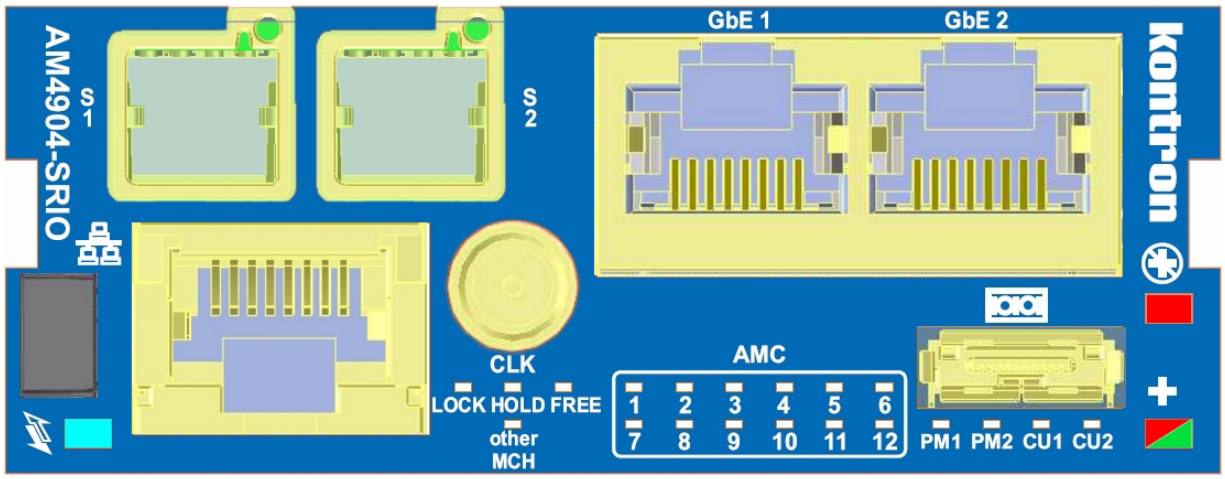


Figure 2-5: AM4904-PCIe Front Panel LEDs and Interfaces



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Figure 2-6: AM4904-sRIO Front Panel LEDs and Interfaces



2.6.1 Module Management LEDs

Table 2-10: Module Management LEDs Function

Module Management LEDs	Color	Description
LED1 (Out-of-Service LED)	red	OFF= MCH is operational ON= MCH boots-up or is not operational. Blinking= Not defined
	amber	OFF= MCH is operational and assigned the 'active MCH' role ON= MCH boots-up or is not operational. (alternative to red for certain countries) Blinking= Not defined
	green	Not mandatory OFF= Not defined ON= MCH is operational and assigned the 'Standby MCH 'role

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Table 2-10: Module Management LEDs Function

Module Management LEDs	Color	Description
LED2 (Health LED)	red	Not mandatory OFF= Not defined ON= Not defined Blinking= Not defined
	amber	OFF= Not defined ON= The payload is on and at least one health sensor is asserted Blinking= Not defined
	green	ON= The payload is on and all sensors related are in range. None of the health sensors is asserted. MCH is assigned the 'active MCH' role Blinking= The payload is on and all sensors related are in range. None of the health sensors is asserted. MCH is assigned the 'standby MCH' role
HS LED (Hot Swap LED)	blue	OFF= MCH is in M3 or M4 state, normal state when module is in operation. ON= MCH is ready for hot swap Short blink= Module is in M5 state (Deactivation Request) or in M6 state (Deactivation in progress) Long blink= Deactivation in progress

2.6.2 MCH/AMC Status LEDs

The AM4904 delivers 12 AMC and 1 other MCH status LEDs.

Indication parameters are customized per CLI command (see “Managed Ethernet Switch” on page 16). AMC LEDs can indicate:

- Present of AMC or other MCH (default), or
- M4/M5 (Payload active state) of AMC or other MCH, or
- Fabric A link up of AMC or other MCH, or
- Fabric DEFG link up of AMC or other MCH

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Table 2-11: AMC and other MCH LEDs

LED	Color	Description
AMC1	green	OFF: AMC not present or incompatible (default), or AMC is not in M4/M5 (Payload active) state, or AMC Fabric A link is down, or AMC Fabric DEFG is down ON: AMC is present (default), or AMC is in M4/M5 (Payload active) state, or AMC Fabric A link is up, or AMC Fabric DEFG is up
AMC2	green	
AMC3	green	
AMC4	green	
AMC5	green	
AMC6	green	
AMC7	green	
AMC8	green	
AMC9	green	
AMC10	green	
AMC11	green	
AMC12	green	
other MCH	green	OFF: Other MCH not present or incompatible (default), or Other MCH is not in M4/M5 (Payload active) state, or Other MCH Fabric A link is down, or Other MCH Fabric DEFG is down ON: Other MCH is present (default), or Other MCH is in M4/M5 (Payload active) state, or Other MCH Fabric A link is up, or Other MCH Fabric DEFG is up

2.6.3 Synchronisation Clock LEDs

Table 2-12: Synchronisation Cock LEDs

LED	Color	Description
Lock	green	OFF= PLL not locked to reference input ON= PLL is frequency and phase locked to reference input Blinking= Not defined
Hold	green	OFF= PLL is locked or in free running mode ON= PLL is in holdover mode Blinking= Not defined
Free	green	OFF= PLL is locked or in hold over mode or no Telco Clock support ON= PLL is in free running mode Blinking= Not defined

The PLL Status is displayed by the combination of the LOCK and HOLD LED, according to following table.

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Table 2-13: PLL Status

LOCK	HOLD	Description
Low	Low	Free running mode.
Low	High	PLL is in holdover mode.
High	Low	PLL is locked.
High	High	PLL is not present.

2.6.4 Power Module and Cooling Unit Status LEDs

The AM4904 LEDs for PM indicates communication to the first 2 PM in the MicroTCA chassis.

Table 2-14: MCH LED Status

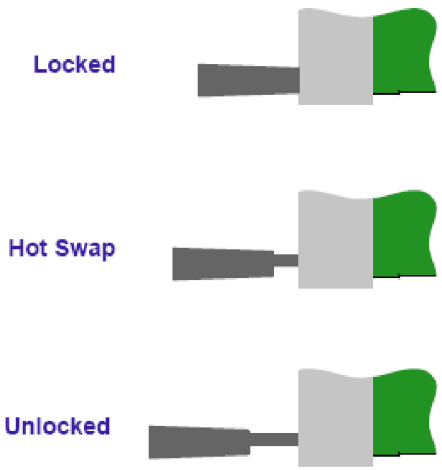
MCH	Color	Description
PM1	green	OFF= No IPMB0 communication to PUx ON= IPMB0 communication established Blinking=: Not defined
PM2		
CU1	green	OFF= No IPMB0 communication to CUx ON= IPMB0 communication established Blinking= Not defined
CU2		

2.6.5 Module Handle Positions

At the front panel, the AM4904 provides a module handle for module extraction for securing the module in the chassis and actuating the hot swap switch.

The module handle supports a three-position operation.

Figure 2-7: Module Handle Positions



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Table 2-15: Module Handle Positions

Module Handle Position	Function
Locked	When the AM4904 is installed, the module handle is pushed in the "Locked" position and the following actions result: • The module is locked in the chassis • The hot swap switch is actuated
Hot Swap	When an extraction process of the AM4904 is initiated, the module handle is pulled in the "Hot Swap" position and the following actions result: • The module is locked in the chassis • The hot swap switch is deactivated
Unlocked	When the module handle is pulled to the "Unlocked" position, the AM4904 can be fully extracted and the following actions result: • The module is unlocked in the chassis • The hot swap switch is deactivated

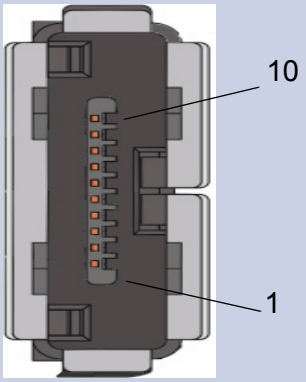
Note...

For normal operation, the module handle must be in the "Locked" position.

2.6.6 Serial Port

An RS232 interface of the Unit Computer is the serial port which is routed to a miniature connector on the front plate. An adapter cable is available from Kontron to establish a connection with a terminal with a standard DB9 serial port.

Table 2-16: Serial Port Pinout

Pin Number	Signal	
1	N.C.	
2	RXD	
3	TXD	
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	N.C.	
10	N.C.	

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2.6.7 Management Ethernet Interface (10/100/1000Base-T)

The default setting of the PHY is to operate in auto-negotiation enabled mode, 10/100/1000, Full or Half duplex. The LEDs indicate Link/Activity (LED: Green) and Speed (LED: Green).

The standard RJ45 connector has the following pin assignment:

Table 2-17: Management RJ45 Connector Pin Assignment

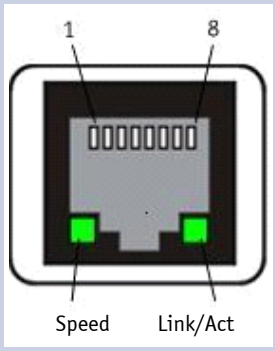
Pin	Function	
1	TX+	
2	TX-	
3	RX+	
4	NU	
5	NU	
6	RX-	
7	NU	
8	NU	

Table 2-18: Management LEDs Signification

	Green LED (Link/Activity)
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity
	Green LED (Speed)
OFF	10/100 Mbps reduced speed
ON	1000 Mbps
BLINKING	Not defined

2.6.8 Uplink Ethernet Ports

2.6.8.1 10/100/1000Base-T Ports

The 2 uplink Ethernet ports provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation) and are implemented as an RJ-45 connector on the front panel. Auto wire switching for crossed cables is also supported (Auto-MDI/X). This interface is connected as an uplink port to the on-board Ethernet switch.

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The following figure and table provide pinout information on the Gigabit Ethernet connectors.

Table 2-19: GbE Connector

Pin	Signal 10/100Base-T	Signal 1000Base-T
1	TX+	BI-DA+
2	TX-	BI-DA-
3	RX+	BI-DB+
4	NU	BI-DC+
5	NU	BI-DC-
6	RX-	BI-DB-
7	NU	BI-DD+
8	NU	BI-DD-

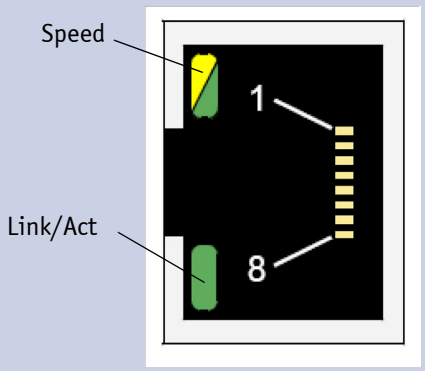


Table 2-20: Ethernet LED Status

	Green LED (Link/Activity)
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity
	Green LED (Speed)
OFF and ACT ON	10Base-T connection
ON	100Base-TX connection
BLINKING	Not defined
	Yellow LED (Speed)
OFF and ACT ON	10Base-T connection
ON	1000Base-T connection
BLINKING	Not defined

2.6.9 sRIO DensiShield™ Interfaces

The two front DensiShield™ uplink connectors provide cable access to the sRIO Fabric switch. The ports are numbered on the front panel overlay.

Table 2-21: sRIO Connections

Port	Connection
S1	Switch Unit 0 P8
S2	Switch Unit 1 P8

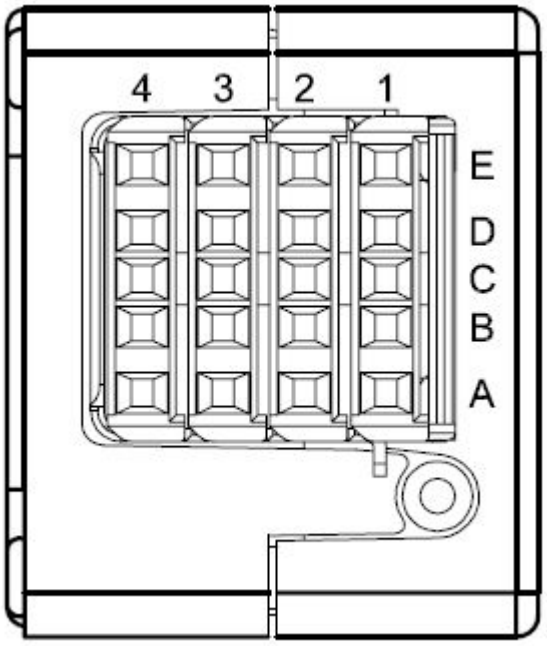
DensiShield™ cables or adapters can be obtained from FCI and other manufacturers. The connector pinout is as follows.

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Table 2-22: DensiShield™ Uplink Connector Pinout

DensiShield™ Connector		Column			
		1	2	3	4
Row	E	SRIO_Px_RX0+	SRIO_Px_RX1+	SRIO_Px_RX2+	SRIO_Px_RX3+
	D	SRIO_Px_RX0-	SRIO_Px_RX1-	SRIO_Px_RX2-	SRIO_Px_RX3-
	C	GND	GND	GND	GND
	B	SRIO_Px_TX0-	SRIO_Px_TX1-	SRIO_Px_TX2-	SRIO_Px_TX3-
	A	SRIO_Px_TX0+	SRIO_Px_TX1+	SRIO_Px_TX2+	SRIO_Px_TX3+

Figure 2-8: DensiShield™ Uplink Cable Connector Face (Front Connector is mirrored)



Note...

When selecting a DensiShield™ to InfiniBand adapter, note that there are different wiring options available. Be sure to select the version where the polarity is not inverted. The correct wiring is given in the table below.

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Table 2-23: DensiShield™ to InfiniBand Adapter Wiring

DensiShield™	Signal (DensiShield™)	Infiniband
C1-C4	GND	G1-G9
A1	TX0+	S1
B1	TX0-	S2
D1	RX0-	S15
E1	RX0+	S16
A2	TX1+	S3
B2	TX1-	S4
D2	RX1-	S13
E2	RX1+	S14
A3	TX2+	S5
B3	TX2-	S6
D3	RX2-	S11
E3	RX2+	S12
A4	TX3+	S7
B4	TX3-	S8
D4	RX3-	S9
E4	RX3+	S10

2.7 MCH Interconnection

The AM4904 communicates with the MicroTCA™ backplane via the MCH Card-edge connector, which is a serial interface optimized for high-speed interconnects. The MCH Card-edge connectors support a variety of fabric topologies divided into the following functional groups:

- Fabric interface
- MCH-specific interfaces, such as:
  - IPMB-L interface
  - IPMB-0 interface
  - MCH update channel interface
  - MCH PWR_ON interface
- JTAG interface
- CLK1, CLK2 and CLK3 interfaces

The following sections provide detailed information on these interfaces.

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2.7.1 Fabric Interface

The MicroTCA™ backplane provides optional Fabric connectivity to each of the supported AMCs and between the MCHs on Tongue 1 (Fabric [A]) and Tongues 3 and 4 (Fabric [DEFG]).

The AM4904-Base provides support for Fabric [A], GbE for 12 AMC ports and the MCH interlink.

Equipped with additional sRIO and PCIe fabric boards the product provides support for Fabric [DEFG] for 12 AMCs and the MCH interlink.

2.7.2 IPMB-L Interface

The IPMB-L interface of the AM4904 serves 12 discrete interfaces to tongue 1. These interfaces provide the E-Keying information as well as all other management information between the MCH and the AMCs. On the MCH, all 12 AMC interfaces are combined via a switch matrix to one interface, which is presented to the MCMC.

2.7.3 IPMB-0 Interface

The IPMB-0 interface, consisting of the IPMB-0 [A] and the IPMB-0 [B] interfaces, is used for the communication between the MCH and the power modules as well as between the MCH and the cooling units in a MicroTCA™ system to control the power served to the dedicated AMCs as well as the system cooling state.

2.7.4 MCH Update Channel Interface

The MCH update channel on the AM4904 is realized as a SerDes interface to the on-board Ethernet switch. Thus, two MCHs can be interconnected across the MicroTCA backplane.

2.7.5 JTAG Interface

JTAG support is provided on the MCH Card-edge connector. The JTAG interface is used for vendor product test and logic update.

On the AM4904, the PLD JTAG port is connected to the debug JTAG connector.

2.7.6 Pinout of MCH Card-edge Connectors

The MCH Card-edge connectors are a high-speed serial interface with 170 pins. The following table provides the pinout of the MCH Card-edge connectors.

Table 2-24: MCH Card-edge Tongue 1 Connectors Pinout

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
85	GND		First	Logic-Ground	86	GND		First	Logic-Ground
84	PWR	PM	First	Payload-Power	87	IPMBL-SDA-12	IPMI-Agent	Third	IPMB-L to AMC12
83	PS0#	BkPLane (GND)	Last	MCH Presence	88	IPMBL-SCL-12	IPMI-Agent	Third	IPMB-L to AMC12
82	GND		First	Logic-Ground	89	GND		First	Logic-Ground
81	XOVER2-	Other-MCH	Third	Cross-over_Interface2-	90	IPMBL-SDA-11	IPMI-Agent	Third	IPMB-L to AMC11

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Table 2-24: MCH Card-edge Tongue 1 Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mat-ing	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
80	XOVER2+	Other-MCH	Third	Cross-over_Interface2+	91	IPMBL-SCL-11	IPMI-Agent	Third	IPMB-L to AMC11
79	GND		First	Logic-Ground	92	GND		First	Logic-Ground
78	XOVER1-	MCH-Other-MCH	Third	Cross-over_Interface1-	93	IPMBL-SDA-10	IPMI-Agent	Third	IPMB-L to AMC10
77	XOVER1+	MCH-Other-MCH	Third	Cross-over_Interface1+	94	IPMBL-SCL-10	IPMI-Agent	Third	IPMB-L to AMC10
76	GND		First	Logic-Ground	95	GND		First	Logic-Ground
75	XOVER0-	MCH	Third	Cross-over_Interface0-	96	IPMBL-SDA-9	IPMI-Agent	Third	IPMB-L to AMC9
74	XOVER0+	MCH	Third	Cross-over_Interface0+	97	IPMBL-SCL-9	IPMI-Agent	Third	IPMB-L to AMC9
73	GND		First	Logic-Ground	98	GND		First	Logic-Ground
72	PWR	PM	First	Payload-Power	99	IPMBL-SDA-8	IPMI-Agent	Third	IPMB-L to AMC8
71	SDA_L	MCH-Other-MCH	Second	IPMB-L Cross-over Data	100	IPMBL-SCL-8	IPMI-Agent	Third	IPMB-L to AMC8
70	GND		First	Logic-Ground	101	GND		First	Logic-Ground
69	RxFA-12-	AMC-12	Third	Fabric A to AMC12, Receive-	102	IPMBL-SDA-7	IPMI-Agent	Third	IPMB-L to AMC7
68	RxFA-12+	AMC-12	Third	Fabric A to AMC12, Receive+	103	IPMBL-SCL-7	IPMI-Agent	Third	IPMB-L to AMC7
67	GND		First	Logic-Ground	104	GND		First	Logic-Ground
66	TxFA-12-	MCH	Third	Fabric A to AMC12 Transmit-	105	IPMBL-SDA-6	IPMI-Agent	Third	IPMB-L to AMC6
65	TxFA-12+	MCH	Third	Fabric A to AMC12 Transmit+	106	IPMBL-SCL-6	IPMI-Agent	Third	IPMB-L to AMC6
64	GND		First	Logic-Ground	107	GND		First	Logic-Ground
63	RxFA-11-	AMC-11	Third	Fabric A to AMC11, Receive-	108	IPMBL-SDA-5	IPMI-Agent	Third	IPMB-L to AMC5
62	RxFA-11+	AMC-11	Third	Fabric A to AMC11, Receive+	109	IPMBL-SCL-5	IPMI-Agent	Third	IPMB-L to AMC5
61	GND		First	Logic-Ground	110	GND		First	Logic-Ground
60	TxFA-11-	MCH	Third	Fabric A to AMC11 Transmit-	111	IPMBL-SDA-4	IPMI-Agent	Third	IPMB-L to AMC4
59	TxFA-11+	MCH	Third	Fabric A to AMC11 Transmit+	112	IPMBL-SCL-4	IPMI-Agent	Third	IPMB-L to AMC4
58	GND		First	Logic-Ground	113	GND		First	Logic-Ground
57	PWR	PM	First	Payload-Power	114	IPMBL-SDA-3	IPMI-Agent	Third	IPMB-L to AMC3
56	SCL_L	MCH-Other-MCH	Second	IPMB-L Cross-over Clock	115	IPMBL-SCL-3	IPMI-Agent	Third	IPMB-L to AMC3
55	GND		First	Logic-Ground	116	GND		First	Logic-Ground
54	RxFA-10-	AMC-10	Third	Fabric A to AMC10, Receive-	117	IPMBL-SDA-2	IPMI-Agent	Third	IPMB-L to AMC2
53	RxFA-10+	AMC-10	Third	Fabric A to AMC10, Receive+	118	IPMBL-SCL-2	IPMI-Agent	Third	IPMB-L to AMC2
52	GND		First	Logic-Ground	119	GND		First	Logic-Ground
51	TxFA-10-	MCH	Third	Fabric A to AMC10 Transmit-	120	IPMBL-SDA-1	IPMI-Agent	Third	IPMB-L to AMC1
50	TxFA-10+	MCH	Third	Fabric A to AMC10 Transmit+	121	IPMBL-SCL-1	IPMI-Agent	Third	IPMB-L to AMC1
49	GND		First	Logic-Ground	122	GND		First	Logic-Ground
48	RxFA-9-	AMC-9	Third	Fabric A to AMC9, Receive-	123	IPMB0-SDA-B	IPMI-Agent	Third	IPMB-0 B Data
47	RxFA-9+	AMC-9	Third	Fabric A to AMC9, Receive+	124	IPMB0-SCL-B	IPMI-Agent	Third	IPMB-0 B Clock
46	GND		First	Logic-Ground	125	GND		First	Logic-Ground

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Table 2-24: MCH Card-edge Tongue 1 Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mat-ing	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
45	TxFA-9-	MCH	Third	Fabric A to AMC9 Transmit-	126	IPMB0-SDA-A	IPMI-Agent	Third	IPMB-0 A Data
44	TxFA-9+	MCH	Third	Fabric A to AMC9 Transmit+	127	IPMB0-SCL-A	IPMI-Agent	Third	IPMB-0 A Clock
43	GND		First	Logic-Ground	128	GND		First	Logic-Ground
42	PWR	PM	First	Payload-Power	129	I2C_SDA	MCH	Third	Carrier FRU I2C Data
41	ENABLE#	Backplane	Second	Enable	130	I2C_SCL	MCH	Third	Carrier FRU I2C Clock
40	GND		First	Logic-Ground	131	GND		First	Logic-Ground
39	RxFA-7-	AMC-7	Third	Fabric A to AMC7, Receive-	132	RSVD		Third	
38	RxFA-7+	AMC-7	Third	Fabric A to AMC7, Receive+	133	TMREQ#	JTAG-Agent	Third	Test Master Request
37	GND		First	Logic-Ground	134	GND		First	Logic-Ground
36	TxFA-7-	MCH	Third	Fabric A to AMC7 Transmit-	135	RxFA-8-	AMC-8	Third	Fabric A to AMC8, Receive-
35	TxFA-7+	MCH	Third	Fabric A to AMC7 Transmit+	136	RxFA-8+	AMC-8	Third	Fabric A to AMC8, Receive+
34	GND		First	Logic-Ground	137	GND		First	Logic-Ground
33	RxFA-5-	AMC-5	Third	Fabric A to AMC5, Receive-	138	TxFA-8-	MCH	Third	Fabric A to AMC8 Trans-mit-
32	RxFA-5+	AMC-5	Third	Fabric A to AMC5, Receive+	139	TxFA-8+	MCH	Third	Fabric A to AMC8 Trans-mit+
31	GND		First	Logic-Ground	140	GND		First	Logic-Ground
30	TxFA-5-	MCH	Third	Fabric A to AMC5 Transmit-	141	RxFA-6-	AMC-6	Third	Fabric A to AMC6, Receive-
29	TxFA-5+	MCH	Third	Fabric A to AMC5 Transmit+	142	RxFA-6+	AMC-6	Third	Fabric A to AMC6, Receive+
28	GND		First	Logic-Ground	143	GND		First	Logic-Ground
27	PWR	PM	First	Payload-Power	144	TxFA-6-	MCH	Third	Fabric A to AMC6 Trans-mit-
26	GA2	Backplane	Second	Geographic Address	145	TxFA-6+	MCH	Third	Fabric A to AMC6 Trans-mit+
25	GND		First	Logic-Ground	146	GND		First	Logic-Ground
24	RxFA-3-	AMC-3	Third	Fabric A to AMC3, Receive-	147	RxFA-4-	AMC-4	Third	Fabric A to AMC4, Receive-
23	RxFA-3+	AMC-3	Third	Fabric A to AMC3, Receive+	148	RxFA-4+	AMC-4	Third	Fabric A to AMC4, Receive+
22	GND		First	Logic-Ground	149	GND		First	Logic-Ground
21	TxFA-3-	MCH	Third	Fabric A to AMC3 Transmit-	150	TxFA-4-	MCH	Third	Fabric A to AMC4 Trans-mit-
20	TxFA-3+	MCH	Third	Fabric A to AMC3 Transmit+	151	TxFA-4+	MCH	Third	Fabric A to AMC4 Trans-mit+
19	GND		First	Logic-Ground	152	GND		First	Logic-Ground
18	PWR	PM	First	Payload-Power	153	RxFA-2-	AMC-2	Third	Fabric A to AMC2, Receive-
17	GA1	Backplane	Second	Geographic Address	154	RxFA-2+	AMC-2	Third	Fabric A to AMC2, Receive+
16	GND		First	Logic-Ground	155	GND		First	Logic-Ground
15	RxFUA-	Other-MCH	Third	Fabric Update Receive-	156	TxFA-2-	MCH	Third	Fabric A to AMC2 Trans-mit-
14	RxFUA+	Other-MCH	Third	Fabric Update Receive+	157	TxFA-2+	MCH	Third	Fabric A to AMC2 Trans-mit+
13	GND		First	Logic-Ground	158	GND		First	Logic-Ground
12	TxFUA-	MCH	Third	Fabric Update Transmit-	159	RxFA-1-	AMC-1	Third	Fabric A to AMC1, Receive-
11	TxFUA+	MCH	Third	Fabric Update Transmit+	160	RxFA-1+	AMC-1	Third	Fabric A to AMC1, Receive+

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Table 2-24: MCH Card-edge Tongue 1 Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
10	GND		First	Logic-Ground	161	GND		First	Logic-Ground
9	PWR	PM	First	Payload-Power	162	TxFA-1-	MCH	Third	Fabric A to AMC1 Transmit-
8	RSVD		Second		163	TxFA-1+	MCH	Third	Fabric A to AMC1 Transmit+
7	GND		First	Logic-Ground	164	GND		First	Logic-Ground
6	RSVD		Second		165	TCK	JTAG-Agent	Third	Test Clock
5	GA0	Backplane	Second	Geographic Address	166	TMS	JTAG-Agent	Third	Test Mode Select
4	MP	PM	First	Management Power	167	TRST#	JTAG-Agent	Third	Test Reset
3	PS1#	MCH	Last	MCH Presence	168	TDO	JTAG-Agent	Third	Test Data Out
2	PWR	PM	First	Payload-Power	169	TDI	JTAG-Agent	Third	Test Data In
1	GND		First	Logic-Ground	170	PWR_ON	MCH	First	MCH/AdvancedMC Differentiator to PM(s)

Table 2-25: MCH Card-edge Tongue 2 (Clocking) Connectors Pinout

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
85	GND		First	Logic-Ground	86	GND		First	Logic-Ground
84	CLK1-12-	MCH	Third	CLK1- to AMC12	87	CLK2-12-	AMC-12	Third	CLK2- from AMC12
83	CLK1-12+	MCH	Third	CLK1+ to AMC12	88	CLK2-12+	AMC-12	Third	CLK2+ from AMC12
82	GND		First	Logic-Ground	89	GND		First	Logic-Ground
81	CLK1-11-	MCH	Third	CLK1- to AMC11	90	CLK2-11-	AMC-11	Third	CLK2- from AMC11
80	CLK1-11+	MCH	Third	CLK1+ to AMC11	91	CLK2-11+	AMC-11	Third	CLK2+ from AMC11
79	GND		First	Logic-Ground	92	GND		First	Logic-Ground
78	CLK1-10-	MCH	Third	CLK1- to AMC10	93	CLK2-10-	AMC-10	Third	CLK2- from AMC10
77	CLK1-10+	MCH	Third	CLK1+ to AMC10	94	CLK2-10+	AMC-10	Third	CLK2+ from AMC10
76	GND		First	Logic-Ground	95	GND		First	Logic-Ground
75	CLK1-9-	MCH	Third	CLK1- to AMC9	96	CLK2-9-	AMC-9	Third	CLK2- from AMC9
74	CLK1-9+	MCH	Third	CLK1+ to AMC9	97	CLK2-9+	AMC-9	Third	CLK2+ from AMC9
73	GND		First	Logic-Ground	98	GND		First	Logic-Ground
72	CLK1-8-	MCH	Third	CLK1- to AMC8	99	CLK2-8-	AMC-8	Third	CLK2- from AMC8
71	CLK1-8+	MCH	Third	CLK1+ to AMC8	100	CLK2-8+	AMC-8	Third	CLK2+ from AMC8
70	GND		First	Logic-Ground	101	GND		First	Logic-Ground
69	CLK1-7-	MCH	Third	CLK1- to AMC7	102	CLK2-7-	AMC-7	Third	CLK2- from AMC7
68	CLK1-7+	MCH	Third	CLK1+ to AMC7	103	CLK2-7+	AMC-7	Third	CLK2+ from AMC7
67	GND		First	Logic-Ground	104	GND		First	Logic-Ground
66	CLK1-6-	MCH	Third	CLK1- to AMC6	105	CLK2-6-	AMC-6	Third	CLK2- from AMC6
65	CLK1-6+	MCH	Third	CLK1+ to AMC6	106	CLK2-6+	AMC-6	Third	CLK2+ from AMC6
64	GND		First	Logic-Ground	107	GND		First	Logic-Ground
63	CLK1-5-	MCH	Third	CLK1- to AMC5	108	CLK2-5-	AMC-5	Third	CLK2- from AMC5
62	CLK1-5+	MCH	Third	CLK1+ to AMC5	109	CLK2-5+	AMC-5	Third	CLK2+ from AMC5
61	GND		First	Logic-Ground	110	GND		First	Logic-Ground
60	CLK1-4-	MCH	Third	CLK1- to AMC4	111	CLK2-4-	AMC-4	Third	CLK2- from AMC4
59	CLK1-4+	MCH	Third	CLK1+ to AMC4	112	CLK2-4+	AMC-4	Third	CLK2+ from AMC4

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Table 2-25: MCH Card-edge Tongue 2 (Clocking) Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
58	GND		First	Logic-Ground	113	GND		First	Logic-Ground
57	CLK1-3-	MCH	Third	CLK1- to AMC3	114	CLK2-3-	AMC-3	Third	CLK2- from AMC3
56	CLK1-3+	MCH	Third	CLK1+ to AMC3	115	CLK2-3+	AMC-3	Third	CLK2+ from AMC3
55	GND		First	Logic-Ground	116	GND		First	Logic-Ground
54	CLK1-2-	MCH	Third	CLK1- to AMC2	117	CLK2-2-	AMC-2	Third	CLK2- from AMC2
53	CLK1-2+	MCH	Third	CLK1+ to AMC2	118	CLK2-2+	AMC-2	Third	CLK2+ from AMC2
52	GND		First	Logic-Ground	119	GND		First	Logic-Ground
51	CLK1-1-	MCH	Third	CLK1- to AMC1	120	CLK2-1-	AMC-1	Third	CLK2- from AMC1
50	CLK1-1+	MCH	Third	CLK1+ to AMC1	121	CLK2-1+	AMC-1	Third	CLK2+ from AMC1
49	GND		First	Logic-Ground	122	GND		First	Logic-Ground
48	CLK3-6-	MCH	Third	CLK3- to AMC6	123	CLK3-12-	MCH	Third	CLK3- to AMC12
47	CLK3-6+	MCH	Third	CLK3+ to AMC6	124	CLK3-12+	MCH	Third	CLK3+ to AMC12
46	GND		First	Logic-Ground	125	GND		First	Logic-Ground
45	CLK3-5-	MCH	Third	CLK3- to AMC5	126	CLK3-11-	MCH	Third	CLK3- to AMC11
44	CLK3-5+	MCH	Third	CLK3+ to AMC5	127	CLK3-11+	MCH	Third	CLK3+ to AMC11
43	GND		First	Logic-Ground	128	GND		First	Logic-Ground
42	CLK3-4-	MCH	Third	CLK3- to AMC4	129	CLK3-10-	MCH	Third	CLK3- to AMC10
41	CLK3-4+	MCH	Third	CLK3+ to AMC4	130	CLK3-10+	MCH	Third	CLK3+ to AMC10
40	GND		First	Logic-Ground	131	GND		First	Logic-Ground
39	CLK3-3-	MCH	Third	CLK3- to AMC3	132	CLK3-9-	MCH	Third	CLK3- to AMC9
38	CLK3-3+	MCH	Third	CLK3+ to AMC3	133	CLK3-9+	MCH	Third	CLK3+ to AMC9
37	GND		First	Logic-Ground	134	GND		First	Logic-Ground
36	CLK3-2-	MCH	Third	CLK3- to AMC2	135	CLK3-8-	MCH	Third	CLK3- to AMC8
35	CLK3-2+	MCH	Third	CLK3+ to AMC2	136	CLK3-8+	MCH	Third	CLK3+ to AMC8
34	GND		First	Logic-Ground	137	GND		First	Logic-Ground
33	CLK3-1-	MCH	Third	CLK3- to AMC1	138	CLK3-7-	MCH	Third	CLK3- to AMC7
32	CLK3-1+	MCH	Third	CLK3+ to AMC1	139	CLK3-7+	MCH	Third	CLK3+ to AMC7
31	GND		First	Logic-Ground	140	GND		First	Logic-Ground
30	RSVD		Third		141	RSVD		Third	
29	RSVD		Third		142	RSVD		Third	
28	GND		Third	Logic-Ground	143	GND		Third	Logic-Ground
27	RSVD		Third		144	RSVD		Third	
26	RSVD		Third		145	RSVD		Third	
25	GND		Third	Logic-Ground	146	GND		Third	Logic-Ground
24	RSVD		Third		147	RSVD		Third	
23	RSVD		Third		148	RSVD		Third	
22	GND		Third	Logic-Ground	149	GND		Third	Logic-Ground
21	RSVD		Third		150	RSVD		Third	
20	RSVD		Third		151	RSVD		Third	
19	GND		Third	Logic-Ground	152	GND		Third	Logic-Ground
18	RSVD		Third		153	RSVD		Third	
17	RSVD		Third		154	RSVD		Third	
16	GND		Third	Logic-Ground	155	GND		Third	Logic-Ground
15	RSVD		Third		156	RSVD		Third	
14	RSVD		Third		157	RSVD		Third	
13	GND		Third	Logic-Ground	158	GND		Third	Logic-Ground

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Table 2-25: MCH Card-edge Tongue 2 (Clocking) Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
12	CLK1_Tx-	MCH	Third	CLK1 Update Transmit-	159	CLK1_Rx-	Other MCH	Third	CLK1 Update Receive-
11	CLK1_Tx+	MCH	Third	CLK1 Update Transmit+	160	CLK1_Rx+	Other MCH	Third	CLK1 Update Receive+
10	GND		First	Logic-Ground	161	GND		First	Logic-Ground
9	CLK3_Tx-	MCH	Third	CLK3 Update Transmit-	162	CLK3_Rx-	Other MCH	Third	CLK3 Update Receive-
8	CLK3_Tx+	MCH	Third	CLK3 Update Transmit+	163	CLK3_Rx+	Other MCH	Third	CLK3 Update Receive+
7	GND		First	Logic-Ground	164	GND		First	Logic-Ground
6	RSVD		Third		165	RSVD		Third	
5	RSVD		Third		166	RSVD		Third	
4	GND		Third	Logic-Ground	167	GND		Third	Logic-Ground
3	RSVD		Third		168	RSVD		Third	
2	RSVD		Third		169	RSVD		Third	
1	GND		First	Logic-Ground	170	GND		First	Logic-Ground

Table 2-26: MCH Card-edge Tongue 3 (PCIe fabric) Connectors Pinout

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
85	GND		First	Logic Ground	86	GND		First	Logic Ground
84	TxFG-6-	MCH	Third	Fabric G to AMC6 Transmit-	87	RxFG-6-	AMC-6	Third	Fabric G to AMC6 Receive-
83	TxFG-6+	MCH	Third	Fabric G to AMC6 Transmit+	88	RxFG-6+	AMC-6	Third	Fabric G to AMC6 Receive+
82	GND		First	Logic Ground	89	GND		First	Logic Ground
81	TxFF-6-	MCH	Third	Fabric F to AMC6 Transmit-	90	RxFF-6-	AMC-6	Third	Fabric F to AMC6 Receive-
80	TxFF-6+	MCH	Third	Fabric F to AMC6 Transmit+	91	RxFF-6+	AMC-6	Third	Fabric F to AMC6 Receive+
79	GND		First	Logic Ground	92	GND		First	Logic Ground
78	TxFE-6-	MCH	Third	Fabric E to AMC6 Transmit-	93	RxFE-6-	AMC-6	Third	Fabric E to AMC6 Receive-
77	TxFE-6+	MCH	Third	Fabric E to AMC6 Transmit+	94	RxFE-6+	AMC-6	Third	Fabric E to AMC6 Receive+
76	GND		First	Logic Ground	95	GND		First	Logic Ground
75	TxFD-6-	MCH	Third	Fabric D to AMC6 Transmit-	96	RxFD-6-	AMC-6	Third	Fabric D to AMC6 Receive-
74	TxFD-6+	MCH	Third	Fabric D to AMC6 Transmit+	97	RxFD-6+	AMC-6	Third	Fabric D to AMC6 Receive+
73	GND		First	Logic Ground	98	GND		First	Logic Ground
72	TxFG-5-	MCH	Third	Fabric G to AMC5 Transmit-	99	RxFG-5-	AMC-5	Third	Fabric G to AMC5 Receive-
71	TxFG-5+	MCH	Third	Fabric G to AMC5 Transmit+	100	RxFG-5+	AMC-5	Third	Fabric G to AMC5 Receive+
70	GND		First	Logic Ground	101	GND		First	Logic Ground
69	TxFF-5-	MCH	Third	Fabric F to AMC5 Transmit-	102	RxFF-5-	AMC-5	Third	Fabric F to AMC5 Receive-
68	TxFF-5+	MCH	Third	Fabric F to AMC5 Transmit+	103	RxFF-5+	AMC-5	Third	Fabric F to AMC5 Receive+
67	GND		First	Logic Ground	104	GND		First	Logic Ground
66	TxFE-5-	MCH	Third	Fabric E to AMC5 Transmit-	105	RxFE-5-	AMC-5	Third	Fabric E to AMC5 Receive-
65	TxFE-5+	MCH	Third	Fabric E to AMC5 Transmit+	106	RxFE-5+	AMC-5	Third	Fabric E to AMC5 Receive+
64	GND		First	Logic Ground	107	GND		First	Logic Ground
63	TxFD-5-	MCH	Third	Fabric D to AMC5 Transmit-	108	RxFD-5-	AMC-5	Third	Fabric D to AMC5 Receive-
62	TxFD-5+	MCH	Third	Fabric D to AMC5 Transmit+	109	RxFD-5+	AMC-5	Third	Fabric D to AMC5 Receive+
61	GND		First	Logic Ground	110	GND		First	Logic Ground
60	TxFG-4-	MCH	Third	Fabric G to AMC4 Transmit-	111	RxFG-4-	AMC-4	Third	Fabric G to AMC4 Receive-

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Table 2-26: MCH Card-edge Tongue 3 (PCIe fabric) Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
59	TxFG-4+	MCH	Third	Fabric G to AMC4 Transmit+	112	RxFG-4+	AMC-4	Third	Fabric G to AMC4 Receive+
58	GND		First	Logic Ground	113	GND		First	Logic Ground
57	TxFF-4-	MCH	Third	Fabric F to AMC4 Transmit-	114	RxFF-4-	AMC-4	Third	Fabric F to AMC4 Receive-
56	TxFF-4+	MCH	Third	Fabric F to AMC4 Transmit+	115	RxFF-4+	AMC-4	Third	Fabric F to AMC4 Receive+
55	GND		First	Logic Ground	116	GND		First	Logic Ground
54	TxFE-4-	MCH	Third	Fabric E to AMC4 Transmit-	117	RxFE-4-	AMC-4	Third	Fabric E to AMC4 Receive-
53	TxFE-4+	MCH	Third	Fabric E to AMC4 Transmit+	118	RxFE-4+	AMC-4	Third	Fabric E to AMC4 Receive+
52	GND		First	Logic Ground	119	GND		First	Logic Ground
51	TxFD-4	MCH	Third	Fabric D to AMC4 Transmit-	120	RxFD-4	AMC-4	Third	Fabric D to AMC4 Receive-
50	TxFD-4+	MCH	Third	Fabric D to AMC4 Transmit+	121	RxFD-4+	AMC-4	Third	Fabric D to AMC4 Receive+
49	GND		First	Logic Ground	122	GND		First	Logic Ground
48	TxFG-3-	MCH	Third	Fabric G to AMC3 Transmit-	123	RxFG-3-	AMC-3	Third	Fabric G to AMC3 Receive-
47	TxFG-3+	MCH	Third	Fabric G to AMC3 Transmit+	124	RxFG-3+	AMC-3	Third	Fabric G to AMC3 Receive+
46	GND		First	Logic Ground	125	GND		First	Logic Ground
45	TxFF-3-	MCH	Third	Fabric F to AMC3 Transmit-	126	RxFF-3-	AMC-3	Third	Fabric F to AMC3 Receive-
44	TxFF-3+	MCH	Third	Fabric F to AMC3 Transmit+	127	RxFF-3+	AMC-3	Third	Fabric F to AMC3 Receive+
43	GND		First	Logic Ground	128	GND		First	Logic Ground
42	TxFE-3-	MCH	Third	Fabric E to AMC3 Transmit-	129	RxFE-3-	AMC-3	Third	Fabric E to AMC3 Receive-
41	TxFE-3+	MCH	Third	Fabric E to AMC3 Transmit+	130	RxFE-3+	AMC-3	Third	Fabric E to AMC3 Receive+
40	GND		First	Logic Ground	131	GND		First	Logic Ground
39	TxFD-3-	MCH	Third	Fabric D to AMC3 Transmit-	132	RxFD-3-	AMC-3	Third	Fabric D to AMC3 Receive-
38	TxFD-3+	MCH	Third	Fabric D to AMC3 Transmit+	133	RxFD-3+	AMC-3	Third	Fabric D to AMC3 Receive+
37	GND		First	Logic Ground	134	GND		First	Logic Ground
36	TxFG-2-	MCH	Third	Fabric G to AMC2 Transmit-	135	RxFG-2-	AMC-2	Third	Fabric G to AMC2 Receive-
35	TxFG-2+	MCH	Third	Fabric G to AMC2 Transmit+	136	RxFG-2+	AMC-2	Third	Fabric G to AMC2 Receive+
34	GND		First	Logic Ground	137	GND		First	Logic Ground
33	TxFF-2-	MCH	Third	Fabric F to AMC2 Transmit-	138	RxFF-2-	AMC-2	Third	Fabric F to AMC2 Receive-
32	TxFF-2+	MCH	Third	Fabric F to AMC2 Transmit+	139	RxFF-2+	AMC-2	Third	Fabric F to AMC2 Receive+
31	GND		First	Logic Ground	140	GND		First	Logic Ground
30	TxFE-2-	MCH	Third	Fabric E to AMC2 Transmit-	141	RxFE-2-	AMC-2	Third	Fabric E to AMC2 Receive-
29	TxFE-2+	MCH	Third	Fabric E to AMC2 Transmit+	142	RxFE-2+	AMC-2	Third	Fabric E to AMC2 Receive+
28	GND		First	Logic Ground	143	GND		First	Logic Ground
27	TxFD-2-	MCH	Third	Fabric D to AMC2 Transmit-	144	RxFD-2-	AMC-2	Third	Fabric D to AMC2 Receive-
26	TxFD-2+	MCH	Third	Fabric D to AMC2 Transmit+	145	RxFD-2+	AMC-2	Third	Fabric D to AMC2 Receive+
25	GND		First	Logic Ground	146	GND		First	Logic Ground
24	TxFG-1-	MCH	Third	Fabric G to AMC1 Transmit-	147	RxFG-1-	AMC-1	Third	Fabric G to AMC1 Receive-
23	TxFG-1+	MCH	Third	Fabric G to AMC1 Transmit+	148	RxFG-1+	AMC-1	Third	Fabric G to AMC1 Receive+
22	GND		First	Logic Ground	149	GND		First	Logic Ground
21	TxFF-1-	MCH	Third	Fabric F to AMC1 Transmit-	150	RxFF-1-	AMC-1	Third	Fabric F to AMC1 Receive-
20	TxFF-1+	MCH	Third	Fabric F to AMC1 Transmit+	151	RxFF-1+	AMC-1	Third	Fabric F to AMC1 Receive+
19	GND		First	Logic Ground	152	GND		First	Logic Ground
18	TxFE-1-	MCH	Third	Fabric E to AMC1 Transmit-	153	RxFE-1-	AMC-1	Third	Fabric E to AMC1 Receive-
17	TxFE-1+	MCH	Third	Fabric E to AMC1 Transmit+	154	RxFE-1+	AMC-1	Third	Fabric E to AMC1 Receive+
16	GND		First	Logic Ground	155	GND		First	Logic Ground
15	TxFD-1-	MCH	Third	Fabric D to AMC1 Transmit-	156	RxFD-1-	AMC-1	Third	Fabric D to AMC1 Receive-
14	TxFD-1+	MCH	Third	Fabric D to AMC1 Transmit+	157	RxFD-1+	AMC-1	Third	Fabric D to AMC1 Receive+

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Table 2-26: MCH Card-edge Tongue 3 (PCIe fabric) Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
13	GND		First	Logic Ground	158	GND		First	Logic Ground
12	TxFUE-	MCH	Third	Update Channel E, Transmit-	159	RxFUE-	Other MCH	Third	Update Channel E, Receive-
11	TxFUE+	MCH	Third	Update Channel E, Transmit+	160	RxFUE+	Other MCH	Third	Update Channel E, Receive+
10	GND		First		161	GND		First	
9	TxFUD-	MCH	Third	Update Channel D, Transmit-	162	RxFUD-	Other MCH	Third	Update Channel D, Receive-
8	TxFUD+	MCH	Third	Update Channel D, Transmit+	163	RxFUD+	Other MCH	Third	Update Channel D, Receive+
7	GND		First		164	GND		First	
6	RSVD		Third		165	RSVD		Third	
5	RSVD		Third		166	RSVD		Third	
4	GND		Third		167	GND		Third	
3	RSVD		Third		168	RSVD		Third	
2	RSVD		Third		169	RSVD		Third	
1	GND		First		170	GND		First	

Table 2-27: MCH Card-edge Tongue 3 (sRIO fabric) Connectors Pinout

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
85	GND		First	Logic Ground	86	GND		First	Logic Ground
84	TxFG-6-	MCH	Third	Fabric G to AMC6 Transmit-	87	RxFG-6-	AMC-6	Third	Fabric G to AMC6 Receive-
83	TxFG-6+	MCH	Third	Fabric G to AMC6 Transmit+	88	RxFG-6+	AMC-6	Third	Fabric G to AMC6 Receive+
82	GND		First	Logic Ground	89	GND		First	Logic Ground
81	TxFF-6-	MCH	Third	Fabric F to AMC6 Transmit-	90	RxFF-6-	AMC-6	Third	Fabric F to AMC6 Receive-
80	TxFF-6+	MCH	Third	Fabric F to AMC6 Transmit+	91	RxFF-6+	AMC-6	Third	Fabric F to AMC6 Receive+
79	GND		First	Logic Ground	92	GND		First	Logic Ground
78	TxFE-6-	MCH	Third	Fabric E to AMC6 Transmit-	93	RxFE-6-	AMC-6	Third	Fabric E to AMC6 Receive-
77	TxFE-6+	MCH	Third	Fabric E to AMC6 Transmit+	94	RxFE-6+	AMC-6	Third	Fabric E to AMC6 Receive+
76	GND		First	Logic Ground	95	GND		First	Logic Ground
75	TxFD-6-	MCH	Third	Fabric D to AMC6 Transmit-	96	RxFD-6-	AMC-6	Third	Fabric D to AMC6 Receive-
74	TxFD-6+	MCH	Third	Fabric D to AMC6 Transmit+	97	RxFD-6+	AMC-6	Third	Fabric D to AMC6 Receive+
73	GND		First	Logic Ground	98	GND		First	Logic Ground
72	TxFG-5-	MCH	Third	Fabric G to AMC5 Transmit-	99	RxFG-5-	AMC-5	Third	Fabric G to AMC5 Receive-
71	TxFG-5+	MCH	Third	Fabric G to AMC5 Transmit+	100	RxFG-5+	AMC-5	Third	Fabric G to AMC5 Receive+
70	GND		First	Logic Ground	101	GND		First	Logic Ground
69	TxFF-5-	MCH	Third	Fabric F to AMC5 Transmit-	102	RxFF-5-	AMC-5	Third	Fabric F to AMC5 Receive-
68	TxFF-5+	MCH	Third	Fabric F to AMC5 Transmit+	103	RxFF-5+	AMC-5	Third	Fabric F to AMC5 Receive+
67	GND		First	Logic Ground	104	GND		First	Logic Ground
66	TxFE-5-	MCH	Third	Fabric E to AMC5 Transmit-	105	RxFE-5-	AMC-5	Third	Fabric E to AMC5 Receive-
65	TxFE-5+	MCH	Third	Fabric E to AMC5 Transmit+	106	RxFE-5+	AMC-5	Third	Fabric E to AMC5 Receive+
64	GND		First	Logic Ground	107	GND		First	Logic Ground
63	TxFD-5-	MCH	Third	Fabric D to AMC5 Transmit-	108	RxFD-5-	AMC-5	Third	Fabric D to AMC5 Receive-
62	TxFD-5+	MCH	Third	Fabric D to AMC5 Transmit+	109	RxFD-5+	AMC-5	Third	Fabric D to AMC5 Receive+
61	GND		First	Logic Ground	110	GND		First	Logic Ground

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Table 2-27: MCH Card-edge Tongue 3 (sRIO fabric) Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
60	TxFG-4-	MCH	Third	Fabric G to AMC4 Transmit-	111	RxFG-4-	AMC-4	Third	Fabric G to AMC4 Receive-
59	TxFG-4+	MCH	Third	Fabric G to AMC4 Transmit+	112	RxFG-4+	AMC-4	Third	Fabric G to AMC4 Receive+
58	GND		First	Logic Ground	113	GND		First	Logic Ground
57	TxFF-4-	MCH	Third	Fabric F to AMC4 Transmit-	114	RxFF-4-	AMC-4	Third	Fabric F to AMC4 Receive-
56	TxFF-4+	MCH	Third	Fabric F to AMC4 Transmit+	115	RxFF-4+	AMC-4	Third	Fabric F to AMC4 Receive+
55	GND		First	Logic Ground	116	GND		First	Logic Ground
54	TxFE-4-	MCH	Third	Fabric E to AMC4 Transmit-	117	RxFE-4-	AMC-4	Third	Fabric E to AMC4 Receive-
53	TxFE-4+	MCH	Third	Fabric E to AMC4 Transmit+	118	RxFE-4+	AMC-4	Third	Fabric E to AMC4 Receive+
52	GND		First	Logic Ground	119	GND		First	Logic Ground
51	TxFD-4	MCH	Third	Fabric D to AMC4 Transmit-	120	RxFD-4	AMC-4	Third	Fabric D to AMC4 Receive-
50	TxFD-4+	MCH	Third	Fabric D to AMC4 Transmit+	121	RxFD-4+	AMC-4	Third	Fabric D to AMC4 Receive+
49	GND		First	Logic Ground	122	GND		First	Logic Ground
48	TxFG-3-	MCH	Third	Fabric G to AMC3 Transmit-	123	RxFG-3-	AMC-3	Third	Fabric G to AMC3 Receive-
47	TxFG-3+	MCH	Third	Fabric G to AMC3 Transmit+	124	RxFG-3+	AMC-3	Third	Fabric G to AMC3 Receive+
46	GND		First	Logic Ground	125	GND		First	Logic Ground
45	TxFF-3-	MCH	Third	Fabric F to AMC3 Transmit-	126	RxFF-3-	AMC-3	Third	Fabric F to AMC3 Receive-
44	TxFF-3+	MCH	Third	Fabric F to AMC3 Transmit+	127	RxFF-3+	AMC-3	Third	Fabric F to AMC3 Receive+
43	GND		First	Logic Ground	128	GND		First	Logic Ground
42	TxFE-3-	MCH	Third	Fabric E to AMC3 Transmit-	129	RxFE-3-	AMC-3	Third	Fabric E to AMC3 Receive-
41	TxFE-3+	MCH	Third	Fabric E to AMC3 Transmit+	130	RxFE-3+	AMC-3	Third	Fabric E to AMC3 Receive+
40	GND		First	Logic Ground	131	GND		First	Logic Ground
39	TxFD-3-	MCH	Third	Fabric D to AMC3 Transmit-	132	RxFD-3-	AMC-3	Third	Fabric D to AMC3 Receive-
38	TxFD-3+	MCH	Third	Fabric D to AMC3 Transmit+	133	RxFD-3+	AMC-3	Third	Fabric D to AMC3 Receive+
37	GND		First	Logic Ground	134	GND		First	Logic Ground
36	TxFG-2-	MCH	Third	Fabric G to AMC2 Transmit-	135	RxFG-2-	AMC-2	Third	Fabric G to AMC2 Receive-
35	TxFG-2+	MCH	Third	Fabric G to AMC2 Transmit+	136	RxFG-2+	AMC-2	Third	Fabric G to AMC2 Receive+
34	GND		First	Logic Ground	137	GND		First	Logic Ground
33	TxFF-2-	MCH	Third	Fabric F to AMC2 Transmit-	138	RxFF-2-	AMC-2	Third	Fabric F to AMC2 Receive-
32	TxFF-2+	MCH	Third	Fabric F to AMC2 Transmit+	139	RxFF-2+	AMC-2	Third	Fabric F to AMC2 Receive+
31	GND		First	Logic Ground	140	GND		First	Logic Ground
30	TxFE-2-	MCH	Third	Fabric E to AMC2 Transmit-	141	RxFE-2-	AMC-2	Third	Fabric E to AMC2 Receive-
29	TxFE-2+	MCH	Third	Fabric E to AMC2 Transmit+	142	RxFE-2+	AMC-2	Third	Fabric E to AMC2 Receive+
28	GND		First	Logic Ground	143	GND		First	Logic Ground
27	TxFD-2-	MCH	Third	Fabric D to AMC2 Transmit-	144	RxFD-2-	AMC-2	Third	Fabric D to AMC2 Receive-
26	TxFD-2+	MCH	Third	Fabric D to AMC2 Transmit+	145	RxFD-2+	AMC-2	Third	Fabric D to AMC2 Receive+
25	GND		First	Logic Ground	146	GND		First	Logic Ground
24	TxFG-1-	MCH	Third	Fabric G to AMC1 Transmit-	147	RxFG-1-	AMC-1	Third	Fabric G to AMC1 Receive-
23	TxFG-1+	MCH	Third	Fabric G to AMC1 Transmit+	148	RxFG-1+	AMC-1	Third	Fabric G to AMC1 Receive+
22	GND		First	Logic Ground	149	GND		First	Logic Ground
21	TxFF-1-	MCH	Third	Fabric F to AMC1 Transmit-	150	RxFF-1-	AMC-1	Third	Fabric F to AMC1 Receive-
20	TxFF-1+	MCH	Third	Fabric F to AMC1 Transmit+	151	RxFF-1+	AMC-1	Third	Fabric F to AMC1 Receive+
19	GND		First	Logic Ground	152	GND		First	Logic Ground
18	TxFE-1-	MCH	Third	Fabric E to AMC1 Transmit-	153	RxFE-1-	AMC-1	Third	Fabric E to AMC1 Receive-
17	TxFE-1+	MCH	Third	Fabric E to AMC1 Transmit+	154	RxFE-1+	AMC-1	Third	Fabric E to AMC1 Receive+
16	GND		First	Logic Ground	155	GND		First	Logic Ground
15	TxFD-1-	MCH	Third	Fabric D to AMC1 Transmit-	156	RxFD-1-	AMC-1	Third	Fabric D to AMC1 Receive-

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Table 2-27: MCH Card-edge Tongue 3 (sRIO fabric) Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
14	TxFD-1+	MCH	Third	Fabric D to AMC1 Transmit+	157	RxFD-1+	AMC-1	Third	Fabric D to AMC1 Receive+
13	GND		First	Logic Ground	158	GND		First	Logic Ground
12	TxFUE-	MCH	Third	Update Channel E, Transmit-	159	RxFUE-	Other MCH	Third	Update Channel E, Receive-
11	TxFUE+	MCH	Third	Update Channel E, Transmit+	160	RxFUE+	Other MCH	Third	Update Channel E, Receive+
10	GND		First		161	GND		First	
9	TxFUD-	MCH	Third	Update Channel D, Transmit-	162	RxFUD-	Other MCH	Third	Update Channel D, Receive-
8	TxFUD+	MCH	Third	Update Channel D, Transmit+	163	RxFUD+	Other MCH	Third	Update Channel D, Receive+
7	GND		First		164	GND		First	
6	RSVD		Third		165	RSVD		Third	
5	RSVD		Third		166	RSVD		Third	
4	GND		Third		167	GND		Third	
3	RSVD		Third		168	RSVD		Third	
2	RSVD		Third		169	RSVD		Third	
1	GND		First		170	GND		First	

Table 2-28: MCH Card-edge Tongue 4 Connectors Pinout

Pin No.	Signal	Driven By	Mating	Pin Function on MCH	Pin No.	Signal	Driven By	Mating	Pin Function on MCH
85	GND		First	Logic-Ground	86	GND		First	Logic-Ground
84	TxFG-12-	MCH	Third	Fabric G to AMC12 Transmit-	87	RxFG-12-	AMC-12	Third	Fabric G to AMC12 Receive-
83	TxFG-12+	MCH	Third	Fabric G to AMC12 Transmit+	88	RxFG-12+	AMC-12	Third	Fabric G to AMC12 Receive+
82	GND		First	Logic-Ground	89	GND		First	Logic-Ground
81	TxFF-12-	MCH	Third	Fabric F to AMC12 Transmit-	90	RxFF-12-	AMC-12	Third	Fabric F to AMC12 Receive-
80	TxFF-12+	MCH	Third	Fabric F to AMC12 Transmit+	91	RxFF-12+	AMC-12	Third	Fabric F to AMC12 Receive+
79	GND		First	Logic-Ground	92	GND		First	Logic-Ground
78	TxFE-12-	MCH	Third	Fabric E to AMC12 Transmit-	93	RxFE-12-	AMC-12	Third	Fabric E to AMC12 Receive-
77	TxFE-12+	MCH	Third	Fabric E to AMC12 Transmit+	94	RxFE-12+	AMC-12	Third	Fabric E to AMC12 Receive+
76	GND		First	Logic-Ground	95	GND		First	Logic-Ground
75	TxFD-12-	MCH	Third	Fabric D to AMC12 Transmit-	96	RxFD-12-	AMC-12	Third	Fabric D to AMC12 Receive-
74	TxFD-12+	MCH	Third	Fabric D to AMC12 Transmit+	97	RxFD-12+	AMC-12	Third	Fabric D to AMC12 Receive+
73	GND		First	Logic-Ground	98	GND		First	Logic-Ground
72	TxFG-11-	MCH	Third	Fabric G to AMC11 Transmit-	99	RxFG-11-	AMC-11	Third	Fabric G to AMC11 Receive-
71	TxFG-11+	MCH	Third	Fabric G to AMC11 Transmit+	100	RxFG-11+	AMC-11	Third	Fabric G to AMC11 Receive+
70	GND		First	Logic-Ground	101	GND		First	Logic-Ground
69	TxFF-11-	MCH	Third	Fabric F to AMC11 Transmit-	102	RxFF-11-	AMC-11	Third	Fabric F to AMC11 Receive-
68	TxFF-11+	MCH	Third	Fabric F to AMC11 Transmit+	103	RxFF-11+	AMC-11	Third	Fabric F to AMC11 Receive+
67	GND		First	Logic-Ground	104	GND		First	Logic-Ground
66	TxFE-11-	MCH	Third	Fabric E to AMC11 Transmit-	105	RxFE-11-	AMC-11	Third	Fabric E to AMC11 Receive-
65	TxFE-11+	MCH	Third	Fabric E to AMC11 Transmit+	106	RxFE-11+	AMC-11	Third	Fabric E to AMC11 Receive+
64	GND		First	Logic-Ground	107	GND		First	Logic-Ground
63	TxFD-11-	MCH	Third	Fabric D to AMC11 Transmit-	108	RxFD-11-	AMC-11	Third	Fabric D to AMC11 Receive-
62	TxFD-11+	MCH	Third	Fabric D to AMC11 Transmit+	109	RxFD-11+	AMC-11	Third	Fabric D to AMC11 Receive+

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Table 2-28: MCH Card-edge Tongue 4 Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mat-ing	Pin Function on MCH	Pin No.	Signal	Driven By	Mat-ing	Pin Function on MCH
61	GND		First	Logic-Ground	110	GND		First	Logic-Ground
60	TxFG-10-	MCH	Third	Fabric G to AMC10 Transmit-	111	RxFG-10-	AMC-10	Third	Fabric G to AMC10 Receive-
59	TxFG-10+	MCH	Third	Fabric G to AMC10 Transmit+	112	RxFG-10+	AMC-10	Third	Fabric G to AMC10 Receive+
58	GND		First	Logic-Ground	113	GND		First	Logic-Ground
57	TxFF-10-	MCH	Third	Fabric F to AMC10 Transmit-	114	RxFF-10-	AMC-10	Third	Fabric F to AMC10 Receive-
56	TxFF-10+	MCH	Third	Fabric F to AMC10 Transmit+	115	RxFF-10+	AMC-10	Third	Fabric F to AMC10 Receive+
55	GND		First	Logic-Ground	116	GND		First	Logic-Ground
54	TxFE-10-	MCH	Third	Fabric E to AMC10 Transmit-	117	RxFE-10-	AMC-10	Third	Fabric E to AMC10 Receive-
53	TxFE-10+	MCH	Third	Fabric E to AMC10 Transmit+	118	RxFE-10+	AMC-10	Third	Fabric E to AMC10 Receive+
52	GND		First	Logic-Ground	119	GND		First	Logic-Ground
51	TxFD-10	MCH	Third	Fabric D to AMC10 Transmit-	120	RxFD-10	AMC-10	Third	Fabric D to AMC10 Receive-
50	TxFD-10+	MCH	Third	Fabric D to AMC10 Transmit+	121	RxFD-10+	AMC-10	Third	Fabric D to AMC10 Receive+
49	GND		First	Logic-Ground	122	GND		First	Logic-Ground
48	TxFG-9-	MCH	Third	Fabric G to AMC9 Transmit-	123	RxFG-9-	AMC-9	Third	Fabric G to AMC9 Receive-
47	TxFG-9+	MCH	Third	Fabric G to AMC9 Transmit+	124	RxFG-9+	AMC-9	Third	Fabric G to AMC9 Receive+
46	GND		First	Logic-Ground	125	GND		First	Logic-Ground
45	TxFF-9-	MCH	Third	Fabric F to AMC9 Transmit-	126	RxFF-9-	AMC-9	Third	Fabric F to AMC9 Receive-
44	TxFF-9+	MCH	Third	Fabric F to AMC9 Transmit+	127	RxFF-9+	AMC-9	Third	Fabric F to AMC9 Receive+
43	GND		First	Logic-Ground	128	GND		First	Logic-Ground
42	TxFE-9-	MCH	Third	Fabric E to AMC9 Transmit-	129	RxFE-9-	AMC-9	Third	Fabric E to AMC9 Receive-
41	TxFE-9+	MCH	Third	Fabric E to AMC9 Transmit+	130	RxFE-9+	AMC-9	Third	Fabric E to AMC9 Receive+
40	GND		First	Logic-Ground	131	GND		First	Logic-Ground
39	TxFD-9-	MCH	Third	Fabric D to AMC9 Transmit-	132	RxFD-9-	AMC-9	Third	Fabric D to AMC9 Receive-
38	TxFD-9+	MCH	Third	Fabric D to AMC9 Transmit+	133	RxFD-9+	AMC-9	Third	Fabric D to AMC9 Receive+
37	GND		First	Logic-Ground	134	GND		First	Logic-Ground
36	TxFG-8-	MCH	Third	Fabric G to AMC8 Transmit-	135	RxFG-8-	AMC-8	Third	Fabric G to AMC8 Receive-
35	TxFG-8+	MCH	Third	Fabric G to AMC8 Transmit+	136	RxFG-8+	AMC-8	Third	Fabric G to AMC8 Receive+
34	GND		First	Logic-Ground	137	GND		First	Logic-Ground
33	TxFF-8-	MCH	Third	Fabric F to AMC8 Transmit-	138	RxFF-8-	AMC-8	Third	Fabric F to AMC8 Receive-
32	TxFF-8+	MCH	Third	Fabric F to AMC8 Transmit+	139	RxFF-8+	AMC-8	Third	Fabric F to AMC8 Receive+
31	GND		First	Logic-Ground	140	GND		First	Logic-Ground
30	TxFE-8-	MCH	Third	Fabric E to AMC8 Transmit-	141	RxFE-8-	AMC-8	Third	Fabric E to AMC8 Receive-
29	TxFE-8+	MCH	Third	Fabric E to AMC8 Transmit+	142	RxFE-8+	AMC-8	Third	Fabric E to AMC8 Receive+
28	GND		First	Logic-Ground	143	GND		First	Logic-Ground
27	TxFD-8-	MCH	Third	Fabric D to AMC8 Transmit-	144	RxFD-8-	AMC-8	Third	Fabric D to AMC8 Receive-
26	TxFD-8+	MCH	Third	Fabric D to AMC8 Transmit+	145	RxFD-8+	AMC-8	Third	Fabric D to AMC8 Receive+
25	GND		First	Logic-Ground	146	GND		First	Logic-Ground
24	TxFG-7-	MCH	Third	Fabric G to AMC7 Transmit-	147	RxFG-7-	AMC-7	Third	Fabric G to AMC7 Receive-
23	TxFG-7+	MCH	Third	Fabric G to AMC7 Transmit+	148	RxFG-7+	AMC-7	Third	Fabric G to AMC7 Receive+
22	GND		First	Logic-Ground	149	GND		First	Logic-Ground
21	TxFF-7-	MCH	Third	Fabric F to AMC7 Transmit-	150	RxFF-7-	AMC-7	Third	Fabric F to AMC7 Receive-
20	TxFF-7+	MCH	Third	Fabric F to AMC7 Transmit+	151	RxFF-7+	AMC-7	Third	Fabric F to AMC7 Receive+
19	GND		First	Logic-Ground	152	GND		First	Logic-Ground
18	TxFE-7-	MCH	Third	Fabric E to AMC7 Transmit-	153	RxFE-7-	AMC-7	Third	Fabric E to AMC7 Receive-
17	TxFE-7+	MCH	Third	Fabric E to AMC7 Transmit+	154	RxFE-7+	AMC-7	Third	Fabric E to AMC7 Receive+
16	GND		First	Logic-Ground	155	GND		First	Logic-Ground

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Table 2-28: MCH Card-edge Tongue 4 Connectors Pinout (Continued)

Pin No.	Signal	Driven By	Mat-ing	Pin Function on MCH	Pin No.	Signal	Driven By	Mat-ing	Pin Function on MCH
15	TxFD-7-	MCH	Third	Fabric D to AMC7 Transmit-	156	RxFD-7-	AMC-7	Third	Fabric D to AMC7 Receive-
14	TxFD-7+	MCH	Third	Fabric D to AMC7 Transmit+	157	RxFD-7+	AMC-7	Third	Fabric D to AMC7 Receive+
13	GND		First	Logic-Ground	158	GND		First	Logic-Ground
12	TxFUG-	MCH	Third	Update Channel G, Transmit-	159	RxFUG-	Other MCH	Third	Update Channel G, Receive-
11	TxFUG+	MCH	Third	Update Channel G, Transmit+	160	RxFUG+	Other MCH	Third	Update Channel G, Receive+
10	GND		First		161	GND		First	
9	TxFUF-	MCH	Third	Update Channel F, Transmit-	162	RxFUF-	Other MCH	Third	Update Channel F, Receive-
8	TxFUF+	MCH	Third	Update Channel F, Transmit+	163	RxFUF+	Other MCH	Third	Update Channel F, Receive+
7	GND		First		164	GND		First	
6	RSVD		Third		165	RSVD		Third	
5	RSVD		Third		166	RSVD		Third	
4	GND		Third		167	GND		Third	
3	RSVD		Third		168	RSVD		Third	
2	RSVD		Third		169	RSVD		Third	
1	GND		First		170	GND		First	

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Chapter 3

Operating the Unit

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3 Operating the Unit

This chapter describes how to operate the unit by accessing the board with the available tools. The boot-loader is part of the Software on the AM4904 and is also described.

The Software accomplishes operation of the switching hardware as well as the MCMC SW and is therefore also referenced as Firmware. It is pre-installed on the system and can only be updated by a dedicated update procedure. This chapter describes all parts of the Firmware and introduces the update procedure.

3.1 Board Access

The board provides access through the following externally accessible management interfaces.

Table 3-1: Management Interfaces

Interface	Type	Description
Front Serial	RS232 type interface	Serial interface connected to CPU UART0
Front connector Ethernet	10/100/1000BASE-T Ethernet	Ethernet interface to CPU interface eth0
Internal Network port	Ethernet over PCI Express	Switch Management network port. Used for in-band management and protocol traffic.
Internal Network port	1000BASE-X Ethernet	Internal Ethernet interface between switch silicon and CPU interface eth1. Normally not active. Can be used for special applications
Backplane connector IPMB-L	IPMB-L	The IPMB-L is the standard AMC interface for carrier to MMC communication.
Backplane connector IPMB-0	IPMB-0	Main redundant IPMB connection to MicroTCA EMMC, for example power modules.

The serial Interface is the low level debug interface. If connected to the front serial connector, the user will have access to the linux shell. The shell provides tools and applications used for example to manage the system, the CM and the FASTPATH switching software.

Serial connection port settings are:

- 115,200 bps (serial speed might be different for customized board variants)
- 8 bit, no parity, 1 stop bit (8N1)
- no flow control

Log in as root and enter root password (“root”).

```
(none) login: root
Password:

Wind River Linux glibc_small (standard) 2.0



BusyBox v1.4.1 (2009-06-25 18:25:09 CEST) Built-in shell (ash)
Enter 'help' for a list of built-in commands.

#
```


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For additional information about the available tools and application, see “System Configuration Tools” on page 59.

If connected to the Ethernet I/F, either front or Network port, the user will be automatically switched to the FASTPATH CLI. For additional information on how to use the FASTPATH CLI, see *“AM4904/AM4910 CLI Reference Manual”*.

3.2 MCMC/CM application

The MicroTCA MCMC/CM (short CM) application implements a standard compliant MicroTCA Management Controller and Carrier Manager. It supports a standard MicroTCA carrier, including power modules, cooling units and up to 12 AdvancedMC modules.

On startup, the Carrier Manager will read and verify its configuration files. After that, the Carrier Manager will initiate the startup sequence to determine its current role. It then either acts as only MCMC or as a combined MCMC/CM. In a redundant configuration, if the role is determined as Master, the Carrier Manager will act as a combined MCMC/CM, the slave will act as a MCMC only.

The user always connects to the Carrier Manager and not to the MCMC function.

The Carrier manager provides a CLI for management purposes. For information on how to use the CLI, see “CM Command Line Interface (CLI)” on page 51.

The precedence of config settings is as follows:

Table 3-2: Configuration File Precedence

Precedence	File/Source	Description
1	/opt/kontron/lib/cm.cfg	Base configuration config file, defaults from build
2	-f /opt/kontron/lib/variant-X.cfg	Configuration file read by option –f, based on X VPD variant by default /etc/init.d/cm startup script
3	/etc/cm.cfg	Default user changeable configuration, changes are persistent in /etc unionfs
4	-s SETTING=VALUE	User settings passed on command line
5	sdr_config_file_1 option (/opt/kontron/lib/sdr-variant-X.cfg)	Configuration file set by configuration option, based on X VPD variant by default /etc/init.d/cm startup script
6	/opt/kontron/lib/autoconfig-cm.cfg	Autoconfiguration database loaded by standard cm startup script
7	sdr_config_file_2 option	Configuration file set by configuration option
8	sdr_config_file_3 option	Configuration file set by configuration option

3.2.1 CM Configuration Options

There are a lot of user changeable configuration options, that can be used to setup the system according the user needs. The settings can be enabled/disabled/set in the file /etc/cfg. Appendix A “Configuration Options” shows a list of useable settings. Custom board settings have to be used very carefully. In case of questions, please ask the Kontron support for help.

For additional information about setting up PCIe, see “Configuring PCI Express” on page 62. For additional information about setting up sRIO, see “Configuring sRIO” on page 64.

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3.2.2 CM Modules

The CM provides counters and logs for the different parts of the software (modules), which can be used for debugging purposes.

The following list gives an overview about module names used for counter and log commands. For information about the commands, see “CM Command Line Interface (CLI)” on page 51.

Table 3-3: Available Modules

Module Name used in CM CLI	Description
CCLI	Core CLI
FCLI	Frontend CLI
I2C	Internal I2C
IIPMB	IPMB busses, including IPMB-0 and all IPMB-L
IRCMP	RMCP/RMCP+ I/F
IFRU	FRU data.
ICMDIN	IPMI Core Command In Functions.
ICMDOUT	IPMI Core Command Out Functions.
IFIA	FRU Information Agent.
ISEL	IPMI SEL
ISENS	IPMI Sensors
IPM	MTCA Power Module
ICM	MTCA Carrier Manager.
IEKEY	E-Keying
PERST	Persistent data
IIFACE	IPMI Interfaces
SENS	Sensor Handling
SRIO	sRio
PCIE	PCIe
FPGA	FPGA

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3.3 CM Command Line Interface (CLI)

Using a serial connection to the MCH, the command line interface is accessed from the Linux shell. It is implemented in FCLI and CCLI modules. The frontend is implemented as a standalone Linux application, clicm.

The CLI output is usually in ASCII format, but it can optionally also be set to output in a format that is easier to process automatically, e.g. CSV.

The FCLI module implements a socket server, accepting parallel connection requests. Each connection is associated with a local session ID, that is passed to the CCLI module as a PARM_TID with each request.

The unix domain socket protocol is very simple: the clitool sends a '\n' terminated command, and retrieves one or more '\n' terminated response lines. When the command is finished, it receives a single byte '\001' (hex 0x1), to indicate the end of the command response.

All command responses must only contain printable ASCII characters, and the '\001' end marker, and '\n' line delimiters. No other non-printable characters are allowed.

3.3.1 Accessing MCMC: clicm

The command "clicm" opens the CM CLI shell. Exit the CM shell by using the command "quit".

```
# clicm
CM>
CM> quit
#
```

3.3.2 CM Commands

The CM commands provide access to the carrier manager.

Table 3-4: CLI CM Commands

Command	Description
cm activate <FRU-ID>	Activate specified FRU device
cm control cold reset <FRU-ID>	Invoke cold reset command on FRU device
cm control warm reset <FRU-ID>	Invoke warm reset command on FRU device
cm control diag <FRU-ID>	Invoke diagnostic interrupt command on FRU device
cm control graceful <FRU-ID>	Invoke graceful reboot command on FRU device
cm deactivate <FRU-ID>	Deactivate specified FRU device
cm show all	Show all present FRU devices
cm show <FRU-ID>	Show FRU devices information
cm restart	Restart MCMC/CM
cm terminate	Terminate MCMC/CM

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3.3.3 Counter Commands

The counter commands provide access to various counters and statistics provided by the modules.

Counters are grouped by internal modules they belong to. In addition, counters are flagged as either error counters, indicating unusual events, and non-error counters, indicating normal operational statistics.

Table 3-5: CLI Counter Commands

Command	Description
counter clear <MODULE>	Clear counter statistics for a specified MODULE
counter clear all	Clear all counter statistics for all modules
counter show	Show non zero counter statistics for all modules
counter show all	Show all counter statistics for all modules
counter show error	Show non zero error counter statistics for all modules
counter show error all	Show all error counter statistics for all modules
counter show error module <MODULE>	Show all error counter statistics for a specified MODULE
counter show module <MODULE>	Show all counter statistics for a specified MODULE

3.3.4 Ekeying Commands

The ekeying commands provide information about e-keying status of all units installed.

Table 3-6: CLI Ekeying Commands

Command	Description
ekeying clock status show <FRUID>	Show enabled backplane clocks of the specified FRUID
ekeying map show <FRUID>	Show the p2p connectivity from the specified FRUID
ekeying status show <FRUID>	Show enabled ekeying ports for FRUID
ekeying records show <FRUID>	Show the p2p records from the specified FRUID

3.3.5 Fan Commands

The fan commands provide access to the local fan control application.

Table 3-7: CLI Fan Commands

Command	Description
fan get <FRU>	Get FAN level of FRU device
fan properties <FRU>	Show FAN properties of FRU device
fan set <FRU><LEVEL><LOCAL-CONTROL-STATE>	Set FAN level of FRU device

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3.3.6 Fru Commands

The fru commands provide access to local and remote FRU data.

Table 3-8: CLI Fru Commands

Command	Description
fru info <FRU-ID>	Show FRU information of the specified FRU-ID
fru mcmc read <FRU-ID> <FILE>	Read FRU data from MCMC's FRU-ID to the specified file
fru mcmc show <FRU-ID>	Show FRU data of MCMC of the specified FRU-ID
fru mcmc show detail <FRU-ID>	Show FRU detail information of the specified FRU-ID
fru mcmc write <FRU-ID> <FILE>	Write FRU data to MCMC's FRU-ID from specified file
fru raw <FRU-ID> [OFFSET] [COUNT]	Dump raw FRU data from FRU device
fru read <FRU-ID> <FILE>	Read FRU data from FRU-ID to the specified file
fru show <FRU-ID>	Show boardinfo and productinfo of the specified FRU-ID
fru show boardinfo all	Show boardinfo area of all FRU-IDs in the system
fru show detail <FRU-ID>	Show all areas in verbose mode of the specified FRU-ID
fru show productinfo all	Show productinfo area of all FRU-IDs in the system
fru write <FRU-ID> <FILE>	Write FRU data from specified file to FRU-ID

3.3.7 IPMB Commands

The ipmb commands provide access to low level IPMB I2C statistics.

Table 3-9: CLI IPMB Commands

Command	Description
ipmb clear stats all	Clear all IPMB counter for all controller
ipmb raw <ADDR> <LUN> <NETFN> <CMD> [DATA...]	Send IPMI command to specified IPMB address
ipmb raw si <LUN> <NETFN> <CMD> [DATA...]	Send IPMI command to local MCMC
ipmb show stats	Show IPMB non-zero counter for all controller
ipmb show stats all	Show all IPMB counter for all controller
ipmb show stats global	Show global IPMB counter
ipmb show stats id <ID>	Show IPMB counter for a controller with ID

3.3.8 Boot option Commands

Table 3-10: CLI boot option Commands

Command	Description
kontron boot get <FRU-ID> <DEVICE-ID>	Get Kontron boot option of device
kontron boot set <FRU-ID> <DEVICE-ID>	Set Kontron boot option of device

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3.3.9 I2C Commands

Table 3-11: CLI I2C Commands

Command	Description
i2c read <CONTROLLER> <I2CSLAVE> <BYTES>	Read from I2C slave
i2c write <CONTROLLER> <I2CSLAVE> {<BYTES>...}	Write to I2C slave
i2c wrrd <CONTROLLER> <I2CSLAVE> <BYTES-TO-READ} {<BYTES>...}	Write/Read to I2C slave

3.3.10 LAN Commands

Table 3-12: CLI LAN Commands

Command	Description
lan clear stats <FRU-ID> <CHANNEL>	Clear LAN statistics
lan show <FRU-ID> <CHANNEL>	Show LAN settings of FRU device
lan show raw <FRU-ID> <CHANNEL>	Show LAN settings of FRU device in RAW format
lan show stats <FRU-ID> <CHANNEL>	Show LAN statistics

3.3.11 Log Commands

Each internal module can be instrumented to provide debug log output. This output includes warnings, major and critical errors. In addition, for debugging/support purposes, special trace enabled CM versions can provide detailed output for debugging purposes.

The log commands provide configuration access to the level of output generated.

Table 3-13: CLI Log Commands

Command	Description
log level <MODULE> {debug | trace | minor | major | critical | none}	Toggle internal tracing output verbosity for specified MODULE
log level all {debug | trace | minor | major | critical | none}	Toggle internal tracing output verbosity for all modules
log target {none | console | syslog}	Set target for internal tracing
log show	Show internal tracing output verbosity

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3.3.12 MC Commands

The mc commands provide access to the management controllers of all intelligent/manages units installed.

Table 3-14: CLI MC Commands

Command	Description
mc show <FRU-ID>	Show management controller information of FRU device
mc reset warm <FRU-ID>	Invoke warm reset of management controller of FRU device
mc reset cold <FRU-ID>	Invoke cold reset of management controller of FRU device
mc led {presence | link-status}	Configure MCH front panel LEDs
mc carrier number	Shows currently used Carrier Number

3.3.13 Memory Commands

The memory commands provide access to memory usage information.

Table 3-15: CLI Memory Commands

Command	Description
memory stats show	Show current memory allocation statistics

3.3.14 Monitor Commands

The monitor commands provide access to monitoring functionality for IPMI messages, either on IPMB-L, IPMB-0 or RMCP.

Table 3-16: CLI Monitor Commands

Command	Description
monitor file <FILE>	Set name of file FILE where IPMB traffic is written to
monitor file size <SIZE>	Limit IPMB log file to size SIZE
monitor file keep <NUM>	When IPMB file size is reached, rotate files and keep NUM files
monitor file enable	Enable logging of IPMB traffic to file
monitor file disable	Disable logging of IPMB traffic to file
monitor console enable	Enable logging of IPMB traffic to serial console
monitor console disable	Disable logging of IPMB traffic to serial console
monitor show	Show setting of IPMB traffic logging
monitor i2c trace console enable	Enable tracing of I2C events (to console only)
monitor i2c trace console disable	Disable tracing of I2C events (to console only)
monitor ip <IP>	Set IP address of target host where IPMB traffic is written to
monitor ip enable	Enable logging of IPMB traffic to IP address
monitor ip disable	Disable logging of IPMB traffic to IP address

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3.3.15 MP Commands

The mp commands provide access to the internal message bus statistics. The internal message bus traffic can be used very efficiently to analyze issues. It can be logged to a binary file format for later analysis.

Table 3-17: CLI MP Commands

Command	Description
mp log file <FILE>	Set name of file FILE internal messages are written to
mp log file size <SIZE>	Limit log file to specified size
mp log file keep <NUM>	When file size is reached, rotate files and keep this number of files
mp log file enable	Enable logging of all internal messages
mp log file disable	Disable logging of all internal messages
mp log show	Show setting of internal message logging
mp stats show	Show internal message passing
mp log console enable	Enable logging to serial console
mp log console disable	Disable logging to serial console

3.3.16 PCIe Commands

The pcie commands provide access to the PCI Express infrastructure. The commands allow to show status and configuration settings and allows to read/write PCI Express register settings. For PCIe default settings, see “Configuring PCI Express” on page 62.

Table 3-18: CLI PCIe Commands

Command	Description
pcie clock disable all	Disable all PCIE backplane clocks
pcie reg read <STATION> <PORT> <ADDR>	Read PCIE switch register value.
pcie reg write <STATION> <PORT> <ADDR> <VALUE>	Write PCIE switch register value.
pcie show config	Show PCIE switch fabric power up configuration settings.
pcie show status	Show PCIE switch fabric port link status.

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3.3.17 PM Commands

The pm commands provide information about current power channel status and power budget allocation, as well as global power module status information.

Table 3-19: CLI PM Commands

Command	Description
pm channel show <CHANNEL>	Show power channel status
pm module show <ID>	Show power module global status
pm channel status request <SITE-ID>	Requests channel status from power module

3.3.18 Redundancy Commands

Table 3-20: CLI RM Commands

Command	Description
rm status	Show redundancy status
rm xover reset	Force other MCHto reset

3.3.19 SEL Commands

The SEL commands provide access to the system event log.

Table 3-21: CLI SEL Commands

Command	Description
sel info show	Show SEL global information
sel show all [STARTID]	Show SEL entries, optionally starting with specified SEL entry
sel show < ID>	Show full SEL entry
sel clear	Clear the SEL
sel raw <ID>	Show specified SEL entry in raw format
sel raw all	Show all SEL entries in raw format

3.3.20 Sensor Commands

The sensor commands provide access to the sensor data records and sensor reading.

Table 3-22: CLI Sensor Commands

Command	Description
sensor decode <ID>	Show specified sensor/SDR information in raw decoded format
sensor info show	Show sensor SDR count per FRU-ID
sensor raw <ID>	Show specified sensor SDR information in raw format
sensor show <ID>	Show specified sensor SDR information
sensor show all	Show all available sensors SDR

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Table 3-22: CLI Sensor Commands (Continued)

Command	Description
sensor show asserted	Show all asserted sensors SDR
sensor show fru <FRU-ID>	Show all sensors SDR located on specified FRU-ID
sensor show type {temperature | voltage | current | fan | hotswap | analog | discrete}	Show all sensors SDR of specified type
sensor theshold set <ID> {lnr | lcr | lnc | unc | ucr | unr} <VALUE>	Set threshold for specified SDR ID

3.3.21 SRIO Commands

The serial RapidIO commands provide access to the serial RapidIO switch fabric chips and related CM configuration options. They are not available on other variants.

Note that initial configuration of sRIO strappings is configured using the standard CM configuration file. For information about sRIO default settings, see “Configuring sRIO” on page 64.

Table 3-23: CLI sRIO Commands

Command	Description
srio reg read <UNIT> <ADDR>	Read register from sRIO switch through I2C
srio reg write <UNIT> <ADDR> <VALUE>	Write register to sRIO switch through I2C
srio show status	Show sRIO switch fabric port link status.

3.3.22 Clock Commands

The clocking commands provide access to the PLL and the clock driver

Table 3-24: CLI Clock Commands

Command	Description
clock disable <clk1 | clk2> <line0-11>	Disable all clock driver and receiver for specified device
clock connect output <PLL-LINE> <clk | clk2> <line0-11>	Connnect a PLL signal via PLD mux to clock line on the edge connector
clock connect input <PLL-LINE> {<clk2> <line0..11> | <clk1 | clk3> update | <front> | <none>}	Connnect a clock line via PLD mux to a PLL reference input
clock pll config set <PARAMETER> <VALUE>	Set PLL Configuration
clock pll config show	Show PLL configuration
clock pll mode {normal | holdover | freerun | auto} [<DEVICE> | front | none]	Set PLL running mode
clock reference expect <PLL-LINE> <frequency>	Set expected reference frequency for clock e-keying
clock reference show	Show PLL reference information
clock status show	Show Clock status information
clock synth show	Show synthesizer settings

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3.3.23 Miscellaneous Commands

Table 3-25: CLI Miscellaneous Commands

Command	Description
cooling show	Show cooling information
alarm show {info | capability [<FRU-ID]}	Show information about alarm module or capabilities
help [command]	Show help for command prefix or all commands
sleep <SECONDS>	Let the CM sleep for the desired time
config show [<config option>]	Show configuration settings
support info	Show board information for technical support
quit	Quit the CLI session

3.4 System Configuration Tools

A number of tools and applications is supplied to support configuring, using, diagnosing and installing the board. All tools are accessible from the Linux shell.

3.4.1 Accessing the PLD: pldtool

Tool for reading and writing to the PLD glue logic.

```
# pldtool
usage: pldtool <options> <command>

Options:
    -?          display help and exit

Commands:
    list            list all PLD regs
    read            <reg 1> ... <reg N> read one or more PLD register
    write           <reg> <value> write a value to one PLD reg
    mask            <reg> <mask> <compare_value> compares the register with the mask
    dump            <reg> <count> hex dump of multiple memory
    spidump         dump SPI eeprom content
    spiinit         write file to user SPI eeprom
    spiverify       verify file to factory (0) or user (1) SPI eeprom
#
```

3.4.2 Accessing Switch Management: fpcli

This command opens the FASTPATH CLI shell.

Log in as admin and enter privileged mode by typing '**enable**' (no passwords required by default).Exit it by entering either Control+V or Control+X.

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For additional information about FASTPATH CLI , refer to “AM4904/AM4910 Switch Management CLI Reference Manual”

```
# fpcli
Connected to FASTPATH console. Press Control+V or Control+X to disconnect.

(Ethernet Fabric) #
*** IDLE TIMEOUT ***

(Ethernet Fabric)
User:admin
Password:
(Ethernet Fabric) >enable
Password:

(Ethernet Fabric) #

Disconnected from FASTPATH console.
#
```

3.4.3 Accessing MCMC: ipmitool

The board firmware includes the ipmitool, based on version 1.8.8. It allows accessing the MCMC through RMCP interface. For information about ipmittol features, refer to:

http://ipmitool.sourceforge.net/

There is a specially customized version “ipmitoolcm” available on the board, which is prepared to directly communicate with the Carrier Manager without knowing parameters like user/password. See example below

```
# ipmitool -I lan -H localhost -U admin -P admin -A PASSWORD mc info
Device ID                 : 14
Device Revision           : 0
Firmware Revision         : 2.1
IPMI Version              : 2.0
Manufacturer ID           : 15000
Manufacturer Name         : Kontron
Product ID                : 1100 (0x044c)
Device Available          : yes
Provides Device SDRs      : yes
Additional Device Support :
Aux Firmware Rev Info     :
    0x00
    0x00
    0x00
    0x00
```

“ipmitoolcm" is ipmitool with all neccessary parameters preset to access the carrier mananger!

```
# ipmitoolcm mc info
Device ID                 : 14
Device Revision           : 0
Firmware Revision         : 2.1
IPMI Version              : 2.0
Manufacturer ID           : 15000
Manufacturer Name         : Kontron
Product ID                : 1100 (0x044c)
Device Available          : yes
```


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```
Provides Device SDRs      : yes
Additional Device Support :
    Sensor Device
    SEL Device
    FRU Inventory Device
    IPMB Event Receiver
    IPMB Event Generator
Aux Firmware Rev Info     :
    0x00
    0x00
    0x00
    0x00
```

3.4.4 Configuring services: chkconfig

Tool for configuring services that are started during Linux startup. This tool allows listing available services and allows switching a service on and off.

Currently only a single run level S is supported. Service scripts are stored in /etc/init.d. Services that are activated have a corresponding link in /etc/rcS.d/SNNservice where NN is a number and service is the service name. The higher the number, the later a service is started.

By default services are inserted with NN=99. For a service, this can be changed by including a standard "# chkconfig LLL XX YY" line. The XX from this line will then be taken as the start NN number.

This is similar to the standard Fedora chkconfig tool.

```
Usage:
chkconfig --list      -- list current service status
chkconfig SERVICE on  -- switch on service on next reboot
chkconfig SERVICE off -- switch off service on next reboot
```

The --list option shows the current setting of the available services startup behaviour.

```
# chkconfig --list
cm                  : S:on
data                : S:on
fastpath            : S:on
network             : S:off
ntpd                : S:off
portmap             : S:off
shutdown-script     : S:off
sshd                : S:off
syslogd             : S:on
telnetd             : S:on
tftpd               : S:off
usermode-agent      : S:off
#
```


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3.4.5 Configuring PCI Express

This section is only valid for the PCI Express variant.

The PCI Express infrastructure can be configured using the file "/opt/kontron/lib/variant-3.cfg"

The following listing shows the default "variant-3.cfg" file:

```
pcie_activate=1
pcie_reset_delay_ms=200
pcie_i2c_config_enable=1
pcie_init_early.0=pcie clock disable all
# set all port speeds to 2.5GT/s
pcie_init_late.0=pcie reg write 0 0 0x00000098 0x00000001
pcie_init_late.1=pcie reg write 0 1 0x00000098 0x00000001
pcie_init_late.2=pcie reg write 0 2 0x00000098 0x00000001
pcie_init_late.3=pcie reg write 0 3 0x00000098 0x00000001
pcie_init_late.4=pcie reg write 5 0 0x00000098 0x00000001
pcie_init_late.5=pcie reg write 5 1 0x00000098 0x00000001
pcie_init_late.6=pcie reg write 5 2 0x00000098 0x00000001
pcie_init_late.7=pcie reg write 5 3 0x00000098 0x00000001
pcie_init_late.8=pcie reg write 4 0 0x00000098 0x00000001
pcie_init_late.9=pcie reg write 4 1 0x00000098 0x00000001
pcie_init_late.10=pcie reg write 4 2 0x00000098 0x00000001
pcie_init_late.11=pcie reg write 4 3 0x00000098 0x00000001

# Configuration Release
pcie_init_late.12=pcie reg write 0 0 0x000003ac 0x00000001

# reset PCIE express fabric if settings change
pcie_always_reset=2

# set root complex to AMC site 1
pcie_rc_site=1
# set PCIE clock to Non-SSC mode
pcie_ssc=0

# and always activate pcie_rc_site AMC laste
# this ensures PCIe end points get active before
# root complex
cm_pcie_activate_rc_last=1
```

The CM reads the config file on startup. It will first load factory default configurations from /opt/kontron/lib/variant-3.cfg. Then it will load configuration settings from /etc/cm.cfg (not present by default).

Settings in files loaded later take precedence over settings in files that are loaded earlier.

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The following table shows possible settings

Table 3-26: PCI Express Settings

Variable	Default	Settings/Description
pcie_activate	0	0 = Do not take PCIE tongue out of reset if present 1 = Do assume PCIE tongue is installed, take PCIE tongue out of reset and execute init sequence
pcie_always_reset	0	1 = Always reset PCIE switch when MCMC/CM starts 0 = Skip PCIE initialization if PCIE is not in reset 2 = Reset PCIe switch if root complex setting pcie_rc_site or SSC setting changed
pcie_rc_site	1	set PCIE root-complex to AMC site (1..12)
pcie_reset_delay_ms	200	Delay in ms after PCIE tongue is taken out of reset.
pcie_ssc	0	1 = Enable PCI Express clock SSC (spread spectrum) mode. This is a global setting. All PCI Express Clock outputs are SSC then. 0 = Enable PCI Express clock Non-SSC (normal) mode
cm_enable_pcie_clock_when_pcie_present	0	1 = enable PCI Express to slot when AMC that has PCI Express described in FRU data is enabled for payload power 0 = CM does not manage PCI Express clock
cm_pcie_activate_rc_last	0	1 = activate PCIE RC last in sequence, independent of backplane activation sequence 0 = use standard activation sequence from backplane FRU data

Configuration status can be shown by the following clicm command

```
# clicm
CM> pcie show status
Fabric   Station Port Type       State    Speed    Status Width Port Mode Serdes
======== ======= ==== ========== ======== ======== ====== ===== ========= ========
DEFG[1]        0    0 UPSTREAM   ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[2]        0    1 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[3]        0    2 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[4]        0    3 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[5]        5    0 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[6]        5    1 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[7]        5    2 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[8]        5    3 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[9]        4    0 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[10]       4    1 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[11]       4    2 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
DEFG[12]       4    3 DOWNSTREAM ENABLE   2.5 GT/s DOWN          E-KEYING  ENABLE
```

The clicm command “clicm pcie show config” shows the root complex configuration.

```
CM> pcie show config
Strapping                                  Value
========================================== ==========
ROOT-COMPLEX AMC1 I2C_CONFIG_ENABLE              0x0
```

For additional information about clicm commands, see “Managed Ethernet Switch” on page 27.

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3.4.6 Configuring sRIO

This section is only valid for the serial RapidIO fabric.

The sRIO infrastructure can be configured using the file "/opt/kontron/lib/variant-4.cfg"

The following listing shows the default "variant-4.cfg" file:

```
srio_activate=1
# enable INPUT/OUTPUT pins on 0x40
srio_init_early.0=i2c write 5 0x40 6 0xDD
# Enable I2C loading on SW1 and SW2
srio_init_early.1=i2c write 5 0x40 2 0x00
# enable OUTPUT pins on 0x42
srio_init_early.2=i2c write 5 0x42 6 0x01
srio_init_early.3=i2c write 5 0x42 7 0x01
# configure all ports for x4 SRIO mode
srio_init_early.4=i2c write 5 0x42 2 0x00
srio_init_early.5=i2c write 5 0x42 3 0x00
# enable OUTPUT pins on 0x44
srio_init_early.6=i2c write 5 0x44 6 0x03
srio_init_early.7=i2c write 5 0x44 7 0x00
# enable OUTPUT pins on 0x46
srio_init_early.8=i2c write 5 0x46 6 0x03
srio_init_early.9=i2c write 5 0x46 7 0x00
# disable POWERDOWN mode on all ports
srio_init_early.10=i2c write 5 0x44 2 0x00
srio_init_early.11=i2c write 5 0x44 3 0x00
srio_init_early.12=i2c write 5 0x46 2 0x00
srio_init_early.13=i2c write 5 0x46 3 0x00
#
```

The CM reads the config file on startup. It will first load factory default configurations from /opt/kontron/lib/variant-4.cfg. Then it will load configuration settings from /etc/cm.cfg (not present by default).

Settings in files loaded later take precedence over settings in files that are loaded earlier.

The following table shows possible settings

Table 3-27: SRIO Settings

Setting	Default	Description
srio_powerdown_default	1	0 = sRIO power down mode is done through e-keying 1 = ports are enabled by default 2 = ports are disabled by default
srio_powerdown_port.X	0	0 = port X is in the same mode as srio_powerdown_default 1 = port X is enabled 2 = port X is disabled
srio_init_early.N	n/a	SRIO initialization sequence executed before T3 is taken out of reset. There are a number of I2C initialization sequences executed during startup and before the sRIO T3 is taken out of reset. srio_init_early.N contains CLI commands to be executed during initialization. This can be mainly the I2C commands.

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Table 3-27: SRIO Settings (Continued)

Setting	Default	Description
srio_init_late.N		SRIO initialization sequence executed after T3 is taken out of reset. There are a number of I2C initialization sequences executed during startup and after the sRIO T3 is taken out of reset. srio_init_late.N contains CLI commands to be executed during initialization. This can be mainly the I2C commands.
srio_activate	0	0 = do not take sRIO T3 out of reset if present 1 = do assume sRIO T3 is installed, take sRIO T3 tongue out of reset and execute init sequence
srio_reset_delay_ms	200	Delay in ms after sRIO T3 tongue is taken out of reset.
srio_always_reset	0	1 = always take sRIO T3 into reset first 0 = skip sRIO initialization if sRIO T3 is not in reset

sRIO configuration status can be shown by the following clicm command

```
# clicm srio show status
CM> srio show status
Port          Unit ID Width Link   Status    Flags                Port Mode
============ ==== == ===== ====== ========= ==================== =========
DEFG[1]          0  6 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[2]          0 14 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[3]          0 12 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[4]          0  4 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[5]          0 10 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[6]          0  2 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[7]          1 14 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[8]          1  6 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[9]          1 12 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[10]         1  4 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[11]         1 10 x4    DOWN   POWERDOWN UNINIT               E-KEYING
DEFG[12]         1  2 x4    DOWN   POWERDOWN UNINIT               E-KEYING
Interlink-0      0  0 x4    UP     ACTIVE                         N/A
Interlink-1      1  0 x4    UP     ACTIVE                         N/A
Uplink-1         0  8 x4    DOWN   ACTIVE    UNINIT               N/A
Uplink-2         1  8 x4    DOWN   ACTIVE    UNINIT               N/A
```

3.4.7 Clocking Configuration

The AM4904provides a possibility to configure clocking according to the customer needs for:

- PLL settings
- Clock driver settings
- input clock frequecies
- input clock source
- output clock frequesncies
- output clock line usage

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The PLL supports the following operation mode:

- Manual Normal Mode
  In this mode, automatic reference switching is disabled and the selected reference is determined by the mode selection parameter. If the selected reference fails, the device automatically enters the holdover mode.
- Manual Holdover Mode
  In this mode, automatic reference switching is disabled and DPLL1 stays in the holdover mode.
- Manual Freerun Mode
  In this mode, automatic reference switching is disabled and DPLL1 stays in the free-run mode.
- Automatic Normal Mode (default mode)
  In this mode, automatic reference switching is enabled so that DPLL1 automatically selects the highest priority qualified reference (primary reference). If that reference fails, an automatic reference switchover to the next highest priority (secondary reference) and qualified reference is initiated. If there are no suitable references for selection, DPLL1 will stay in free-run or enter the holdover state.

The following parameters of the PLL can be configured:

Table 3-28: PLL Settings

Parameter	Value	Description
hitless-switching	enable, disable	Configure hitless reference switching
revertive-switching	enable, disable	Configure revertive switching option
switch-mask	SCM|CFM|GST|PFM, None	Set mask for failure indicators (SCM,CFM, PFM and GST) used for automatic reference switching
holdover-mask	SCM|CFM|GST|PFM, None	Set mask for failure indicators (SCM, CFM, GST and PFM) used for automatic holdover
pull-in-range	12, 52, 130, 83	Set DPLL pull-in range value in ppm
wait-restore	0..15	Set time a failed reference must be fault free before it is considered as available for synchronization
disqualify-time	0, 0.5ms, 1ms, 5ms, 10ms, 50ms, 100ms, 500ms, 1s, 2s, 2.5s, 4s, 8s, 16s, 32s, 64s	Set guard soak_timer control bits to disqualify the reference
qualify-time	2, 4, 16, 32	Set timer control bits to qualify the reference in times the time to disqualify
bandwidth	0.1, 1.7, 3.5, 14, 28, 890, fast	Set PLL loop bandwidth in Hz
phase-slope	885ns, 7.5us, 61us, unlimited	Set available phase slope limits
holdover-update	26ms, 1s, 10s, 60s	Set holdover update time
holdover-filter	bypass, 18mHz, 0.6Hz, 10Hz	Set DPLL holdover post filtering bandwidth selection

The PLL synchronizes to telecom reference input clocks 2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz).

The PLL output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz. So, the MCH is for example able to setup two different frequencies 1MHz and 20 MHZ.

The MCH has three clocks CLK1, CLK2, CLK3.

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The standard usage of these clocks is (CLK1...3 as of mTCA spec, TCLKA...D as of AMC.0 R2.0 spec):

- CLK1 (output clock to AMC TCLKA/C)
- CLK2 (input clock from AMC TCLKB/D)
- CLK3 (output clock to AMC FCLK)

Nonetheless, the CLK1 and CLK2 signals to each AMC can be configured as input or output independently.

So, the MCH is prepared to route every incoming reference clock to any AMC TCLK and can use any incoming backplane or BITS lock as reference clock, e.g. MCH CLK1 can be routed as output clock to AMC TCLKA and MCH CLK2 can be routed to AMC TCLKB.

The DPLL also supports wander and jitter filtering by configurable filter settings (default filter bandwidth is 1.7 Hz, selectable range: 0.1- 7 Hz). There are additionaly several configurable DPLL parameters as Pull-In/ Hold-in range and Phase Slope Linits. For additional information on how to use these features, please contact the Kontron support.

For information about CM clocking CLI commands, refer to chapter "Clock Commands" on page 58.

3.4.7.1 Example 1

This example describes how to configure the AM4904 to receive an external clock as primary input for the onboard PLL.

For the example the default mode (Automatic Normal Mode) is chosen.

```
clicm clock config show
STATUS                      VALUE    DESCRIPTION
=========================== ======== ================================================
PLL Mode                    0x03     Automatic Normal Mode
PLL Holdover Mode           0x01     detected
PLL Lock Mode               0x00     not detected
Reference Select Fail       0x01     detected
PLL Pull-in range           0x03     +/- 83 ppm (Stratum 4, G.824)
Reference Switch Mask       0x0c     GST, PFM,
Reference Holdover Mask     0x03     SCM, CFM,
Wait to Restore             0x00     0 min
Disqualify time             0x0a     2.5 s
Qualify time                0x01     4 * 2.5 s
Hitless Switching           0x00     enabled (build-out phase differents)
Bandwidth                   0x01     1.7 Hz
Phase slope limits          0x03     unlimited
Holdover update time        0x00     26 ms
Holdover filter bandwidth   0x00     bypass, no filtering
```

Select PLL Reference

For using an external clock as reference input for the PLL the source has to be selected.

In this example the CLK input on the front is used with a 8kHz clock connected.

```
# clicm clock reference primary front
```


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Now the status and configuration output should look like this:

```
# clicm clock reference show

SOURCE    INFO                 VALUE      DESCRIPTION
========= ==================== ========== ========================================
PRIMARY   PLL reference input  0x02
PRIMARY   SOURCE               0x0d       FRONT
PRIMARY   FREQ.                0x1f40     8kHz
PRIMARY   OOR Limit            0x03       64-83 (+/-ppm)
PRIMARY   Failure Indication   0x00
PRIMARY   Failure Mask         0x0f       SCM, CFM, GST, PFM,
SECONDARY PLL reference input  0x03
SECONDARY SOURCE               0x00       NONE
SECONDARY FREQ.                0x00
SECONDARY OOR Limit            0x03       64-83 (+/-ppm)
SECONDARY Failure Indication   0x0f       SCM, CFM, GST, PFM,
SECONDARY Failure Mask         0x0f       SCM, CFM, GST, PFM,


# clicm clock config show

STATUS                       VALUE    DESCRIPTION
============================ ======== ================================================
PLL Mode                     0x03     Automatic Normal Mode
PLL Holdover Mode            0x00     not detected
PLL Lock Mode                0x01     detected
Reference Select Fail        0x00     not detected
PLL Pull-in range            0x03     +/- 83 ppm (Stratum 4, G.824)
Reference Switch Mask        0x0c     GST, PFM,
Reference Holdover Mask      0x03     SCM, CFM,
Wait to Restore              0x00     0 min
Disqualify time              0x0a     2.5 s
Qualify time                 0x01     4 * 2.5 s
Hitless Switching            0x00     enabled (build-out phase differents)
Bandwidth                    0x01     1.7 Hz
Phase slope limits           0x03     unlimited
Holdover update time         0x00     26 ms
Holdover filter bandwidth    0x00     bypass, no filtering
```

The output displayed by the commands “clock reference show” and “clock config show” are values read from PLL (ZL30143). For more information about these values, please refer to the PLL manual.

Enable clock signal to AMC input

The output buffers to the AMC clocks (CLK1 and CLK2) can be selected independently. The supported devices are: 1=AMC1, 2=AMC2, 3=AMC3 ...

The output signal frequencies of the PLL to source the AMC’s can be selected from the following predefined values:

- 8khz
- 1544khz
- 2048khz
- 19440khz

```
# clicm clock output
Set clock output driver and select frequency
clock output <DEVICE> {clk1|clk2} {8khz|1544khz|2048khz|19440khz}
```


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Example: Enable a 8kHz signal to AMC in slot 1:

```
# clicm clock output 1 clk1 8khz
```

Show the status of the output/input buffers:

```
# clicm clock status show

ID   CLK1-OUT   SRC  FREQ          CLK2-OUT   SRC  FREQ          CLK1-IN    CLK2-IN
==== ========== ==== ========== == ========== ==== ========== == ========== ==========
1    enabled    0x09 8kHz          disabled   0x00               disabled   disabled
2    disabled   0x00               disabled   0x00               disabled   disabled
3    disabled   0x00               disabled   0x00               disabled   disabled
4    disabled   0x00               disabled   0x00               disabled   disabled
5    disabled   0x00               disabled   0x00               disabled   disabled
6    disabled   0x00               disabled   0x00               disabled   disabled
7    disabled   0x00               disabled   0x00               disabled   disabled
8    disabled   0x00               disabled   0x00               disabled   disabled
9    disabled   0x00               disabled   0x00               disabled   disabled
10   disabled   0x00               disabled   0x00               disabled   disabled
11   disabled   0x00               disabled   0x00               disabled   disabled
12   disabled   0x00               disabled   0x00               disabled   disabled
```

Table 3-29: Command output

Column	Description
ID	AMC ID
CLK1-OUT	CLK1 out buffer state
SRC	Selected source (CPLD register 0x60-0x6C)
FREQ	Configured frequency
CLK2-OUT	CLK2 out buffer state
SRC	Selected source (CPLD register 0x70-0x7C)
FREQ	Configured frequency
FCLK-OUT	FCLKA out buffer state (PCIe clock)
FREQ	PCIe frequency
CLK1-IN	CLK1 receive buffer state
CLK2-IN	CLK2 receive buffer state

Clock configuration on Start-up

The configuration will not be stored and reloaded automatically. If a configuration should be applied on start-up the commands has to be added in the “/etc/cm.cfg”.

For the example the following lines has to be added in /etc/cm.cfg:

```
startup_active.0=clock reference primary front
startup_active.1=clock output 1 clk1 8kh
```


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3.4.8 MCH Redundancy Support

The CM can be used in chassis with dual MCH slots. In this configuration, the MCH will detect the presence of a second MCH.

If both MCH are compatible, they will switch to an active/standby mode, where the standby MCH will constantly monitor the active MCH using redundant communication channels. When it does detect that the active MCH is no longer responsding, it will initiate a fail-over, will rediscover currently active modules in the chassis and will take over management of the carrier.

Two independent channels are used for communication. One is the standard redundant backplane IPMB-0. Any MCH will periodically distribute its status on the bus to the other MCH via a Kontron OEM IPMI command send to the MCMC. In addition, a heartbeat is sent periodically between both MCHs using a PLD interlink. This heartbeat is also used to detect health of the other MCH.

When both communication channels indicate a remote failure, the backup MCH may then initiate a failover. It signals this transition to the active MCH using the PLD interlink. The PLD on the active MCH will then safely isolate/shutdown external interfaces related to carrier management on the failed MCH.

Redundancy status of the MCH will be shown using the cm command “rm status”. There is also a command (rm xover reset) that forces the redundant MCH to reset.

For additional information about CM redundance commands, see chapter Redundancy Commands.

3.4.9 Cooling Unit Management

The Carrier Manager implements an intelligent fan control that works together with MicroTCA compliant Cooling Units that are connected to the IPMB-0 bus.

Once the CM has discovered that the chassis supports cooling units it starts the fan control module. The fan control module can be forced off if the config parameter fan_control is set to zero.

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The fan control module implements the following states:

Table 3-30: FAN control states

State	Description	Actions
Normal	The fan control is not in any other state.	The fan level is decreased in steps of fan_stepdown fan level steps each fan_dec_timeout seconds down to the dynamic fan level. When the dynamic fan level is reached it is decremented each fan_dynamic_timeout seconds until fan_norm_level is reached.
Minor	The fan control is not in critical and error state and at least one temperature sensor reports that the upper non-critical threshold has been crossed.	If the current fan level is equal the dynamic fan level and the previous state was normal then the dynamic fan level is increased by one. The current fan level is increased in steps of fan_stepup fan level steps each fan_inc_timeout seconds until the maximum fan level is reached.
Critical	The fan control is not in error state and at least one temperature sensor reports that the upper critical or upper non-recoverable threshold has been crossed.	If the current fan level is equal the dynamic fan level and the previous state was normal then the dynamic fan level is increased by one. The current fan level is set to the maximum value.
Error	At least one of the cooling units is not in M4 or M5 state or the fan control module has not been discovered all cooling units or the fan control is not able to adjust the speed of a cooling unit.	The fan level is set to the maximum value until this state is left.

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3.5 IPMI

3.5.1 Supported IPMI Commands

3.5.1.1 Standard Commands

Part of the command list in IPMI specification 1.5.

Table 3-31: IPMI Device Commands

	IPMI Spec. section	NetFn	CMD	Support on AM4904
IPMI Device "Global" Commands				
Get Device ID	IPMI 1.5	App	01h	YES
Cold Reset	IPMI 1.5	App	02h	YES
Warm Reset	IPMI 1.5	App	03h	YES
Get Self Test Result	IPMI 1.5	App	04h	YES
Manufacturing Test On	IPMI 1.5	App	05h	YES
Set ACPI Power State	IPMI 1.5	App	06h	
Get ACPI Power State	IPMI 1.5	App	07h	
Get Device GUID Command	IPMI 1.5	App	08h	
Broadcast "Get Device ID"	IPMI 1.5	App	01h	YES
BMC Watchdog Timer Commands				
Reset Watchdog Timer	IPMI 1.5	App	22h	YES
Set Watchdog Timer	IPMI 1.5	App	24h	YES
Get Watchdog Timer	IPMI 1.5	App	25h	YES
BMC Device and Messaging Commands				
Set BMC Global Enables	IPMI 1.5	App	2Eh	
Get BMC Global Enables	IPMI 1.5	App	2Fh	
Clear Message Flags	IPMI 1.5	App	30h	
Get Message Flags	IPMI 1.5	App	31h	
Enable Message Channel Receive	IPMI 1.5	App	32h	
Get Message	IPMI 1.5	App	33h	
Send Message	IPMI 1.5	App	34h	YES
Read Event Message Buffer	IPMI 1.5	App	35h	
Get BT Interface Capabilities	IPMI 1.5	App	36h	
Get System GUID	IPMI 1.5	App	37h	
Get Channel Authentication Capabilities	IPMI 1.5	App	38h	YES
Get Session Challenge	IPMI 1.5	App	39h	YES
Activate Session	IPMI 1.5	App	3Ah	YES
Set Session Privilege Level	IPMI 1.5	App	3Bh	YES
Close Session	IPMI 1.5	App	3Ch	YES
Get Session Info	IPMI 1.5	App	3Fh	YES
Get Auth Code	IPMI 1.5	App	3Fh	YES

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Table 3-31: IPMI Device Commands (Continued)

	IPMI Spec. section	NetFn	CMD	Support on AM4904
Set Channel Access	IPMI 1.5	App	40h	YES
Get Channel Access	IPMI 1.5	App	41h	YES
Get Channel Info	IPMI 1.5	App	42h	YES
Set User Access	IPMI 1.5	App	43h	YES
Get User Access	IPMI 1.5	App	44h	YES
Set User Name	IPMI 1.5	App	45h	YES
Get User Name	IPMI 1.5	App	46h	YES
Set User Password	IPMI 1.5	App	47h	
Serial Over LAN support				
Activate Payload	IPMI 2.0	App	48h	
Deactivate Payload	IPMI 2.0	App	49h	
Get Payload Activation Status	IPMI 2.0	App	4Ah	
Get Payload Instance Info	IPMI 2.0	App	4Bh	
Set User Payload Access	IPMI 2.0	App	4Ch	
Get User Payload Access	IPMI 2.0	App	4Dh	
Get Channel Payload Support	IPMI 2.0	App	4Eh	
Get Channel Payload Version	IPMI 2.0	App	4Fh	
Get Channel OEM Payload Info	IPMI 2.0	App	50h	
Master Write-Read	IPMI 1.5	App	52h	
Get Channel Cipher Suites	IPMI 2.0	App	54h	
Suspend/Resume Payload Encryption	IPMI 2.0	App	55h	
Set Channel Security Keys	IPMI 2.0	App	56h	
Get System Interface Capabilities	IPMI 2.0	App	57h	
Chassis Device Commands				
Get Chassis Capabilities	IPMI 1.5	Chassis	00h	YES
Get Chassis Status	IPMI 1.5	Chassis	01h	YES
Chassis Control	IPMI 1.5	Chassis	02h	YES
Chassis Reset	IPMI 1.5	Chassis	03h	YES
Chassis Identify	IPMI 1.5	Chassis	04h	
Set Front Panel Button Enables	IPMI 1.5	Chassis	0Ah	
Set Chassis Capabilities	IPMI 1.5	Chassis	05h	
Set Power Restore Policy	IPMI 1.5	Chassis	06h	
Set Power Cycle Interval	IPMI 1.5	Chassis	0Bh	
Get System Restart Causes	IPMI 1.5	Chassis	07h	
Set System Boot Options	IPMI 1.5	Chassis	08h	
Get System Boot Options	IPMI 1.5	Chassis	09h	
Get POH Counter	IPMI 1.5	Chassis	0Fh	
Event Commands				
Set Event Receiver	IPMI 1.5	S/E	00h	YES
Get Event Receiver	IPMI 1.5	S/E	01h	YES

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Table 3-31: IPMI Device Commands (Continued)

	IPMI Spec. section	NetFn	CMD	Support on AM4904
Platform Event (a.k.a. "Event Message")	IPMI 1.5	S/E	02h	YES
PEF and Alerting Commands				
Get PEF Capabilities	IPMI 1.5	S/E	10h	
Arm PEF Postpone Timer	IPMI 1.5	S/E	11h	
Set PEF Configuration Parameters	IPMI 1.5	S/E	12h	
Get PEF Configuration Parameters	IPMI 1.5	S/E	13h	
Set Last Processed Event ID	IPMI 1.5	S/E	14h	
Get Last Processed Event ID	IPMI 1.5	S/E	15h	
Alert Immediate	IPMI 1.5	S/E	16h	
PET Acknowledge	IPMI 1.5	S/E	17h	
Sensor Device Commands				
Get Device SDR Info	IPMI 1.5	S/E	20h	YES
Get Device SDR	IPMI 1.5	S/E	21h	YES
Reserve Device SDR Repository	IPMI 1.5	S/E	22h	YES
Get Sensor Reading Factors	IPMI 1.5	S/E	23h	YES
Set Sensor Hysteresis	IPMI 1.5	S/E	24h	YES
Get Sensor Hysteresis	IPMI 1.5	S/E	25h	YES
Set Sensor Threshold	IPMI 1.5	S/E	26h	YES
Get Sensor Threshold	IPMI 1.5	S/E	27h	YES
Set Sensor Event Enable	IPMI 1.5	S/E	28h	YES
Get Sensor Event Enable	IPMI 1.5	S/E	29h	YES
Re-arm Sensor Event	IPMI 1.5	S/E	2Ah	
Get Sensor Event Status	IPMI 1.5	S/E	2Bh	
Get Sensor Reading	IPMI 1.5	S/E	2Dh	YES
Set Sensor Type	IPMI 1.5	S/E	2Eh	
Get Sensor Type	IPMI 1.5	S/E	2Fh	
FRU Device Commands				
Get FRU Inventory Area Info	IPMI 1.5	Storage	10h	YES
Read FRU Data	IPMI 1.5	Storage	11h	YES
Write FRU Data	IPMI 1.5	Storage	12h	YES
SDR Device Commands (SDRR)				
Get SDR Repository Info	IPMI 1.5	Storage	20h	
Get SDR Repository Allocation Info	IPMI 1.5	Storage	21h	
Reserve SDR Repository	IPMI 1.5	Storage	22h	
Get SDR	IPMI 1.5	Storage	23h	
Add SDR	IPMI 1.5	Storage	24h	
Partial Add SDR	IPMI 1.5	Storage	25h	
Delete SDR	IPMI 1.5	Storage	26h	
Clear SDR Repository	IPMI 1.5	Storage	27h	
Get SDR Repository Time	IPMI 1.5	Storage	28h	

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Table 3-31: IPMI Device Commands (Continued)

	IPMI Spec. section	NetFn	CMD	Support on AM4904
Set SDR Repository Time	IPMI 1.5	Storage	29h	
Enter SDR Repository Update Mode	IPMI 1.5	Storage	2Ah	
Exit SDR Repository Update Mode	IPMI 1.5	Storage	2Bh	
Run Initialization Agent	IPMI 1.5	Storage	2Ch	
SEL Device Commands				
Get SEL Info	IPMI 1.5	Storage	40h	YES
Get SEL Allocation Info	IPMI 1.5	Storage	41h	YES
Reserve SEL	IPMI 1.5	Storage	42h	YES
Get SEL Entry	IPMI 1.5	Storage	43h	YES
Add SEL Entry	IPMI 1.5	Storage	44h	YES
Partial Add SEL Entry	IPMI 1.5	Storage	45h	
Delete SEL Entry	IPMI 1.5	Storage	46h	YES
Clear SEL	IPMI 1.5	Storage	47h	YES
Set SEL Time	IPMI 1.5	Storage	48h	YES
Get SEL Time	IPMI 1.5	Storage	49h	YES
Get Auxiliary Log Status	IPMI 1.5	Storage	50h	
Set Auxiliary Log Status	IPMI 1.5	Storage	51h	
LAN Device Commands				
Set LAN Configuration Parameters	IPMI 1.5	Transport	01h	
Get LAN Configuration Parameters	IPMI 1.5	Transport	02h	
Suspend BMC ARPs	IPMI 1.5	Transport	03h	
GET IOP/UDP/RMCP Statistics	IPMI 1.5	Transport	04h	
Serial/Modem Device Commands				
Set Serial/Modem Configuration	IPMI 1.5	Transport	10h	
Get Serial/Modem Configuration	IPMI 1.5	Transport	11h	
Set Serial/Modem Mux	IPMI 1.5	Transport	12h	
Get TAP Response Codes	IPMI 1.5	Transport	13h	
Set PPP UDP Proxy Transmit Data	IPMI 1.5	Transport	14h	
Get PPP UDP Proxy Transmit Data	IPMI 1.5	Transport	15h	
Send PPP UDP Proxy Packet	IPMI 1.5	Transport	16h	
Get PPP UDP Proxy Receive Data	IPMI 1.5	Transport	17h	
Serial/Modem Connection Active	IPMI 1.5	Transport	18h	
Callback	IPMI 1.5	Transport	19h	
Set User Callback Options	IPMI 1.5	Transport	1Ah	
Get User Callback Options	IPMI 1.5	Transport	1Bh	
SOL Activating	IPMI 2.0	Transport	20h	
Set SOL Configuration Parameters	IPMI 2.0	Transport	21h	
Get SOL Configuration Parameters	IPMI 2.0	Transport	22h	
Bridge Management Commands (ICMB)	IPMI 1.5	Bridge	00h – 0Ch	
Discovery Commands (ICMB)	IPMI 1.5	Bridge	10h – 14h	

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Table 3-31: IPMI Device Commands (Continued)

	IPMI Spec. section	NetFn	CMD	Support on AM4904
Bridging Commands (ICMB)	IPMI 1.5	Bridge	20h – 21h	
Event Commands (ICMB)	IPMI 1.5	Bridge	30h – 35h	
OEM Commands for Bridge NetFn	IPMI 1.5	Bridge	C0h– FEh	
Other Bridge Commands	IPMI 1.5	Bridge	FFh	

3.5.1.2 PICMG commands

Table 3-32: PICMG Commands

Command name	Standard	NetFn	CMD	Support on AM4904
Get PICMG Properties	PICMG 3.0	PICMG	00h	YES
Get Address Info	PICMG 3.0	PICMG	01h	YES
Get Shelf Address Info	PICMG 3.0	PICMG	02h	YES
Set Shelf Address Info	PICMG 3.0	PICMG	03h	YES
FRU Control	PICMG 3.0	PICMG	04h	YES
Get FRU LED Properties	PICMG 3.0	PICMG	05h	YES
Get LED Color Capabilities	PICMG 3.0	PICMG	06h	YES
Set FRU LED State	PICMG 3.0	PICMG	07h	YES
Get FRU LED State	PICMG 3.0	PICMG	08h	YES
Set IPMB State	PICMG 3.0	PICMG	09h	YES
Set FRU Activation Policy	PICMG 3.0	PICMG	0Ah	YES
Get FRU Activation Policy	PICMG 3.0	PICMG	0Bh	YES
Set FRU Activation	PICMG 3.0	PICMG	0Ch	YES
Get Device Locator Record ID	PICMG 3.0	PICMG	0Dh	YES
Set Port State	PICMG 3.0	PICMG	0Eh	
Get Port State	PICMG 3.0	PICMG	0Fh	
Compute Power Properties	PICMG 3.0	PICMG	10h	
Set Power Level	PICMG 3.0	PICMG	11h	
Get Power Level	PICMG 3.0	PICMG	12h	
Renegotiate Power	PICMG 3.0	PICMG	13h	
Get Fan Speed Properties	PICMG 3.0	PICMG	14h	YES
Set Fan Level	PICMG 3.0	PICMG	15h	YES
Get Fan Level	PICMG 3.0	PICMG	16h	YES
Bused Resource	PICMG 3.0	PICMG	17h	
Get IPMB Link Info	PICMG 3.0	PICMG	18h	
Set Fan Policy	PICMG 3.0	PICMG	1Ch	
Get Fan Policy	PICMG 3.0	PICMG	1Dh	
FRU Control Capabilities	PICMG 3.0	PICMG	1Eh	YES

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Table 3-32: PICMG Commands (Continued)

Command name	Standard	NetFn	CMD	Support on AM4904
FRU Inventory Device Lock Control	PICMG 3.0	PICMG	1Fh	
FRU Inventory Device Write	PICMG 3.0	PICMG	20h	
Get Shelf Manager IP Addresses	PICMG 3.0	PICMG	21h	
Get Shelf Power Allocation	PICMG 3.0	PICMG	22h	

3.5.1.3 AMC.0 Commands

Table 3-33: AMC.0 Commands

Command name	Standard	NetFn	CMD	Support on AM4904
Set AMC Port State	AMC.0	PICMG	19h	YES
Get AMC Port State	AMC.0	PICMG	1Ah	YES
Set Clock State	AMC.0	PICMG	2Ch	YES
Get Clock State	AMC.0	PICMG	2Dh	YES

3.5.1.4 MicroTCA.0 Command

Table 3-34: MicroTCA.0 Commands

Command name	Standard	NetFn	CMD	Support on AM4904
Get Location Information	uTCA.0	PICMG	23h	YES
Power Channel Control	uTCA.0	PICMG	24h	YES
Get Power Channel Stats	uTCA.0	PICMG	25h	YES
PM Reset	uTCA.0	PICMG	26h	YES
Get PM Status	uTCA.0	PICMG	27h	YES
PM Heartbeat	uTCA.0	PICMG	28h	YES
Get Telco Alarm Capability	uTCA.0	PICMG	29h	YES
Set Telco Alarm State	uTCA.0	PICMG	2Ah	YES
Get Telco Alarm State	uTCA.0	PICMG	2Bh	YES

3.5.1.5 Kontron specific OEM Commands

Table 3-35: Kontron specific OEM Commands

Command name	Standard	NetFn	CMD	Support on AM4904
Get Release Info	30h	3	01h	YES
Redundancy management command	30h	3	10h	YES

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3.5.1.5.1 Get Release Info

Command Name	NetFn	LUN	Command Number
Get Release Info	3	30h	01h

	Byte Num	Data Field
Request Data	1	Pass Code 0: ~'S'
	2	Pass Code 1: ~'1'
	3	Pass Code 2: ~'1'
	4	Pass Code 3: ~'0'
	5	Pass Code 4: ~'0'
Response Data	1	Completion Code.
	2..5	Release Code
	6..13	Subrelease Release Code
	14..21	Date Code

3.5.1.5.2 Redundancy management command

Command Name	NetFn	LUN	Command Number
Redundancy management command	3	30h	10h

	Byte Num	Data Field
Request Data	1	Pass Code 0: ~'S'
Response Data	1	Completion Code.
	2	Control block version (1)
	3	SW Major version
	4	SW Minor version
	5	current role: 0=inactive 1=Request_Active 2=Active 3=Backup

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3.5.2 Board FRU Information

This FRU information contains the IPMI defined Board and Product Information areas that hold the part number and serial number of the board and the Multirecord Information Area that contains the PICMG defined Point to Point Information records.

Supported are the following FRU data areas and data fields (shown values are examples, which may differ, depending on the used board typ).

3.5.2.1 CM

The Carrier Manager FRU data (FRU-ID 3/FRU-ID 4 depending on used slot in chassis) contains information about the current software release such as release date and release version.

This data is returned when module is addressed as role CM.

FRU Board Info Area

- Manufacturing date / time: <auto>, e.g. 2010-06-17 11:33
- Board manufacturer: Kontron
- Board Product Name: mTCA Carrier Manager
- Board Serial Number: N/A
- Board Part Number: N/A
- FRU File ID: <release>, e.g. GA 2.01

FRU Product Info Area

- Product manufacturer: Kontron
- Product Name: mTCA Carrier Manager
- Product Part Number: N/A
- Product Version: <auto>, e.g. 2.01
- Product Serial Number: 0
- Asset Tag: 0
- FRU File ID: <auto>

3.5.2.2 MCMC

This data is returned when module is addressed as role MCMC.

FRU Board Info Area

- Board manufacturer: Kontron
- Board Product Name: AM4904-Base
- Board Serial Number: xxxxxxxxxx
- Board Part Number: 1028-5229
- FRU File ID: RU-S1100-FABRIC-BASE-1P0
- Custom field(s): MAC=00:00:00:00:00:00/32

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FRU Product Info Area

- Product manufacturer: Kontron
- Product Name: AM4904-Base
- Product Part Number: 1028-5229
- Product Version: 1
- Product Serial Number: xxxxxxxxxx
- Asset Tag: 0
- FRU File ID: FRU-S1100-FABRIC-BASE-1P0

3.6 Bootloader

On the AM4904 board, the bootloader 'u-boot' (universal bootloader) is used. The bootloader initializes the main components of the board like CPU, SDRAM, serial lines etc. for operation. After this, kernel and application are started from flash.

3.6.1 Power On Self Test

Upon power on or system reset, the bootloader performs a set of Power On Self Tests (POST) to check the integrity of specific components. Components where a POST is available are:

- SDRAM
- PPC405 serial line
- PPC405 I2C
- PPC405 FE

In the case that a POST fails, a POST error code is written into the postcode high byte register of the onboard CPLD. The boot process is not stopped as there are good chances the board can boot even in case of POST errors. The postcode high byte register is also accessible by the PM which can report error codes to a separate management instance. Thus more comprehensive diagnostic tests could be started.

The following table shows a list of available POST routines including POST error codes.

Table 3-36: POST Routines and Error Codes

Device	Test	POST Numerical Error Code	POST Error Code
SDRAM	Data bus - walking 1 test	0x20	PCW_DLINE
SDRAM	Address bus - walking 1 test	0x40	PCW_ALINE
SDRAM	Memory - read/write test	0x80	PCW_MEM
PPC405 UART	Serial loopback teststring	0x01	PCW_SERIAL
PPC405 I2C	Bus scan for devices from I2C_ADDR_LIST	0x02	PCW_I2C
PPC405 FE	Phy access	0x08	PCW_ETH1
PPC405 FE	Phy loopback test using special Ethernet test frame	0x10	PCW_ETH2
KCS	KCS READY signal test	0x04	KCSCTL

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3.6.2 Bootloader shell and options

The boot process can be interrupted by entering the bootstopphrase "stop". Enter the string on the serial console when the 'type configured bootstopkey to abort' message appears on the screen. This will open a bootloader shell session.

“?” provides a list of possible commands, “printenv” provides a list of environment settings.

The bootloader shell can be used to customize boot options and system startup.

For additional information about customization of u-boot, please refer to the u-boot webpage:

http://sourceforge.net/projects/u-boot/

Table 3-37: Bootloader Environment Variables

Name	Description
ethaddr	Contains the default base MAC address of the board. If this is not set, the MAC address from VPD is used.
bootcmd	This variable defines a command string that is automatically executed when the initial countdown is not interrupted. This command is only executed when the variable bootdelay is also defined!
bootcmdflash	Contains the standard startup script for loading OS image from flash partition command. This will load the Linux kernel and start it with a CRAMFS (TBC, maybe INITRD) type root file system.
bootcmdnet	Contains the standard startup script for loading OS image from network
bootcmdprd	Contains the standard startup script for use during board production
bootcmdrecover	Contains standard startup script for board firmware recovery in boot firmware
bootdelay	After reset, U-Boot will wait this number of seconds before it executes the contents of the bootcmd variable. During this time a countdown is printed, which can be interrupted by pressing any key. Set this variable to 0 boots without delay. Be careful: depending on the contents of your bootcmd variable, this can prevent you from entering interactive commands again forever! Set this variable to -1 to disable autoboot. Default: 3 for flash based bootloader, -1 for RAM resident bootloader
bootsource	When the standard boot sequence is used, contains the boot source, either flash, net, prd to select the respective boot sequence to activate. It is only used when bootcmd contains the default startup script, which may be overridden by the user. default: flash
ethact	Default network interface used by network commands (bootp, tftpboot et al) default: ppc_4xx_eth0
loadaddr	Default load address for network transfers. This is used as a temporary storage for netbooting and firmware updates. default: 0x08000000
clear_env	Command script (use with “run clear_env”) that erases the U-Boot environment for the active image
clear_config	Erase config partition to restore factory defaults for Linux BSP settings.
flash_update	Command script to flash a Linux kernel and rootfs image transferred with tftpboot to the active Linux kernel and rootfs partition

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Table 3-37: Bootloader Environment Variables (Continued)

Name	Description
watchdogboot	0 – disable boot monitor watchdog (default) 5...n – timeout in seconds before boot monitor watchdog fires default: 5 Note: This is the pBMWD watchdog
watchdogos	0 – disable OS load watchdog 15..dis.n – timeout in seconds before load OS watchdog fires default: 45 Note: This is the pOSWD watchdog
recover_flash	Command script that is executed when the onboard flash is corrupted
reset_unknown	0 – do not cold reset when unknown reset type is detected 1 – enable cold reset when unknown reset type is detected (default)
stop_posterr	0 – ignore POST errors (default) 1 – Start CLI on POST errors
disable_rollback	0 – rollback when CRC check of kernel or rootfs fails (default) 1 – do not rollback
pci_ethreset	1 – do not automatically disable ETH RESET to T2/T3 (default) 0 – do automatically disable ETH RESET to T2/T3

3.7 Firmware Administration

A running AM4904 system requires – after the bootloader has passed control to the kernel – the kernel itself, the root file system (initrd), the FASTPATH switching application and the CM application. These software components make up the AM4904 firmware.

The board supports two permanent storage devices, one is an on-board integrated 64 MB NOR flash that is also used as the power-up boot source and contains bootloader as well as operating system and application data. The other is an onboard NAND flash device.

The onboard NOR flash is logically divided into two banks, where the first bank is used during regular system operation. The second bank normally contains an exact copy of the first bank and can be used to restore normal system operation in case the first bank contains an invalid boot image. The first bank include flash partitions mtd0-mtd4, the second bank (rollback image) is stored in flash partition mtd6. Persistent system data is stored in partition mtd5 and backed up in mtd7. The write protected partition mtd8, which consists of 1 single flash sector, holds the boot firmware.

The partition scheme of the flash is shown below:

Table 3-38: FLASH Partition Scheme (64MB)

Partition	Description	Size	MTD
u-boot	Secondary bootloader based on U-Boot	512 kB	mtd0
vpd	Vital Product Data	256 kB	mtd1
env	Redundant bootloader environment (each 128 KB)	256 kB	mtd2
kernel	Linux system (kernel and initrd multi image)	26112 kB	mtd3
config	Read/Write Configuration data	4352KB	mtd4

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Table 3-38: FLASH Partition Scheme (64MB) (Continued)

Partition	Description	Size	MTD
pdata	Persistent system data (SEL, FRU data)	1024 kB	mtd5
backup	Contains backup image. Copy of mtd0-4	31488 kB	mtd6
pdata_b	Backup of pdata (mtd5) partition	1024 kB	mtd7
boot-fw	Write protected boot firmware based on U-Boot	512 kB	mtd8

When the system boots up, software is always loaded from the first logical flash bank. The second logical flash bank serves as a backup in case that the first bank fails due to data corruption or a failing update procedure.

If the firmware in logical flash bank 1 gets corrupted, the system fails sooner or later and will be rebooted. In this case the corrupted firmware will recover automatically without user interaction. The system recognizes the error condition and starts recovery of logical flash bank 1 from logical flash bank 2. After recovery has been finished, the system will restart and boot the recovered flash bank. Persistent system data which is stored in flash partition mtd5 is not changed by this procedure.

3.7.1 Updating Firmware

Firmware update is always done in the first logical flash bank. In case that the updated firmware gets corrupted due to power loss or similar reasons, the updated firmware will fail. This will cause flash recovery with logical flash bank 2 contents which is unmodified at that time. Only when the updated firmware is started properly, logical flash bank 2 can be overwritten to have both active and recovery firmware synchronized to the same contents.

A software release for the AM4904 consists of one software package, am4904-<base|pcie|srio>-update-<release>. The package is a tar archive containing an image of the software and a MD5 checksum file for consistency check. The name of the package file is arbitrary but the file names in the archive must not be altered.

When performing a firmware update, the software package is loaded from a remote TFTP server. A software update of the AM4904 is done by performing the following steps:

1. Prepare network access of the board
2. log in to the privileged exec mode of the CLI of the board
3. Download initrd image into image 1 (=logical flash bank 1) of the flash memory

   ```
   (Ethernet Fabric) #copy tftp://192.168.50.5/<updatepackage-name>.pkg image1
   ```

   This downloads the specified package file via TFTP and writes the image into the logical flash bank of image 1. The CRC32 checksum of the image is checked before writing it into flash.

   Note: It is not possible to copy the update package into image 2! Note also that new SW will always use a default configuration.

4. Restart the board

   ```
   (Ethernet Fabric) #reload
   ```


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This command starts the updated software image copied before. As described above, a corrupted software image will be detected and an automatic rollback is performed. The user will always end up in a shell with either the updated software or the rollback system booted. This allows a fail-safe upgrade of the AM4904 software.

5. Check availability of valid boot image in image1 using the command

```
(Ethernet Fabric) #show bootvar
Image Descriptions
  active (image1): Product ID          : 1100
                   Product Variant     : 0
                   U-Boot Release      : GA 2.00
                   Manufacturer ID     : 15000
                   Build-Date          : 20090916042035

  backup (image2): Product ID          : 1100
                   Product Variant     : 0
                   U-Boot Release      : GA 2.00
                   Manufacturer ID     : 15000
                   Build-Date          : 20090916042035


Images currently available on Flash

  active (image1)   backup (image2)
  ----------------  ----------------
  GA 0.00         GA 0.00
```

6. After the updated image has been checked to operating correctly, it is recommended to copy image 1 to image 2 to have a fully redundant system

```
(Ethernet Fabric) #copy image1 image2
```

3.7.2 Updating PLD



Note...

PLD (FPGA) updates should be treated very carefully. Please refer to Software Release Notes about information, whether a PLD update is required at all.



Note...

The new FPGA code will be used after the next power-cycle of the complete board. This means that the board must be removed and re-inserted from its slot.

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The onboard FPGA can be updated using the 'copy' command from the Fastpath CLI:

```
(Ethernet Fabric) #copy tftp://<ip_addr>/am4904-pld-update-GA-2.03.pkg image2

Mode..................................... TFTP
Set Server IP.............................. 192.168.50.5
Path..................................... ./
Filename................................. am4904-pld-update-GA-2.03.pkg
Data Type................................ Code
Destination Filename..................... image2

Management access will be blocked for the duration of the transfer
Are you sure you want to start? (y/n) y
Write image to flash starting...

File transfer operation completed successfully.

(Ethernet Fabric) #
```


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Chapter 4

Hardware Installation

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4 Hardware Installation

The AM4904 has been designed for easy installation. However, the following standard precautions, installation procedures and general information must be observed to ensure proper installation and to preclude damage to the product, other system components, or injury to personnel.

4.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AM4904. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

WARNING

MCH modules require, by design, a considerable amount of force in order to (dis)engage the module from/in the MicroTCA™ backplane connector. For this reason, when inserting or extracting the module, apply only as much force as required to preclude damage to either the module's handle or the front panel.

DO NOT push on the module handle to seat the module in the backplane connector. Do not use the module handle as a grip to handle the board outside of the chassis slot.

Use of excessive force, bending or rotation of the module handle will result in damage to the handle or the module's locking mechanism. Kontron disclaims all liability for damage to the module or the system as a result of failure to comply with this warning.



ESD Sensitive Device

This AMC board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

WARNING

This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

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Caution, Laser Light!



Laser light from fiber-optic transmission cables and components can damage your eyes. The laser components plugged into the switch are Class 1 laser components. Class 1 laser is considered incapable of producing damaging radiation levels during normal operation or maintenance.

To avoid damaging your eyes and to continue safe operation in case of abnormal circumstances:

- Never look directly into the outlets of fiber-optic transmission components or fiber-optic cables with unprotected eyes.
- Never allow fiber-optic transmission path to operate until all the connections have been made.
- Always fit protective plugs to any unused ports of the switch.

4.2 Hot Swap Procedures

The AM4904 is designed for hot swap operation. Hot swapping allows the coordinated insertion and extraction of modules without disrupting other operational elements within the system.

The procedures contained in this section are also applicable for “non-operating systems” with the exception of indications and functions which require power to be applied.

4.2.1 Hot Swap Insertion

To insert the MCH module proceed as follows:

1. Ensure that the safety requirements indicated in section 4.1 are observed.

WARNING



Failure to comply with the instruction above may cause damage to the board or result in improper system operation.



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2. Ensure that the module is properly configured for operation in accordance with the application requirements before installation.

WARNING



Care must be taken when applying the procedures below to ensure that neither the AM4904 nor other system boards are physically damaged by the application of these procedures.



3. Ensure that the module handle is in the “Unlocked” position.
4. Using the front panel as a grip, carefully insert the module into the slot designated by the application requirements until it makes contact with the backplane connector.
5. Apply pressure to the front panel until the module is properly seated in the backplane connector. This may require a considerable amount of force. Apply pressure only to the front panel, not the module handle. During seating in the connector, there is a noticeable “snapping” of the board into the connector. When the board is seated it should be flush with the system front panel.

In the case of a running system, the following occurs:

- The BLUE HS LED turns on.
  When the module is seated, the module management power is applied and the BLUE HS LED turns on. (No payload power is applied at this time).
- Connect all external interfacing cables to the module as required and ensure that they are properly secured.
- Push the module handle in the “Locked” position. When the module handle is in the “Locked” position, the module is locked and the hot swap switch is actuated.

In the case of a running system, the following occurs:

- The BLUE HS LED turns off.
  The power module now enables the payload power for the MCH.
- The MCH module is now operating.

4.2.2 Hot Swap Extraction

To extract the MCH module proceed as follows:

1. Ensure that the safety requirements indicated in section 4.1 are observed.
2. Pull the module handle in the “Hot Swap” position.

When the module handle is in the “Hot Swap” position, the extraction process of the module is initiated and the following occurs:

- The BLUE HS LED displays short blinks. When the power module IPMI controller receives the handle opened event, it sends a command to the MCMC with a request to perform short blinks of the BLUE HS LED.
  This indicates that the MCH is waiting to be deactivated.
  Once the MCH receives the permission to continue the deactivation, all used ports are disabled.
- The BLUE HS LED turns on.
  The Intelligent Platform Management Controller on the power module disables the module's payload power and the BLUE HS LED is turned on.
  Now the module is ready to be safely extracted.

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WARNING



The Blue LED has to be solid on before removing the module. If the system does not support Hot Swap, it has to be assured that the 12V payload power is switched off.

Removing the module with 12V payload power still enabled may damage it.



3. Pull the module handle in the “Unlocked” position.
4. Disconnect any interfacing cables that may be connected to the module.
5. Disengage the module from the backplane connector by pulling on the module handle. On four-tongue-MCHs with fabric DEFG infrastructure, an additional extraction grip is available because of the enhanced extraction force.
6. Using the front panel as a grip, remove the module from the chassis.
7. Dispose of the module as required.

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Chapter 5

Power Considerations

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5 Power Considerations

5.1 AM4904 Input Voltage Ranges

The AM4904 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The AM4904 requires two power sources, the module management power (nominal: 3.3V DC) and payload power (nominal: 12V DC).

The following table specifies the ranges for the different input power voltages within which the board is functional. The AM4904 is not guaranteed to function if the board is not operated within the operating range.

Table 5-1: DC Operational Input Voltage Ranges

Input Supply Voltage	Absolute Range (according AMC.0)	Operating Range (backplane requirements)
Payload Power (nominal: 12V DC)	10.0 V min. to 14 V max.	10.8 V min. to 13.2 V max.
Module Management Power (nominal: 3.3V DC)	3.0 V min. to 3.6 V max.	3.135 V min. to 3.465 V max.

WARNING

The AM4904 must not be operated beyond the absolute range indicated in the table above. Failure to comply with the above may result in damage to the board.

5.2 Carrier Power Requirements

5.2.1 Payload Power

Payload power is the power provided to the module from the backplane for the main function of the module.

It is recommended that Payload Power voltage provided by the system is at the higher end of the specified voltage range under no load conditions so that under high load conditions the current will be as low as possible.

The payload power voltage shall be at least 10.8 V and not more than 13.8 V at the module contacts during normal conditions under all loads (see “DC Operational Input Voltage Ranges” on page 91).

The bandwidth-limited periodic noise due to switching power supplies or any other source shall not exceed 200 mV peak to peak.

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5.2.2 Management Power

The AM4904 management power is used for IPMB interfaces and Module operation state control (PWR_ON#) and display (BLUE LED).

The management power voltage shall be 3.3 V ± 5% at the module contacts during normal conditions under all loads (see “DC Operational Input Voltage Ranges” on page 91)

5.2.3 Payload and Management Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the AM4904:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band. The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.3 Power Consumption

5.3.1 Payload Power Consumption

The payload power consumption table below lists the typical and maximum payload power consumption for the AM4904 variants. All measurements were conducted at a temperature of 25°C with a payload power of 12 V.

Table 5-2: Payload Power Consumption

Board type	typical	max
AM4904-BASE	22.0 W	26.0 W
AM4904-sRIO	31.0 W	35.0 W
AM4904-PCIe	34.0 W	40.0W



Note...

The power consumption values indicated can vary depending on the ambient temperature. This can result in deviations of the power consumption values of up to 10%.

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5.3.2 Management Power Consumption

The maximum current is below 100mA. Management Power is 330 mW max.

5.4 Payload Start-Up Current of the AM4904

The payload start-up current of the AM4904 during the first 2-3 seconds after the payload power has been applied is 1.8 A.

For further information on the start-up current, please contact Kontron.

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Chapter 6

Thermal Considerations

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6 Thermal Considerations

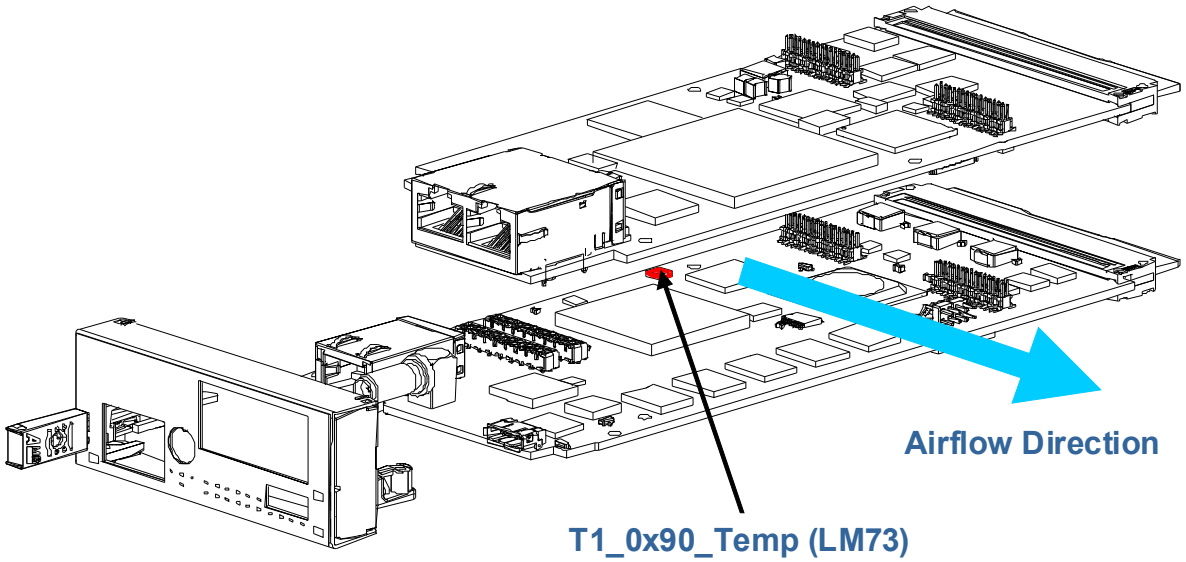
The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing AM4904 applications.

6.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AM4904, all onboard components must remain within the maximum temperature specifications. The DC converters on the AM4904 have internal temperature sensors. One additional sensor in an LM73 device keeps track of the inlet temperature.

Operating the AM4904 above the maximum operating limits may result in permanent damage to the board. To ensure functionality at the maximum temperature, the MCMC supports temperature monitoring features. Although temperature sensing information is made available to the MCMC, the AM4904 itself does not provide any active means of temperature regulation.

Figure 6-1: Temperature Sensor Locations AM4904 (Base variant, top view)



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Figure 6-2: Temperature Sensor Locations AM4904 (Base variant, bottom view)

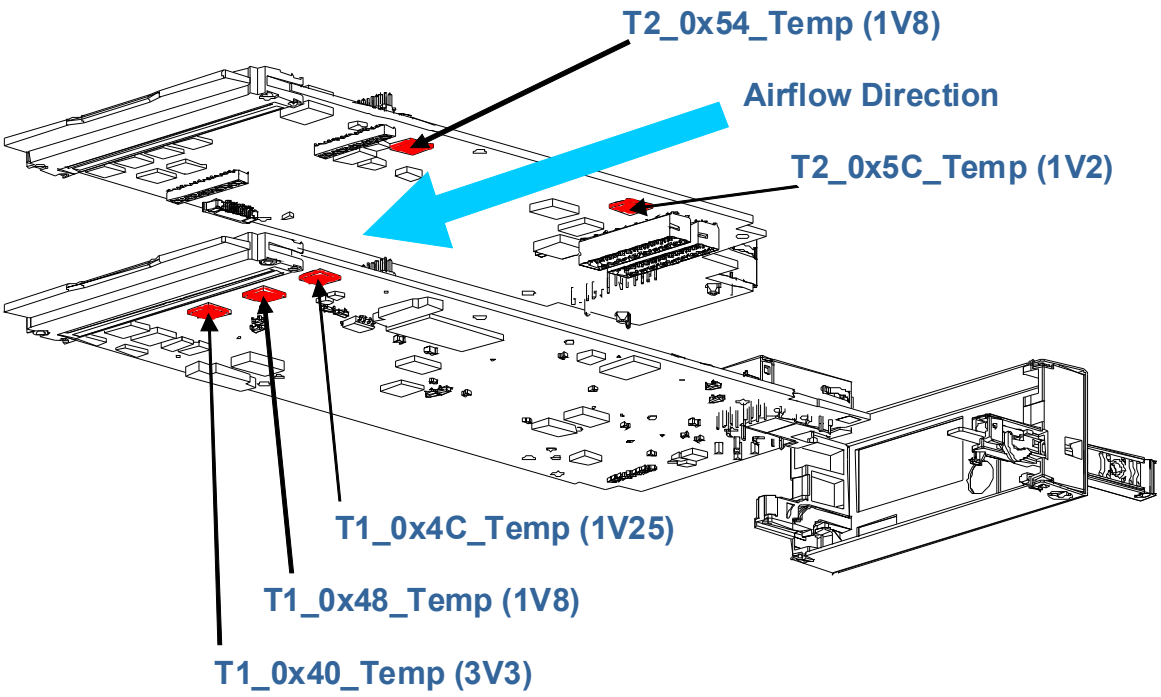
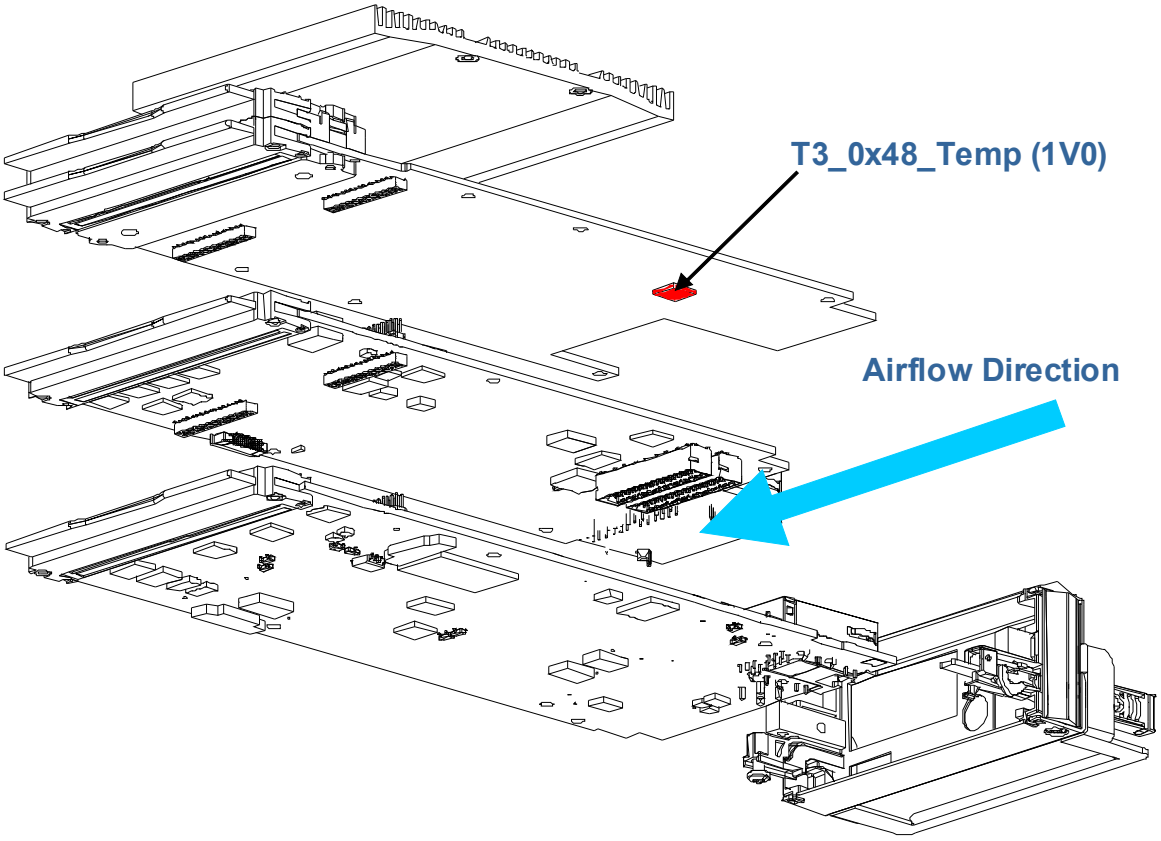
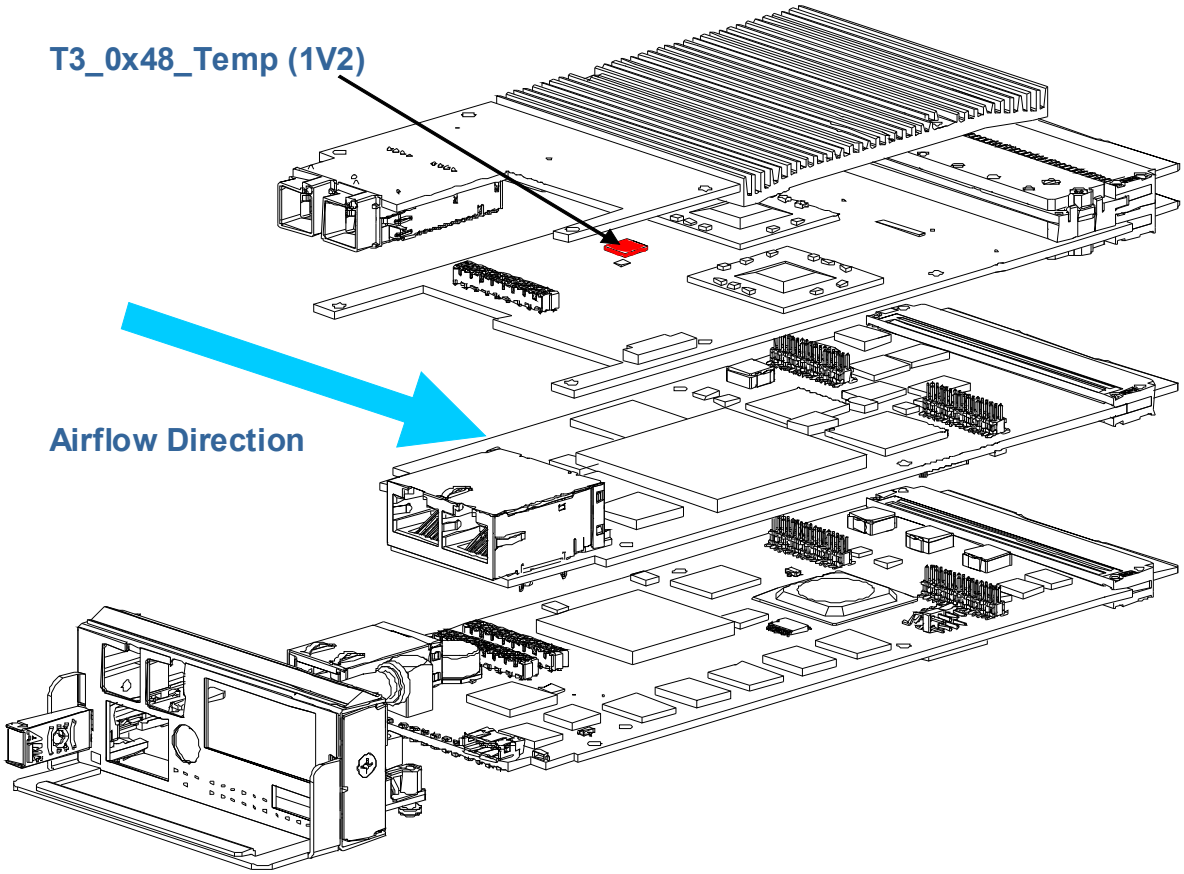


Figure 6-3: Temperature Sensor Locations AM4904 (PCIe variant, bottom view)



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Figure 6-4: Temperature Sensor Locations AM4904 (sRIO variant, top view)



The following table shows the temperature thresholds of all three sensors. Note that only upper thresholds are defined.Temperature values are measured with an accuracy of +/-3°C if not stated otherwise.

Table 6-1: MCMC Temperature Sensors Thresholds

Sensor	Device	Upper Non Critical	Upper Critical	Upper Non Recoverable	Comment
T1_0x90_Temp	LM73	45	60	70	PCB sensor +/-2 °C accuracy
T1_0x40_Temp	3V3	115	125	135	
T1_0x48_Temp	1V8	115	125	135	
T1_0x4C_Temp	1V25	115	125	135	
T2_0x54_Temp	1V8	115	125	135	
T2_0x5C_Temp	1V2	115	125	135	
T3_0x48_Temp	1V0	115	125	135	AM4904 PCIe only
T3_0x48_Temp	1V2	115	125	135	AM4904 sRIO only

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6.2 Thermal Regulation

When developing applications using the AM4904, the system integrator must be aware of the overall system thermal requirements. A system chassis must be provided which satisfy these requirements.

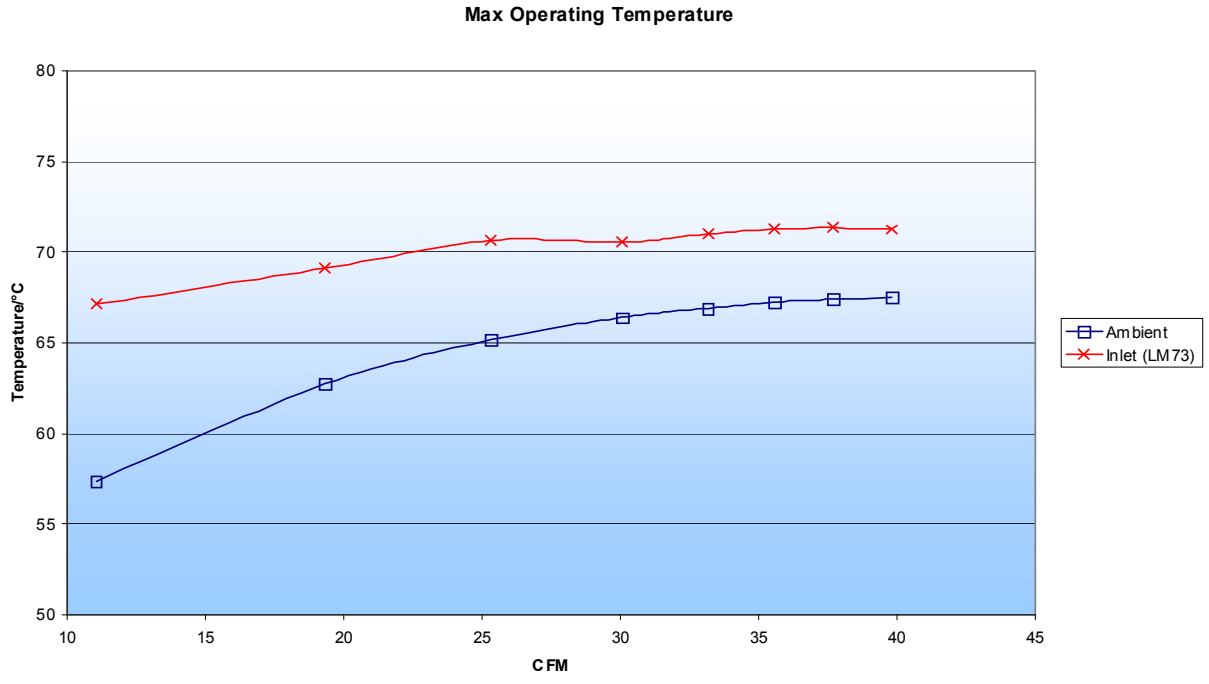
Measurements proofed that operation in worst case conditions (maximum ambient temperature of 55°C under maximum load) is possible while all temperatures of on-board components stay below their critical thresholds.

WARNING

As Kontron assumes no responsibility for any damage to the AM4904 or other equipment resulting from overheating any of the components, it is highly recommended that system integrators as well as end users confirm that the operational environment of the AM4904 complies with the thermal considerations set forth in this document.

The following diagram shows the maximum allowed ambient and inlet temperature (as measured by the T1_0x90_Temp LM73 sensor) in dependency of the airflow. The values are based on actual measurements and are subject to certain inaccuracies which is reflected in the slightly irregular shape of the graph.

Figure 6-5: Maximum ambient and inlet temperature versus airflow



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6.3 Airflow

In order to allow system integrators to optimize environmental conditions for the AM4904, airflow measurements according to CP-TA Interoperability Compliance Document (AdvancedTCA Book 1.1) were performed.

For each AM4904 variant, the pressure drop between inlet and outlet was measured (upper graph). The red curve represents an AMC reference board as defined by the CP-TA.

Figure 6-6: Impedance Curve AM4904-Base

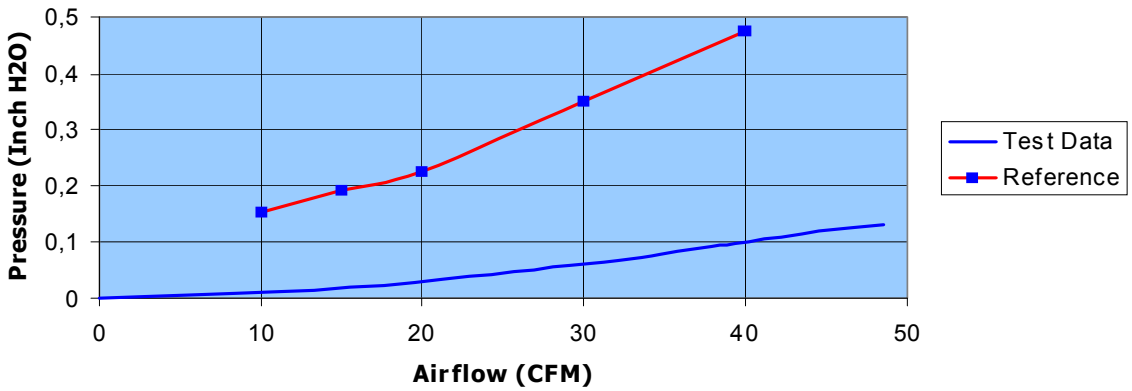
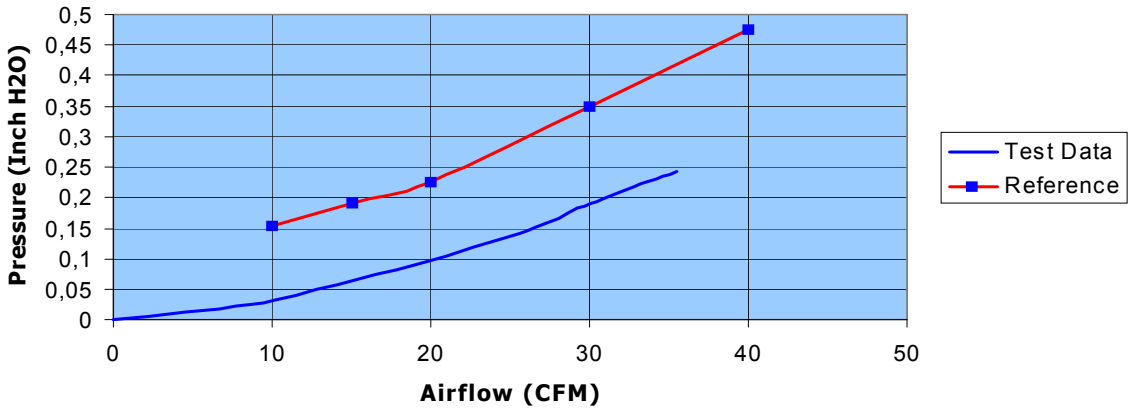
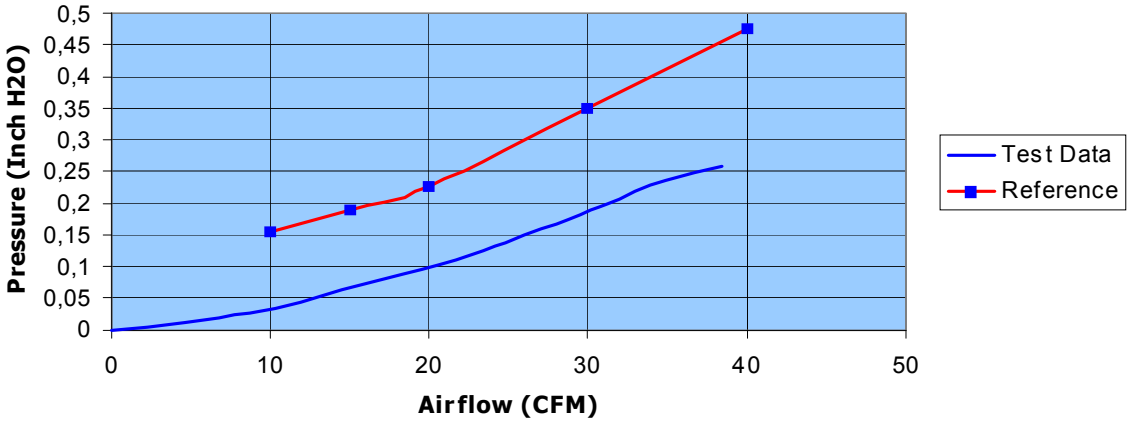


Figure 6-7: Impedance Curve AM4904-PCIe



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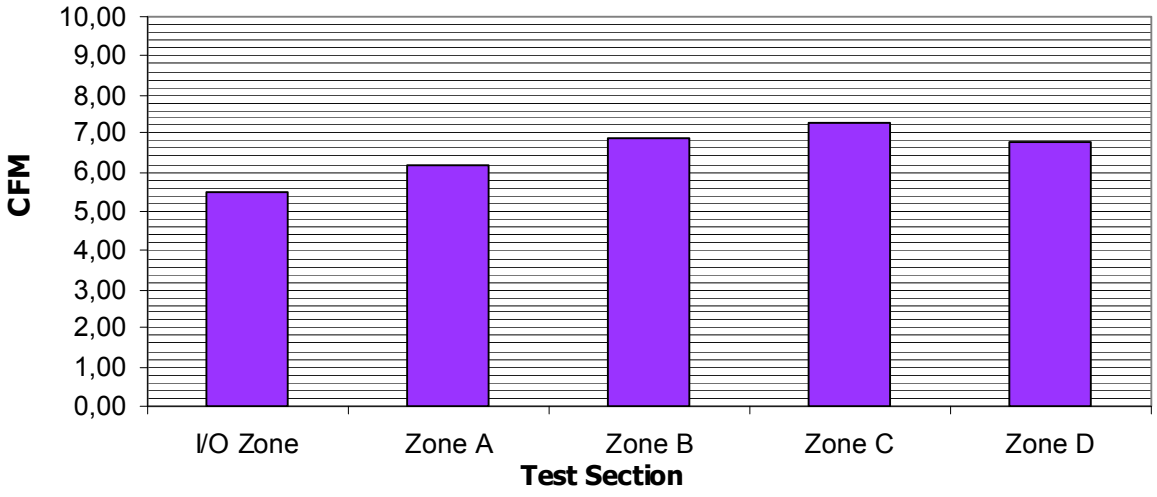
Figure 6-8: Impedance Curve AM4904-sRIO



The area between the front panel and the MCH backplane connector is divided into five zones, one I/O zone and four uniform thermal zones, A, B, C, and D. The PICMG AMC.0 Specification states that the uniformity of the airflow paths' resistance should provide an impedance on the A, B, C, and D zones that is within ± 25% of the average value of the four thermal zones.

The pressure drop between inlet and oulet was measured (upper graph). The red curve represents an AMC reference board as defined by the CP-TA.

Figure 6-9: Airflow Distribution AM4904-Base



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Figure 6-10: Airflow Distribution AM4904-PCIe

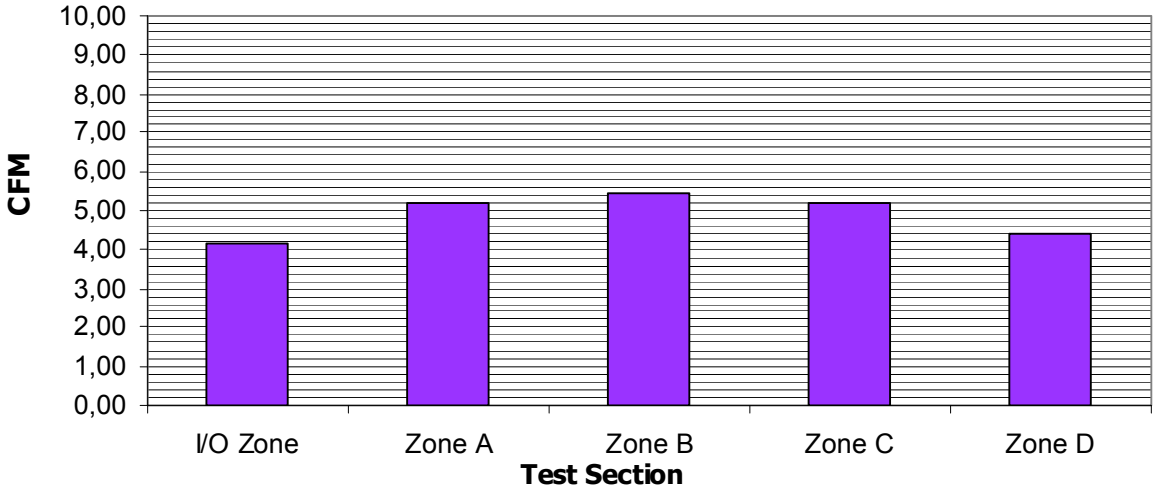
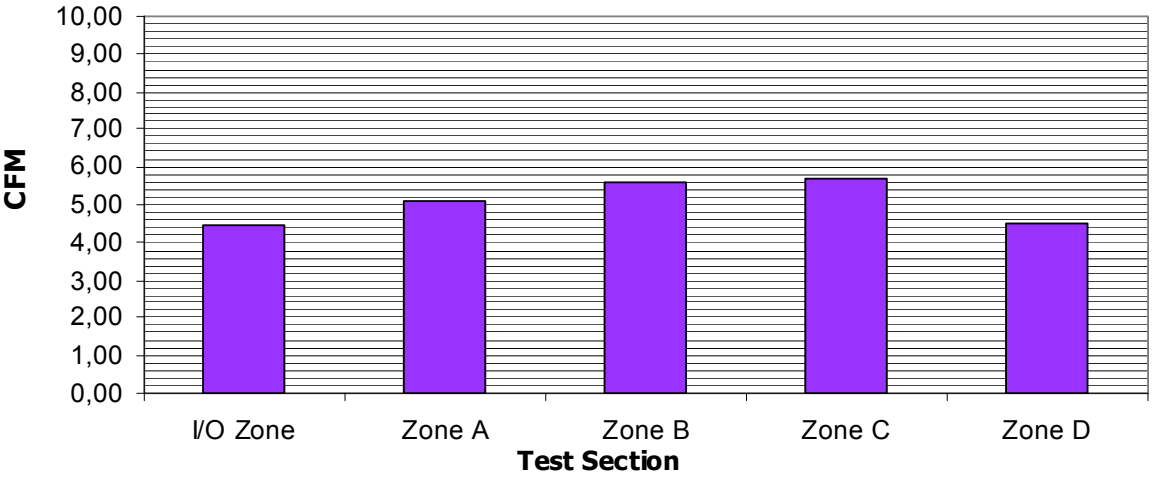


Figure 6-11: Airflow Distribution AM4904-sRIO



The airflow through the AM4904 is well balanced. The deviations of each zone's airflow from the mean value are within the required range.

Table 6-2: Airflow values

Variant	I/O Zone [cfm]	Zone A [cfm]	Zone B [cfm]	Zone C [cfm]	Zone D [cfm]	Mean (Zones A to D) [cfm]	Max Deviation [%]	Min Deviation [%]
Base	5.52	6.24	6.89	7.27	6.78	6.80	6.99	8.17
PCIe	4.16	5.23	5.45	5.22	4.42	5.08	7.28	12.99
sRIO	4.46	5.11	5.63	5.71	4.51	5.24	8.97	13.93

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Appendix A

CM Configuration Options

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A Configuration Options

The following list shows all possible configuration settings that can be used to change system behaviour. To change these, use the file /etc/cm.cfg.

The following list shows all available settings with a short explanation.

Table A-1: CM configuration file settings

Setting	Default	Description
auto_config_file.N auto_board_manufacturer.N auto_board_part_number.N auto_board_name.N auto_product_manufacturer.N auto_product_part_number.N auto_product_name.N	N/A	Load config file auto_config_file.N if any of the strings set in auto_board_X.N or auto_product_X.N matches the corresponding board info area or product info area field of the chassis backplane FRU data or if it is not set in the config file (i.e. “”) These settings can be used to create a number of auto configuration settings that are loaded for specific backplanes. Note that not all settings are valid when auto_config_file.N gets loaded, as basic initialisation has already been finished. But selecting chassis implementations (e.g. pm_om6060) and other settings are possible.
auto_detect_config	1	0=disable autodetection of configuration settings as defined by auto_config_file.N etc settings. 1=enable automatic loading of configuration files based on auto_config_file.N etc settings
bg_num_threads	4	Max. number of background threads for BG processing routines
cli_ro_users	“”	list of Unix users that can access only read-only CLI commands using clicm
cli_rw_users	root	list of Unix users that can access read-write commands using clicm
cm_activation_readiness	0	If set overrides the the activation readiness value found in carrier FRU data information
cm_enable_pcie_clock_when_pcie_present	1	1=enable PCI Express to slot when AMC that has PCI Express capability described in FRU data is enabled for payload power 0=CM does not manage PCI Express clock Note: This setting only works when MCH is also active carrier manager. For redundant configurations, PCI Express clocks should always be managed by AMC Clock E-Keying, which is not supported in SW version BETA 1.02 and earlier
cm_fake_quiesced.N	0	Do not wait for the module with FRU id N to send a quiesced event. Assumes that module is quiesced when the response to the FRUControl(Quiesce) command is received
cm_ignore_fru_merge_err.N	0	Ignore FRU merge errors during module activation for FRU id N
cm_ignore_handle.N	0	Used to force CM to ignore handle status from this module with FRU id N. Needed for example for power modules that have no handle sensor implemented or always report handle open.
cm_ignore_sens_merge_err.N	0	Ignore SDR merge errors during module activation for this FRU

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Table A-1: CM configuration file settings (Continued)

Setting	Default	Description
cm_inhibit_activation_by_cm.N	0	If set inhibits auto-activation by CM if configured in FRU data
cm_inhibit_deactivation_by_cm.N	0	If set inhibits auto-deactivation by CM if configured in FRU data
cm_override_pm_ready	0	If set consider pm module to be ready unconditionally, needed for unmanaged chassis
cm_ovr_slot_power.N	0	Override max. allowed power budget for FRU id N
cm_pcie_activate_rc_last	0	1=activate PCIE RC last in sequence, independent of back-plane activation sequence, 0=use standard activation sequence from backplane FRU data
cm_quiesce_timeout	0	Fake quiesced event after configured seconds
fake_fru_data_file.N		Override FRU FRU data for given FRU
fan_control	1	Enable intelligent cooling algorithm
fan_dec_timeout	120	Decrement fan level each fan_dec_timeout seconds if system is in normal cooling state
fan_dynamic_timeout	3600	Decrease dynamic fan level if fan level was stable on dynamic fan level for fan_dynamic_timeout seconds
fan_inc_timeout	60	Increment fan level each fan_inc_timeout seconds if minor temperature alert is raised
fan_initial_max_level	15	Try to set fan level to this level in case system is not yet fully discovered
fan_norm_level	5	Normal fan level
fan_stepdown	1	Step-down interval the system is in normal cooling state
fan_stepup	1	Step-up interval if minor temperature alert is raised
fcli_unix_socket	/tmp/cmcli.socket	File name for the FCLI socket
fru_backplane_eeprom_access_retry	5	Number of retries for backplane EEPROM access
fru_backplane_eeprom_page_size	32	Page size of backplane EEPROM
fru_logical_carrier_size	0	Specifies the size of logical Carrier FRU information partition (FRU-ID 253). 0 = determine size form partition tableX = size of partition in bytes
i2c_bus_stuck_grace_period	3	Number of seconds to wait between successive I2C bus resets
i2c_enable_bp_pullup	1	Enable I2C pullup as active MCH
i2c_tp_enable.N	0	Enable tracepoint generation for I2C controller N
ipmb_allow_bridging_on_same_if	0	1 = allow IPMI SendMsg command to bridge between IPMB-L interfaces, 0 = reject such messages (normal behavior)
ipmb_i2c_reset_on_m7	1	1 = Reset I2C controller for IPMB-L as if bus stuck was detected, in case a COMM_LOST indication is detected. This setting does not apply to IPMB-0. This may help in recovering from more I2C errors, especially a hung local controller. 0 = do nothing
ipmi_c1_retries	5	Retries for ipmi c1 condition

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Table A-1: CM configuration file settings (Continued)

Setting	Default	Description
ipmi_disable_rr	0	Disable round robin scheduling of requests on IPMB-0 (to PM, OEM, CU, FAN modules)
ipmi_t6_timeout_ms	220	Timeout for ipmi t6 period
local_sensor_loop_time	10	Refresh all local sensors every configured seconds
max_local_sensor_valid_time	20	Timeout for sensor valid flag in seconds
mcmc_fru_data_file	/etc/fru-data-mcmc.bin	Data file for MCMC FRU data
mcmc_fru_data_size	8192	MCMC FRU data size
nios_lm73_test	0	NIOS LM73 test routine
nios_loopback_bi_test	0	NIOS bi-directional loopback test routine
nios_loopback_test	0	NIOS loopback test routine
nios_loopback_test_c1	0	NIOS loopback test routine
nios_loopback_test_c2	0	NIOS loopback test routine
nios_par_memory_test	0	NIOS parallel memory test routine
nvctable_save_file	/etc/nvctable.save	Data file for non-volatile data storage
om6060_mp_dis_3v_ctrl	N/A	register value to write to TPS2359 when disabling 3A/3B channel in OM6060
om6060_mp_en_3v_ctrl	N/A	register value to write to TPS2359 when enabling 3A/3B channel in OM6060
om6060_pp_dis_12v_ctrl	N/A	register value to write to TPS2359 when disabling 12A/12B channel in OM6060
om6060_pp_en_12v_ctrl	N/A	register value to write to TPS2359 when enabling 12A/12B channel in OM6060
pcie_activate	0	0 = do not take S1301 / T3 out of reset if present, 1 = do assume S1301 is installed, take S1301 / T3 out of reset and execute init sequence
pcie_always_reset	0	1 = always reset PCIE switch when MCMC/CM starts, 0 = skip PCIE initialization if PCIE is not in reset, 2=reset PCIe switch if root complex setting pcie_rc_site, pcie_i2c_config_enable or SSC setting changed
pcie_i2c_config_enable	0	0=normal initialization sequence for PLX 1=initial configuration through I2C. PLX will not start automatically, but will wait for configuration release through register 0x3AC. See PLX datasheet for details.
pcie_init_early.N	n/a	PCIE initialization sequence executed before T3 is taken out of reset. There are a number of I2C initialization sequences executed during startup and before the PCIE T3 is taken out of reset. srio_init_early.N contains CLI commands to be executed during initialization. This can be mainly the I2C commands.

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Table A-1: CM configuration file settings (Continued)

Setting	Default	Description
pcie_init_late.N	n/a	PCIE initialization sequence executed after T3 is taken out of reset. There are a number of I2C initialization sequences executed during startup and after the PCIE T3 is taken out of reset. pcie_init_late.N contains CLI commands to be executed during initialization. This can be mainly the I2C commands.
pcie_link_mode.N	0	Controls PCIe link state of Fabric DEFG Port ID N 0 = use ekeying to enable or disable link 1 = force link to be enabled 2 = force link to be disabled
pcie_rc_site	1	set PCIE root-complex to AMC site (1..12)
pcie_reset_delay_ms	200	Delay in ms after PCIE T3 tongue is taken out of reset.
pcie_ssc	0	1=Enable PCI Express clock SSC (spread spectrum) mode. This is a global setting. All PCI Express Clock outputs are SSC then. 0=Enable PCI Express clock Non-SSC (normal) mode
pm_fake_primary_pm	0	1 = fake a primary power module. Will make all AMC slots to be always present, enabled and power up. Useful for backplanes that do always power on all slots.
pm_heartbeat_interval	2000	PM heartbeat poll interval (msec)
pm_heartbeat_timeout	8500	PM heartbeart timeout (msec)
pm_ignore_ovr_from_pol	0	1=ignore maximum current override from power policy capability records 0=process maximum current override records
pm_no_redundant_pm	0	1=Do not configure redundant power channel 0=configured redundant power channel if available
pm_om6060	0	Activate backplane integrated power subsystem module in IPMI_PM
pm_override_hb_mc_info_alt	0	1=use BMC info command instead of PM heartbeat message for PM detection 0=use uTCA compliant PM heartbeats for PM detection
pm_override_max_current	0	0=take PM maximum current from PM N=override maximum current output for PM to N 1/10 A
pm_override_max_current	0	0=take maximum power output from power module capability record, N=set maximum power output to N 1/10 A for primary power module site. Only for use in specific systems. Do not use with pluggable power modules.
pm_override_pm_site_id_bitmask	0	Used to force power module sites to be pinged even when there is no activation record found in the backplane FRU data. Can be used to force use of a PM in cases where the backplane FRU data is incorrect. Example: for some OM6040, use this with value 1
pm_poll_interval	4000	Interval in milliseconds for power module background polling of specific power subsystem, for example OM6060. For standard system, interval at which power channel status indications are requested from PM. Set to 0 to disable PM polling mode.

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Table A-1: CM configuration file settings (Continued)

Setting	Default	Description
pm_redundant_pm_site_id		0=take redundant PM site from backplane FRU data N=assume site N is redundant PM site (1..4)
power_channel_primary_site_override	0	0=take primary PM site from backplane FRU data N=assume site N is primary PM site (1..4)
power_channel_redundant_site_override.N	0	0=automatic redundant PM selection X=assume PM site X (1..4) as redundant PM for power channel N (1..16)
rm_delay_startup_slot1_ms	0	Timeout to delay role determination during startup for MCH in slot 1 (default active MCH)
rm_delay_startup_slot2_ms	3500	Timeout to delay role determination during startup for MCH in slot 2 (default backup MCH)
rm_force_active	0	Forces MCH to become active MCH, even when role determination will tell otherwise. Should be used with extreme care, as two active MCHs may render a system unusable. Also tells MCH to ignore all backplane FRU data and GA address decoder errors. Redundancy management will be turned off, so XOVER is not enabled and no master advertisement requests are sent. 1=force active 2=force inactive 0=automatic role determination
rm_ignore_invalid_bp	0	Used to force startup of CM/MCMC in case of invalid backplane FRU data. 0=do not start when backplane FRU data is invalid. 1=do start with default values when backplane FRU data is invalid.
rm_ignore_invalid_carrier_number	0	1 = Ignore invalid carrier number in backplane FRU data and backplane Carrier Number device 0=normal operation, do not start CM when carrier number is invalid
rm_ignore_invalid_ga	0	1 = Ignore invalid geographical address 0=normal operation, do not start CM when carrier number is invalid
rm_inhibit_cm_startup	0	Do not start carrier manager function
rm_master_rate_ms	1000	Send master advertisement every interval milliseconds
rm_master_timeout_ms	2600	After this timeout period, the backup will declare the master IPMB heartbeat from the active mch failed if it is enabled
rm_watchdog_fastpath_delay	30	Initial number of seconds to wait before sending first ping to FASTPATH
rm_watchdog_fastpath_secs	2	Heartbeat interval for pinging FASTPATH. Every 5 seconds a ping is sent to FASTPATH by default. Set to 0 to disable ping/watchdog of FASTPATH. Note that if the watchdog is disabled globally, this option has no effect.
rm_watchdog_fastpath_timeout	4	Number of seconds to wait for answer from FASTPATH. When this time expires or ping is not answered, CM will stop updating the watchdog. This will eventually reset the board then.

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Table A-1: CM configuration file settings (Continued)

Setting	Default	Description
rm_watchdog_tick	500	Watchdog tick interval in ms. Note that this interval at which other timeouts are checked (rm_master_timeout_ms, rm_deviceid_timeout_ms, rm_xover_timeout_ms), thus it should be less than these.
rm_watchdog_timeout	5000	Watchdog timeout value in ms.
rm_xover_timeout_ms	2600	After this timeout period, the backup will declare the xover heartbeat to the active mch failed if it is enabled
rmcp_udp_port	623	UDP port number for RMCP
sel_reset_sel_pdata	0	0=normal operation, scan SEL on startup 1 = completely reset PDATA SEL flash storage to empty
srio_activate	0	0 = do not take S1302 / T3 out of reset if present, 1 = do assume s1302 is installed, take S1302 / T3 out of reset and execute init sequence
srio_always_reset	0	1 = always take SRIO into reset first, 0 = skip SRIO initialization if SRIO is not in reset
srio_init_early.N	n/a	SRIO initialization sequence executed before T3 is taken out of reset. There are a number of I2C initialization sequences executed during startup and before the SRIO T3 is taken out of reset. srio_init_early.N contains CLI commands to be executed during initialization. This can be mainly the I2C commands.
srio_init_late.N	n/a	SRIO initialization sequence executed after T3 is taken out of reset. There are a number of I2C initialization sequences executed during startup and after the SRIO T3 is taken out of reset. srio_init_late.N contains CLI commands to be executed during initialization. This can be mainly the I2C commands.
srio_link_mode.N	0	Controls SRIO link state of Fabric DEFG Port ID N 0 = use ekeying to enable or disable link 1 = force link to be enabled 2 = force link to be disabled
srio_reset_delay_ms	200	Delay in ms after SRIO T3 tongue is taken out of reset.
startup_active.N	n/a	Standard CLI initialization sequence executed when CM is starting as active carrier manager. startup_active.N contains CLI commands to be executed during initialization.
startup_inactive.N	n/a	Standard CLI initialization sequence executed when CM is starting as inactive/backup carrier manager. startup_inactive.N contains CLI commands to be executed during initialization.
om6060_slot_cnt	6	Limit number of supported slots for OM6060 compatible backplanes
fan_local		Enable support for a fan controller on the backplane. “MB04D-101” sets fan controller support for this backplane

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Appendix B

Getting Help

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B Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support-kom@kontron.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555 Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

B.1 Returning Defective Merchandise

Before returning any merchandise please do one of the following:

- Call
  - Call our Technical Support department in North America at (450) 437-5682 or in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order # and the Serial Number of the defective unit.
  - Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.
  - The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.
  - Make sure you receive an RMA # from our Technical Support before returning any merchandise.

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- Fax
  - Send us a fax at: North America (450) 437-0304, EMEA +49 (0) 8341 803 339. In the fax, you must include your name, your company name, your address, your city, your postal/zip code, your phone number and your e-mail. You must also include the serial number of the defective product and a description of the problem.

- E-mail
  - Send us an e-mail at: RMA@ca.kontron.com in North America or at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

B.2 When Returning a Unit

- In the box, you must include the name and telephone number of a person, in case further explanations are required. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

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Boisbriand, Québec	87600 Kaufbeuren
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Appendix C

Glossary

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C Glossary

Acronyms	Descriptions
AdvancedMC	(Same as AMC). Advanced Mezzanine Card.
AMC	(Same as AdvancedMC). Advanced Mezzanine Card.
AMC.0	Advanced Mezzanine Card Base Specification.
AMC.1	PCI Express and Advanced Switching on AdvancedMC. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.2	Ethernet Advanced Mezzanine Card Specification. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.3	Advanced Mezzanine Card Specification for Storage. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ARP	Address Resolution Protocol
ASCII	American Standard Code for Information Interchange. ASCII codes represent text in computers, communications equipment, and other devices that work with text.
BMC	Base Management Controller
CLI	Command-Line Interface
CLK1	AdvancedTCA bused resource Synch clock group 1
CLK1A	AdvancedTCA bused resource Synch clock group 1, bus A
CLK1B	AdvancedTCA bused resource Synch clock group 1, bus A
CLK2	AdvancedTCA bused resource Synch clock group 2
CLK2A	AdvancedTCA bused resource Synch clock group 2, bus A
CLK2B	AdvancedTCA bused resource Synch clock group 2, bus B
CLK3	AdvancedTCA bused resource Synch clock group 3
CLK3A	AdvancedTCA bused resource Synch clock group 3 , bus A
CLK3B	AdvancedTCA bused resource Synch clock group 3 , bus B
CPLD	Complex Programmable Logic Device
CTS	Clear To Send
DDR2	(Same as DDR-II). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DIMM	Dual In-line Memory Module
DIN	Deutsches Institut für Normung. German Institute for Standardization.
DMA	Direct Memory Access
DMI	Desktop Management Interface
DRAM	Dynamic Random Access Memory
DTC	Data Transfer Controller
DTR	Data Terminal Ready
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge

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Acronyms	Descriptions
ESI	Enterprise South bridge Interface. Interface to the I/O legacy bridge component of the Intel ICHx.
ETSI	European Telecommunications Standards Institute
FI	Fabric Interface. Backplane connectivity defined by the ATCA.
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit. Any entity that can be replaced by a user in the field. Not all FRUs are hot swappable
FTP	File Transfer Protocol
FW	FirmWare
GARP	Generic Attribute Registration Protocol
Gb	Gigabit
GB	(Same as GByte) GigaByte.
GByte	(Same as GB) GigaByte.
GbE	Gigabit Ethernet
GHz	GigaHertz
GND	GrouND
GPIO	General Purpose Input Output
I2C	Inter Integrated Circuit bus
IO	(Same as I/O). Input Output
IOL	IPMI-Over-LAN
IP	Internet Protocolww.kontron.com
IPM	Intelligent Platform Management
IPMB	Intelligent Platform Management Bus
IPMB-0	Intelligent Platform Management Bus Channel 0, the logical aggregation of IPMB-A and IPMB-B.
IPMB-A	Intelligent Platform Management Bus A
IPMB-B	Intelligent Platform Management Bus B
IPMB-L	Intelligent Platform Management Bus Local
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
IPMIFWU	Intelligent Platform Management Interface FirmWare Update
ISO	International Organization for Standardization
ITU	International Telecommunication Union
JTAG	Joint Test Action Group
KB	KiloByte
KHz	KiloHertz
LAN	Local Area Network
LED	Light-Emitting Diode
MAC	Media Access Controller address of a computer networking device.
MB	MegaByte
MC	Management Controller
MCH	Memory Controller Hub
MHz	MegaHertz

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Acronyms	Descriptions
MMC	Module Management Controller. MMCs are linked to the IPMC.
MMIO	Memory-Mapped IOw.kontron.com
MTBF	Mean Time Between Failures
NAND	Type of Flash Memory, used for mass storage.
OEM	Original Equipment Manufacturer
OOS	Out Of Service
OS	Operating System
OSI	Open Source Initiative
PCB	Printed Circuit Board
PCIe	(Same as PCI-E). PCI-Express. Next generation I/O standard
PCI-E	(Same as PCIe). PCI-Express. Next generation I/O standard.
PHY	PHYsical layer. Generic electronics term referring to a special electronic integrated circuit or functional block of a circuit that takes care of encoding and decoding between a pure digital domain (on-off) and a modulation in the analog domain.
PICMG	PCI Industrial Computer Manufacturers Group
PICMG®	PCI Industrial Computer Manufacturers Group
PLD	Programmable Logic Device
PLL	Phase Lock Loop
POR	Power-On Reset
POST	Power-On Self-Test
RAM	Random Access Memory
RoHS	Restriction of the Use of Certain Hazardous Substances
ROM	Read Only Memory. Also refers to option ROM or expansion ROM code used during POST to provide services for specific controllers, such as boot capabilities.
RS-232	(Same as RS232). Recommended Standard 232.
RS232	(Same as RS-232). Recommended Standard 232.
RTC	Real Time Clock
RTM	Rear Transition Module
RTS	Request To Send
SCL	Serial CLock
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SEEPROM	Serial EEPROM
SEL	System Event Log
SERDES	SERializer/DESerializer. Pair of functional blocks commonly used in high speed communications. These blocks convert data between serial data and parallel interfaces in each direction.
SSGMII	Serial Gigabit Media Independent Interface. Standard interface used to connect a Gigabit Ethernet MAC-block to a PHY.
ShMC	Shelf Management Controller
SMB	(Same as SMBus/SMBUS). System Management Bus.
SONET	Synchronous Optical NETworking
SPI	Serial Peripheral Interface

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Acronyms	Descriptions
SSH	Secure SHell. A network protocol that allows data to be exchanged over a secure channel between two computers.
TCLKA	Telecom CLocK A. AMC Clock Interface.
TCLKB	Telecom CLocK B. AMC Clock Interface.
TCLKC	Telecom CLocK C. AMC Clock Interface.
TCLKD	Telecom CLocK D. AMC Clock Interface.
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VLAN	Virtual Local Area Network
WD	WatchDog
WDT	WatchDog Timer
CAS	Serial Attached SCSI
CM	Carrier Manager
CPCI	CompactPCI
CPU	Central Processing Unit
CSV	Character Separated Values
DIP	Dual Inline Package
MCMC	MicroTCA Carrier Management Controller
MP	MultiProcessor
NVRAM	Non-Volatile Random Access Memory
PM	Power Management
RFC	Remote Function Call
RGMII	Reduced Gigabit Media Independent Interface
SAS	Serial Attached SCSI
SCSI	Small Computer System Interface
SNMP	Simple Network Management Protocol
SPD	Serial Presence Detect
sRIO	Serial RapidIO
SSGMII	Serial Gigabit Media Independent Interface. Standard interface used to connect a Gigabit Ethernet MAC-block to a PHY.
TMRCLK	Time Reference Clock
TSOP	Thin Small-Outline Package
UDP	User Datagram Protocol. An Internet Protocol

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